TIMING DIAGRAM

- Timing Diagram is a graphical representation.
- It represents the execution time taken by each instruction in a graphical format.
- The execution time is represented in T-states.

CONTROL SIGNALS

IO/M(Active Low)	S1	S2	Data Bus Status(Output)
0	0	0	Halt
0	0	1	Memory WRITE
0	1	0	Memory READ
1	0	1	IO WRITE
1	1	0	IO READ
0	1	1	Opcode fetch
1	1	1	Interrupt acknowledge

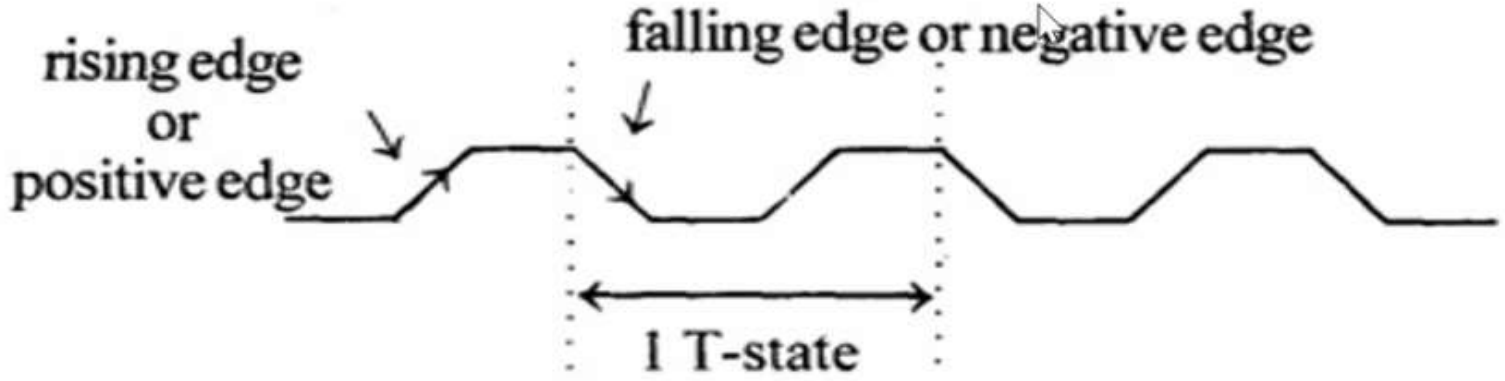
MACHINE CYCLE

- The time required to access the memory or input/output devices is called machine cycle.

T-STATE

- The machine cycle and instruction cycle takes multiple clock periods.
- A portion of an operation carried out in one system clock period is called as T-

Note : *Time period, $T = 1/f$; where f = Internal clock frequency*



MACHINE CYCLES OF 8085

The 8085 microprocessor has 5 basic machine cycles.

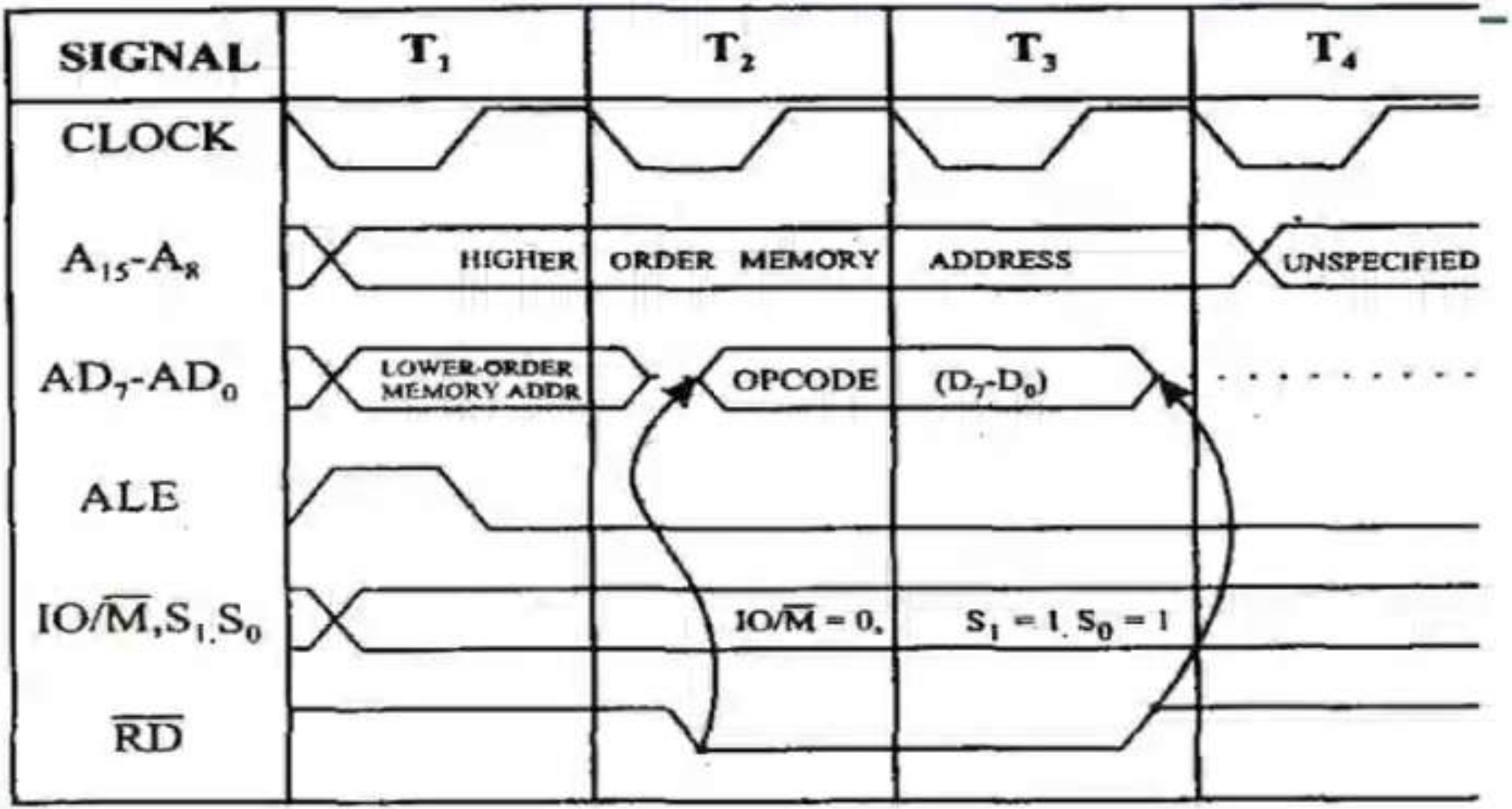
They are

1. Opcode fetch cycle (4T)
2. Memory read cycle (3 T)
3. Memory write cycle (3 T)
4. I/O read cycle (3 T)
5. I/O write cycle (3 T)

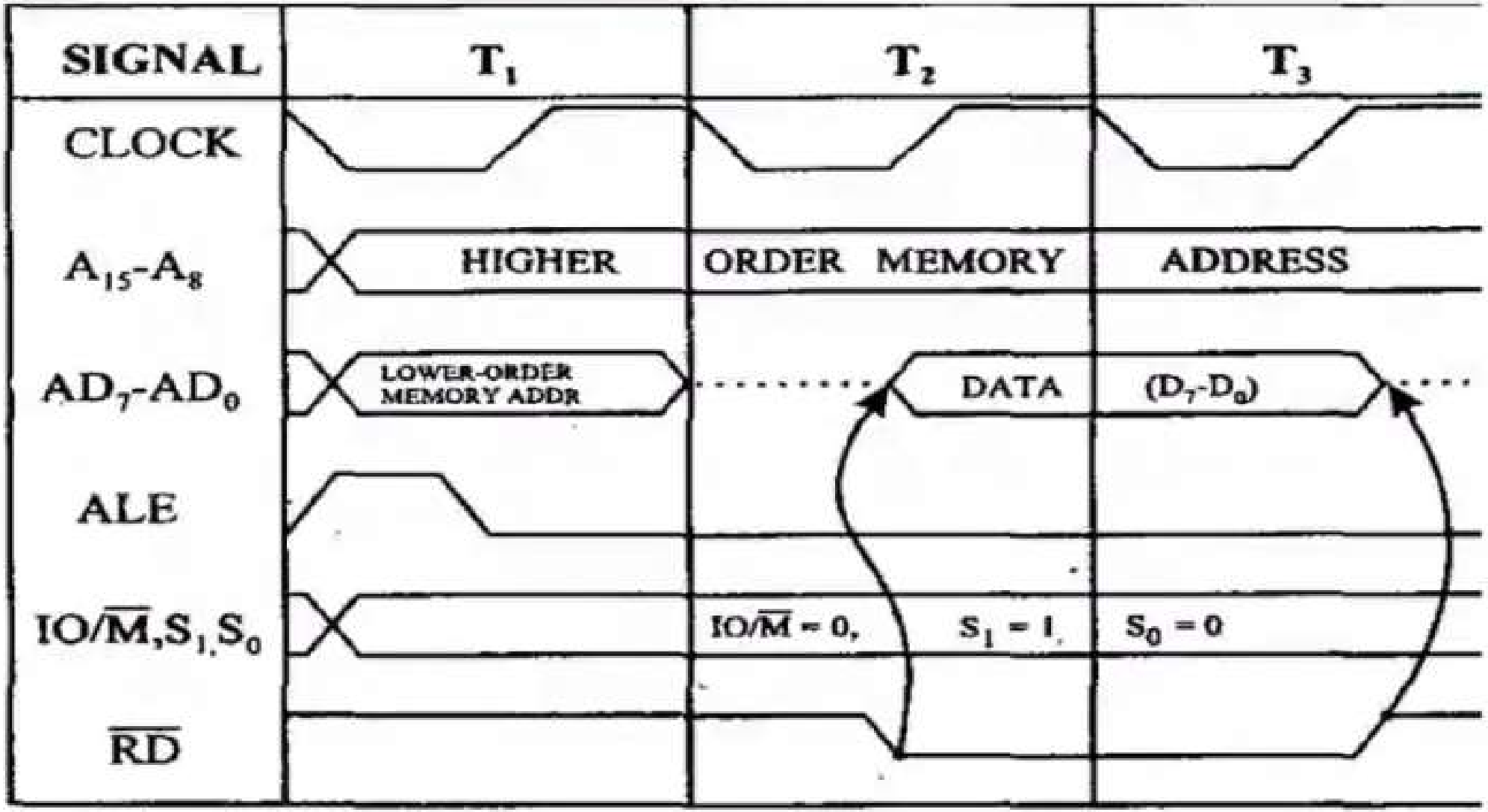
MACHINE CYCLES OF 8085

- The processor takes a definite time to execute the machine cycles. The time taken by the processor to execute a machine cycle is expressed in T-states.
- One T-state is equal to the time period of the internal clock signal of the processor.
- The T-state starts at the falling edge of a clock.

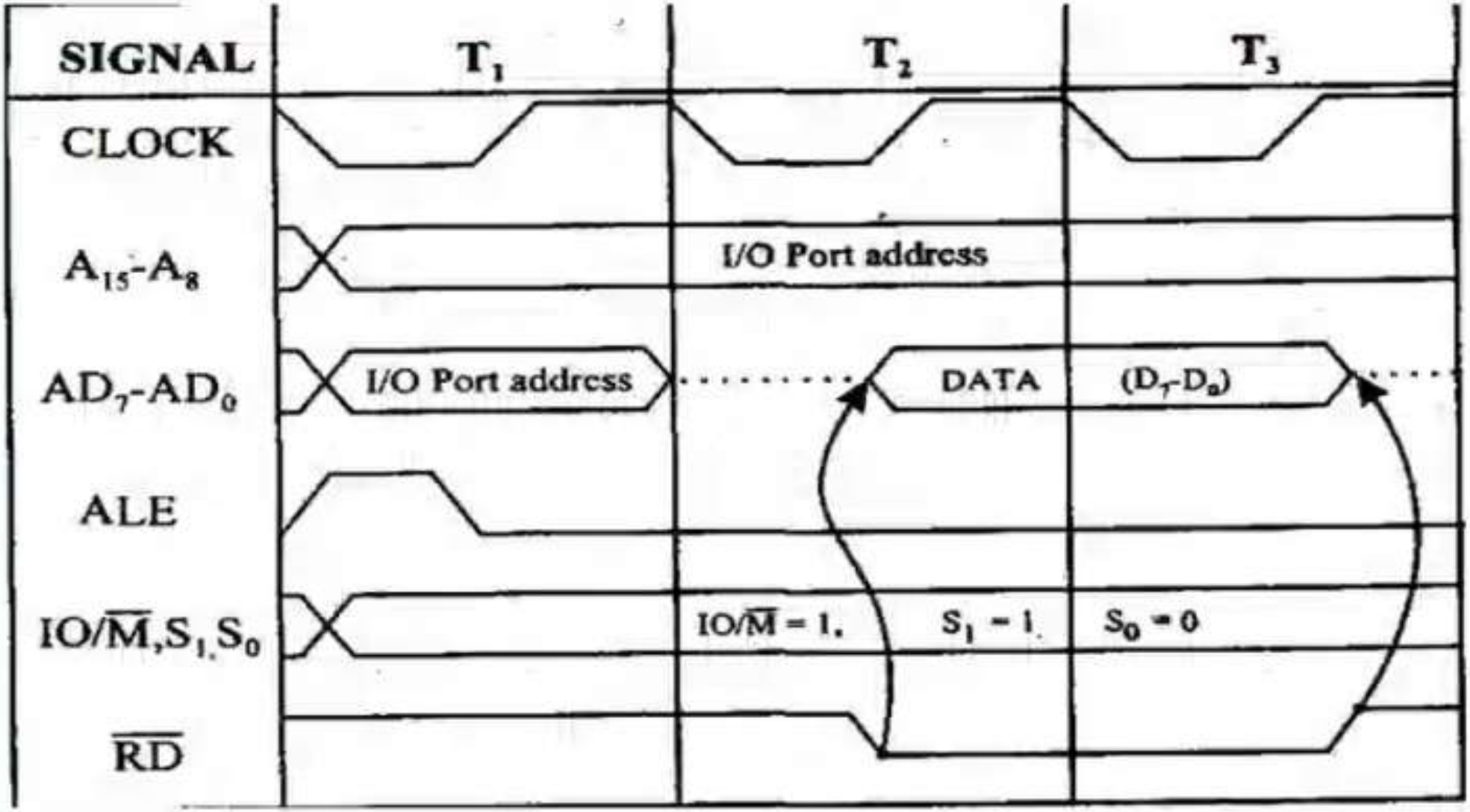
OPCODE FETCH MACHINE CYCLE OF 8085



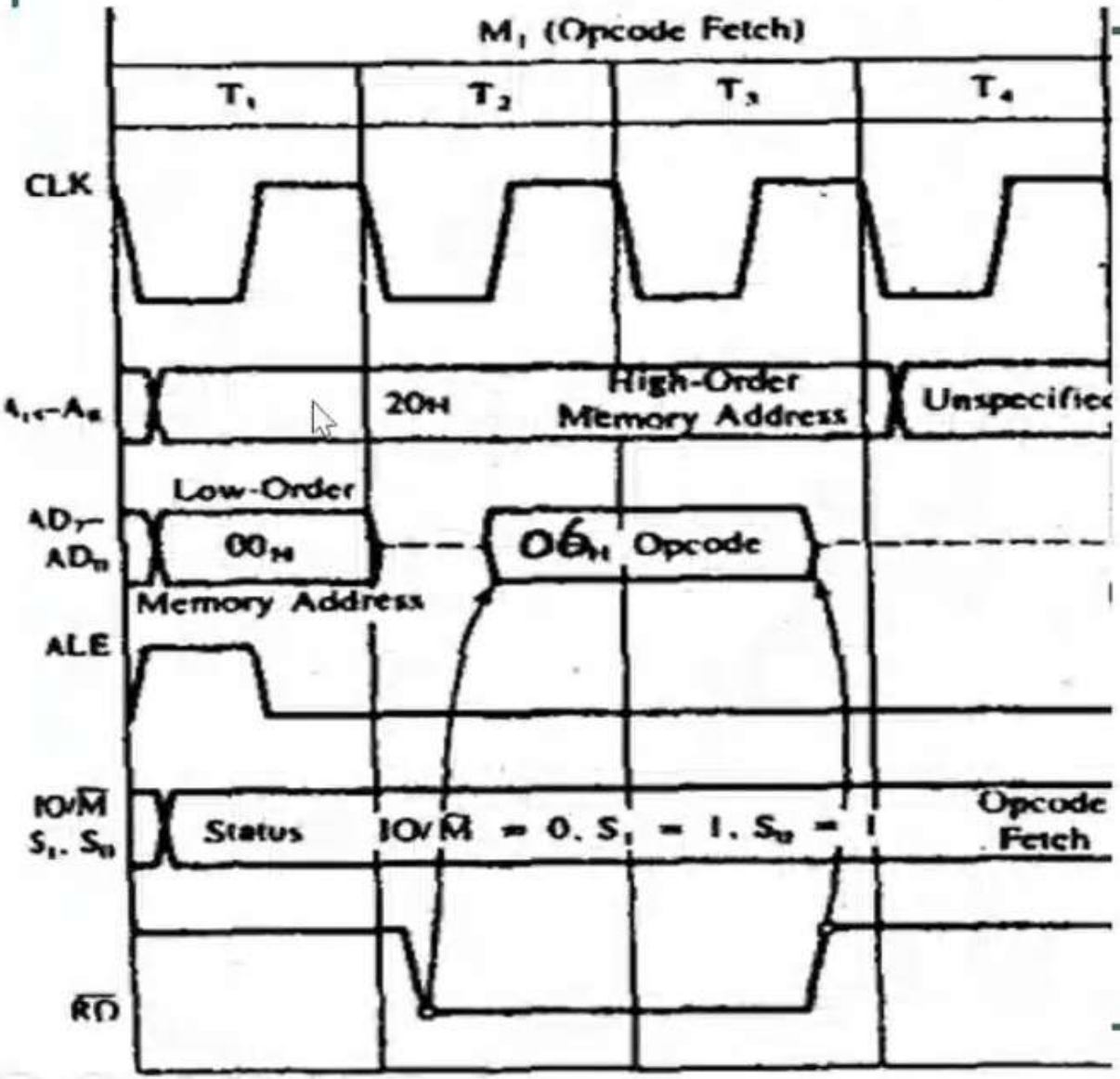
MEMORY READ MACHINE CYCLE OF 8085



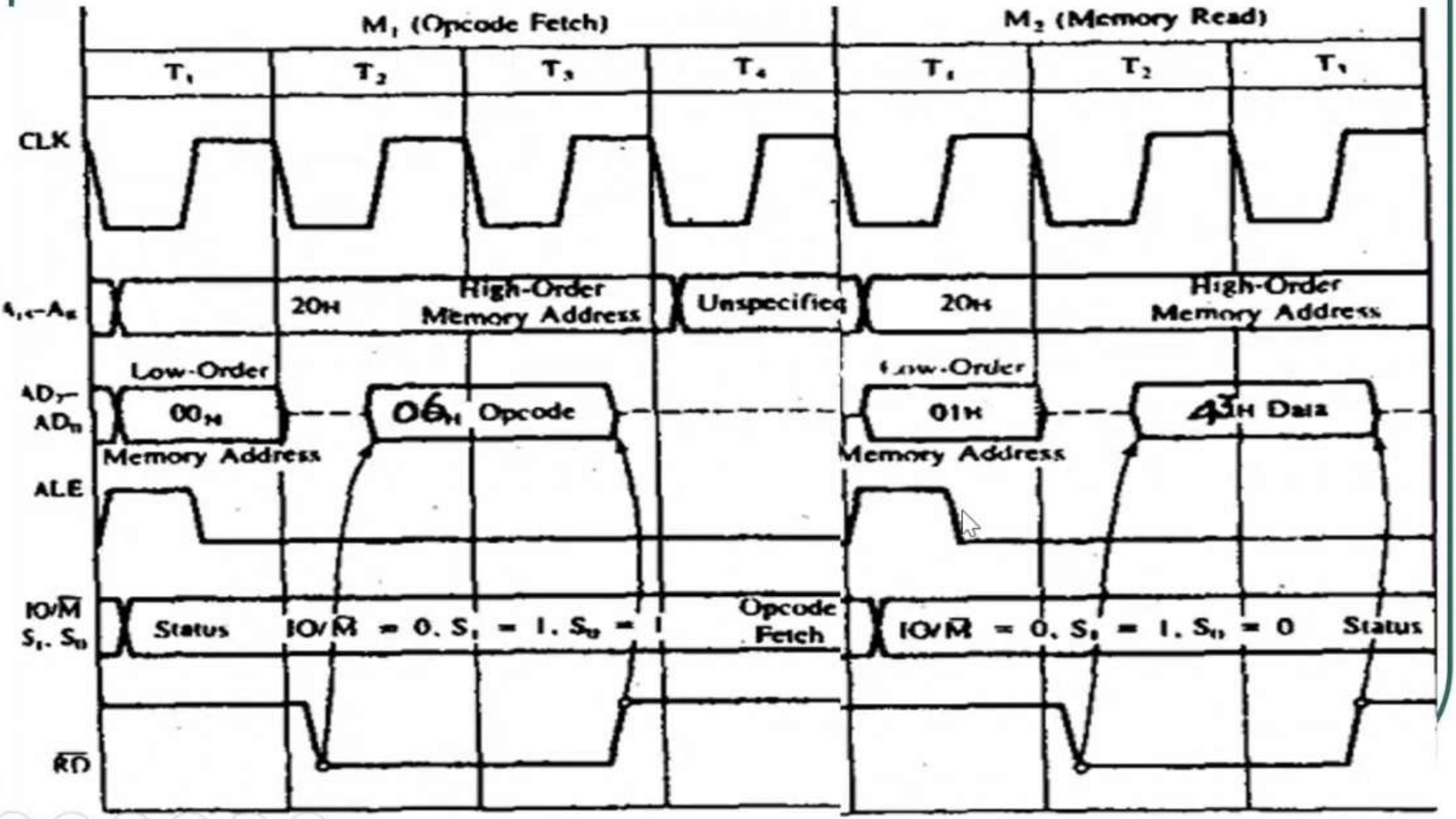
I/O READ CYCLE OF 8085



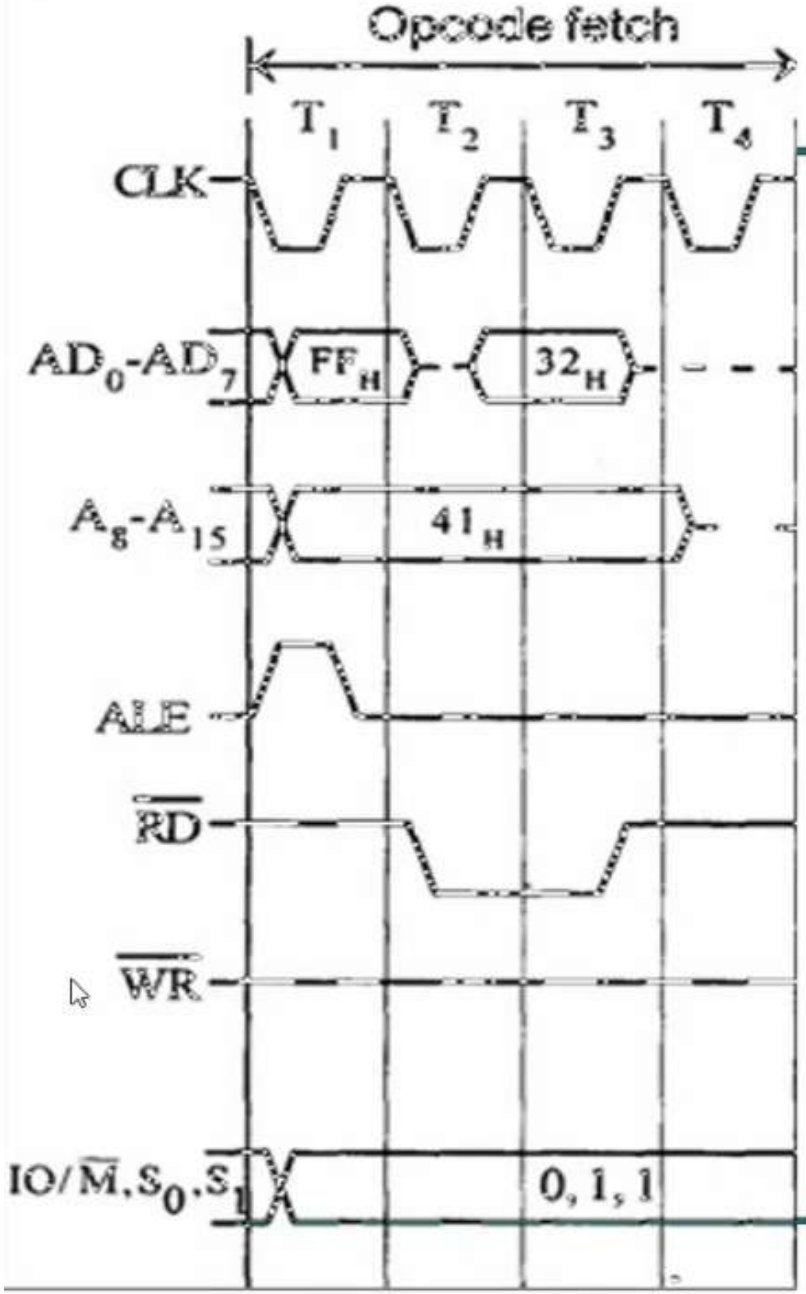
EXAMPLE INSTRUCTION : MVI B, 43



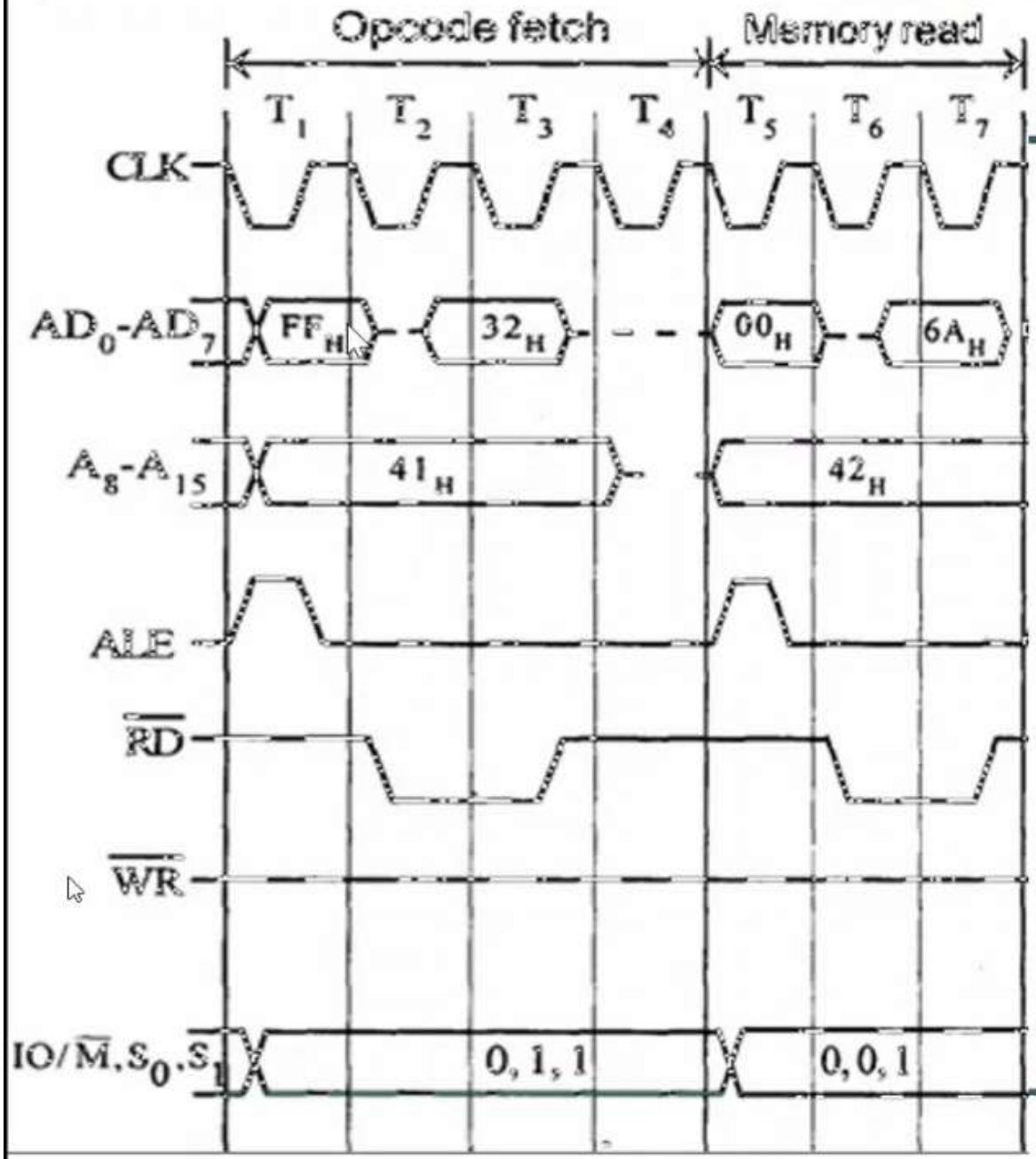
EXAMPLE INSTRUCTION : MVI B, 43



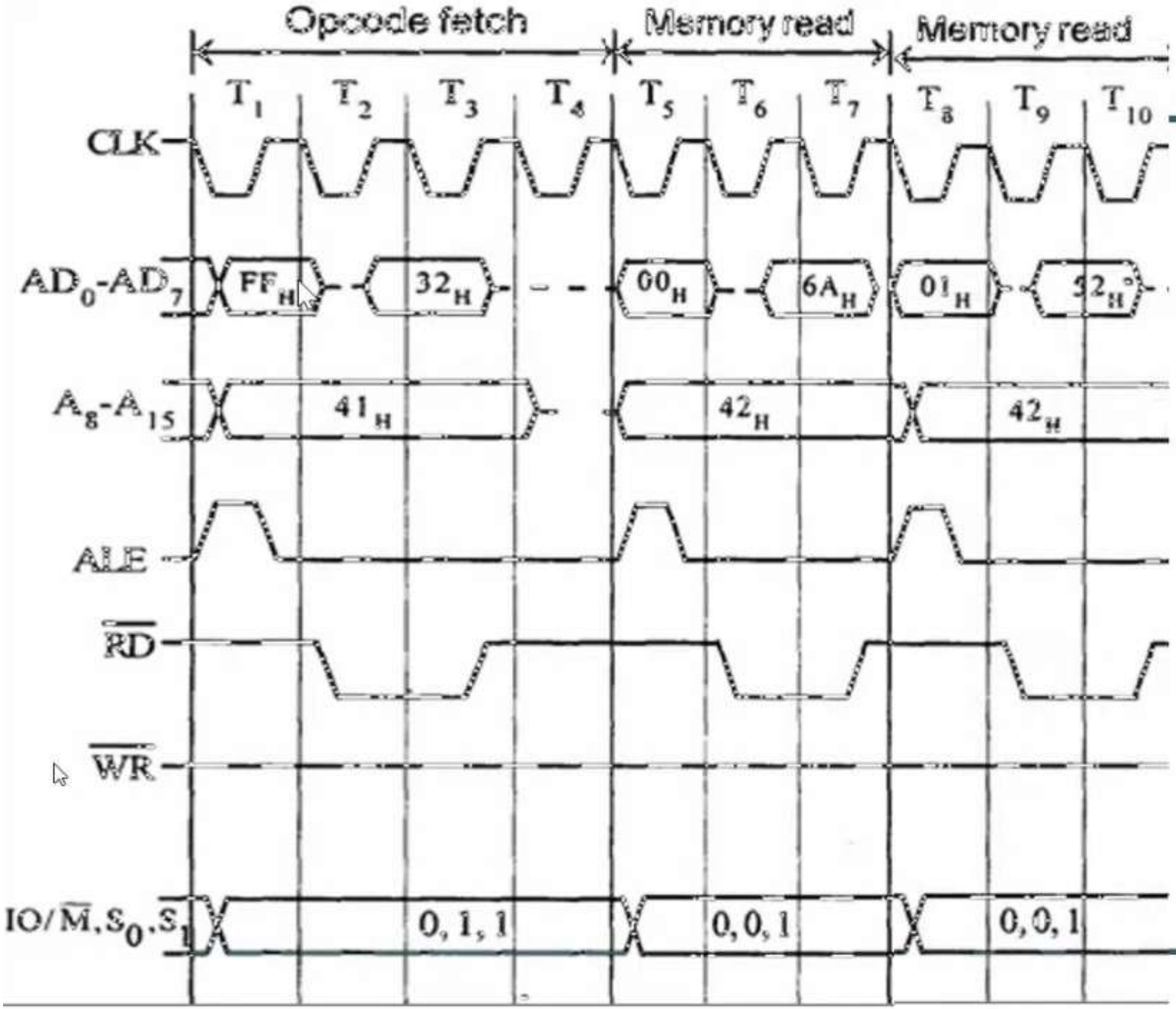
EXAMPLE INSTRUCTION : STA 526A



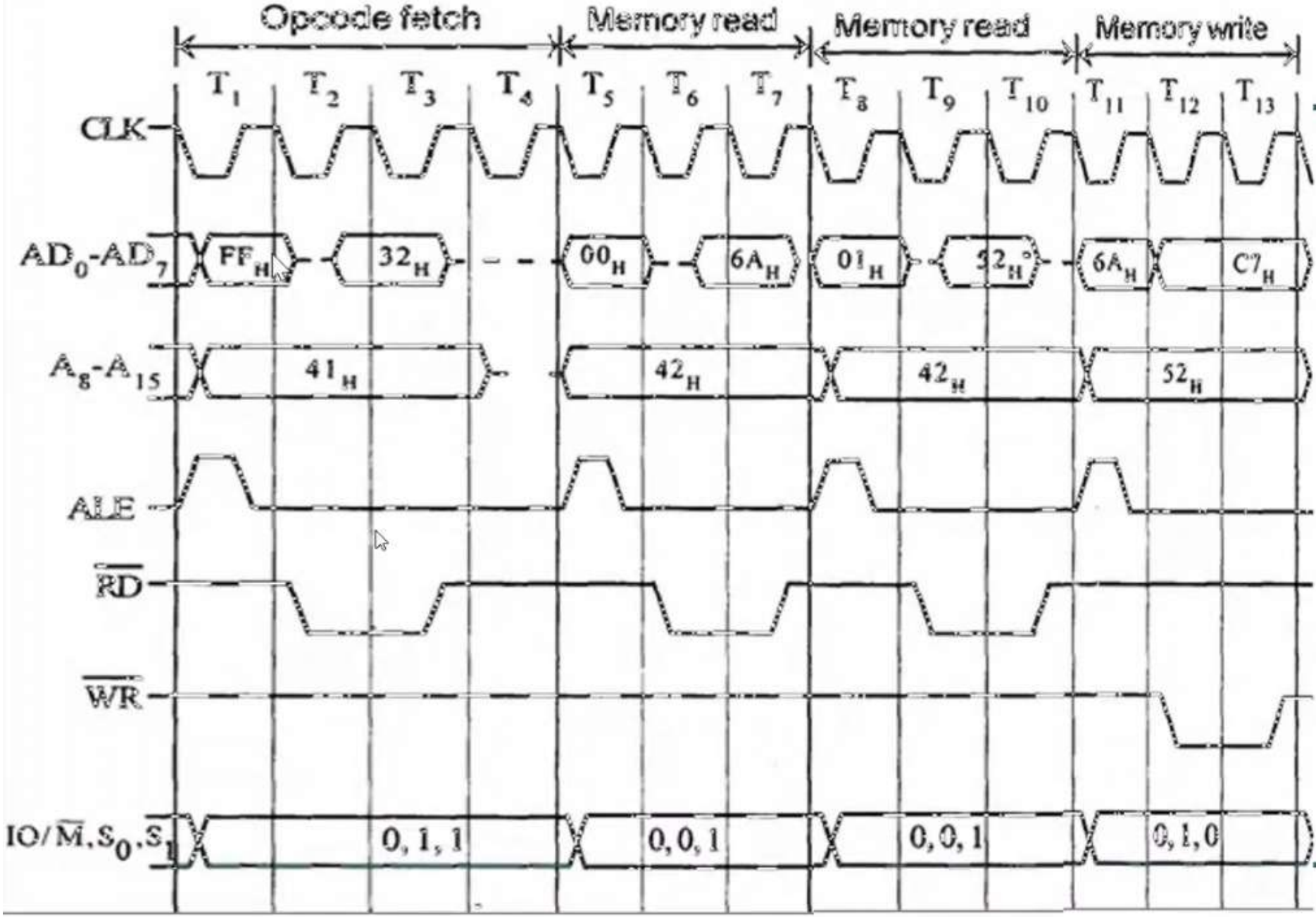
EXAMPLE INSTRUCTION : STA 526A



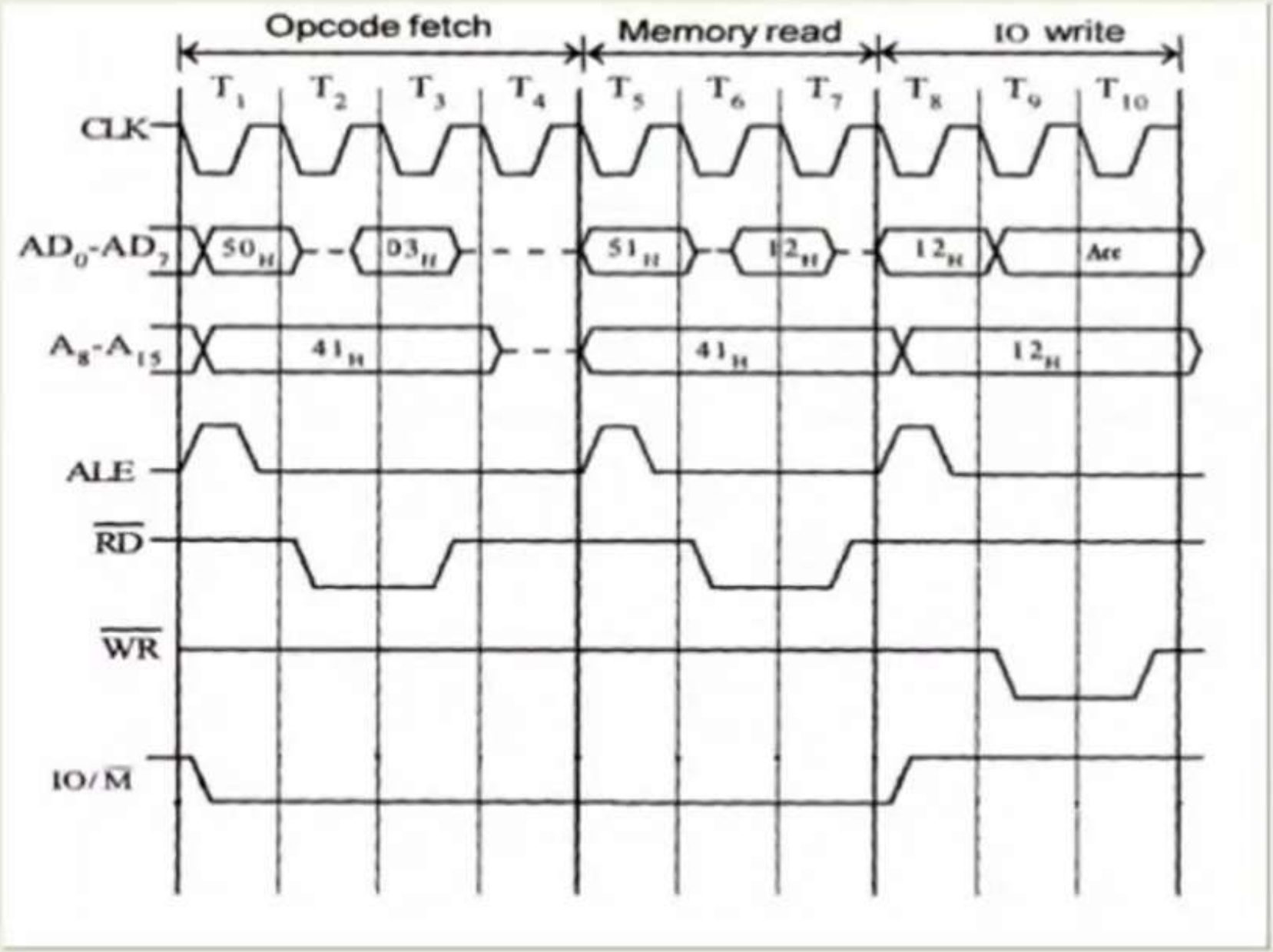
EXAMPLE INSTRUCTION : STA 526A



EXAMPLE INSTRUCTION : STA 526A



Timing Diagram of 'OUT' instruction



OUT 12H

Memory	Code
4150H	D3H
4151H	12H

IN TIMING DIAGRAM