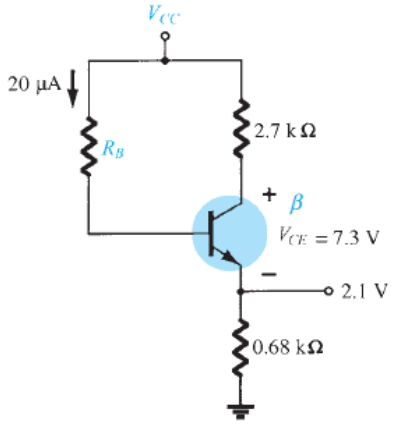
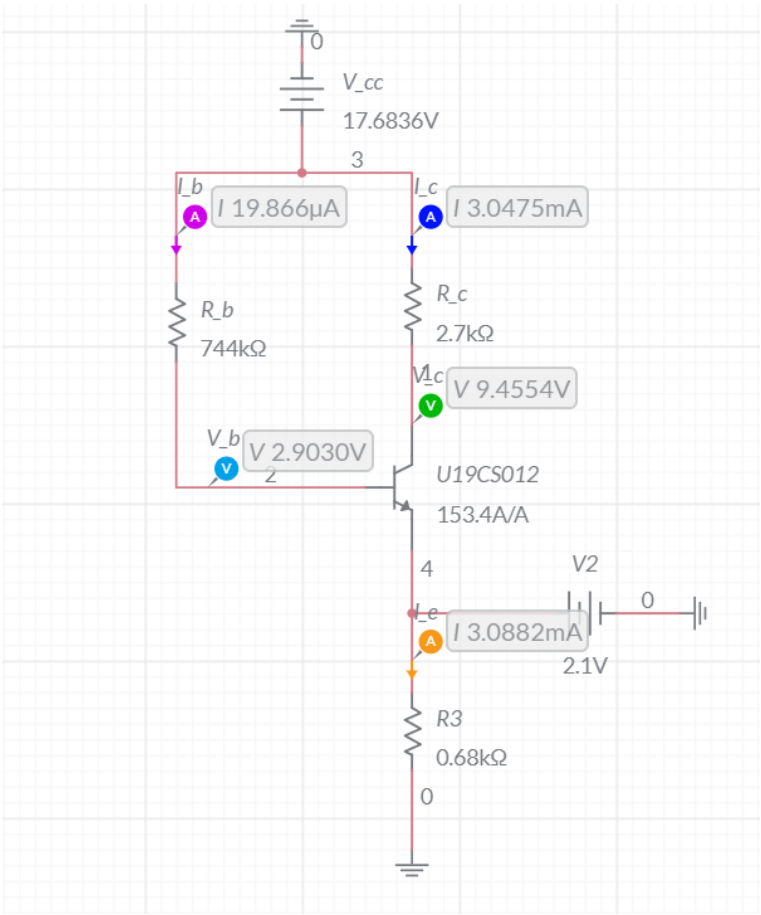
ASSIGNMENT-10

U19CS012

1.) Using the information provided in the figure below, determine the values of Beta, Vcc and Rb theoretically. Also compute and verify the values of Ic, Vb, and Vc by implementing the circuit on Multisim.



1.) Circuit Image:

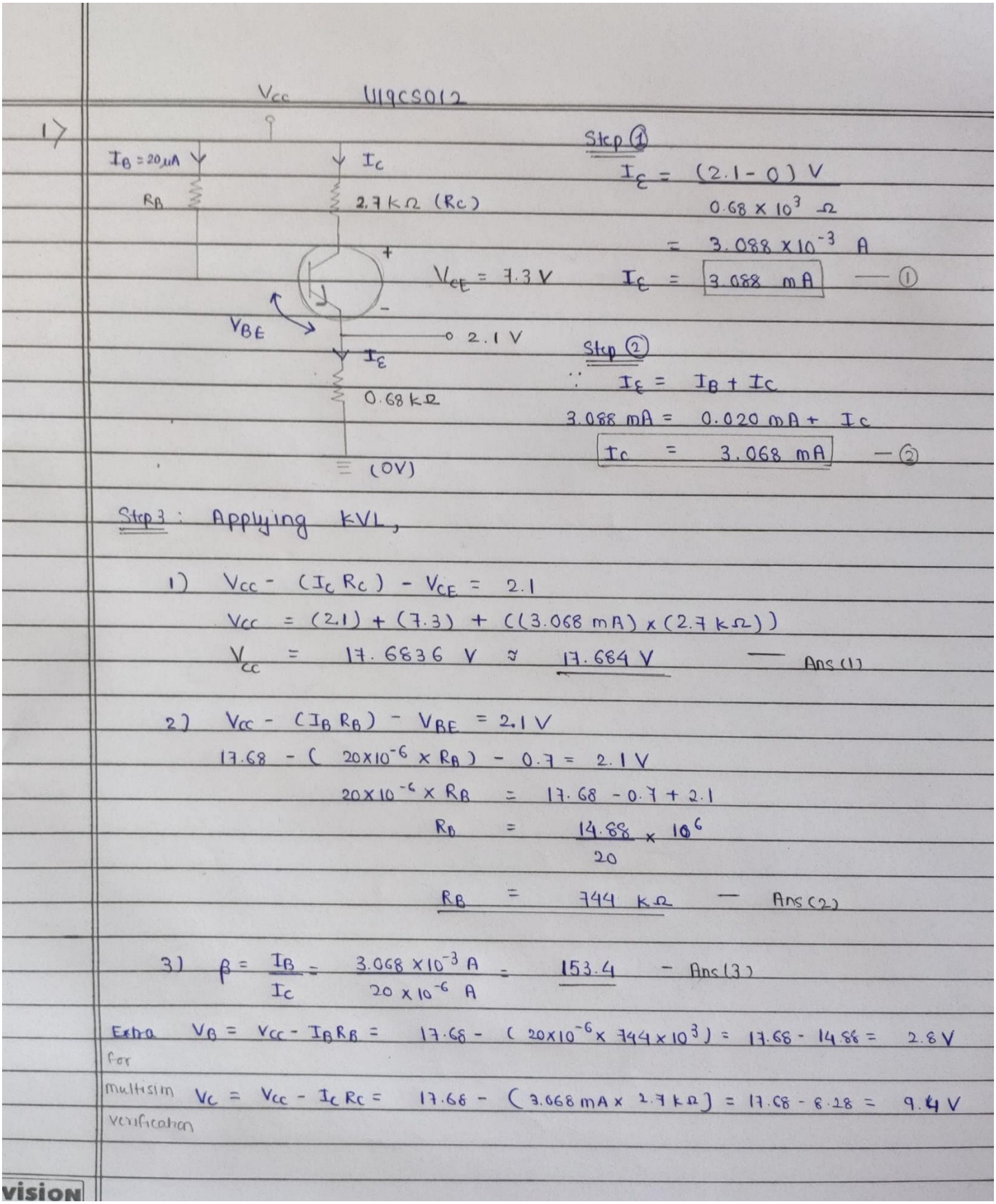


2.) *Grapher Image*:

Parameter	Graph	Theoretical
V_b	2.9030 V	2.8 V
V_c	9.4554 V	9.4 V
I_b	0.019866 mA	0.020 mA
I_c	3.0475 mA	3.068 mA
I_e	3.0882 mA	3.088 mA

We can Clearly See Both the **Theoretical** and **Multisim Values** are *Approximately Equal*. Hence the Experiment was Performed Successfully and Circuit is verified.

3.) Calculations



Step ①

$$I_E = \frac{(2.1 - 0)\ V}{0.68 \times 10^3\ \Omega} = 3.088 \times 10^{-3}\ A$$

$$I_E = \boxed{3.088\ mA} \quad — ①$$

Step ②

$$\therefore I_E = I_B + I_C$$

$$3.088\ mA = 0.020\ mA + I_C$$

$$\boxed{I_C = 3.068\ mA} \quad — ②$$

Step 3 : Applying KVL,

1) $V_{cc} - (I_C R_C) - V_{CE} = 2.1$

$V_{cc} = (2.1) + (7.3) + ((3.068\ mA) \times (2.7\ k\Omega))$

$V_{cc} = 17.6836\ V \approx \underline{17.684\ V}$ — Ans (1)

2) $V_{cc} - (I_B R_B) - V_{BE} = 2.1\ V$

$17.68 - (20 \times 10^{-6} \times R_B) - 0.7 = 2.1\ V$

$20 \times 10^{-6} \times R_B = 17.68 - 0.7 + 2.1$

$R_B = \frac{14.88}{20} \times 10^6$

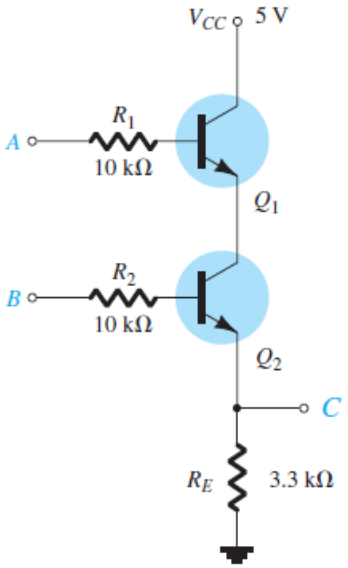
$\underline{R_B = 744\ k\Omega}$ — Ans (2)

3) $\beta = \frac{I_B}{I_C} = \frac{3.068 \times 10^{-3}\ A}{20 \times 10^{-6}\ A} = \underline{153.4}$ — Ans (3)

Extra for multisim verification: $V_B = V_{cc} - I_B R_B = 17.68 - (20 \times 10^{-6} \times 744 \times 10^3) = 17.68 - 14.88 = 2.8\ V$

$V_C = V_{cc} - I_C R_C = 17.68 - (3.068\ mA \times 2.7\ k\Omega) = 17.68 - 8.28 = 9.4\ V$

2. Simulate the below given circuit on Multisim and predict the type of Digital Logic implemented by the same. Use the default transistor available in Multisim. Attach all the four screenshots (00, 05, 50 and 55).



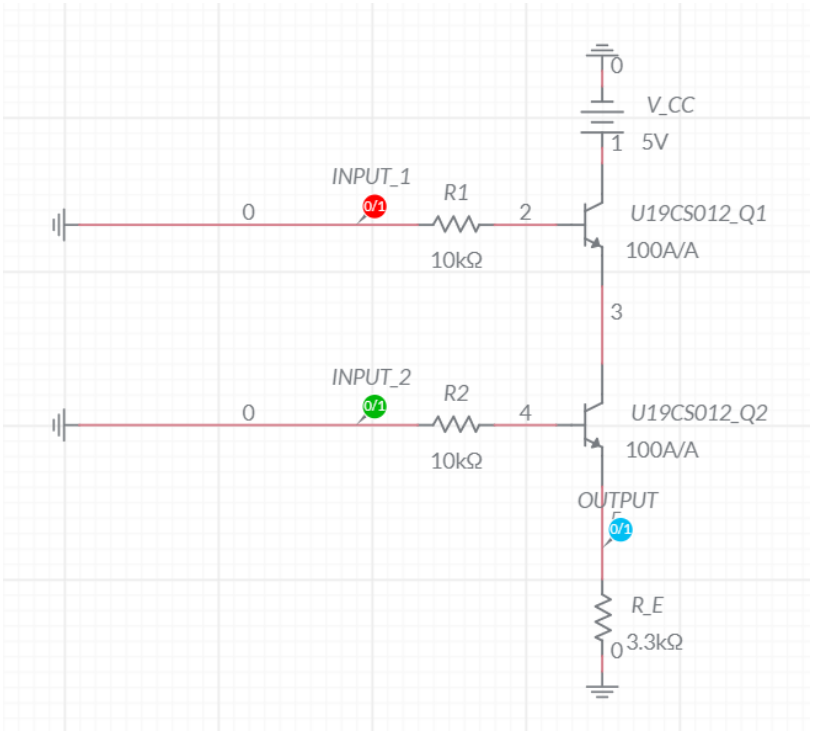
Answer:

By Observing the Truth Table Obtained from Multisim Simulation, We can clearly see that the Above Circuit [Equivalent to] represents the **Logical AND** Gate.

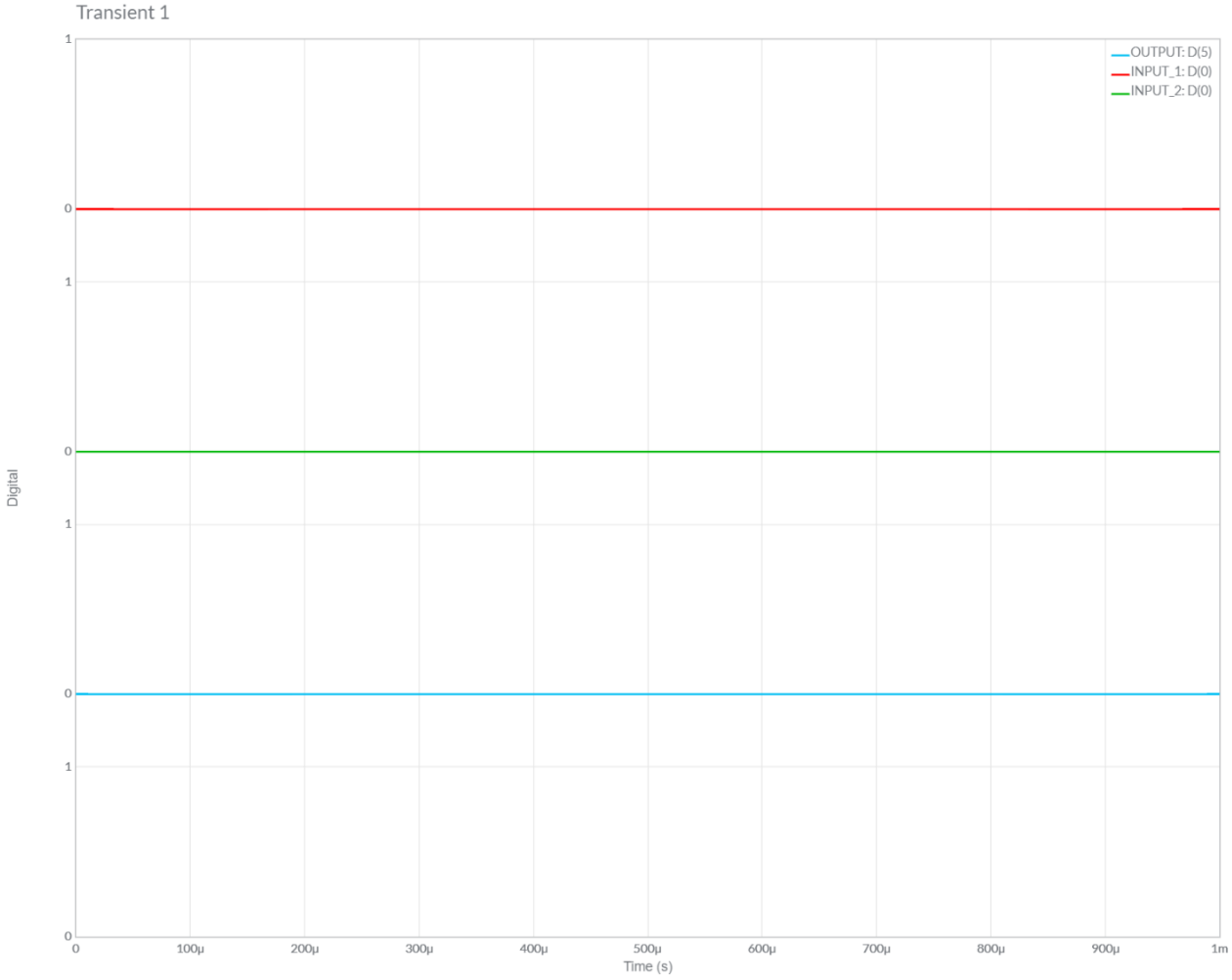
INPUT1	INPUT2	OUTPUT
0	0	0
0	1	0
1	0	0
1	1	1

A.) Case #1: 00

1.) *Circuit Image*:

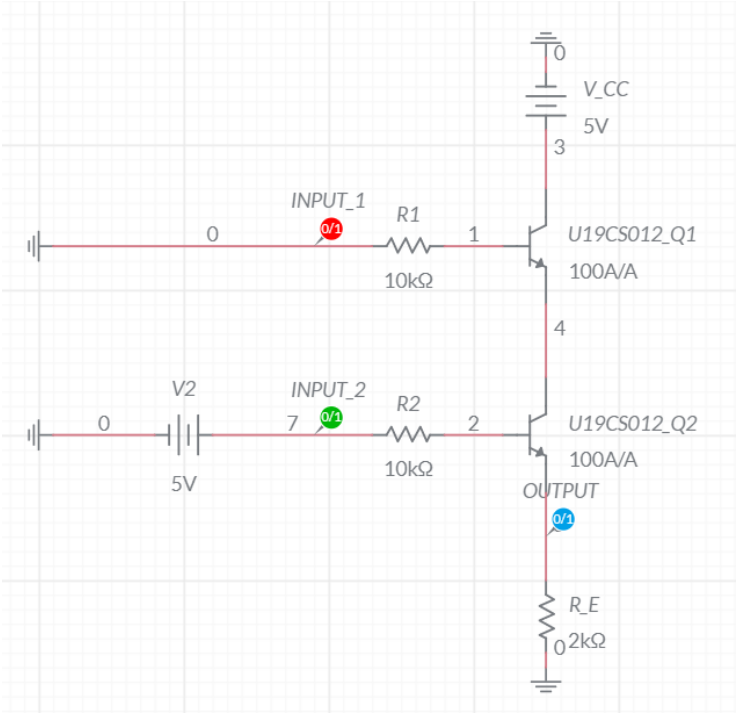


2.) *Grapher Image*:

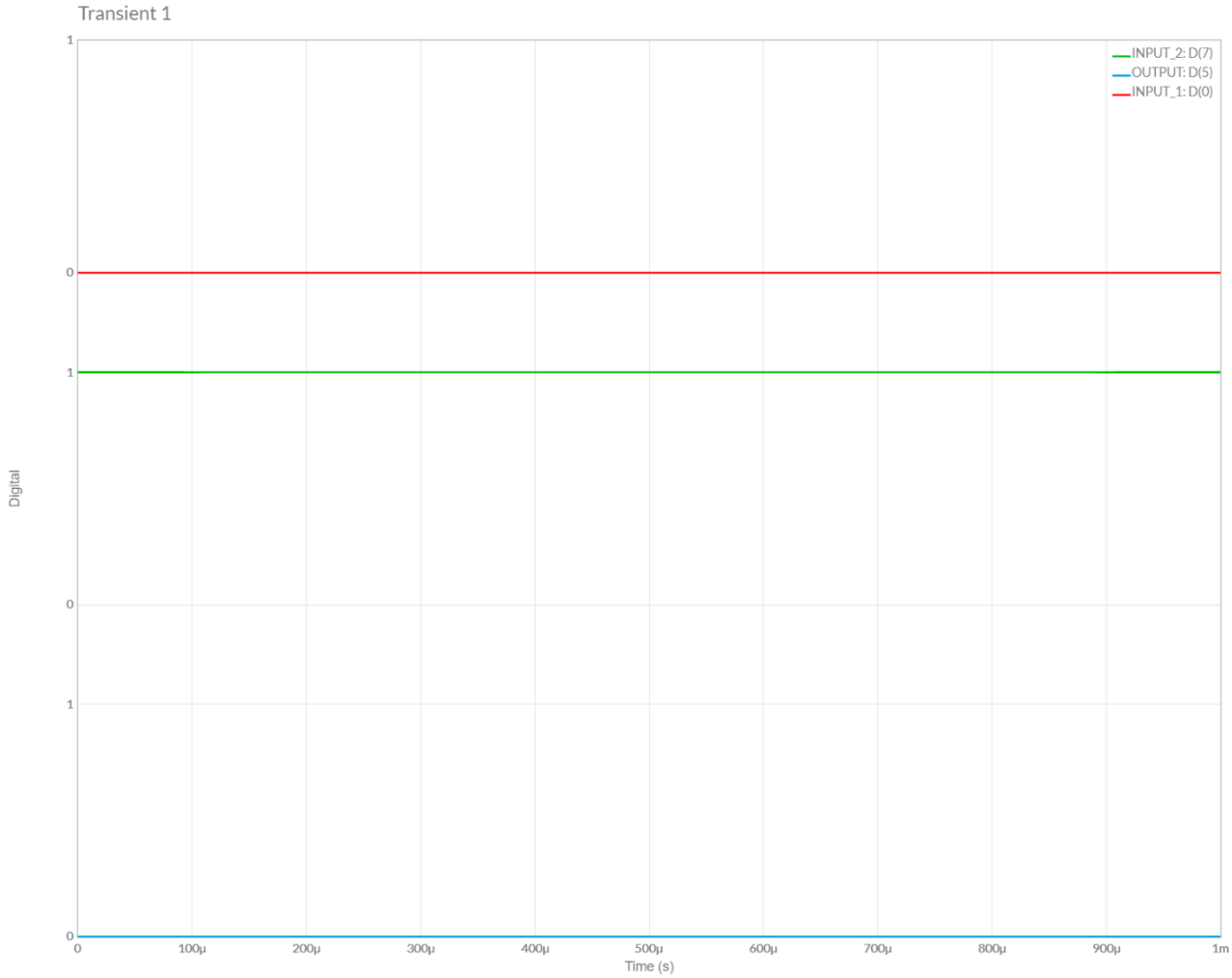


B.) Case #2: 05

1.) Circuit Image:

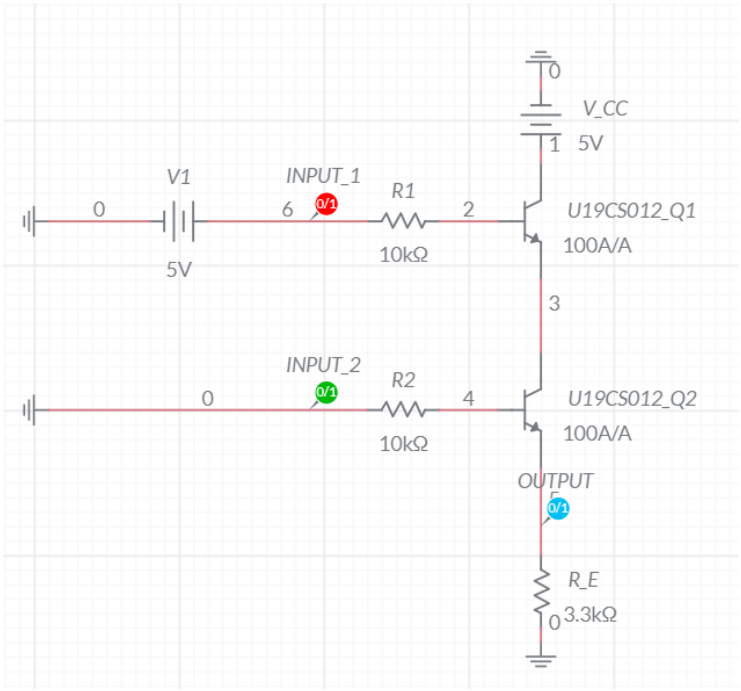


2.) Grapher Image:

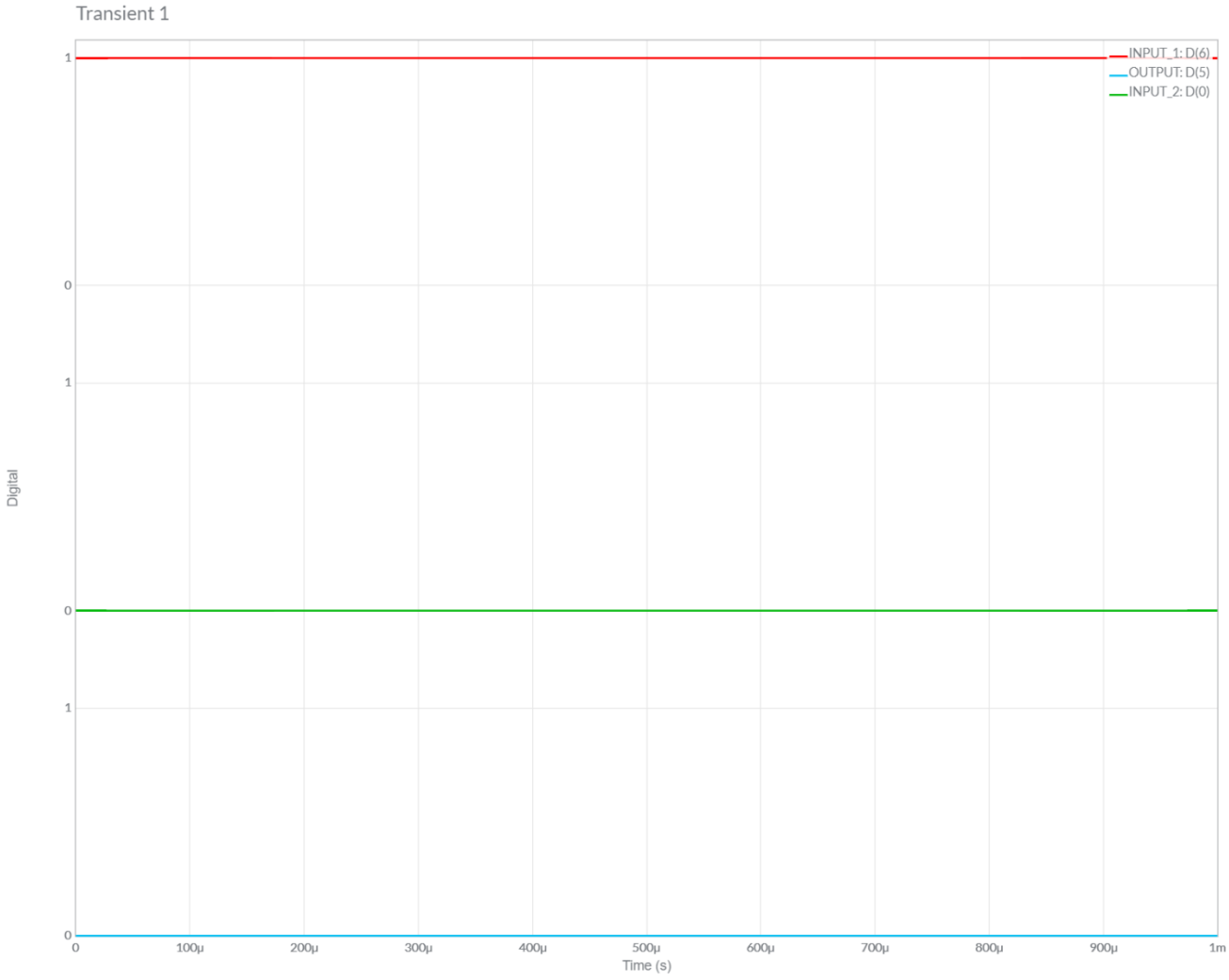


C.) Case #3: 50

1.) *Circuit Image*:

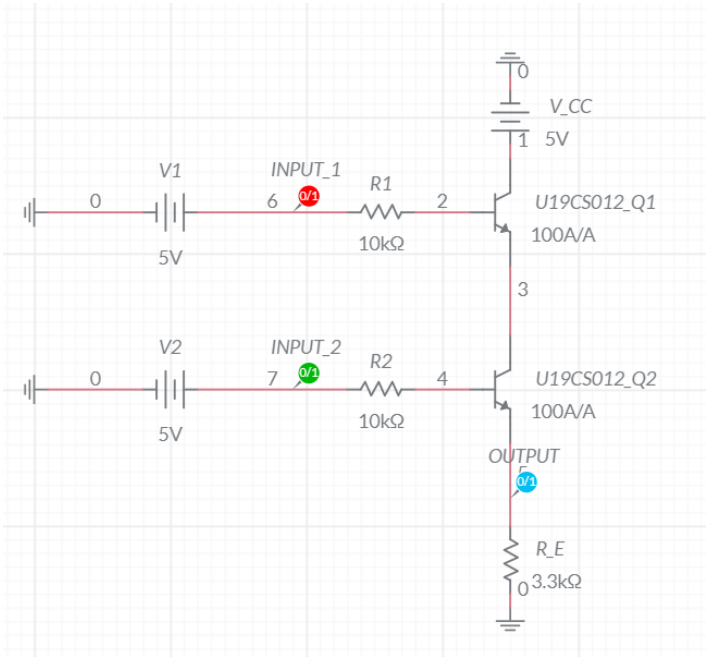


2.) *Grapher Image*:



D.) Case #4: 55

1.) Circuit Image:



2.) Grapher Image: