CO-PipeLining

If possible, write digit in the short answer
If answer is in text, write in CAPITAL LETTERS only

* Required

For simplicity to understand, which hardware diagram is used to implement MIPS 32-bit pipelining? *

○ Single Cycle

⦿ Multi Cycle

If a hardware unit of pipelining stage completes its task before the allotted clock cyle period, d) None of the mentioned *

○ the system gets hang

○ it will remain idle for the remaining time

⦿ it will perform some other task in the remaining time

○ its time gets reallocated to a different task

Which of the following is true about the MIPS 32-bit processor? *

⦿ Both of these

○ Data transfer can be done from memory to memory

○ ALU requires only register operands

○ None of these

Which of the following is an advantage of pipelining? *

○ None of these

⦿ Both of these

○ Instruction throughput increases

○ Pipelining increases the overall performance of the CPU

In pipelining the pipeline stage which requires the least time is performed first. *

⦿ False

○ True

In the pipelining, each stage of instructions should get completed within
_____ clock cycle to increase the speed of performance. *

1

MIPS Processor uses only register data for ALU operation, so it is possible to
implement pipelining. *

◉ True

○ False

MIPS processor requires _____ programmer invisible storage components to
implement 5-stage pipelining. *

○ 3

○ Option 4

○ None of these

◉ 2

The MIPS-32 bit processor has _____ bit instruction code in the pipelining. *

32

Which of the following is the advantage of Pipelining?A. cycle time of the
processor is reduced.B. The design of pipelined processor is complex and costly
to manufacture.C. The instruction latency is more.D. Both B and C *

○ The design of pipelined processor is complex and costly to manufacture

○ Execution time of the processor is increased

○ None of these

◉ Both of these

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