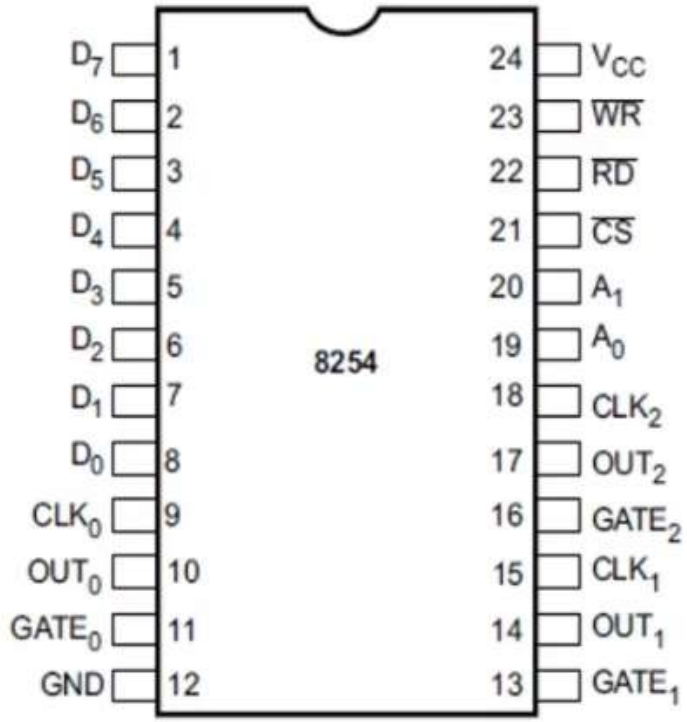
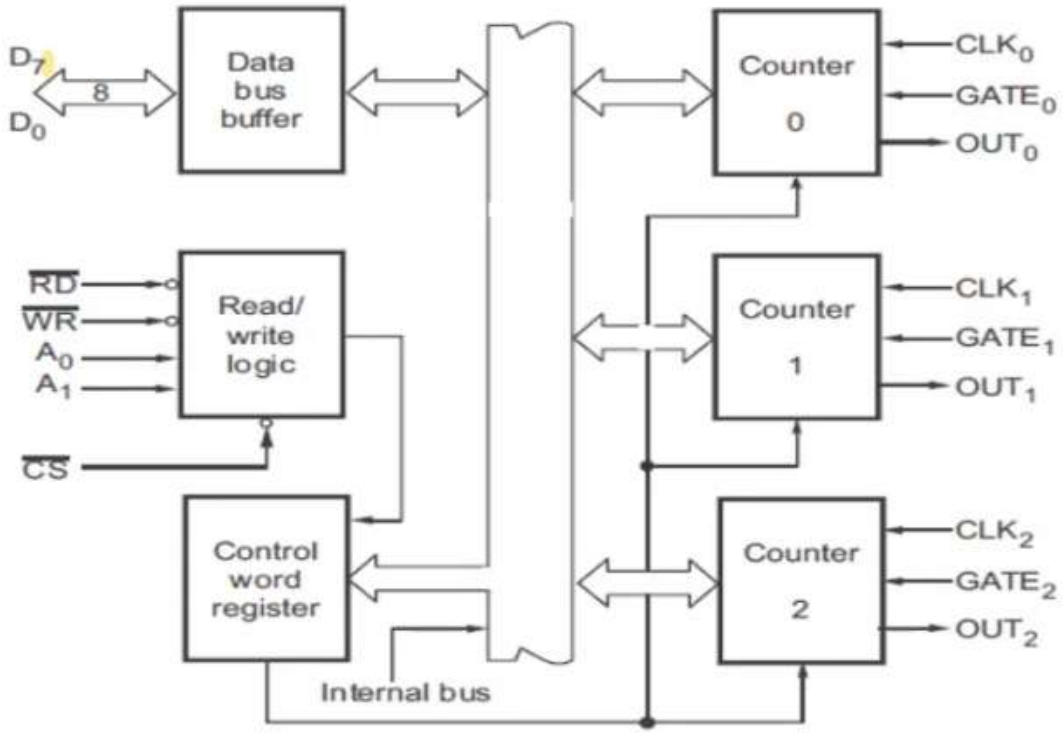
PIN Diagram of 8254



Block diagram



- It includes three counters, a data bus buffer, Read/Write control logic, and a control register.
- Each counter has two input signals CLOCK and GATE and one output signal OUT.
- Data Bus Buffer : tri-state, bi-directional, 8-bit buffer is used to interface the 8253/54 to the system data bus. The Data bus buffer has three basic functions.
- Programming the modes of 8253/54.
- Loading the count registers.
- Reading the count values.

Read/write logic

- Has five signals : RD, WR, CS and the address lines A0 and A1.
- In the peripheral I/O mode, the RD, and WR signals are connected to IOR and IOW, respectively. In memory-mapped I/O, these are connected to MEMR and MEMW.
- Address lines A0 and A1 of the CPU are usually connected to lines A0 and A1 of the 8253/54, and CS is tied to a decoded address.
- The control word register and counters are selected according to the signals on lines A0 and A1.

A_1	A_0	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control word Register

Control word Register and counters

- This register is accessed when lines A0 and A1 are at logic 1.It is used to write a command word which specifies the counter to be used (binary or BCD), its mode, and either a read or write operation.
- Each counter consists of a single, 16 bit, pre-settable, down counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of modes stored in the control word register.
- The counters are fully independent. The programmer can read the contents of any of the three counters without disturbing the actual count in process.

Control word register format (8-bit)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC_1	SC_0	RW_1	RW_0	M_2	M_1	M_0	BCD

SC - Select counter

SC_1	SC_0	
0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2
1	1	Illegal for 8253 Read -Back command for 8254 (See Read operations)

M - Mode

M_2	M_1	M_0	
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
x	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW - Read /Write

RW_1	RW_0	
0	0	Counter latch command (See Read operations)
0	1	Read / Write least significant byte only
1	0	Read / Write most significant byte only
1	1	Read / write least significant byte first, then most significant byte

BCD :

0	Binary counter 16 - bits
1	Binary coded decimal (BCD) Counter (4 Decades)

Programming 8253/54

- Each counter of the 8253/54 is individually programmed by writing a control word into the control word register (A0 - A1 = 11)

- Bits SC1 and SC0 select the counter, bits RW1 and RW0 select the read, write or latch command, bits M2, M1 and M0 select the mode of operation and bit BCD decides whether it is a BCD counter or binary counter

WRITE operation

- Write a control word into control register.
- Load the low-order byte of a count in the counter register.
- Load the high-order byte of count in the counter register.

READ Operation

- In some applications, especially in event counters, it is necessary to read the value of the count in process.
- This can be done by three possible methods:

- **Simple Read** : It involves reading a count after inhibiting the counter by controlling the gate input or the clock input of the selected counter, and two I/O read operations are performed by the CPU. The first I/O operation reads the low-order byte, and the second I/O operation reads the high order byte

- **Counter Latch Command** : In the second method, an appropriate control word is written into the control register to latch a count in the output latch, and two I/O read operations are performed by the CPU. The first I/O operation reads the low-order byte, and the second I/O operation reads the high order byte.

- **Read-Back Command (Available only for 8254)** : The third method uses the Read-Back command. This command allows the user to check the count value, programmed Mode, and current status of the OUT pin and Null count flag of the selected counter(s).

Control Word register for READ-BACK command

A_0, A_1 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT_2	CNT_1	CNT_0	0

D_5 : 0 = Latch count of selected counter(s)
D_4 : 0 = Latch status of selected counter(s)
D_3 : 1 = Select counter 2
D_2 : 1 = Select counter 1
D_1 : 1 = Select counter 0
D_0 : Reserved for future expansion : must be 0.

- The Read-Back command may be used to latch multiple counter output latches by setting the COUNT bit D5 = 0 and selecting the desired counter (s).
- Each counter's latch count in held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read.

Other features of READ-BACK command

- The Read-Back command may also be used to latch status information of selected counter(s) by setting STATUS bit D4 = 0. The contents of the counter must be latched before reading. The status of a counter is then accessed by a read from that counter.
- **Interleaved Read and Write :** Another feature of the 8254 is that reads and writes of the same counter may be interleaved. For example, if the counter is programmed for the two byte counts, the following sequence is valid.
- 1.Read least significant byte. 2. Write new least significant byte.
- 3. Read most significant byte. 4. Write new most significant byte

- Bit D5 - D0 contains the counter's programmed mode exactly as written in the last mode control word. Bit D7 contains the current status of the output pin.
- In 8254, it is not possible to read count from the counter, if the count is not loaded into the counting element (CE). The Bit D6 indicates whether the counting element has count or not. If D6= 0, counting element has count otherwise null count.

Control status format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
OUTPUT	NULL COUNT	RW_1	RW_0	M_2	M_1	M_0	BCD

D_7 1 = OUT pin is 1.

0 = OUT pin is 0.

D_6 1 = NULL count.

0 = Count available for reading.

D_5-D_0 = Counter programmed mode. ([redacted])

MODE 0 : Interrupt on Terminal count

- The output will be initially low after the mode set operation.
- Once count is loaded in the register counter is decremented at every cycle. When reaches zero, OUT goes high.
- Used as an interrupt
- OUT remains high until a new count or command word is loaded
- **Gate Disable**
- 1) Gate = 1 enables counting.
- 2) Gate = 0 disables counting.
- Gate has no effect on OUT

MODE 0

- **New Count**
- If a new count is written to the counter, it will be loaded on the next CLK pulse and counting will continue from the new count
- **In case of two byte count :**
- 1) Writing the first byte disables counting.
- 2) Writing the second byte loads the new count on the next CLK pulse and counting will continue from the new count.

MODE 1 : Hardware Retriggerable One-shot

- The output will be initially high.
- When Gate triggered , OUT goes low and at the end of the count , OUT goes high again.
- Generate one-shot pulse.

MODE 1

- **New count**
- If the counter is loaded during one shot pulse, the current one shot is not affected unless the counter is retriggered. If retriggered, the counter is loaded with the new count and the one-shot pulse continues until the new count expires