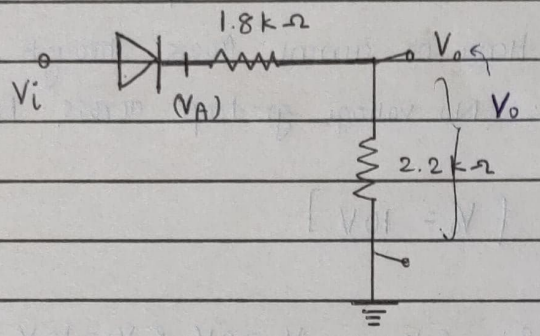
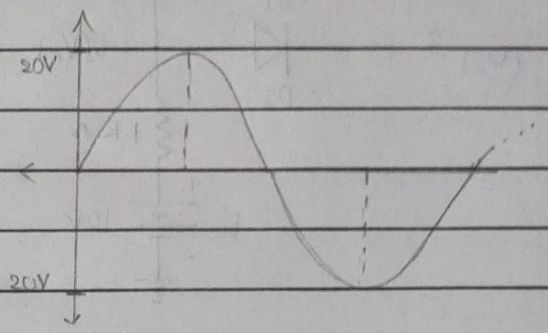
DELD ASSIGNMENT 6 (UMACS012)

Q1.)



Input waveform:



V_A = Vinput − 0.7 (forward voltage of Si diode)

= (20 − 0.7) V

= 19.3 V

Applying Voltage division Rule,

$$V_o = V_A * \frac{(2.2\,k\Omega)}{(2.2+1.8\,k\Omega)}$$

$$= 19.3 * \left(\frac{2.2}{4}\right) = \boxed{10.615\ V}$$

In Forward Bias ⇒ —— (short circuit)

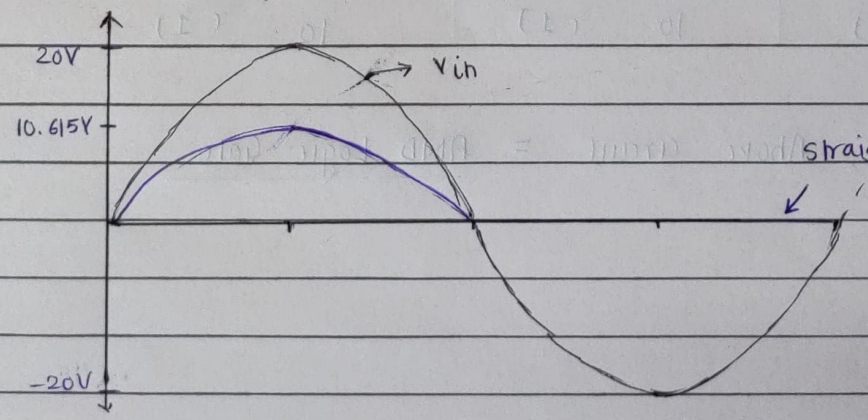
Reverse Bias ⇒ o o (open circuit) ⇒ i = 0 ⇒ No drop across resistor 2.2kΩ

[follows input waveform]

Positive half cycle ↑ V_o = 10.615 V at V_{in} = 20V

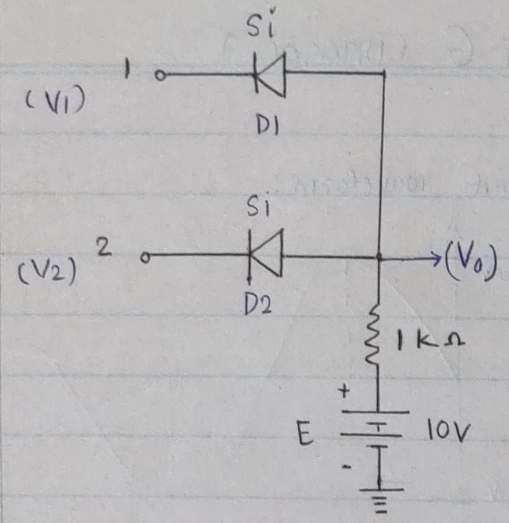
Negative half cycle V_o = 0 V [Negative clipper]

Expected Output Waveform:



(U19CS012)

2.)



CASE 1: Voltage at ① & ② is 10 V

$V_1 = 10$ $V_2 = 10$

∴ Circuit becomes open (∵ Both D1 & D2 reverse)

Hence no current flows through resistor

∴ No voltage ~~gr~~ drop across 1kΩ resistor

$[V_0 = 10V]$

CASE 2: Either $V_1 = 0V$ & $V_2 = 10V$

or $V_1 = 10V$ & $V_2 = 0V$

Due to one volt = 0 V, the Diode becomes Forward bias & acts as short circuit. [V_1 & V_2 are connected to ground) ie $V_i = 0V$

∴ $[V_0 = 0V]$

CASE 3:

$V_1 = 0V$ $V_2 = 0V$

Both are grounded

∴ D1 & D2 both forward Biased

∴ $[V_0 = 0V]$

Truth Table (Theoratical)

INPUTS				OUTPUT (in volts)	
1 (volt)		2 (volt)			
0	(0)	0	(0)	0	(0)
10	(1)	0	(0)	0	(0)
0	(0)	10	(1)	0	(0)
10	(1)	10	(1)	10	(1)

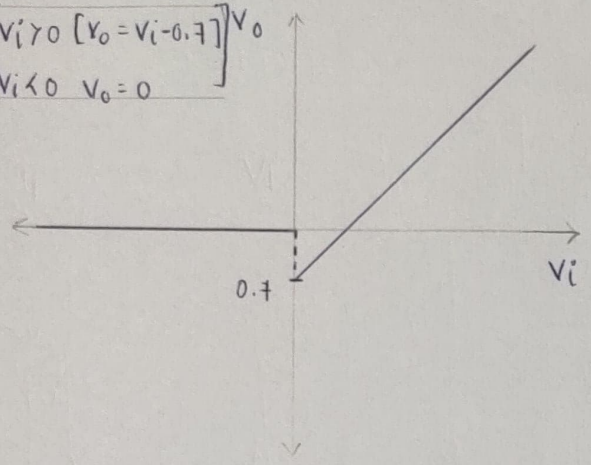
Therefore, Above circuit = AND Logic Gate

(Q3) U19CS012.

(A) Negative clipper

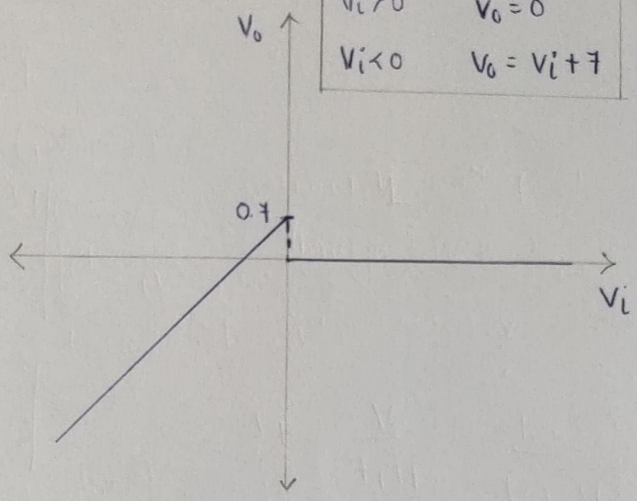
$V_i > 0$ $[V_o = V_i - 0.7]$

$V_i < 0$ $V_o = 0$



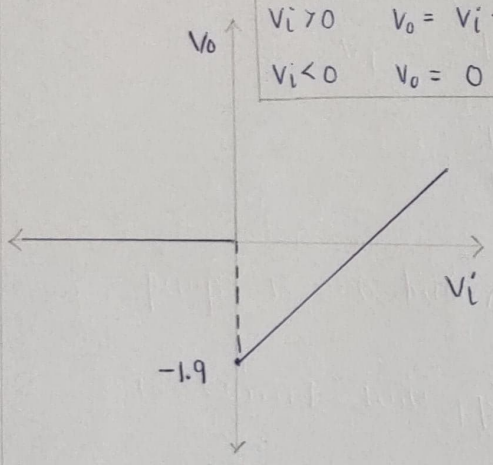
(B) Positive clipper

$V_i > 0$	$V_o = 0$
$V_i < 0$	$V_o = V_i + 7$



(C) Negative clipper with Bias - I (1.2+0.7)

$V_i > 0$	$V_o = V_i - 1.9$
$V_i < 0$	$V_o = 0$



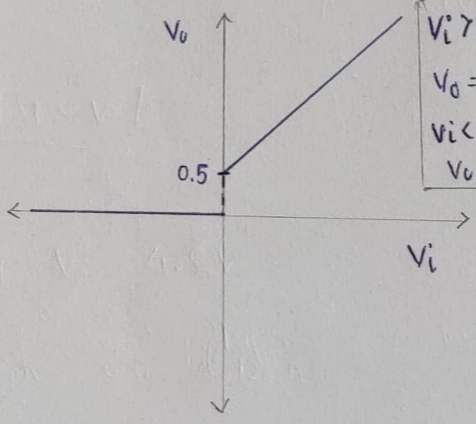
(D) Negative clipper with Bias - II

$V_i > 0$

$V_o = V_i + 1.2 - 0.7 = V_i + 0.5$

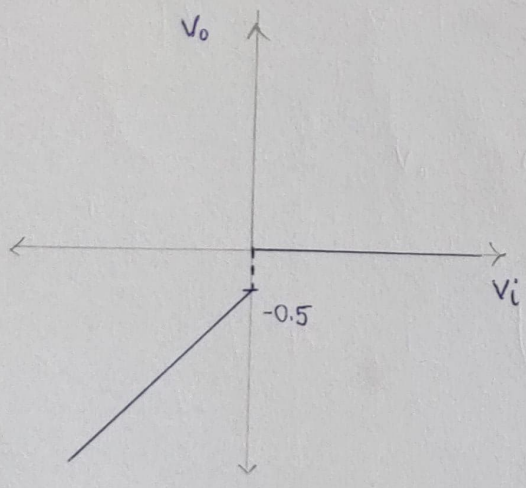
$V_i < 0$

$V_o = 0$



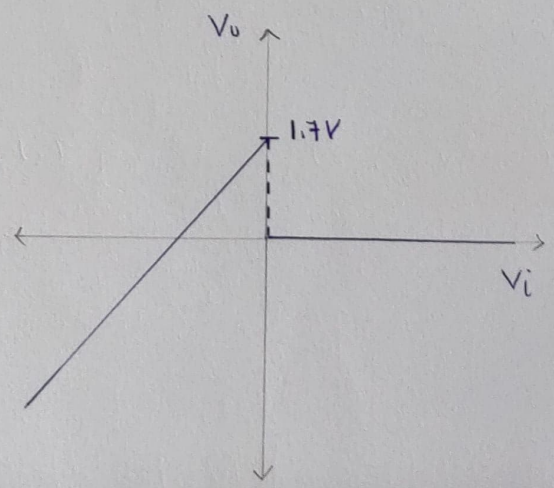
(E) Positive clipper with Bias - I

$V_i > 0$	$V_o = 0$
$V_i < 0$	$V_o = V_i - 0.5$



(F) Positive clipper with Bias - II

$V_i > 0$	$V_o = 0$
$V_i < 0$	$V_o = V_i + 1.9$



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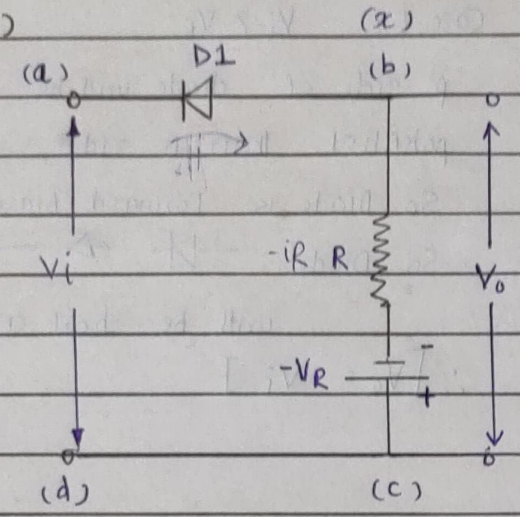
Q4.) (A)

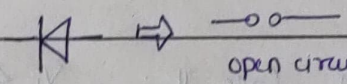


V_i = symmetrical sine wave

[$V_{peak} > V_{ref}$]

(I) During positive half cycle (~~-~~ x volts)

∵ Diode D1 will be in reverse bias [V_b = -ve & V_a = +ve]



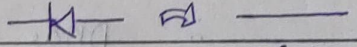
open circuit

therefore no current will flow

(II) During Negative half cycle (after $-\overset{x}{\cancel{0}}$ V)

[$V_o = -V_R + (0 * R) = -V_R$] — ①

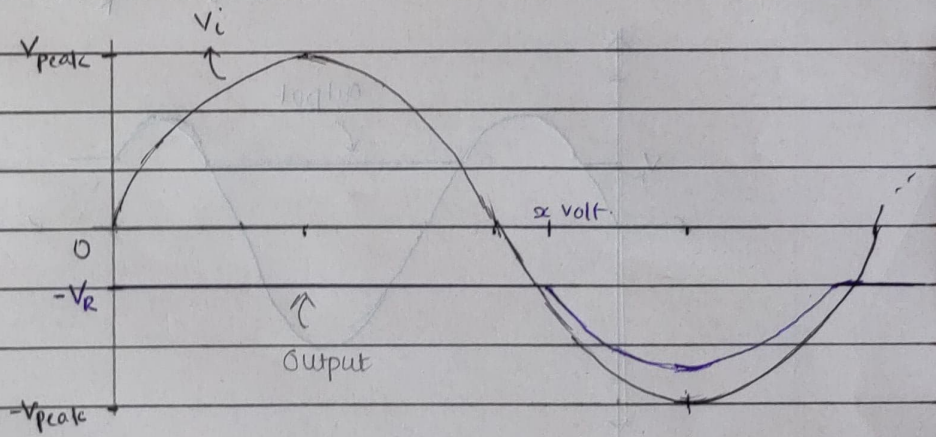
The Diode D1 behaves as



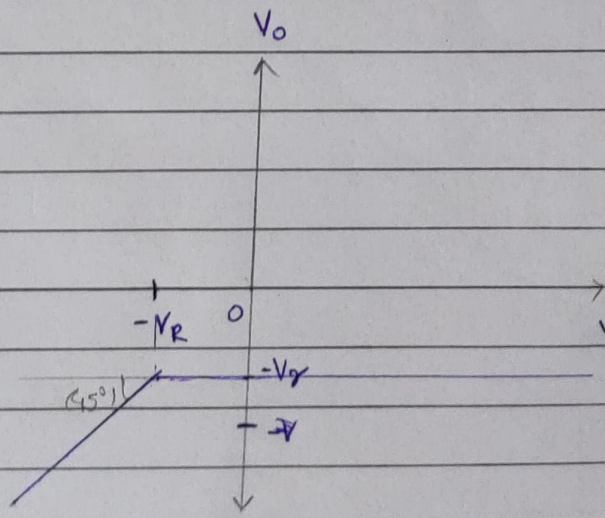
~~op~~ (short circuit)

∴ [$V_o = V_i$]

Predicted output :



Transfer characteristics



① $V_i \geq -V_R$ | $V_o = -V_R$ |

② $V_i < -V_R$ ~~$V_o = -V_R \pm \delta$~~

$\delta = \frac{1}{1} R$

[$V_o = V_i$]

vision

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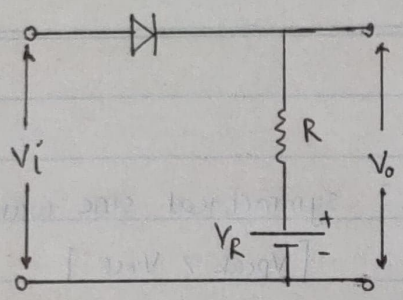
(B)



(I) Case I: $V_i > V_R$

p side of diode will be at higher potential than n side,

So Diode is Forward Biased.

So Diode 

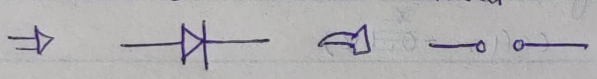
will be short-circuited

$\therefore [V_o = V_i]$

(II) Case II: $V_i < V_R$

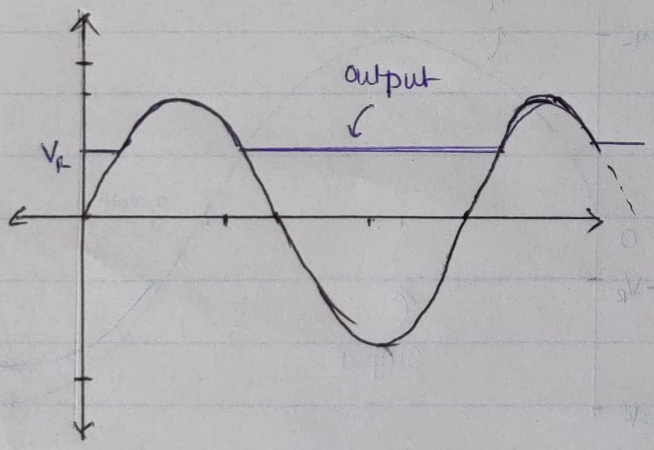
p side of Diode will be at low potential than n side

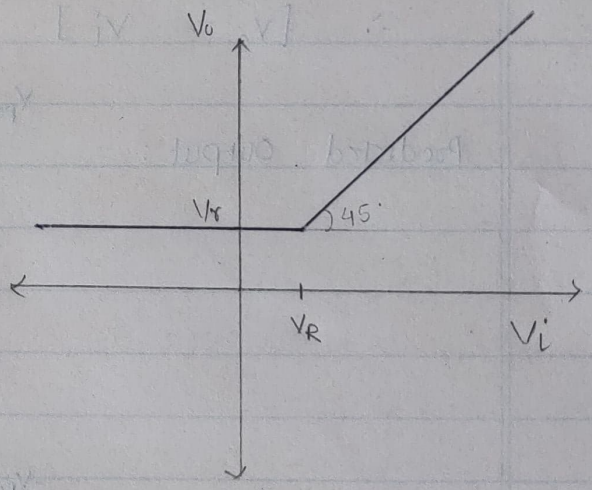
So Diode is Reverse biased



$\therefore$ Diode is Open-circuit

$\therefore [V_o = V_R]$





Transfer characteristics of circuit