Segment 6

8255A Programmable Peripheral Interface (PPI)

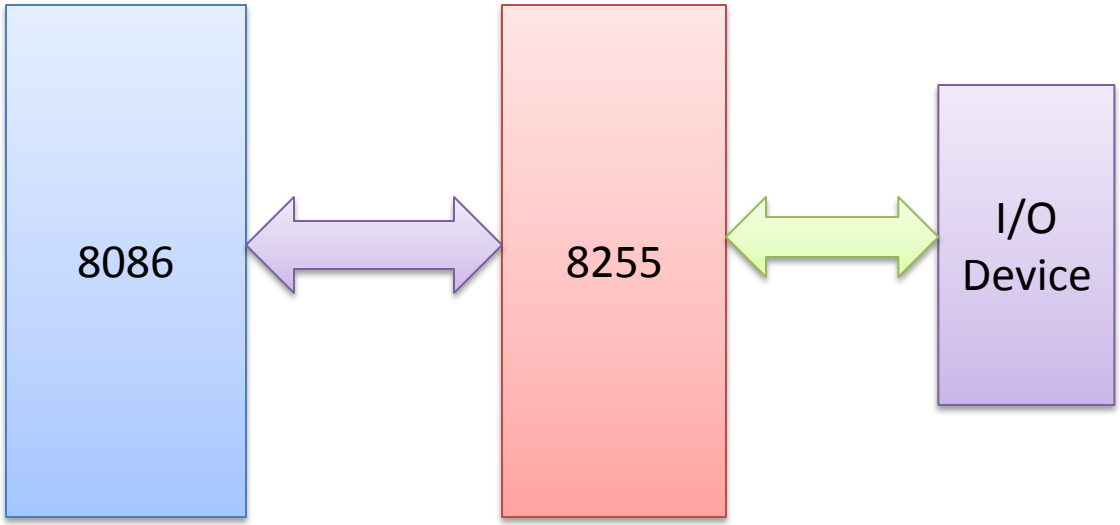
Content

- Why 8255A?
- Handshaking and Handshaking Signal
- Parallel Data Transfer
- 8255A Internal Block Diagram
- Description of 8255A Internal Block Diagram
- Programming Modes of 8255A
- Related Problems

Prepared By:
Mohammed Abdul kader
Lecturer, EEE, IIUC

Why 8255A ??

- Intel 8255A is a general purpose parallel I/O interface.
- The peripheral devices are slower than the microprocessor. PPI makes an inter-relation between microprocessor and peripheral devices.
- It provides three I/O port (Port A, Port B and Port C)

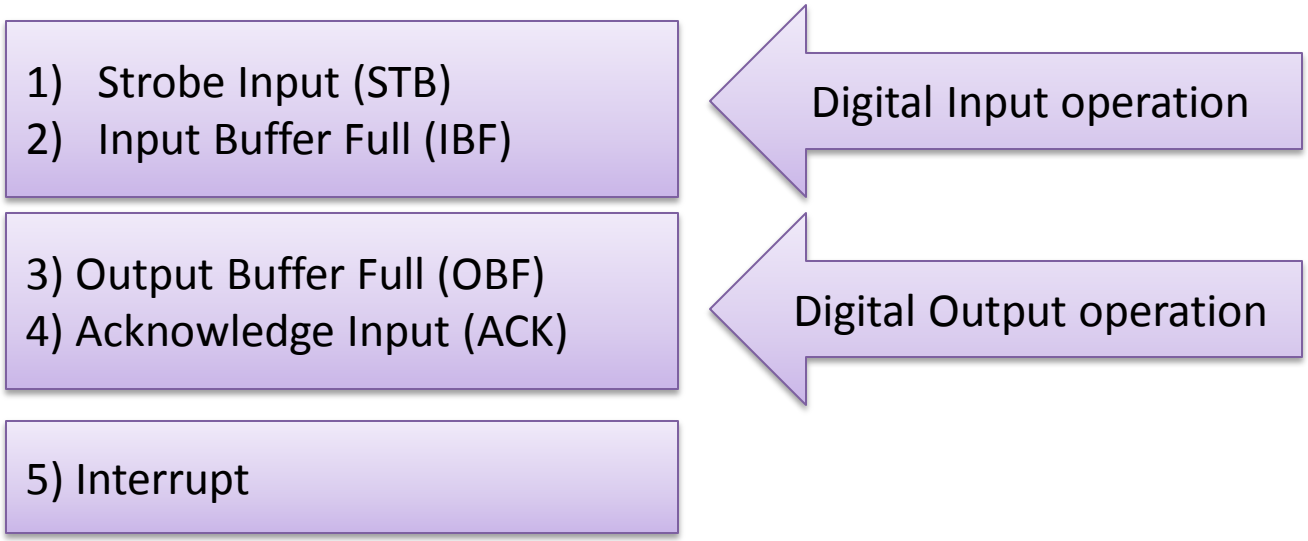


Handshaking

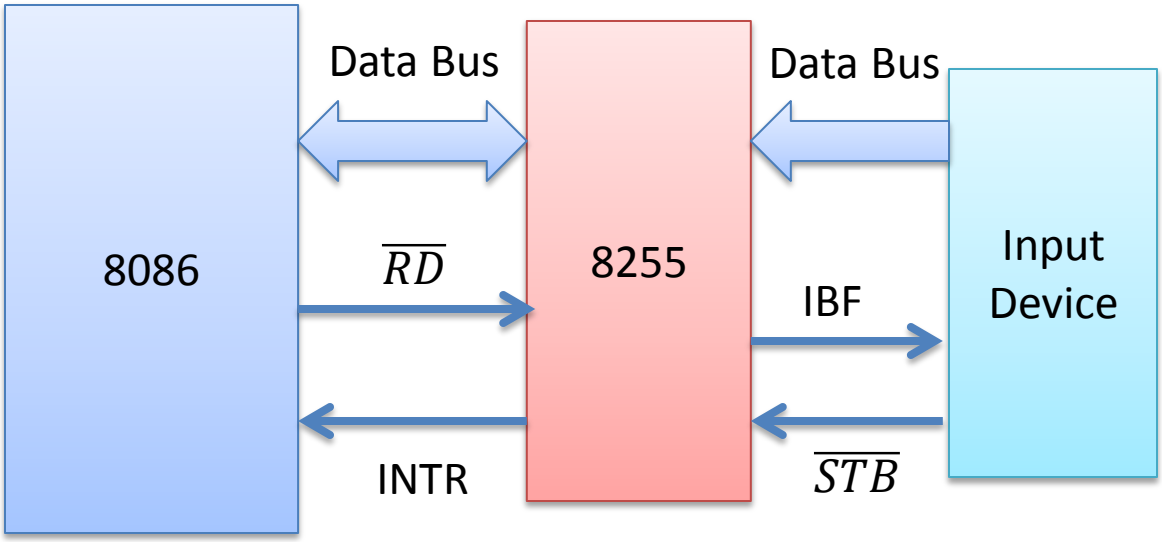
The making of inter relation between slower peripheral device and microprocessor is called handshaking.

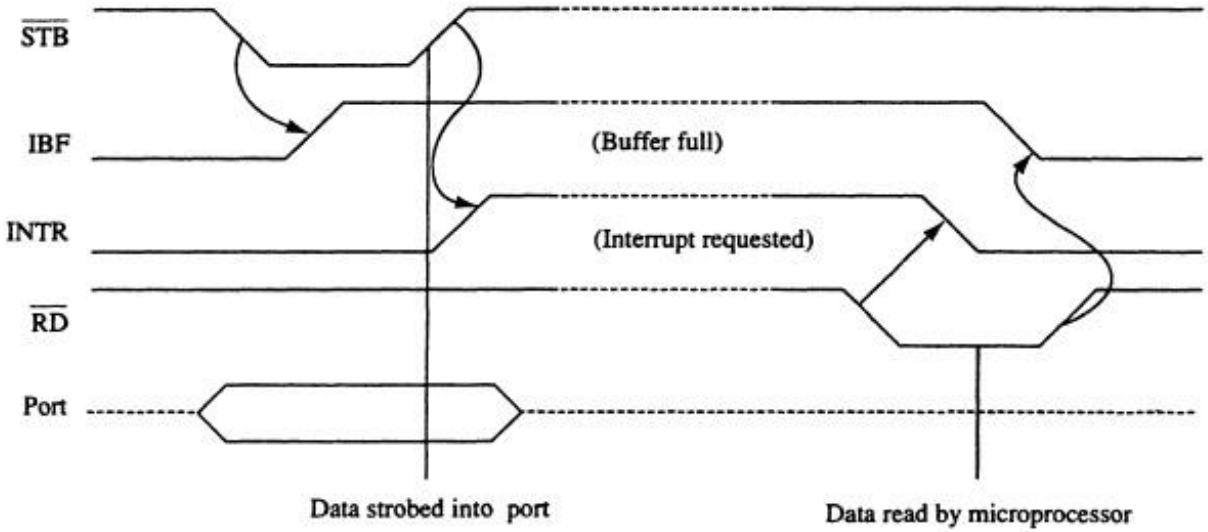
Handshaking Signal

Before making the inter-relation between peripheral device and microprocessor the PPI send some signals to microprocessor and peripheral device to perform the process, these signals are called handshaking signal. 8255-based devices that perform handshaking support following handshaking signals:



Handshaking Signal (Continued)





Read Operation

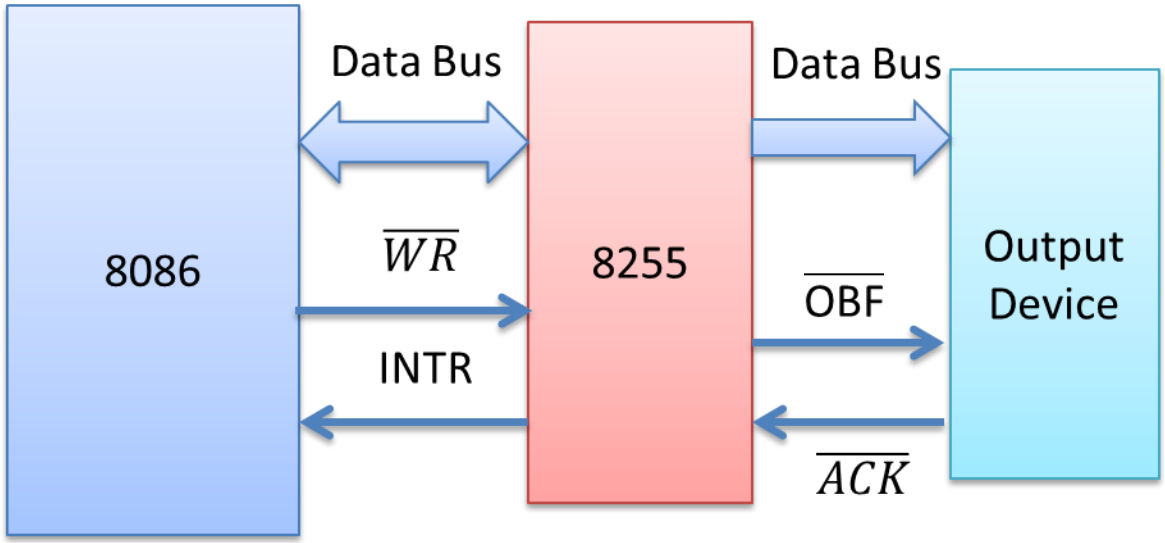
STB goes low indicates that data are loads into port latch.

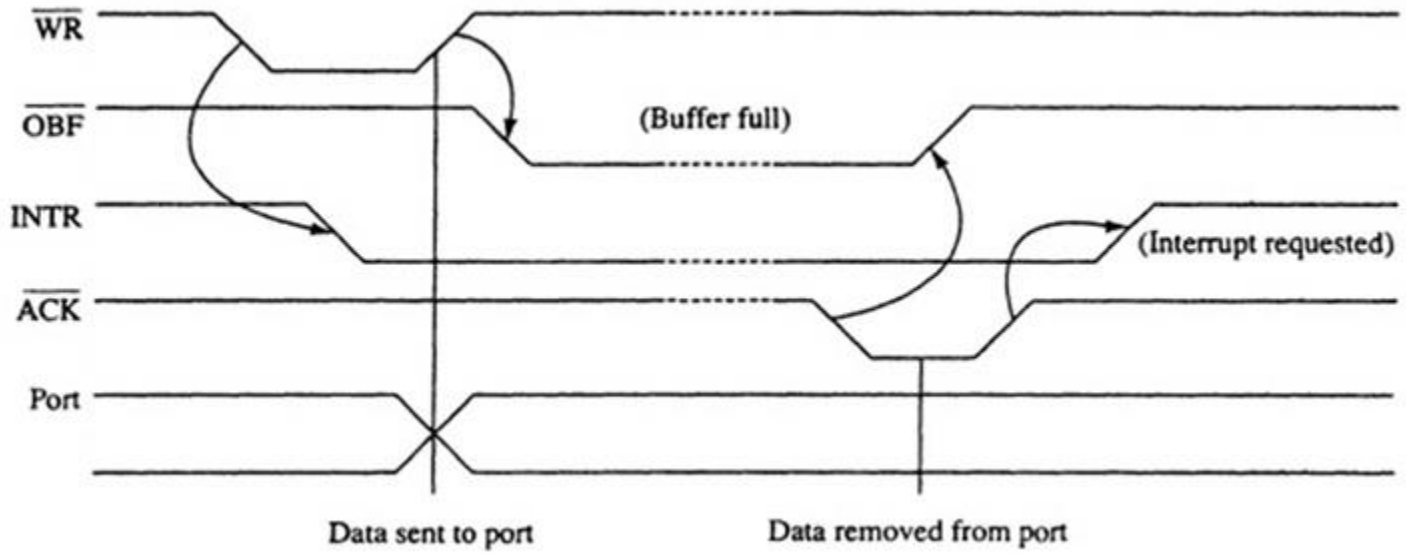
IBF Becomes high (at high to low transition of STB) indicates that input latch contains data.

INTR Becomes high (at low to high transition of STB) uP goes interrupt subroutine to read data. **RD becomes low.**

IBF becomes low when read complete, RD becomes high and IBF goes low.
IBF low means input latch has no data (Read complete)

Handshaking Signal (Continued)





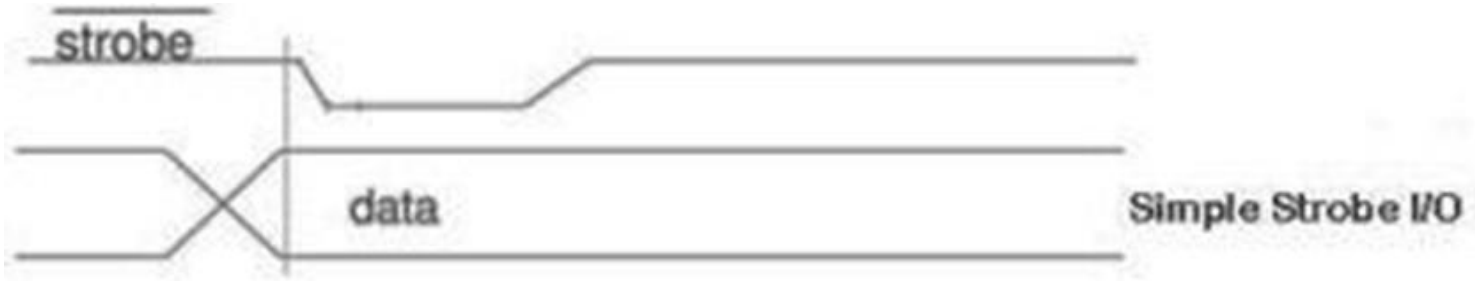
Parallel Data Transfer:

Simple I/O:

This data transfer method is used when the I/O devices need no communication before the data transfer. Such devices are thermostat, LED. The crossed lines on the wave form represent the time at which a new data byte becomes valid on the output lines of the port.

Simple Strobe I/O:

The sending device, such as a keyboard, outputs parallel data on the data lines, and then outputs an $\overline{STB}$ signal to let the receiving device know that valid data is present.



Parallel Data Transfer (Continued):

Single handshake Data transfer:

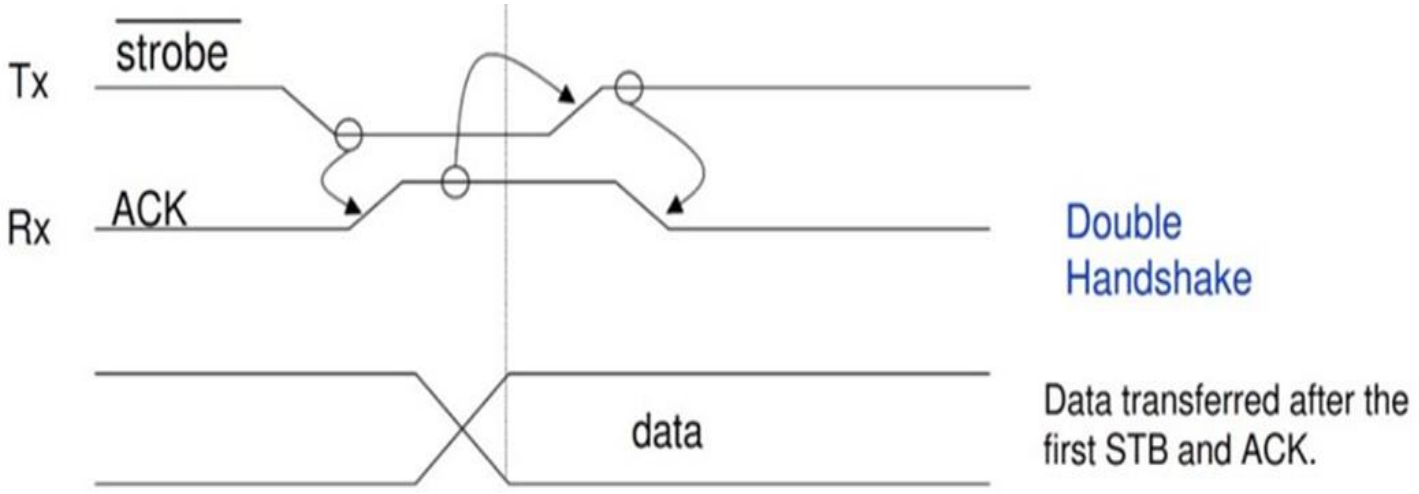
- The sending device outputs some parallel data and sends an $\overline{STB}$ signal to the receiving device. (i.e. sending device says receiving device, “I have some data for you”)
- As a response of $\overline{STB}$ signal receiver device reads data and send an acknowledge signal to indicate that the data has been read. (i.e. by acknowledge signal receiving device says to sending device, “your sending data is received and I am ready to get new data”)

Single Handshake

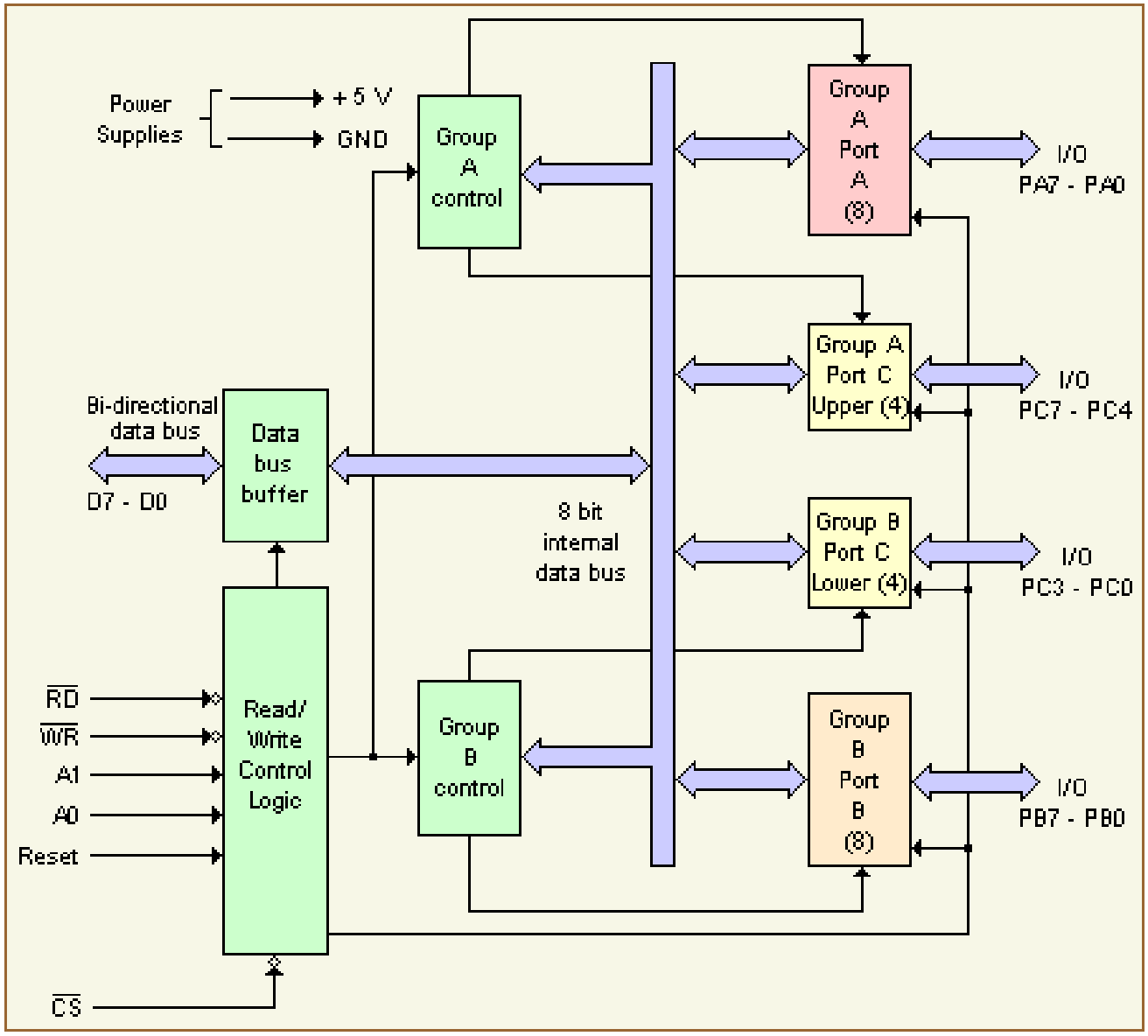
Parallel Data Transfer (Continued):

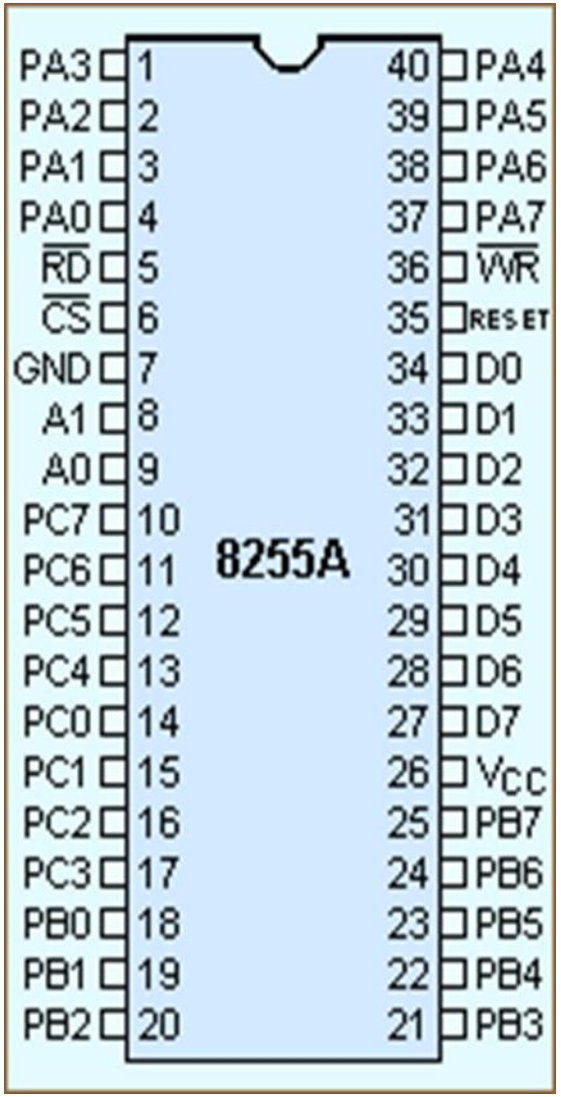
Double Handshake Data Transfer:

- The sending device asserts its $\overline{STB}$ line low to ask the receiving device “are you ready?”
- The receiving device raises its ACK line high to say “I am ready”.
- The peripheral device then sends the byte of data and raises its $\overline{STB}$ line high to say “Here is some valid data for you”.
- After it has read in the data, the receiving data drops its ACK line low to say “I have the data”. The receiving device is then ready to be requested for accepting the next data byte.



8255A Internal Block Diagram





Description of 8255A Internal Block Diagram

Data Bus Buffer

- This three-state bi-directional 8-bit buffer is used to interface the 8255 to the system data bus.
- Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU.
- Control words and status information are also transferred through the data bus buffer.

Read/Write Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words.

(CS) Chip Select. A "low" on this input pin enables the communication between the 8255 and the CPU.

(RD) Read. A "low" on this input pin enables 8255 to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255.

(WR) Write. A "low" on this input pin enables the CPU to write data or control words into the 8255.

(A0 and A1) These input signals, control the selection of one of the three ports or the control word register.

A1	A0	SELECTION
0	0	PORT A
0	1	PORT B
1	0	PORT C
1	1	CONTROL

(RESET) Reset. A "high" on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode.

Description of 8255A Internal Block Diagram (Continued)

Group A and Group B Controls

Each of the Control blocks (Group A and Group B) accepts "commands" from the CPU as "control word" and configure the ports (Port A, Port B and Port C) accordingly.
Port A and upper 4 bits of Port C are controlled by Group A
Port B and lower part of Port C are controlled by Group B

Ports A, B, and C

The 8255 has three 8 bit I/O ports and each one can be connected to the physical lines of an external device. All can be configured to a wide variety of functional characteristics by the system software .These ports are labeled as PA0-PA7 (PortA), PB0-PB7 (PortB) and PC0-PC7 (PortC).

GND (Ground) and Vcc

Summary of 8255A Pins

Port Pins: 24 (Port A = 8,Port B =8,Port C =8)
Control Pins: 6 (RD, WR, CS, RESET, A1, A0)
Data Lines: 8
Power Supply: 2 (VCC, GND)

Total 40 pins

Programming 8255A

Modes of Operation

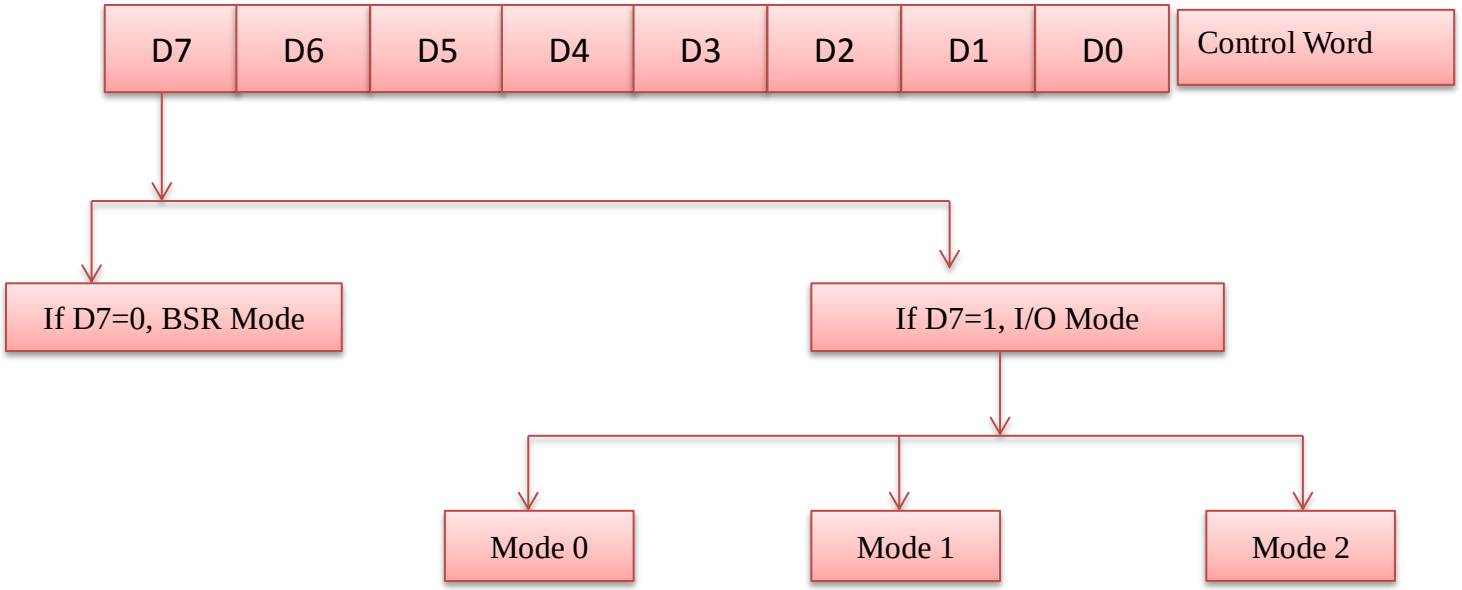
8255 can be configured in two modes

- BSR (Bit Set Reset) Mode
- I/O (Input-Output) Mode: Mode 0, Mode 1 and Mode 2

Modes are configured by Control Word

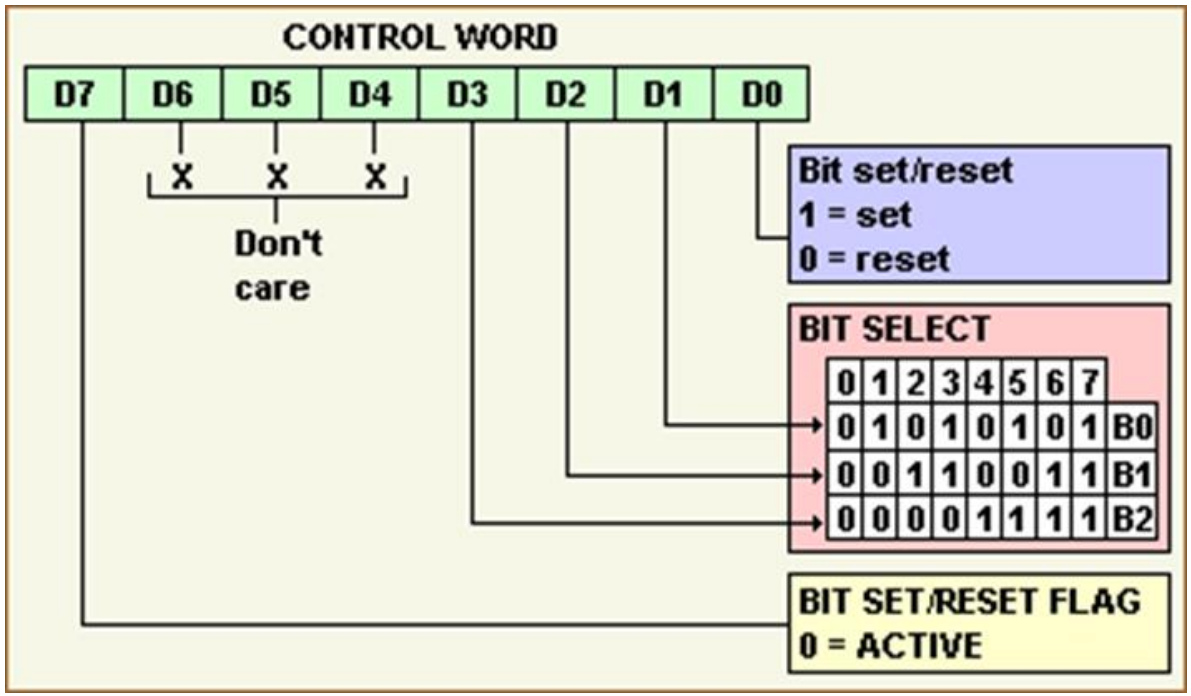
Control Word

A Control Word is an 8-bit data that stored in control register. Control Words are two types: (a) BSR Control Word (b) Mode definition Control Word



BSR Mode (Configured by Bit Set-Reset Control Word)

- If bit 7 of control word is a logic 0 then 8255 will be configured as BSR (Bit Set Rest) mode.
- In this mode we can set or reset the pins of port C



N.B: *Don't Cares are Generally set as zero.*

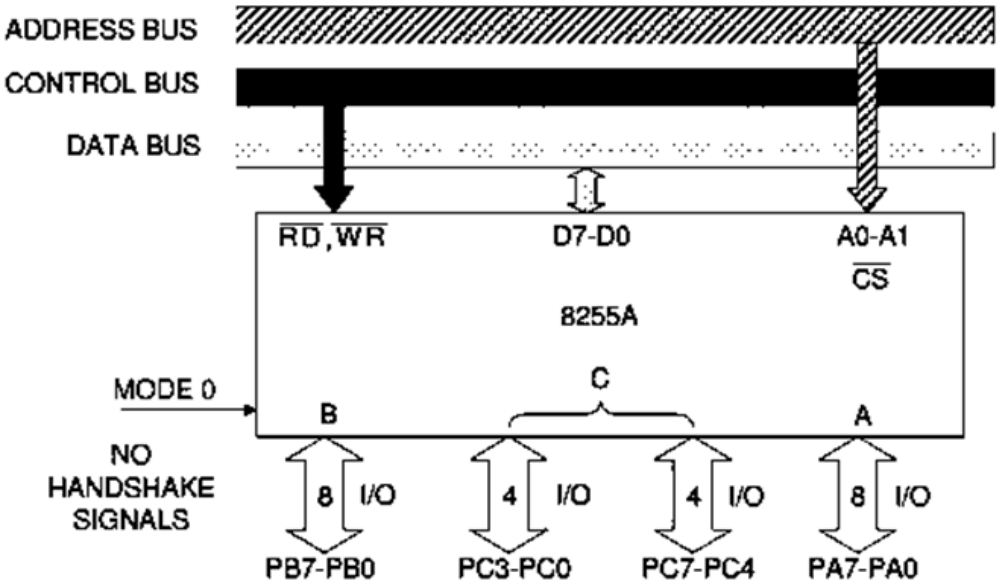
Problems: (a) Write a control word to reset PC5. (Ans: 0AH)
(b) Write a Control Word to Set PC2. (Ans: 05H)

I/O Mode (Configured by Mode definition CR)

- If bit 7 of the control word is a logical 1 then the 8255 will be configured as I/O mode.
- I/O mode consists of Mode0, Mode1 and Mode2.

Mode 0

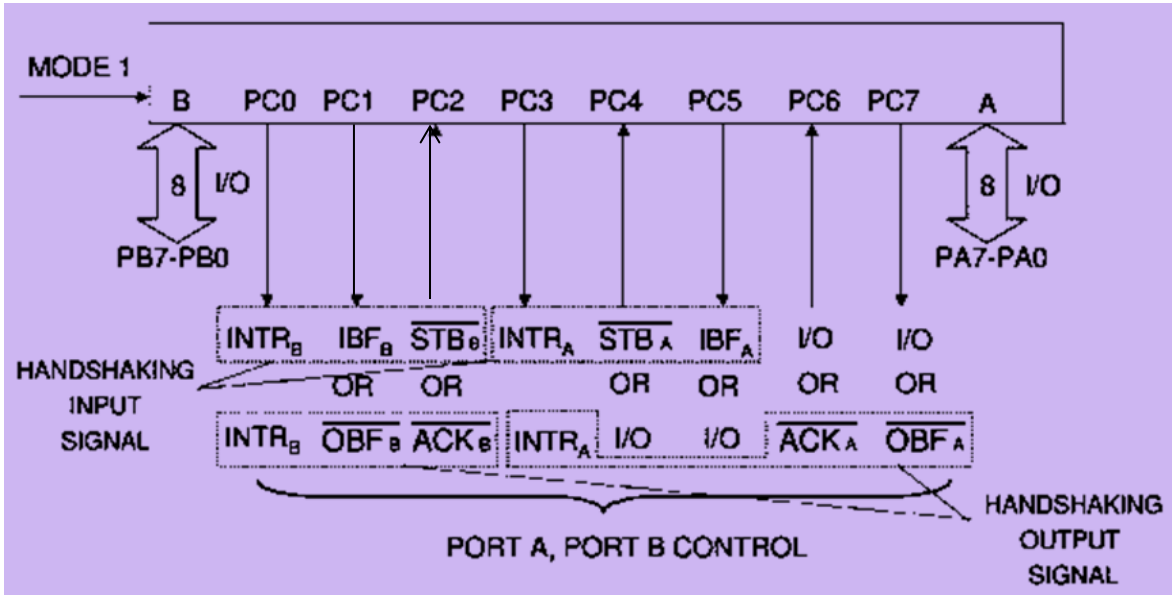
- Port A works as simple input or output without handshaking.
- Port B works as simple input or output without handshaking.
- Port C can be used together as an additional 8 bit port or they can be used individually as two 4-bit ports.
- When used as outputs, the Port C lines can be individually set or reset by sending a special control word to the control register address.



I/O Mode (Cont.)

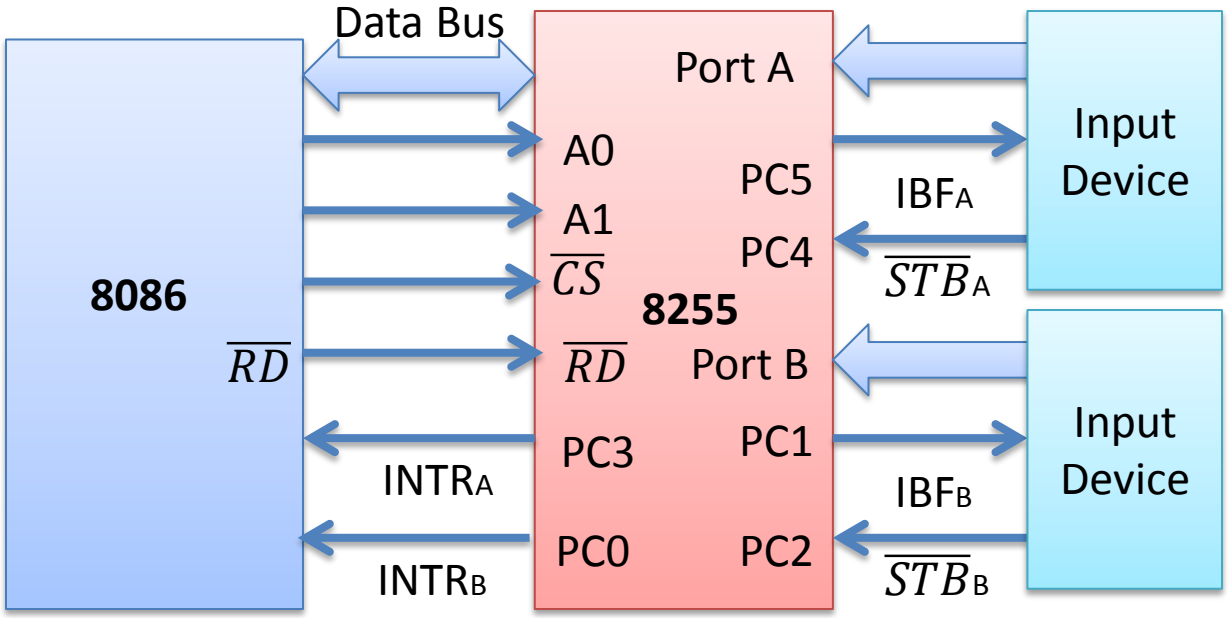
Mode 1

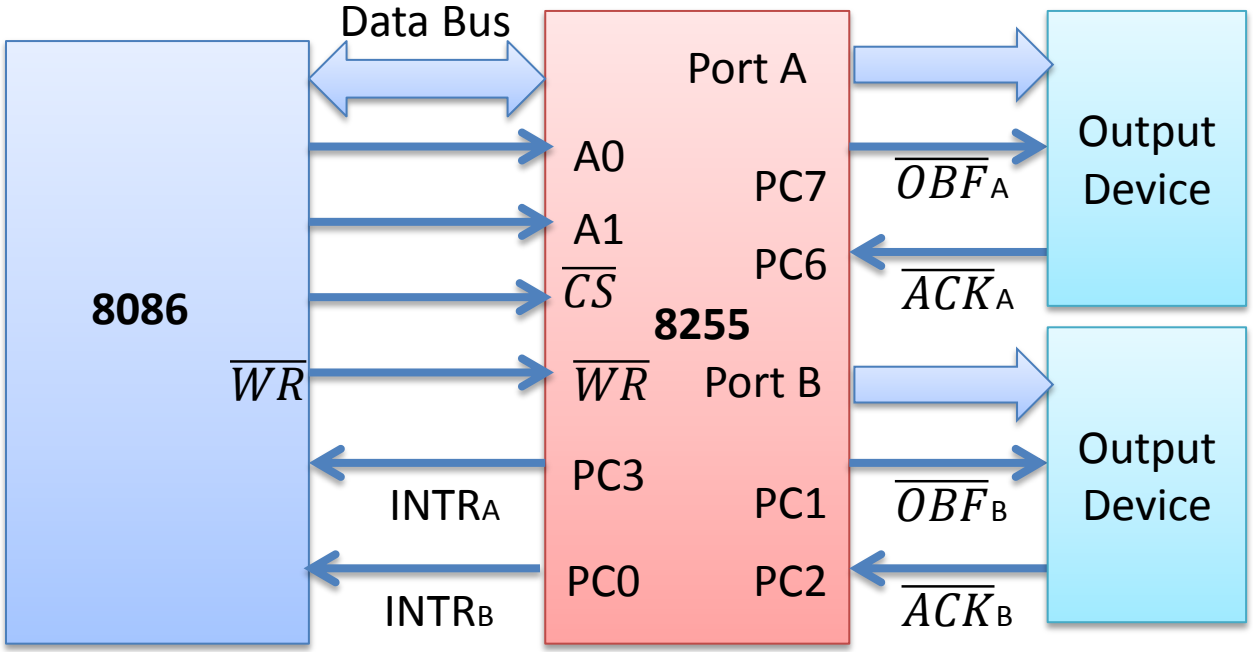
- Used for handshake input/output operation.
- Port B is initialized in mode 1 for either input or output, Pins PC0, PC1 and PC2 function as handshake lines.
- Port A can also be configured as input or output in mode 1. But handshake signal pins are not same for input and output mode as like Port B.
- If port A is initialized in mode 1 as handshake input port, then pins PC3, PC4 and PC5 function as handshake signals. (PC6 and PC7 are available for using as input lines or output lines)
- If port A is initialized as handshake output port, then PC3, PC6 and PC7 function as handshake signals. (PC4 and PC5 are available for using as input or output lines)



I/O Mode (Cont.)

Connection of Handshaking lines when Port A and Port B configured as Input in Mode 1



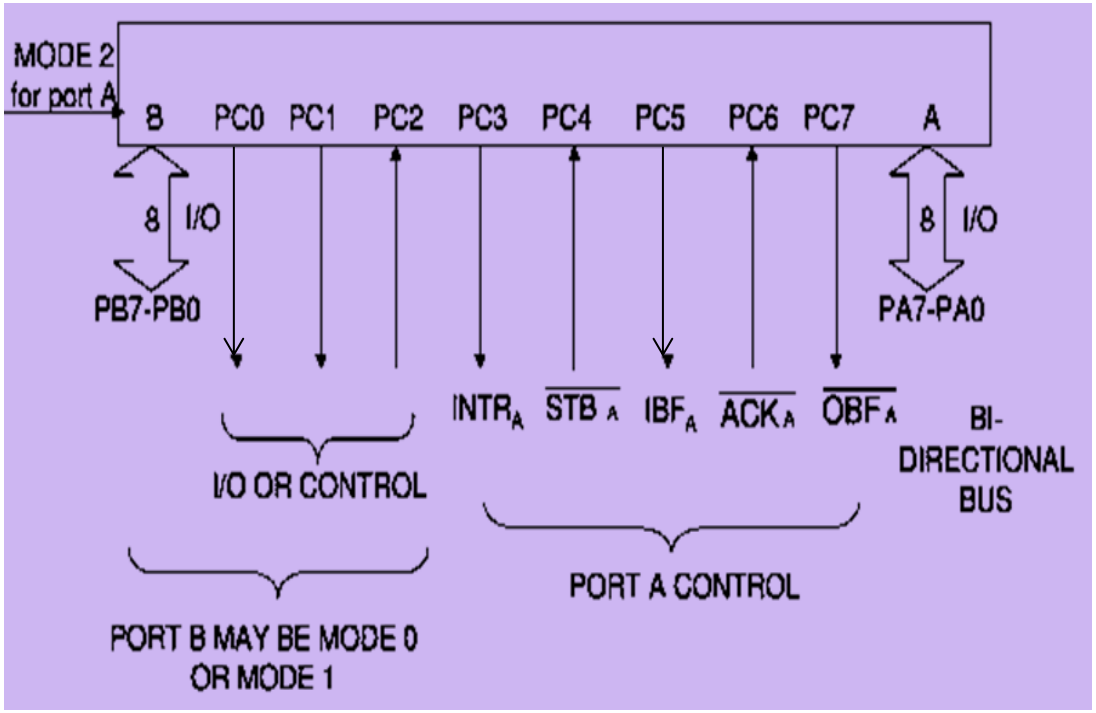


Connection of Handshaking lines when Port A and Port B configured as Output in Mode 1

I/O Mode (Cont.)

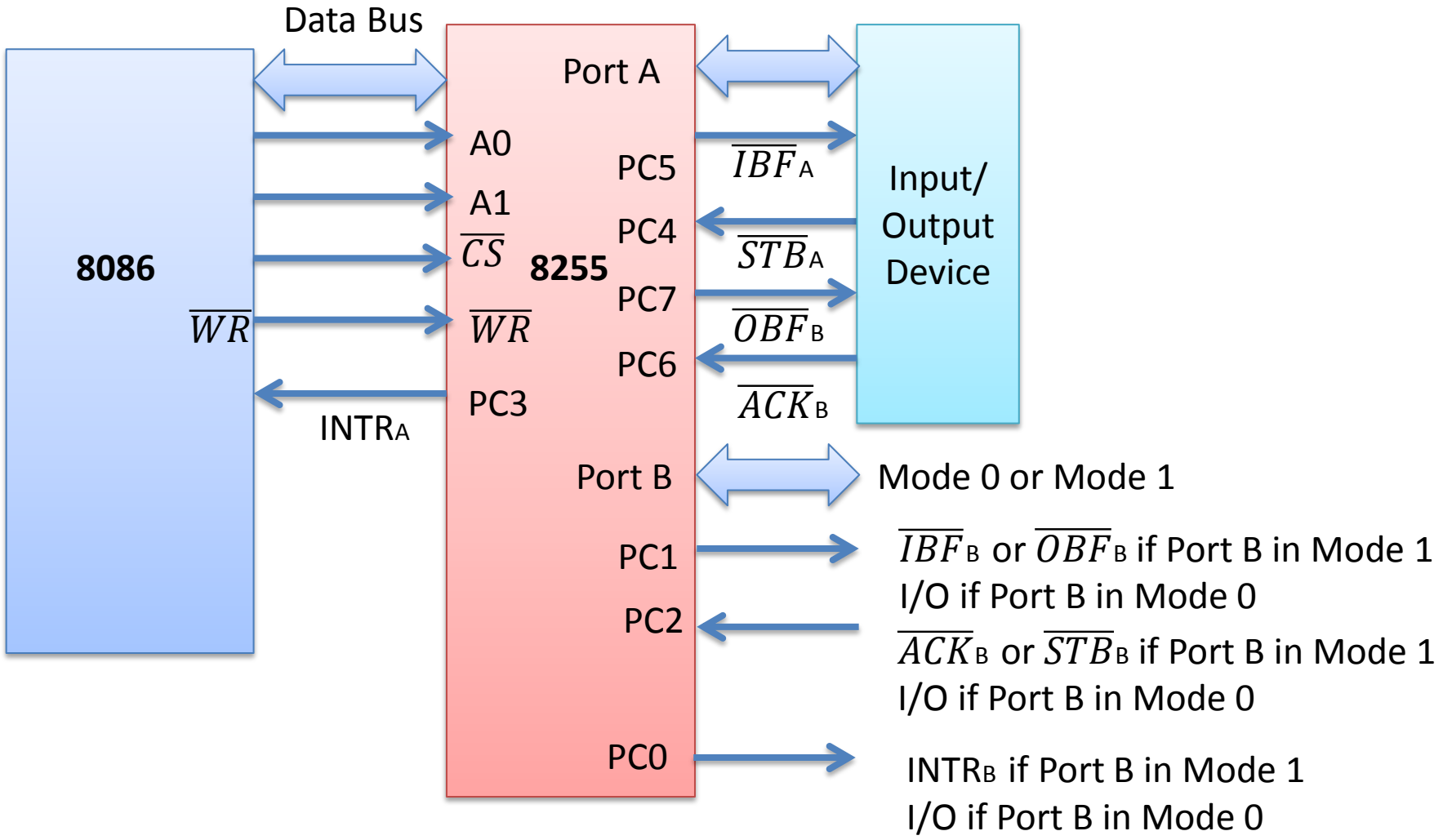
Mode 2

- Only port A can be initialized in mode 2.
- In mode 2, port A can be used for “bi-directional handshake” data transfer i.e. data can be input or output on the same eight lines.
- Pins PC3, PC4, PC5, PC6, PC7 used as handshake lines for port A.
- Port B is operating in either mode 0 or mode 1.
- If port B is in mode 0, then PC0, PC1 and PC2 used for I/O.
- If port B is in mode 1, then PC0, PC1 and PC2 used as handshake lines.



I/O Mode (Cont.)

Handshaking Lines in Mode 2



I/O Mode (Cont.)

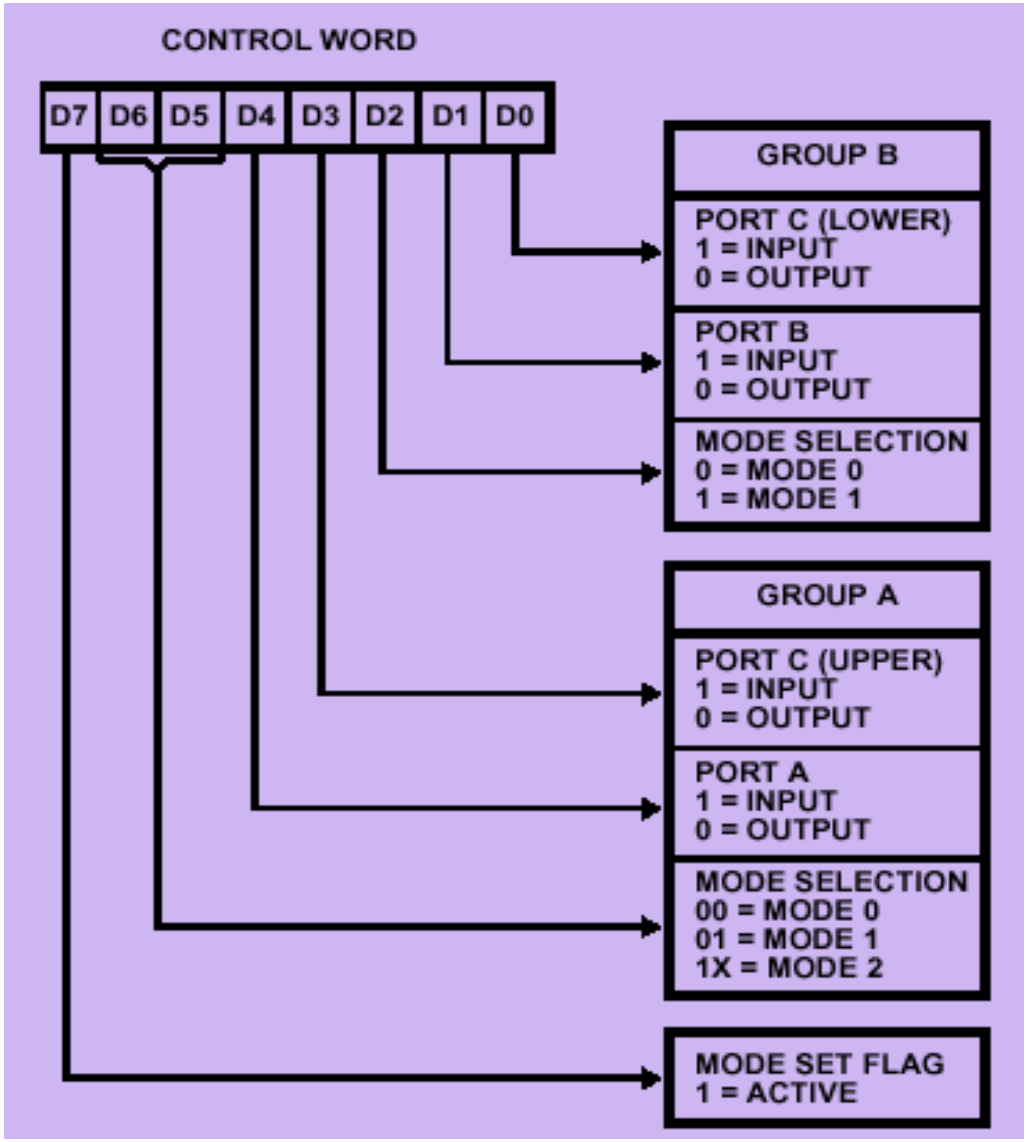
8255A modes summarization

Mode	8- Bit Port A	8-Bit Port B	Handshake lines for mentioned Mode	Other Port C pins available for I/O
0	I/O	I/O	N/A	PC7- PC4 and PC3- PC0
1	Input	I/O	PC3, PC4, PC5 (Port A) PC0, PC1, PC2 (Port B)	PC6, PC7
1	Output	I/O	PC3, PC6, PC7 (Port A) PC0, PC1, PC2 (Port B)	PC4, PC5
2	Bi-Directional	N/A	PC3, PC4, PC5, PC6, PC7	PC0, PC1, PC2 (If Port B in Mode 0)

I/O Mode (Cont.)

Configuring I/O Mode

I/O Mode is configured by Mode Definition Control Word



Problems

Problem1: Write a control word to configure port A as input port in mode 0 and port B in mode 1 as output port.

Solution:

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	1	0	0

The control word is 94H.

N.B. D0 and D3 are low if port C is used as output or if unused.

Problem 2: A control word is given CW=CDH. Explain the conditions of ports of 8255A.

Solution:

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	1	1	0	1

D7=1; I/O Mode.
D6=1 and D5=0; Port A is in Mode 2.
D4=0; Port A is output port
D3=1; Port C (Upper) is input port.
D2=1; Port B is in Mode 1.
D1=0; Port B is output Port.
D0=0; Port C (Lower) is input port.

Q3: Configure Port A in Mode 2, Port B as o/p in mode 1.

Problems

Problem 3: Configure Port A in Mode 2, Port B as o/p in mode 1.

Solution:

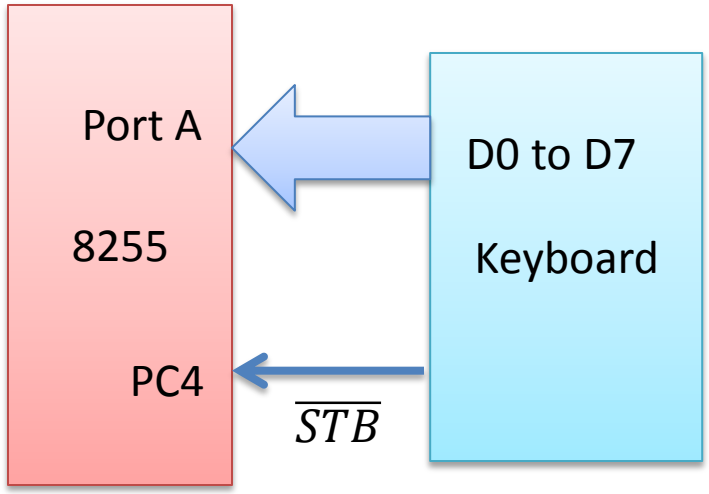
D7	D6	D5	D4	D3	D2	D1	D0
1	1	X	X	X	1	0	X

Control word is C4H / C5H….. etc

Problem 4: Write an 8086 assembly language procedure to read an ASCII character from a keyboard via PORT A of an 8255 PPI when PORT C bit PC4 is strobed low. Assume a base address of 20H.

Solution:

```
   PORTA      EQU   20H
   PORTC      EQU   22H
   CONTROL  EQU    23H
READ PROC NEAR
   MOV AL, 98H    ; 1001 1000
   OUT CONTROL, AL    ; Initialize PORTS
READ1:
   IN AL, PORTC    ; Is Strobe PC4 Low?
   TEST AL, 10H    ; 0001 0000
   JNZ READ1
   IN AL, PORTA    ; Read ASCII Character
   RET
READ ENDP
```

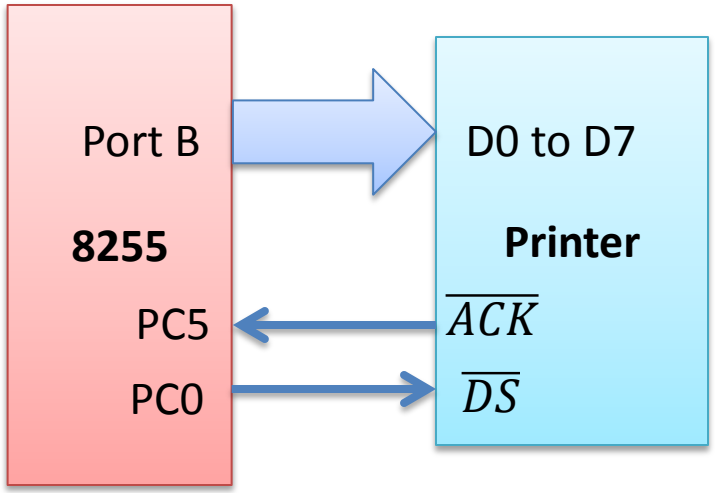


Problems

Problem 5: Write an 8086 assembly language procedure to send an ASCII character, stored in register AH, to a printer via PORT B of an 8255 PPI when PORTC bit PCO is strobed low and after an active low acknowledge signal is detected on PORT C bit PC5 from the printer. Assume a base address of 60H.

Solution:

```
   PORTB   EQU   61H
   PORTC   EQU   62H
   CONTROL   EQU 63H
PRINT PROC NEAR
   MOV AL, 88H    ; 1000 1000
   OUT CONTROL, AL;
PRINT1:
   IN AL, PORTC    ; Is Acknowledge PC5 Low?
   TEST AL, 20H    ; 0010 000
   JNZ PRINT1
   MOV AL, AH    ; Send character
   OUT PORTB, AL;
   MOV AL, FEH   ; 1111 1110
   OUT PORTC, AL    ; strobe output PC0
   RET
PRINT ENDP
```



Problems

Problem 6: An 8086-8255 based microcomputer is required to drive an LED connected to bit 2 of Port B based on two switch inputs connected to bit 6 and 7 of port A. If both switches are either high or low, LED will turn on ; otherwise, it will remain OFF. Assume base address of 60H . Write an 8086 assembly language program to accomplish this.

Solution:

```
PORTA    EQU    60H
PORTB    EQU    61H
CONTR    EQU   63H
MOV AL, 10010000B; Configure Port A as input and Port B as output.
OUT CNTRL, AL;
MAIN : IN  AL, PORTA;
          AND AL, 11000000B;
          JPE  LEADON;   (JPE= Jump if parity even, p=1)
          MOV AL, 00H;
         OUT PORTB, AL;
         JMP  MAIN;
LEDON : MOV  AL, 00000100B;
           OUT PORTB, AL;
           JMP  MAIN;
```

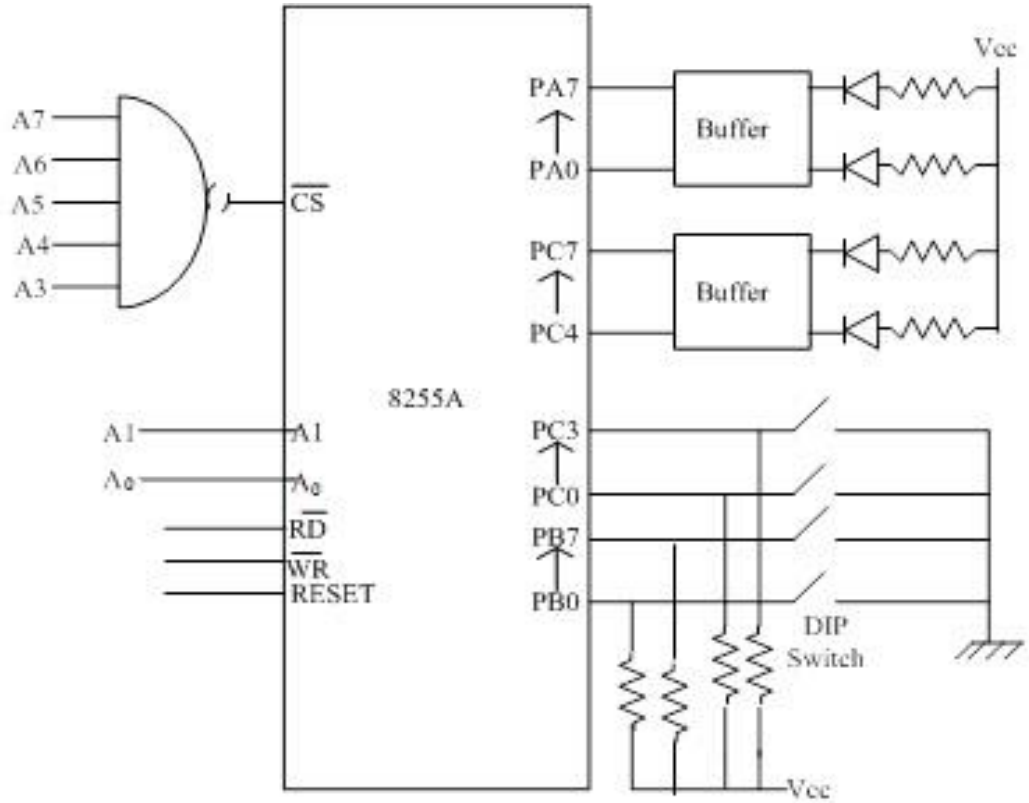
Problems

Problem 7: Figure shows an 8255A interfaced with 8086 microprocessor. Perform the following-

(a) Identify the Port Address.

(b) Identify the Mode 0 control word to configure Port A and Port C_U as output ports and Port B and Port C_L as input ports.

(c) Write a program to read the DIP switches and display the reading from Port B at Port A, and from Port C_L at Port C_U.



Problems

Solution of problem 7:

(a) When A3 to A7 are high then chip select ($\overline{CS}$) is enabled.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address of Port
0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	00F8H (Port A)
0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	1	00F9H (Port B)
0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	00FAH (Port C)
0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	00FBH (CR)

(b) Control Word

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	1
Mod Set	Port A in Mode 0		Port A I/O	Port C upper o/p	Port B in Mode 0	Port B input	Port C lower input

Control Word = 83 H

Problems

Solution of problem 7(c)

Program

```
PPICR   EQU  00FBH
PPIC    EQU  00FAH
PPIB    EQU  00F9H
PPIA    EQU  00F8H
MOV AL, 83H
OUT  PPICR , AL
IN AL, PPIB
OUT PPIA, AL
IN AL, PPIC
AND AL, 0FH
MOV CL, 04H
ROL  AL, CL
OUT PPIC, AL
HLT
```

OR

Solution of problem 7(c)

Program

```
PPICR   EQU  00FBH
PPIC    EQU  00FAH
PPIB    EQU  00F9H
PPIA    EQU  00F8H
MOV AL, 83H
OUT  PPICR , AL
IN AL, PPIB
OUT PPIA, AL
IN AL, PPIC
MOV CL, 04H
SHL  AL, CL
OUT PPIC, AL
HLT
```

Problems

Problem 8:

Write a BSR control word subroutine to set bit PC7 and PC3 and reset them after 10ms. Use the previous schematic (Figure of problem 7). Also write the delay procedure considering the processor clock at 5 MHz

Solution:

BSR Control Word:

	D7	D6	D5	D4	D3	D2	D1	D0	Control Word
To set Bit PC7	0	0	0	0	1	1	1	1	0FH
To reset PC7	0	0	0	0	1	1	1	0	0EH
To set PC3	0	0	0	0	0	1	1	1	07H
To reset PC3	0	0	0	0	0	1	1	0	06H

Address of control register: 8003H (See previous problem)

Duration of 1 clock pulse= (1/5MHz) = 200 ns

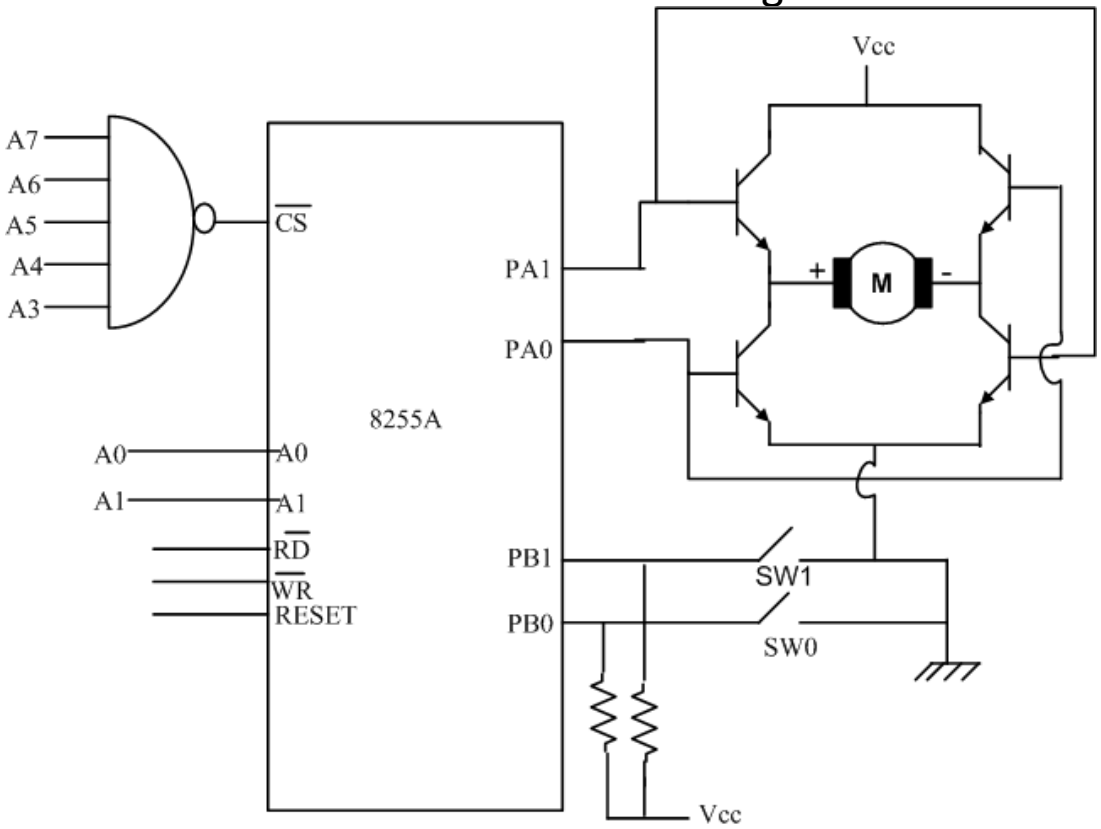
So, for 10ms we have to count = (10ms/200ns) = 50,000

Subroutine:

```
PPICR EQU 8003H
BSR: MOV AL, 0FH
     OUT  PPICR, AL
     MOV AL, 07H
     OUT PPICR, AL
     CALL DELAY
     MOV AL, 06H
     OUT PPICR, AL
     MOV AL, 0EH
     OUT PPICR, AL
     RET
DELAY  PROC  NEAR
MOV CX, 50,000
HERE: LOOP HERE
RET
DELAY  ENDP
```

Problems

Problem 9: Write an assembly language instruction set to drive the DC motor interfaced with 8086 microprocessor as shown in figure. The switches SW0 and SW1 control the motor status according to the table.



SW1	SW0	Motor status
OFF	OFF	No rotation
OFF	ON	Forward rotation
ON	OFF	Reverse rotation
ON	ON	No rotation

Solution:

D7	D6	D5	D4	D3	D2	D1	D0	Control Word
1	0	0	0	0	0	1	0	82H

Problems

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address of Port
0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	00F8H (Port A)
0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	1	00F9H (Port B)
0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	00FAH (Port C)
0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	00FBH (CR)

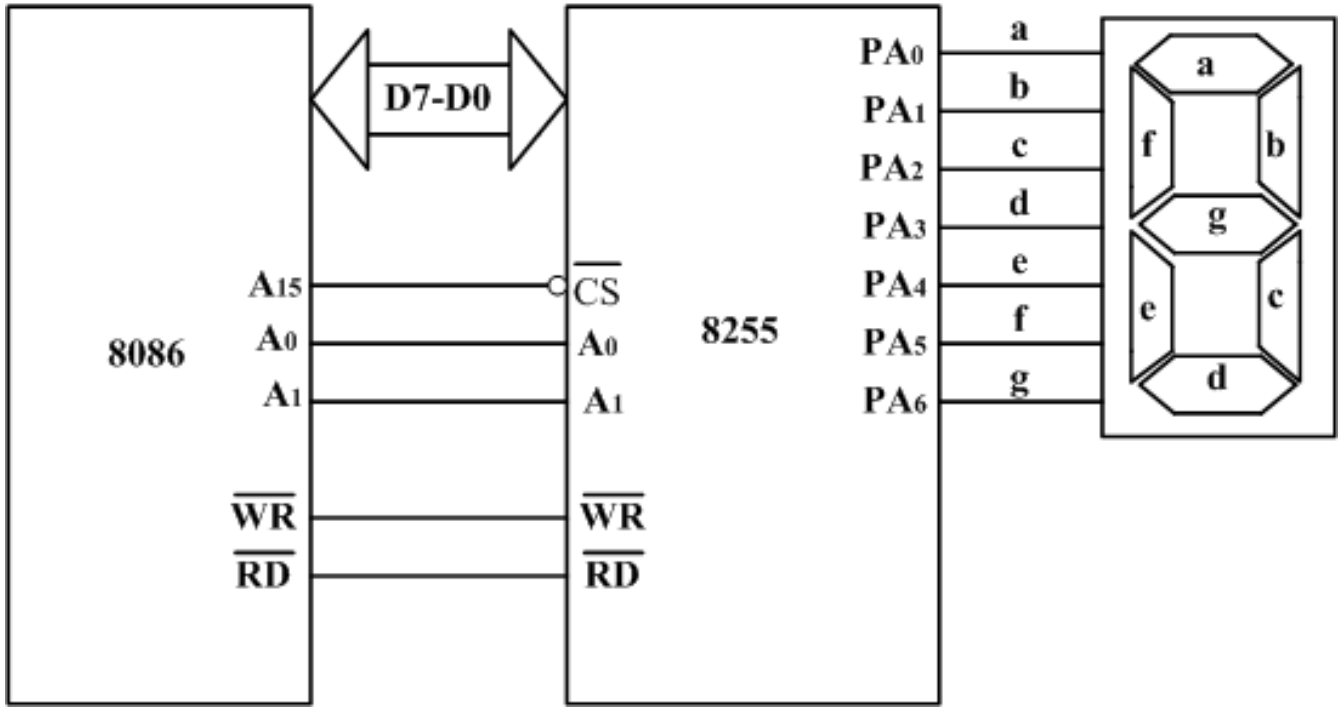
```
PORTA   EQU   00F8H
PORTB   EQU   00F9H
CONTR   EQU   00FBH
MOV AL, 82H
OUT CNTRL, AL;    Control word sent to CR
MAIN : IN  AL, PORTB;
          AND AL, 00000011B;  Check switch
          JPE  STOP;   (JPE=Jump if parity even, p=1)
; if two switches are on or off, parity will be even

TEST AL, 00000001B; check whether SW0 is on or off
 JZ FORWARD  ; if SW0 is on, result becomes zero (Z=1)
 MOV AL, 00000001B;
 OUT  PORTA, AL; motor rotate reverse direction
 JMP  MAIN;
```

```
STOP : MOV  AL, 00000000B;
          OUT PORTA, AL;
          JMP  MAIN;

FORWARD: MOV AL, 00000010
            OUT  PORTA, AL
            JMP MAIN
```

Assignment-1: A 8086-8255A based system is given in fig. The Port A of 8255A is connected with a 7-segment display. Write an assembly language program to display the numbers 1,3,5,7,9 repeatedly



Assignment-2: An 8X8 dot matrix LED display is connected to 8255-8086 based system. The rows of the display are connected to PORTA and columns to PORTB as shown in Figure. A. The internal circuit of the dot matrix display is shown in Figure. B. Write an assembly language program to show Bengali number “1” on the display. Assume that the addresses of PORTA, PORTB and control register are 60H, 61H and 63H respectively.

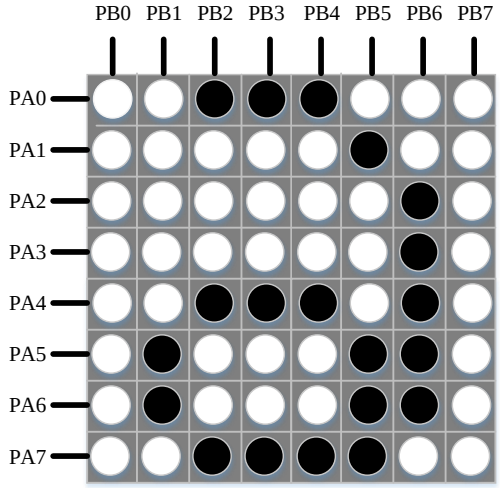


Figure. A.

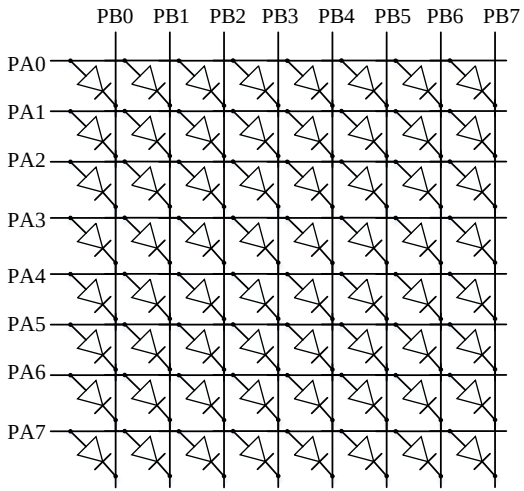


Figure. B.