CO-Basic

Total points 7/10

The respondent's email address (**u19cs012@coed.svnit.ac.in**) was recorded on submission of this form.

Step to read new instruction from the memory is called * 1/1

- (•) Fetch
- ( ) Decode
- ( ) Execute
- ( ) None of these

Step to execute the operation specified by the instruction is called * 1/1

- ( ) Fetch
- ( ) Decode
- (•) Execute
- ( ) None of these

The control memory contains a set of words where each word is * 1/1

- ( ) program
- ( ) sets
- (•) microinstruction
- ( ) all of these

A type of processor designed with limited number of instructions is called * 1/1

- ( ) CPU
- ( ) CISC
- (•) RISC
- ( ) None of these

A type of processor designed with more number of instructions, addressing mode, address range and variable length instruction is called * 1/1

- [ ] CPU
- [x] CISC
- [ ] RISC
- [ ] None of these

The instruction set can have variable length instruction format primarily due to * 0/1

- [x] varying number of operands
- [ ] varying length of opcodes
- [ ] both of these
- [ ] none of these

The addressing mode of branch instruction is known as * 1/1

- [ ] Immediate Addressing Mode
- [ ] Pseudo-Direct Addressing Mode
- [x] PC-Relative Addressing Mode
- [ ] none of these

The addressing mode of Jump instruction is known as * 1/1

- [ ] Immediate Addressing Mode
- [x] Pseudo-Direct Addressing Mode
- [ ] PC-Relative Addressing Mode
- [ ] none of these

The address calculation of branch instruction is done in which stage of MIPS multi cycle processor * 0/1

- [ ] IF
- [ ] ID
- [x] EX
- [ ] MEM

The address calculation of Jump instruction is done in which stage of MIPS multi cycle processor * 0/1

- [ ] IF
- [ ] ID
- [x] EX
- [ ] MEM