4 DC Biasing—BJTs

CHAPTER OBJECTIVES

- Be able to determine the dc levels for the variety of important BJT configurations.
- Understand how to measure the important voltage levels of a BJT transistor configuration and use them to determine whether the network is operating properly.
- Become aware of the saturation and cutoff conditions of a BJT network and the expected voltage and current levels established by each condition.
- Be able to perform a load-line analysis of the most common BJT configurations.
- Become acquainted with the design process for BJT amplifiers.
- Understand the basic operation of transistor switching networks.
- Begin to understand the troubleshooting process as applied to BJT configurations.
- Develop a sense for the stability factors of a BJT configuration and how they affect its operation due to changes in specific characteristics and environmental changes.

4.1 INTRODUCTION

The analysis or design of a transistor amplifier requires a knowledge of both the dc and the ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality,

any increase in ac voltage, current, or power is the result of a transfer of energy from the applied dc supplies.

The analysis or design of any electronic amplifier therefore has two components: a dc and an ac portion. Fortunately, the superposition theorem is applicable, and the investigation of the dc conditions can be totally separated from the ac response. However, one must keep in mind that during the design or synthesis stage the choice of parameters for the required dc levels will affect the ac response, and vice versa.

The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. In Section 4.2 we specify the range for the bipolar junction transistor (BJT) amplifier. Once the desired dc current and voltage levels have been defined, a network must be constructed that will establish the desired operating point. A number of these networks are analyzed in this chapter. Each design will also determine the stability of the system, that is, how sensitive the system is to temperature variations, another topic to be investigated in a later section of this chapter.

Although a number of networks are analyzed in this chapter, there is an underlying similarity in the analysis of each configuration due to the recurring use of the following important basic relationships for a transistor:

$$V_{BE} \cong 0.7\ \text{V} \tag{4.1}$$

$$I_E = (\beta + 1)I_B \cong I_C \tag{4.2}$$

$$I_C = \beta I_B \tag{4.3}$$

In fact, once the analysis of the first few networks is clearly understood, the path toward the solution of the networks to follow will begin to become quite apparent. In most instances the base current I_B is the first quantity to be determined. Once I_B is known, the relationships of Eqs. (4.1) through (4.3) can be applied to find the remaining quantities of interest. The similarities in analysis will be immediately obvious as we progress through the chapter. The equations for I_B are so similar for a number of configurations that one equation can be derived from another simply by dropping or adding a term or two. The primary function of this chapter is to develop a level of familiarity with the BJT transistor that would permit a dc analysis of any system that might employ the BJT amplifier.

4.2 OPERATING POINT

The term *biasing* appearing in the title of this chapter is an all-inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an *operating point* on the characteristics that define the region that will be employed for amplification of the applied signal. Because the operating point is a fixed point on the characteristics, it is also called the *quiescent point* (abbreviated *Q*-point). By definition, *quiescent* means quiet, still, inactive. Figure 4.1 shows a general output device characteristic with four operating points indicated. The

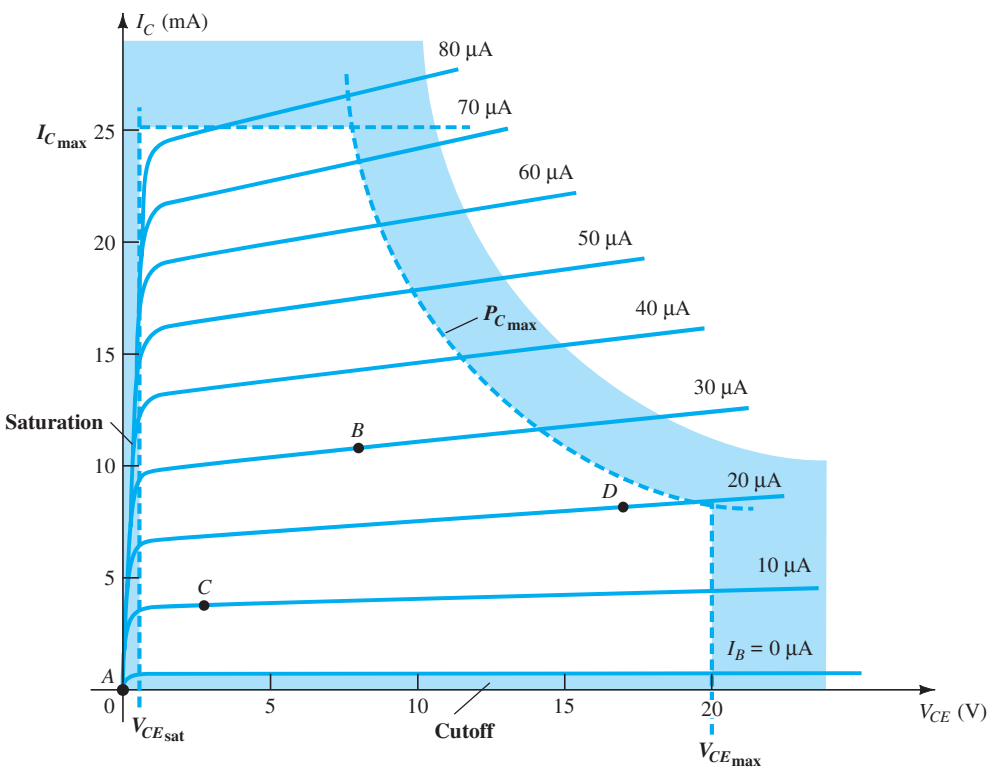

FIG. 4.1
Various operating points within the limits of operation of a transistor.

2. *Cutoff-region operation:*
   Base–emitter junction reverse-biased
   Base–collector junction reverse-biased
3. *Saturation-region operation:*
   Base–emitter junction forward-biased
   Base–collector junction forward-biased

4.3 FIXED-BIAS CONFIGURATION

The fixed-bias circuit of Fig. 4.2 is the simplest transistor dc bias configuration. Even though the network employs an *npn* transistor, the equations and calculations apply equally well to a *pnp* transistor configuration merely by changing all current directions and voltage polarities. The current directions of Fig. 4.2 are the *actual* current directions, and the voltages are defined by the standard double-subscript notation. For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open-circuit equivalent because the reactance of a capacitor is a function of the applied frequency. For dc, $f = 0$ Hz, and $X_C = \frac{1}{2}\pi fC = \frac{1}{2}\pi(0)C = \infty\,\Omega$. In addition, the dc supply V_{CC} can be separated into two supplies (for analysis purposes only) as shown in Fig. 4.3 to permit a separation of input and output circuits. It also reduces the linkage between the two to the base current I_B. The separation is certainly valid, as we note in Fig. 4.3 that V_{CC} is connected directly to R_B and R_C just as in Fig. 4.2.

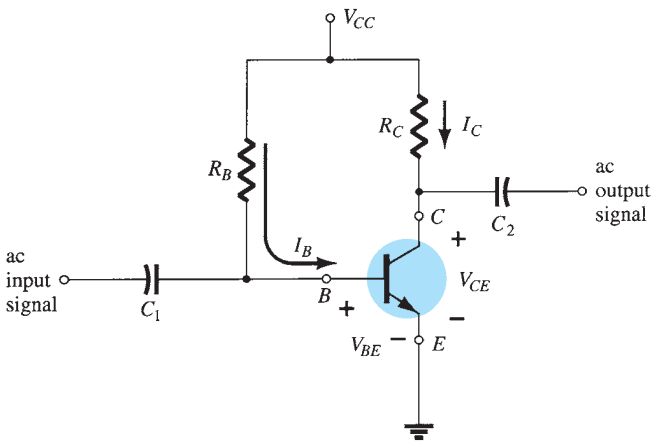

FIG. 4.2
Fixed-bias circuit.

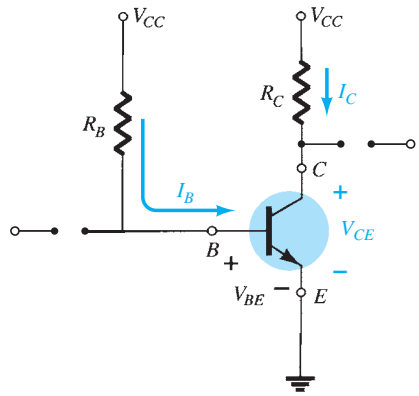

FIG. 4.3
DC equivalent of Fig. 4.2.

Forward Bias of Base–Emitter

Consider first the base–emitter circuit loop of Fig. 4.4. Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Note the polarity of the voltage drop across R_B as established by the indicated direction of I_B. Solving the equation for the current I_B results in the following:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{4.4}$$

Equation (4.4) is certainly not a difficult one to remember if one simply keeps in mind that the base current is the current through R_B and by Ohm's law that current is the voltage across R_B divided by the resistance R_B. The voltage across R_B is the applied voltage V_{CC} at one end less the drop across the base-to-emitter junction (V_{BE}). In addition, because the supply voltage V_{CC} and the base–emitter voltage V_{BE} are constants, the selection of a base resistor R_B sets the level of base current for the operating point.

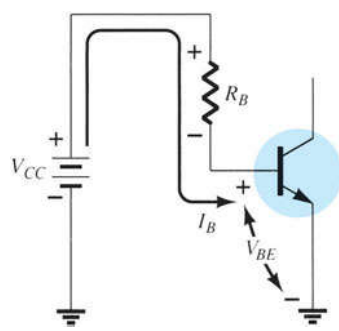

FIG. 4.4
Base–emitter loop.

EXAMPLE 4.3 Given the load line of Fig. 4.16 and the defined Q-point, determine the required values of V_{CC}, R_C, and R_B for a fixed-bias configuration.

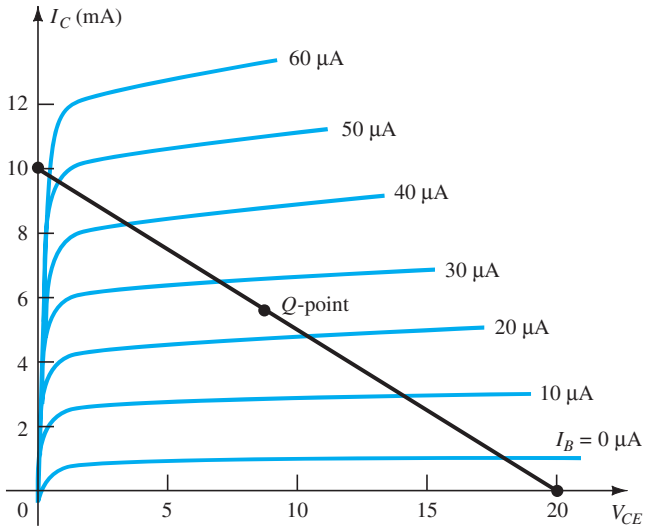

FIG. 4.16
Example 4.3.

Solution: From Fig. 4.16,

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0\ \text{mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0\ \text{V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ \text{V}}{10\ \text{mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\ \text{V} - 0.7\ \text{V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

4.4 EMITTER-BIAS CONFIGURATION

The dc bias network of Fig. 4.17 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration. The more stable a configuration, the less its response will change due to undesireable changes in temperature and parameter

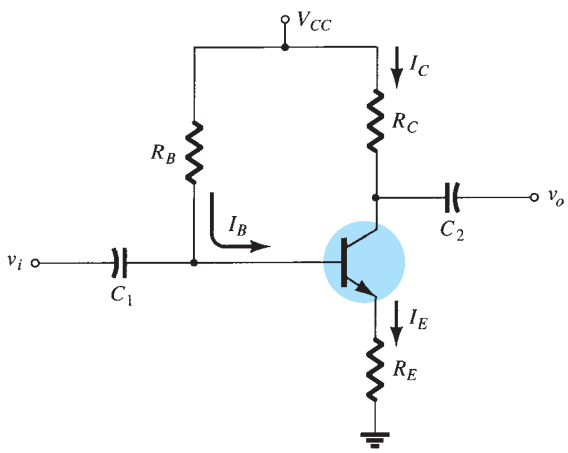

FIG. 4.17
BJT bias circuit with emitter resistor.

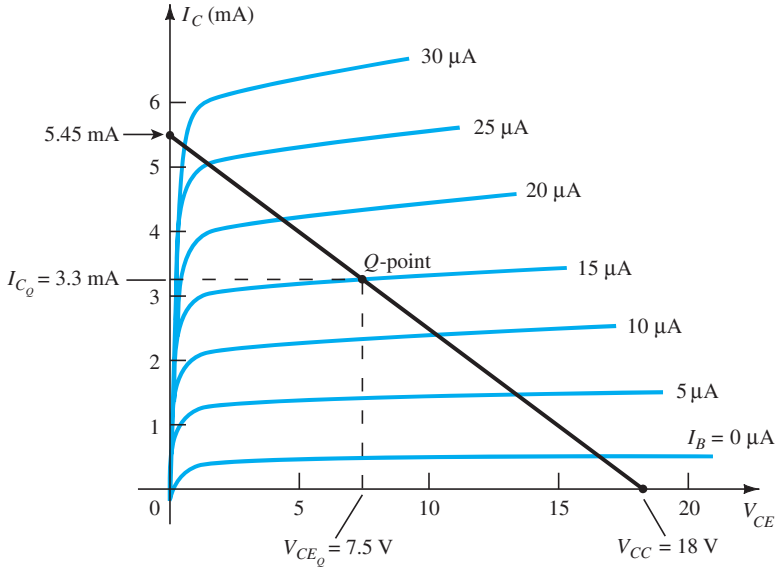

FIG. 4.27
Example 4.7.

d. Applying Eq. 4.17:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{18\text{ V} - 0.7\text{ V}}{R_B + (220 + 1)(1.1\text{ k}\Omega)}$$

$$\text{and } 15\ \mu\text{A} = \frac{17.3\text{ V}}{R_B + (221)(1.1\text{ k}\Omega)} = \frac{17.3\text{ V}}{R_B + 243.1\text{ k}\Omega}$$

$$\text{so that } (15\ \mu\text{A})(R_B) + (15\ \mu\text{A})(243.1\text{ k}\Omega) = 17.3\text{ V}$$

$$\text{and } (15\ \mu\text{A})(R_B) = 17.3\text{ V} - 3.65\text{ V} = 13.65\text{ V}$$

$$\text{resulting in } R_B = \frac{13.65\text{ V}}{15\ \mu\text{A}} = \mathbf{910\ k\Omega}$$

4.5 VOLTAGE-DIVIDER BIAS CONFIGURATION

In the previous bias configurations the bias current I_{C_Q} and voltage V_{CE_Q} were a function of the current gain β of the transistor. However, because β is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent on, or in fact is independent of, the transistor beta. The voltage-divider bias configuration of Fig. 4.28 is such a network. If analyzed on an exact basis, the sensitivity to changes in beta is quite small. If the circuit parameters are properly chosen, the resulting levels of I_{C_Q} and V_{CE_Q} can be almost totally independent of beta. Recall from previous discussions that a Q-point is defined by a fixed level of I_{C_Q} and V_{CE_Q} as shown in Fig. 4.29. The level of I_{B_Q} will change with the change in beta, but the operating point on the characteristics defined by I_{C_Q} and V_{CE_Q} can remain fixed if the proper circuit parameters are employed.

As noted earlier, there are two methods that can be applied to analyze the voltage-divider configuration. The reason for the choice of names for this configuration will become obvious in the analysis to follow. The first to be demonstrated is the *exact method*, which can be applied to *any* voltage-divider configuration. The second is referred to as the *approximate method* and can be applied only if specific conditions are satisfied. The approximate approach permits a more direct analysis with a savings in time and energy. It is also particularly helpful in the design mode to be described in a later section. All in all, the approximate approach can be applied to the majority of situations and therefore should be examined with the same interest as the exact method.

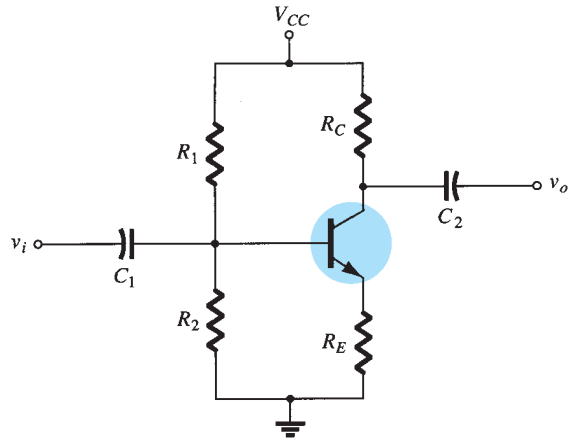

FIG. 4.28
Voltage-divider bias configuration.

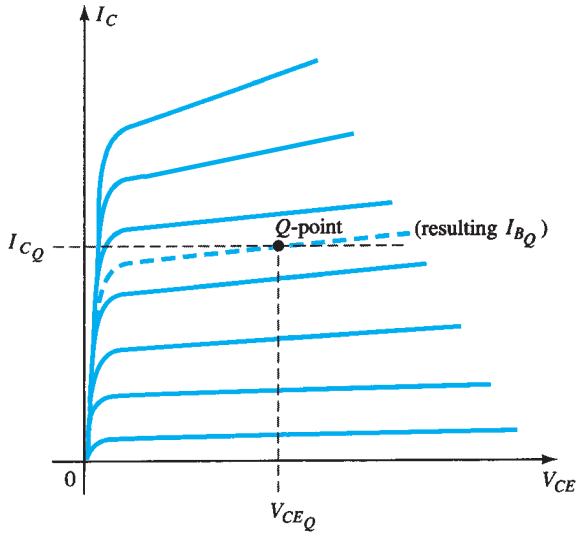

FIG. 4.29
Defining the Q-point for the voltage-divider bias configuration.

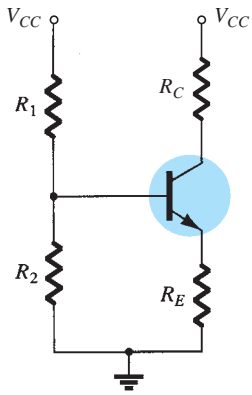

FIG. 4.30
DC components of the voltage-divider configuration.

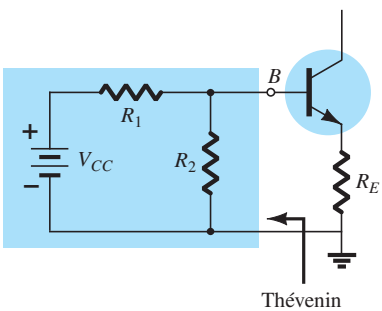

FIG. 4.31
Redrawing the input side of the network of Fig. 4.28.

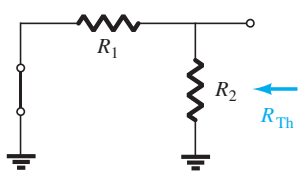

FIG. 4.32
Determining R_{Th}.

Exact Analysis

For the dc analysis the network of Fig. 4.28 can be redrawn as shown in Fig. 4.30. The input side of the network can then be redrawn as shown in Fig. 4.31 for the dc analysis. The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:

***R*Th** The voltage source is replaced by a short-circuit equivalent as shown in Fig. 4.32:

$$R_{\text{Th}} = R_1 \| R_2 \tag{4.28}$$

***E*Th** The voltage source V_{CC} is returned to the network and the open-circuit Thévenin voltage of Fig. 4.33 determined as follows:

Applying the voltage-divider rule gives

$$E_{\text{Th}} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2} \tag{4.29}$$

The Thévenin network is then redrawn as shown in Fig. 4.34, and I_{B_Q} can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated:

$$E_{\text{Th}} - I_B R_{\text{Th}} - V_{BE} - I_E R_E = 0$$

Substituting $I_E = (\beta + 1)I_B$ and solving for I_B yields

$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E} \tag{4.30}$$

Although Eq. (4.30) initially appears to be different from those developed earlier, note that the numerator is again a difference of two voltage levels and the denominator is the base resistance plus the emitter resistor reflected by $(\beta + 1)$—certainly very similar to Eq. (4.17).

Once I_B is known, the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is,

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \tag{4.31}$$

which is exactly the same as Eq. (4.19). The remaining equations for V_E, V_C, and V_B are also the same as obtained for the emitter-bias configuration.

Tabulating the results, we have:

Comparing the exact and approximate approaches.

	I_{C_Q} (mA)	V_{CE_Q} (V)
Exact	1.98	4.54
Approximate	2.59	3.88

The results reveal the difference between exact and approximate solutions. I_{C_Q} is about 30% greater with the approximate solution, whereas V_{CE_Q} is about 10% less. The results are notably different in magnitude, but even though βR_E is only about three times larger than R_2, the results are still relatively close to each other. For the future, however, our analysis will be dictated by Eq. (4.33) to ensure a close similarity between exact and approximate solutions.

Transistor Saturation

The output collector–emitter circuit for the voltage-divider configuration has the same appearance as the emitter-biased circuit analyzed in Section 4.4. The resulting equation for the saturation current (when V_{CE} is set to 0 V on the schematic) is therefore the same as obtained for the emitter-biased configuration. That is,

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E} \tag{4.38}$$

Load-Line Analysis

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of Fig. 4.25, with

$$I_C = \left.\frac{V_{CC}}{R_C + R_E}\right|_{V_{CE}=0\text{ V}} \tag{4.39}$$

and

$$V_{CE} = V_{CC}|_{I_C=0\text{ mA}} \tag{4.40}$$

The level of I_B is of course determined by a different equation for the voltage-divider bias and the emitter-bias configurations.

4.6 COLLECTOR FEEDBACK CONFIGURATION

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig. 4.38. Although the Q-point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations. The analysis will again be performed by first analyzing the base–emitter loop, with the results then applied to the collector–emitter loop.

Base–Emitter Loop

Figure 4.39 shows the base–emitter loop for the voltage feedback configuration. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$$V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0$$

It is important to note that the current through R_C is not I_C, but I'_C (where $I'_C = I_C + I_B$). However, the level of I_C and I'_C far exceeds the usual level of I_B, and the approximation $I'_C \cong I_C$ is normally employed. Substituting $I'_C \cong I_C = \beta I_B$ and $I_E \cong I_C$ results in

$$V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$$

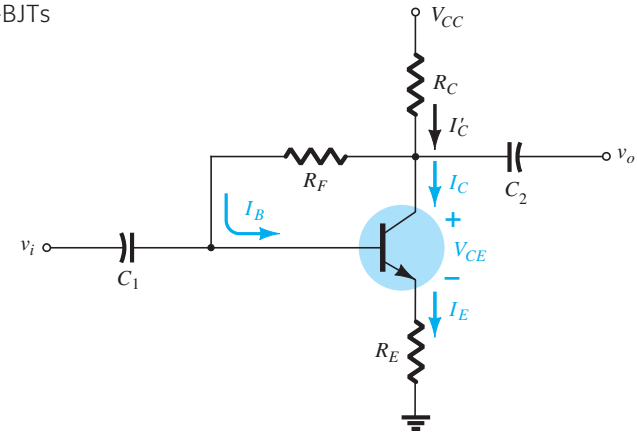

FIG. 4.38
DC bias circuit with voltage feedback.

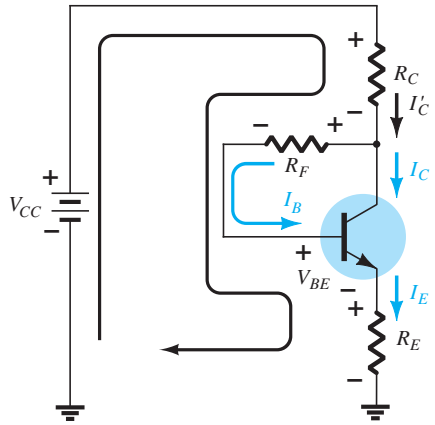

FIG. 4.39
Base–emitter loop for the network of Fig. 4.38.

Gathering terms, we have

$$V_{CC} - V_{BE} - \beta I_B(R_C + R_E) - I_B R_F = 0$$

and solving for I_B yields

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)} \tag{4.41}$$

The result is quite interesting in that the format is very similar to equations for I_B obtained for earlier configurations. The numerator is again the difference of available voltage levels, whereas the denominator is the base resistance plus the collector and emitter resistors reflected by beta. In general, therefore, the feedback path results in a reflection of the resistance R_C back to the input circuit, much like the reflection of R_E.

In general, the equation for I_B has the following format, which can be compared with the result for the fixed-bias and emitter-bias configurations.

$$I_B = \frac{V'}{R_F + \beta R'}$$

For the fixed-bias configuration $\beta R'$ does not exist. For the emitter-bias setup (with $\beta + 1 \cong \beta$), $R' = R_E$.

Because $I_C = \beta I_B$,

$$I_{C_Q} = \frac{\beta V'}{R_F + \beta R'} = \frac{V'}{\frac{R_F}{\beta} + R'}$$

In general, the larger R' is compared with $\frac{R_F}{\beta}$, the more accurate the approximation that

$$I_{C_Q} \cong \frac{V'}{R'}$$

The result is an equation absent of β, which would be very stable for variations in β. Because R' is typically larger for the voltage-feedback configuration than for the emitter-bias configuration, the sensitivity to variations in beta is less. Of course, R' is 0 Ω for the fixed-bias configuration and is therefore quite sensitive to variations in beta.

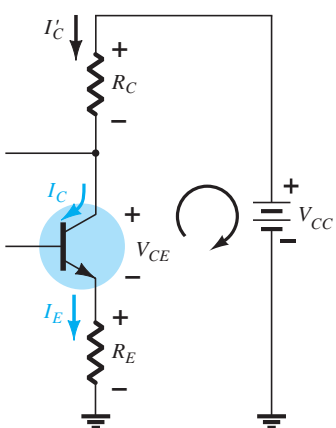

FIG. 4.40
Collector–emitter loop for the network of Fig. 4.38.

Collector–Emitter Loop

The collector–emitter loop for the network of Fig. 4.38 is provided in Fig. 4.40. Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction results in

$$I_E R_E + V_{CE} + I_C' R_C - V_{CC} = 0$$