

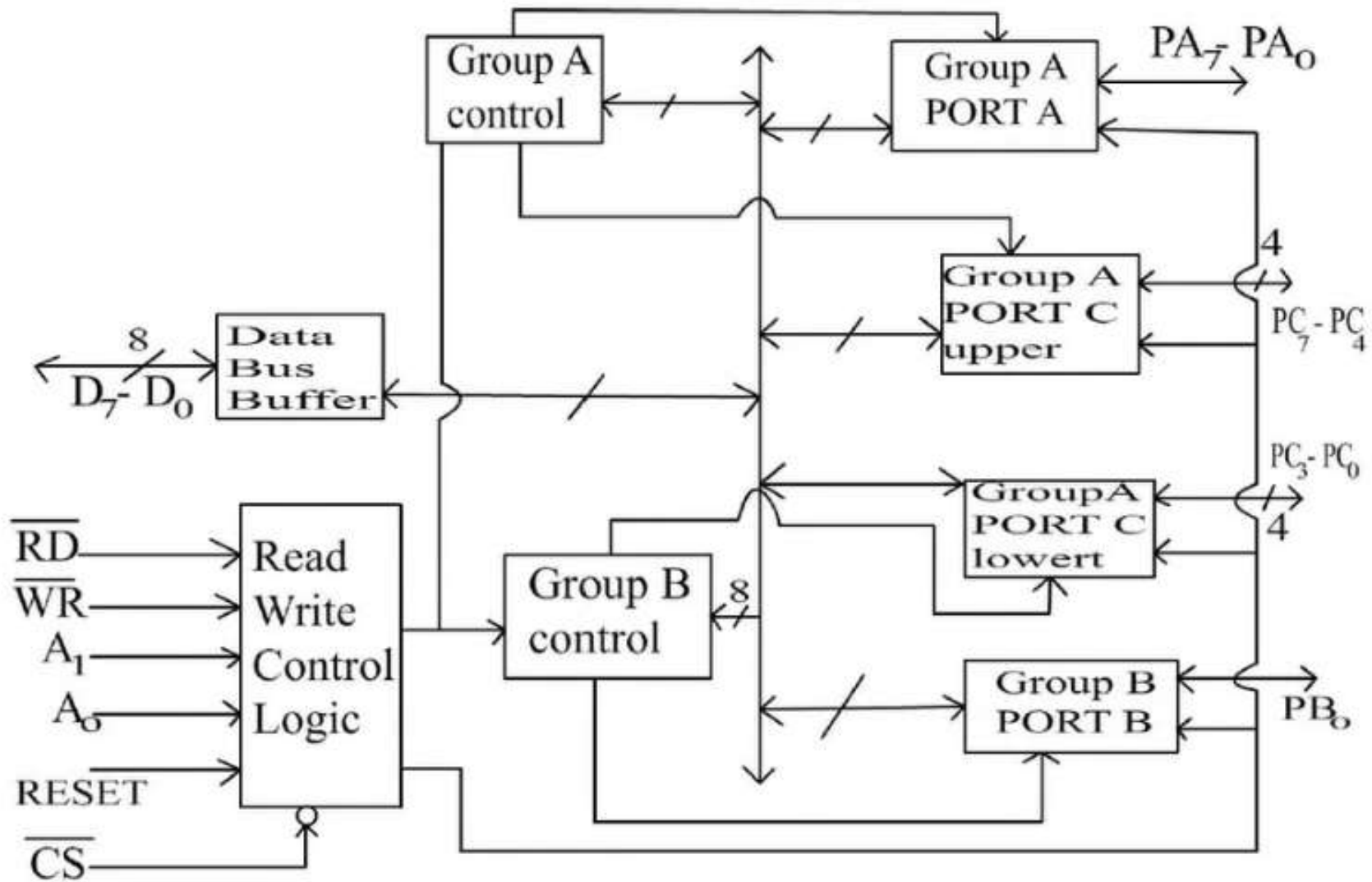
The block diagram is shown below:



PB2 + 20 21 + PB3

GND - Ground

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The 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It consists of three 8-bit bidirectional I/O ports (24 I/O lines) that can be configured to meet different system I/O needs. The three ports are PORT A, PORT B & PORT C. Port A contains one 8-bit output latch/buffer and one 8-bit input buffer. Port B is same as PORT A or PORT B. However, PORT C can be split into two parts PORT C lower ( $PC_0-PC_3$ ) and PORT C upper ( $PC_7-PC_4$ ) by the control word. The three ports are divided in two groups Group A (PORT A and upper PORT C) Group B (PORT B and lower PORT C). The two groups can be programmed in three different modes. In the first mode (mode 0), each group may be programmed in either input mode or output mode (PORT A, PORT B, PORT C lower, PORT C upper). In mode 1, the second's mode, each group may be programmed to have 8-lines of input or output (PORT A or PORT B) of the remaining 4-lines (PORT C lower or PORT C upper) 3-lines are used for hand shaking and interrupt control signals.



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The 8255 is contained in a 40-pin package, whose pin out is shown below:

### Functional Description:

This support chip is a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. It is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

### Data Bus Buffer:

It is a tri-state 8-bit buffer used to interface the chip to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer. The data lines are connected to BDB of  $\mu$ p.

### Read/Write and logic control:

The function of this block is to control the internal operation of the device and to control the transfer of data and control or status words. It accepts inputs from the CPU address and control buses and in turn issues command to both the control groups.

### $\overline{CS}$ Chip Select:

A low on this input selects the chip and enables the communication between the 8255 A & the CPU. It is connected to the output of address decode circuitry to select the device when it  $\overline{RD}$  (Read). A low on this input enables the 8255 to send the data or status information to the CPU on the data bus.

### $\overline{WR}$ (Write):

A low on this input pin enables the CPU to write data or control words into the 8255 A.

### $A_1, A_0$ port select:

These input signals, in conjunction with the  $\overline{RD}$  and  $\overline{WR}$  inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus ( $A_0$  and  $A_1$ ).

Following Table gives the basic operation,

		$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input operation



control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus ( $A_0$  and  $A_1$ ).

Following Table gives the basic operation,

$A_1$	$A_0$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input operation
0	0	0	1	0	PORT A $\longrightarrow$ Data bus
0	1	0	1	0	PORT B $\longrightarrow$ Data bus
1	0	0	1	0	PORT C $\longrightarrow$ Data bus
					<u>Output operation</u>
0	0	1	0	0	Data bus $\longrightarrow$ PORT A
0	1	1	0	0	Data bus $\longrightarrow$ PORT B
1	0	1	0	0	Data bus $\longrightarrow$ PORT C
1	1	1	0	0	Data bus $\longrightarrow$ control

All other states put data bus into tri-state/illegal condition.

**RESET:**



## **Operation Description:**

### **Mode selection:**

There are three basic modes of operation that can be selected by the system software.

Mode 0: Basic Input/output

Mode 1: Strobes Input/output

Mode 2: Bi-direction bus.

When the reset input goes HIGH all ports are set to mode '0' as input which means all 24 lines are in high impedance state and can be used as normal input. After the reset is removed the 8255A remains in the input mode with no additional initialization. During the execution of the program any of the other modes may be selected using a single output instruction.

The modes for PORT A & PORT B can be separately selected while

# Control Word Format for I/O Mode

