DIGITAL ELECTRONICS & LOGIC DESIGN LAB

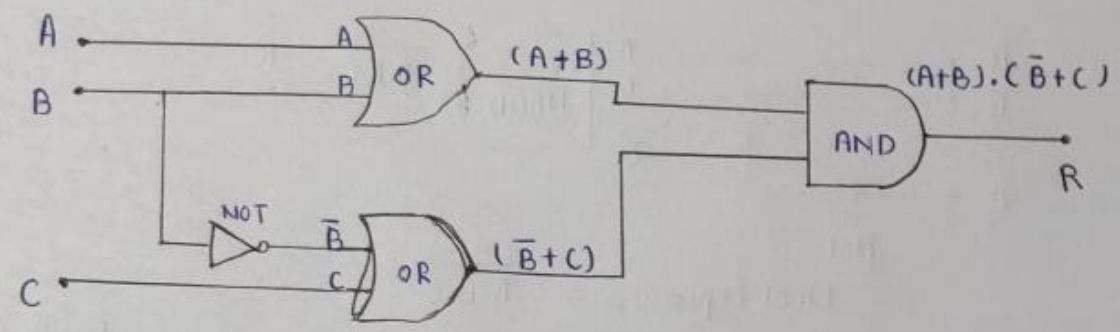
LAB 2 (20 AUG): ASSIGNMENT – LOGIC CIRCUIT

SUBMITTED BY: U19CS012 (D-12)
BHAGYA VINOD RANA | C.S.E., S.V.N.I.T.

Question –1

a.) Calculate the Logic Gates Circuit's Output [Theoretical]

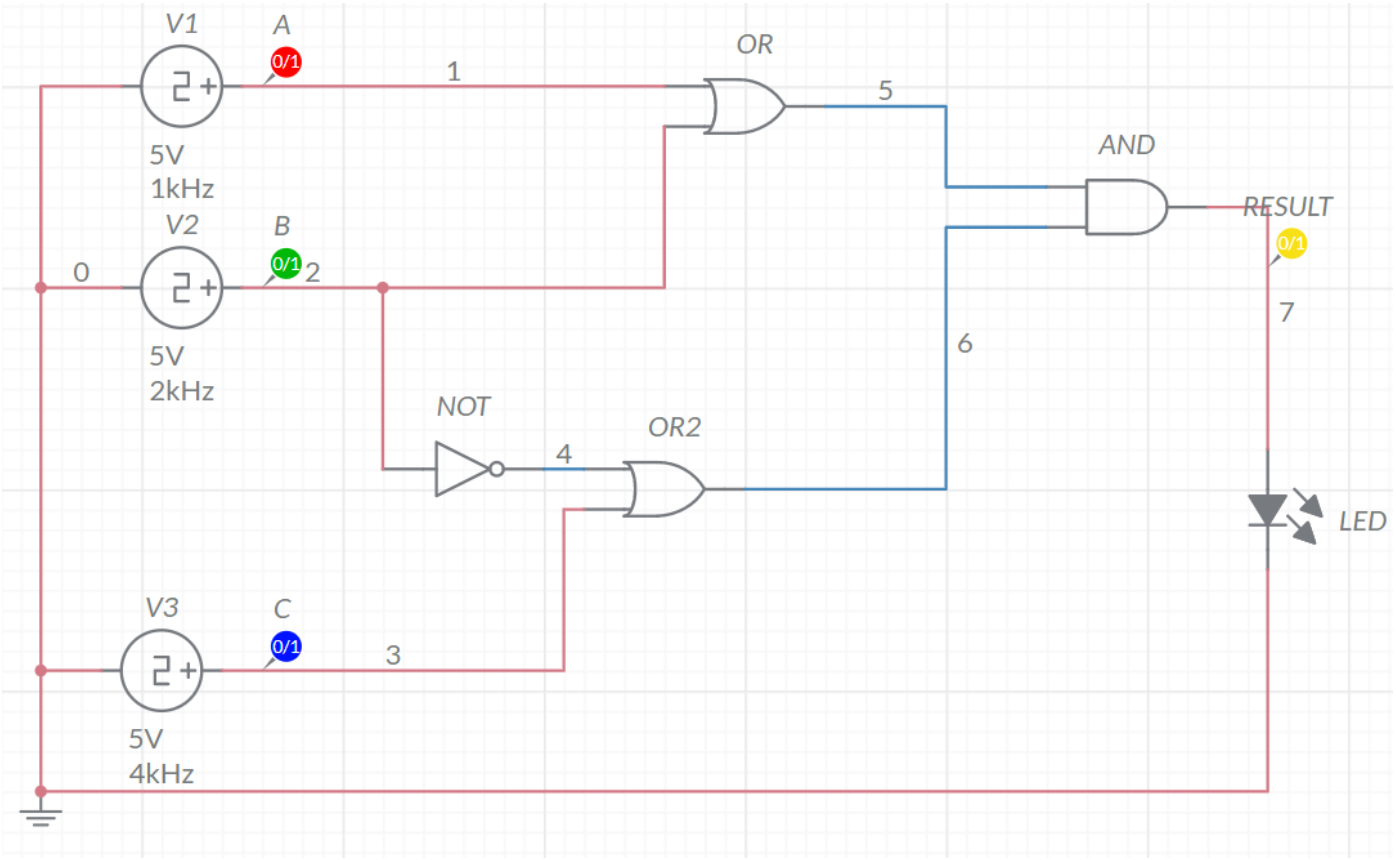
(A) Circuit 1



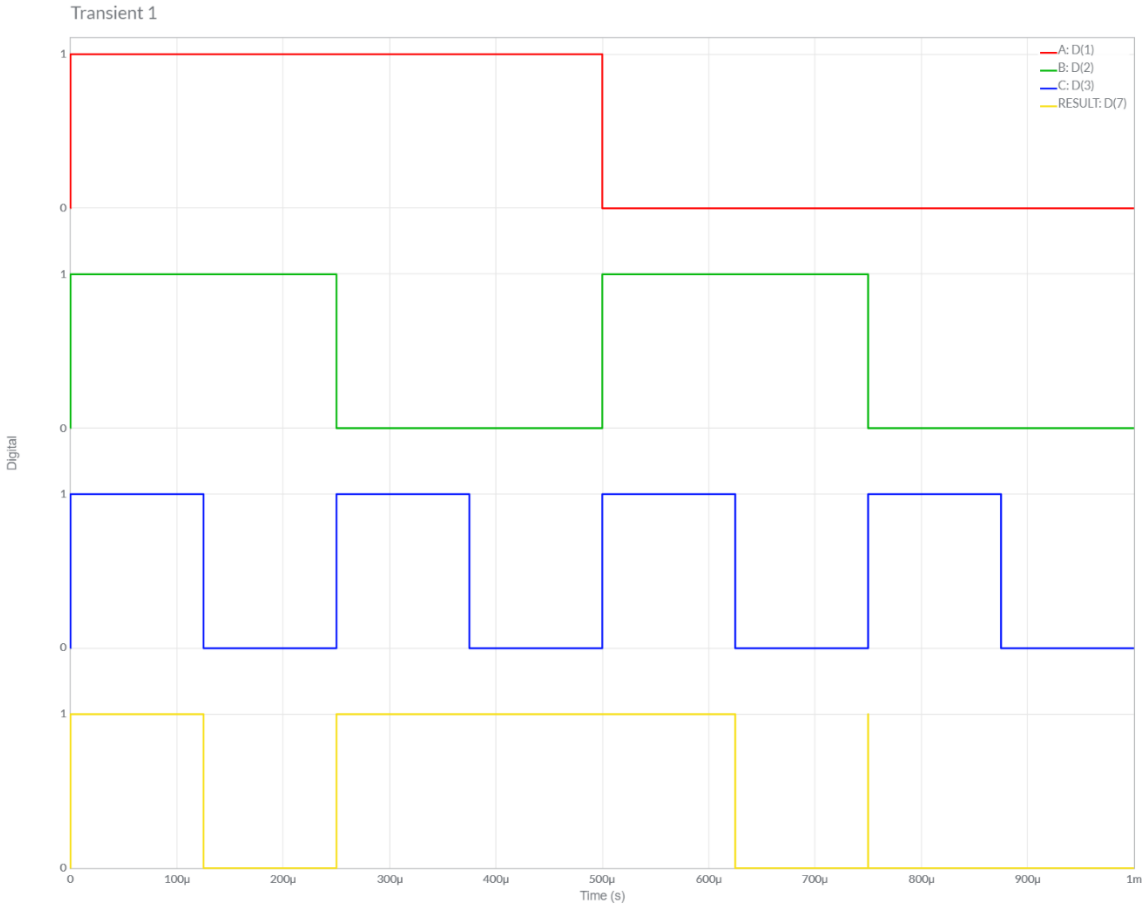
Final Expression = $(A+B).(\bar{B}+C)$

Sr No	A	B	C	$\bar{B}$	A+B	$\bar{B}+C$	Result : $(A+B).(\bar{B}+C)$
1.)	0	0	0	1	0	1	0
2.)	0	0	1	1	0	1	0
3.)	0	1	0	0	1	0	0
4.)	0	1	1	0	1	1	1
5.)	1	0	0	1	1	1	1
6.)	1	0	1	1	1	1	1
7.)	1	1	0	0	1	0	0
8.)	1	1	1	0	1	1	1

b.) Implement the circuit as shown in Figure in Multisim online.



c.) Time Graph



d.) Final Result and Conclusion

	A	B	C	Graph O/I	Theoratical O/I
1	0	0	0	0	0
2	0	0	1	0	0
3	0	1	0	0	0
4	0	1	1	1	1
5	1	0	0	1	1
6	1	0	1	1	1
7	1	1	0	0	0
8	1	1	1	1	1

Conclusion:

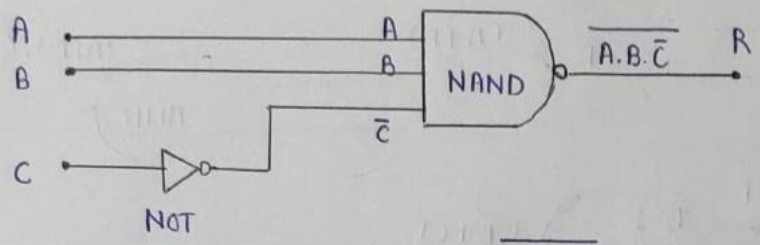
We can observe from Above Table, Both the *Theoretical* and *Multisim* Values of Given Circuit are **Equal**.

Hence, Experiment is Performed Successfully (without any Error).

Question -2

a.) Calculate the Logic Gates Circuit's Output [Theoretical]

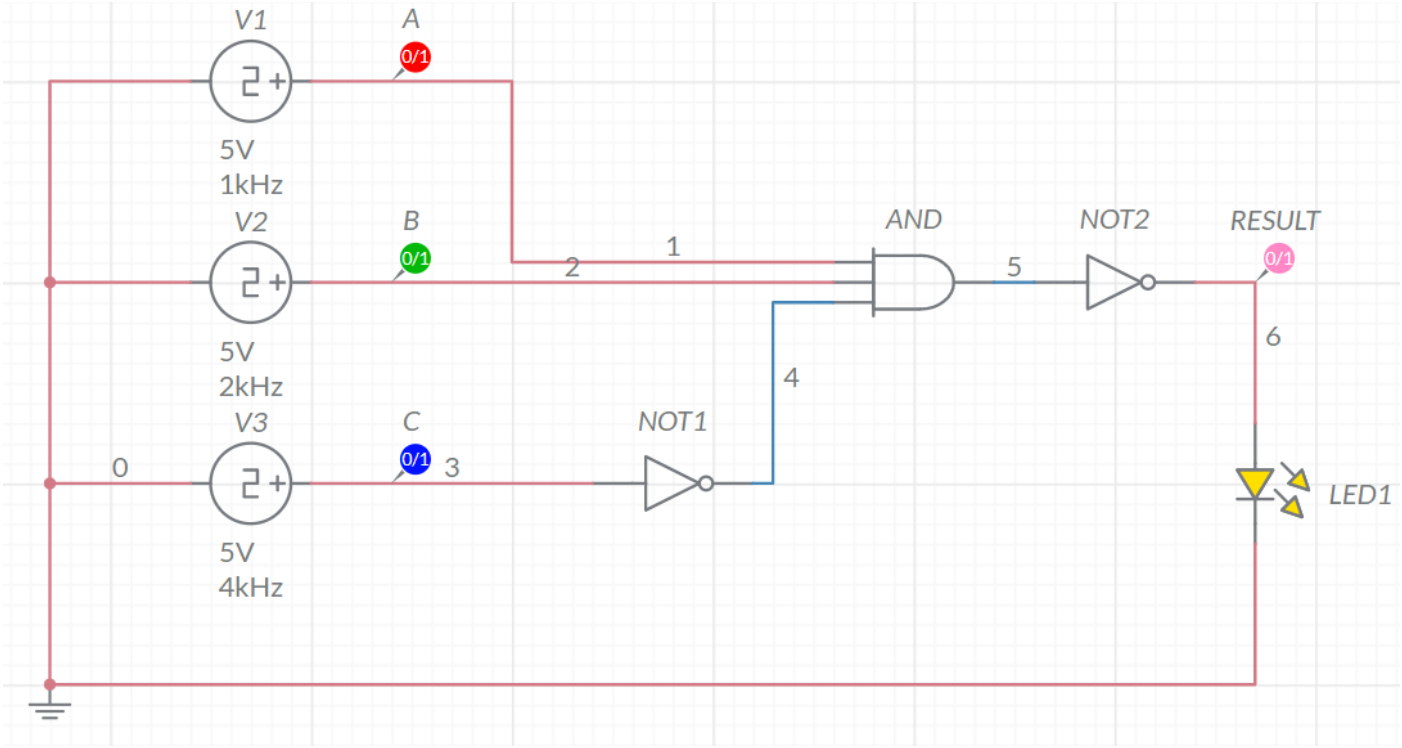
Circuit 2 :



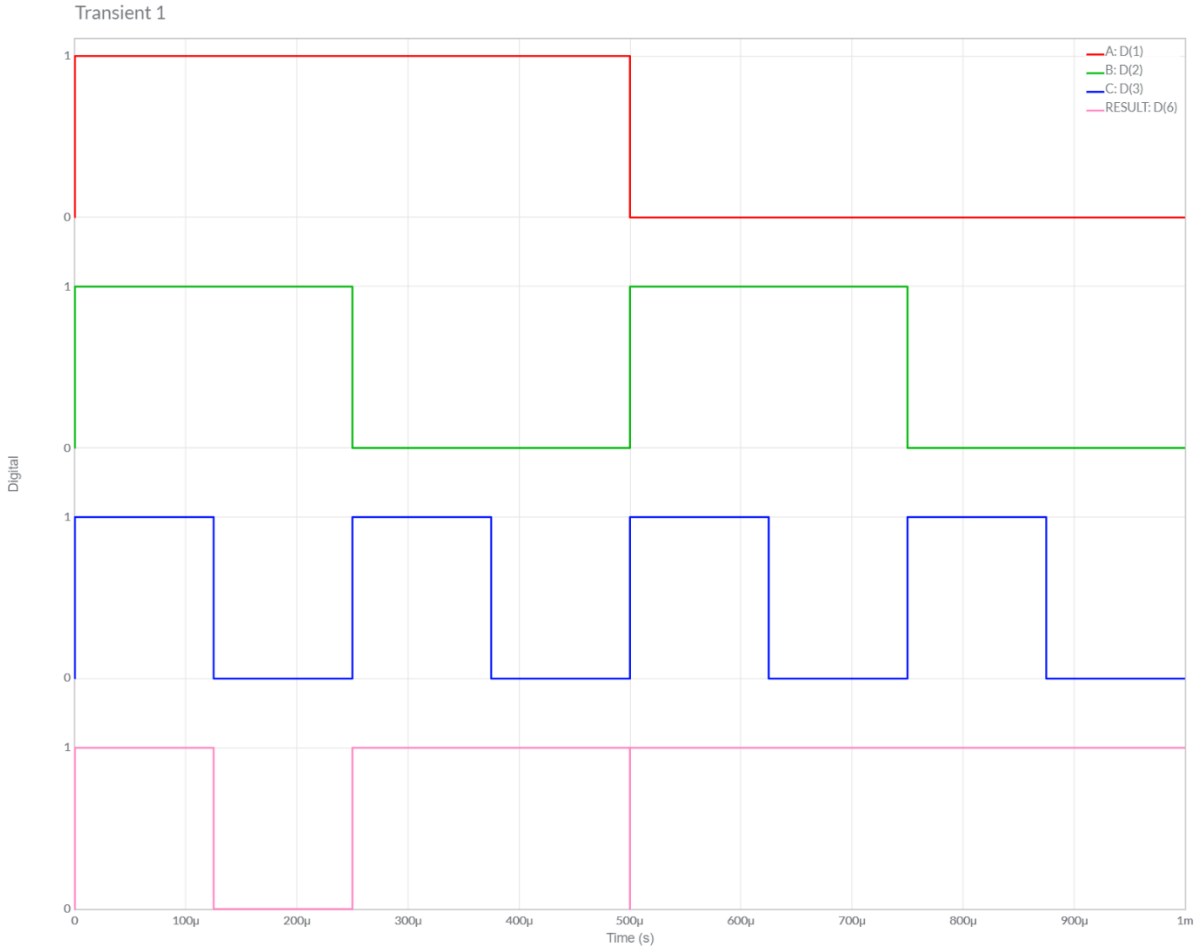
Final Expression = $\overline{A.B.\bar{C}}$

Sr No	A	B	C	$\bar{C}$	$A.B.\bar{C}$	Result : $\overline{A.B.\bar{C}}$
1.)	0	0	0	1	0	1
2.)	0	0	1	0	0	1
3.)	0	1	0	1	0	1
4.)	0	1	1	0	0	1
5.)	1	0	0	1	0	1
6.)	1	0	1	0	0	1
7.)	1	1	0	1	1	0
8.)	1	1	1	0	0	1

b.) Implement the circuit as shown in Figure in Multisim online.



c.) Time Graph



d.) Final Result and Conclusion

	A	B	C	Graph O/I	Theoratical O/I
1	0	0	0	1	1
2	0	0	1	1	1
3	0	1	0	1	1
4	0	1	1	1	1
5	1	0	0	1	1
6	1	0	1	1	1
7	1	1	0	0	0
8	1	1	1	1	1

Conclusion:

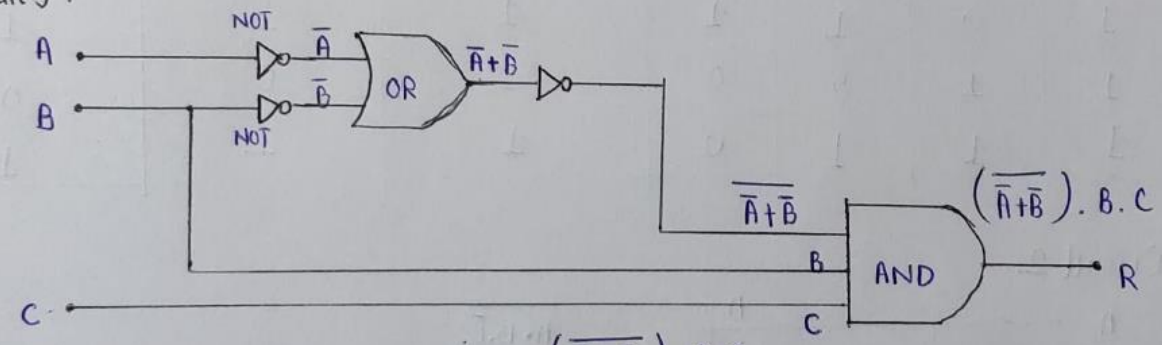
We can observe from Above Graph, Both the *Theoretical* and *Multisim* Values of Given Circuit are **Equal**.

Hence, Experiment is Performed Successfully (without any Error).

Question -3

a.) Calculate the Logic Gates Circuit's Output [Theoretical]

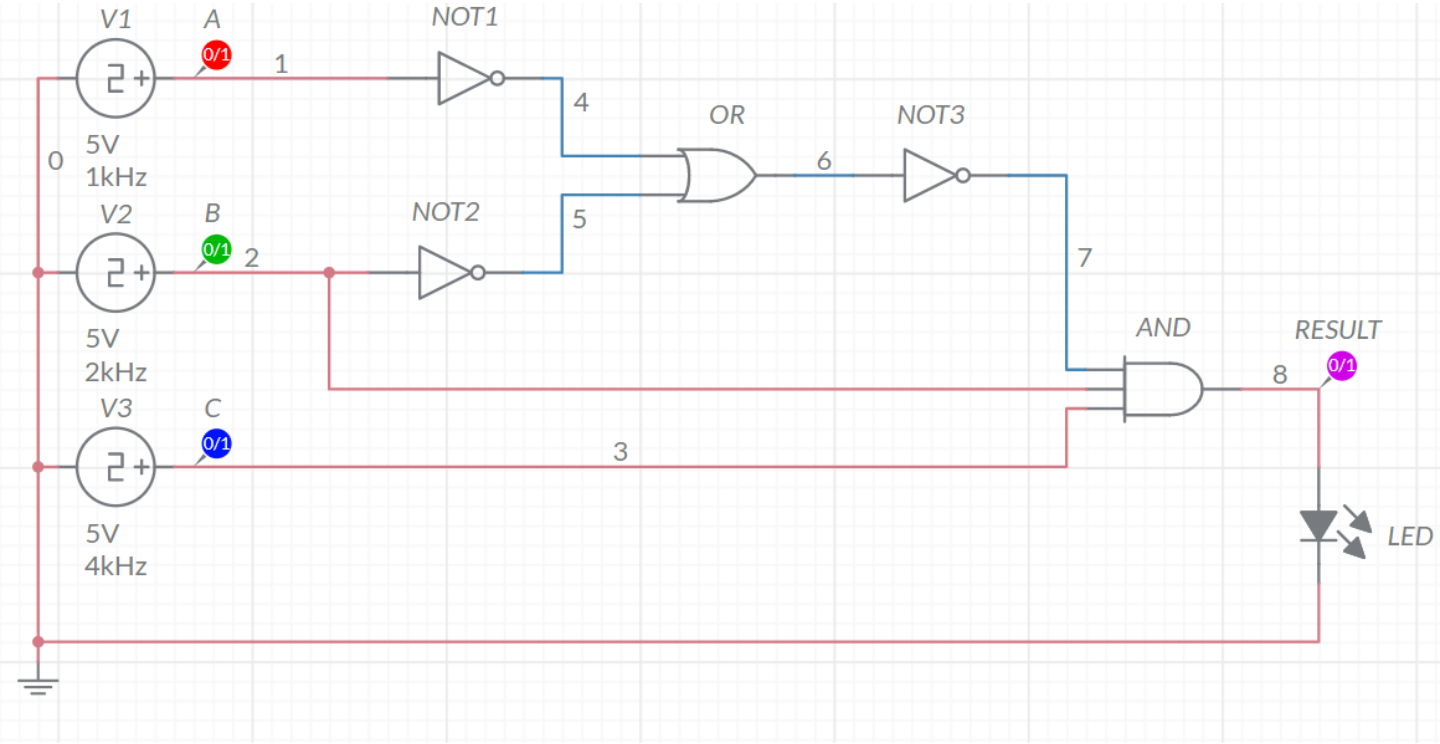
Circuit 3 :



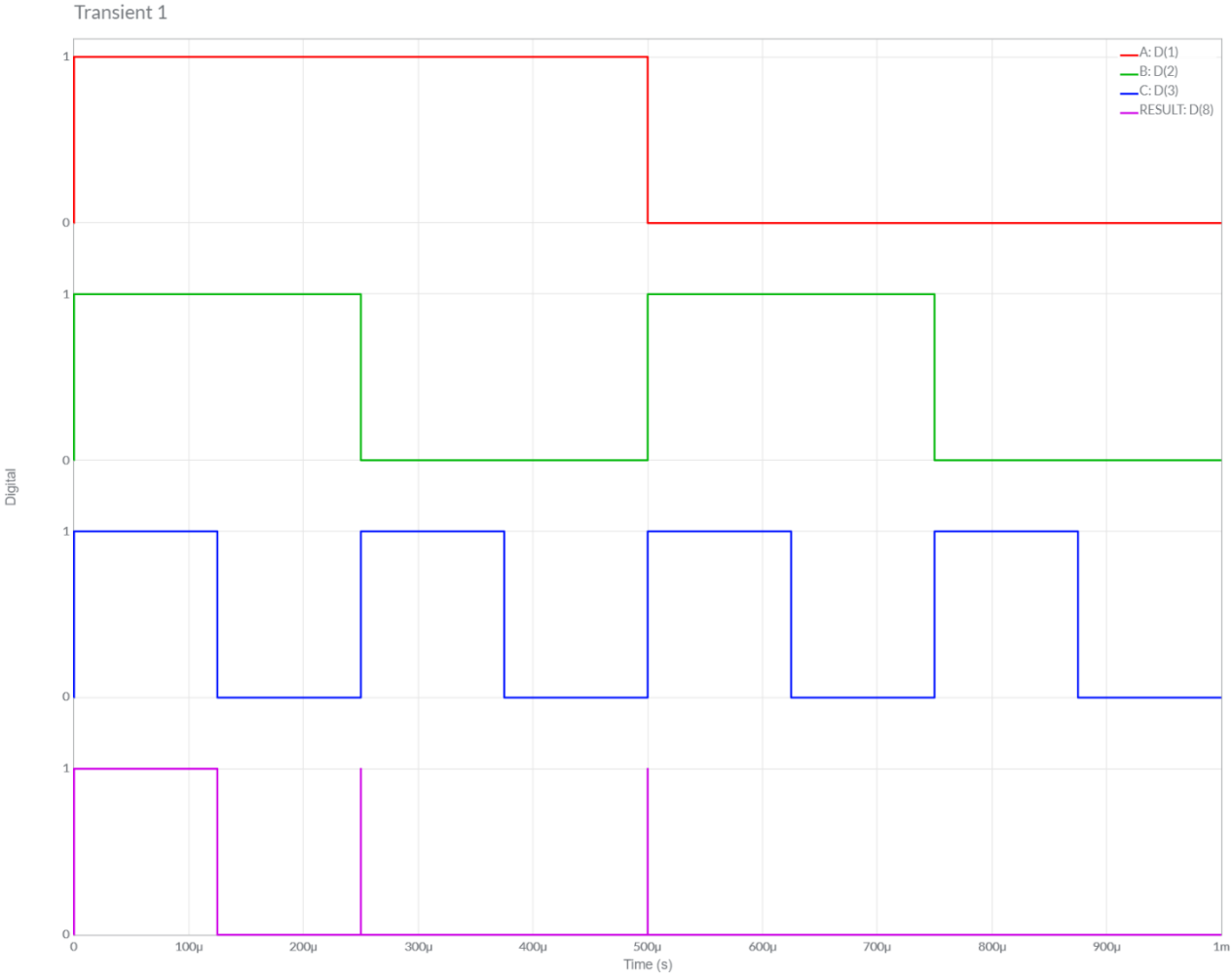
Final Expression : $(\overline{\bar{A}+\bar{B}}).B.C$

Sr No	A	B	C	$\bar{A}$	$\bar{B}$	$\bar{A}+\bar{B}$	$\overline{\bar{A}+\bar{B}}$	Result : $(\overline{\bar{A}+\bar{B}}).B.C$
1.)	0	0	0	1	1	1	0	0
2.)	0	0	1	1	1	1	0	0
3.)	0	1	0	1	0	1	0	0
4.)	0	1	1	1	0	1	0	0
5.)	1	0	0	0	1	1	0	0
6.)	1	0	1	0	1	1	0	0
7.)	1	1	0	0	0	0	1	0
8.)	1	1	1	0	0	0	1	1

b.) Implement the circuit as shown in Figure in Multisim online.



c.) Time Graph



d.) Final Result and Conclusion

	A	B	C	Graph O/I	Theoratical O/I
1	0	0	0	0	0
2	0	0	1	0	0
3	0	1	0	0	0
4	0	1	1	0	0
5	1	0	0	0	0
6	1	0	1	0	0
7	1	1	0	0	0
8	1	1	1	1	1

Conclusion:

We can observe from Above Table, Both the *Theoretical* and *Multisim* Values of Given Circuit are **Equal**.

Hence, Experiment is Performed Successfully (without any Error).

Submitted By:
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