SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT
ELECTRONICS ENGINEERING DEPARTMENT

Expt. No:	9	Full Wave Rectifier
Date:	22/10/2020	

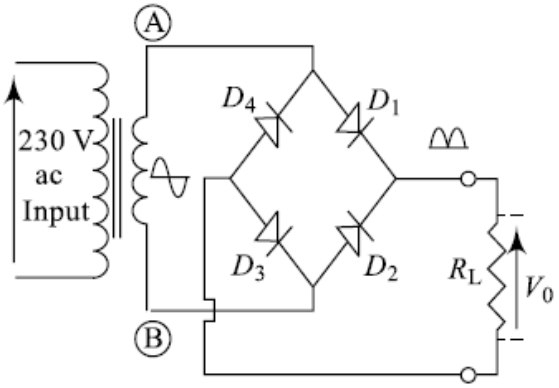
AIM: To study, design and implement Full Wave Rectifier Circuit.

SOFTWARE TOOLS / OTHER REQUIREMENTS:

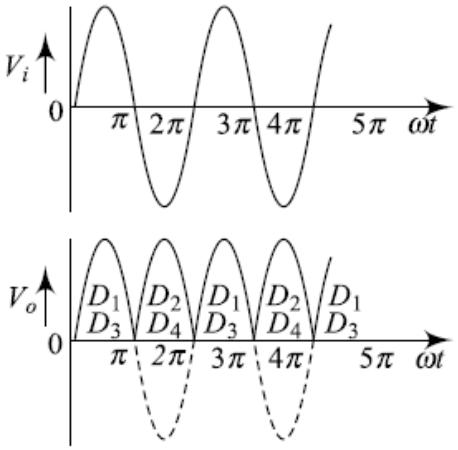
1. Multisim Simulator/Circuit Simulator

THEORY:

The circuit diagram of the Bridge Rectifier along with inou-toutput waveforms is shown in figure below. The four diodes D1, D2, D3 and D4 are arranged in a bridge configuration and hence the name. The circuit contains a transformer that steps down the input ac magnitude depending on the requirement and provides the necessary isolation avoiding any risk of shocks.



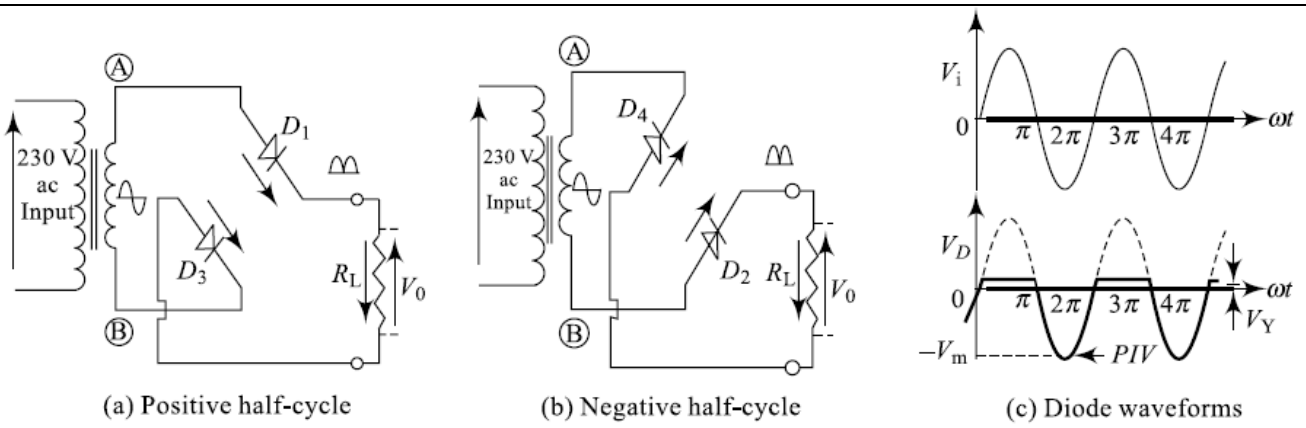
(a) Bridge rectifier circuit



(b) Input/output waveforms

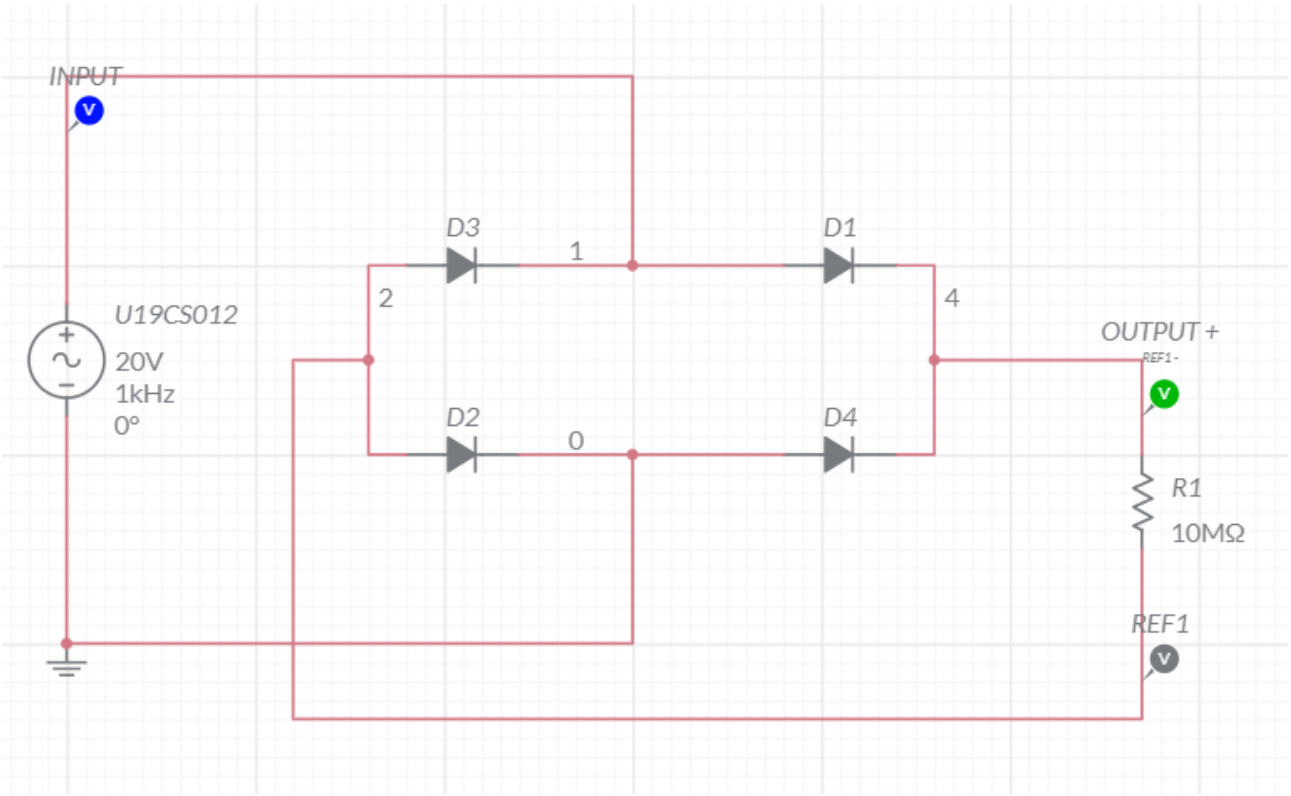
Let Vi = Vm sin wt be the input signal at the transformer secondary, it is a sinusoidal signal with maximum amplitude Vm. During the positive half-cycle of the input, the point A being positive with respect to the point B, the diodes D1 and D3 will be forward biased; however, the diodes D2 and D4 will be reverse biased. The pair of diodes D1 and D3 start conduction resulting in a current ID flowing through the load resistor RL in the direction marked for the entire positive half-cycle, i.e. from wt = 0 to π and the diodes D2 and D4 will be in OFF condition. During the negative half-cycle of the input, the point B will be positive with respect to the point A and the diodes D2 and D4 will be forward biased, and the diodes D1 and D3 will be reverse biased. Diodes D2 and D4 start conduction resulting in a current ID flowing through the load resistor RL again in the same direction (as earlier) for the entire negative half-cycle, i.e.

from wt = π to 2π and the diodes D1 and D3 will be in OFF condition. Thus, between wt = 0 to π, D1 and D3 conduct and result in an output, between wt = π to 2π, D2 and D4 conduct and result in an output Vo as indicated in Fig. (b). It can therefore be observed that for both cycles of input, there is a current flowing, hence the name full-wave rectifier.

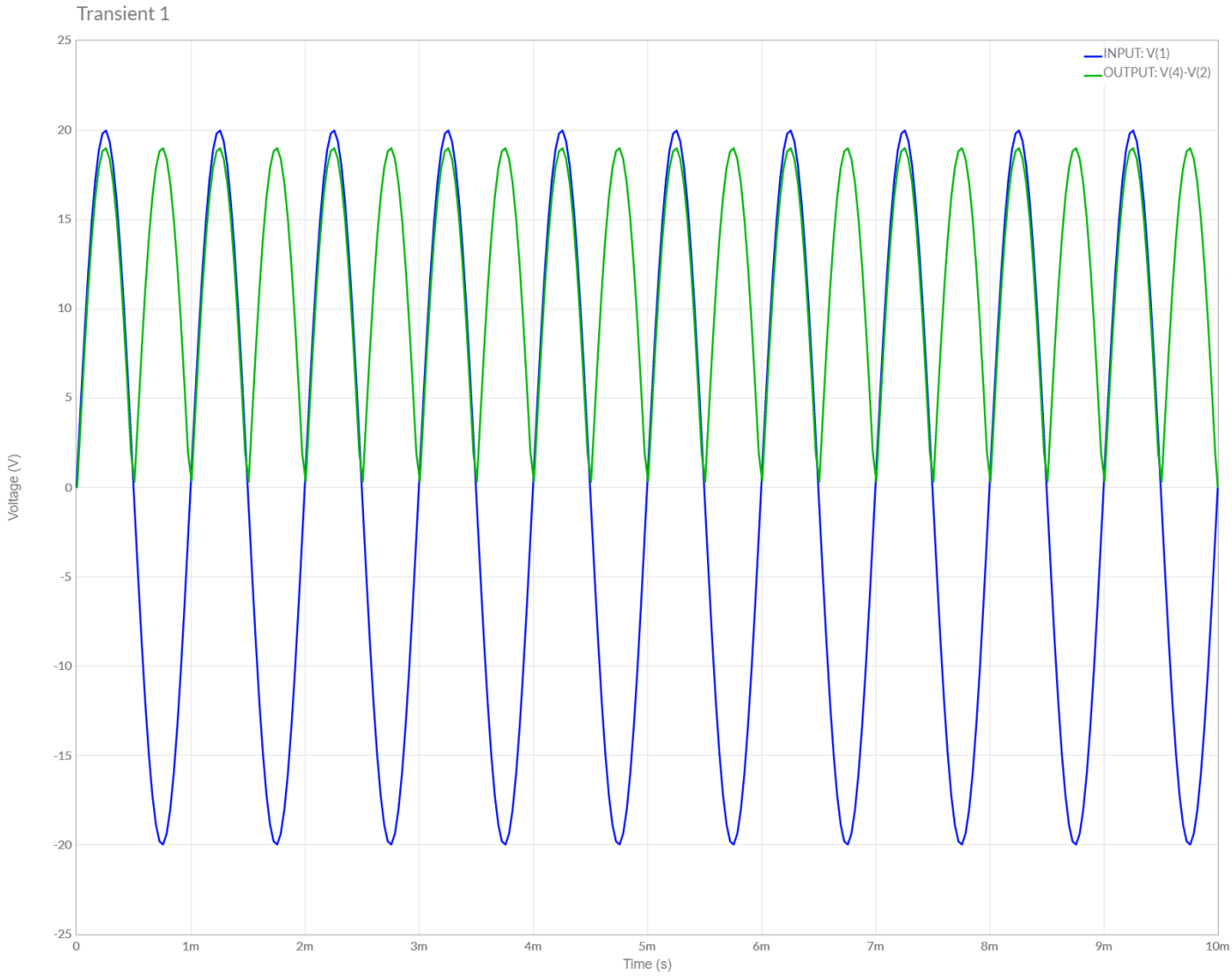


(a) Positive half-cycle (b) Negative half-cycle (c) Diode waveforms

CIRCUIT DIAGRAM (FROM MULTISIM)



WAVEFORMS (FROM MULTISIM)



CONCLUSIONS

1.) In this Experiment, We have studied about Full Wave Rectifier Circuit and its Working.

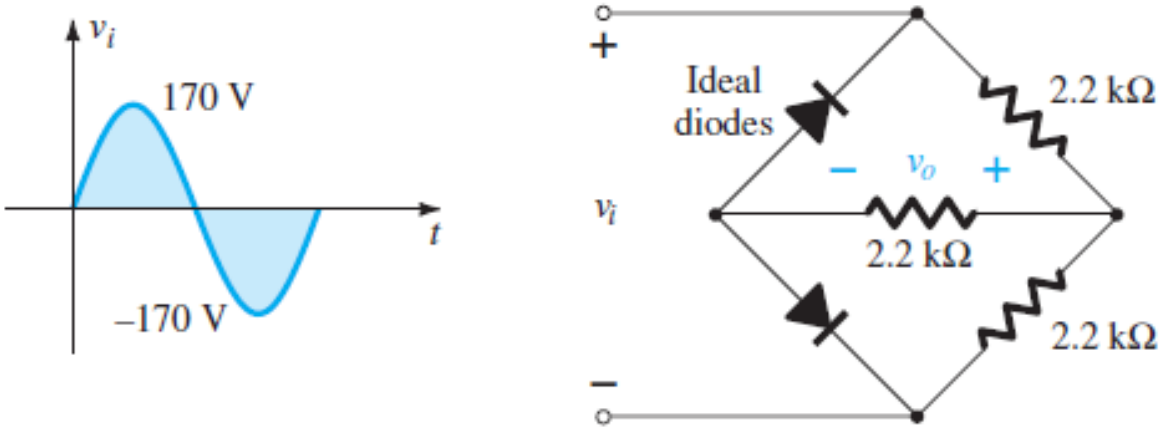
2.) We Verified the Theoretical Knowledge of Full Wave Rectifier Circuit by Performing Simulations of Full Wave Rectifier Circuit in Multisim.

3.) Hence, we have Successfully Designed, Plotted and Verified Full Wave Rectifier Circuit.

ASSIGNMENT-9

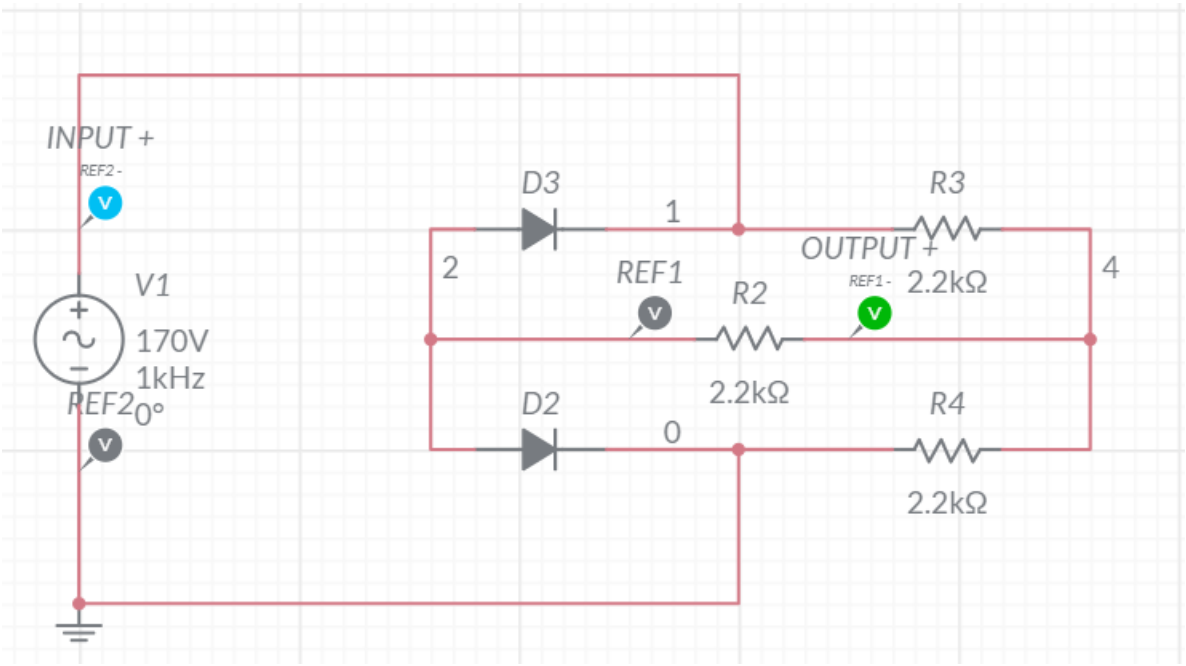
U19CS012

1. Calculate and Plot Vo for the following circuit.

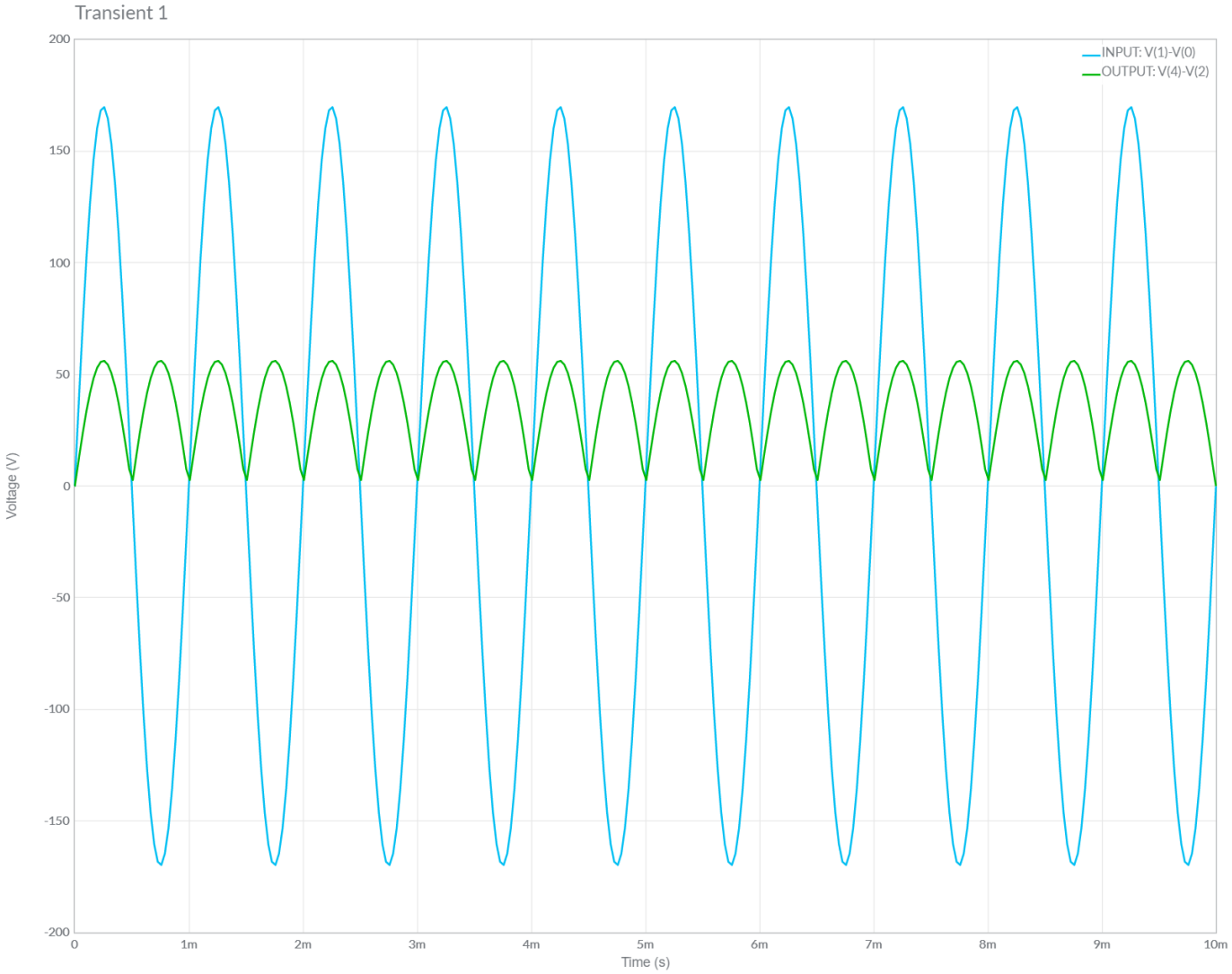


A.) Multisim Calculations:

1.) Circuit Image:



2.) Grapher Image:



B.) Calculation Part

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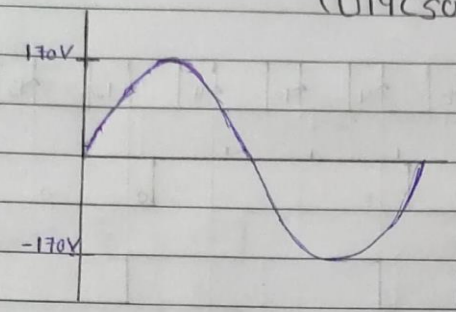
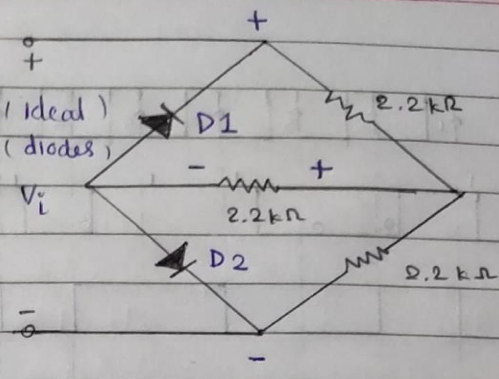
Q2.) (U19CS012)

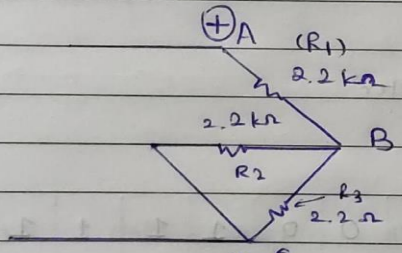




(A) During Positive half of cycle

D1 will be Reverse biased — D1 → open circuit

D2 will be short circuit (forward Biased) — D2 → short



Requivalent = $R_1 + (R_2 \parallel R_3)$

$= 2.2k\Omega + \frac{1}{\left(\frac{1}{2.2} + \frac{1}{2.2}\right)}$

$= [3.3k\Omega]$

$i = \frac{V}{Req} = \frac{170}{(3.3k\Omega)}$

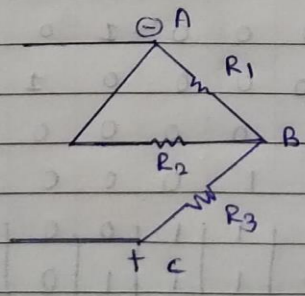
170V

Ans: $\left[V_{R_2} = (V)(x)\ \frac{(1.1)}{(1.1+2.2)}\ k\Omega = 170 \times \frac{1}{3} = \frac{170\ V}{3}\right]$

(B) During Negative half cycle

D1 will be forward biased — D1 → short ckt

D2 will be reverse biased — D2 → open ckt



$Req = R_3 + (R_1 \parallel R_2) = (2.2 + 1.1)k\Omega = 3.3k\Omega$

$V_{R_2} = (V) * \frac{(R_1 \parallel R_2)}{(R_3 + (R_1 \parallel R_2))} = 170 \times \frac{1.1}{(1.1+2.2)}$

Ans: $\left[V_{R_2} = \frac{170\ V}{3}\right]$