6 Field-Effect Transistors

CHAPTER OBJECTIVES

- Become familiar with the construction and operating characteristics of Junction Field Effect (JFET), Metal-Oxide Semiconductor FET (MOSFET), and Metal-Semiconductor FET (MESFET) transistors.
- Be able to sketch the transfer characteristics from the drain characteristics of a JFET, MOSFET, and MESFET transistor.
- Understand the vast amount of information provided on the specification sheet for each type of FET.
- Be aware of the differences between the dc analysis of the various types of FETs.

6.1 INTRODUCTION

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent, those of the BJT transistor described in Chapters 3 through 5. Although there are important differences between the two types of devices, there are also many similarities, which will be pointed out in the sections to follow.

The primary difference between the two types of transistors is the fact that:

The BJT transistor is a current-controlled device as depicted in Fig. 6.1a, whereas the JFET transistor is a voltage-controlled device as shown in Fig. 6.1b.

In other words, the current I_C in Fig. 6.1a is a direct function of the level of I_B. For the FET the current I_D will be a function of the voltage V_{GS} applied to the input circuit as shown in Fig. 6.1b. In each case the current of the output circuit is controlled by a parameter of the input circuit—in one case a current level and in the other an applied voltage.

Just as there are *npn* and *pnp* bipolar transistors, there are *n-channel* and *p-channel* field-effect transistors. However, it is important to keep in mind that the BJT transistor is a *bipolar* device—the prefix *bi* indicates that the conduction level is a function of two charge carriers, electrons and holes. The FET is a *unipolar* device depending solely on either electron (*n*-channel) or hole (*p*-channel) conduction.

The term *field effect* in the name deserves some explanation. We are all familiar with the ability of a permanent magnet to draw metal filings to itself without the need for actual contact. The magnetic field of the permanent magnet envelopes the filings and attracts them to the magnet along the shortest path provided by the magnetic flux lines. For the FET an *electric field* is established by the charges present, which controls the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

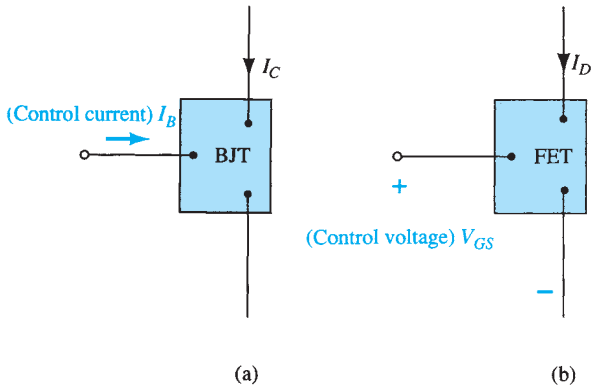


FIG. 6.1
(a) Current-controlled and (b) voltage-controlled amplifiers.

There is a natural tendency when introducing a device with a range of applications similar to one already introduced to compare some of the general characteristics of one to those of the other:

One of the most important characteristics of the FET is its high input impedance.

At a level of 1 MΩ to several hundred megohms it far exceeds the typical input resistance levels of the BJT transistor configurations—a very important characteristic in the design of linear ac amplifier systems. On the other hand, the BJT transistor has a much higher sensitivity to changes in the applied signal. In other words, the variation in output current is typically a great deal more for BJTs than for FETs for the same change in the applied voltage.

For this reason:

Typical ac voltage gains for BJT amplifiers are a great deal more than for FETs.

However,

FETs are more temperature stable than BJTs, and FETs are usually smaller than BJTs, making them particularly useful in integrated-circuit (IC) chips.

The construction characteristics of some FETs, however, can make them more sensitive to handling than BJTs.

Three types of FETs are introduced in this chapter: the *junction field-effect transistor* (JFET), *the metal–oxide–semiconductor field-effect transistor* (MOSFET), and the *metal–semiconductor field-effect transistor* (MESFET). The MOSFET category is further broken down into *depletion* and *enhancement* types, which are both described. The MOSFET transistor has become one of the most important devices used in the design and construction of integrated circuits for digital computers. Its thermal stability and other general characteristics make it extremely popular in computer circuit design. However, as a discrete element in a typical top-hat container, it must be handled with care (to be discussed in a later section). The MESFET is a more recent development and takes full advantage of the high-speed characteristics of GaAs as the base semiconductor material. Although currently the more expensive option, the cost issue is often outweighed by the need for higher speeds in RF and computer designs.

Once the FET construction and characteristics have been introduced, the biasing arrangements will be covered in Chapter 7. The analysis performed in Chapter 4 using BJT transistors will prove helpful in the derivation of the important equations and understanding the results obtained for FET circuits.

Ian Munro Ross and G. C. Dacey (Fig. 6.2) were instrumental in the early stages of development of the field-effect transistor. Take particular note of the equipment used in 1955 for their research.

Drs. Ian Munro Ross (front) and G. C. Dacey jointly developed an experimental procedure for measuring the characteristics of a field-effect transistor in 1955.

Dr. Ross Born: Southport, England; PhD, Gonville and Caius College, Cambridge University; President Emeritus, AT&T Bell Labs; Fellow, IEEE; Member, the National Science Board; Chairman, National Advisory Committee on Semiconductors

Dr. Dacey Born: Chicago, Illinois; PhD, California Institute of Technology; Director of Solid-State Electronics Research, Bell Labs; Vice President, Research, Sandia Corporation; Member IRE, Tau Beta Pi, Eta Kappa Nu

FIG. 6.2
Early development of the field-effect transistor.
(Courtesy of AT&T Archives and History Center.)

6.2 CONSTRUCTION AND CHARACTERISTICS OF JFETs

As indicated earlier, the JFET is a three-terminal device with one terminal capable of controlling the current between the other two. In our discussion of the BJT transistor the *npn* transistor was employed through the major part of the analysis and design sections, with a

section devoted to the effect of using a *pnp* transistor. For the JFET transistor the *n*-channel device will be the prominent device, with paragraphs and sections devoted to the effect of using a *p*-channel JFET.

The basic construction of the *n*-channel JFET is shown in Fig. 6.3. Note that the major part of the structure is the *n*-type material, which forms the channel between the embedded layers of *p*-type material. The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the *drain (D)*, whereas the lower end of the same material is connected through an ohmic contact to a terminal referred to as the *source (S)*. The two *p*-type materials are connected together and to the *gate (G)* terminal. In essence, therefore, the drain and the source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material. In the absence of any applied potentials the JFET has two *p–n* junctions under no-bias conditions. The result is a depletion region at each junction, as shown in Fig. 6.3, that resembles the same region of a diode under no-bias conditions. Recall also that a depletion region is void of free carriers and is therefore unable to support conduction.

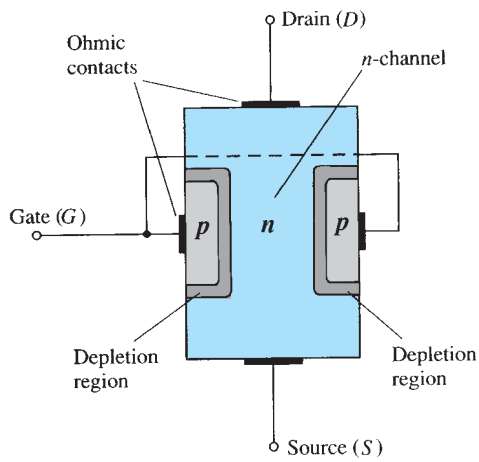


FIG. 6.3
Junction field-effect transistor (JFET).

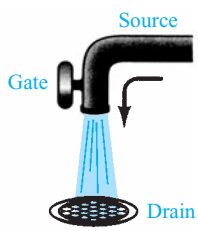


FIG. 6.4
Water analogy for the JFET control mechanism.

Analogies are seldom perfect and at times can be misleading, but the water analogy of Fig. 6.4 does provide a sense for the JFET control at the gate terminal and the appropriateness of the terminology applied to the terminals of the device. The source of water pressure can be likened to the applied voltage from drain to source, which establishes a flow of water (electrons) from the spigot (source). The "gate," through an applied signal (potential), controls the flow of water (charge) to the "drain." The drain and source terminals are at opposite ends of the *n*-channel as introduced in Fig. 6.3 because the terminology is defined for electron flow.

$V_{GS} = 0$ V, V_{DS} Some Positive Value

In Fig. 6.5, a positive voltage V_{DS} is applied across the channel and the gate is connected directly to the source to establish the condition $V_{GS} = 0$ V. The result is a gate and a source terminal at the same potential and a depletion region in the low end of each *p*-material similar to the distribution of the no-bias conditions of Fig. 6.3. The instant the voltage V_{DD} ($=V_{DS}$) is applied, the electrons are drawn to the drain terminal, establishing the conventional current I_D with the defined direction of Fig. 6.5. The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D = I_S$). Under the conditions in Fig. 6.5, the flow of charge is relatively uninhibited and is limited solely by the resistance of the *n*-channel between drain and source.

It is important to note that the depletion region is wider near the top of both *p*-type materials. The reason for the change in width of the region is best described through the help of Fig. 6.6. Assuming a uniform resistance in the *n*-channel, we can break down

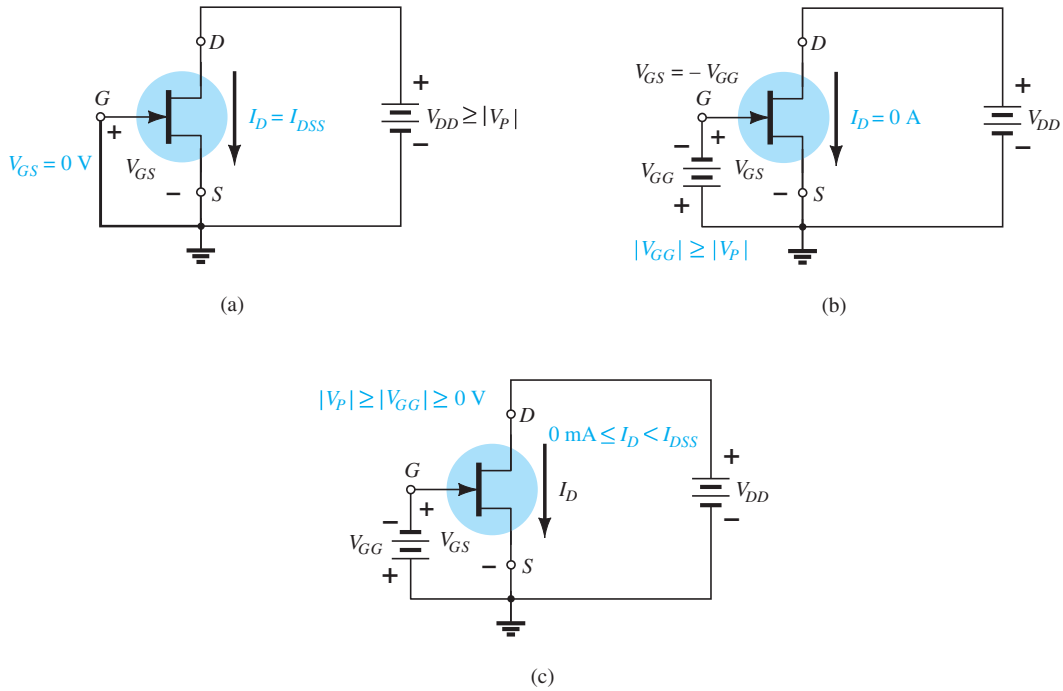


FIG. 6.15

(a) $V_{GS} = 0$ V, $I_D = I_{DSS}$; (b) cutoff ($I_D = 0$ A) V_{GS} less than the pinch-off level; (c) I_D is between 0 A and I_{DSS} for $V_{GS} \leq 0$ V and greater than the pinch-off level.

6.3 TRANSFER CHARACTERISTICS

Derivation

For the BJT transistor the output current I_C and the input controlling current I_B are related by beta, which was considered constant for the analysis to be performed. In equation form,

$$I_C = f(I_B) = \beta I_B \qquad \text{(6.2)}$$

control variable

constant

In Eq. (6.2) a linear relationship exists between I_C and I_B. Double the level of I_B and I_C will increase by a factor of two also.

Unfortunately, this linear relationship does not exist between the output and input quantities of a JFET. The relationship between I_D and V_{GS} is defined by *Shockley's equation* (see Fig. 6.16):

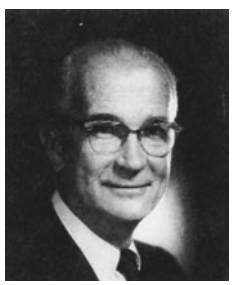
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad \text{(6.3)}$$

control variable

constants

The squared term in the equation results in a nonlinear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitude of V_{GS}.

For the dc analysis to be performed in Chapter 7, a graphical rather than a mathematical approach will in general be more direct and easier to apply. The graphical approach, however, will require a plot of Eq. (6.3) to represent the device and a plot of the network equation relating the same variables. The solution is defined by the point of intersection of the two curves. It is important to keep in mind when applying the graphical approach that the device characteristics will be *unaffected* by the network in which the device is employed.



William Bradford Shockley (1910–1989), co-inventor of the first transistor and formulator of the "field-effect" theory employed in the development of the transistor and the FET.

Shockley Born: London, England; PhD, Harvard, 1936; Head, Transistor Physics Department, Bell Laboratories; President, Shockley Transistor Corp.; Poniatoff Professor of Engineering Science, Stanford University; Nobel Prize in physics in 1956 with Walter Brattain and John Bardeen

FIG. 6.16

Dr. William Bradford Shockley. (Courtesy of AT&T Archives and History Center.)