



# Sardar Vallabhbhai National Institute of Technology, Surat

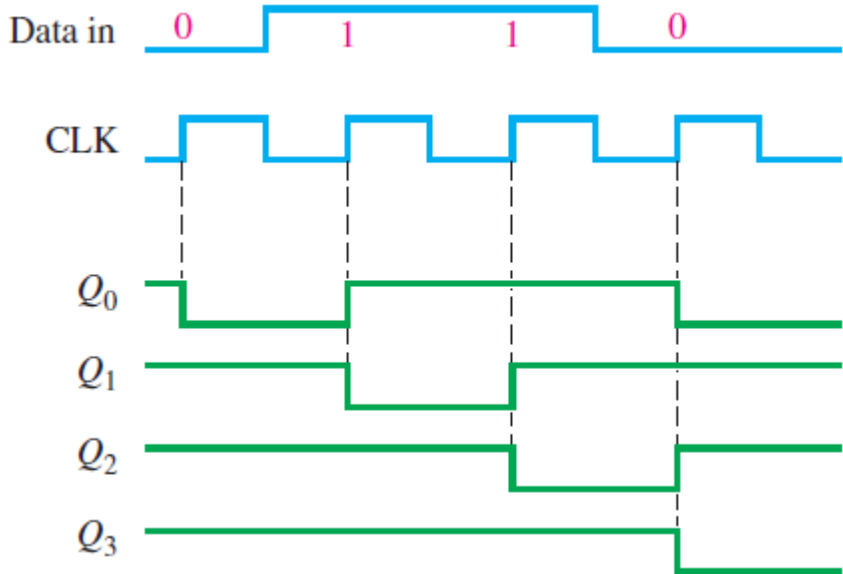
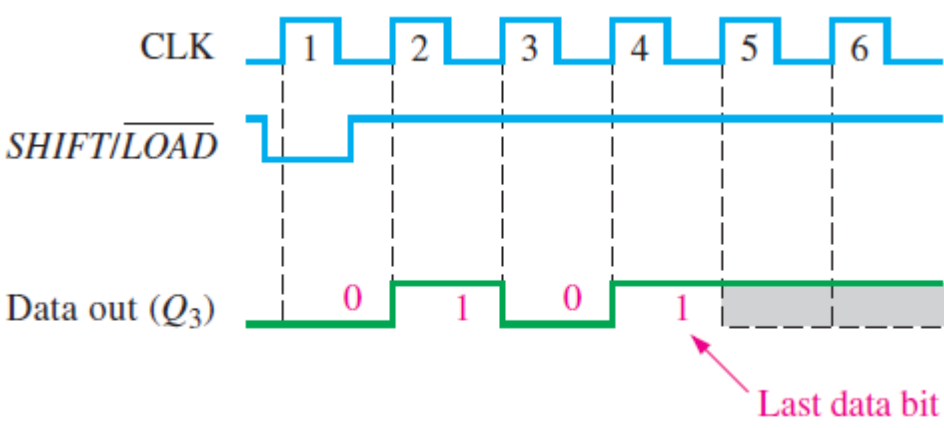
ECED Department

Subject: Digital Electronics & Logic Design (EC-207)

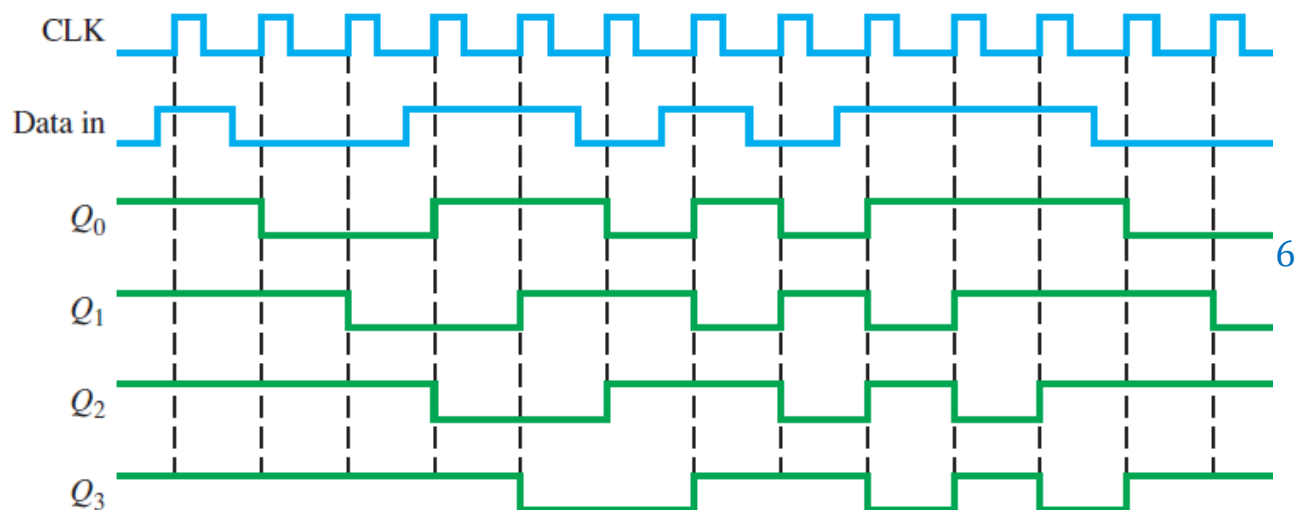
B.Tech Computer, Sem-III, Div - (A&B)

Date: 20-10-2020

## Tutorial – 6 Hints/Solutions

1	 <p>Timing diagram for a 4-bit shift register. Data in: 0, 1, 1, 0. CLK: square wave. Q<sub>0</sub>, Q<sub>1</sub>, Q<sub>2</sub>, Q<sub>3</sub>: outputs. Q<sub>0</sub> is high when Data in is 1. Q<sub>1</sub> is high when Data in is 1 at the previous clock. Q<sub>2</sub> is high when Data in is 1 at the previous clock. Q<sub>3</sub> is high when Data in is 1 at the previous clock.</p>	4
2	 <p>Timing diagram for a shift register. CLK: square wave labeled 1 to 6. SHIFT/LOAD: active low, high for CLK 1, low for CLK 2-6. Data out (Q<sub>3</sub>): 0, 1, 0, 1, then shaded. Last data bit is indicated by an arrow pointing to the 1 at CLK 4.</p>	2

3



4

Initially: 101001111000  
 CLK1: 010100111100  
 CLK2: 001010011110  
 CLK3: 000101001111  
 CLK4: 000010100111  
 CLK5: 100001010011  
 CLK6: 110000101001  
 CLK7: 111000010100  
 CLK8: 011100001010  
 CLK9: 001110000101  
 CLK10: 000111000010  
 CLK11: 100011100001  
 CLK12: 110001110000

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