Analysis of Clocked (Synchronous) Sequential Circuits

- Now that we have flip-flops and the concept of memory in our circuit, we might want to determine what a circuit is doing.

- The behavior of a clocked sequential circuit is determined from its inputs, outputs and state of the flip-flops (i.e., the output of the flip-flops).

- The analysis of a clocked sequential circuit consists of obtaining a table of a diagram of the time sequences of inputs, outputs and states.

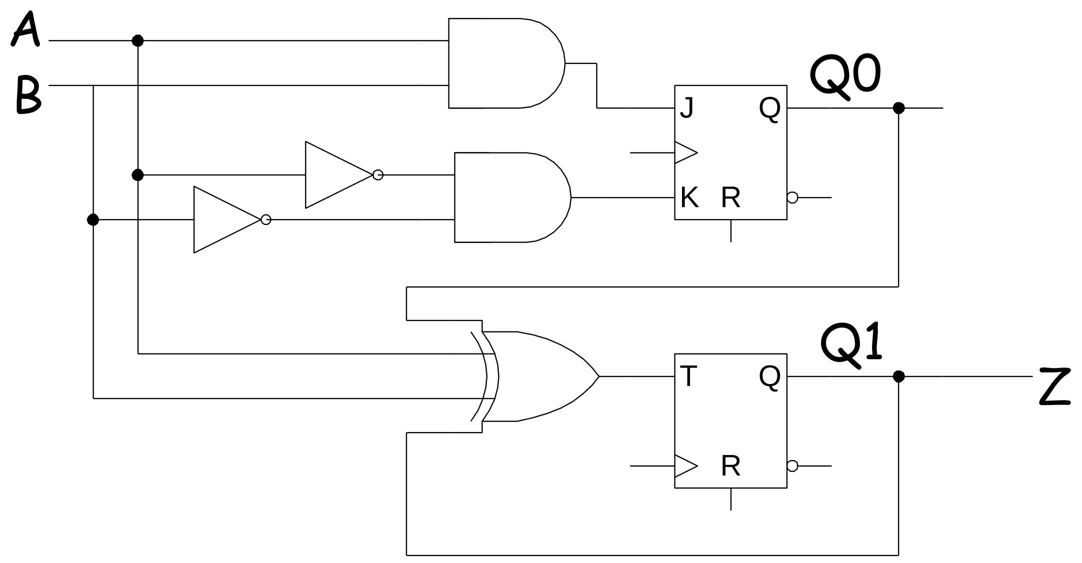
  - E.g., given a current state and current inputs, how will the state and outputs change when the next active clock edge arrives???

Analysis Procedure

- We have a basic procedure for analyzing a clocked sequential circuit:
  - Write down the **equations** for the **outputs** and the **flip-flop inputs**.
  - Using these equations, derive a **state table** which describes the next state.
  - Obtain a **state diagram** from the **state table**.
- It is the state table and/or state diagram that specifies the **behavior** of the circuit.
- Notes:
  - The **flip-flop input equations** are sometimes called the **excitation equations**.
  - The **state table** is sometimes called a **transition table**.
- We can best illustrate the procedure by doing examples…

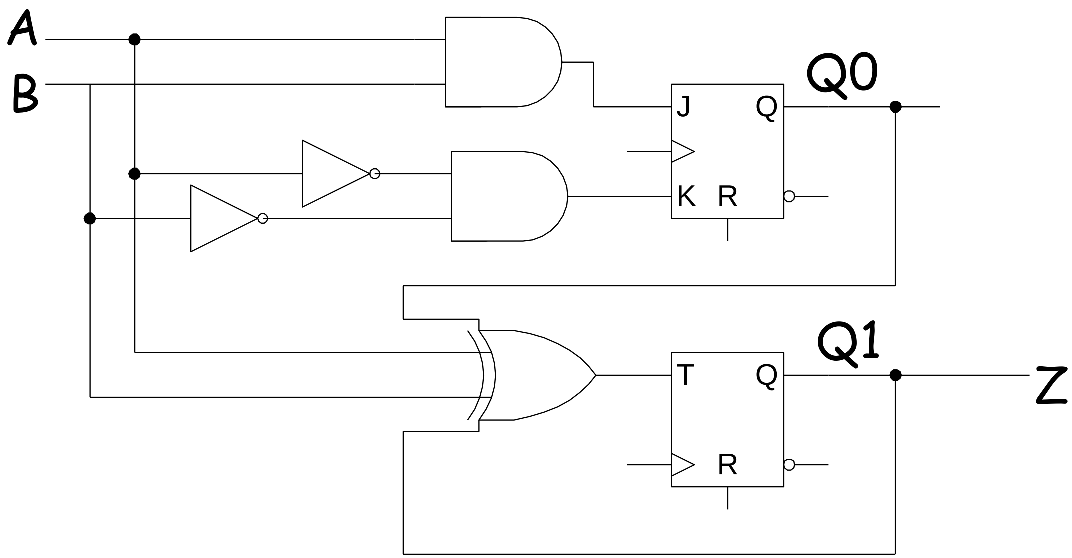
Analysis Example

- Consider the following circuit. We want to determine how it will behave.



- Observations: The circuit has two inputs **A** and **B**, one output **Z** (it happens that the output is equal to one of the flip flop outputs).

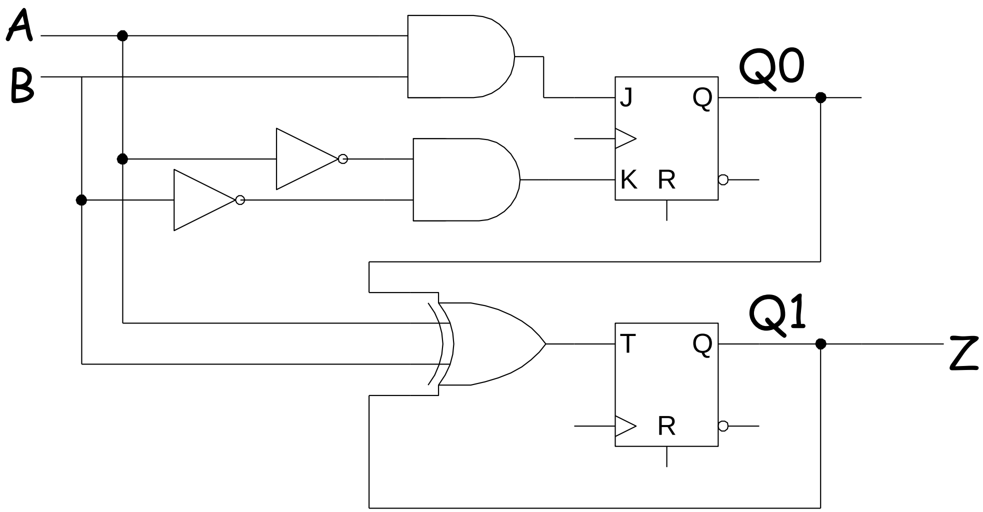
Analysis Example – More Observations



- Observations: The circuit has two flip-flops (different types) with outputs Q_0 and Q_1 **(This implies that there are as many as 4 different states in the circuit, namely Q_0Q_1 = 00, 01, 11, 10).**

- Observations: The circuit output depends on the current state (flip-flop outputs) only.

Analysis Example – Flip-Flop Input Equations and Output Equations



$$Z = Q_1$$

$$J_0 = AB$$
$$K_0 = A'B'$$

$$T_1 = A \oplus B \oplus Q_0 \oplus Q_1$$

- We write down Boolean expressions for the FF inputs and the circuit outputs.
- Done in terms of the **circuit inputs and the current state (flip-flop outputs)** of the system.

Analysis Example – State Table

- Using the FF input equations, we can build a table showing the FF inputs (this is the first step in creating the state table):

Current State	J_0K_0				T_1			
Q_0Q_1	$AB = 00$	01	10	11	$AB = 00$	01	10	11
00	01	00	00	10	0	1	1	0
01	01	00	00	10	1	0	0	1
10	01	00	00	10	1	0	0	1
11	01	00	00	10	0	1	1	0

$$Z = Q_1$$

$$J_0 = AB$$
$$K_0 = A'B'$$

$$T_1 = A \oplus B \oplus Q_0 \oplus Q_1$$

Analysis Example – State Table Continued

- We now have the FF input values, and know the FF behavior (for both JKFF and TFF):

Current State	J_0K_0				T_1			
Q_0Q_1	$AB = 00$	01	10	11	$AB = 00$	01	10	11
00	01	00	00	10	0	1	1	0
01	01	00	00	10	1	0	0	1
10	01	00	00	10	1	0	0	1
11	01	00	00	10	0	1	1	0

J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$Q'(t)$

JKFF Behavior

T	$Q(t+1)$
0	$Q(t)$
1	$Q'(t)$

TFF Behavior

- We can then determine the next FF output values:

Current State Q_0Q_1	Next State Q_0				Next State Q_1			
	$AB = 00$	01	10	11	$AB = 00$	01	10	11
00	0	0	0	1	0	1	1	0
01	0	0	0	1	0	1	1	0
10	0	1	1	1	1	0	0	1
11	0	1	1	1	1	0	0	1

Analysis Example – State Table Summarized

- We can (finally) write the next state information and the output values (based on current state and input values) in the **state table** format:

Current State Q_0Q_1	Next State Q_0Q_1 $AB = 00$	01	10	11	Output Z $AB = 00$	01	10	11
00	00	01	01	10	0	0	0	0
01	00	01	01	10	1	1	1	1
10	01	10	10	11	0	0	0	0
11	01	10	10	11	1	1	1	1

state table

- Observation: The output **Z** (in this example) is only a function of the current state; it does not depend on the inputs.

Analysis Example – State Table Alternative Representation

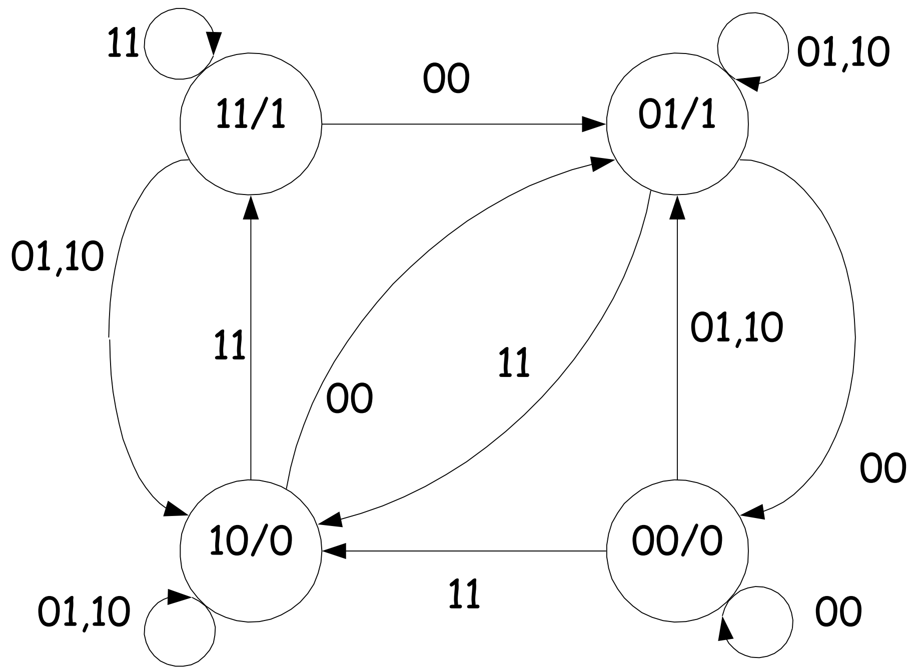
- We can also write the state table in a slightly different (tabular) format if we choose. The information presented is the same.

Current State		Input		Next State		Output
Q_0	Q_1	A	B	Q_0	Q_1	Z
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	1
0	1	1	0	0	1	1
0	1	1	1	1	0	1
1	0	0	0	0	1	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	1	0	1
1	1	1	0	1	0	1
1	1	1	1	1	1	1

alternative state table

State Diagram

- Another way to illustrate the behavior of a clocked sequential circuit is with a **state diagram**.



State Diagram Explained

- Each "bubble" **(state bubble)** in the state diagram represents one state of the system.
  - The flip-flop outputs that correspond to that state are **labeled** inside of the bubble.
- Each edge leaving a bubble represents a possible transition to another state once the active clock edge arrives.
  - The edges are **labeled** with the input values that cause the transition to occur.
- In this state diagram, the **output values** are **labeled** inside of the state bubbles.
  - We can do this because the outputs are only a function of the current state in this example.