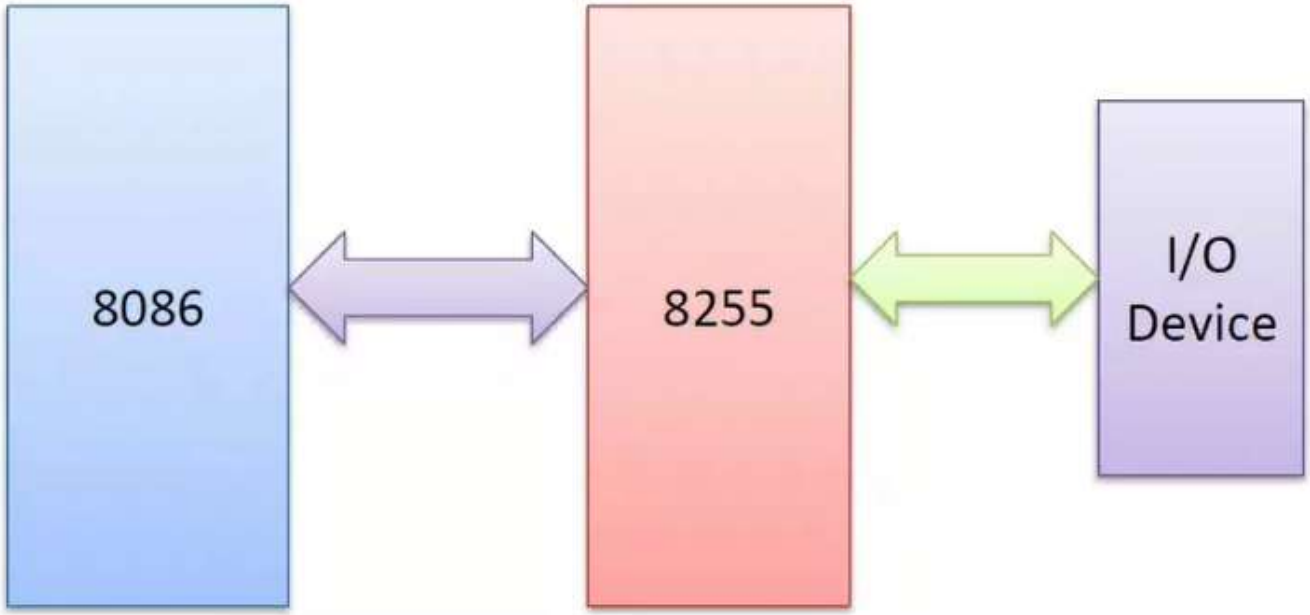
Why 8255A ??

- Intel 8255A is a general purpose parallel I/O interface.
- The peripheral devices are slower than the microprocessor. PPI makes an inter-relation between microprocessor and peripheral devices.
- It provides three I/O port (Port A, Port B and Port C)

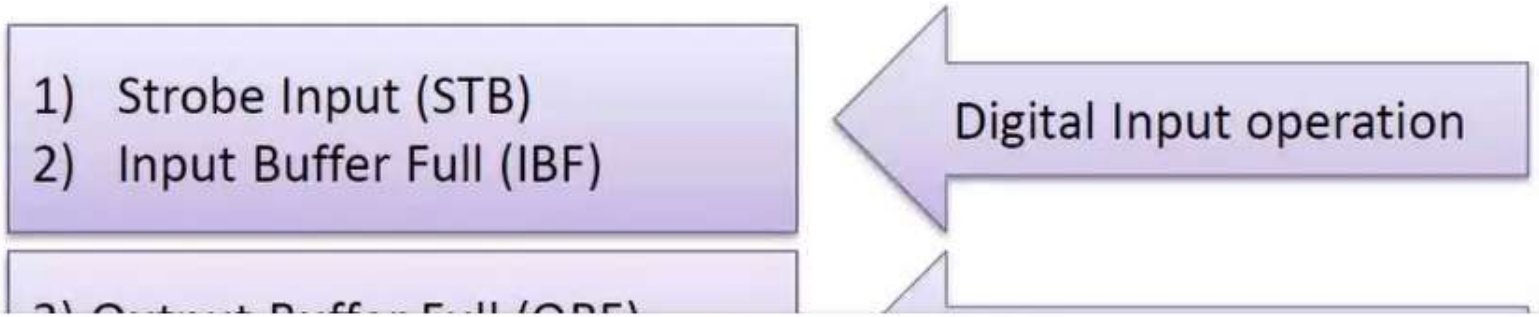


Handshaking

The making of inter relation between slower peripheral device and microprocessor is called handshaking.

Handshaking Signal

Before making the inter-relation between peripheral device and microprocessor the PPI send some signals to microprocessor and peripheral device to perform the process, these signals are called handshaking signal. 8255-based devices that perform handshaking support following handshaking signals:



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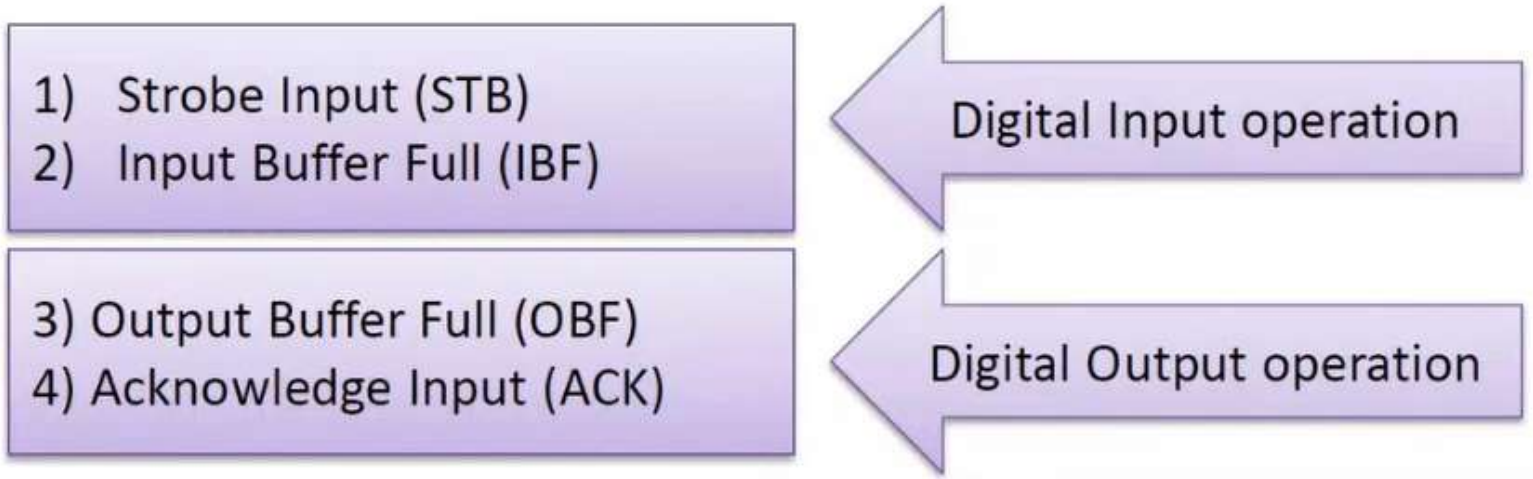
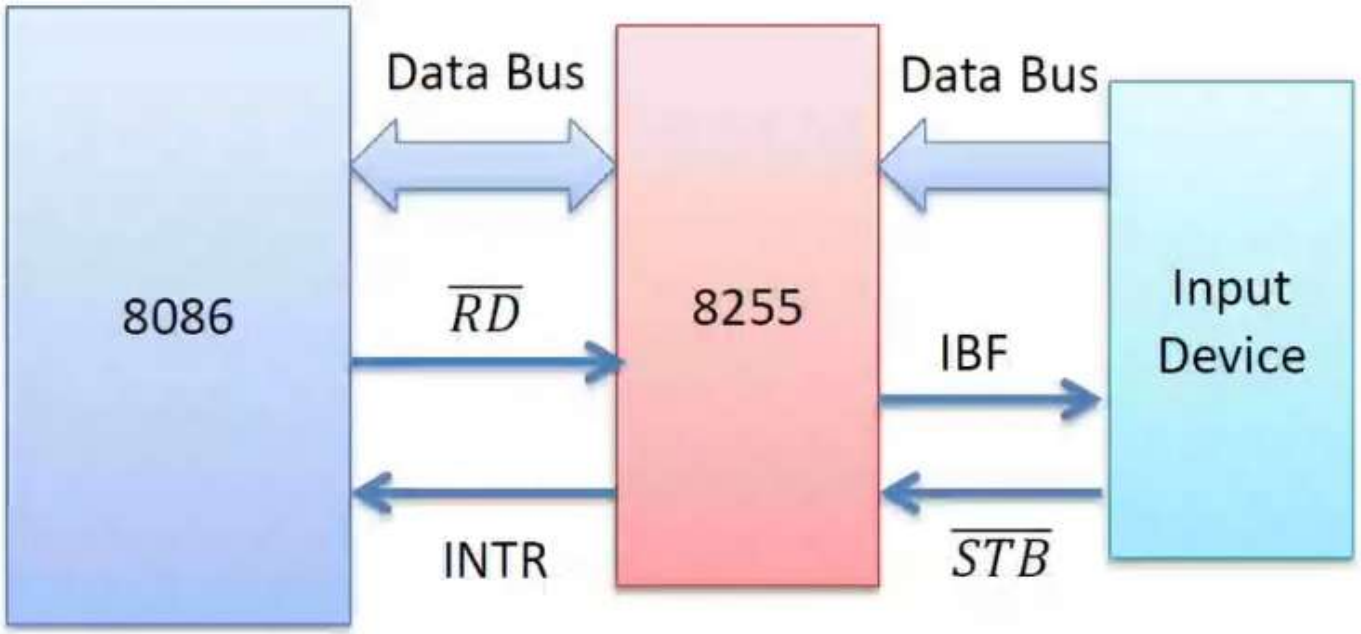
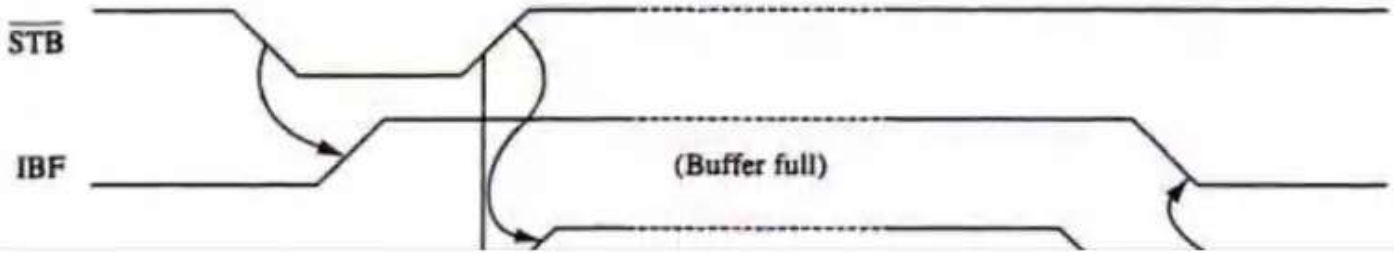


Handshaking Signal (Continued)





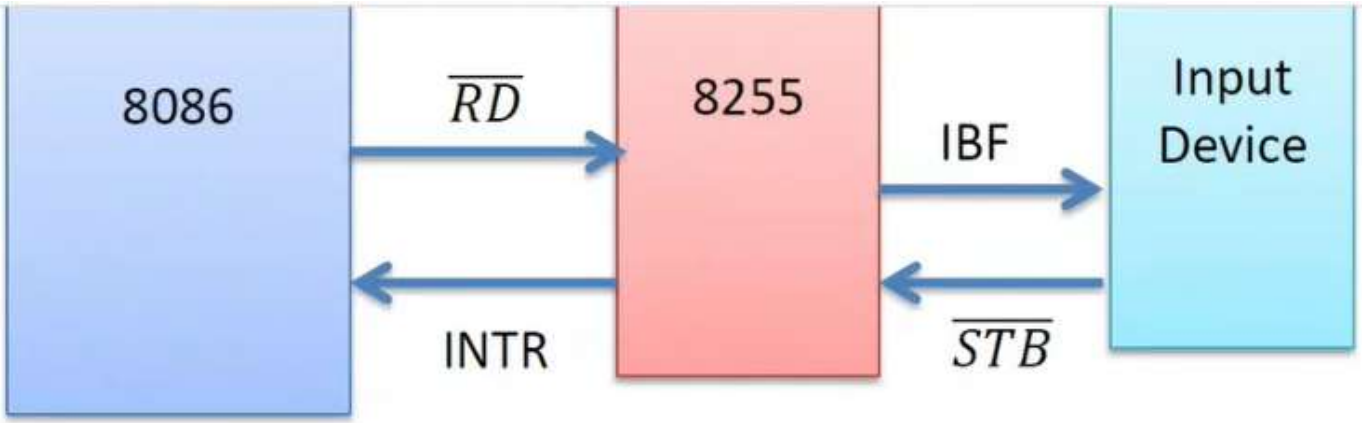
Read Operation

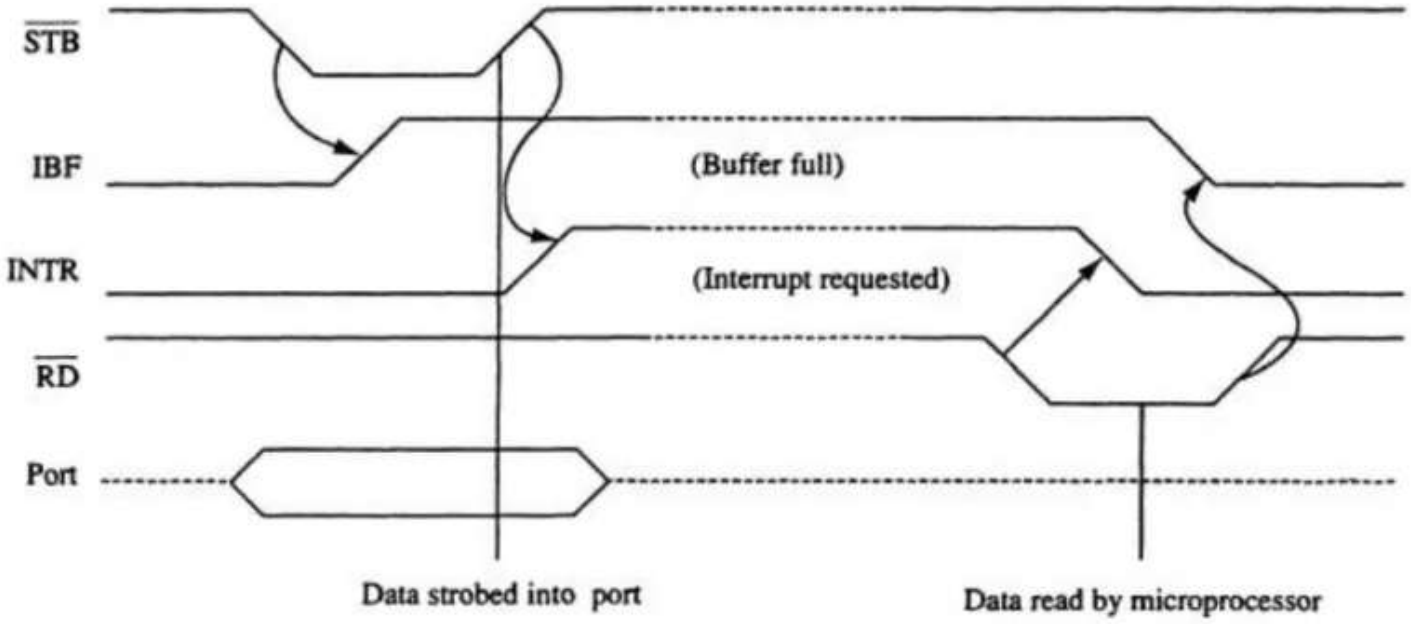
STB goes low indicates that data are loads into port latch.

IBF Becomes high (at high to low transition of STB) indicates that input latch contains data.

INTR Becomes high (at low to high transition of STB) uP goes interrupt subroutine to read data. **RD becomes low.**

IBF becomes low when read complete, RD becomes high and IBF goes low.





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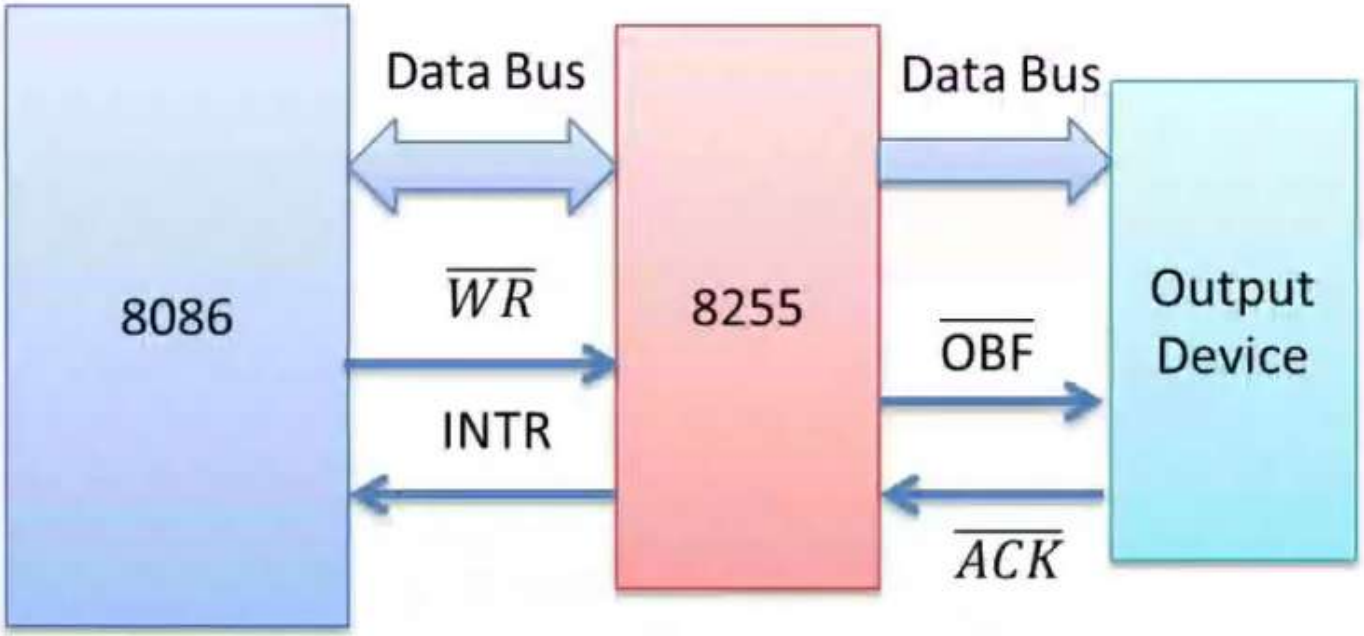
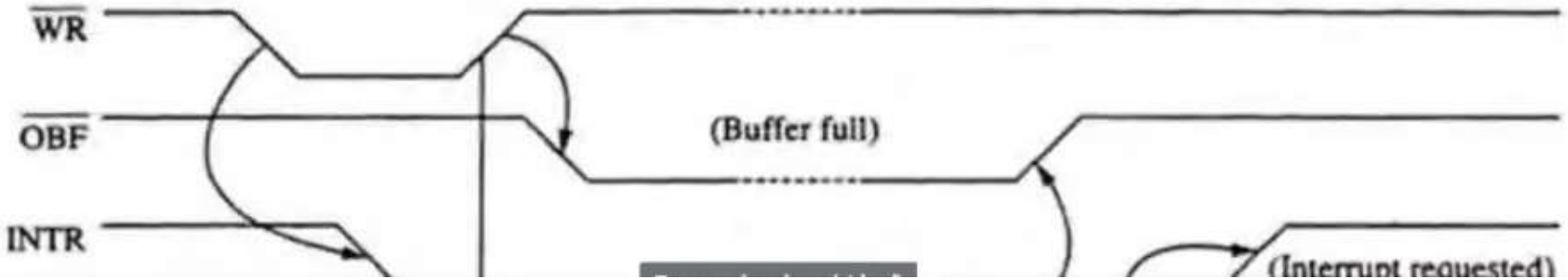
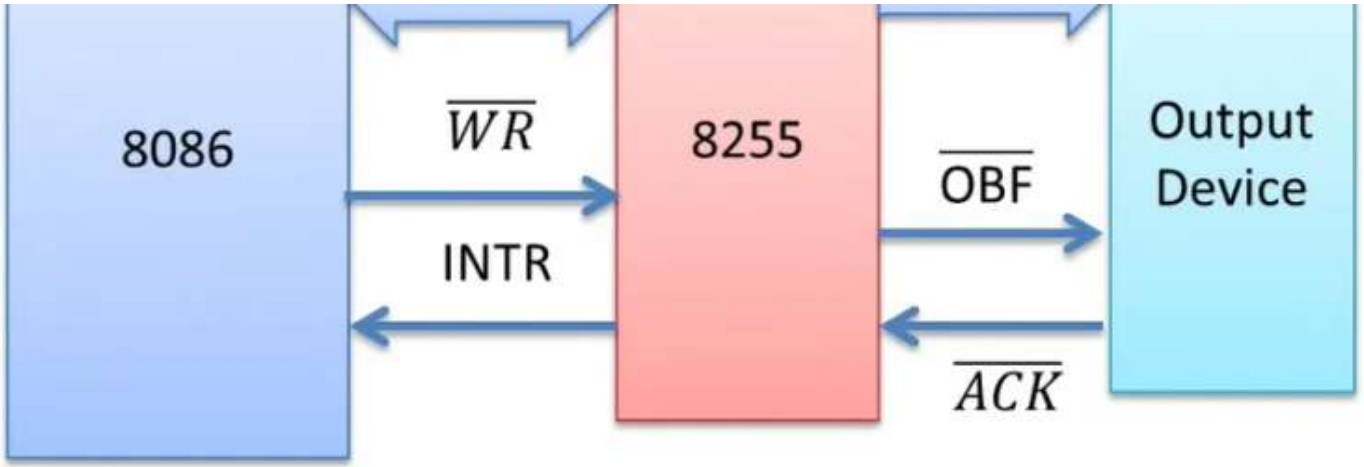
INTR Becomes high (at low to high transition of STB) uP goes interrupt subroutine to read data. **RD becomes low.**

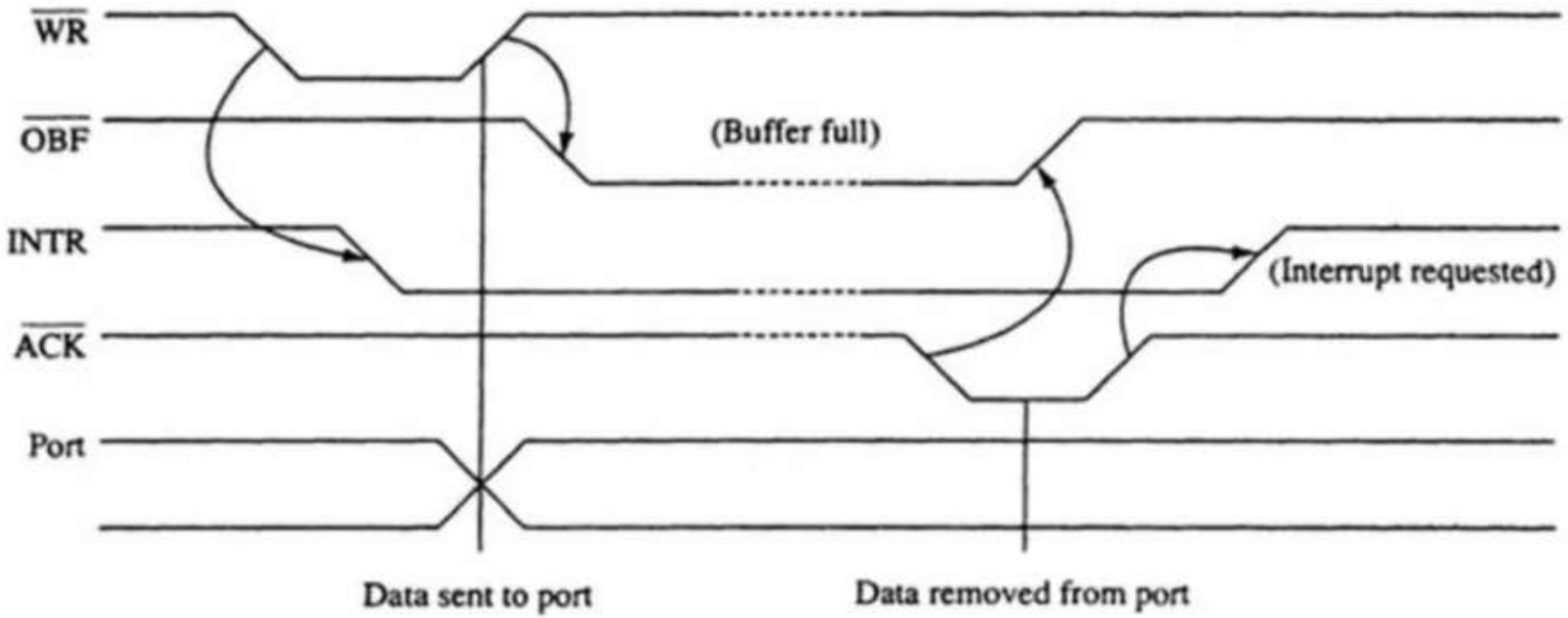
IBF becomes low when read complete, RD becomes high and IBF goes low.
IBF low means input latch has no data (Read complete)

Handshaking Signal (Continued)






8086
$\overline{WR}$
INTR
8255
$\overline{OBF}$
$\overline{ACK}$
Output Device


$\overline{WR}$
$\overline{OBF}$
INTR
$\overline{ACK}$
Port
(Buffer full)
(Interrupt requested)
Data sent to port
Data removed from port

Parallel Data Transfer:

Simple I/O:

This data transfer method is used when the I/O devices need no communication before the data transfer. Such devices are thermostat, LED. The crossed lines on the wave form represent the time at which a new data byte becomes valid on the output lines of the port.

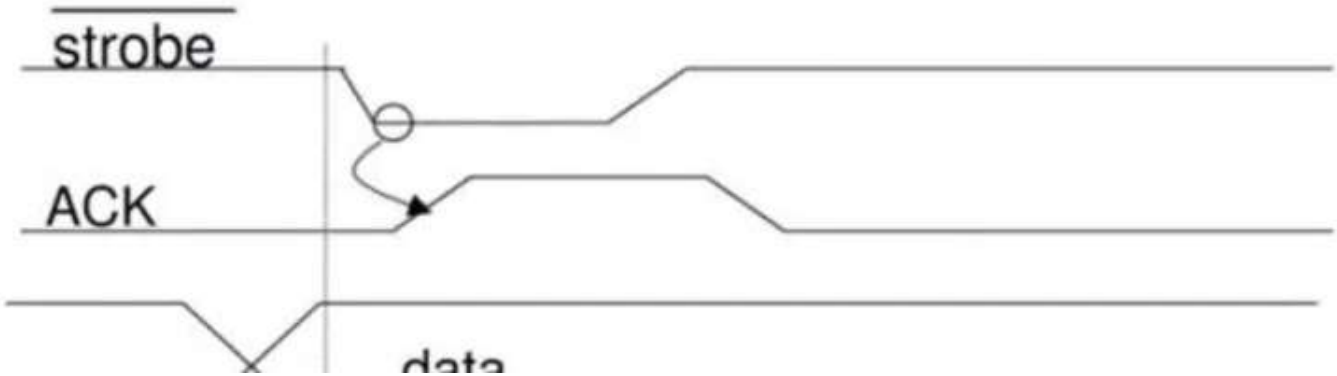
Simple Strobe I/O:

The sending device, such as a keyboard, outputs parallel data on the data lines, and then outputs an $\overline{STB}$ signal to let the receiving device know that valid data is present.

Parallel Data Transfer (Continued):

Single handshake Data transfer:

- The sending device outputs some parallel data and sends an $\overline{STB}$ signal to the receiving device. (i.e. sending device says receiving device, "I have some data for you")
- As a response of $\overline{STB}$ signal receiver device reads data and send an acknowledge signal to indicate that the data has been read. (i.e. by acknowledge signal receiving device says to sending device, "your sending data is received and I am ready to get new data")

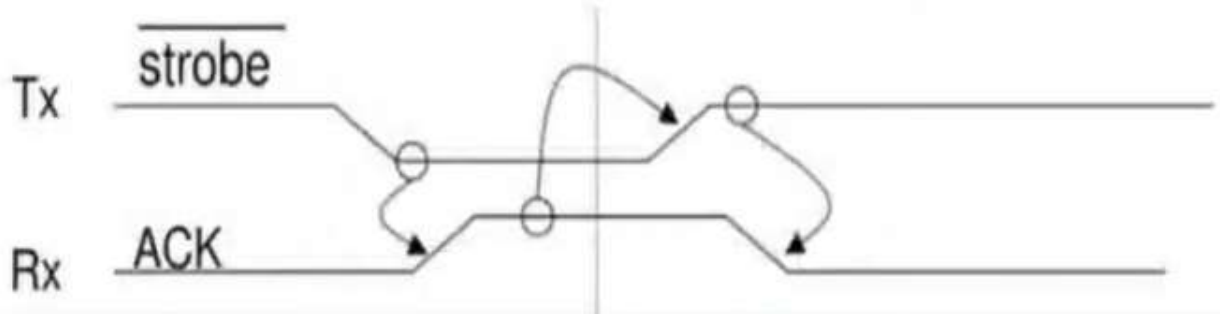


Single Handshake

Parallel Data Transfer (Continued):

Double Handshake Data Transfer:

- The sending device asserts its $\overline{STB}$ line low to ask the receiving device "are you ready?"
- The receiving device raises its ACK line high to say "I am ready".
- The peripheral device then sends the byte of data and raises its $\overline{STB}$ line high to say "Here is some valid data for you".
- After it has read in the data, the receiving data drops its ACK line low to say "I have the data". The receiving device is then ready to be requested for accepting the next data byte.



Programming 8255A

Modes of Operation

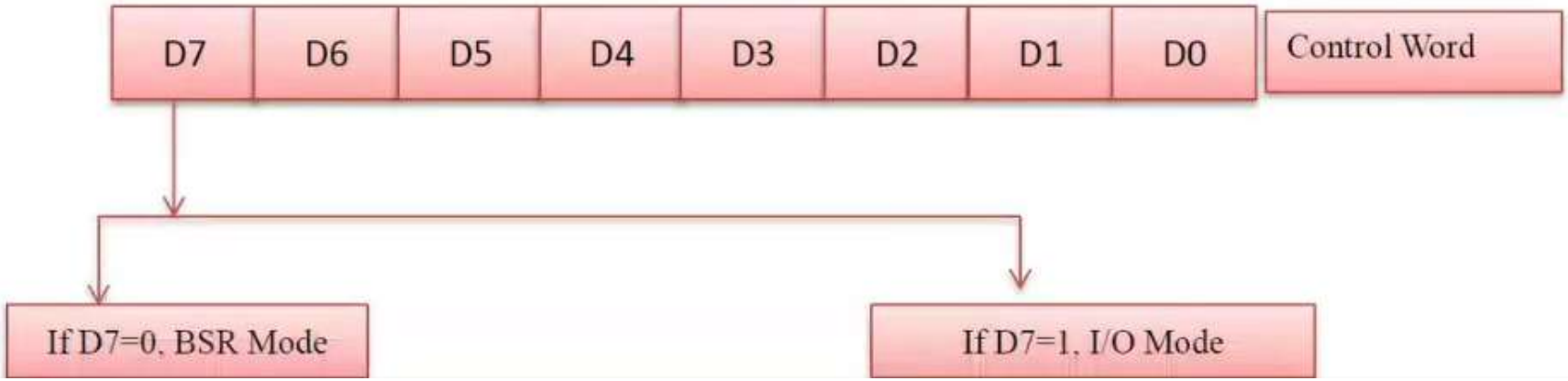
8255 can be configured in two modes

- BSR (Bit Set Reset) Mode
- I/O (Input-Output) Mode: Mode 0, Mode 1 and Mode 2

Modes are configured by Control Word

Control Word

A Control Word is an 8-bit data that stored in control register. Control Words are two types: (a) BSR Control Word (b) Mode definition Control Word



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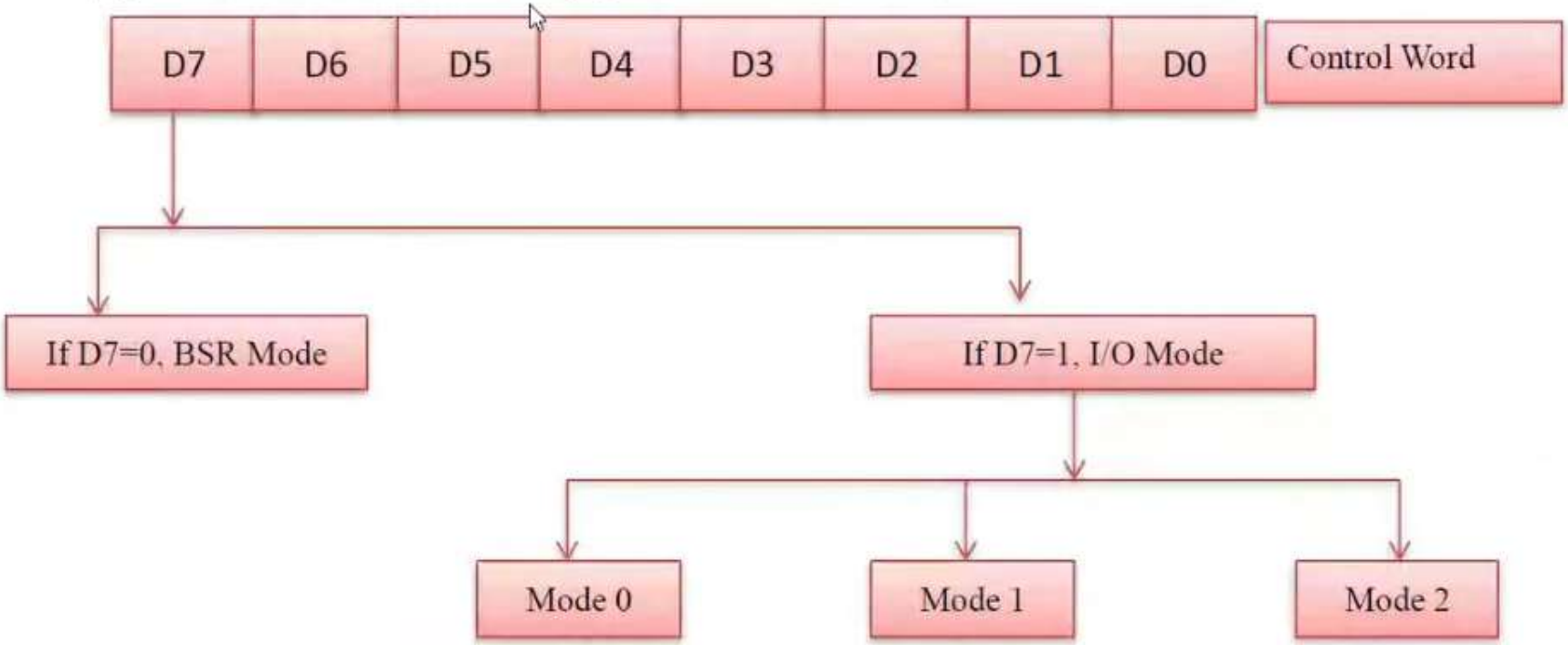
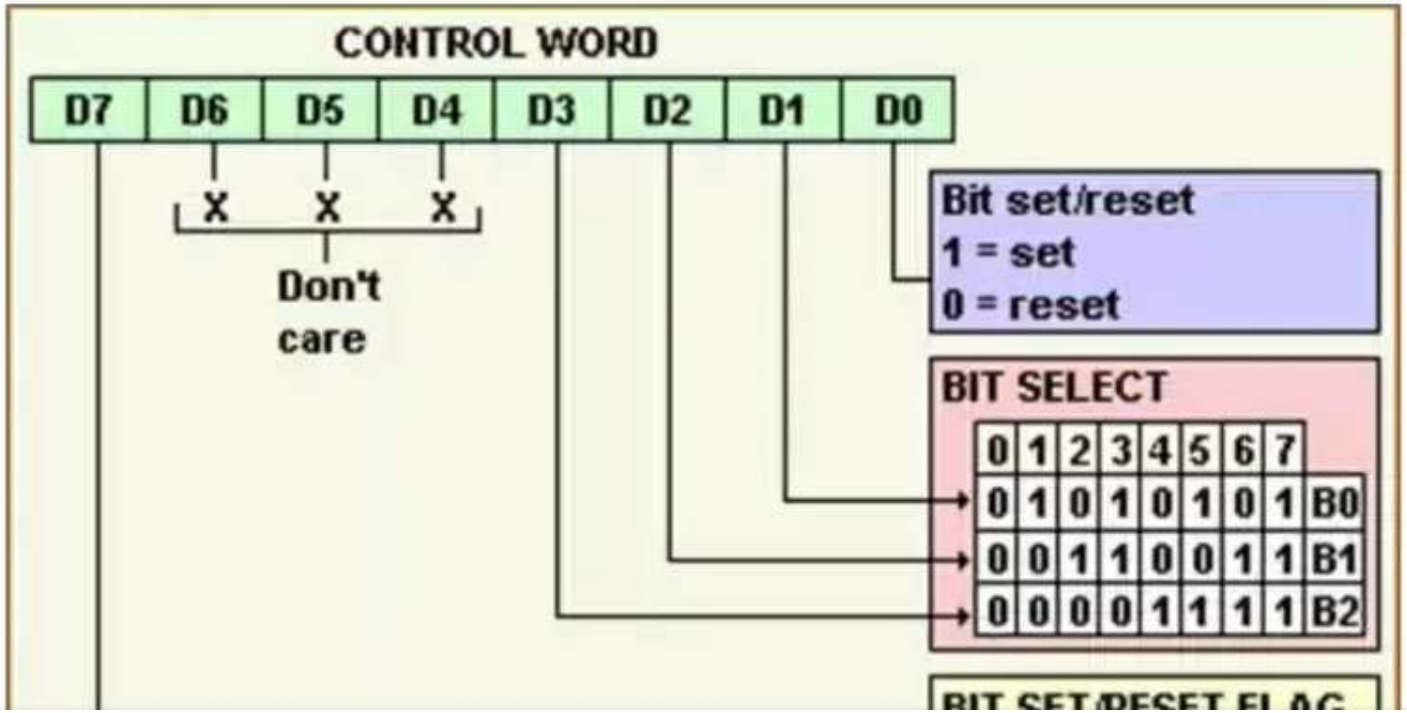


BSR Mode (Configured by Bit Set-Reset Control Word)

- If bit 7 of control word is a logic 0 then 8255 will be configured as BSR (Bit Set Rest) mode.
- In this mode we can set or reset the pins of port C



N.B: *Don't Cares are Generally set as zero.*

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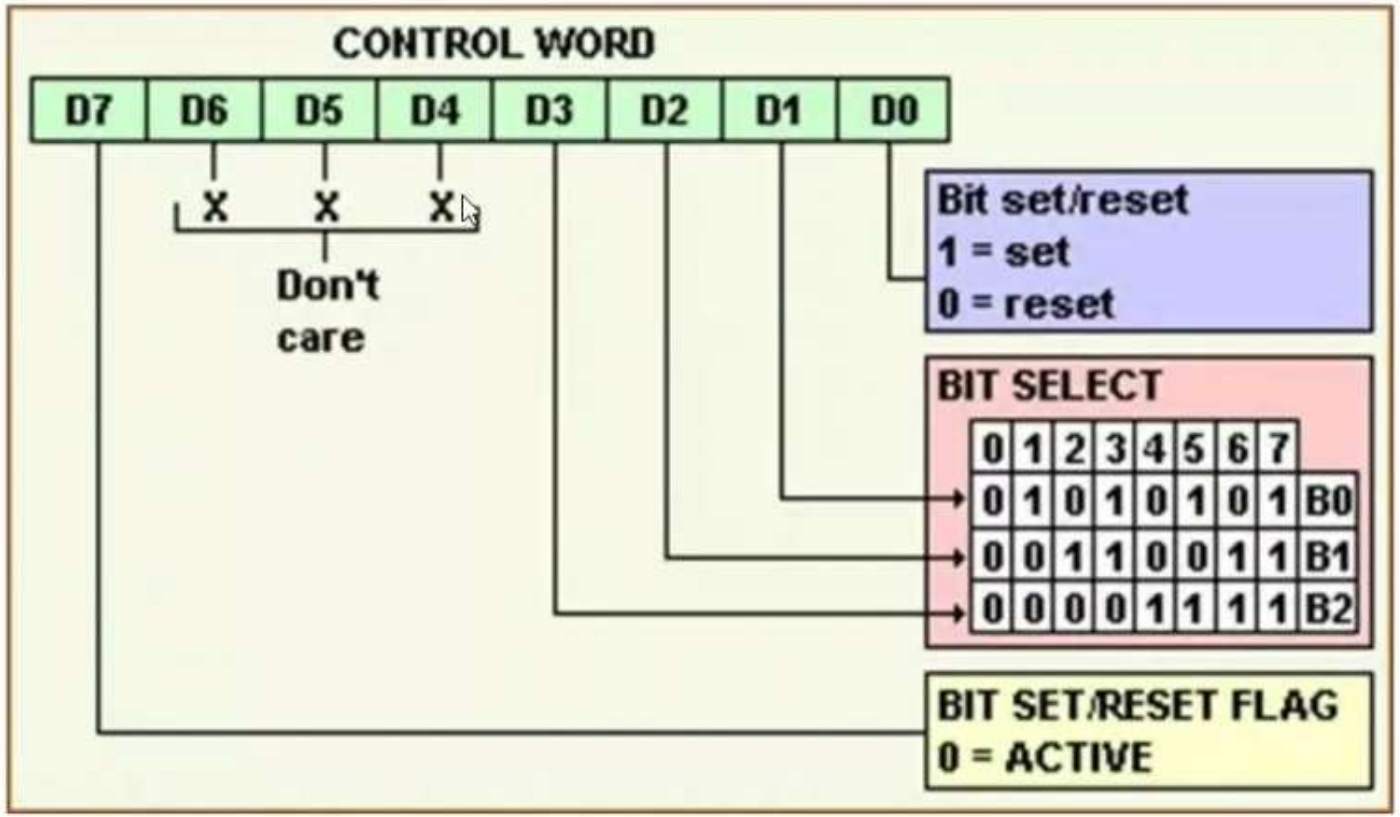

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