DELD

Unit 3

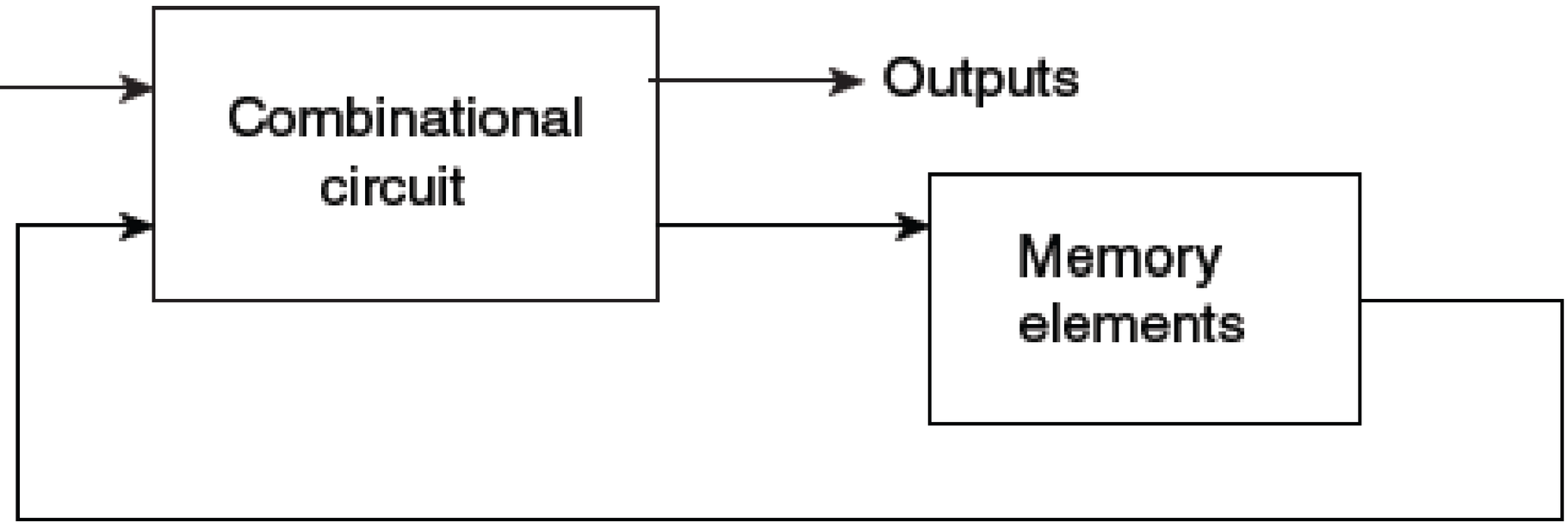
Sequential Circuits

Electronics Engineering Department

Comparison

COMBINATIONAL CIRCUITS	SEQUENTIAL CIRCUITS
Output depends only on the present value of the inputs.	Output depends on both the present and previous state values of the inputs
These circuits will not have any memory as their outputs change with the change in the input value.	Sequential circuits have some sort of memory as their output changes according to the previous and present values.
There are no feedbacks involved.	In a sequential circuit the outputs are connected to it as a feedback path.
Used in basic Boolean operations.	Used in the designing of memory devices.
Implemented in: Half adder circuit, full adder circuit, multiplexers, de-multiplexers, decoders and encoders.	Implemented in: RAM, Registers, counters and other state retaining machines.

Block Diagram



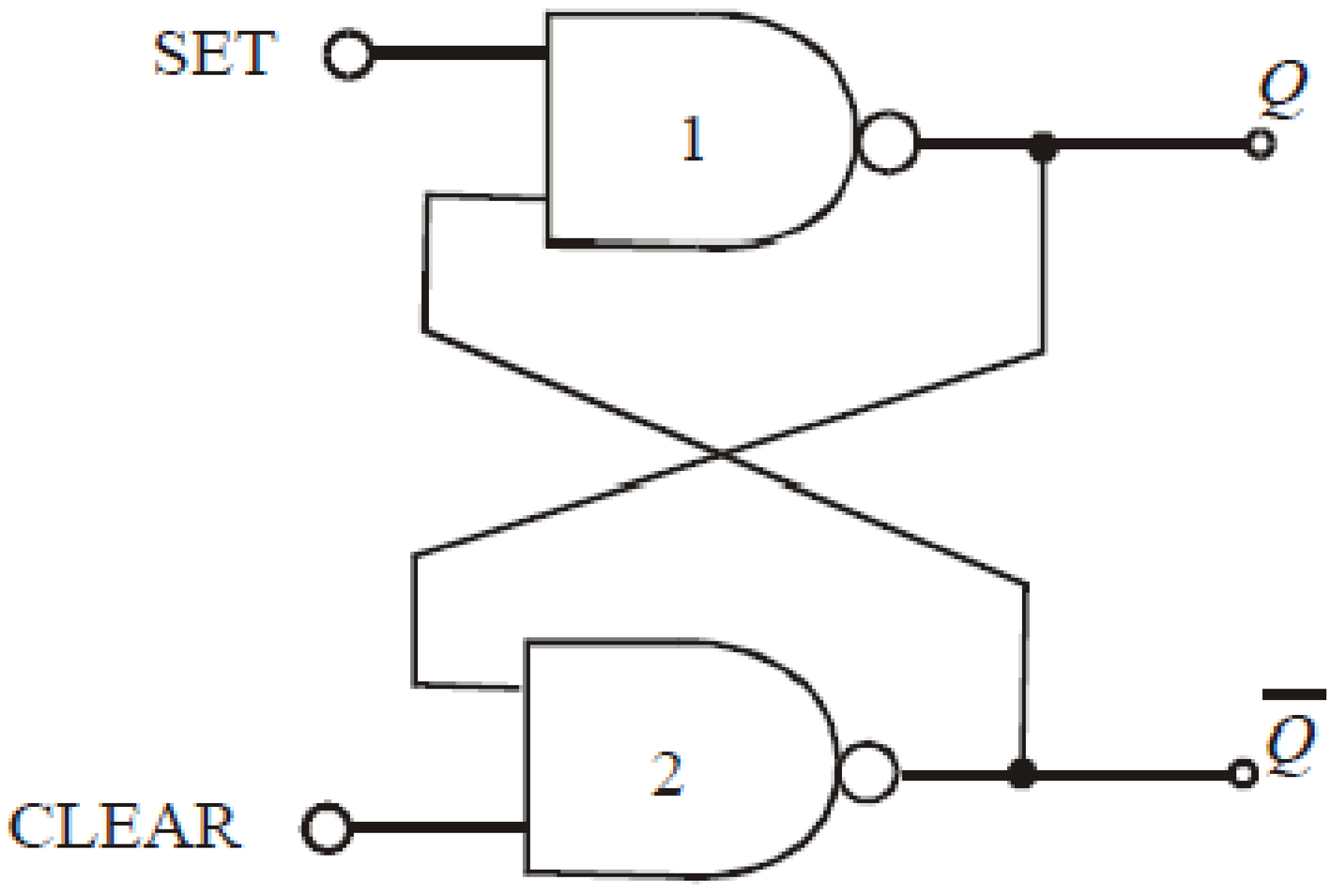
Flip – Flops and its Types

- Basic Memory element of a Digital Computer
- Stores 1 bit of information
- It’s a Bistable device
- Has two outputs, one complement of another (Q and Q’)
- Four Types
  - SR
  - D
  - JK
  - T

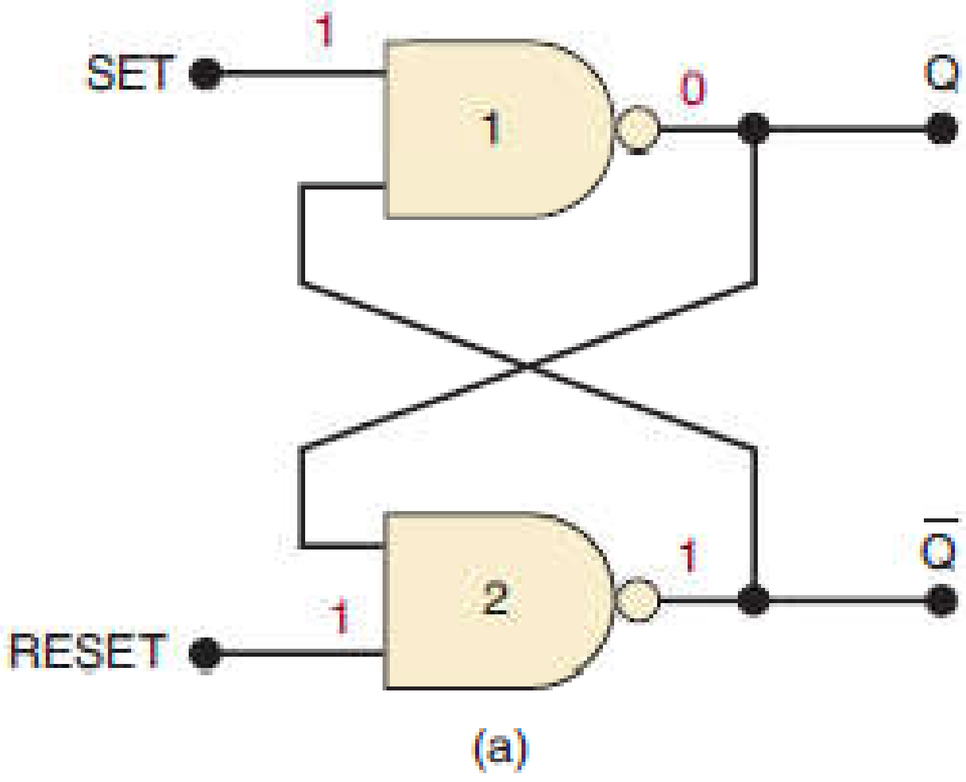
Concept of Latch

- Most basic type of FF circuit
- Can be constructed using NAND or NOR Gates
- These circuits latch to ‘1’ or ‘0’ immediately upon application of inputs
- Two types
  - NAND Gate Latch (Active Low)
  - NOR Gate Latch (Active High)

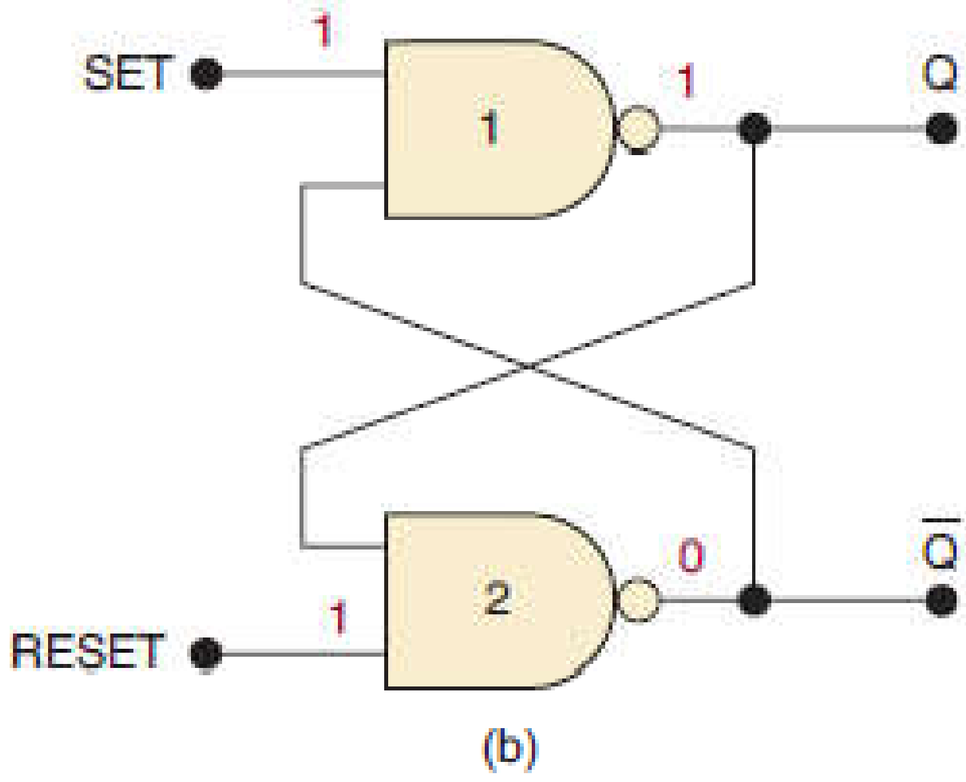
NAND Gate SR Latch



Two Stable States

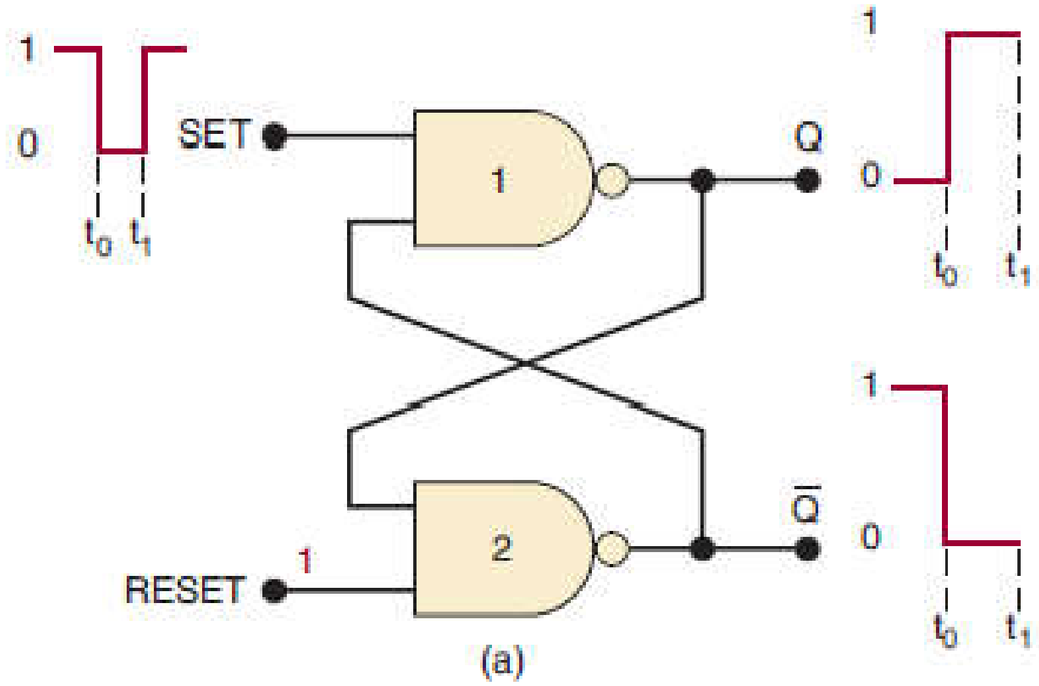


(a)

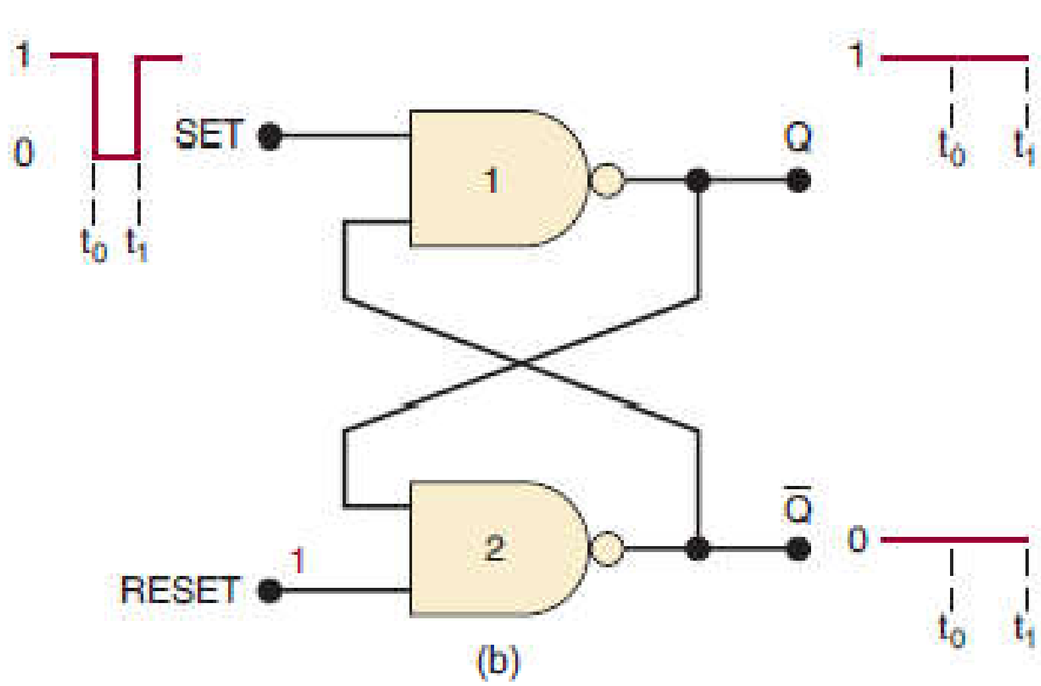


(b)

SET (Q=1)

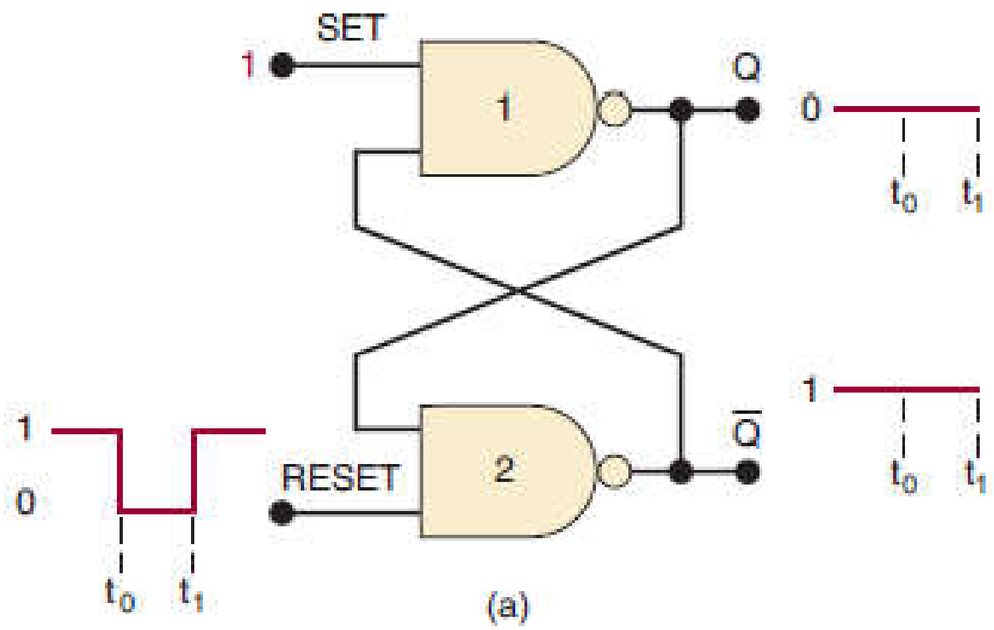

1
0
SET
Q
1
t_0 t_1
1
0
t_0 t_1
$\overline{Q}$
2
1
RESET
1
0
t_0 t_1

(a)

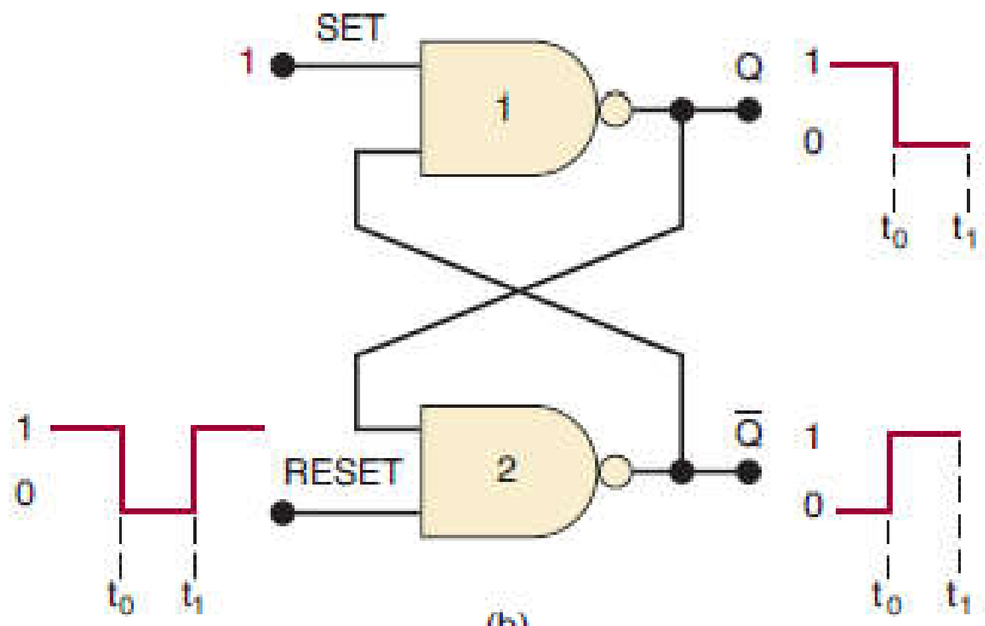

1
0
SET
Q
1
t_0 t_1
$\overline{Q}$
2
1
RESET
1
0
t_0 t_1

(b)

RESET (Q=0)


SET
1
1
Q
0
t_0 t_1
1
0
t_0 t_1
RESET
2
$\overline{Q}$
1
t_0 t_1

(a)

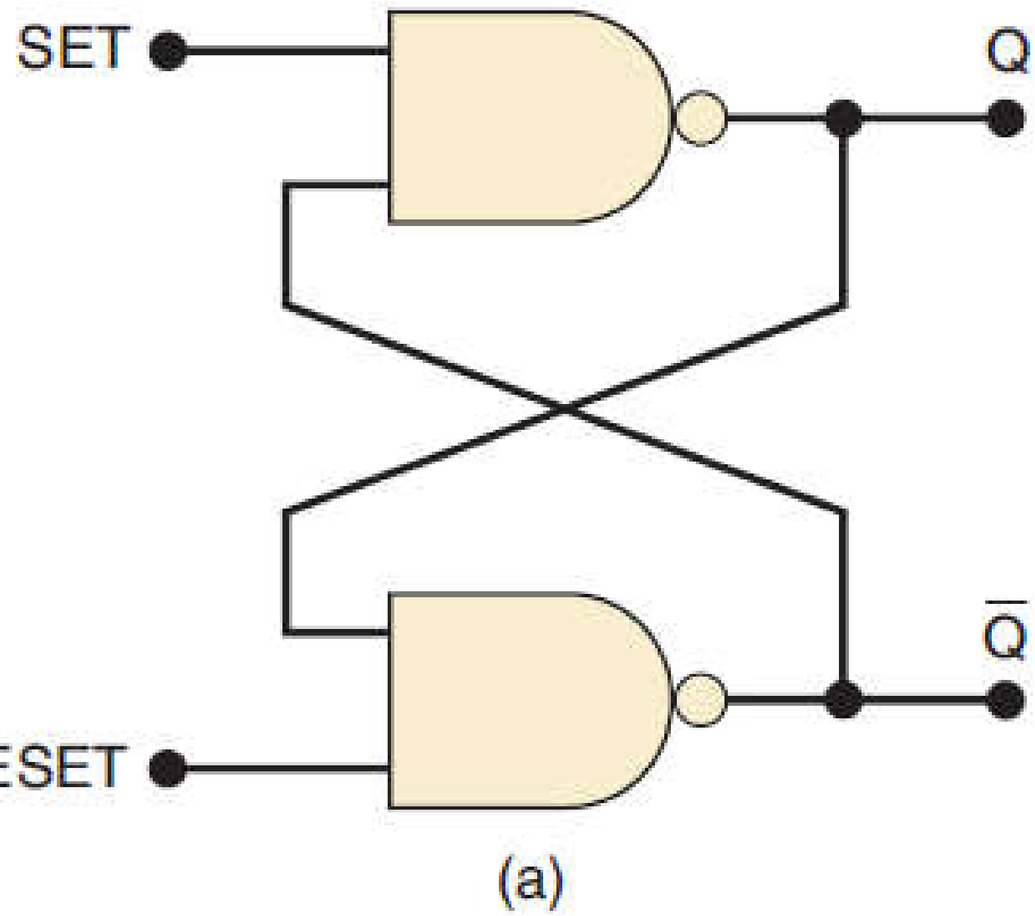

SET
1
1
Q
1
0
t_0 t_1
1
0
t_0 t_1
RESET
2
$\overline{Q}$
1
0
t_0 t_1

(b)

Summary

1. SET = RESET = 1. This condition is the normal resting state, and it has no effect on the output state. The Q and $\overline{Q}$ outputs will remain in whatever state they were in prior to this input condition.
2. SET = 0, RESET = 1. This will always cause the output to go to the $Q = 1$ state, where it will remain even after SET returns HIGH. This is called *setting* the latch.
3. SET = 1, RESET = 0. This will always produce the $Q = 0$ state, where the output will remain even after RESET returns HIGH. This is called *clearing* or *resetting* the latch.
4. SET = RESET = 0. This condition tries to set and clear the latch at the same time, and it produces $Q = \overline{Q} = 1$. If the inputs are returned to 1 simultaneously, the resulting state is unpredictable. This input condition should not be used.

Truth Table



(a)

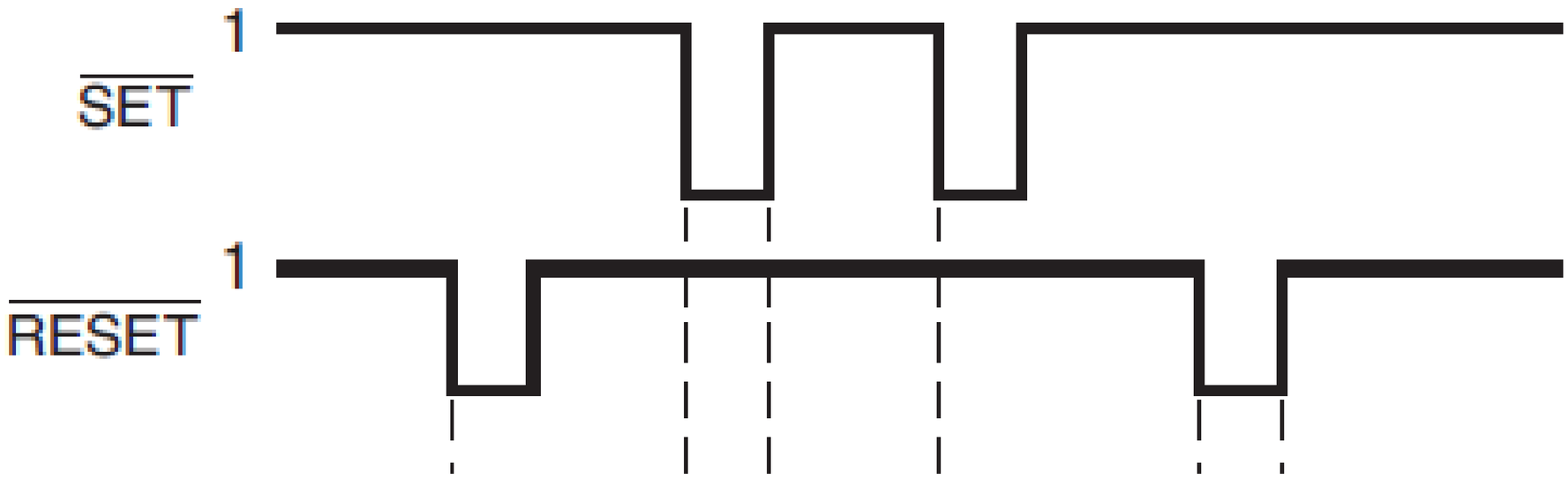
Set	Reset	Output
1	1	No change
0	1	Q = 1
1	0	Q = 0
0	0	Invalid *

*Produces $Q = \overline{Q} = 1$.

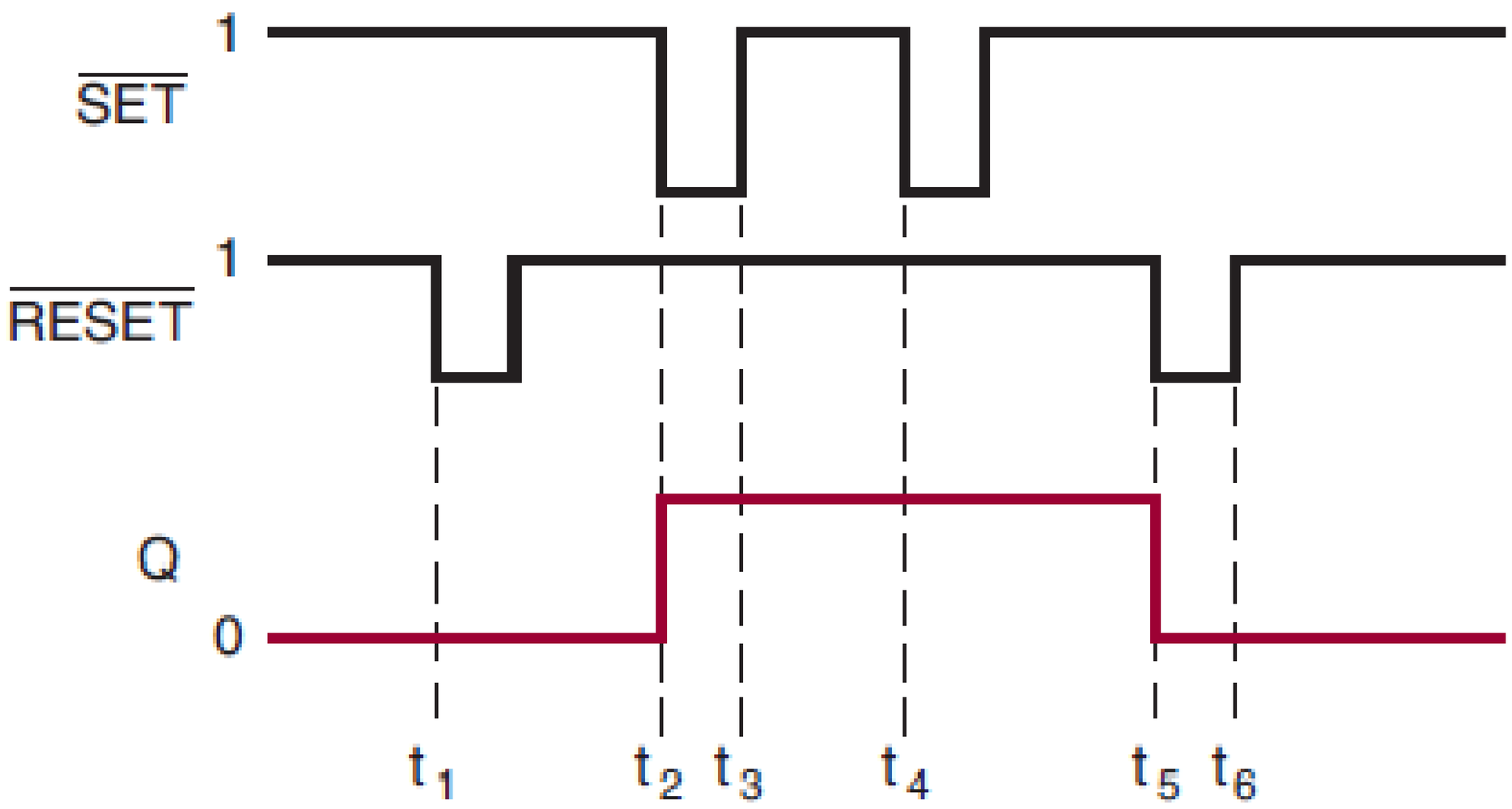
(b)

Concept Check

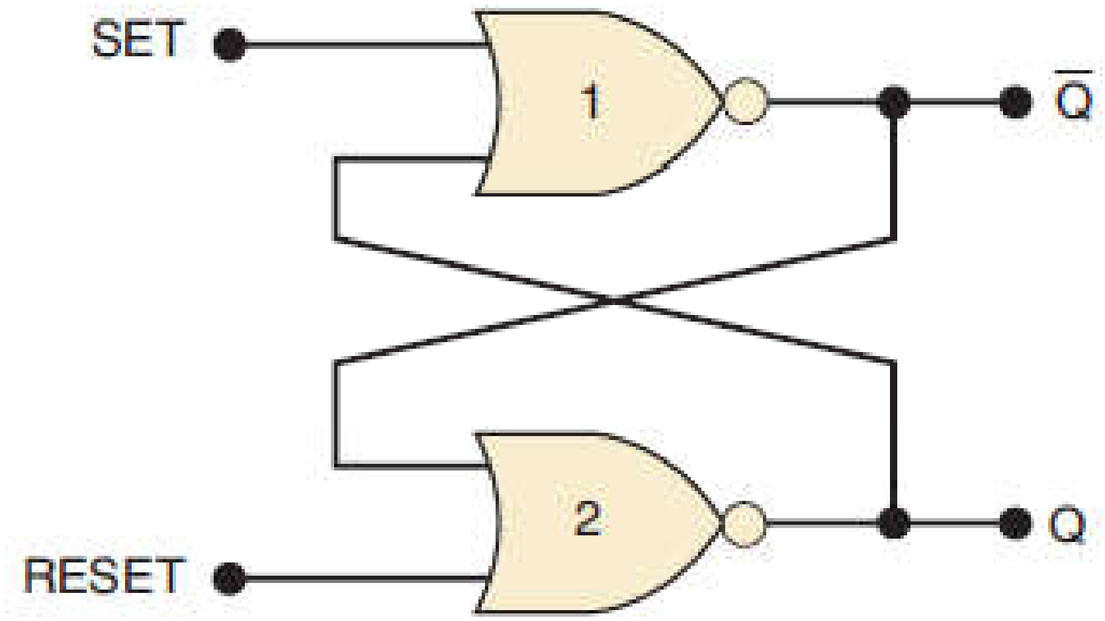
Assuming the Q=0 initially, determine the Q waveform for the NAND Latch



Solution

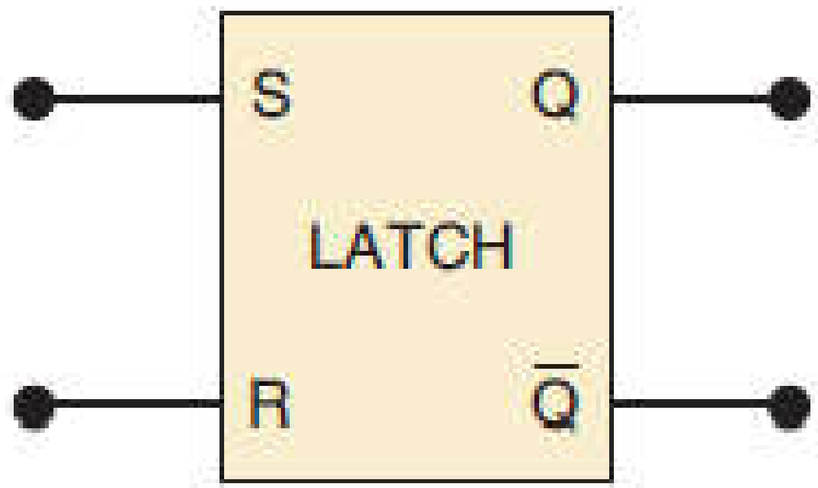


NOR Gate SR Latch



Set	Reset	Output
0	0	No change
1	0	Q = 1
0	1	Q = 0
1	1	Invalid*

*Produces $Q = \overline{Q} = 0$.

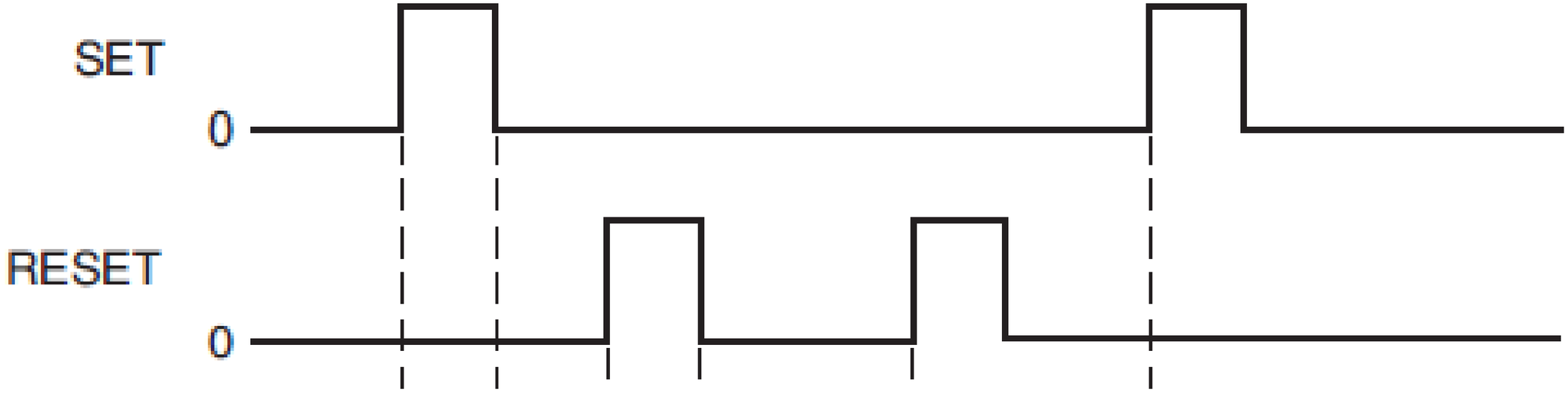


Description

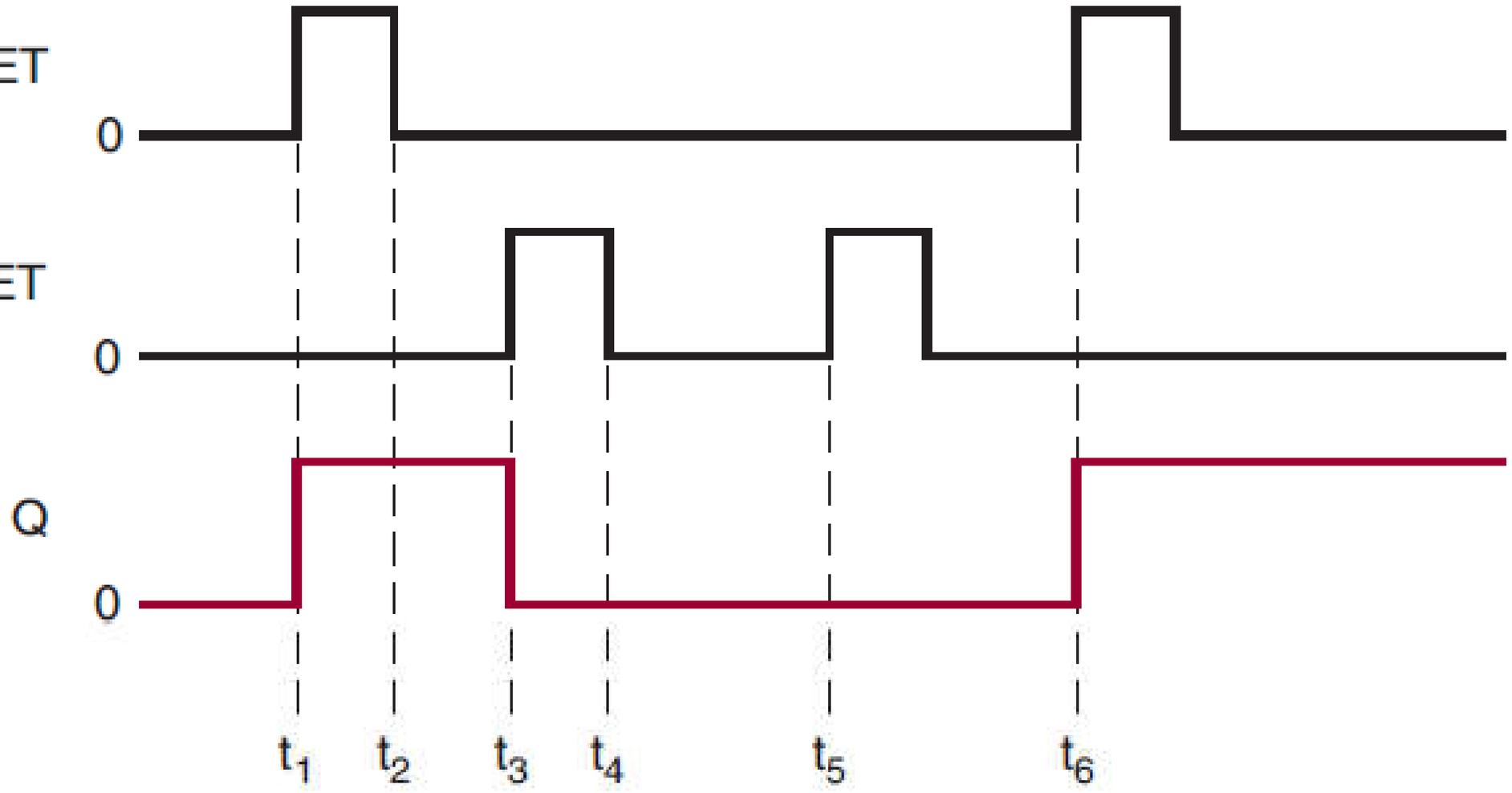
1. SET = RESET = 0. This is the normal resting state for the NOR latch, and it has no effect on the output state. Q and $\overline{Q}$ will remain in whatever state they were in prior to the occurrence of this input condition.
2. SET = 1, RESET = 0. This will always set $Q = 1$, where it will remain even after SET returns to 0.
3. SET = 0, RESET = 1. This will always clear $Q = 0$, where it will remain even after RESET returns to 0.
4. SET = 1, RESET = 1. This condition tries to set and reset the latch at the same time, and it produces $Q = \overline{Q} = 0$. If the inputs are returned to 0 simultaneously, the resulting output state is unpredictable. This input condition should not be used.

Concept Check

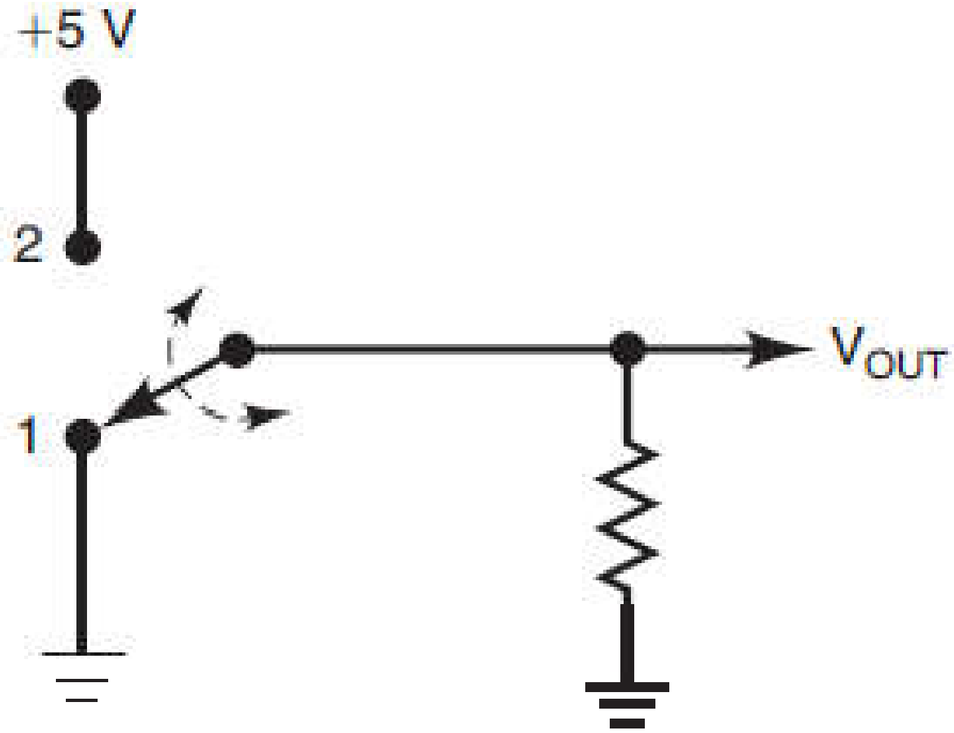
Assuming the Q=0 initially, determine the Q waveform for the NOR Latch



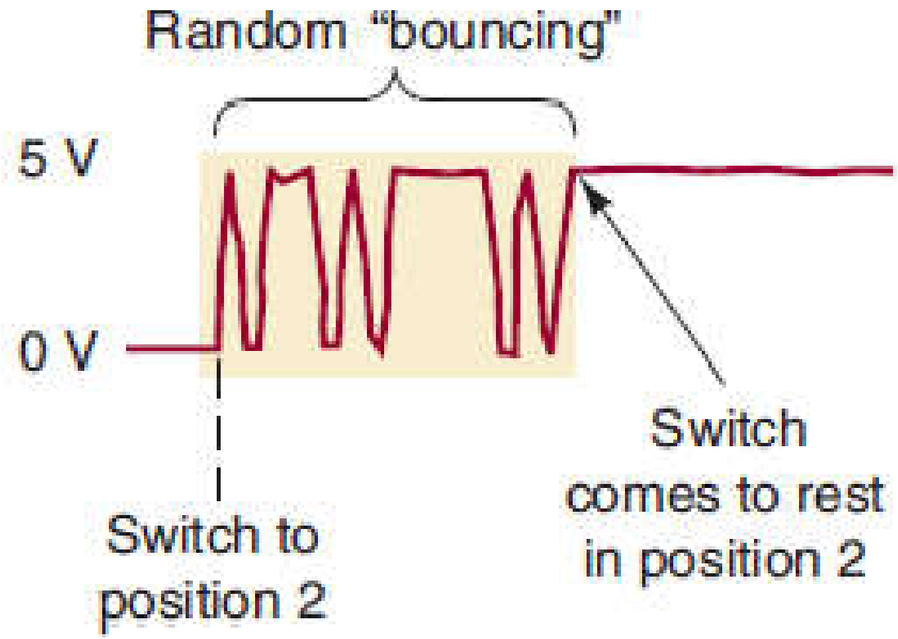
Solution



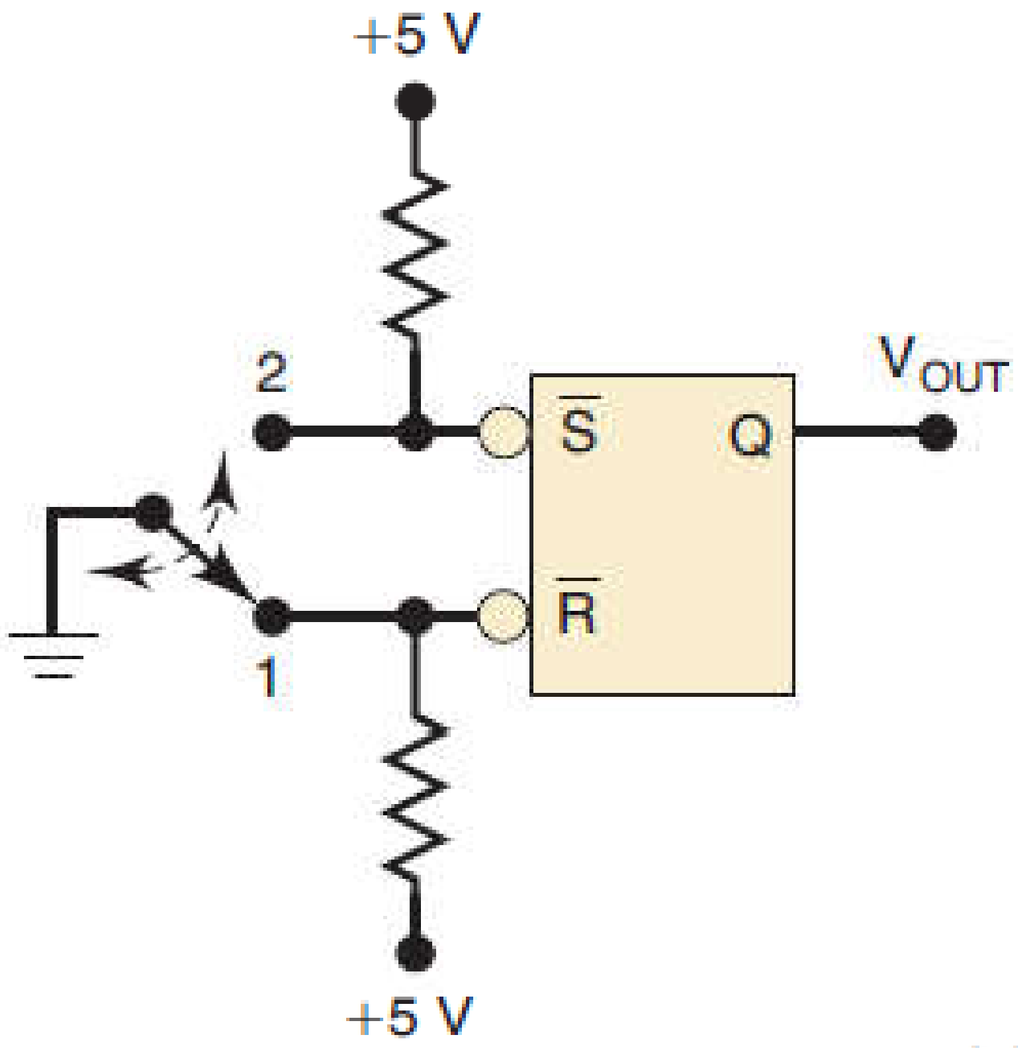
Elimination of Switch De-bounce



(a)



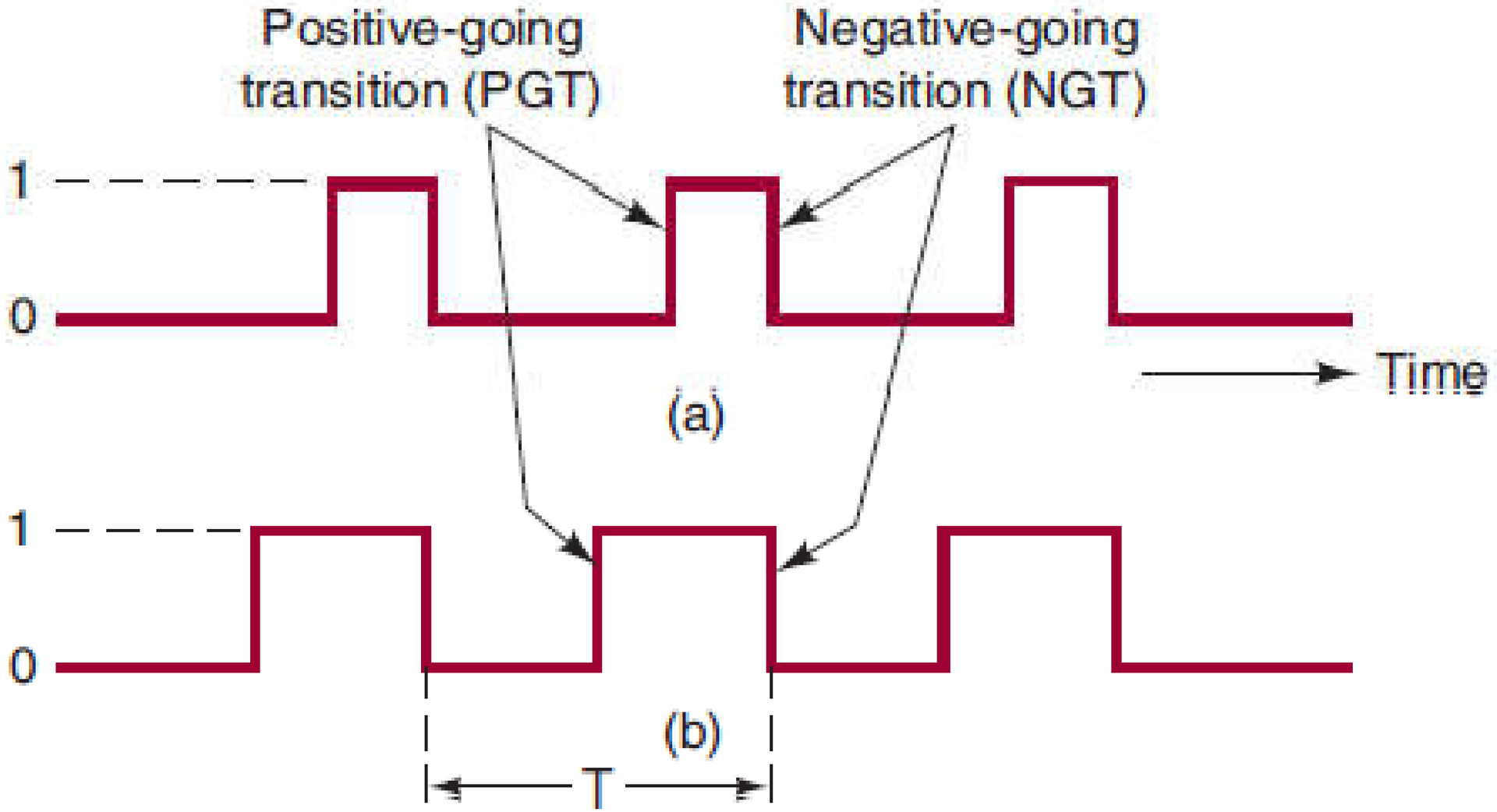
Switch Debounce Cont…



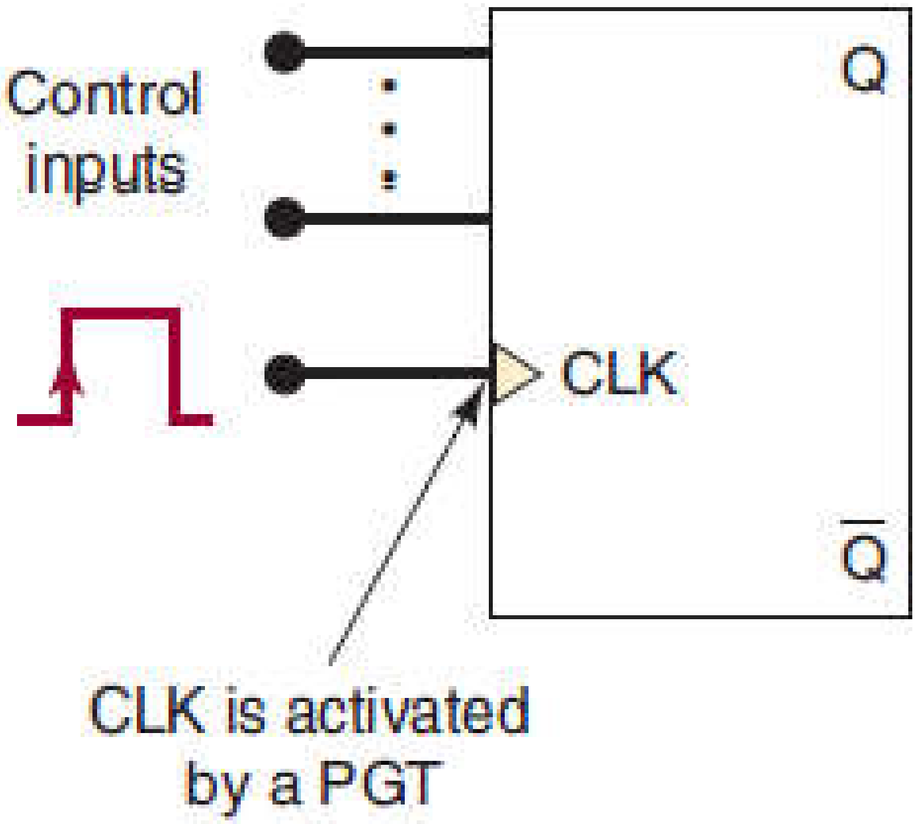
Flip – Flop State on Power UP

When power is applied to a circuit, it is not possible to predict the starting state of a flip-flop's output if its SET and RESET inputs are in their inactive state (e.g., $S = R = 1$ for a NAND latch, $S = R = 0$ for a NOR latch). There is just as much chance that the starting state will be $Q = 0$ as $Q = 1$. It will depend on factors such as internal propagation delays, parasitic capacitance, and external loading. If a latch or FF must start off in a particular state to ensure the proper operation of a circuit, then it must be placed in that state by momentarily activating the SET or RESET input at the start of the circuit's operation. This is often achieved by application of a pulse to the appropriate input.

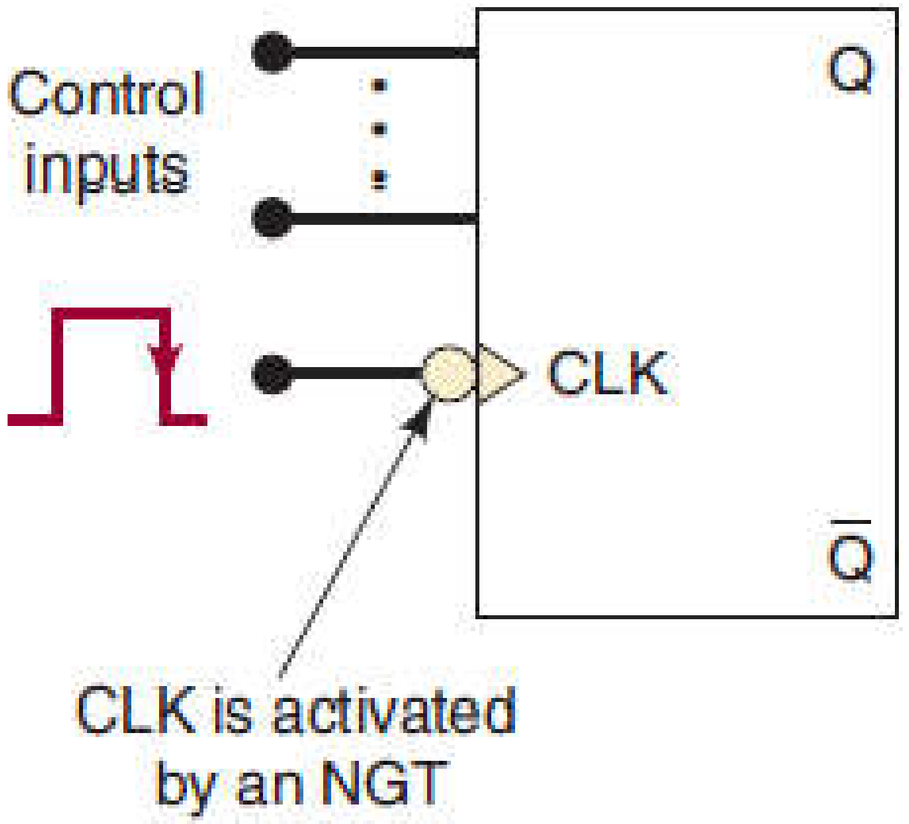
Concept of Pulse and Edge



PET & NET

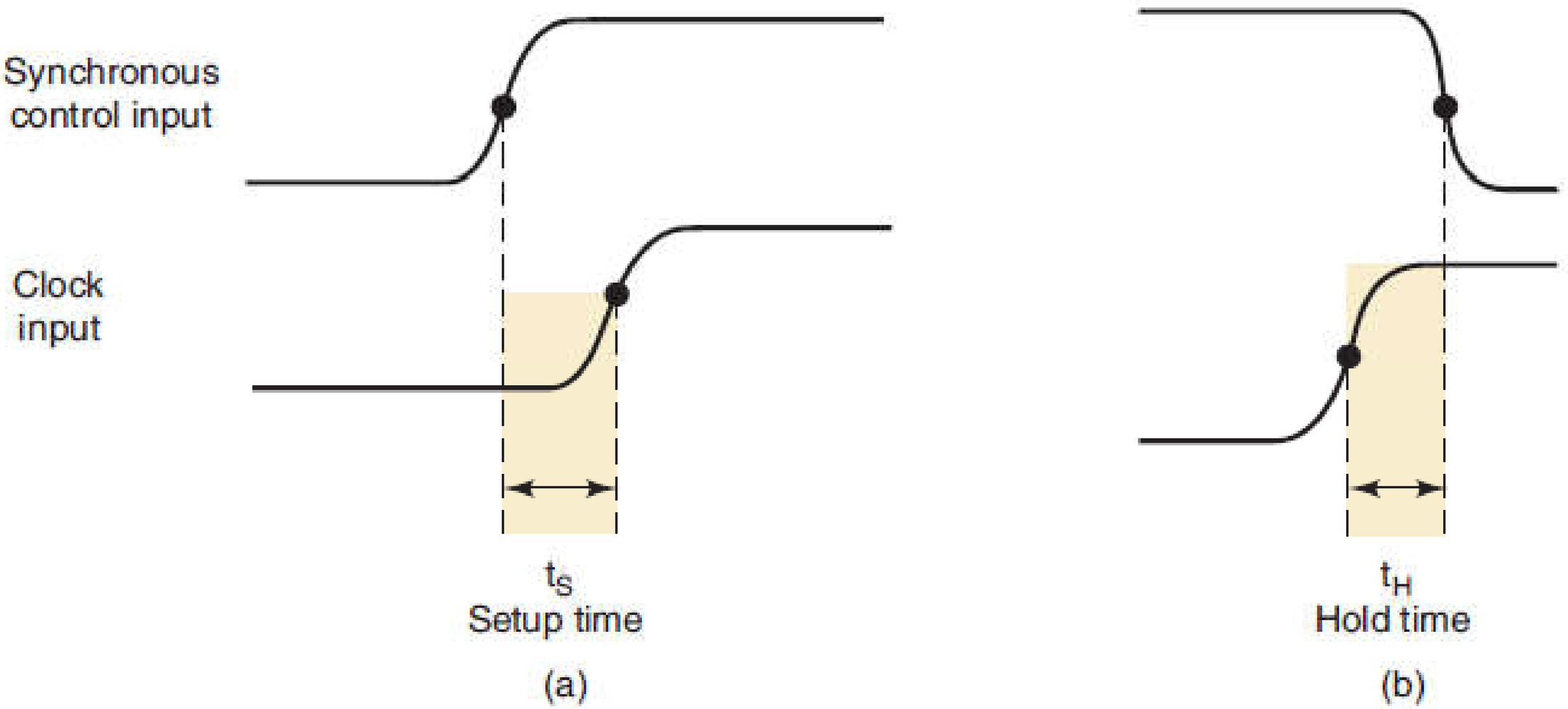

Control inputs
Q
CLK
$\overline{Q}$
CLK is activated by a PGT

(a)

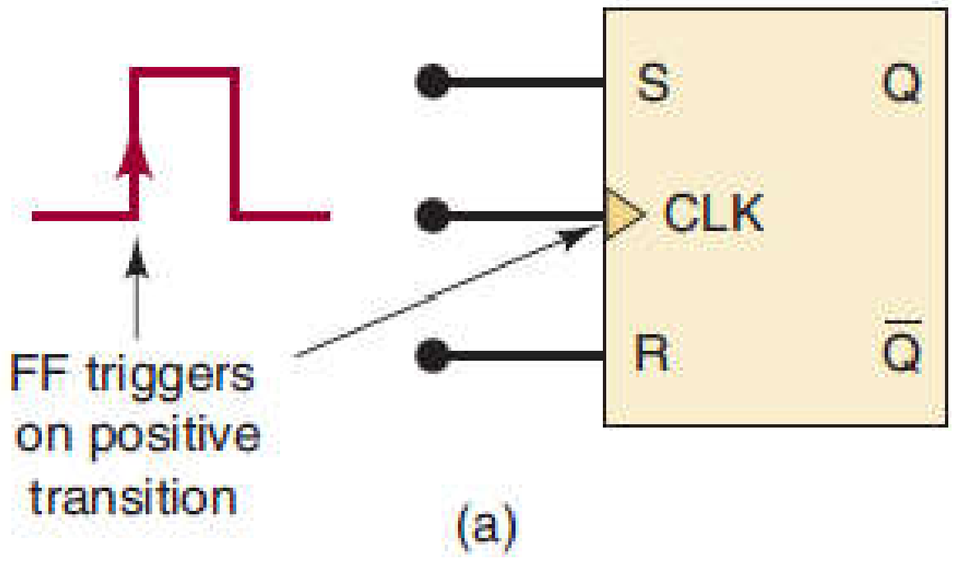

Control inputs
Q
CLK
$\overline{Q}$
CLK is activated by an NGT

(b)

Setup & Hold Times



Clocked SR Flip-Flop



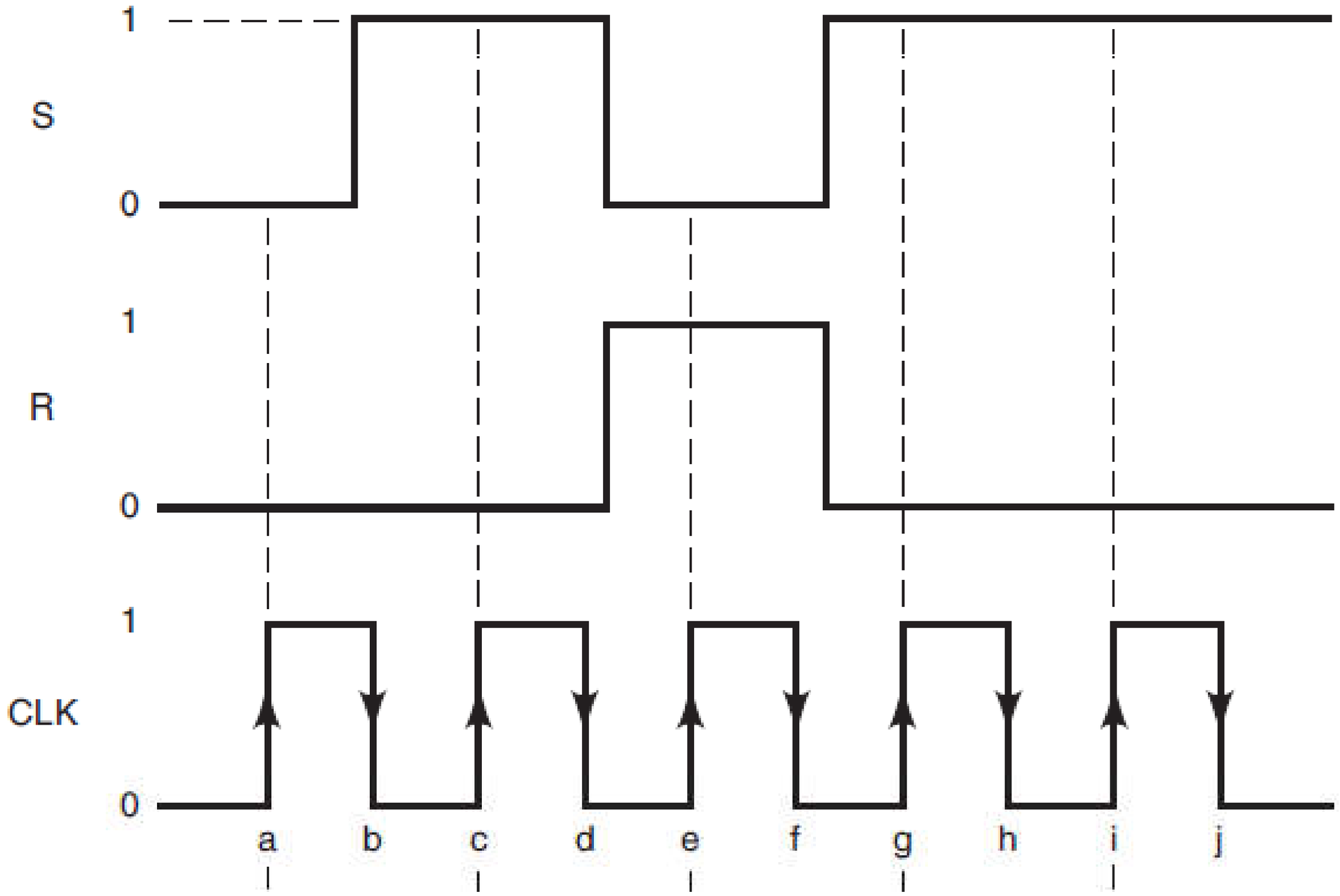
(a)

Inputs			Output
S	R	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

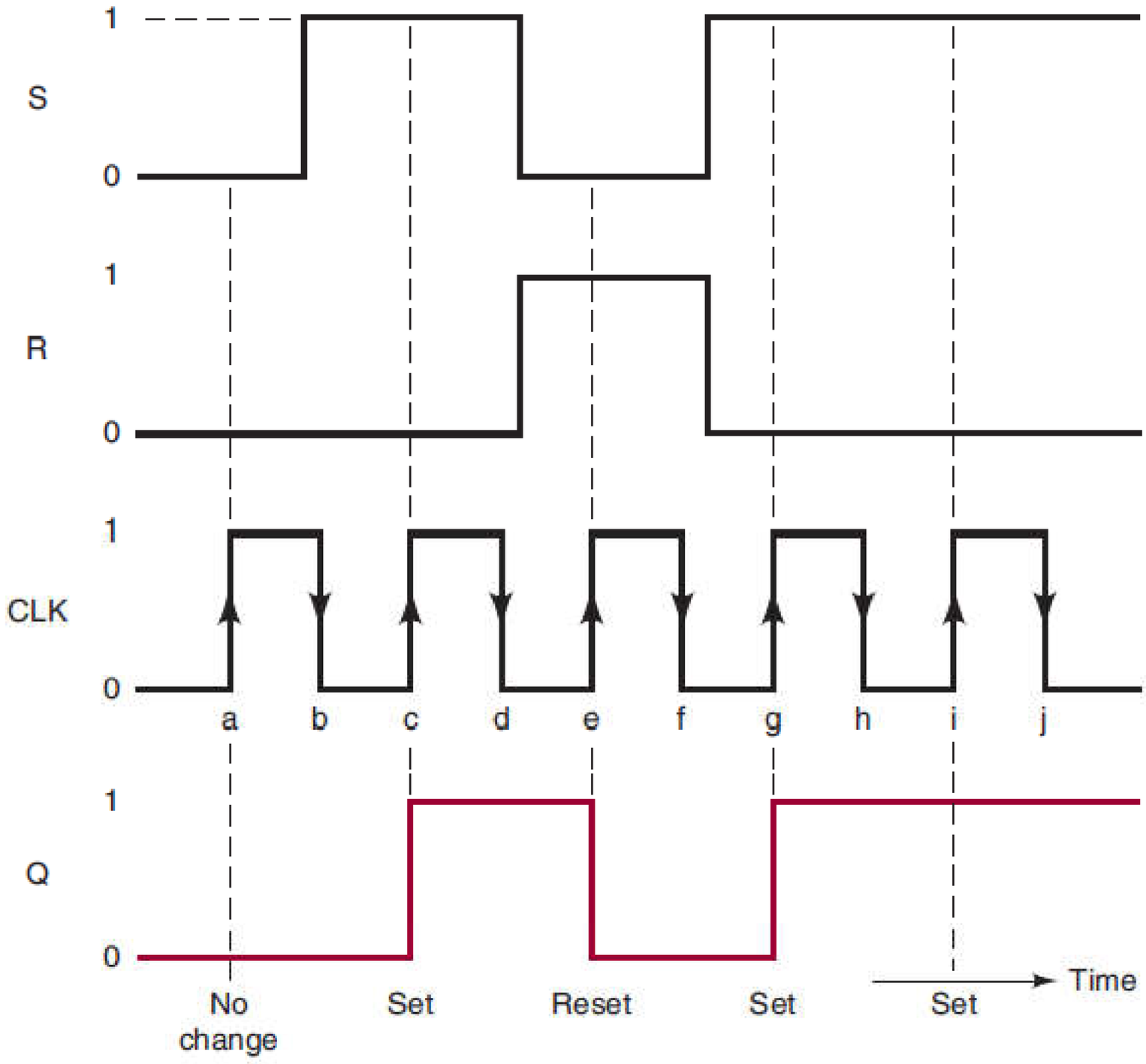
Q_0 is output level prior to ↑ of CLK.
↓ of CLK produces no change in Q.

(b)

Predict the Output



Solution

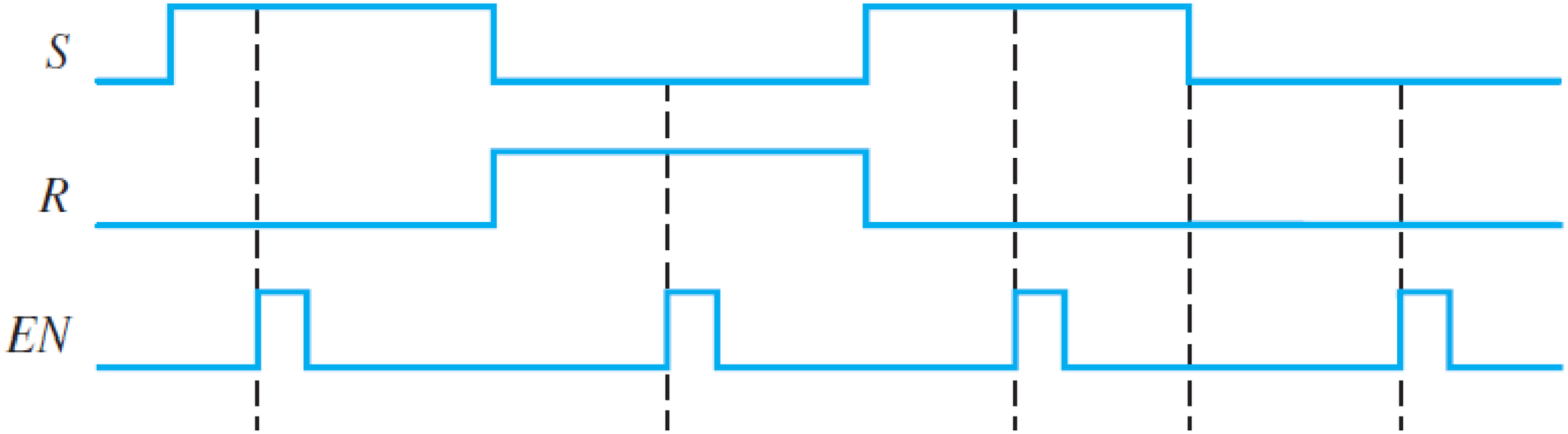


Explanation

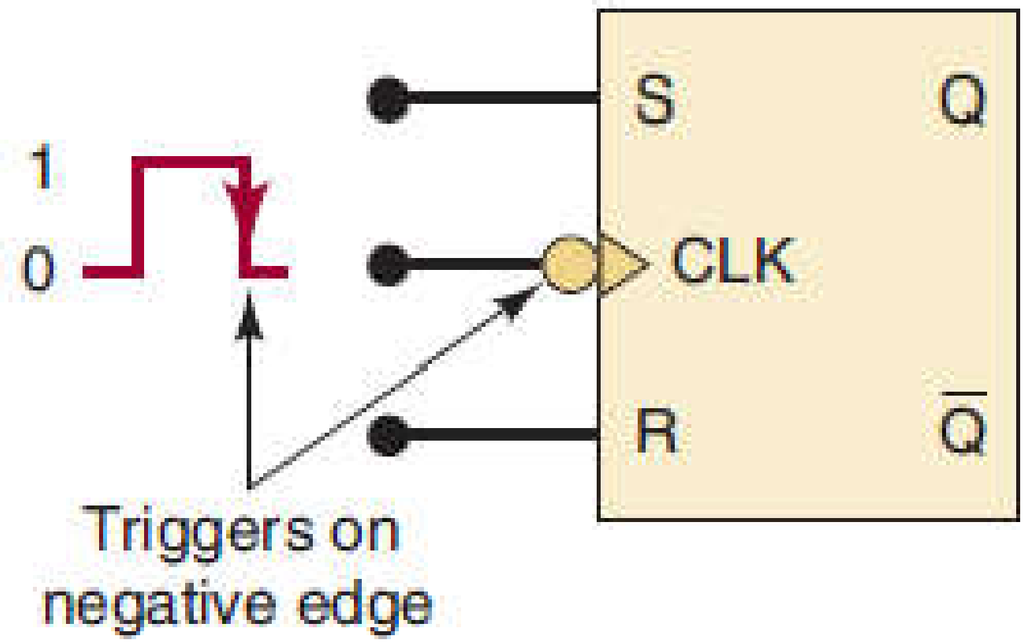
1. Initially all inputs are 0 and the Q output is assumed to be 0; that is, $Q_0 = 0$.
2. When the PGT of the first clock pulse occurs (point a), the S and R inputs are both 0, so the FF is not affected and remains in the $Q = 0$ state (i.e., $Q = Q_0$).
3. At the occurrence of the PGT of the second clock pulse (point c), the S input is now HIGH, with R still LOW. Thus, the FF sets to the 1 state at the rising edge of this clock pulse.
4. When the third clock pulse makes its positive transition (point e), it finds that $S = 0$ and $R = 1$, which causes the FF to clear to the 0 state.
5. The fourth pulse sets the FF once again to the $Q = 1$ state (point g) because $S = 1$ and $R = 0$ when the positive edge occurs.
6. The fifth pulse also finds that $S = 1$ and $R = 0$ when it makes its positive-going transition. However, Q is already HIGH, so it remains in that state.
7. The $S = R = 1$ condition should not be used because it results in an ambiguous condition.

Predict the Output

- Assuming Q=0 initially, Predict the output Waveform For a Gated SR Latch.

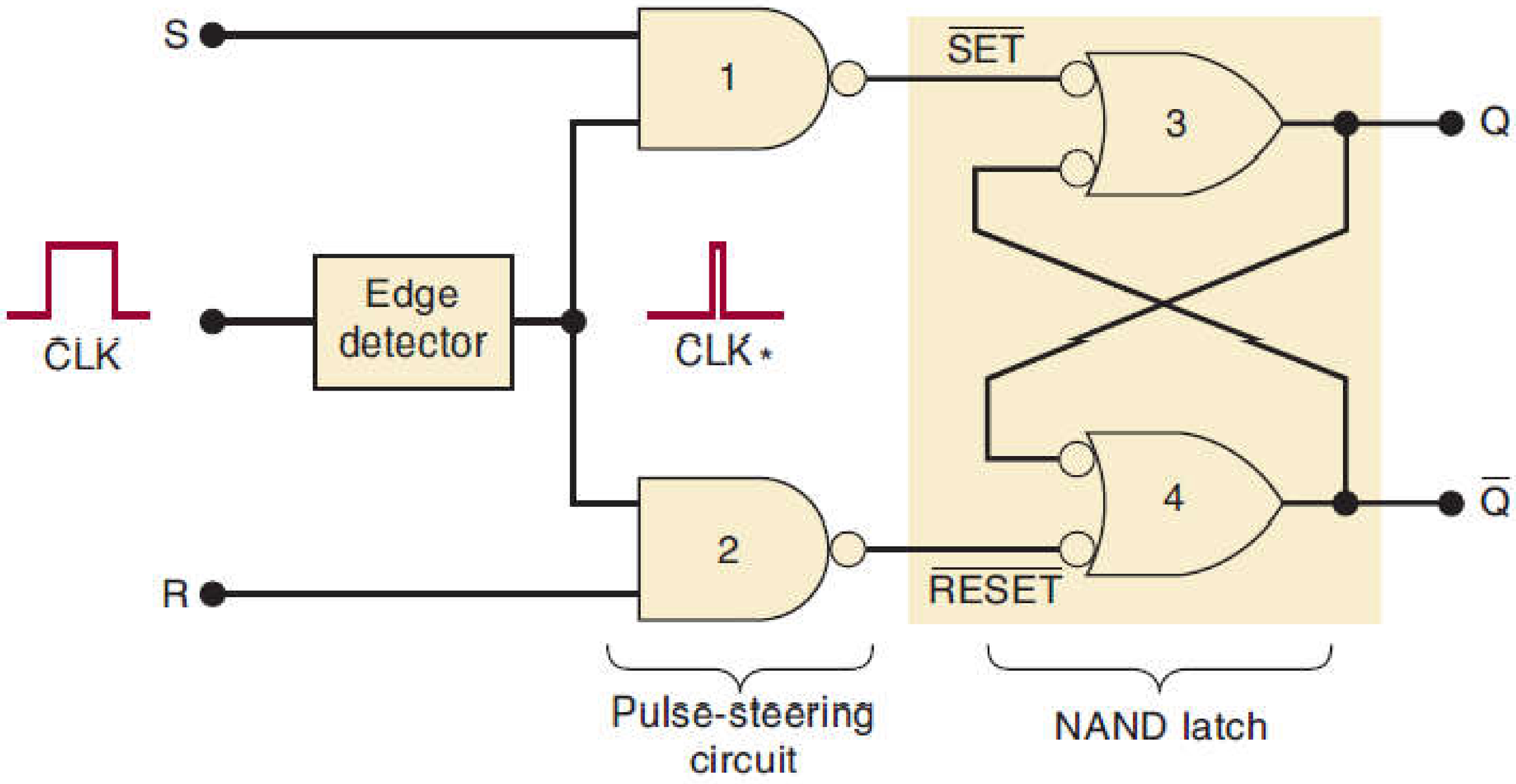


Negative Edge Triggered SR FF

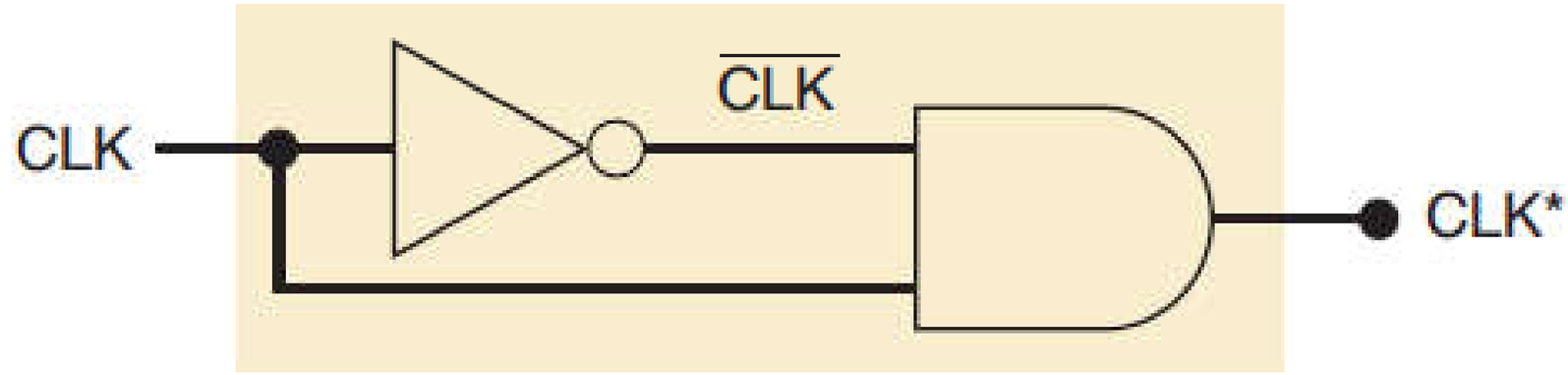


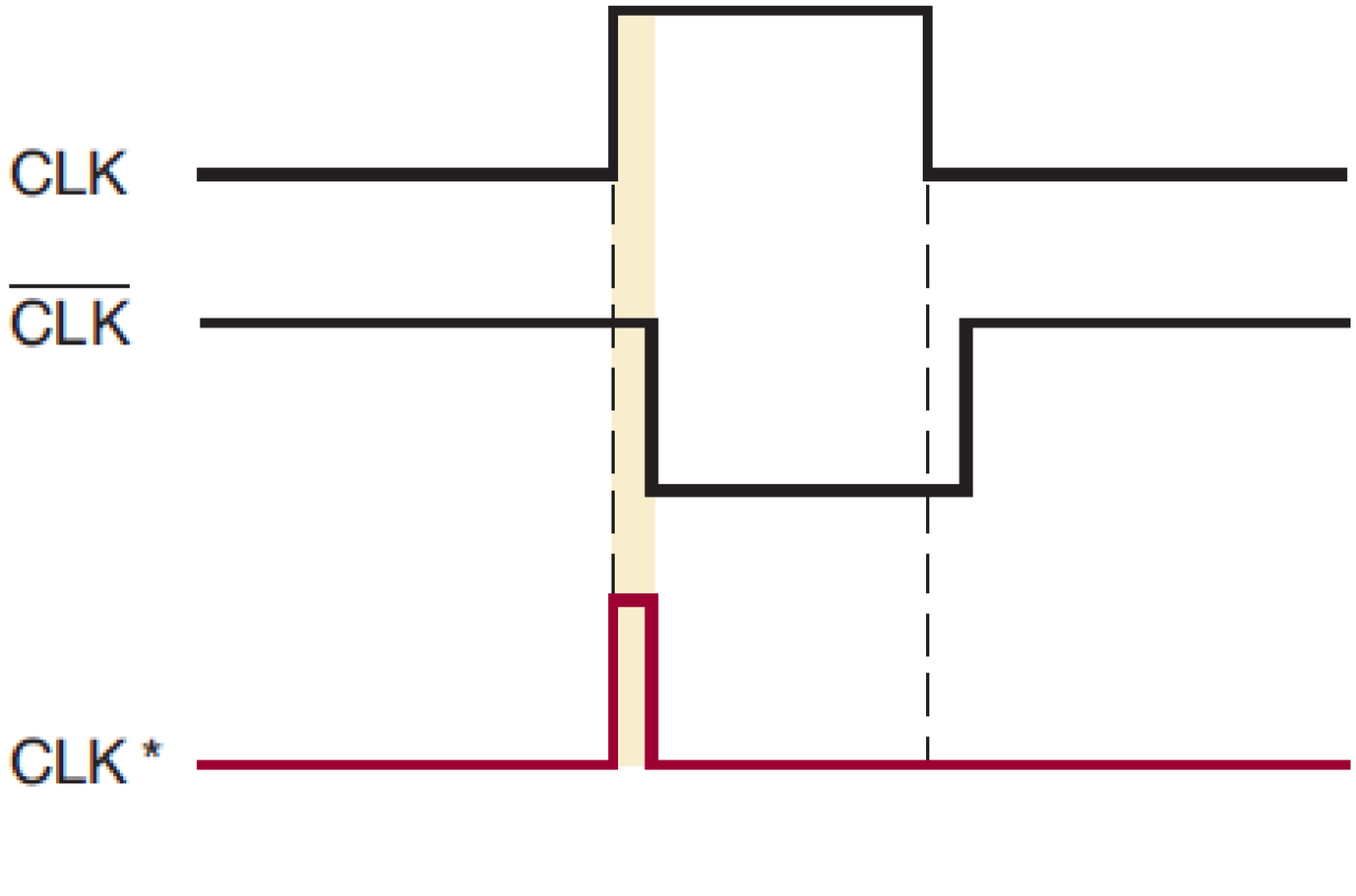
Inputs			Output
S	R	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	Ambiguous

Internal Circuit of Clocked SR-FF

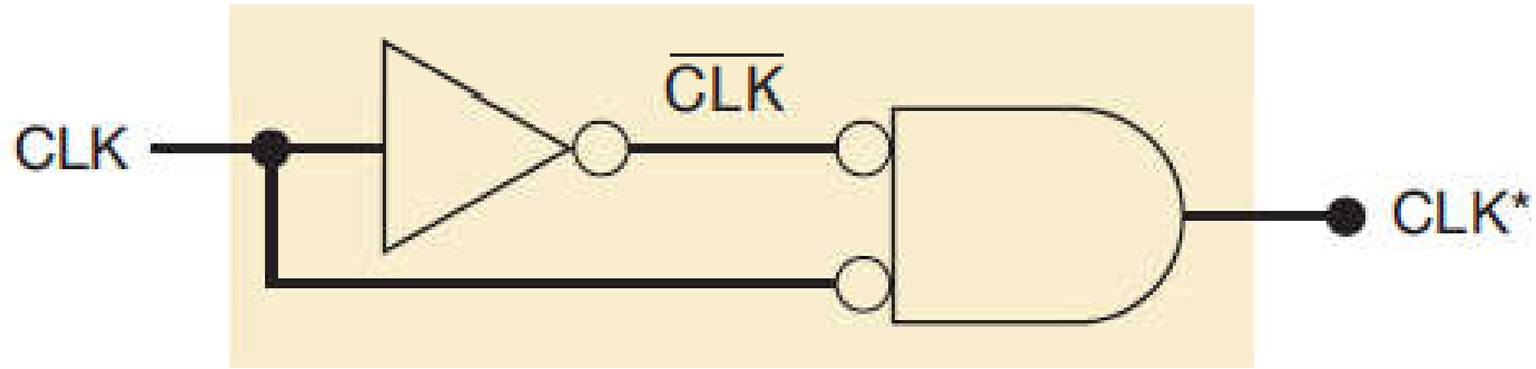


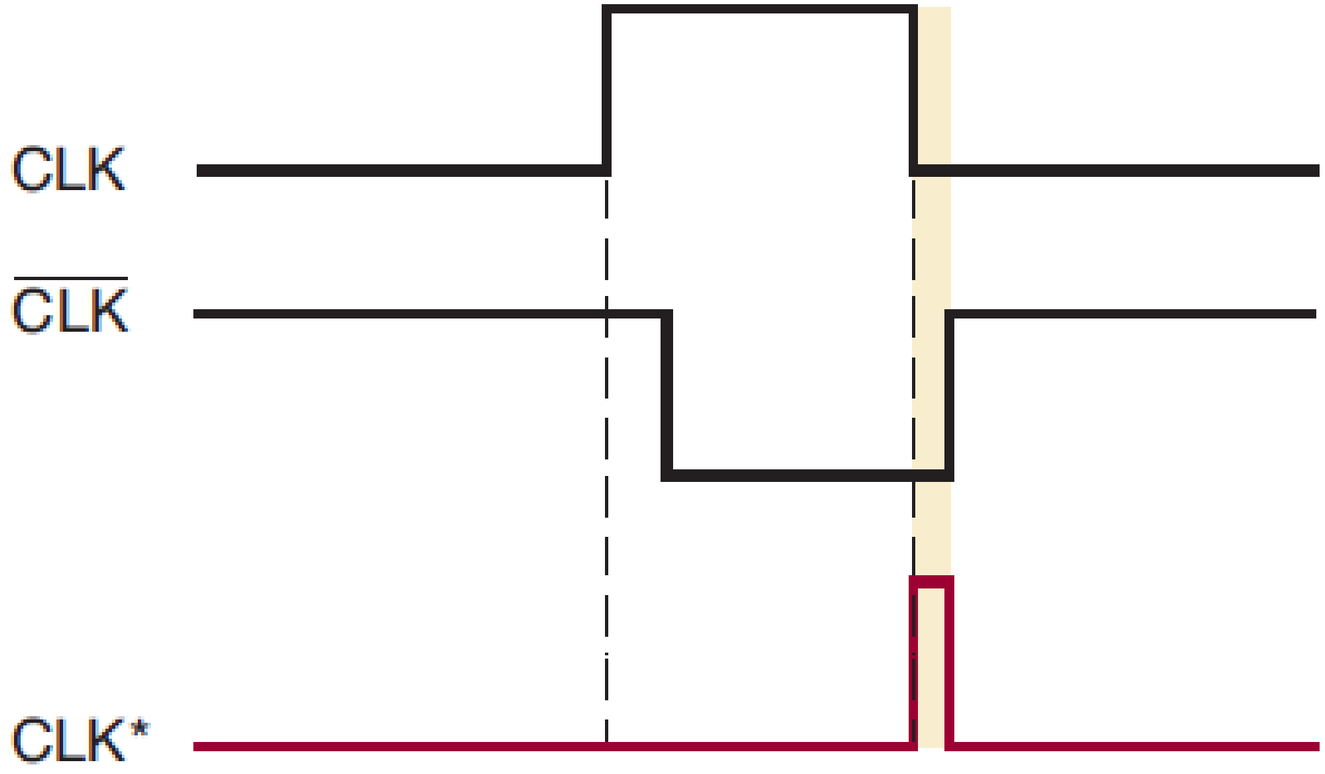
Generation of PET



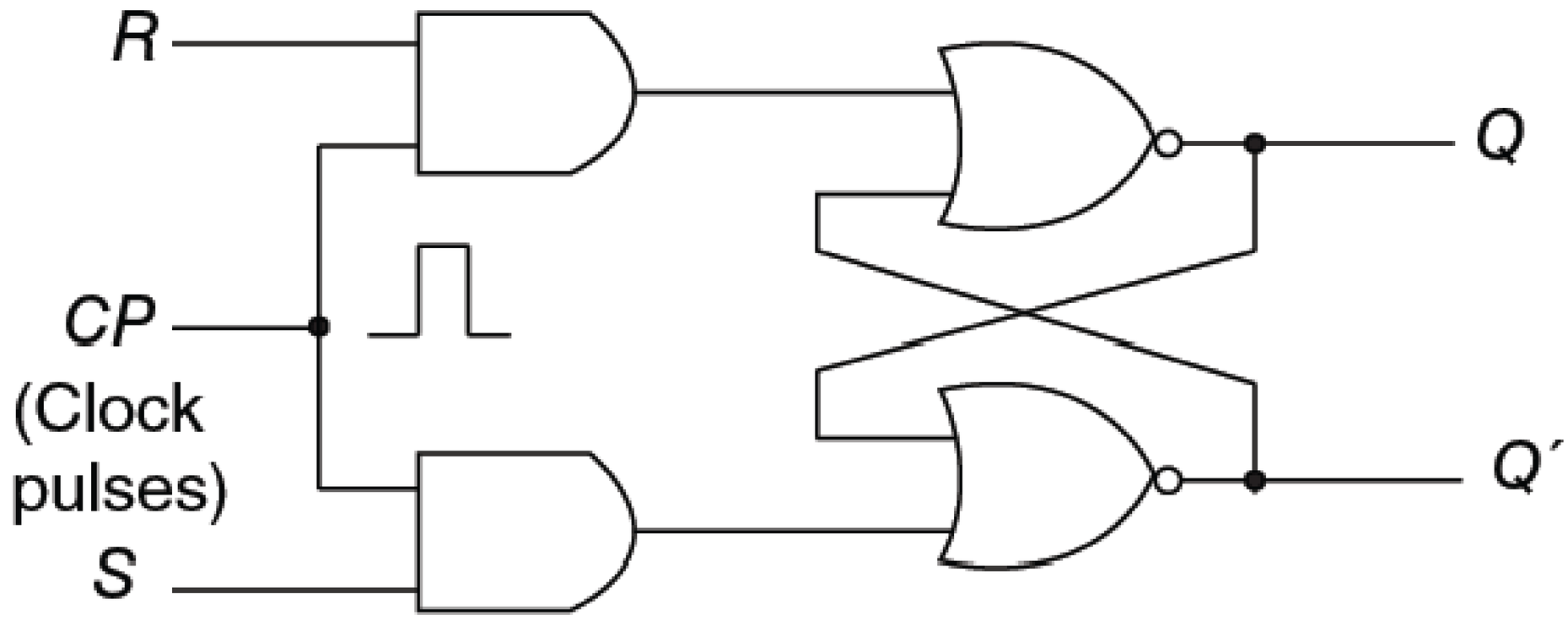


Generation of NET

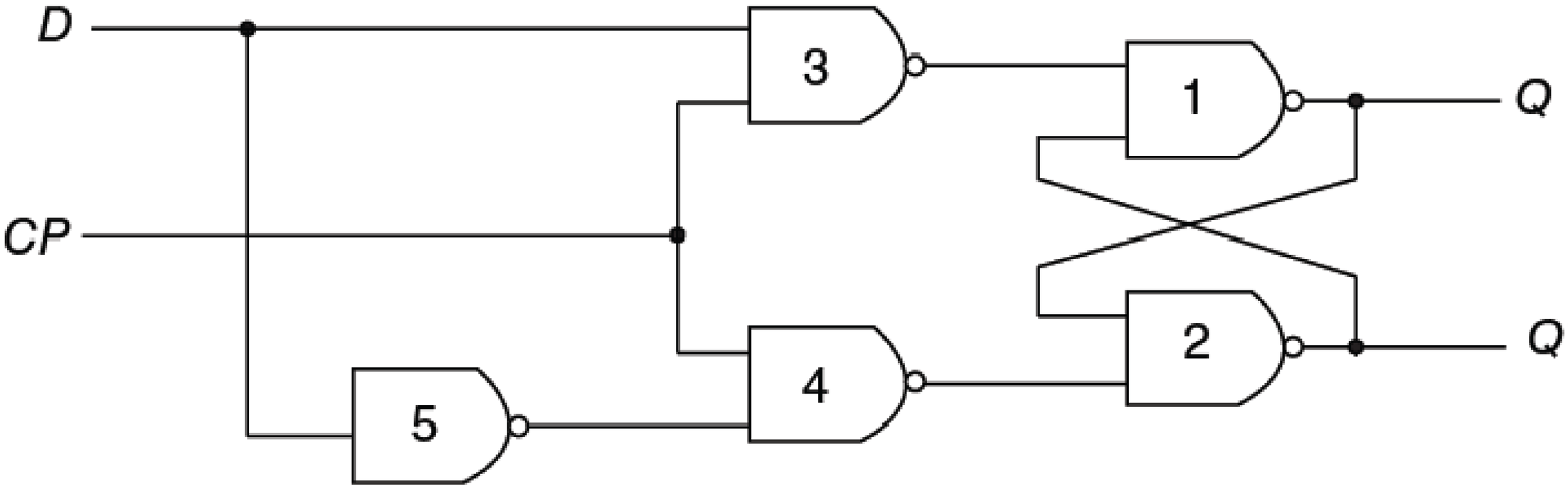


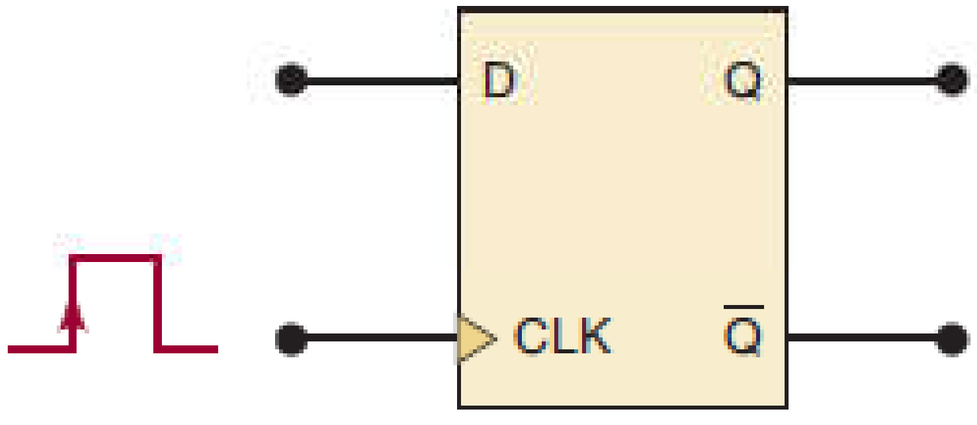


Clkd RS – FF, Another Ckt



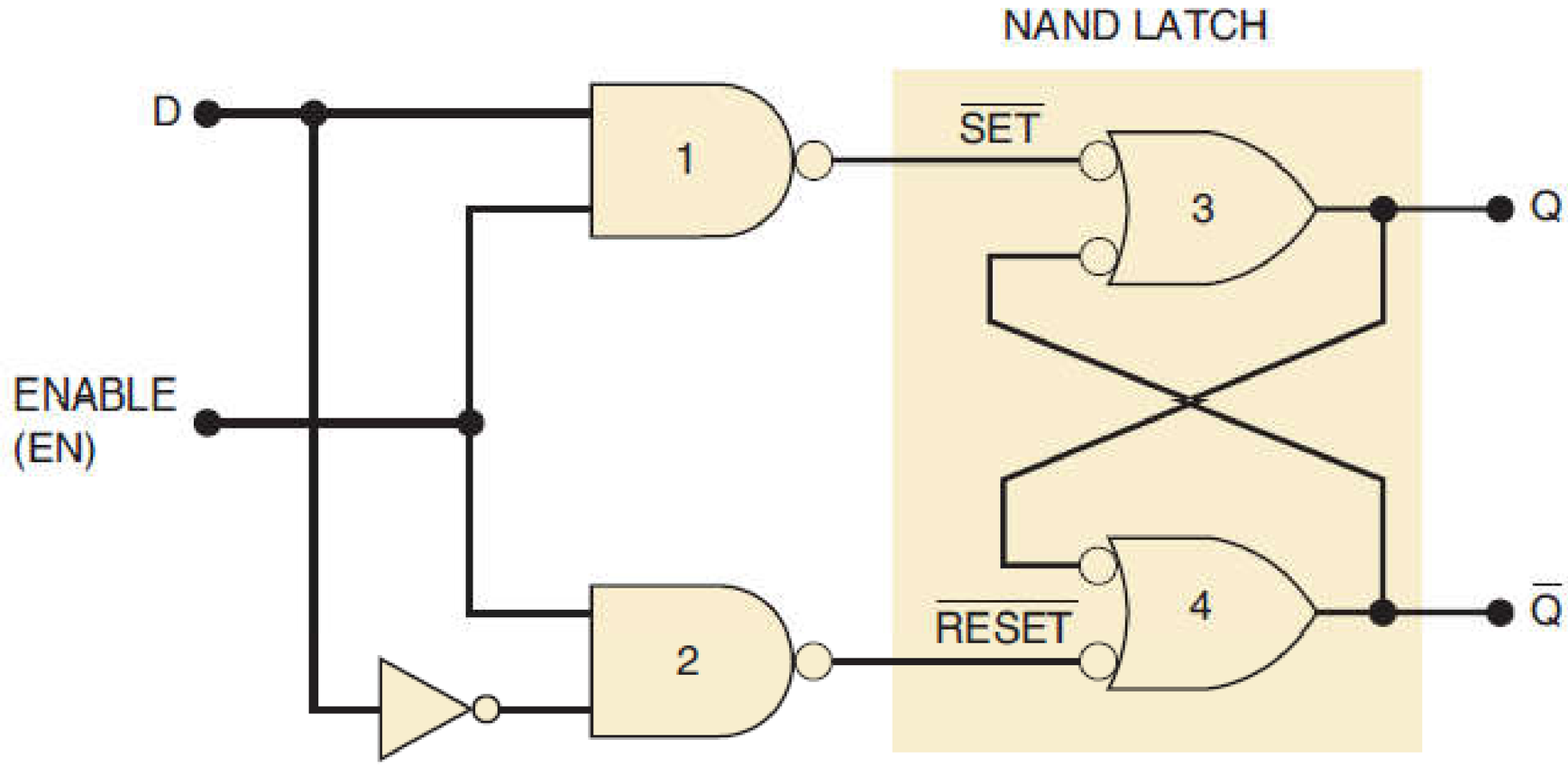
D - FF





D	CLK	Q
0	↑	0
1	↑	1

Another CKT

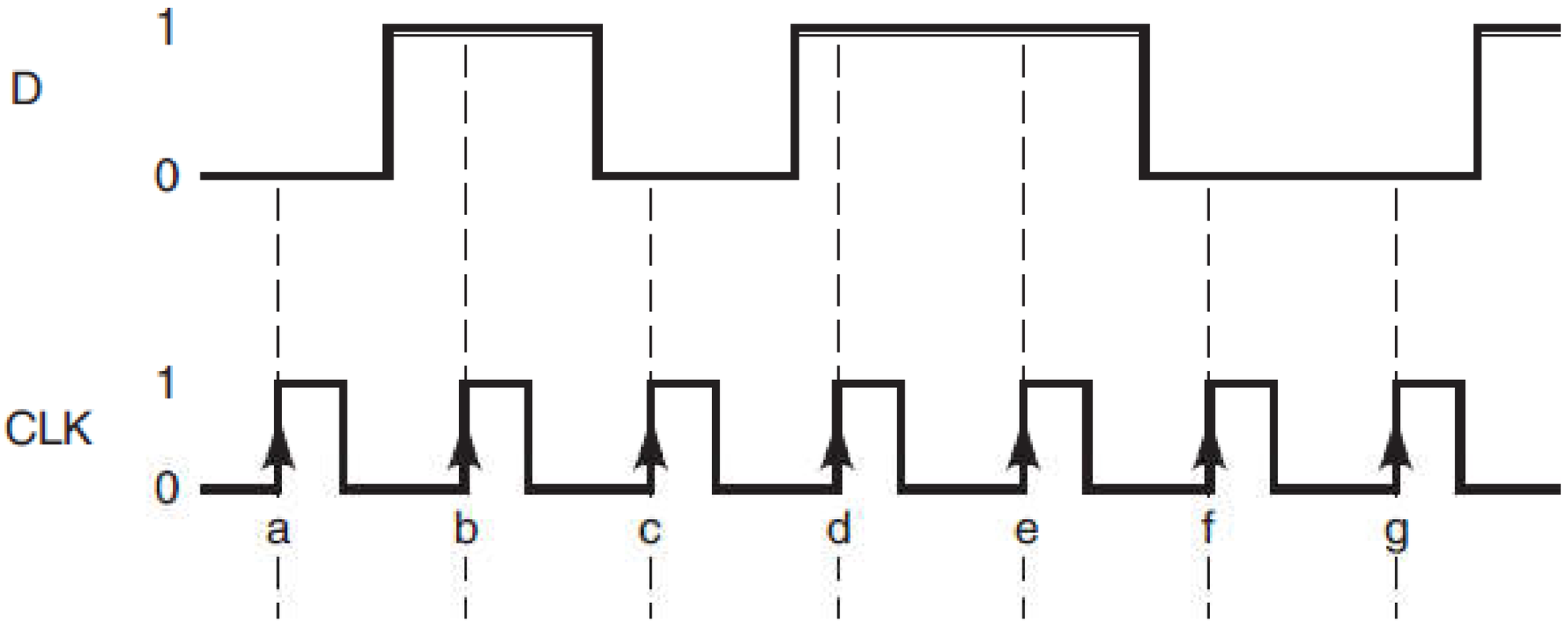


Inputs		Output
EN	D	Q
0	X	Q_0 (no change)
1	0	0
1	1	1

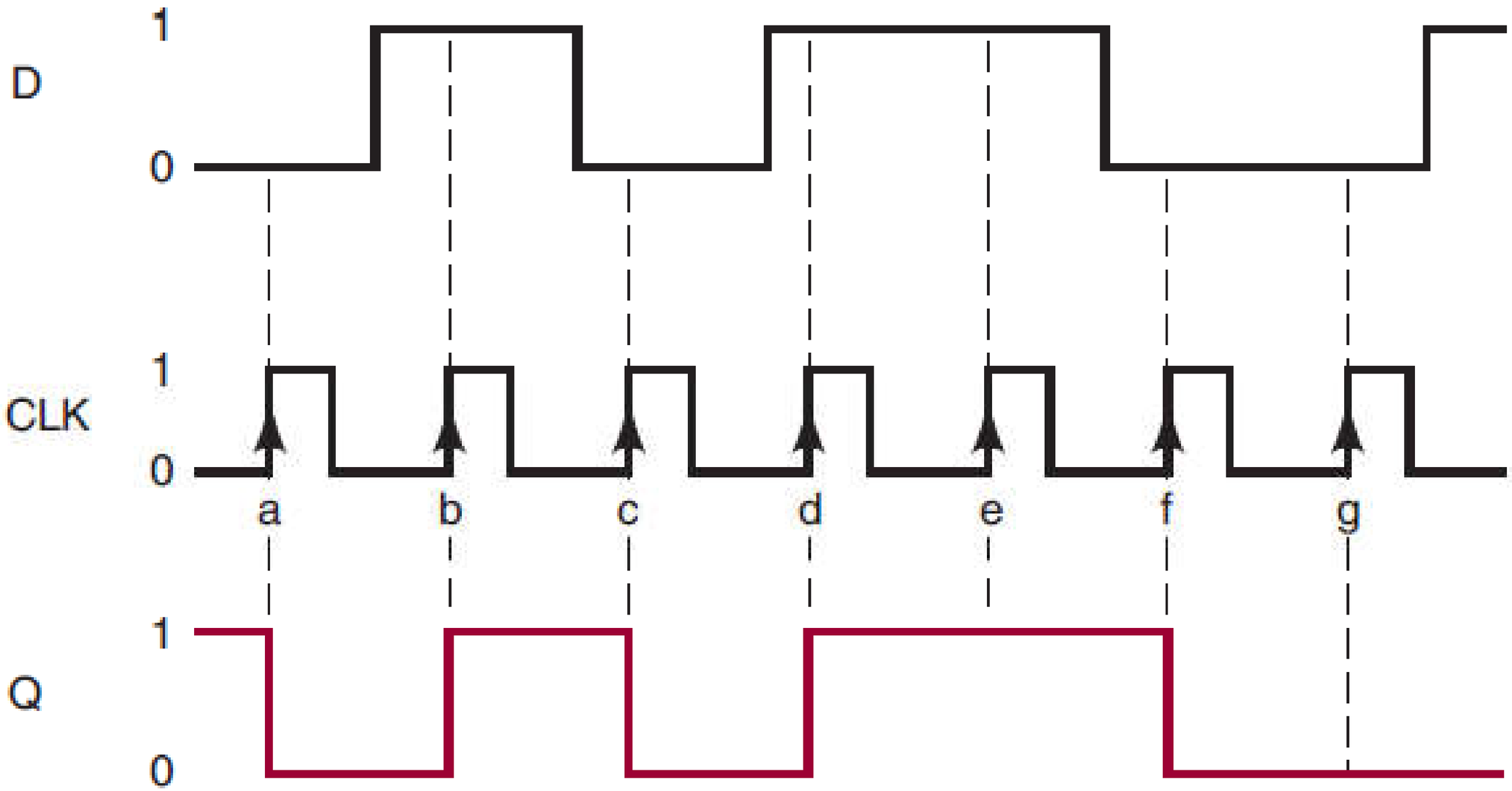
"X" indicates "don't care."
Q_0 is state Q just
prior to EN going LOW.

Predict the Output

Assume the Q is initially High

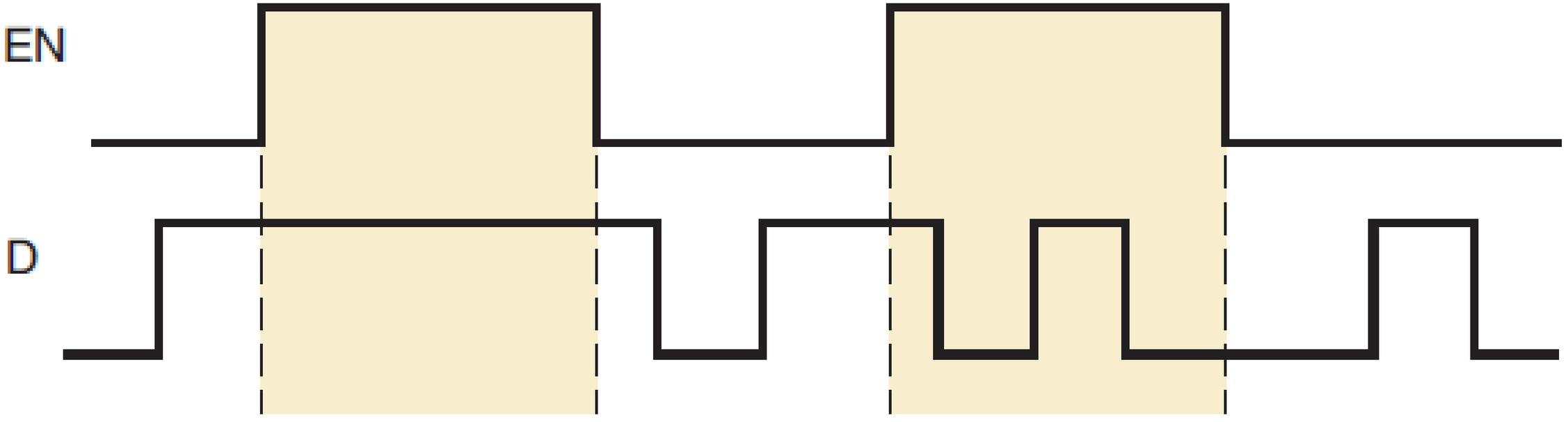


Solution

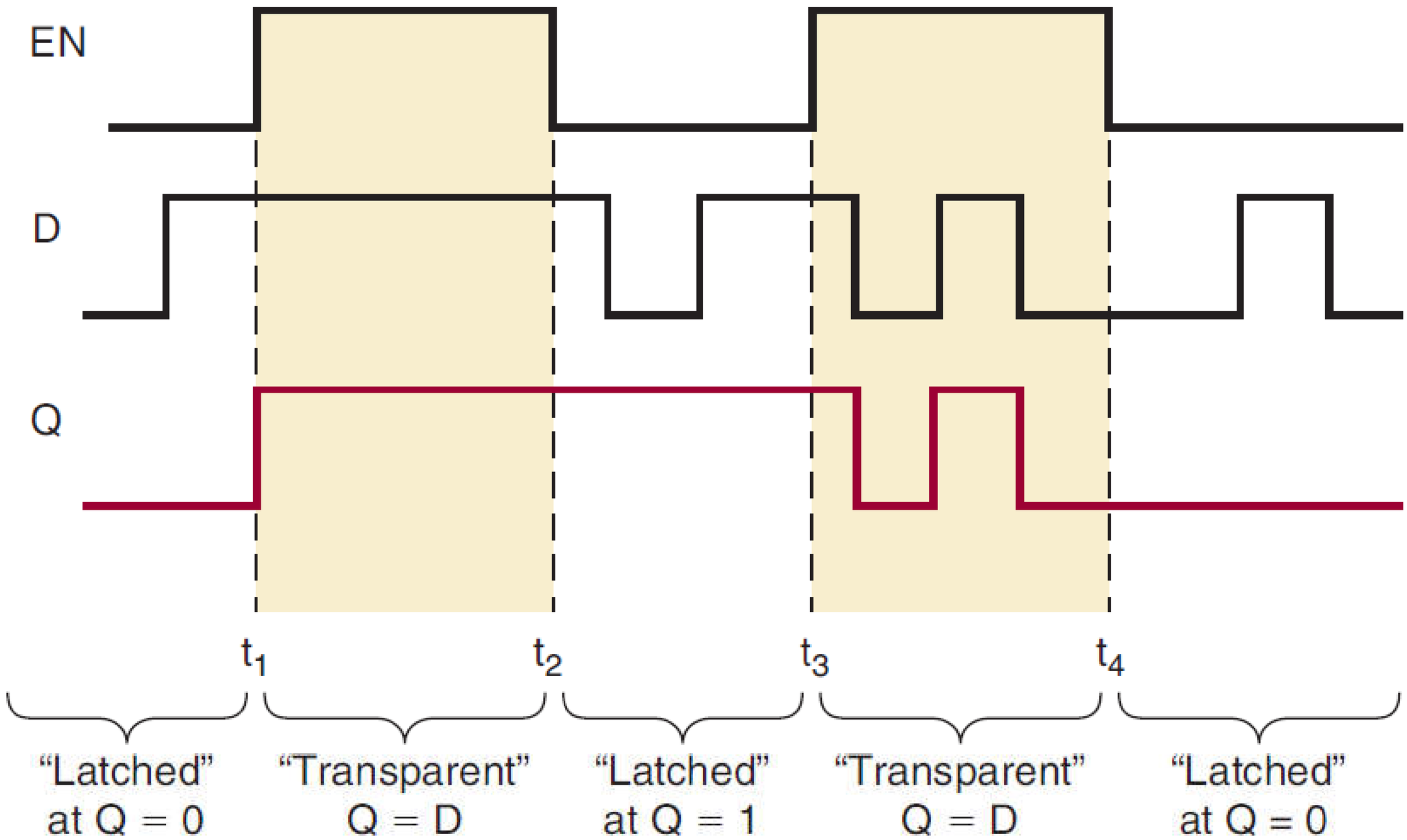


Question

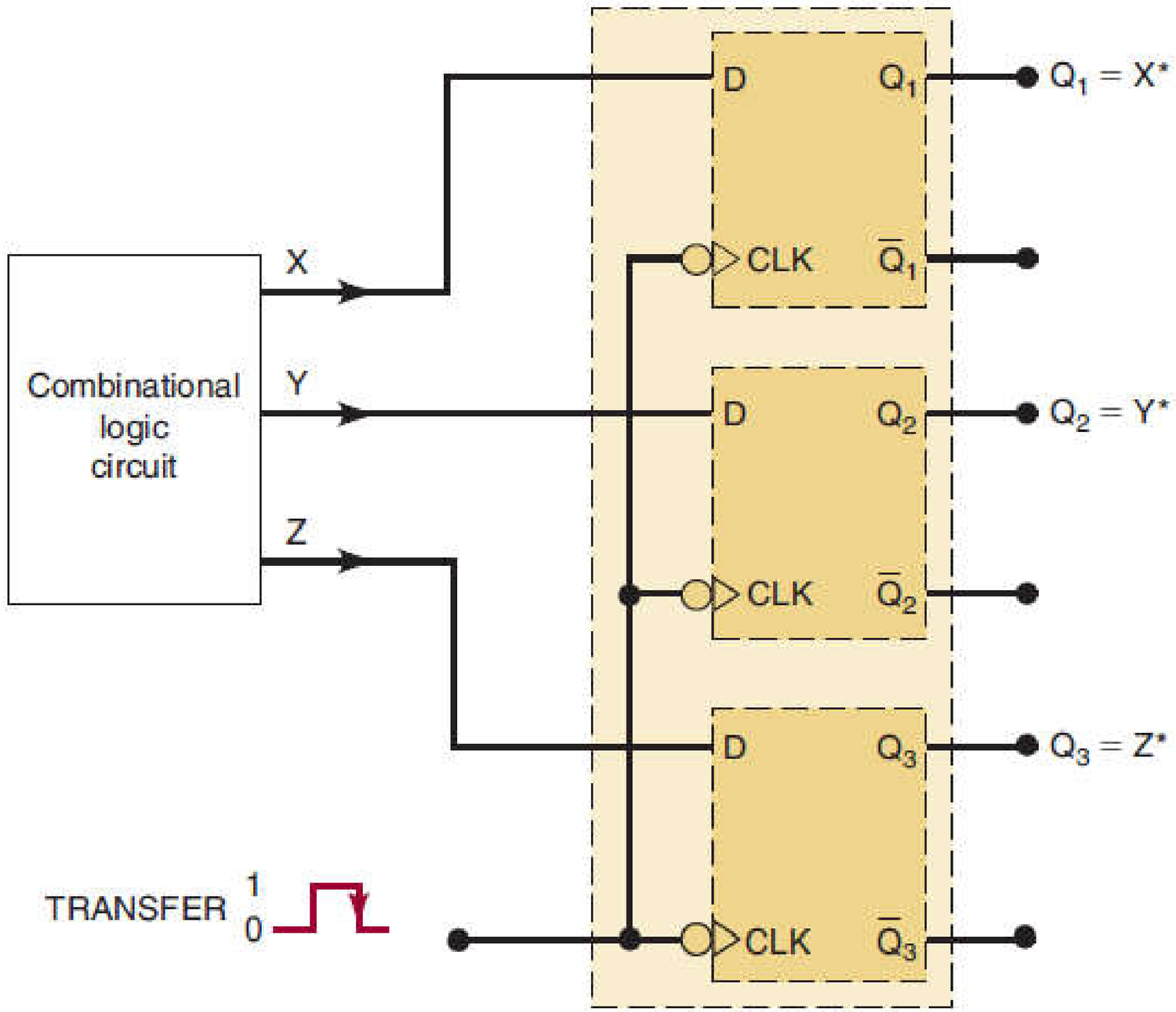
Assume, Q=0 Initially



Solution

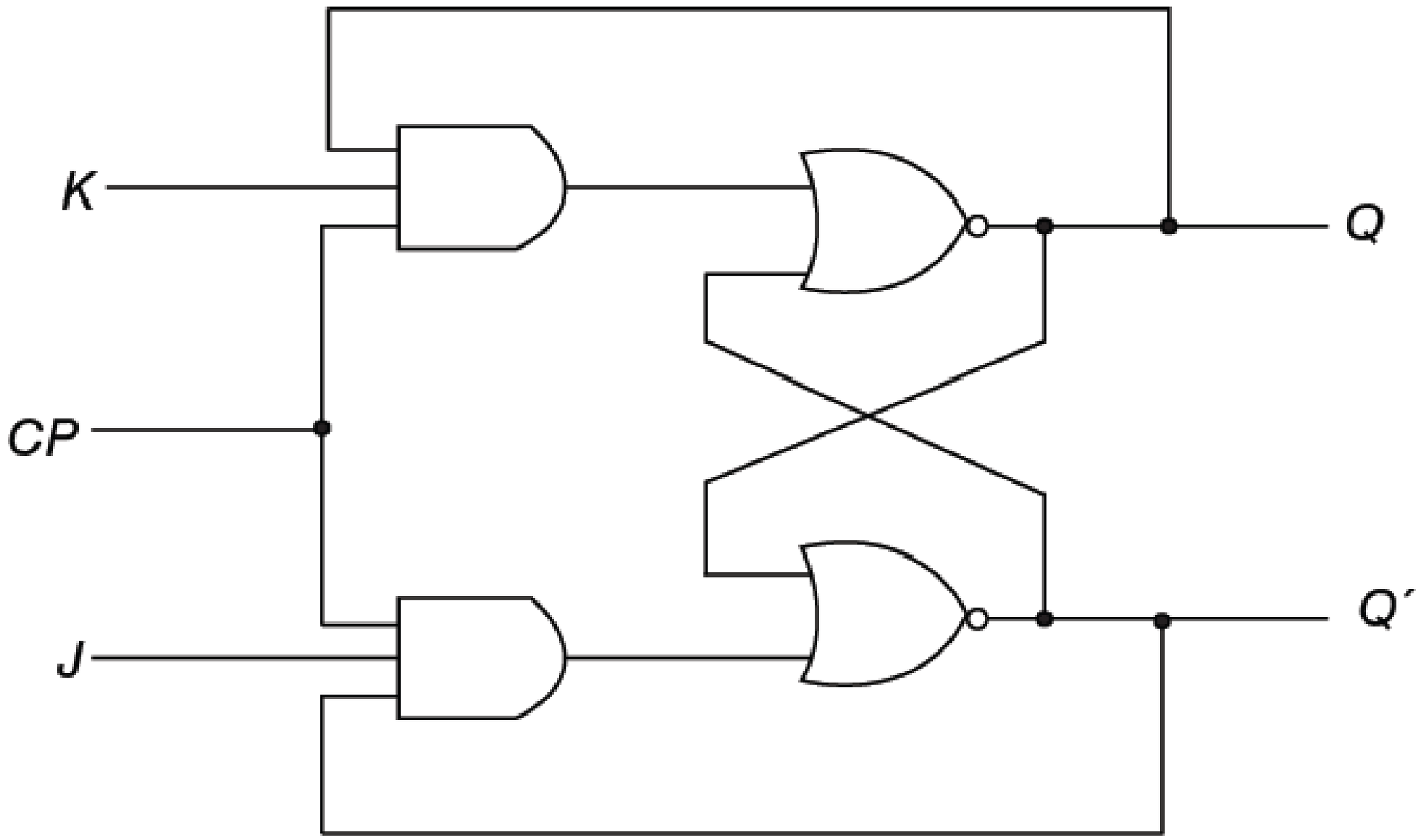

EN
D
Q
t1
t2
t3
t4
"Latched"
at Q = 0
"Transparent"
Q = D
"Latched"
at Q = 1
"Transparent"
Q = D
"Latched"
at Q = 0

D-FF Application

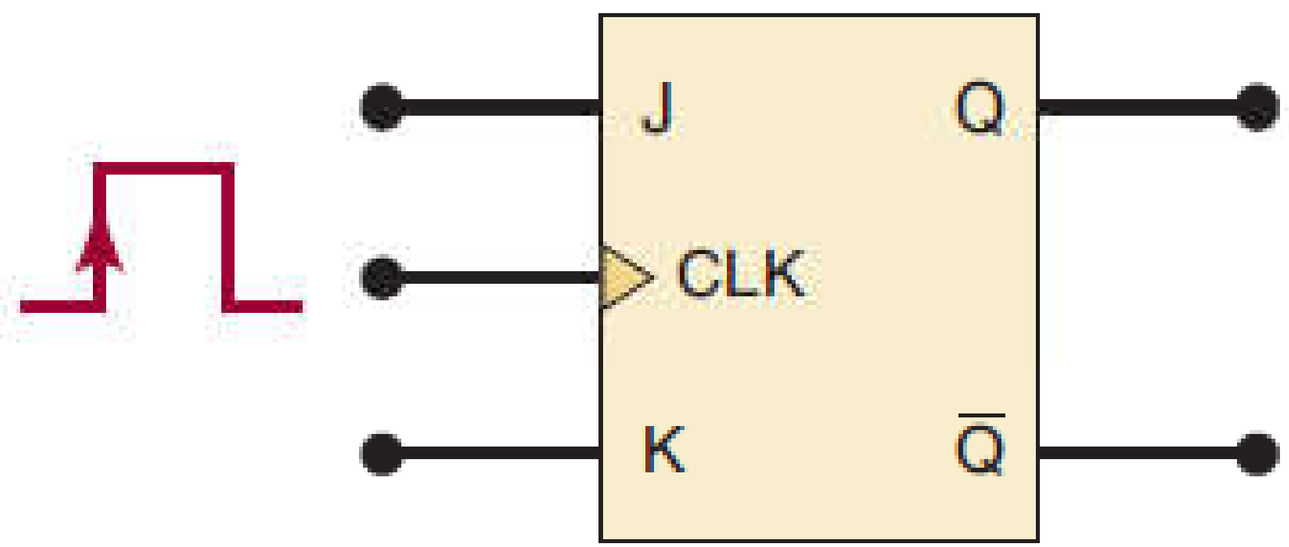


*After occurrence of NGT

JK – Flip Flop



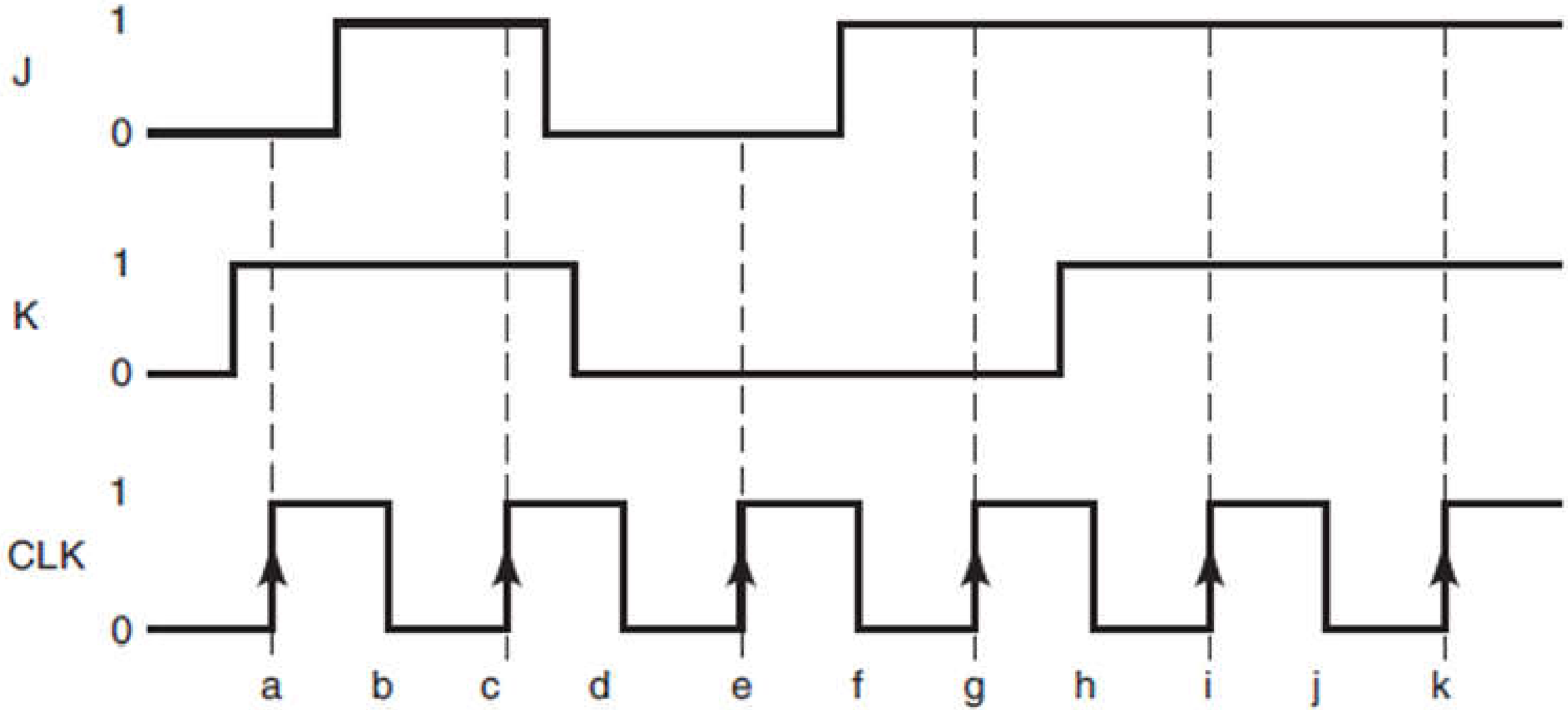
JK FF



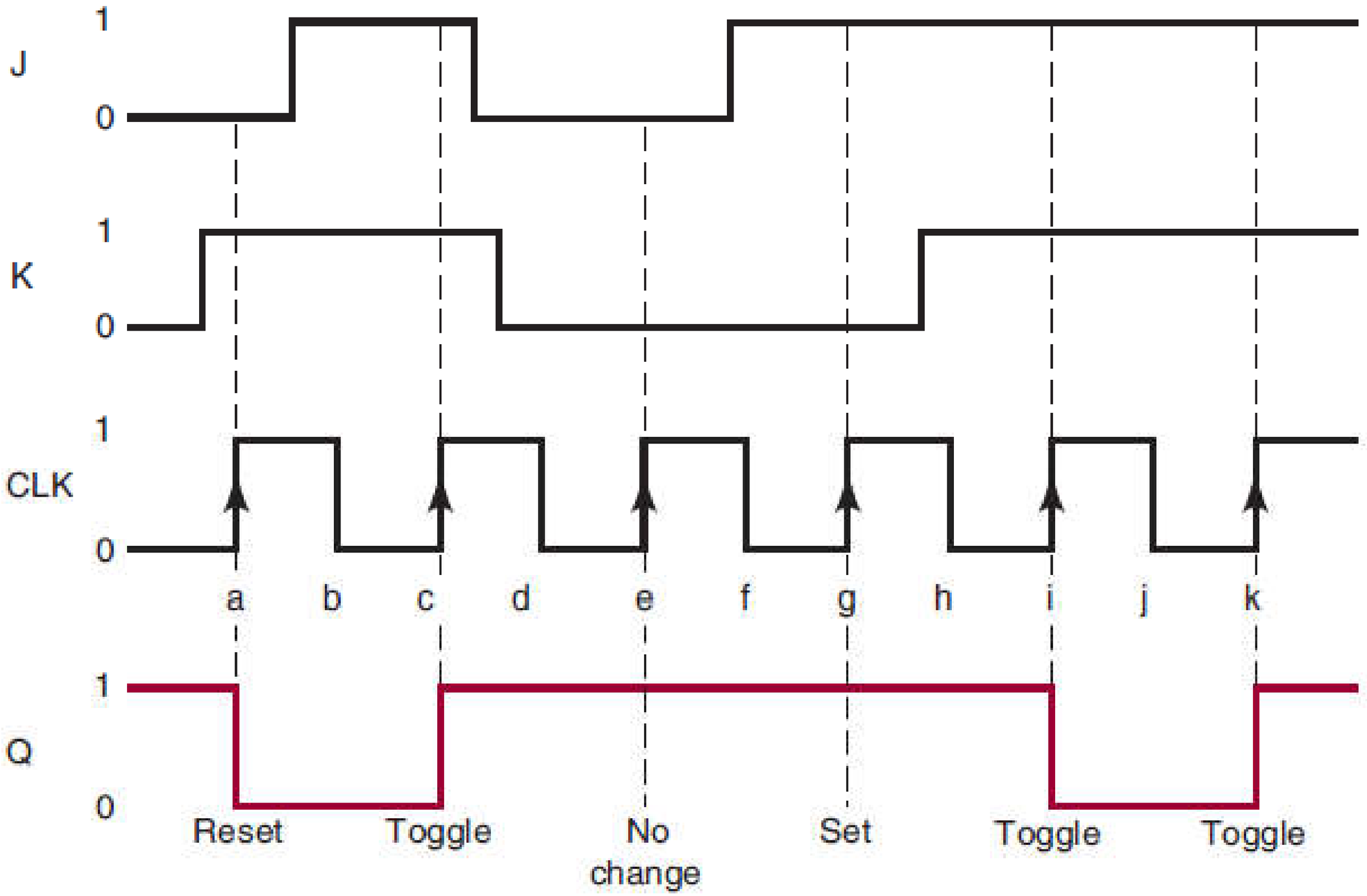
J	K	CLK		Q
0	0	↑		Q_0 (no change)
1	0	↑		1
0	1	↑		0
1	1	↑		$\overline{Q}_0$ (toggles)

Predict the Output

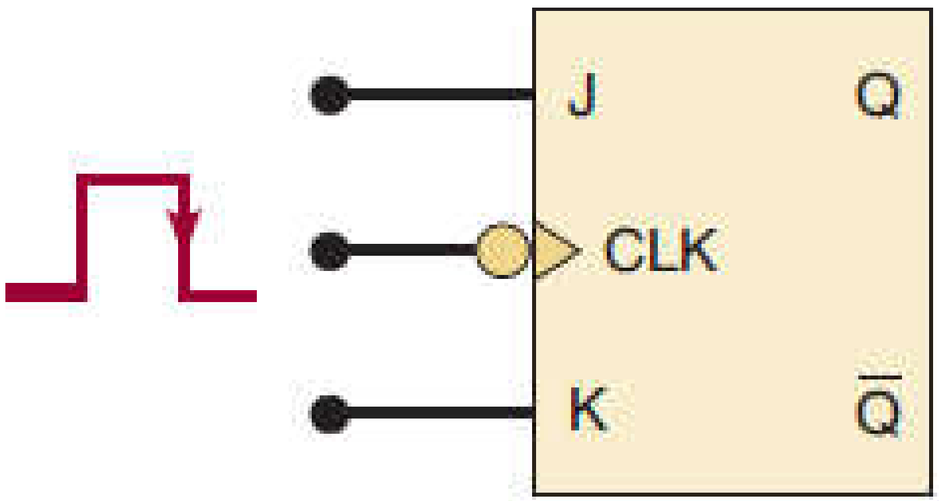
Assume Q=1 initially



Solution

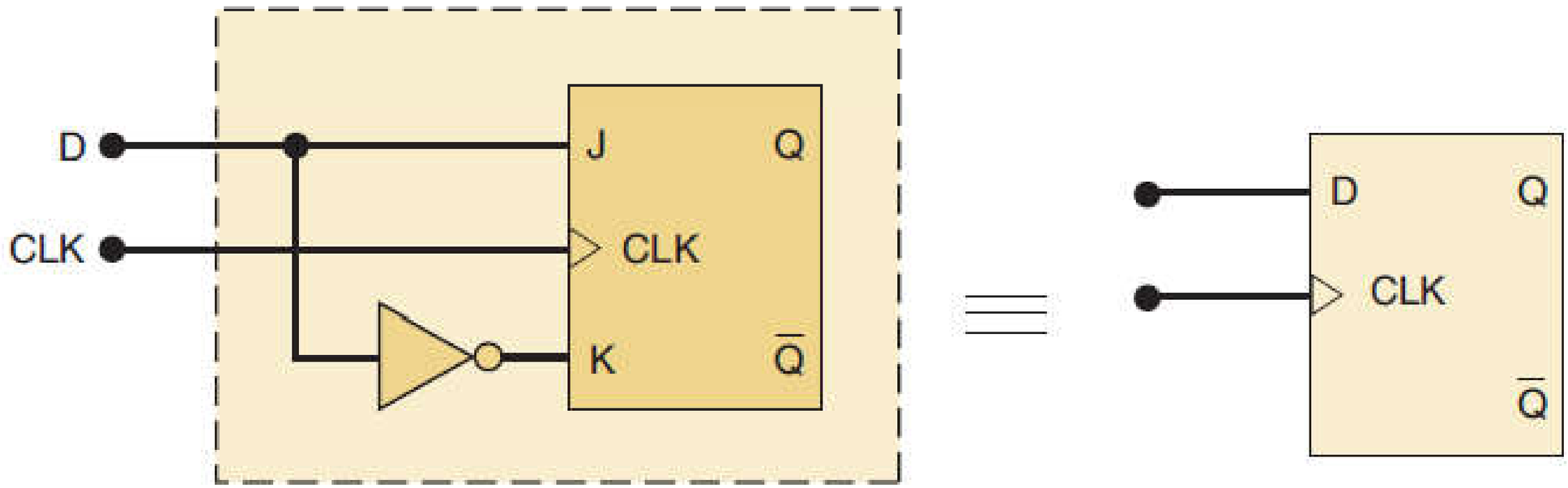

J
1
0
K
1
0
CLK
1
0
a
b
c
d
e
f
g
h
i
j
k
Q
1
0
Reset
Toggle
No change
Set
Toggle
Toggle

JK FF (Negative Edge Triggered)

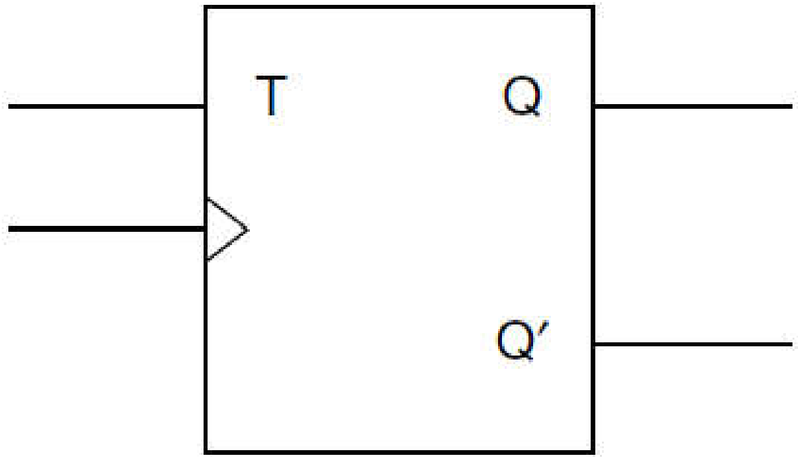


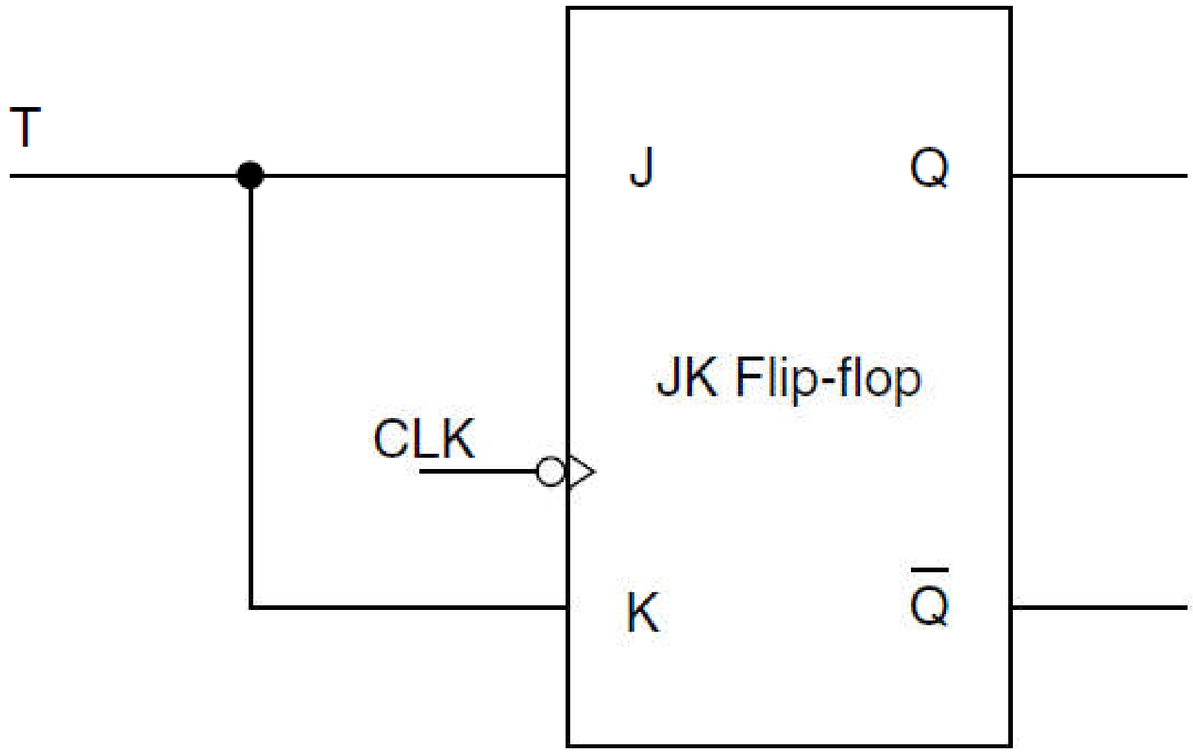
J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	$\overline{Q_0}$ (toggles)

D From JK - FF



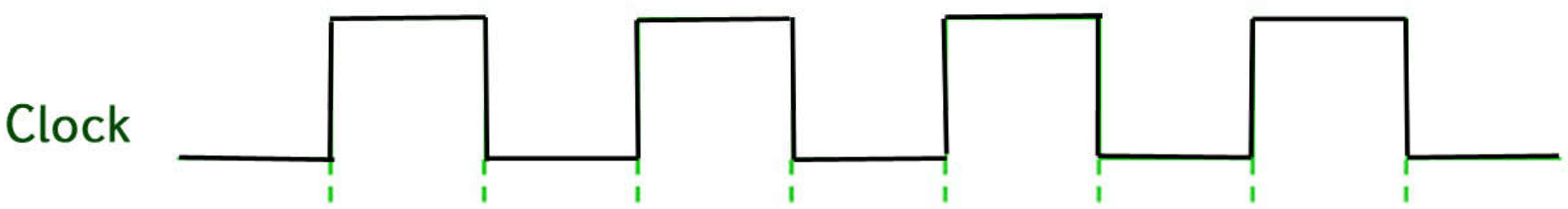
T – Flip Flop



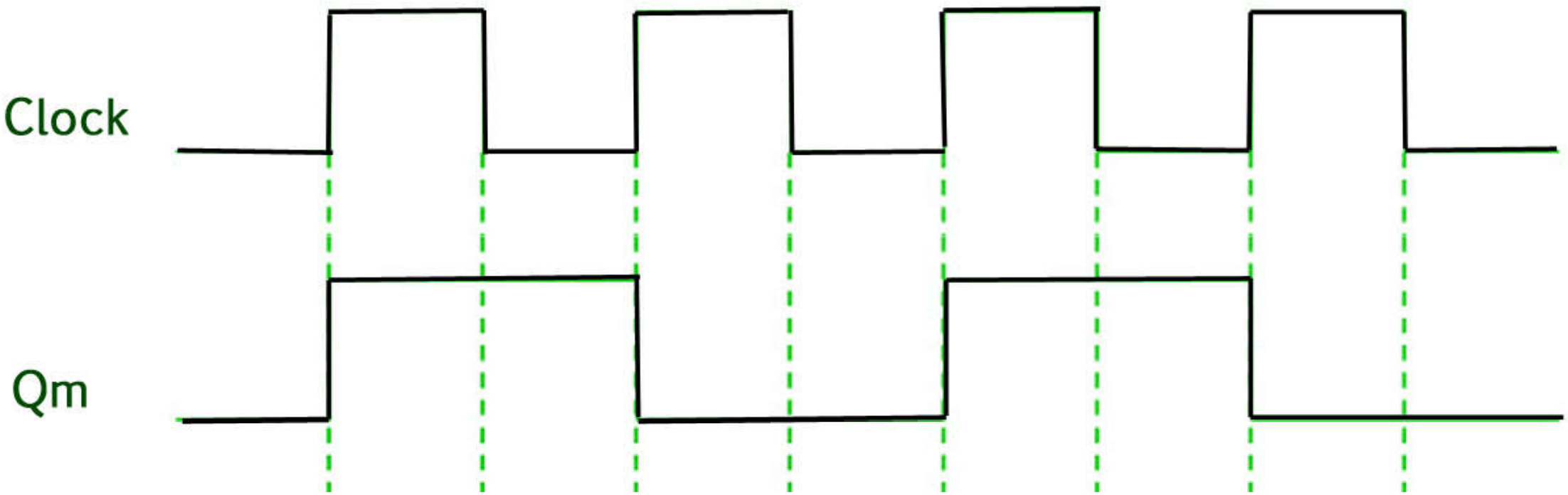


Concept of Frequency Division

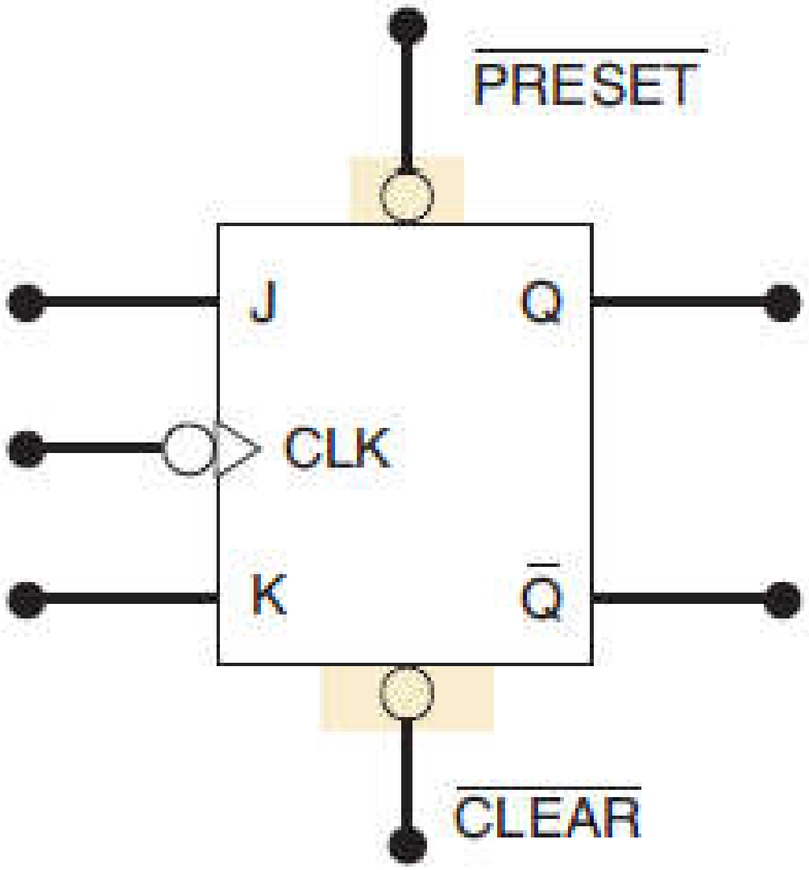
- Flip Flops can be used to divide input frequencies
- The frequency to be divided is applied as clock



Concept of Frequency Division

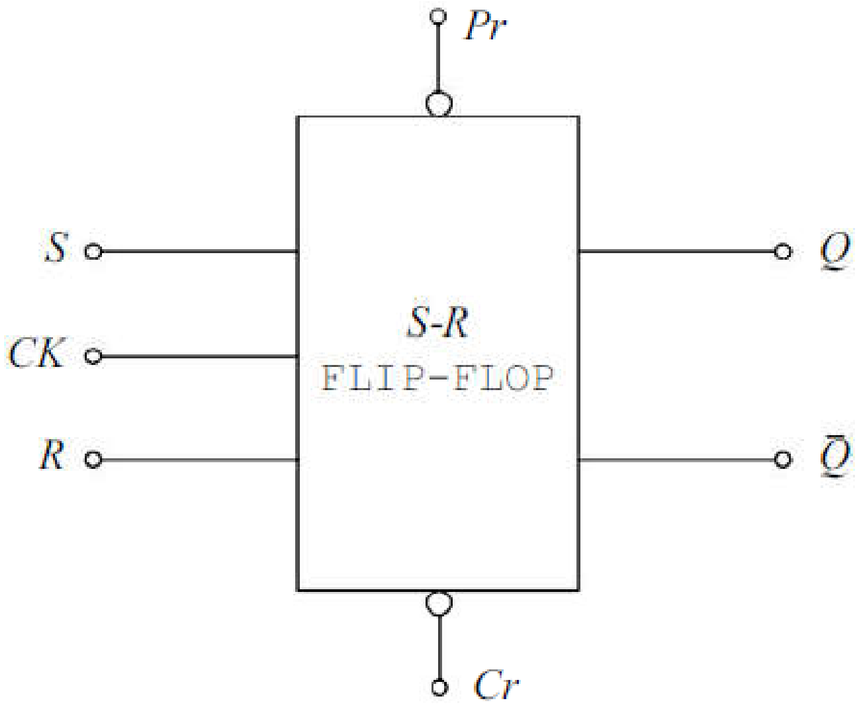


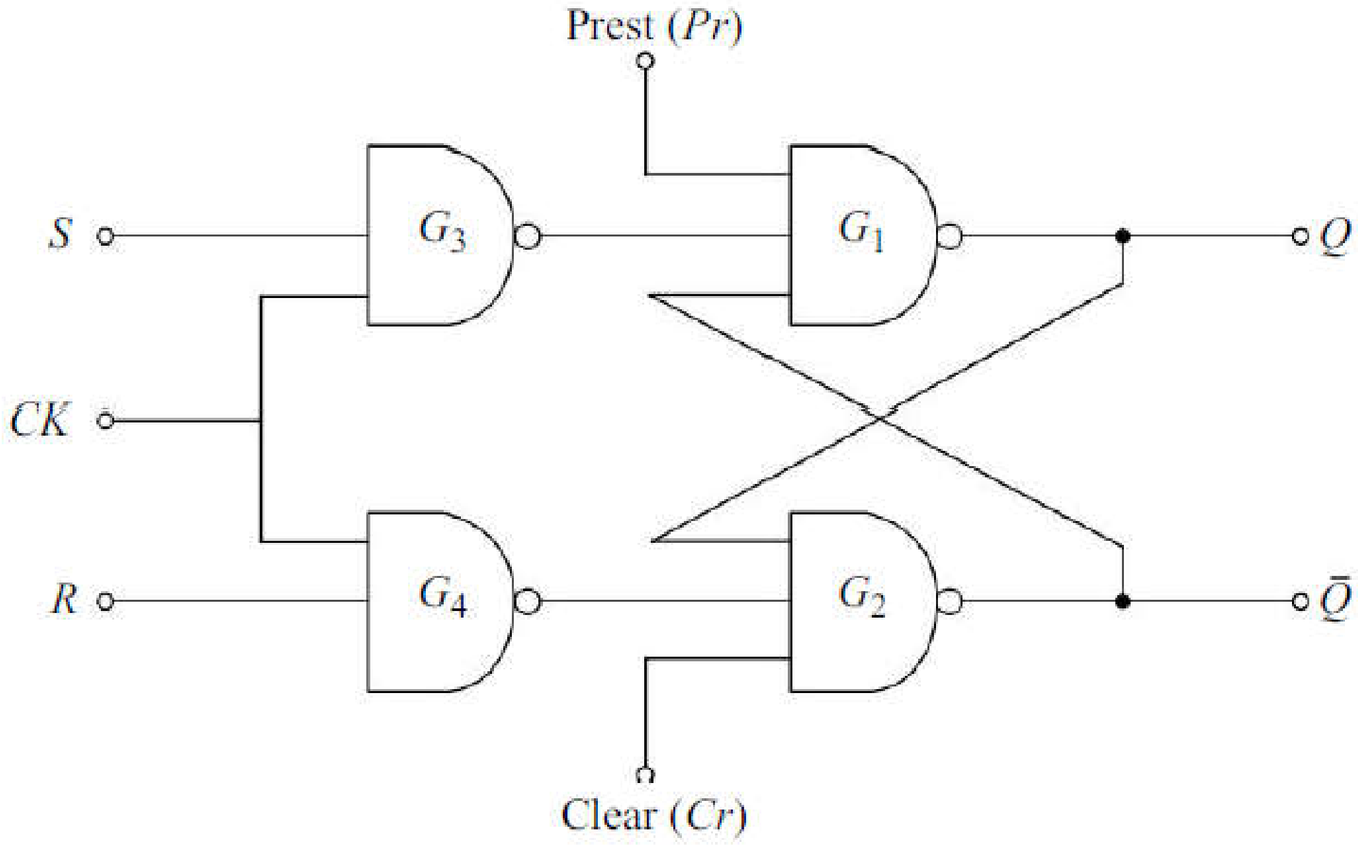
Asynchronous Inputs



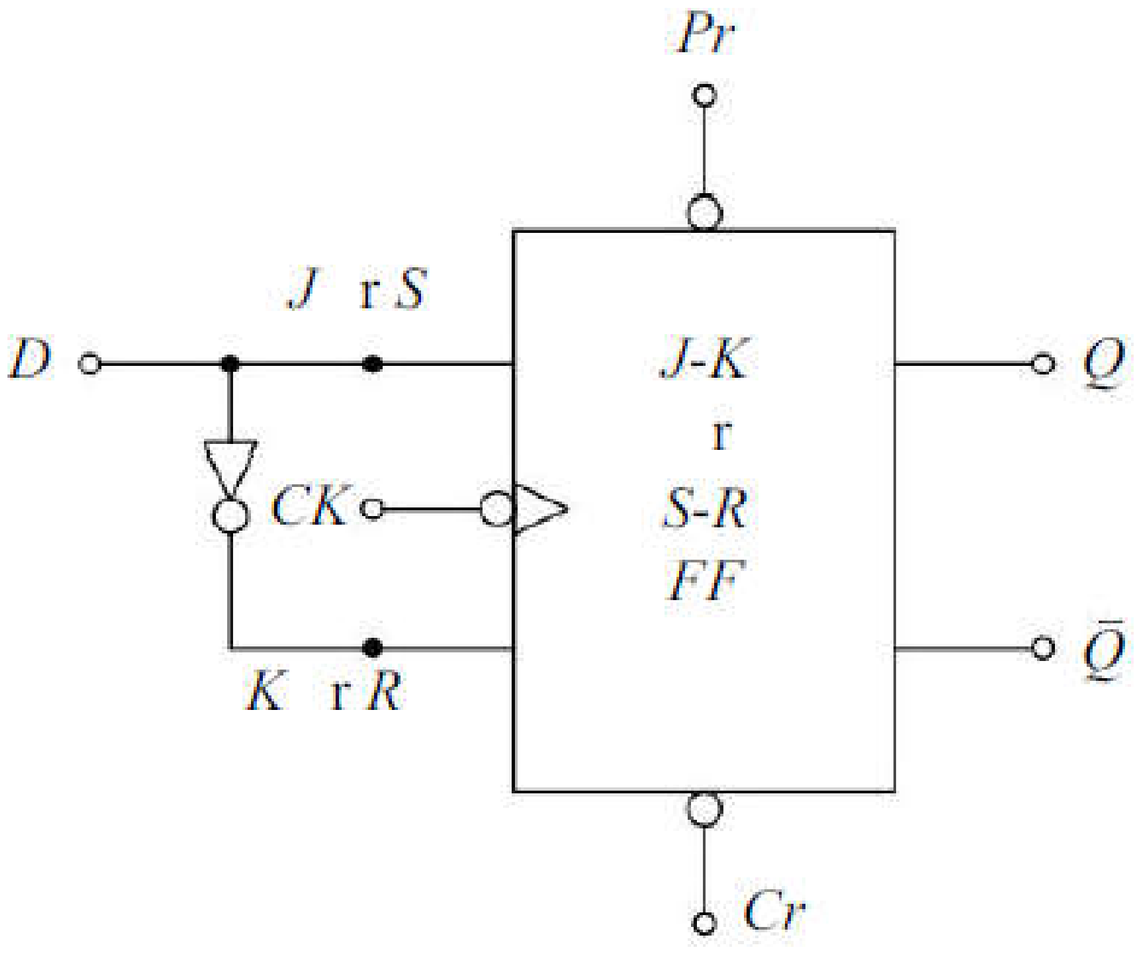
J	K	Clk	$\overline{PRE}$	$\overline{CLR}$	Q
0	0	↓	1	1	Q (no change)
0	1	↓	1	1	0 (Synch reset)
1	0	↓	1	1	1 (Synch set)
1	1	↓	1	1	$\overline{Q}$ (Synch toggle)
x	x	x	1	1	Q (no change)
x	x	x	1	0	0 (asynch clear)
x	x	x	0	1	1 (asynch preset)
x	x	x	0	0	(Invalid)

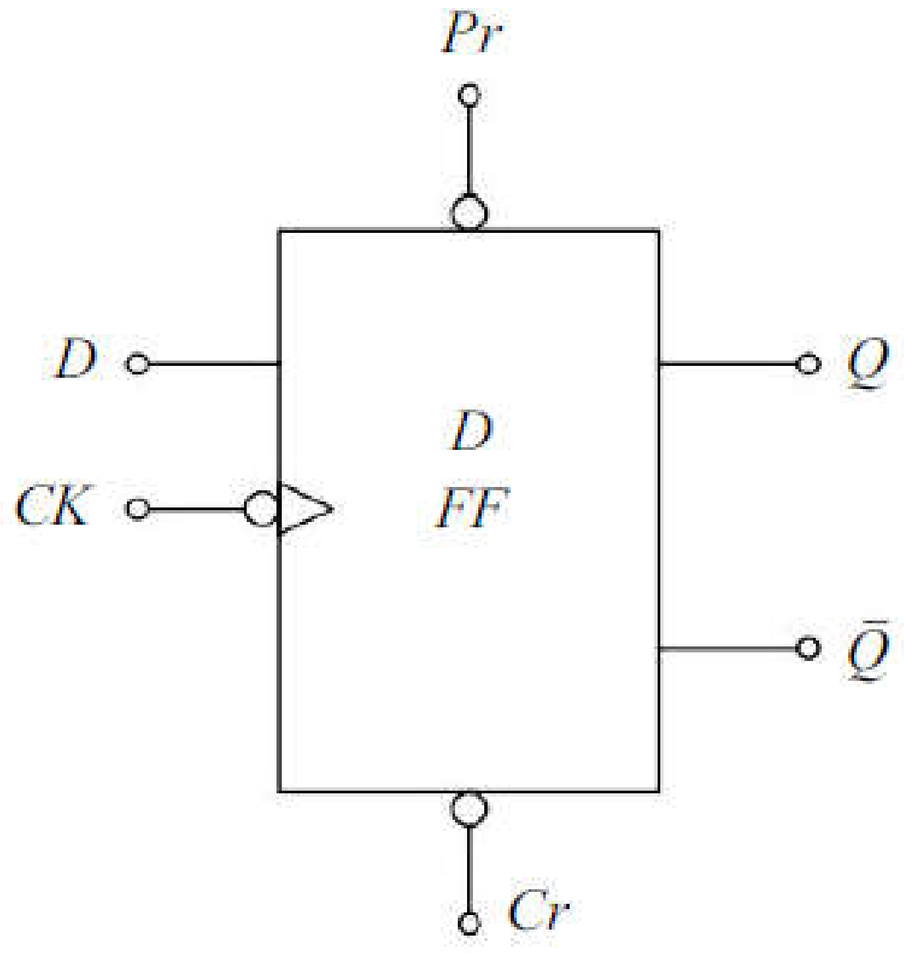
SR – Flip Flop


Pr
S
CK
R
S-R
FLIP-FLOP
Q
$\bar{Q}$
Cr

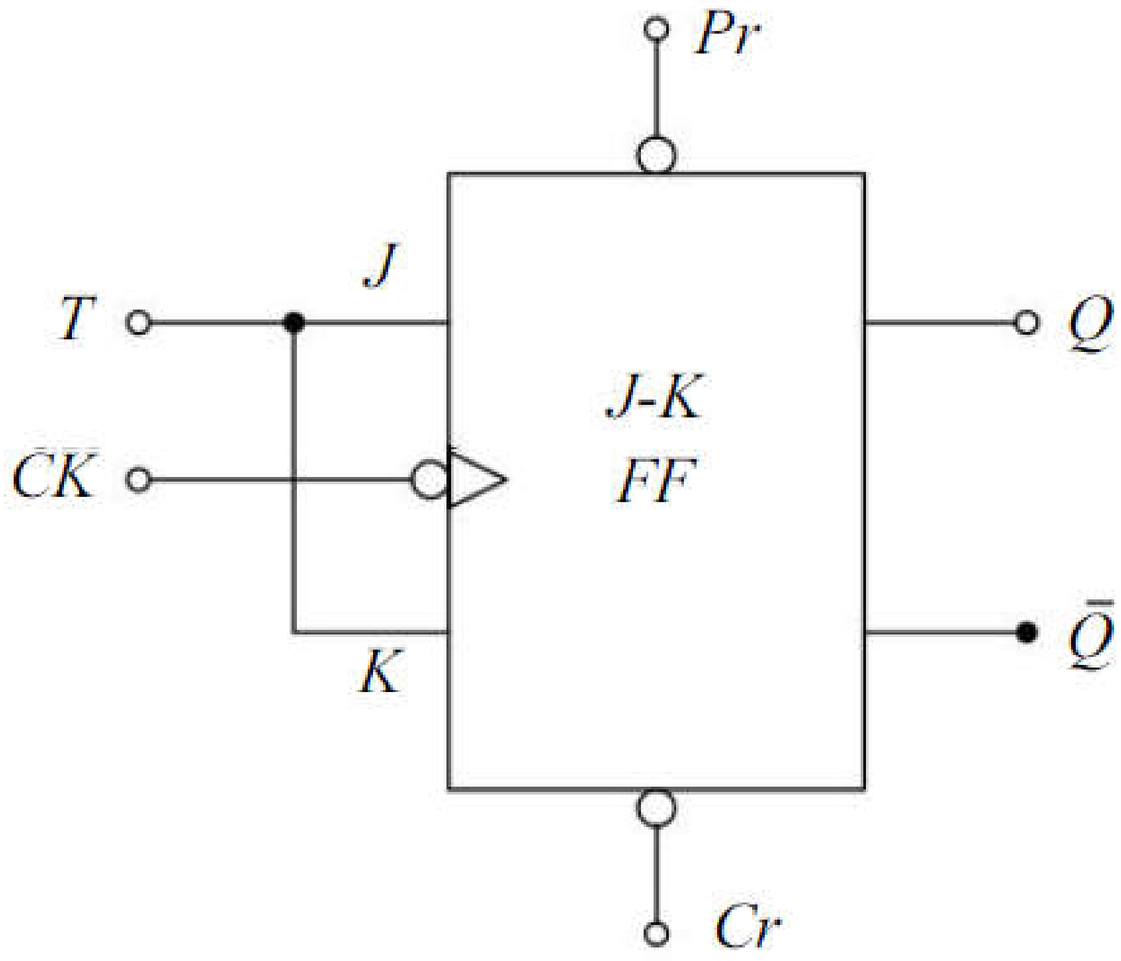

Prest (Pr)
S
CK
R
G_3
G_4
G_1
G_2
Q
$\bar{Q}$
Clear (Cr)

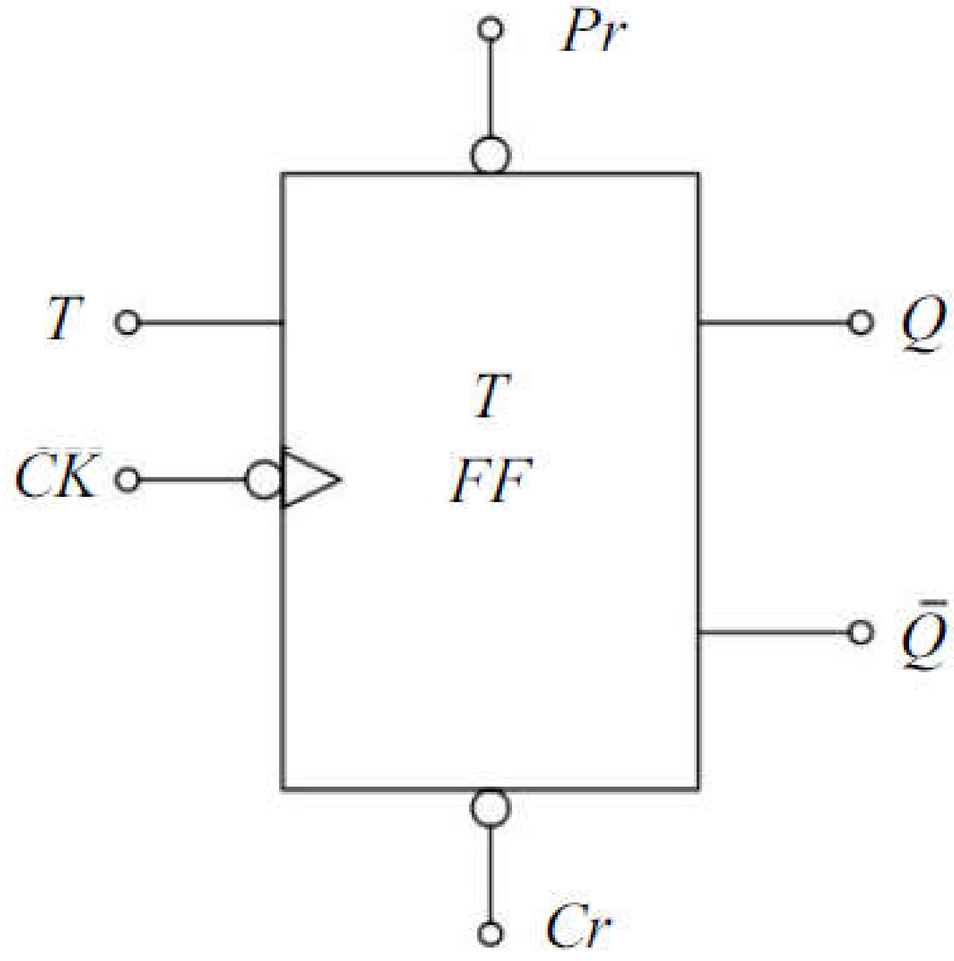
D- Flip Flop





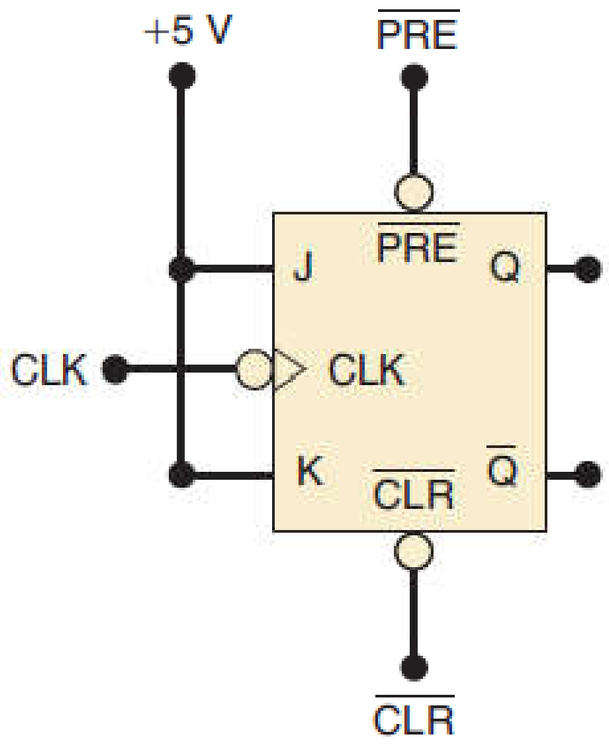
T – Flip Flop

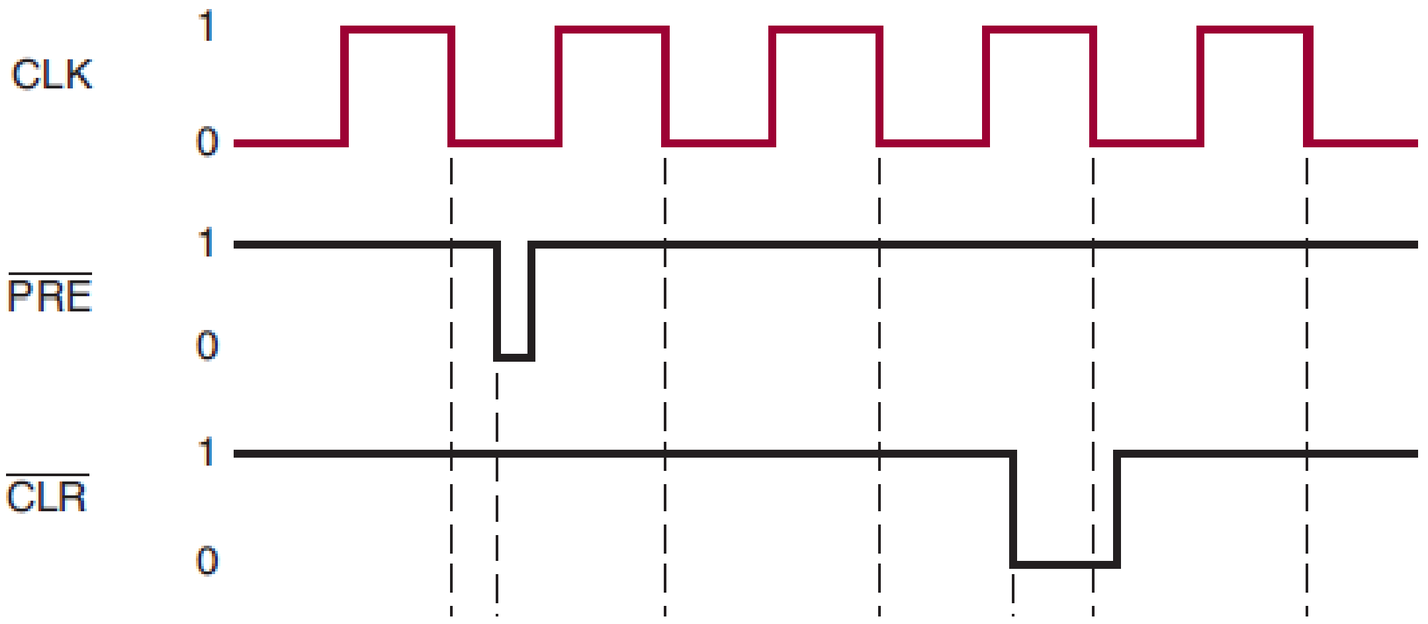




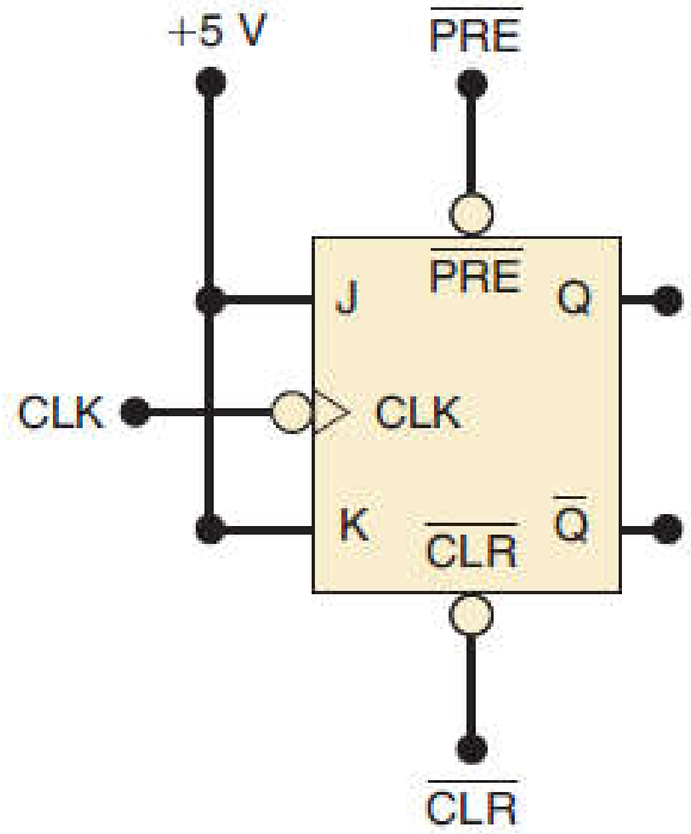
Concept Check

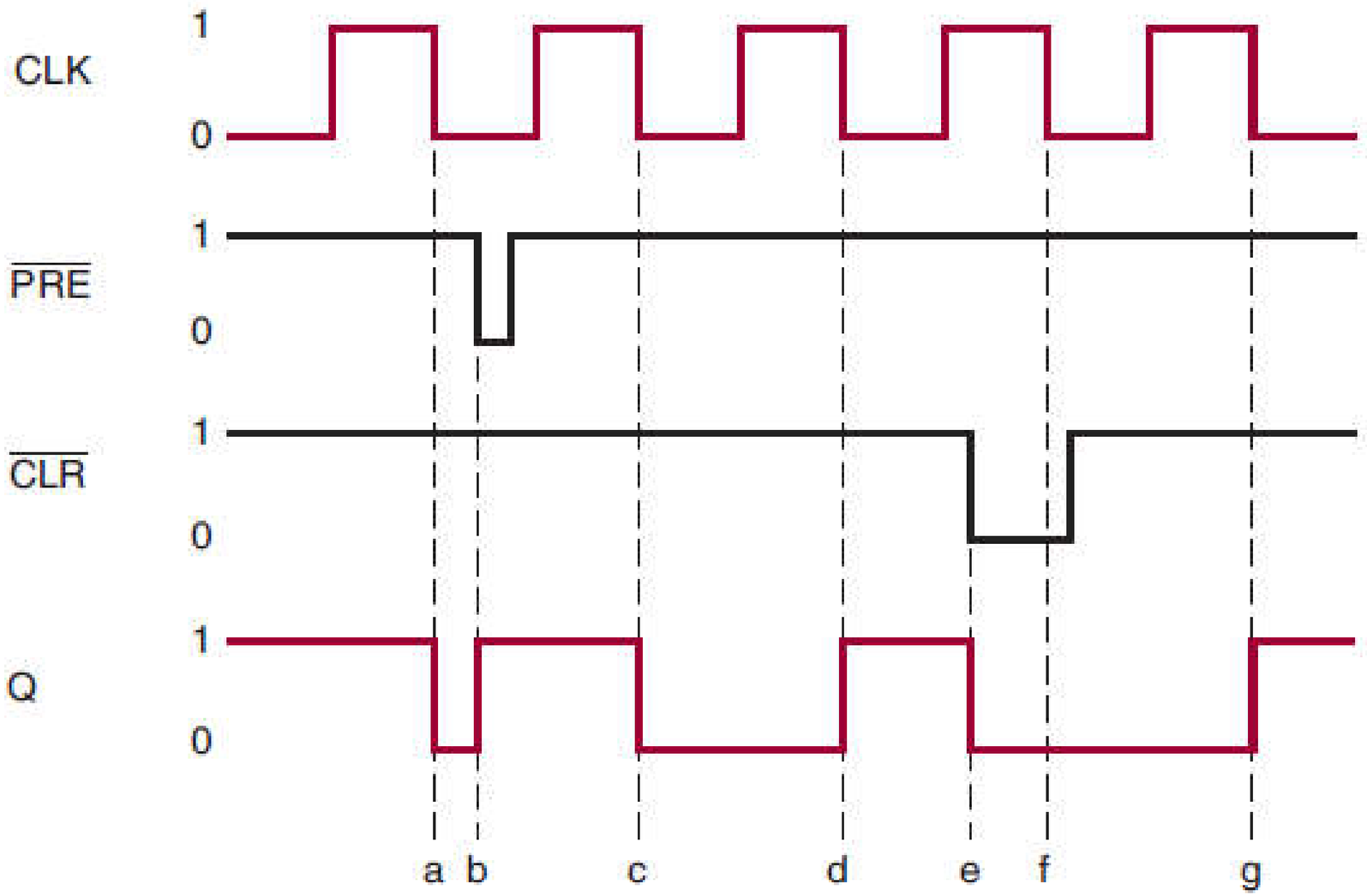
Assume Q=1, Initially



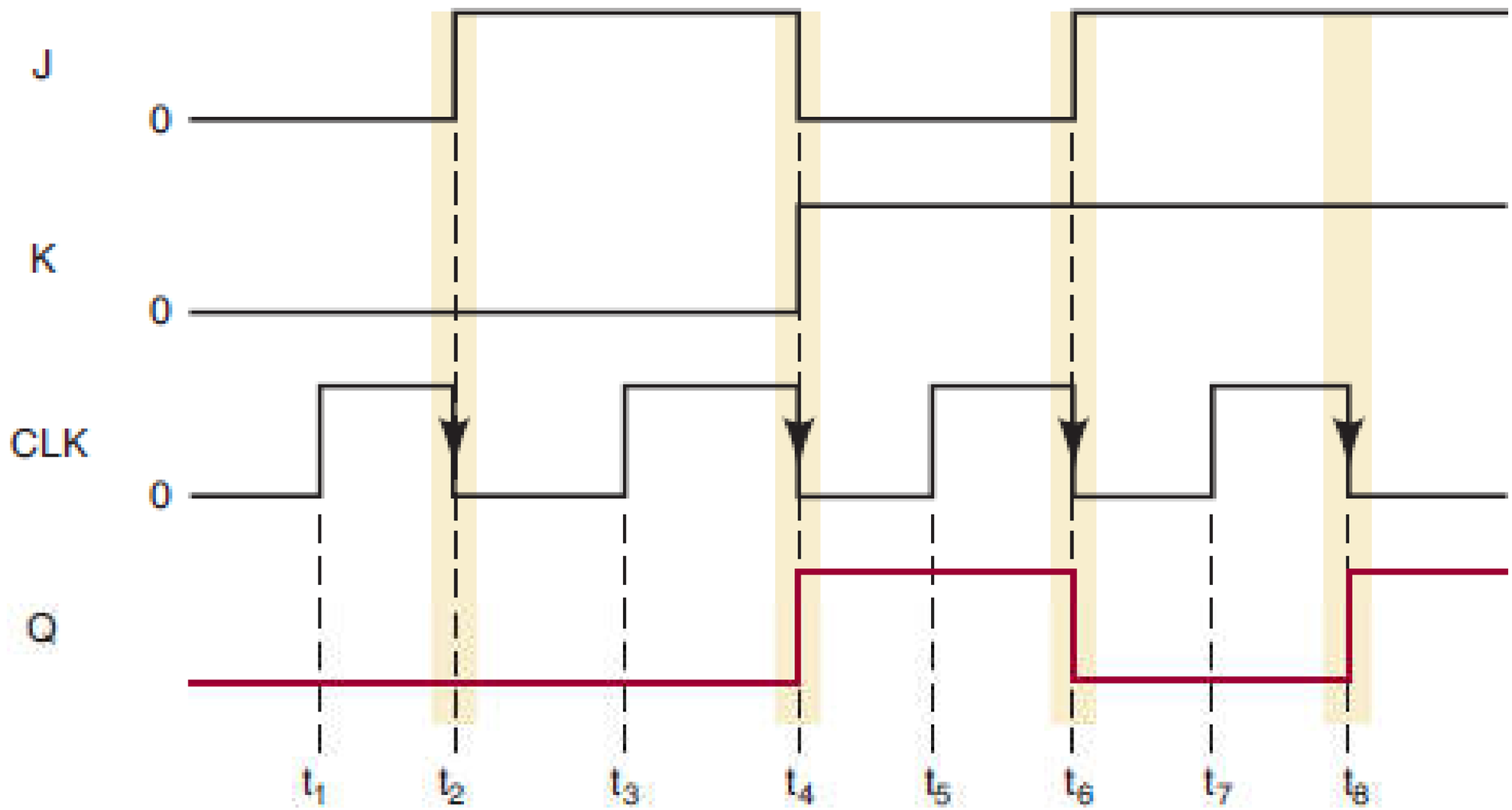


Solution

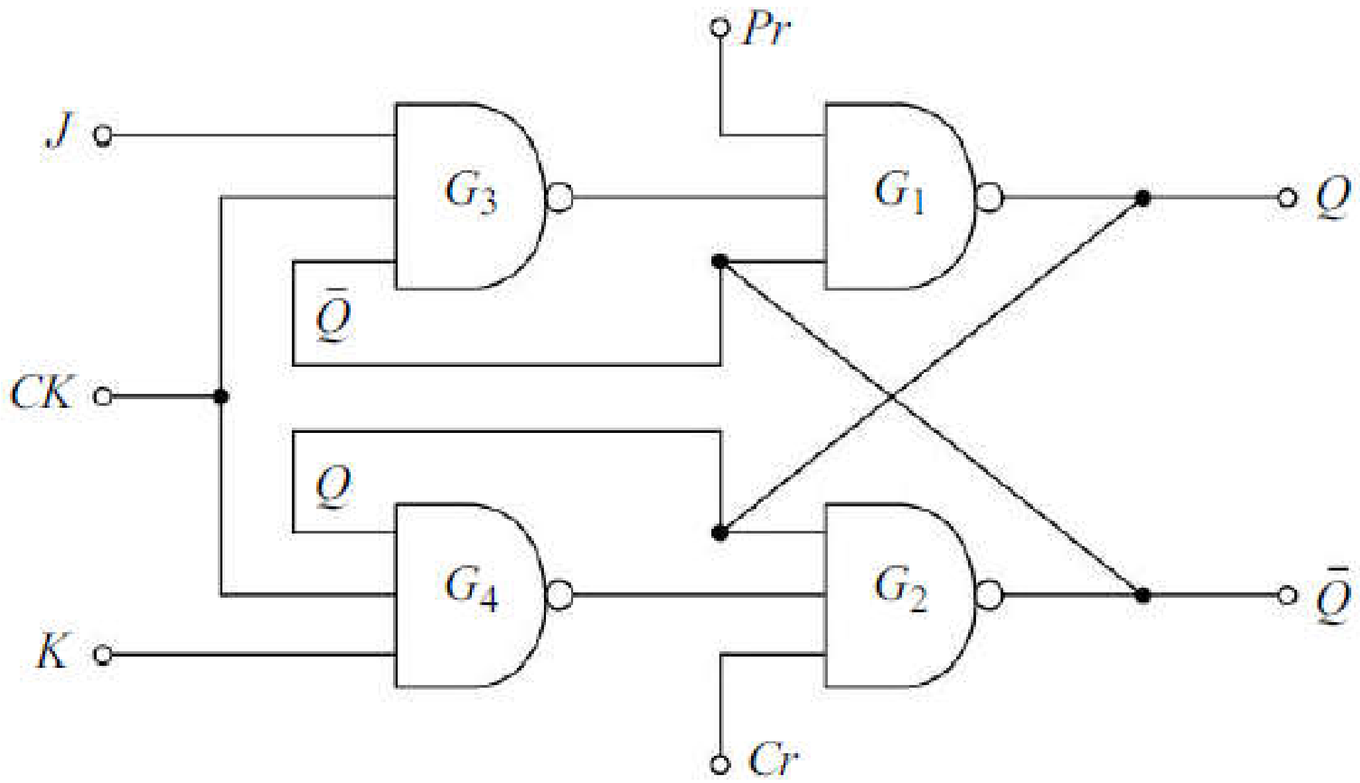


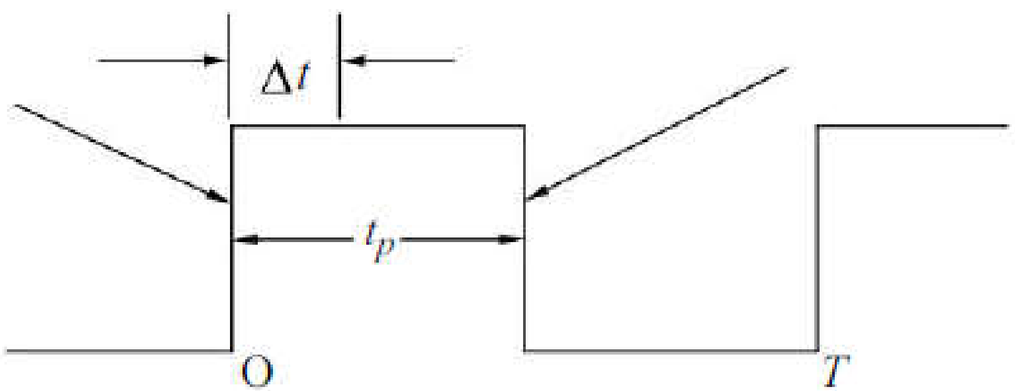


Effect of Propagation Delays



Race Around Condition





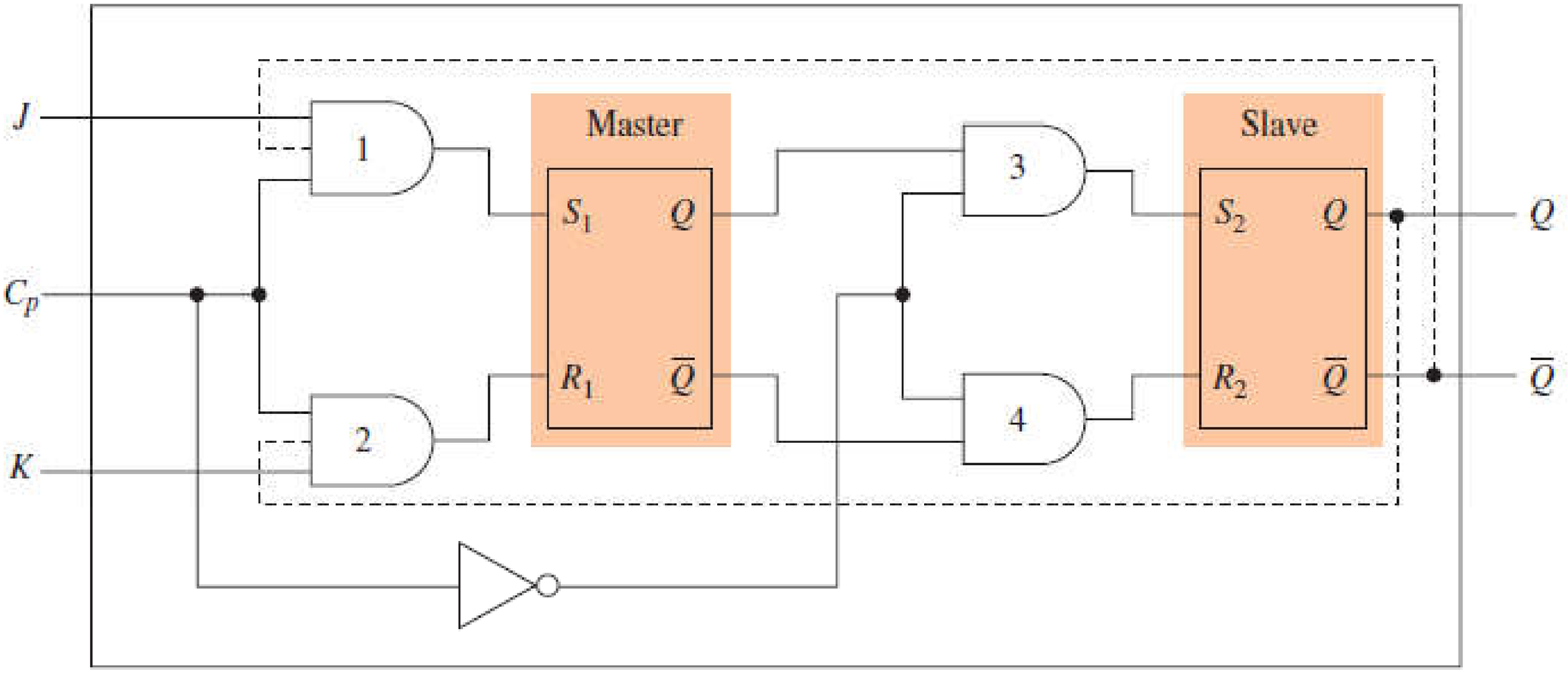
A Clock Pulse

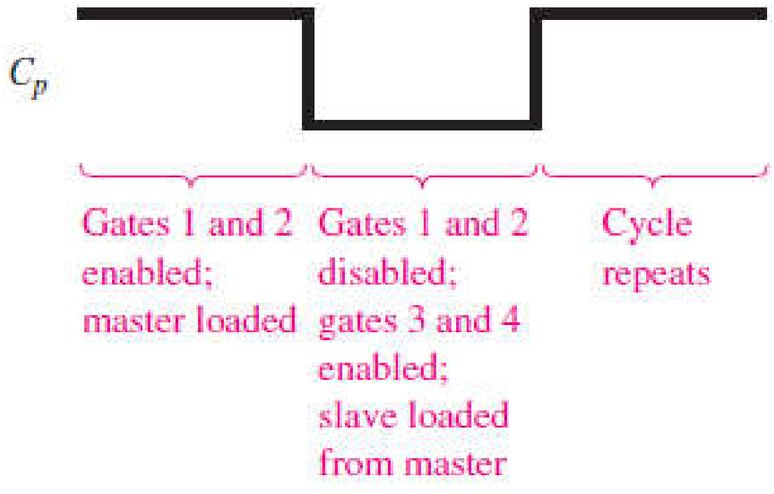
Elimination of RAC

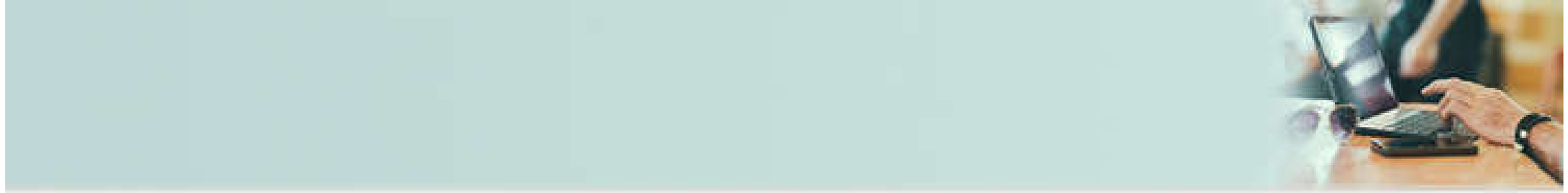
$$t_p < \Delta t < T$$

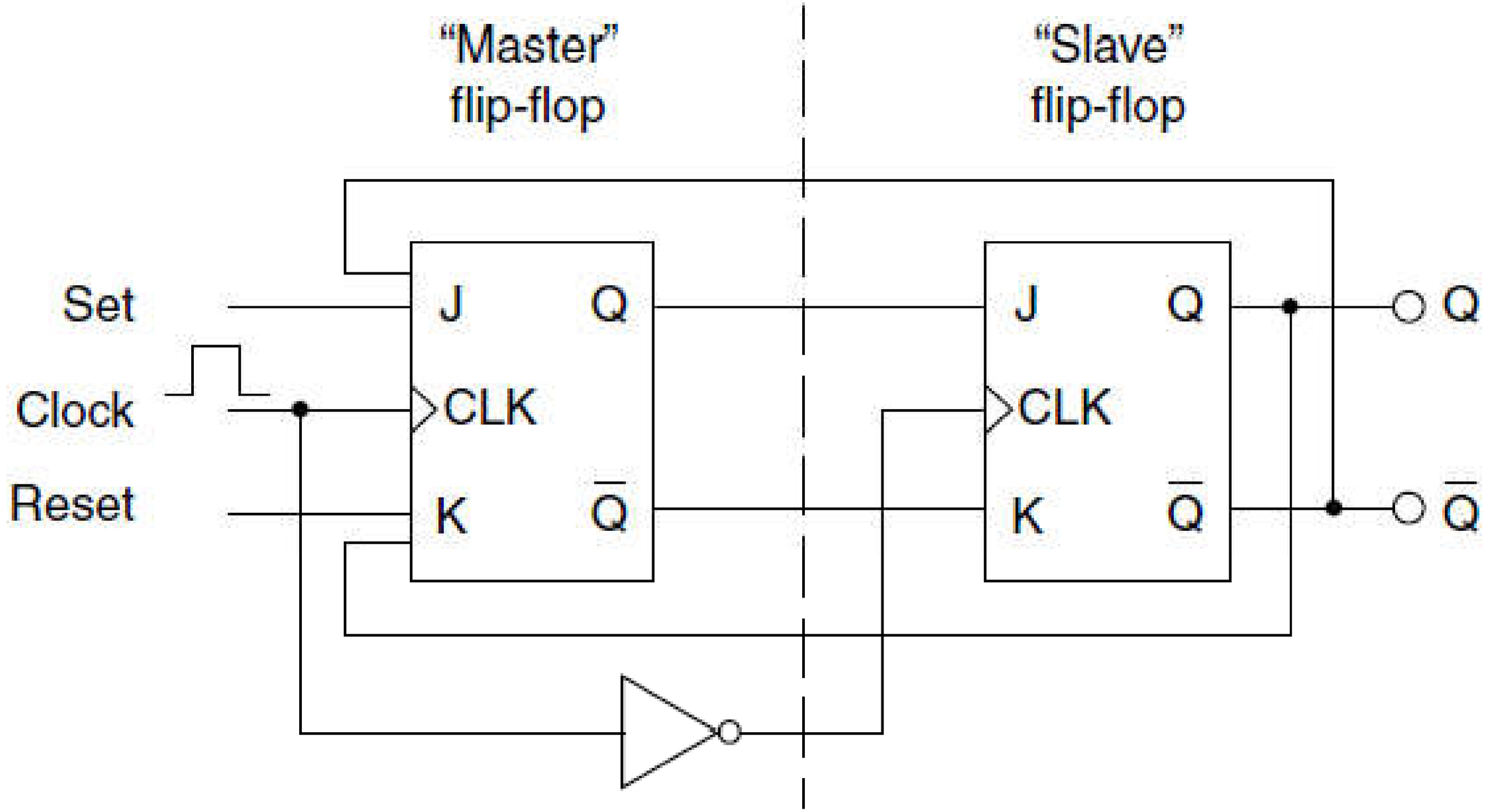
- Pulse width should be less than Propagation Delay
- Use of Master Slave Configuration

Master Slave Configuration



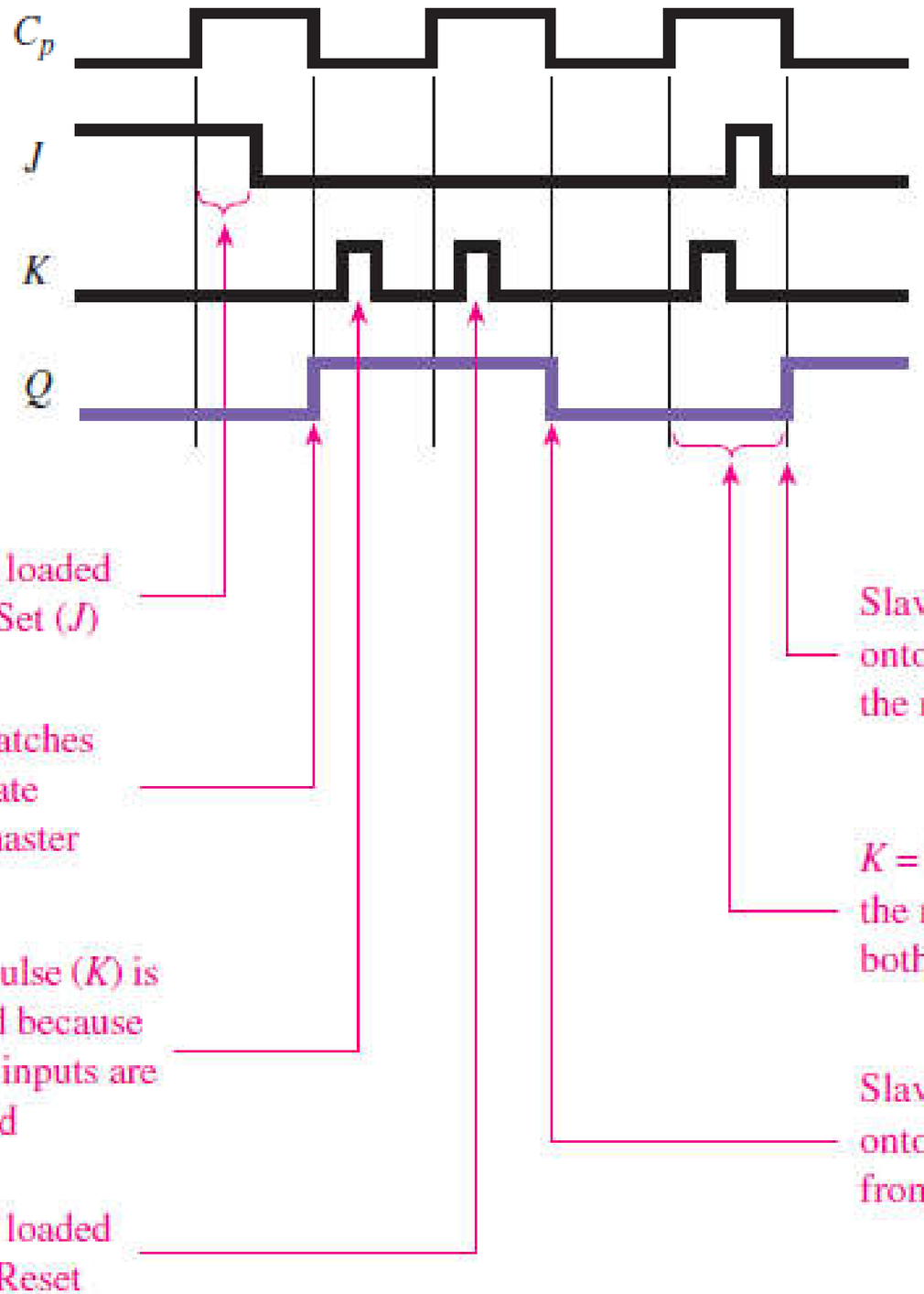





"Master"
flip-flop
"Slave"
flip-flop
Set
Clock
Reset
J
CLK
K
Q
$\overline{Q}$
J
CLK
K
Q
$\overline{Q}$
Q
$\overline{Q}$

Concept Check

Solution:



SR-FF Characteristics Table & Excitation Table

S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Invalid inputs

Characteristic Equation

$Q(t+1) = R'(t)Q(t) + S(t)\ ;\ S(t)R(t) = 0$

Excitation Table

Q(t)	Q(t+1)	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

JK-FF Characteristics Table & Excitation Table

Truth Table

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

Characteristic Equation

$Q(t+1) = K'(t)Q(t) + J(t)Q'(t)$

Excitation Table

Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Finding Characteristic Equation

Table 9.2 State table

J	K	Q_n	$\overline{Q}_n$	Q_{n+1}	$\overline{Q}_{n+1}$	Mode
0	0	0	1	0	1	$Q_n = Q_{n+1}$ and $\overline{Q}_n = \overline{Q}_{n+1}$
0	0	1	0	1	0	
0	1	0	1	0	1	$Q_{n+1} = 0$, reset
0	1	1	0	0	1	
1	0	0	1	1	0	$Q_{n+1} = 1$, set
1	0	1	0	1	0	
1	1	0	1	1	0	$Q_{n+1} = \overline{Q}_n$; toggle
1	1	1	0	0	1	

The Boolean expression for the JK flip-flop is given as:

$$Q_{n+1} = J\overline{Q}_n + K\overline{Q}_n$$

And the Karnaugh map of JK flip-flop is given as in Figure 9.25.

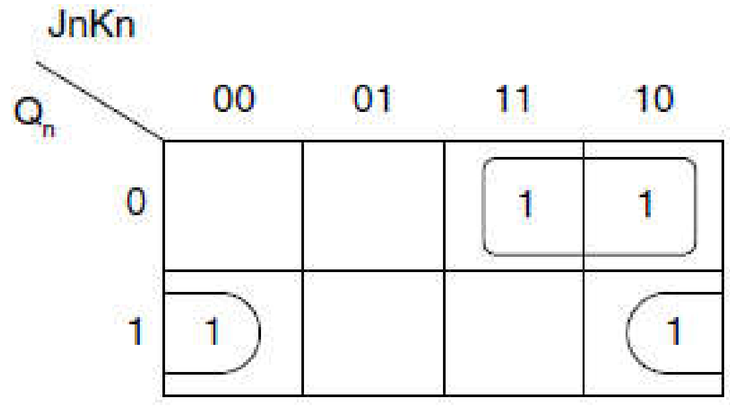


Fig.9.25 Karnaugh map for JK flip-flop

D-FF Characteristics Table & Excitation Table

Truth Table

D	Q(t+1)
0	0
1	1

Characteristic Equation

Q(t+1) = D(t)

Excitation Table

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

T-FF Characteristics Table & Excitation Table

Truth Table

T	Q(t+1)
0	Q(t)
1	Q'(t)

Characteristic Equation

$$Q(t+1) = T'(t)Q(t) + T(t)Q'(t) = T(t) \oplus Q(t)$$

Excitation Table

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Tables

Present State	Next State	*S–R FF*		*J–K FF*		*T-FF*	*D-FF*
		S_n	R_n	J_n	K_n	T_n	D_n
0	0	0	×	0	×	0	0
0	1	1	0	1	×	1	1
1	0	0	1	×	1	1	0
1	1	×	0	×	0	0	1

End of Unit - 3