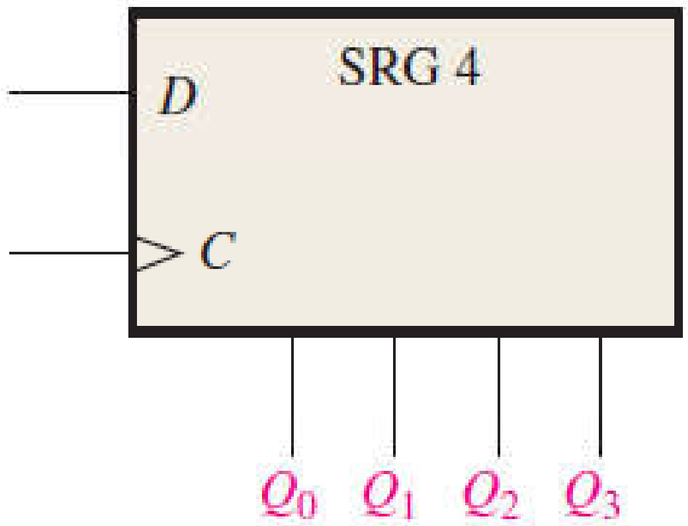
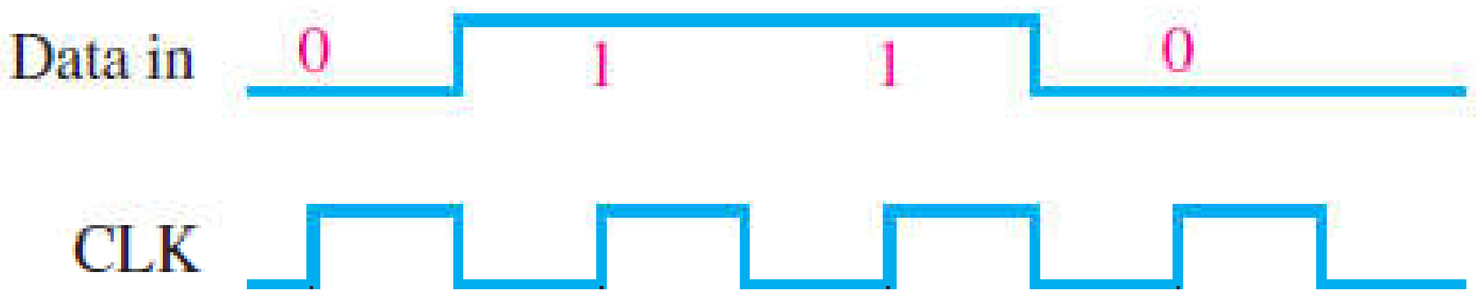
DELD – Tutorial 6

ECED SVNIT

Question - 1

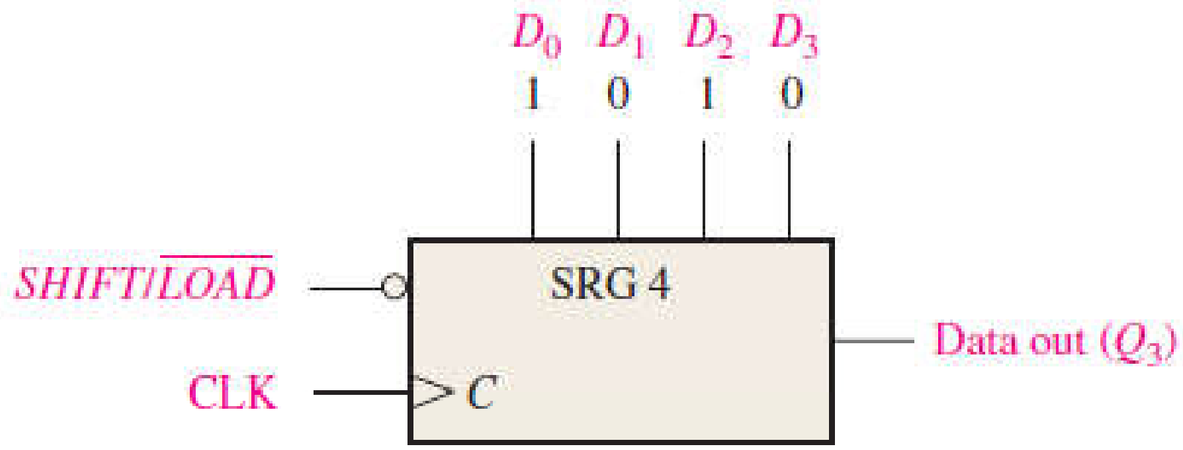
- Predict and draw the FF outputs for the following input. The register initially contains all 1's.

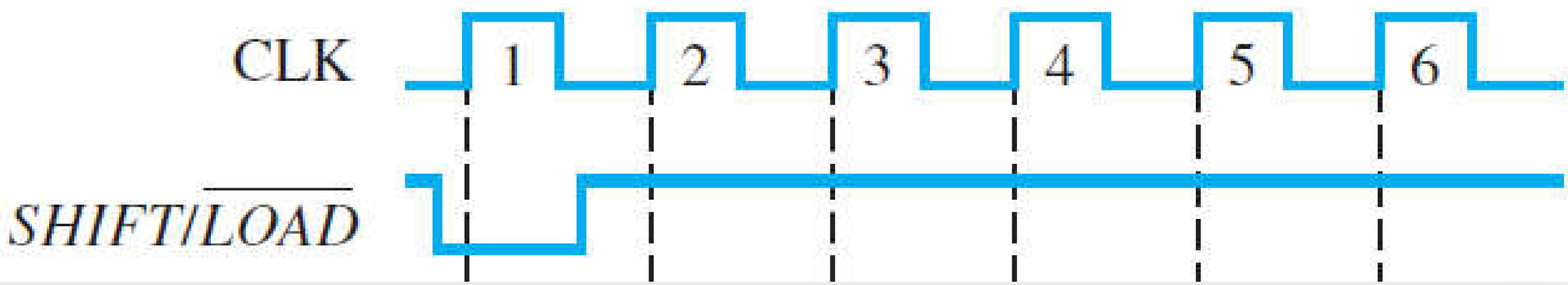




Question - 2

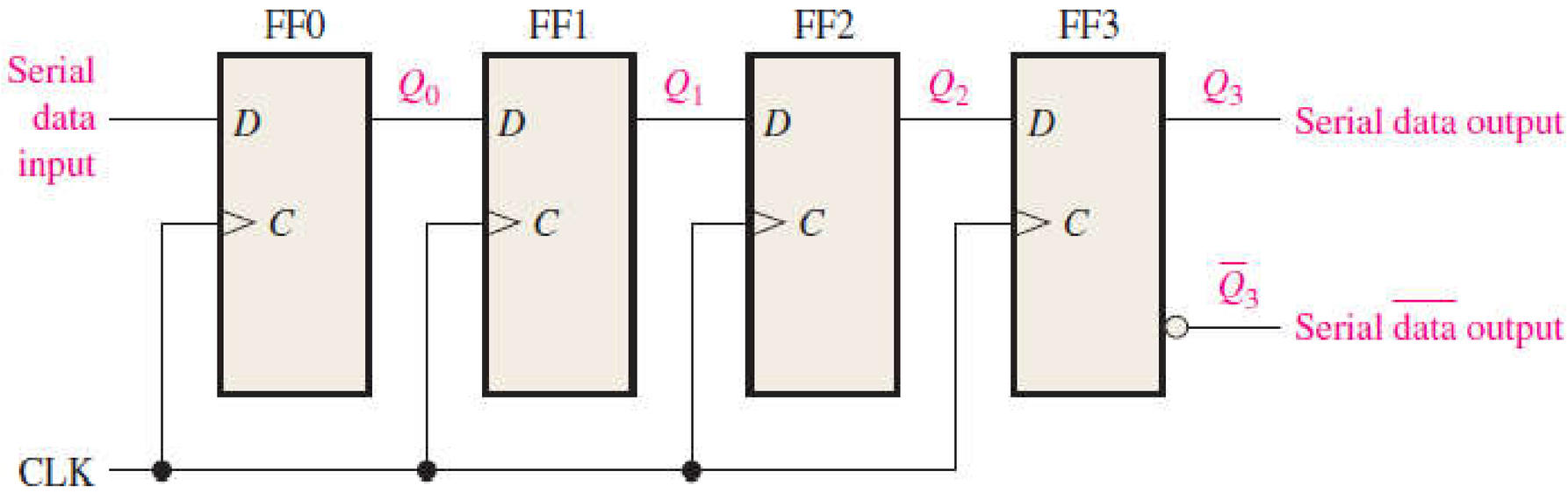
- Show the data output after every clock pulse.

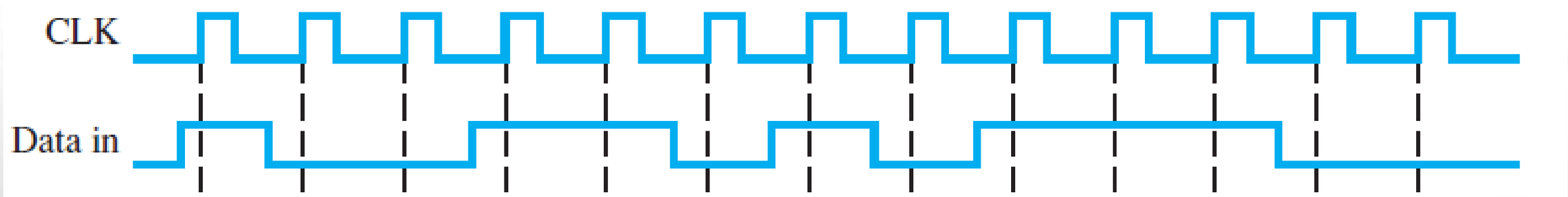




Question - 3

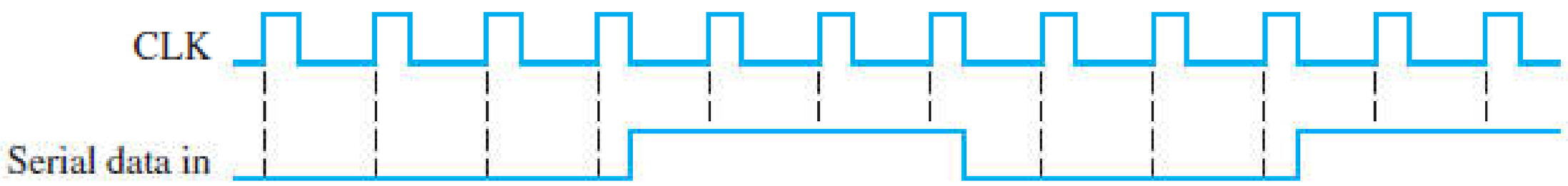
- Sketch the Flip-Flop outputs after every clock pulse. Assume Q=0 initially for all the FFs.





Question - 4

- What is the state of the register in Figure below after each clock pulse if it starts in the 1010011110 00 state?



To Be Continued...