CO-End Sem Quiz

Date: 17/12/2020
Time: 2:30 pm - 3:15 pm
Total Questions: 40
Total Marks: 20

_____Instructions:

1. Press the "TURNED IN" at the end of the quiz in classroom assignment.
2. Try to submit from 3.10 pm, so that your submission can reach to us in defined time limit. Late submission will not be considered.
3. At 3:15 pm descriptive theory questions will be uploaded on Classroom.

Your email address (**u19cs012@coed.svnit.ac.in**) will be recorded when you submit this form. Not you? Switch account

* Required

Any instruction that writes to a register like (a) _____ do/does not do so until that instruction reaches the (b) ___ stage of the pipeline. *

- [x] (a) R-type
- [ ] (b) WB
- [x] (b) MEM
- [x] (a) sw
- [ ] (a) lw

An M-bit processor has *

- (●) M-bit Instruction Register
- ( ) Both of these
- ( ) M-bit Program Counter
- ( ) None of these

The instruction format that has an advantage of short programs when evaluating arithmetic expressions is _____. *

- (●) Three address
- ( ) One address
- ( ) Two address
- ( ) Zero address

There is a system with 1024 cache lines and 32 Bytes per line. Then Index bits are __(a)__ and off set bits are ___(b)___. *

- ( ) (a) 15, (b) 5
- ( ) (a) 5, (b) 10
- ( ) (a) 10, (b) 15
- (●) (a) 10, (b) 5

_____ method is used to establish priority by serially connecting all devices that request an interrupt to/from the processor. *

- (●) Daisy chaining
- ( ) None of these
- ( ) Polling
- ( ) Priority

The instruction(s) which depend/s on the sign extend unit for their correct operation are _____ *

- [ ] beq
- [ ] none of these
- [x] lw
- [x] sw
- [ ] j

Two machines implement support for the same machine language, but have different hardware designs. Except the processor, the two machines are identical w.r.t. RAM, hard drive performance, etc. Machine A has a substantially higher clock rate than machine B. Nevertheless, execution of a certain machine language program, with the same input, takes substantially _____ on machine B than on machine A, because _____ *

- ( ) less time, machine B has a higher average CPI for this program
- ( ) less time, machine B has a lower average CPI for this program
- (•) more time, machine B has a higher average CPI for this program
- ( ) more time, machine B has a lower average CPI for this program

_____ is the faster control unit. *

- ( ) Both of these
- ( ) Microprogrammed
- (•) Hardwired

The addressing mode techniques help *

- [ ] to reduce number of bits in the field of instruction
- [ ] Both of these
- [ ] None of these
- [x] to specify the rule to interpret address field of the instruction

In which addressing mode the operand is given explicitly in the instruction *

- [ ] None of these
- [ ] Register
- [ ] Direct
- [x] Immediate

Modern compiler for RISC based architectures make optimization of instruction scheduling to make use of CPU _____ efficiently. *

- [ ] None of these
- [ ] Both of these
- [x] Without pipeline
- [ ] Pipeline

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In RISC machines, the memory access instructions are *

- (●) none of these
- ( ) PUSH and POP
- ( ) LW and SW
- ( ) CALL and JR

Consider a system of 8-bits. Select the decimal value of the given binary number: 11111111. Assume this binary number is in two's complement format. *

- ( ) None of these
- ( ) 0
- ( ) -255
- ( ) 255
- (●) -1

For the pipeline processor, select the appropriate one: *

- [ ] None of these
- [ ] The control signals relevant to each instruction must move forward, stage by stage.
- [x] The pipeline registers only update on each clock cycle.
- [x] The control signals relevant to each instruction must move forward along with the instruction.
- [ ] The clock cycles are not balanced.

In MIPS, to perform the operation to move data from register $s2 to register $s1, can be done using the following instructions: *

- [x] add $s1, $s2, $zero
- [x] or $s1, $s2, 0
- [ ] subi $s1, $s2, 0
- [x] or $s1, $zero, $s2

In the _____ processor design, ideally one instruction is completed in _____ clock cycle, relative to the _____ clock cycle of the _____ processor design. *

- ( ) single cycle, shorter, long, pipelined
- ( ) none of these
- ( ) both of these
- (•) pipelined, shorter, long, single cycle

Following are the advantages of using a larger page size in virtual memory concept: *

- [x] Fewer TLB misses
- [ ] More TLB misses
- [ ] More page faults
- [x] Page table can be bigger
- [ ] Page table can be smaller
- [x] Fewer page faults

_____ is used to decentralize the decision to avail greater flexibility to avail the I/O system to the processor. *

- ( ) Both of these
- ( ) Centralized
- (•) Arbitration
- ( ) None of these

For the following C Code to MIPS conversion, what are the two instructions group to use from the given options. Consider base address of array is in $s2 register. *

```
for(i = 0; i < 100; i++)
  A[i] = i;
```

```
        add  $t0, $zero, $zero
        addi $t1, $zero, 100
LOOP:   [                    ]
        addi $t0, $t0, 1
        beq  $t0, $t1, LOOP
```

- (•) sw $t0, 0($s2) addi $s2, $s2, 4
- ( ) sw $t1, 0($s2) addi $s2, $s2, 4
- ( ) lw $t0, 0($s2) addi $s2, $s2, 4
- ( ) sw $t1, 0($s2) addi $s2, $s2, 1

When subroutine is called, address of instruction following the call instruction is stored on _____ and program execution is transferred to _____ address. *

- ( ) queue and subroutine
- ( ) stack and callee program
- (•) stack and subroutine

The advantages of cache memory is/are _____. *

- [ ] None of these
- [ ] Both of these
- [x] Reduction of average access time for CPU memory
- [ ] Reduction of bandwidth of available memory of CPU

_____ is a single address space to store both memory and input-output devices. *

- [x] Memory-mapped I/O
- [ ] Isolated I/O
- [ ] Both of these
- [ ] None of these

The hard disk has the characteristics like: Rotation speed: 6000 rpm, Seek time: 10 ms, 500 bytes per disk sector, 200 sectors per track and Overhead time for each I/O request: 2 ms. Select the time in ms required to read one disk sector at a random location on the disk. *

- [ ] 10.10
- [ ] None of these
- [x] 17.05
- [ ] 20.02
- [ ] 15.05

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Performance is defined by execution time. To compute the relative performance of different processors when executing a particular program, we need to know *

- [x] the number of instructions to be executed
- [x] the cycle length for the clock on each processor
- [ ] none of these

The ____(a)____ cache lines, there would be more conflict ___(b)___ and therefore decrease the ____(c)____ rate. *

- ( ) (a) fewer, (b) hit, (c) misses
- (•) (a) more, (b) misses, (c) hit
- ( ) (a) fewer, (b) misses, (c) hit
- ( ) none of these

In a multi cycle processor, using _____ because fetching the instruction and loading the data can occur in _____. *

- (•) one memory is possible, two different cycles
- ( ) none of these
- ( ) both of these
- ( ) one memory is not possible, one single cycle

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To allow many programs to be “running” or at least “ready to run” at once mostly is feasible due to *

- (●) virtual memory
- ( ) none of these
- ( ) cache memory
- ( ) registers

_____ are the modes of transfer between computer and peripheral I/O devices. *

- (●) All of these
- ( ) DMA
- ( ) Interrupt driven I/O
- ( ) Programmed I/O

If ALUSrc control signal stuck at ____, then instructions lw and sw prevented from executing correctly. *

- (●) 0
- ( ) 1
- ( ) X

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Virtual Address corresponds to ____(a)____ and Physical Address corresponds to ____(b)____. *

- (a) OS address length, (b) RAM size bits
- (a) RAM size bits, (b) OS address length
- (a) OS address length, (b) cache size bits
- none of these

Suppose the MemRead control signal was stuck at 0. The instruction(s) could not be executed correctly is (are) _____. *

- [ ] j
- [ ] none of these
- [ ] sw
- [x] lw

The number of bits required to express _____ are determined by the accuracy desired from the computing system. *

- Both of these
- Exponent
- Mantissa
- None of these

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Some instruction(s) like _____ are not affected by the value 0 or 1 of MemtoReg control signal. *

- [ ] j
- [ ] none of these
- [x] sw
- [x] beq

Each instruction is executed by a set of ____(a)_____ stored in ____(b)_____ in microprogrammed control unit. *

- ( ) micro instructions, main memory
- ( ) instructions, main memory
- ( ) instructions, control memory
- (•) micro instructions, control memory

During the program execution content of main memory undergo _____(a)_____ but control memory has _____(b)_____ microprogram. *

- ( ) (a) fixes, (b) changed
- (•) (a) changes, (b) fixed
- ( ) None of these

Following are the program control instructions: *

- ○ Branch
- ○ Jump
- ○ Call a subroutine
- ◉ All of these

For the given ISA design principle "Simple is faster", select the statement from following statements that best describes how the MIPS design affected: *

- ○ MIPS has 32 registers, rather than many more
- ○ Each MIPS native instruction performs one function and requires one cycle to execute
- ○ none of these
- ○ both of these

Following are the correct unsigned and signed decimal values of the given binary number 10110110: *

- ◉ 182, -74
- ○ -82, 74
- ○ 82, -74
- ○ -182, 174

Branch instructions on MIPS can only jump backward _____ and forward _____ instructions. *

- [ ] 32767, 32768
- [x] 32768, 32767
- [ ] 32768, 32769
- [ ] 32766, 32767

Compatible processors implement identical instruction sets and will use the programs with the same number of instructions. But, _____. *

- [ ] they implement the ISA same way, which leads to different CPIs
- [ ] they implement the ISA same way , which leads to same CPIs
- [ ] they implement the ISA differently, which leads to same CPIs
- [x] they implement the ISA differently, which leads to different CPIs

Submit