Expt. No:	**3**	**Half Adder and Half Subtractor**
Date:	**27/08/2020**	

AIM: To design and implement Half Adder and Half Subtractor Circuits.

SOFTWARE TOOLS / OTHER REQUIREMENTS:

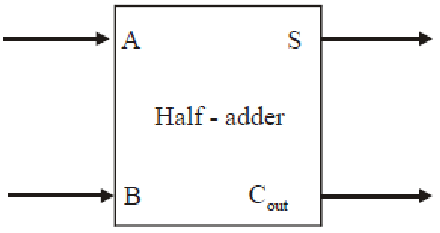
1. Multisim Simulator
2. Logic Gates (AND, NOT and EX-OR)

THEORY:

HALF ADDER:

Adders/Subtractors are important in computers and also in other types of digital systems in which numerical data are processed. An understanding of the basic adder/subtractor operation is fundamental to the study of digital systems.

Figure (a) below shows the logic symbol of a half-adder. As seen from this figure, we find that the half-adder accepts two binary digits on its inputs and produces two digits on its outputs: a sum bit (S) and a carry bit (Cout). Fig (b) shows the truth table for the half-adder.



(*a*) logic symbol

Inputs		*Outputs*	
A	***B***	***S***	C_{out}
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(*b*) truth table

The half-adder follows the basic rules of binary addition:

$$\begin{aligned} 0+1 &= 0 \\ 0+1 &= 1 \\ 1+0 &= 1 \\ 1+1 &= 0 \text{ with a carry of } 1 \end{aligned}$$

The Boolean expression for the sum output (S) can be expressed by the equation.

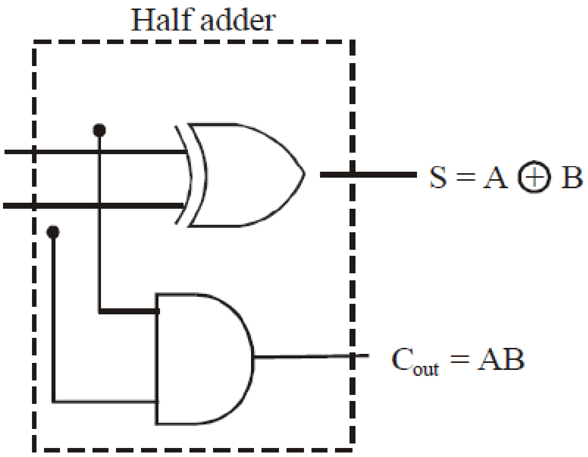
$$S = A\overline{B} + \overline{A}B$$

$$= A \oplus B$$

and the Boolean expression for the carry output by,

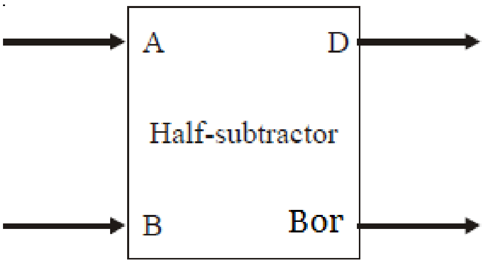
$$C_{ont} = AB$$

The above two equations can be implemented by a logic circuit shown in Fig below. As seen from this figure, the sum output (S) is obtained from an excluse-OR gate while the carry output (Cout) is the output of a two-input AND gate.



HALF SUBTRACTOR:

Fig. (a) below shows the logic symbol of a half-subtractor. As seen from this figure, we find that the half-subtractor accepts two binary digits on its inputs and produce two digits on it outputs : a difference bit (D) and a borrow bit (Bor). Fig (b) shows the truth table for the half-subtractor.



(*a*) logic symbol

Inputs		*Outputs*	
A	*B*	*D*	Bor
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

(*b*) truth table

The half-subtractor follows the basic rules for binary subtraction:

$$\begin{aligned} 0-0 &= 0 \\ 0-1 &= 1 \quad \text{with a borrow of 1} \\ 1-0 &= 1 \\ 1-1 &= 0 \end{aligned}$$

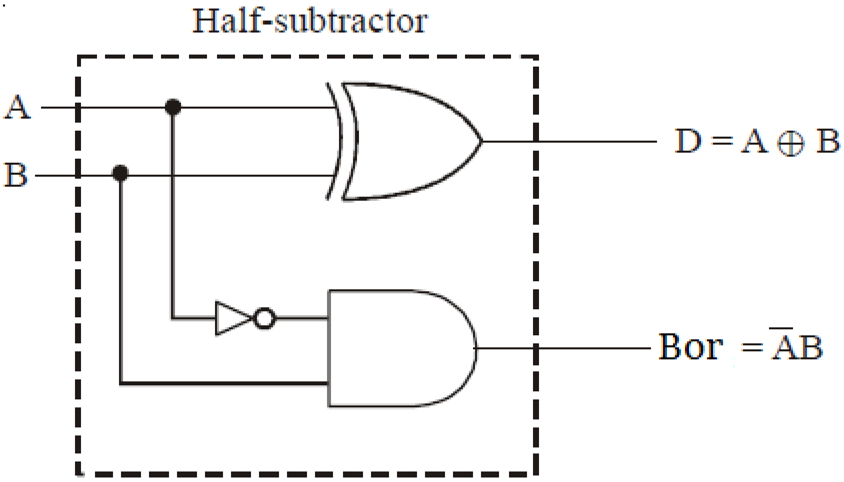
The Boolean expression for the difference bit (D) can be expressed by the equation.

$$\begin{aligned} D &= A\bar{B} + \bar{A}B \\ &= A \oplus B \end{aligned}$$

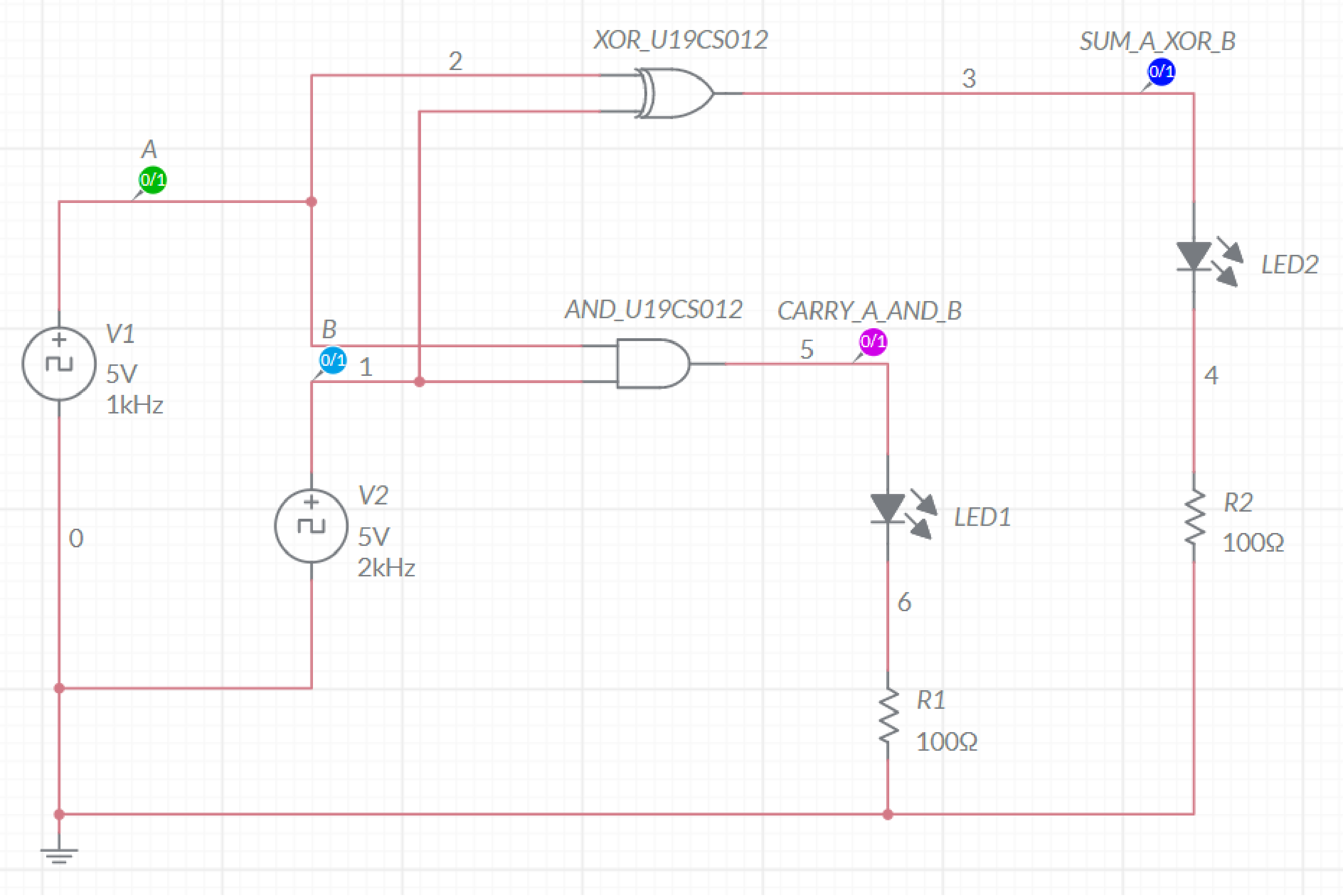
and the Boolean expression for the borrow bit,

$$\text{Bor} = \bar{A}B$$

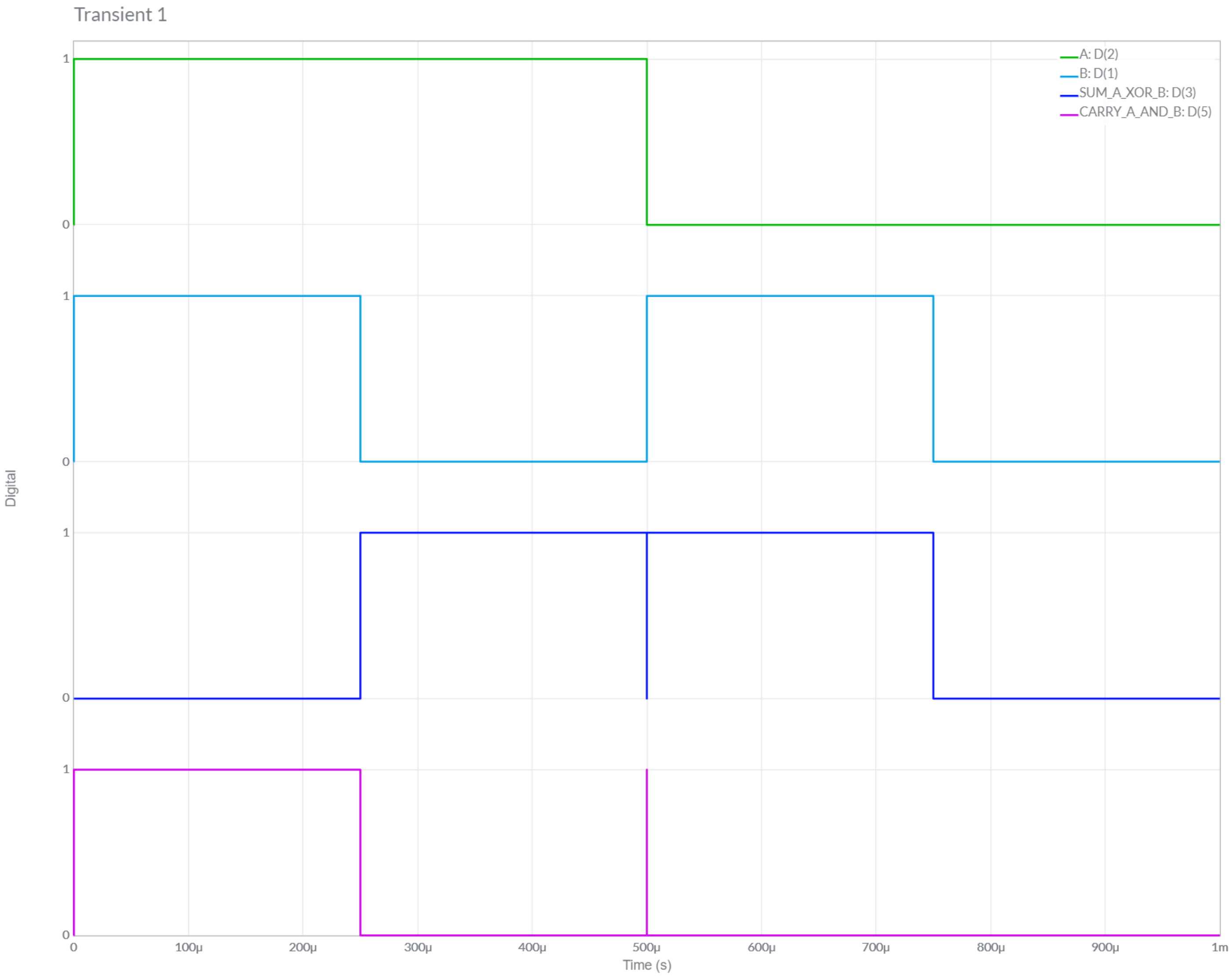
The above two expressions can be implemented by a logic circuit shown in Fig. below. As seen from this figure, the difference output (D) is obtained from an exclusive-OR gate while the borrow bit (Bor) is the output of a two-input AND gate.



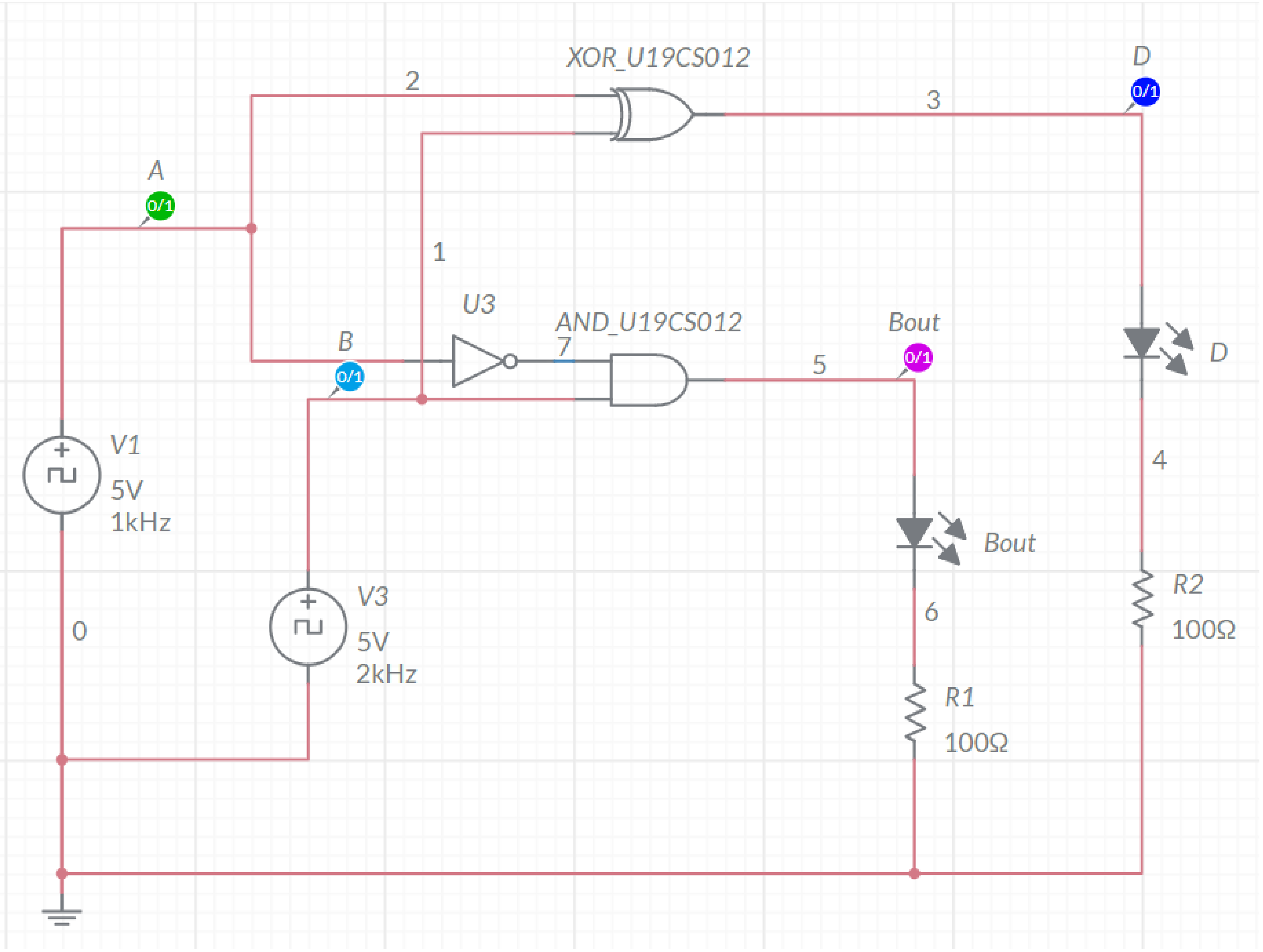
HALF ADDER: CIRCUIT/CONNECTION DIAGRAMS (FROM MULTISIM)



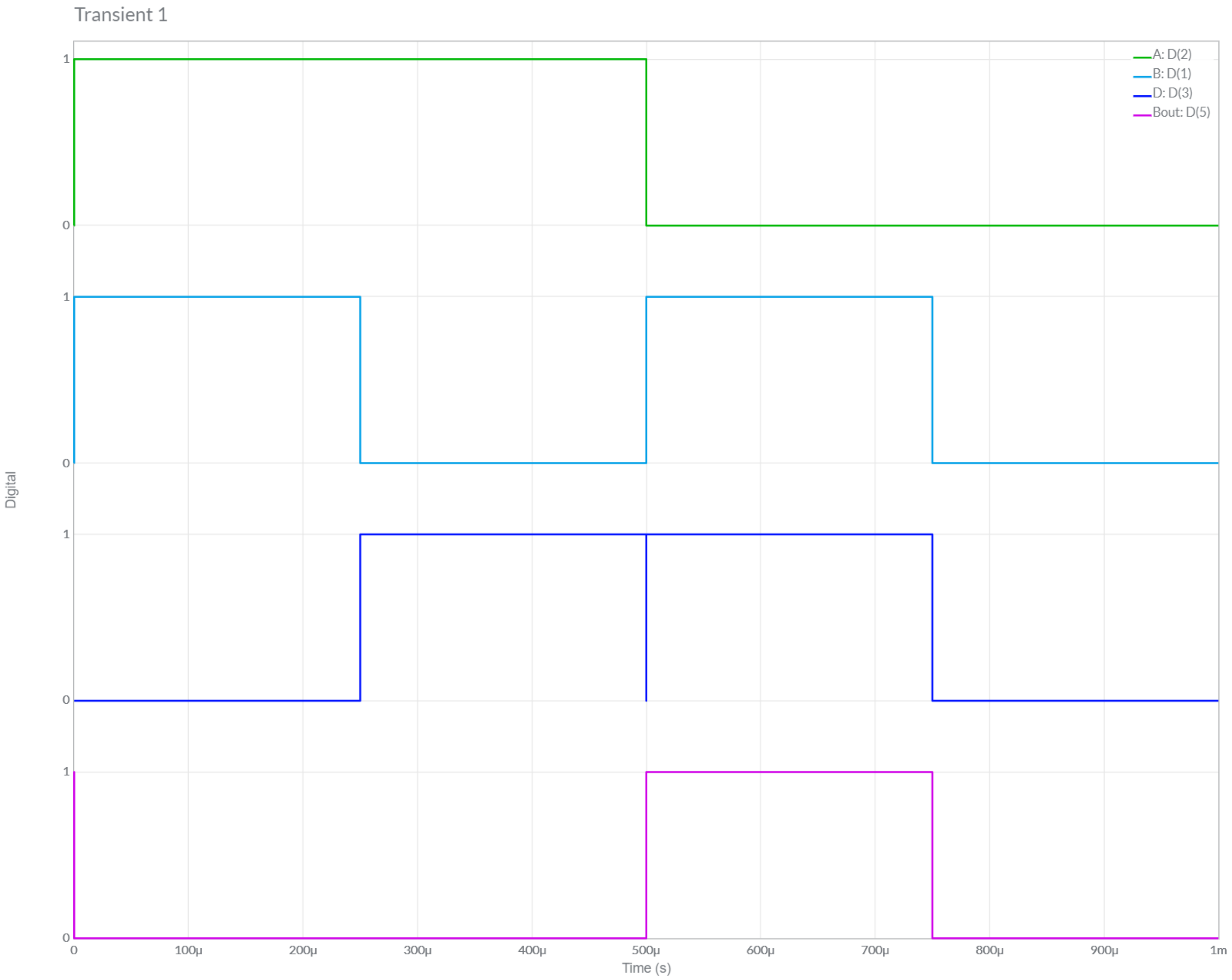
HALF ADDER: OUTPUT PLOTS/WAVEFORMS (FROM MULTISIM):



HALF SUBTRACTOR: CIRCUIT/CONNECTION DIAGRAMS (MULTISIM)



HALF SUBTRACTOR: OUTPUT PLOTS/WAVEFORMS (MULTISIM)



CONCLUSIONS

1.) The Results obtained from the <u>Truth Table</u> from Half-Adder Circuit and <u>Grapher Image</u> [Waveform Simulation] are *Equal*, Hence the Circuit is verified to be Half-Adder.

2.) The Results obtained from the <u>Truth Table</u> from Half-Subtractor Circuit and <u>Grapher Image</u> [Waveform Simulation] are Equal, Hence the Circuit is verified to be Half-Subtractor.

3.) Hence, Half Adder and Half Subtractor Circuit have been Implemented Successfully in Multisim.

ASSIGNMENT-3

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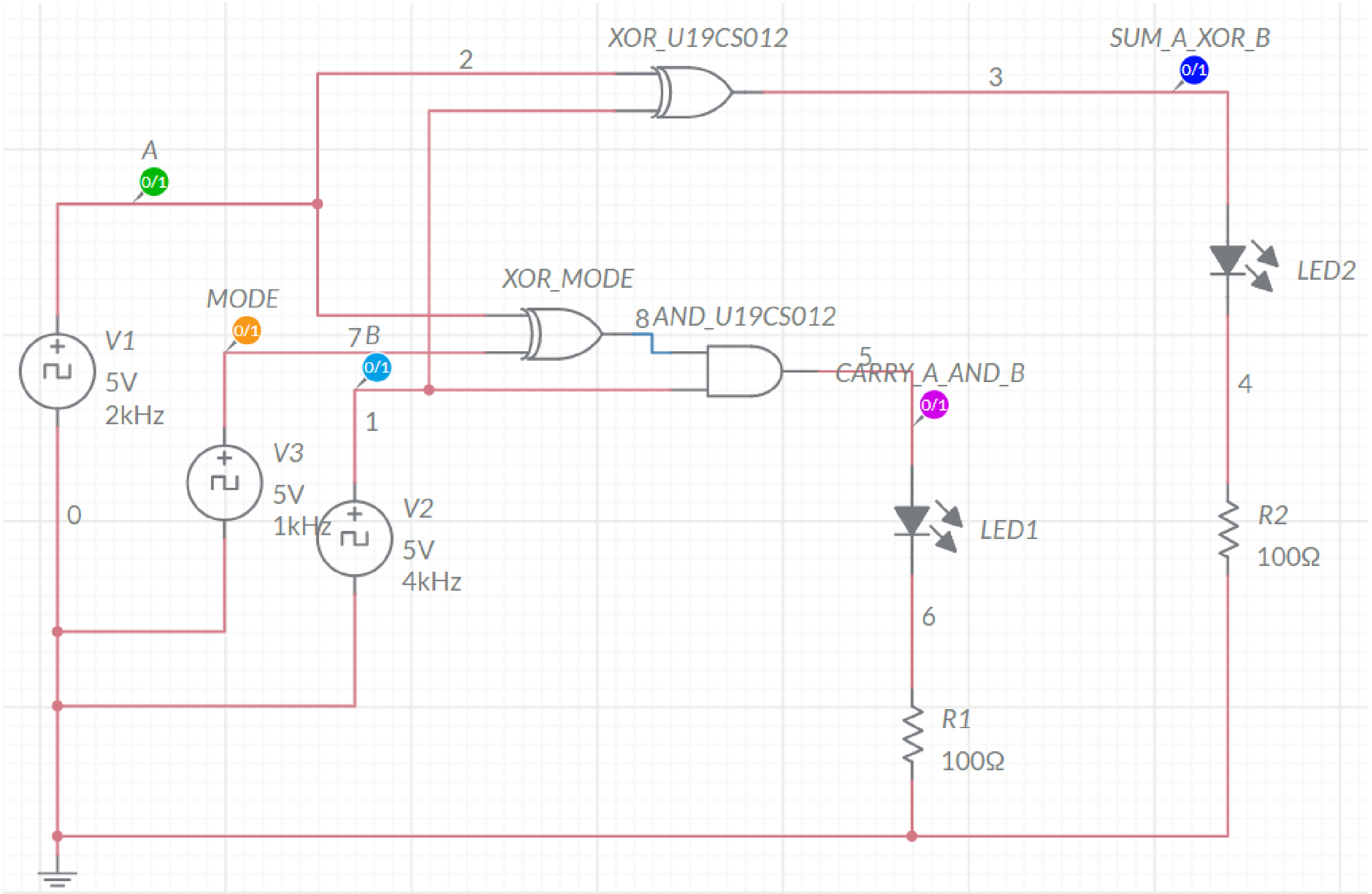
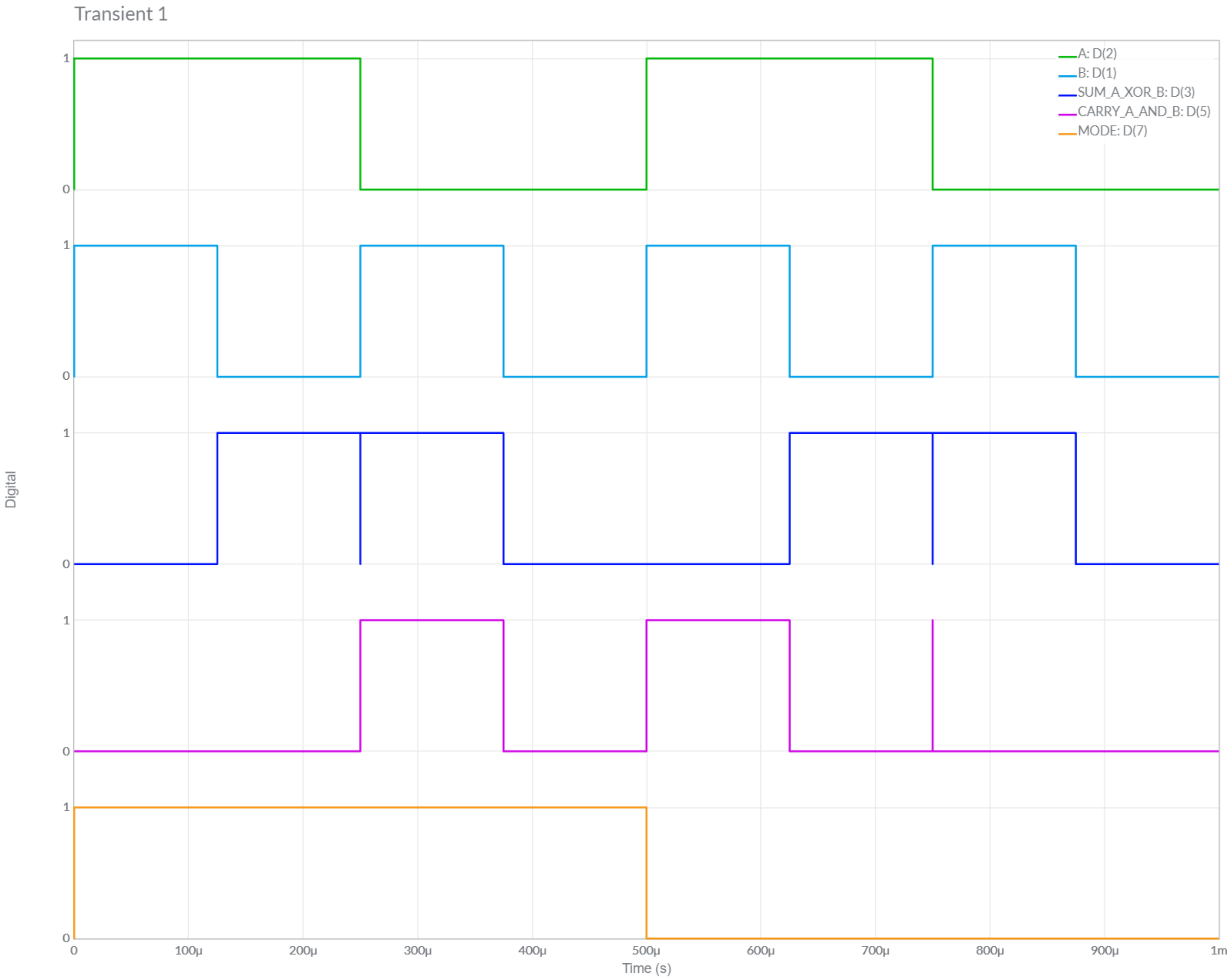
Design and verify their functionality of below circuits with the help of Multisim.

1. Design and implement Half Adder and Half Subtractor (Single Circuit) using Mode Control 'M'.

a.) Implement the circuit in Multisim online



b.) Timing Graph



c.) Truth Table:

When Mode = 1, Circuit Behaves as Half Subtractor Circuit

Borrow Out, Bout= A' . B

Difference, D = A ⊕ B

A	B	B_{out}	D
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

When Mode = 0, Circuit Behaves as Half Adder Circuit
Sum, S = $A \oplus B$
Carry, C = $A \cdot B$

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

The Same Truth Table is Followed for Next 2 Questions as well.

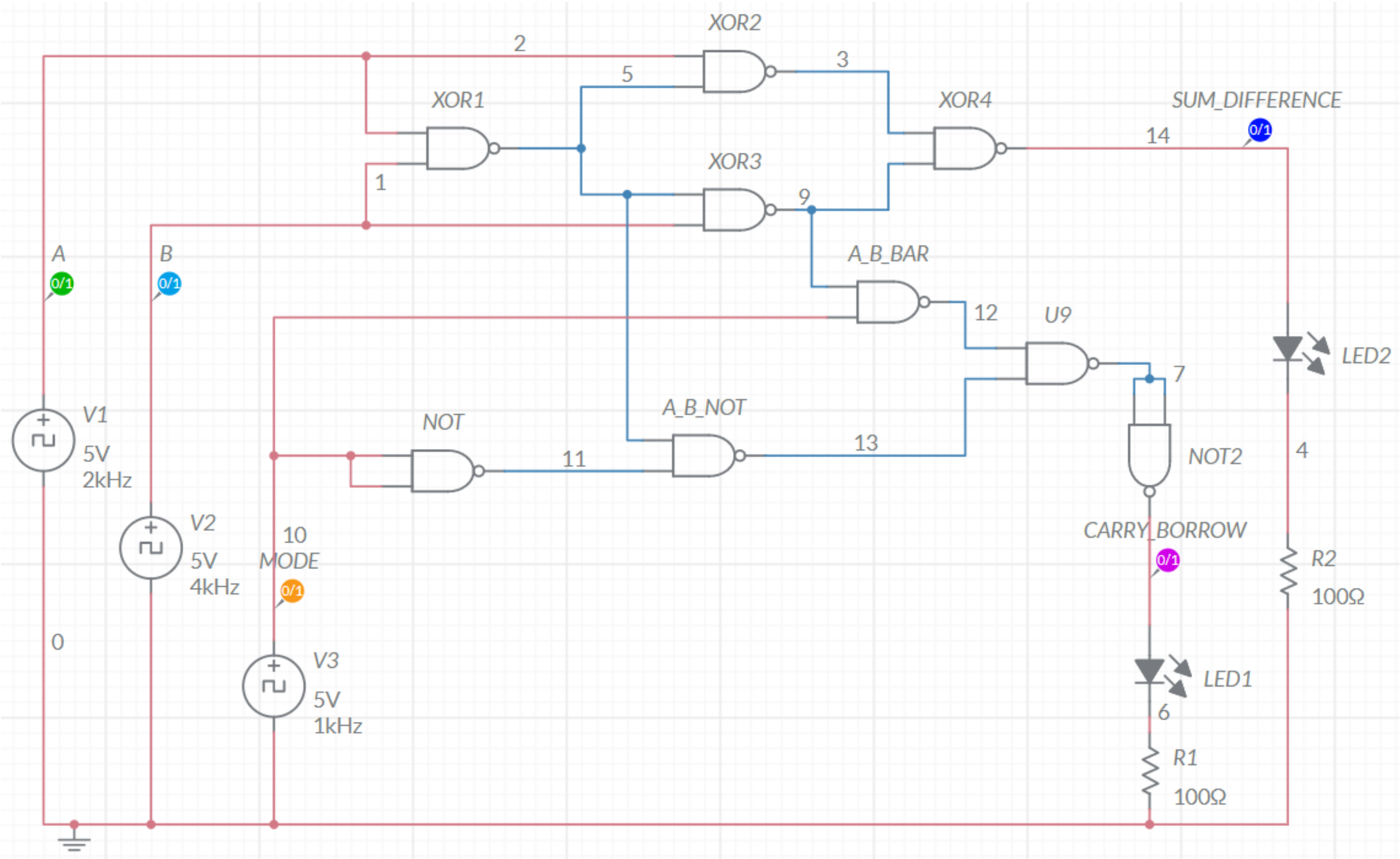
Conclusion:

We can observe from Above Table, Both the *Theoretical* and *Multisim* Values of Given Circuit are **Equal**.
Hence, Experiment is Performed Successfully (without any Error).

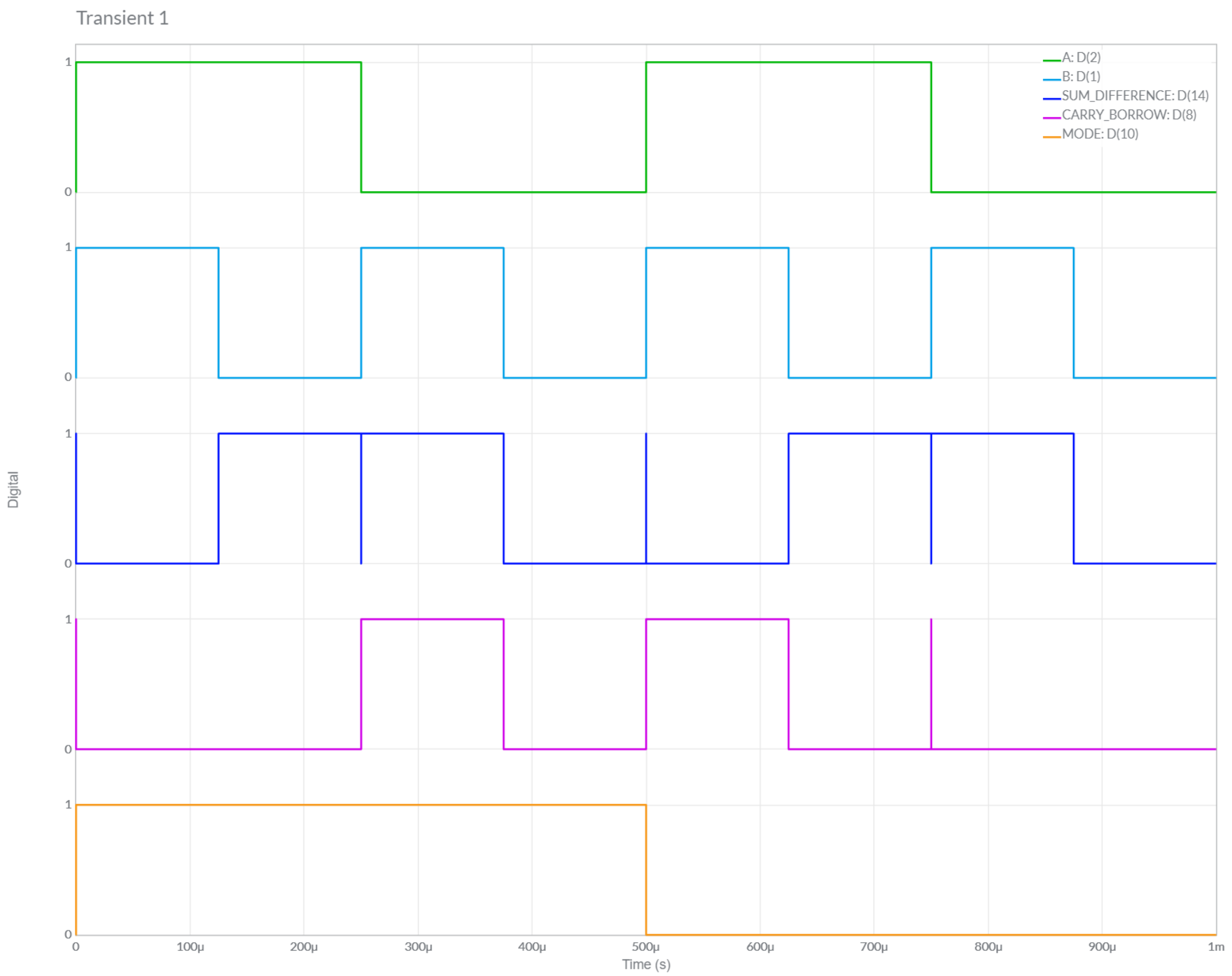
2. Design and implement the circuit in question '1' by using least number of NAND gates only.

Minimum NAND Gates Required = 9

a.) Implement the circuit in Multisim online



b.) Timing Graph



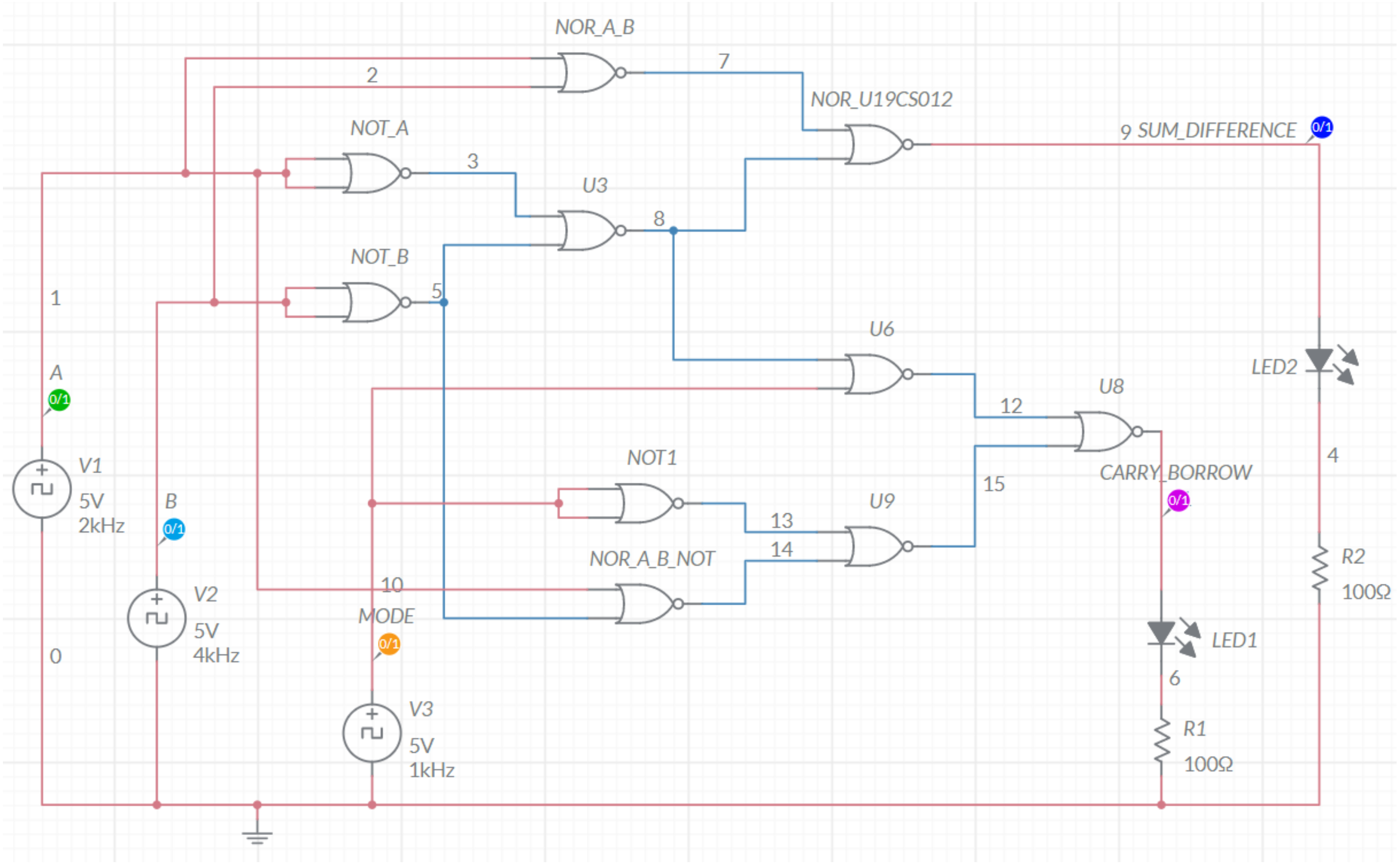
Conclusion:

We can observe from Above Table, Both the *Theoretical* and *Multisim* Values of <u>Given Circuit</u> are **Equal**.
Hence, Experiment is Performed Successfully (without any Error).

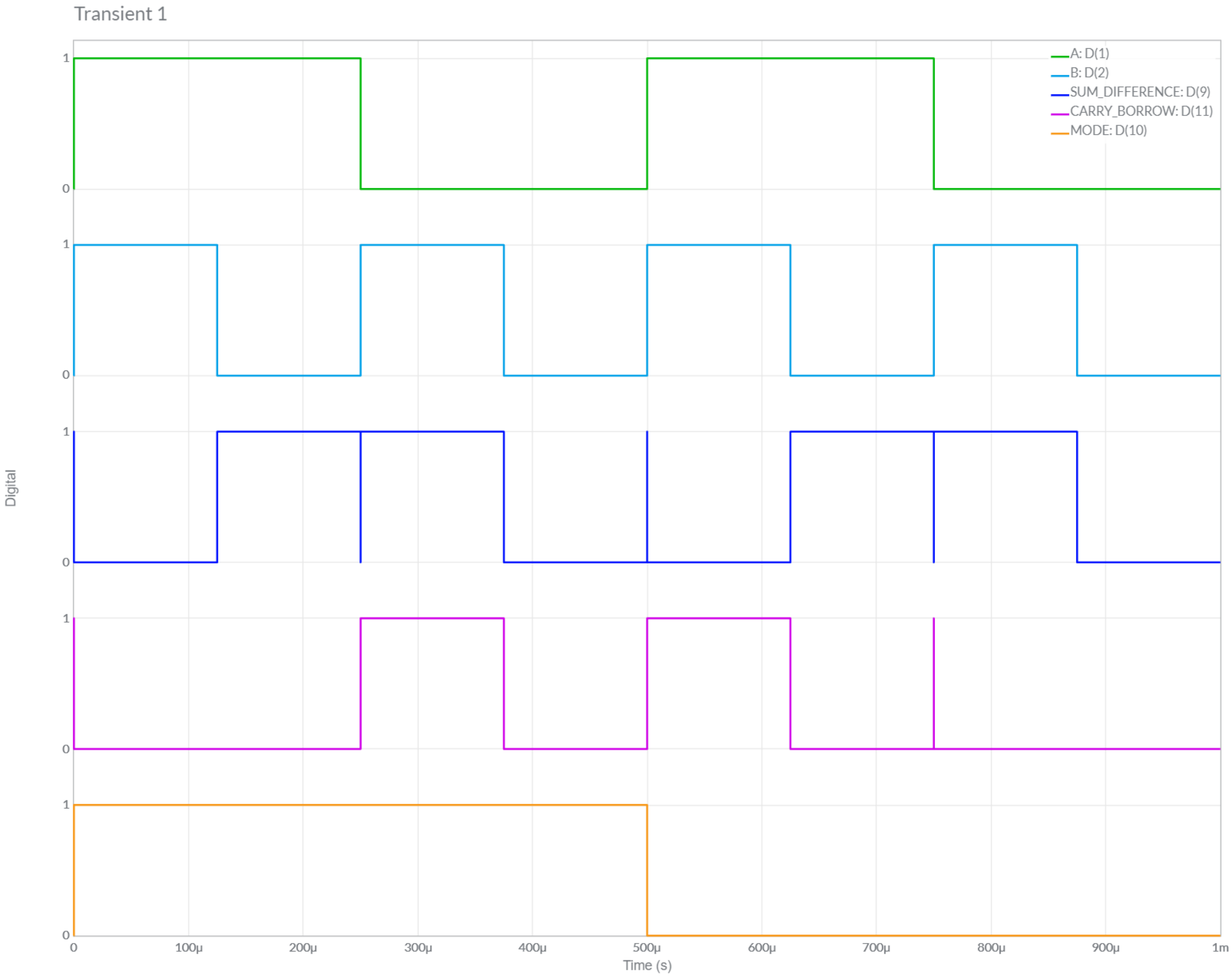
3. Design and implement the circuit in question '1' by using least number of NOR gates only.

Minimum NOR Gates Required = 10

a.) Implement the circuit in Multisim online



b.) Timing Graph



Conclusion:

We can observe from Above Table, Both the *Theoretical* and *Multisim* Values of Given Circuit are **Equal**.
Hence, Experiment is Performed Successfully (without any Error).