SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT
ELECTRONICS ENGINEERING DEPARTMENT

Expt. No:	**10**	**Common Emitter Characteristics & Common Emmiter Amplifier**
Date:	**29-10-2020**	

AIM: To study, the Input-Output characteristics of a BJT in Common Emitter Configuration. Also implement Common Emitter Amplifier.

SOFTWARE TOOLS / OTHER REQUIREMENTS:

1. Multisim Simulator/Circuit Simulator

THEORY:

The most frequently encountered transistor configuration appears in Fig.10.1 for the pnp and npn transistors. It is called the common-emitter configuration because the emitter is common to both the input and output terminals (in this case common to both the base and collector terminals). Two sets of characteristics are again necessary to describe fully the behavior of the common-emitter configuration: one for the input or base–emitter circuit and one for the output or collector–emitter circuit. Both are shown in Fig. 10.2 (a) and 10.2 (b) respectively.

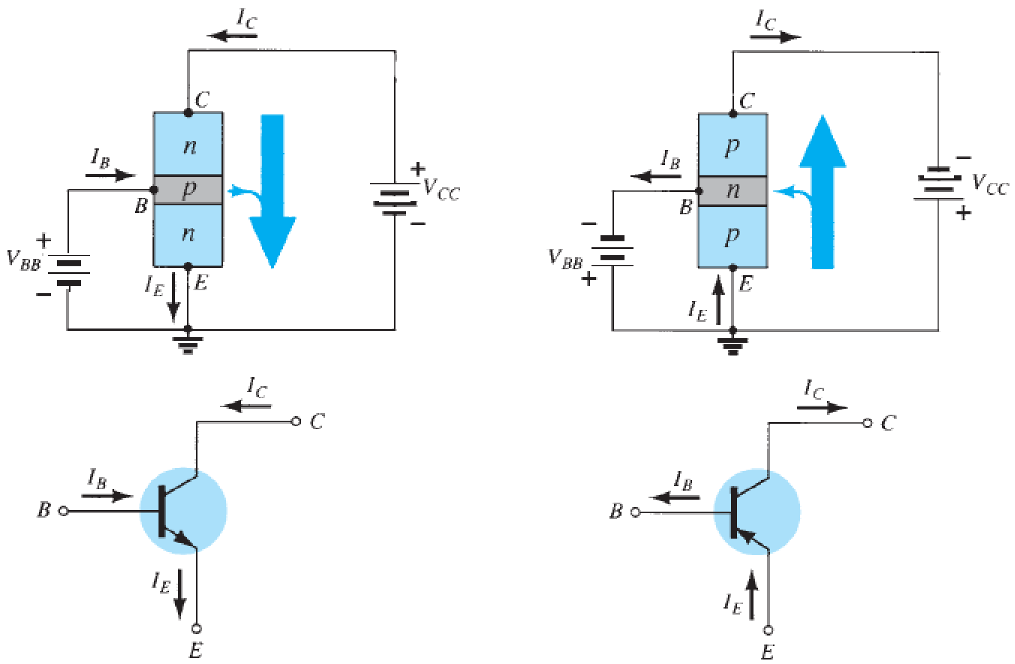


Fig. 10.1

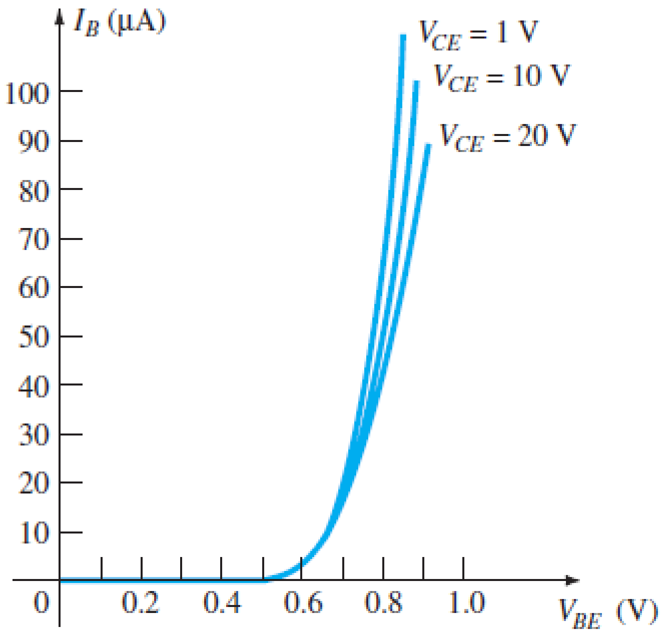


Fig. 10.2 (a) CE Input Characterisitcs

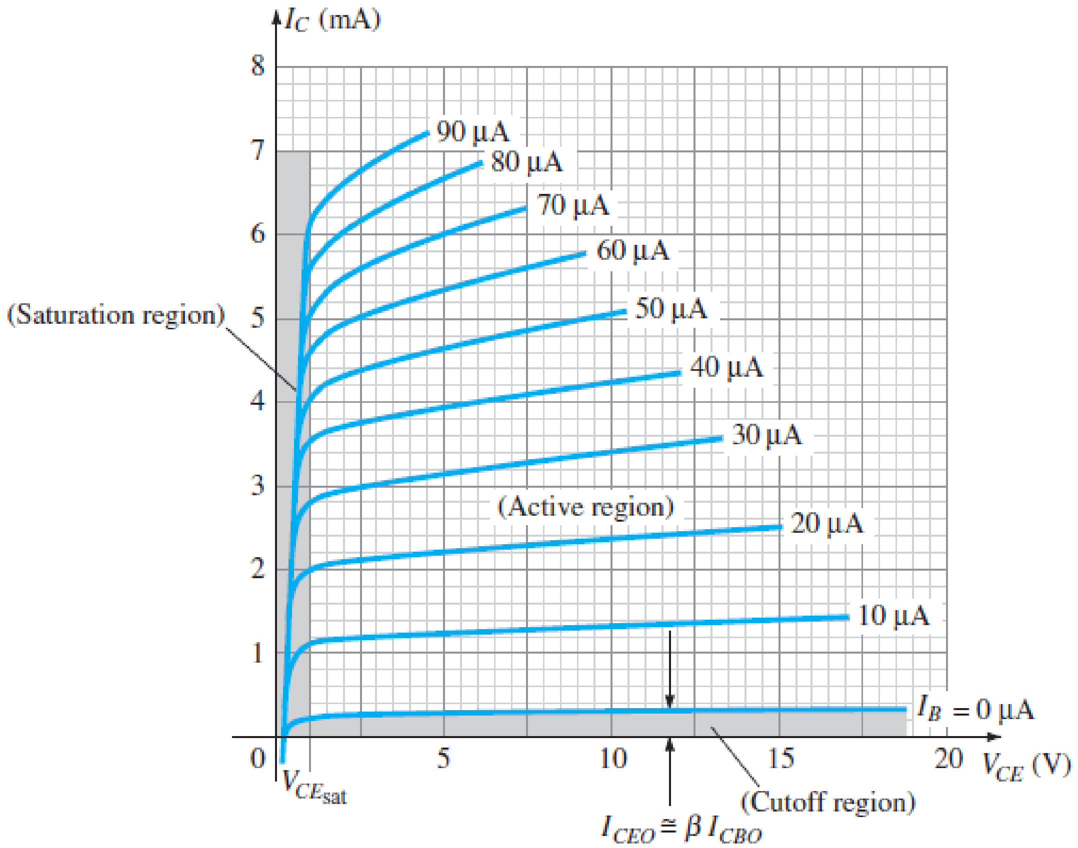


Fig. 10.2 (b) CE Output Characterisitcs

INPUT CHARACTERISTICS

The input characteristics are a plot of the input current (*IB*) versus the input voltage (*VBE*) for a range of values of output voltage (*VCE*). The curve describes the changes in the values of input current with respect to the values of input voltage keeping the output voltage constant.

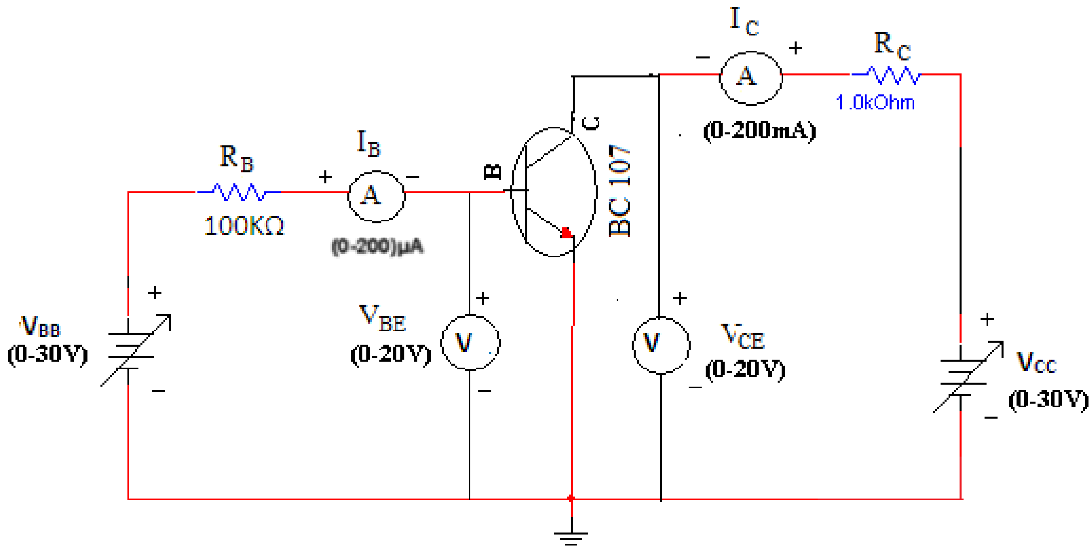


Fig. 10. 3 Circuit Diagram to obtain CE Input/Output Characteristics

PROCEDURE

1. **CONNECT THE CIRCUIT AS SHOWN IN THE CIRCUIT DIAGRAM.**
2. **KEEP OUTPUT VOLTAGE V_{CE} = 0V BY VARYING V_{CC}.**
3. **VARYING V_{BB} GRADUALLY, NOTE DOWN BASE CURRENT I_B AND BASE-EMITTER VOLTAGE V_{BE}.**
4. **STEP SIZE IS NOT FIXED BECAUSE OF NON LINEAR CURVE. INITIALLY VARY V_{BB} IN STEPS OF 0.1V. ONCE THE CURRENT STARTS INCREASING VARY V_{BB} IN STEPS OF 1V UP TO 5V.**
5. **REPEAT ABOVE PROCEDURE (STEP 3) FOR V_{CE} = 3V.**

OUTPUT CHARACTERISTICS

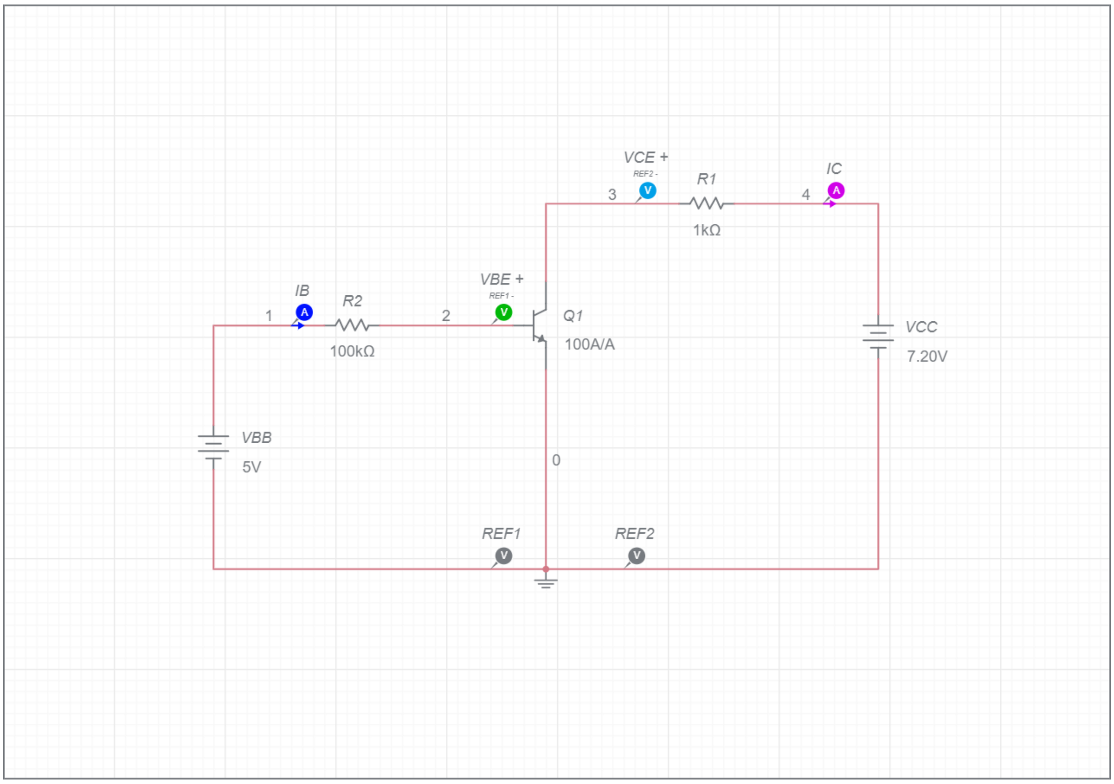
The output characteristics are a plot of the output current (*I C*) versus output voltage (*V CE*) for a range of values of input current (*I B*). The curve describes the changes in the values of output current against output voltage keeping the input current constant.

PROCEDURE

1. CONNECT THE CIRCUIT AS SHOWN IN THE CIRCUIT DIAGRAM.
2. KEEP EMITTER CURRENT I_B = 0μA BY VARYING V_{BB}.
3. VARYING V_{CC} GRADUALLY IN STEPS OF 1V UP TO 5V AND NOTE DOWN COLLECTOR CURRENT I_C AND COLLECTOR-EMITTER VOLTAGE(V_{CE}).
4. REPEAT ABOVE PROCEDURE (STEP 3) FOR I_B = 20μA AND 60μA.

INPUT CHARACTERISTICS

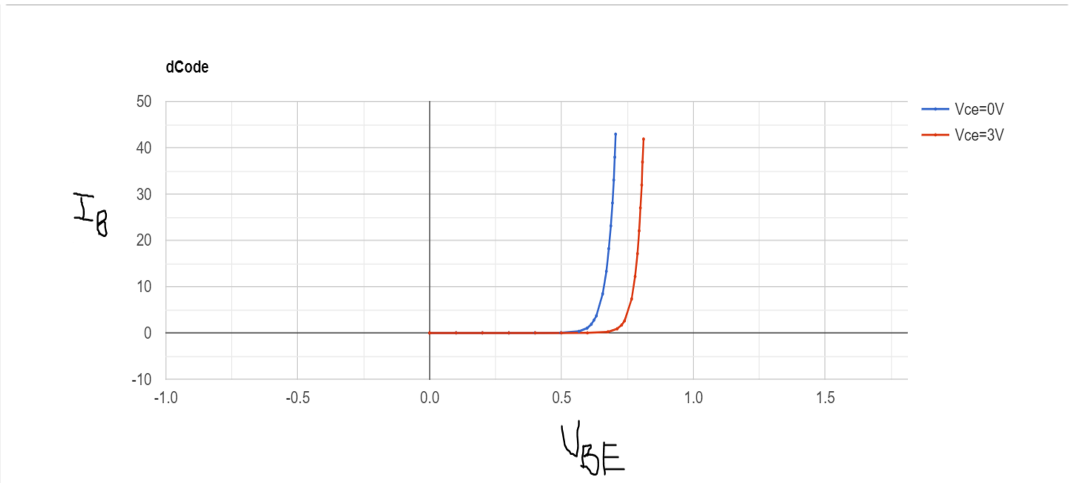
CIRCUIT DIAGRAM (FROM MULTISIM)



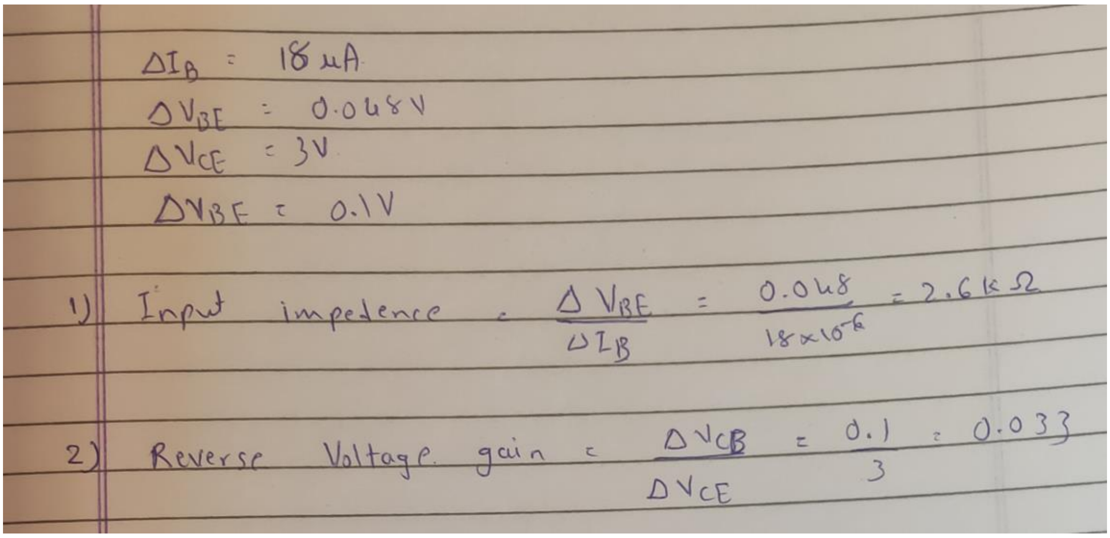
OBSERVATION TABLE

V_{BB}	$V_{CE} = 0V$		$V_{CE} = 3V$	
	V_{BE} (IN VOLTS)	I_B (IN µA)	V_{BE} (IN VOLTS)	I_B (IN µA)
0	0	0	0	0
0.1	0.1	0	0.1	0
0.2	0.2	0	0.2	0
0.3	0.3	0	0.3	0
0.4	0.399	0	0.4	0
0.5	0.497	0.022	0.499	0
0.6	0.566	0.330	0.598	0.011
0.7	0.597	1.029	0.676	0.231
0.8	0.613	1.8684	0.711	0.885
0.9	0.623	2.760	0.728	1.714
1	0.632	3.678	0.739	2.605
1.5	0.656	8.4352	0.766	7.338
2	0.670	13.297	0.779	12.206
2.5	0.679	18.200	0.788	17.119
3	0.687	23.127	0.794	22.053
3.5	0.693	28.069	0.799	27.001
4	0.698	33.020	0.804	31.957
4.5	0.702	37.978	0.807	36.920
5	0.705	42.942	0.811	41.887

GRAPH



CALCULATIONS



$\Delta I_B = 18 \mu A$
$\Delta V_{BE} = 0.048 V$
$\Delta V_{CE} = 3V$
$\Delta V_{BE} = 0.1V$

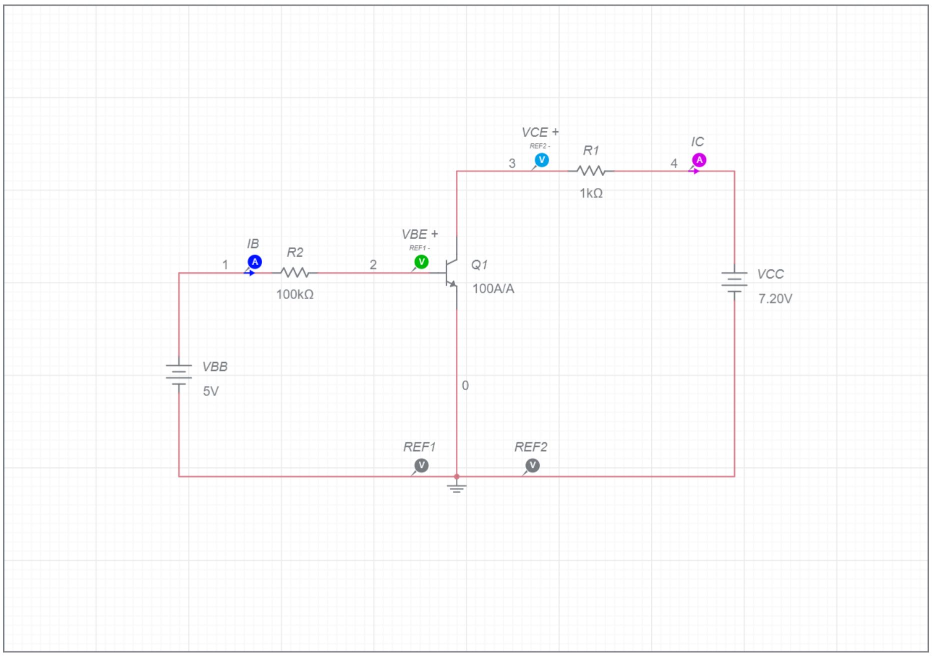
1) Input impedence $= \frac{\Delta V_{BE}}{\Delta I_B} = \frac{0.048}{18 \times 10^{-6}} = 2.6 k\Omega$

2) Reverse Voltage gain $= \frac{\Delta V_{CB}}{\Delta V_{CE}} = \frac{0.1}{3} = 0.033$

Input impedance = hie = Ri = ΔVBE / Δ IB (VCE = constant) =<u>2.6kΩ</u>.
Reverse voltage gain = hre = Δ VEB / Δ VCE (IB = constant) =<u>0.033</u>.

OUTPUT CHARACTERISTICS

CIRCUIT DIAGRAM (FROM MULTISIM)

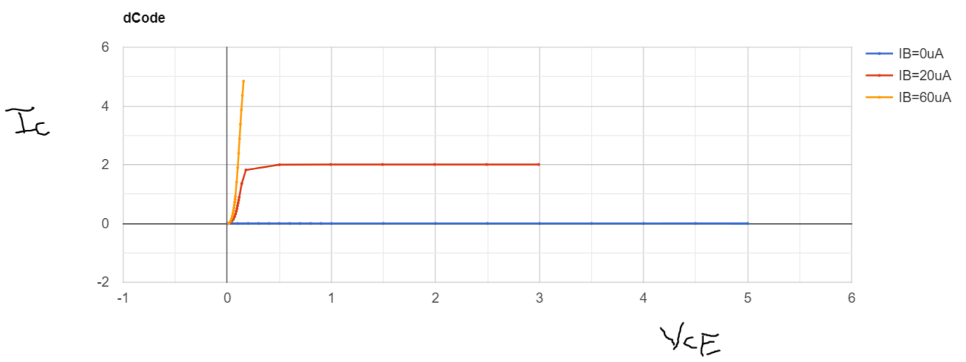


OBSERVATION TABLE

V_{CC}	I_B =0 μA		I_B =20 μA		I_B =60 μA	
	V_{CE} (IN VOLTS)	I_C (IN MA)	V_{CE} (IN VOLTS)	I_C (IN MA)	V_{CE} (IN VOLTS)	I_C (IN MA)
0	0	0	0.010	0	0.014	0
0.1	0.1	0	0.041	0.0586	0.030	0.069
0.2	0.2	0	0.0586	0.141	0.0404	0.159
0.3	0.3	0	0.070	0.229	0.048	0.251
0.4	0.4	0	0.079	0.320	0.054	0.345
0.5	0.5	0	0.086	0.413	0.059	0.440
0.6	0.6	0	0.093	0.506	0.064	0.535
0.7	0.7	0	0.098	0.601	0.068	0.631

0.8	0.8	0	0.104	0.695	0.071	0.728
0.9	0.9	0	0.109	0.790	0.075	0.824
1	1	0	0.114	0.885	0.078	0.921
1.5	1.5	0	0.139	1.360	0.090	1.409
2	2	0	0.179	1.820	0.100	1.899
2.5	2.5	0	0.502	1.997	0.109	2.390
3	3	0	0.992	2.007	0.118	2.881
3.5	3.5	0	1.492	2.007	0.126	3.373
4	4	0	1.992	2.007	0.135	3.864
4.5	4.5	0	2.492	2.007	0.145	4.355
5	5	0	2.992	2.007	0.156	4.843

GRAPH



CALCULATIONS

$\Delta I_C = 2\times10^{-3}$ A

$\Delta I_B = 40\times10^{-6}$ A

$\Delta I_C = 4\times10^{-3}$ A

$\Delta V_{CE} = 1$V

1) Output admittance $= \dfrac{\Delta I_C}{\Delta V_{CE}} = \dfrac{2\times10^{-3}}{1} = 2$m℧

2) forward current gain $= \dfrac{\Delta I_C}{\Delta I_B} = \dfrac{4\times10^{-3}}{40\times10^{-6}} = 100$

Output admittance 1/hoe = Ro = Δ IC / Δ VCE (IB is constant) =2m℧
Forward current gain = hfe = Δ IC / Δ IB (VCE = constant) = 100

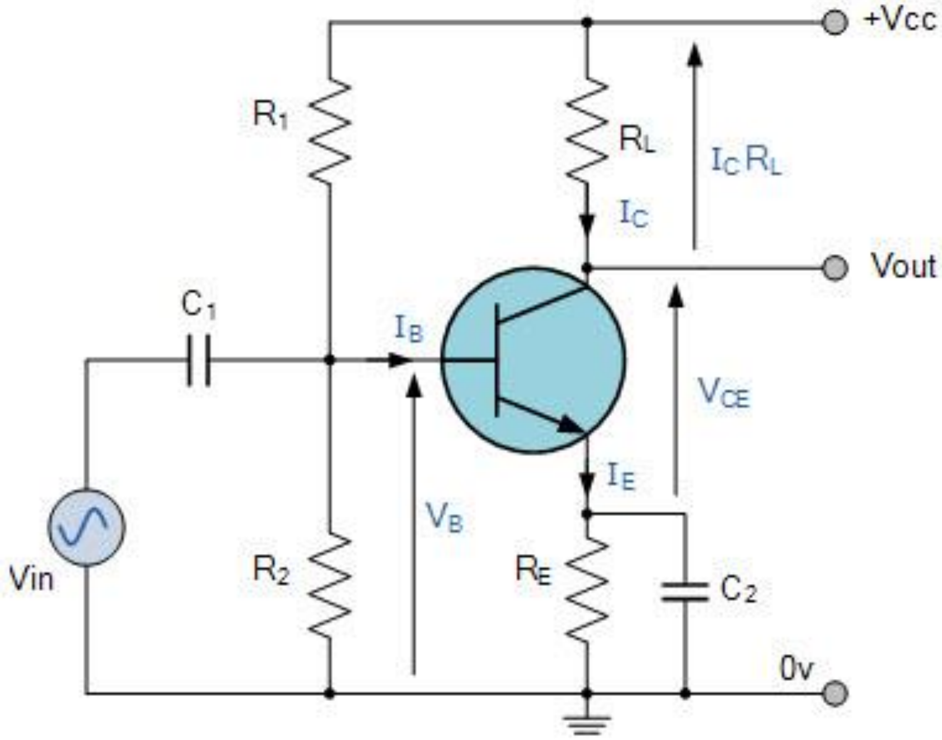
PART – B

COMMON EMITTER AMPLIFIER

All types of transistor amplifiers operate using AC signal inputs which alternate between a positive value and a negative value so some way of "presetting" the amplifier circuit to operate between these two maximum or peak values is required. This is achieved using a process known as Biasing. Biasing is very important in amplifier design as it establishes the correct operating point of the transistor amplifier ready to receive signals, thereby reducing any distortion to the output signal.

The aim of any small signal amplifier is to amplify all of the input signal with the minimum amount of distortion possible to the output signal, in other words, the output signal must be an exact reproduction of the input signal but only bigger (amplified).

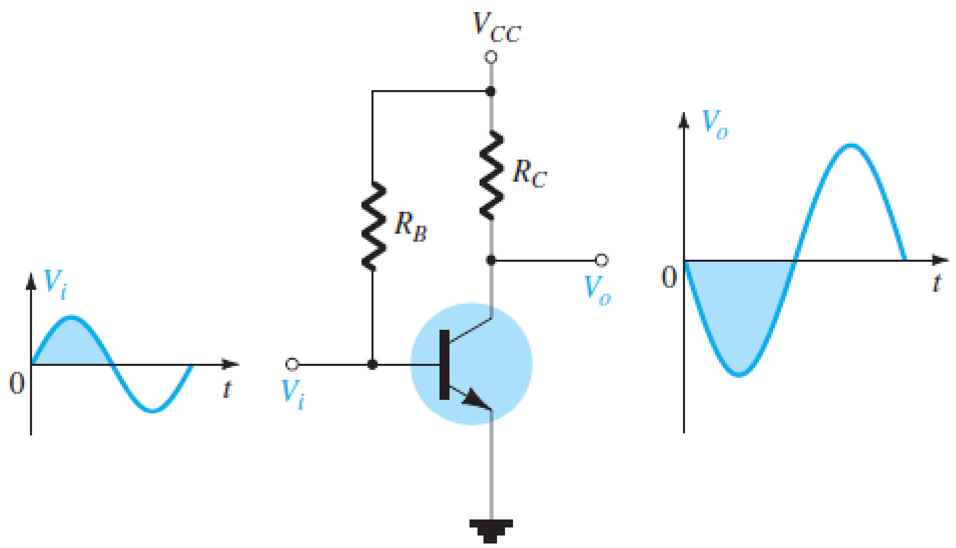
To obtain low distortion when used as an amplifier the operating quiescent point needs to be correctly selected. This is in fact the DC operating point of the amplifier and its position may be established at any point along the load line by a suitable biasing arrangement. The best possible position for this Q-point is as close to the center position of the load line.



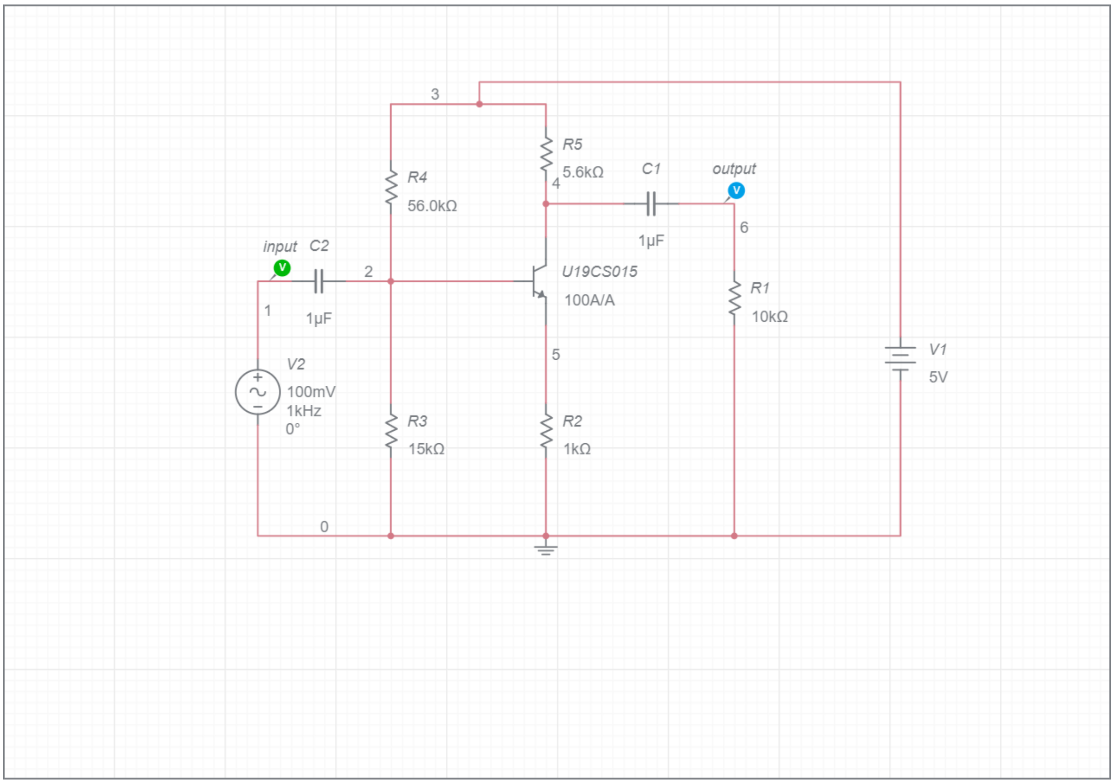
Common Emitter Amplifier Circuit

180 DEGREE PHASE SHIFT

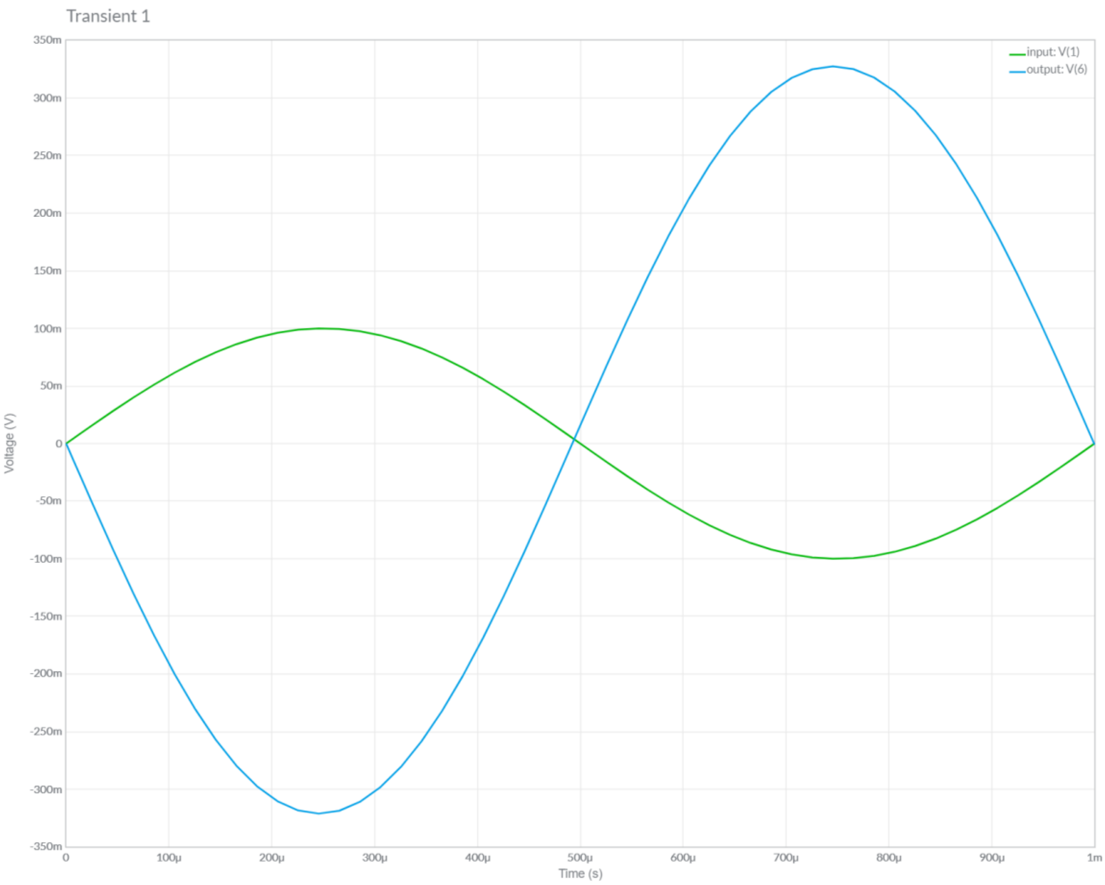
In CE amplifier configuration, there will always a phase-shift of 180 degrees between the input and output as described in figure below.



CIRCUIT DIAGRAM FROM MULTISIM



INPUT – OUTPUT WAVEFORMS



CONCLUSIONS

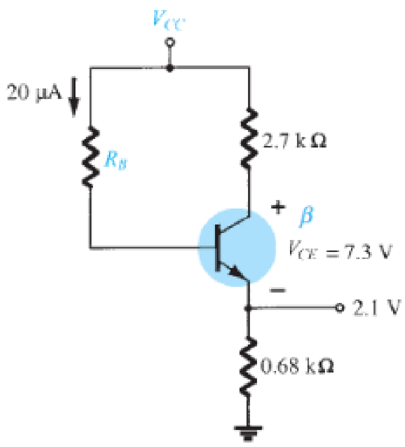
Successfully implemented BJT in Common emitter configuration on multisim and plotted input-output characteristics and also implemented common emitter amplifier and observe its input-output waveform.

DELD Assignment for Practical-10

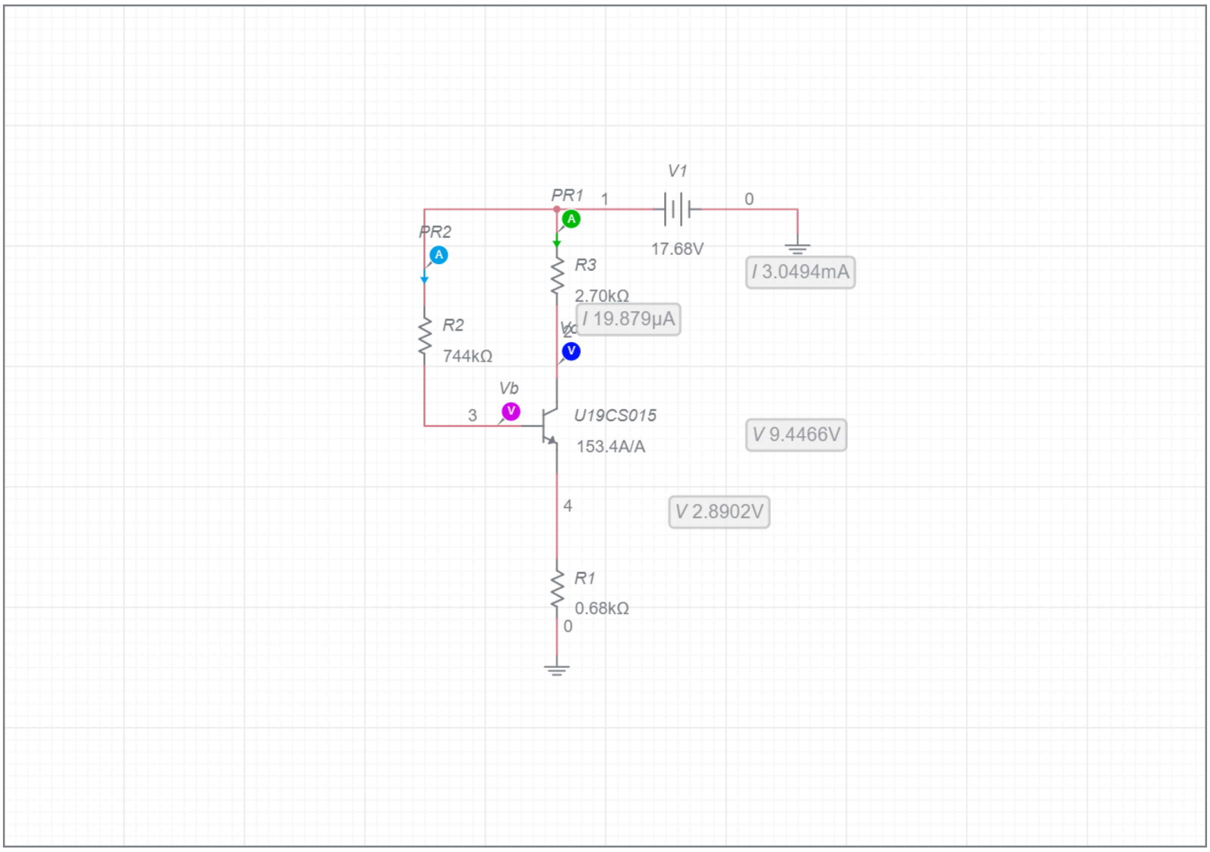
Name: Dhruv Gandhi

ADM No.: U19CS015

1. Using the information provided in the figure below, determine the values of Beta, Vcc and Rb theoritically. Also compute and verify the values of Ic, Vb, and Vc by implementing the circuit on Multisim.



Schematic:



Vb = 2.8902V

Vc = 9.4466V

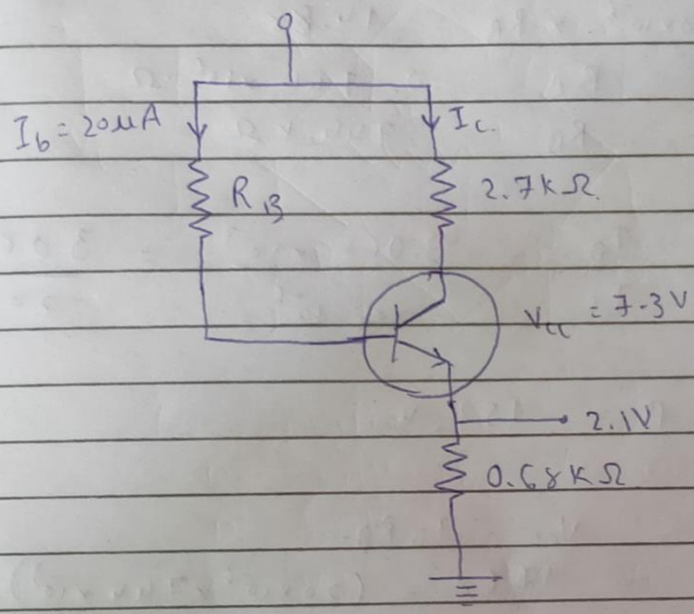
Ic = 3.0494mA

Calculation:

Assignment - 10

U19CS015

1)



$$I_E = \frac{2.1 - 0}{0.68 \times 10^3} = 3.088\ mA$$

Now, $I_E = I_B + I_C$

$3.088 = 0.02 + I_C$

$I_C = 3.068\ mA$

Applying KVL

1) $V_{CC} - I_C R_C - V_{CE} = 2.1$

$V_{CC} = 9.4 + (3.068 \times 2.7)$

$= 17.68\ V$

2) $V_{CC} - I_B R_B - V_{BE} = 2.1V$

$17.68 - 20\times10^{-6} \times R_B - 0.7 = 2.1$

$20\times10^{-6} \times R_B = 14.88$

$R_B = 0.744 \times 10^{6}\ \Omega.$

$R_B = 744\ k\Omega.$

$\beta = \frac{I_B}{I_C} = \frac{3.068 \times 10^{-3}}{20\times 10^{-6}} = \frac{3068}{20}$

$\beta = 153.4$

$V_B = V_{CC} - I_B R_B$

$= 17.68 - (20\times10^{-6} \times 744 \times 10^{3})$

$= 17.68 - 14.83$

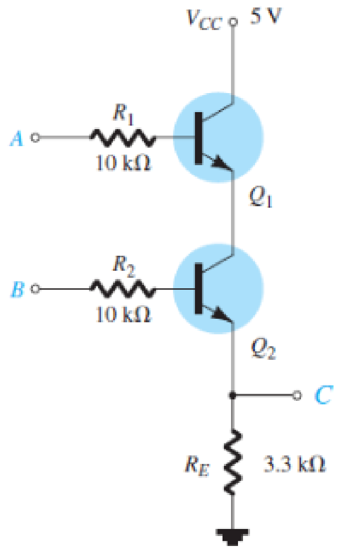
$V_B = 2.9V$

$V_C = V_{CC} - I_C R_C.$

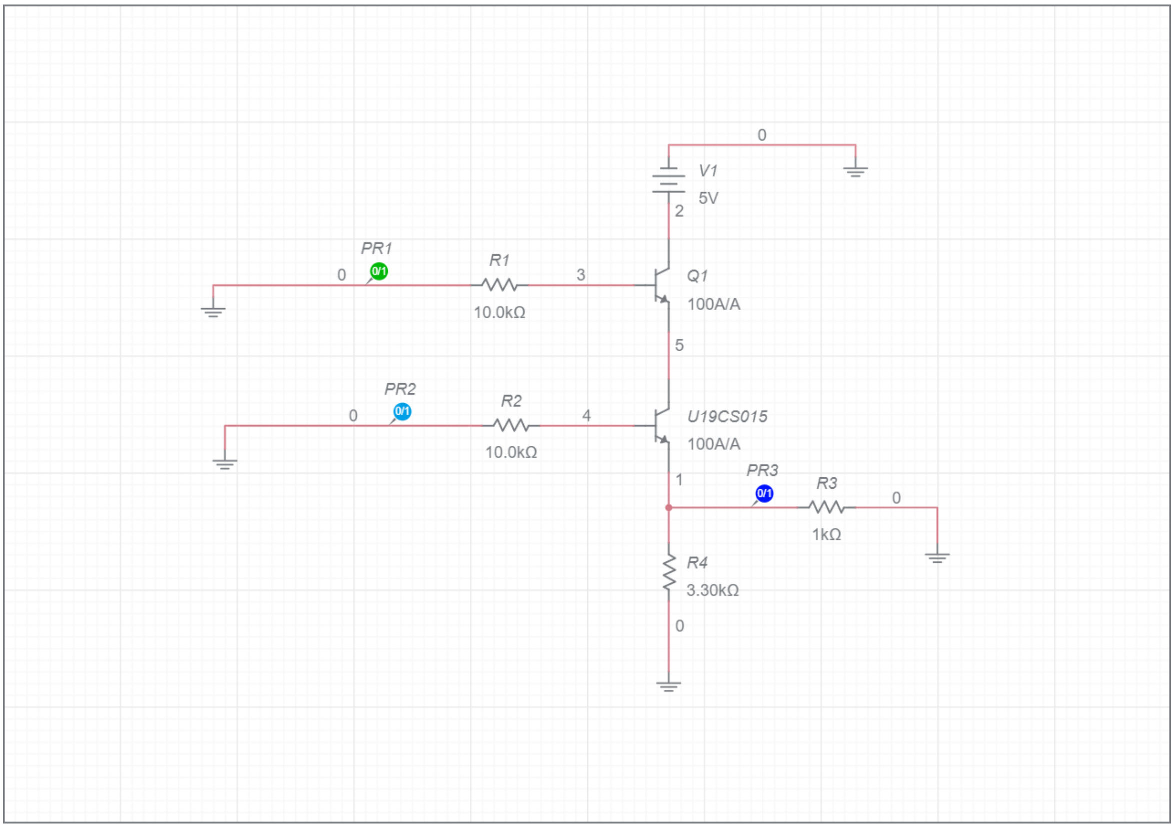
$= 17.68 - 8.28$

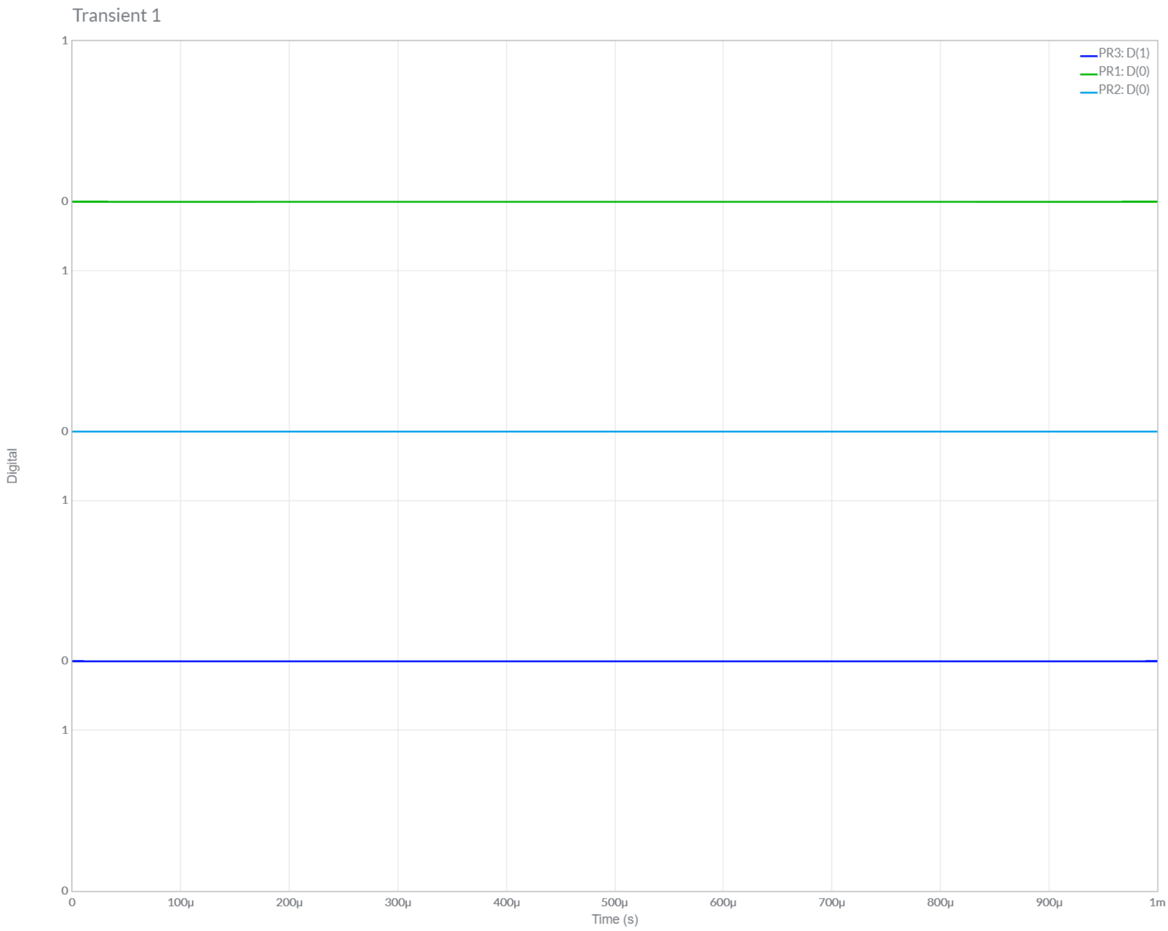
$V_C = 9.4V$

2. Simulate the below given circuit on Multisim and predict the type of Digital Logic implemented by the same. Use the default transistor available in Multisim. Attach all the four screenshots (00,05,50,55).

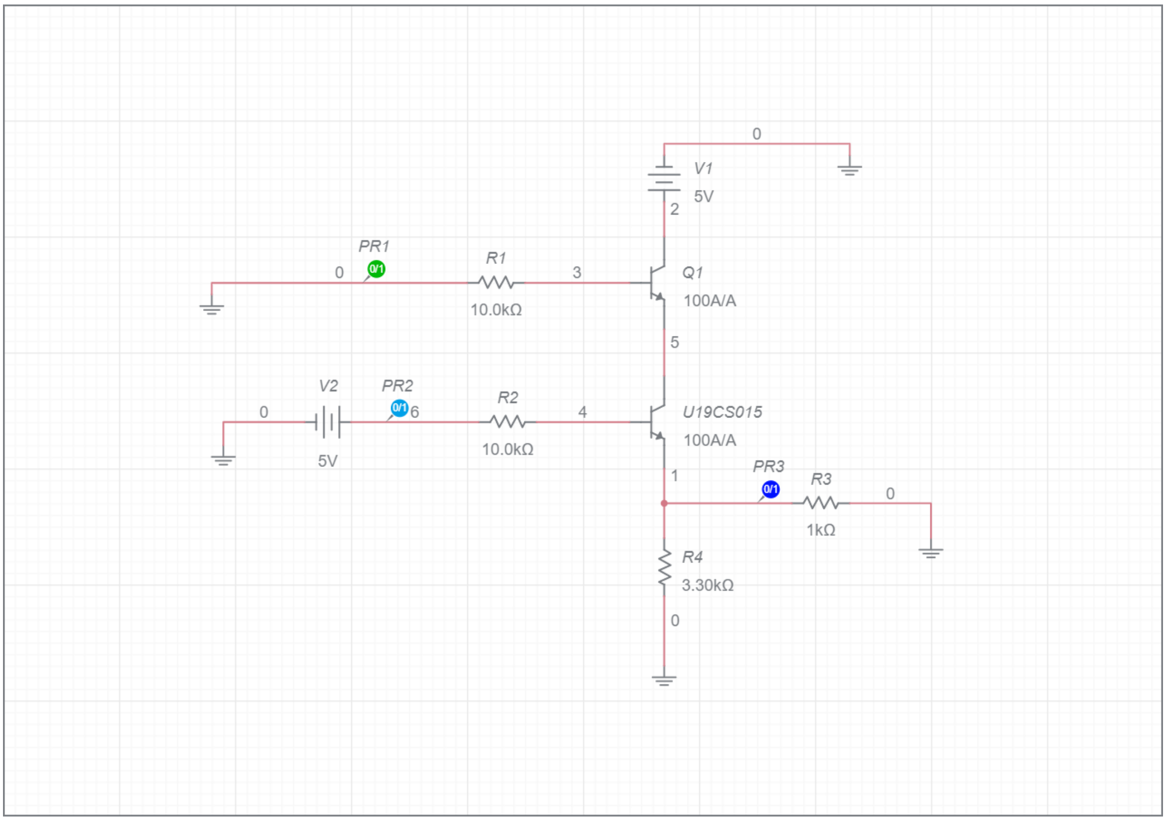


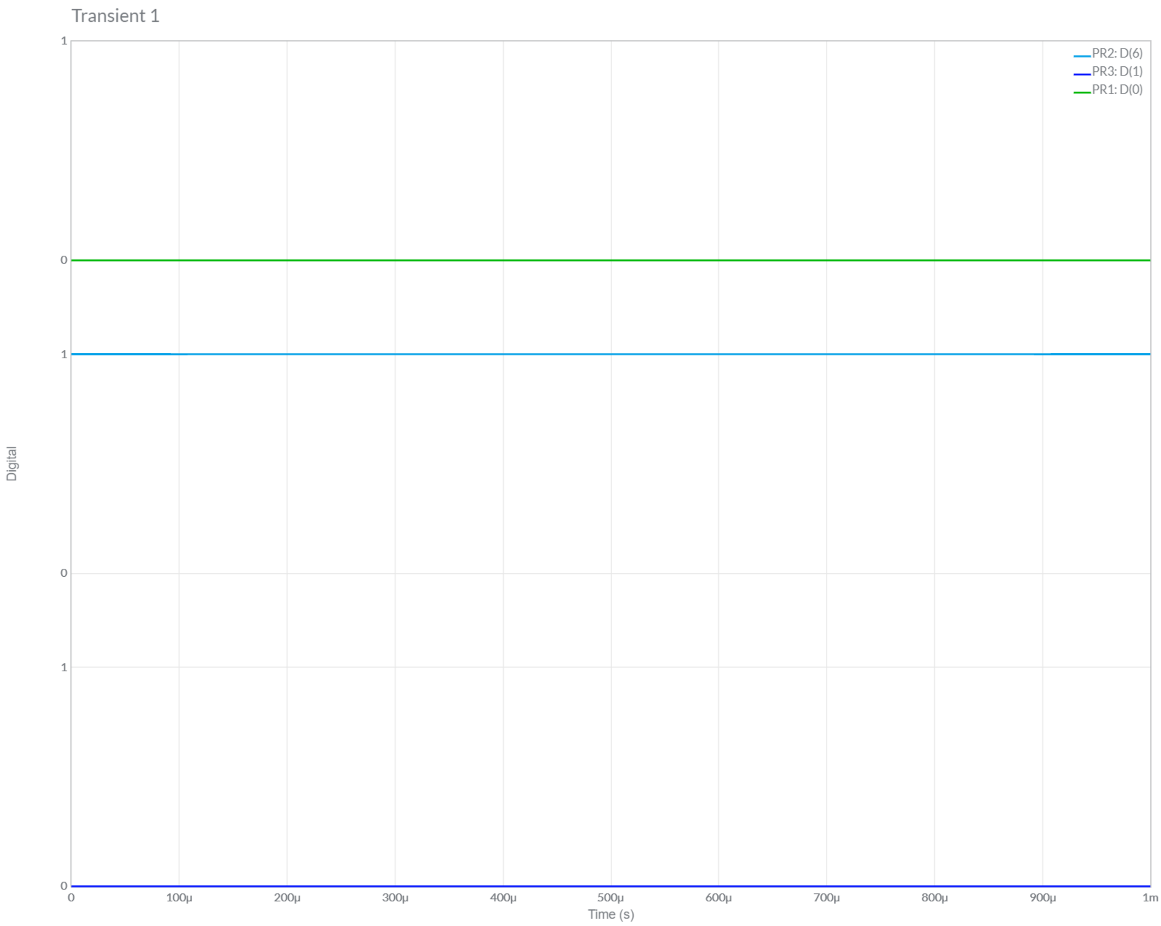
Circuit 1:


V1
5V
Q1
100A/A
U19CS015
100A/A
PR1
PR2
PR3
R1
10.0kΩ
R2
10.0kΩ
R3
1kΩ
R4
3.30kΩ
0
1
2
3
4
5

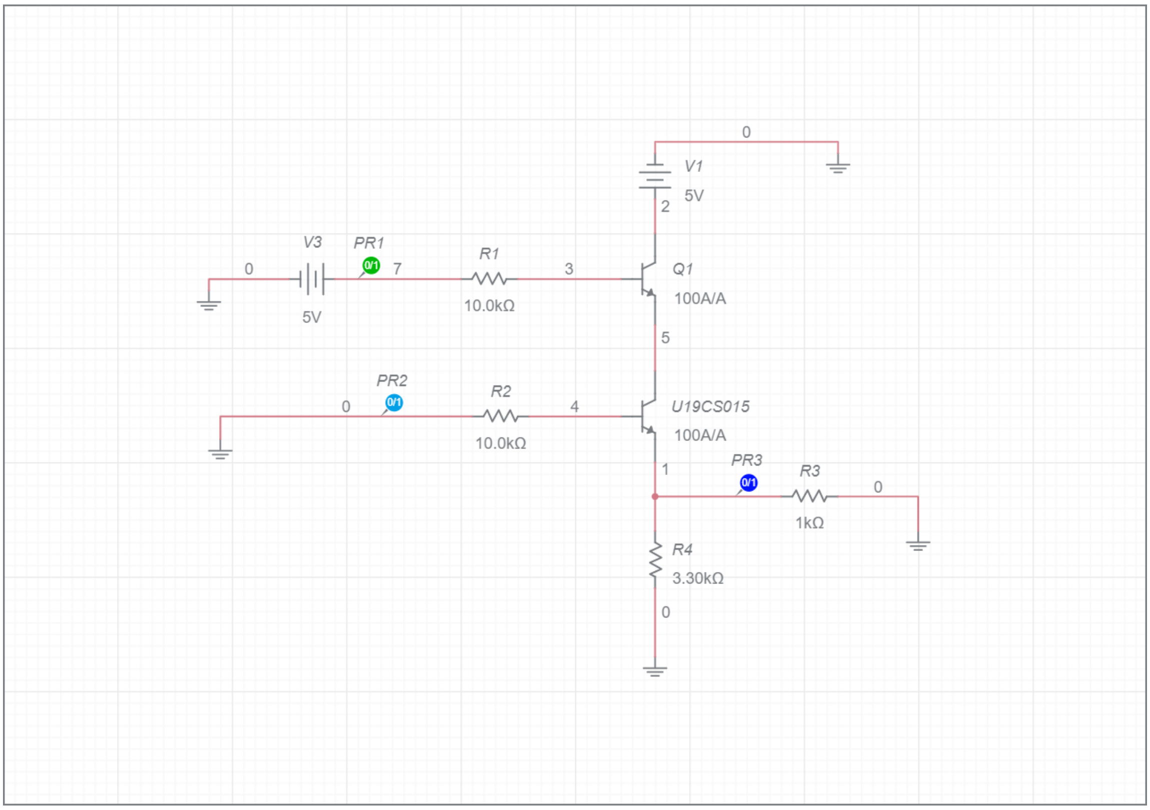

Transient 1
PR3: D(1)
PR1: D(0)
PR2: D(0)
Digital
Time (s)
0
100µ
200µ
300µ
400µ
500µ
600µ
700µ
800µ
900µ
1m

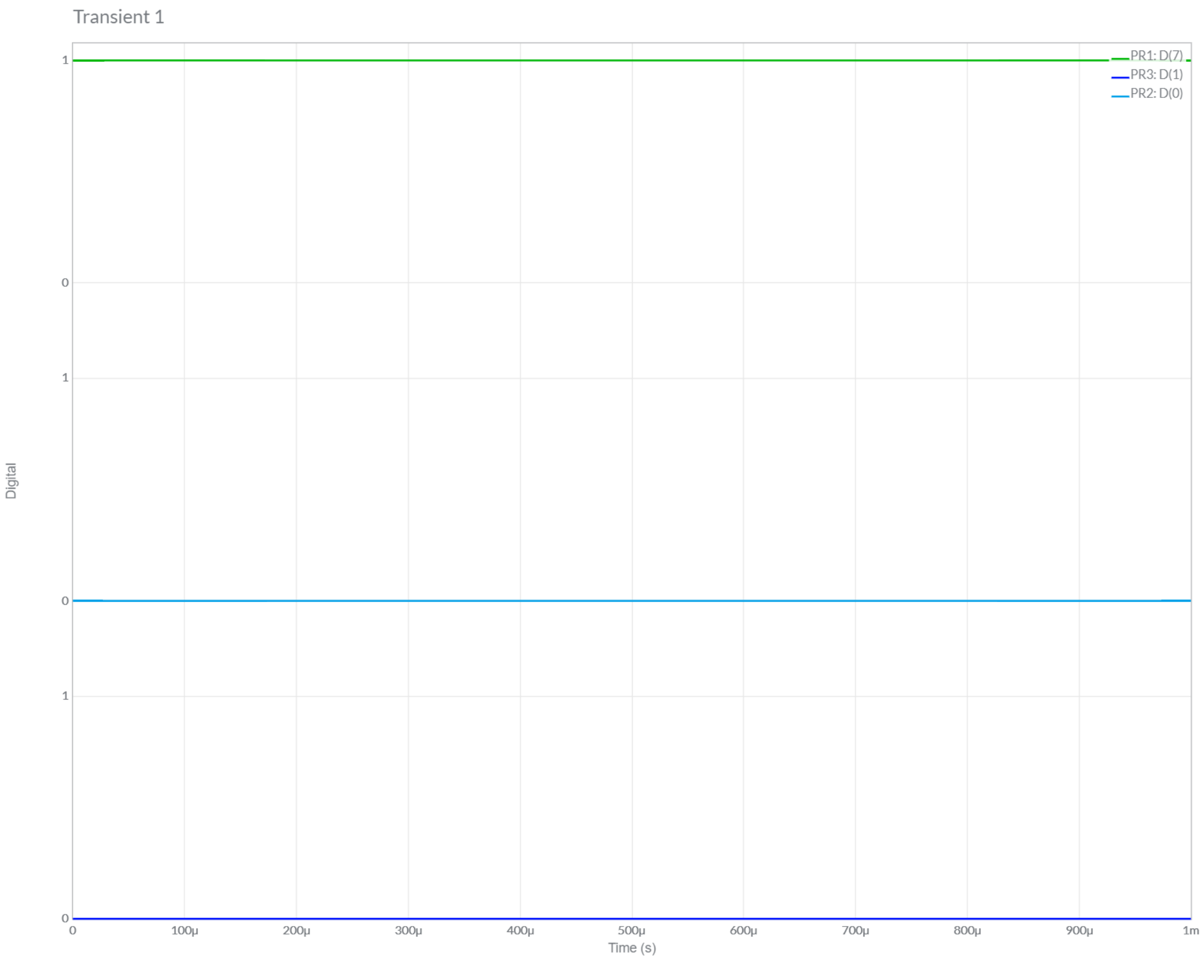
Circuit 2:


0
V1
5V
2
PR1
R1
0
3
Q1
100A/A
10.0kΩ
5
V2
PR2
R2
0
6
4
U19CS015
100A/A
5V
10.0kΩ
PR3
R3
1
0
1kΩ
R4
3.30kΩ
0

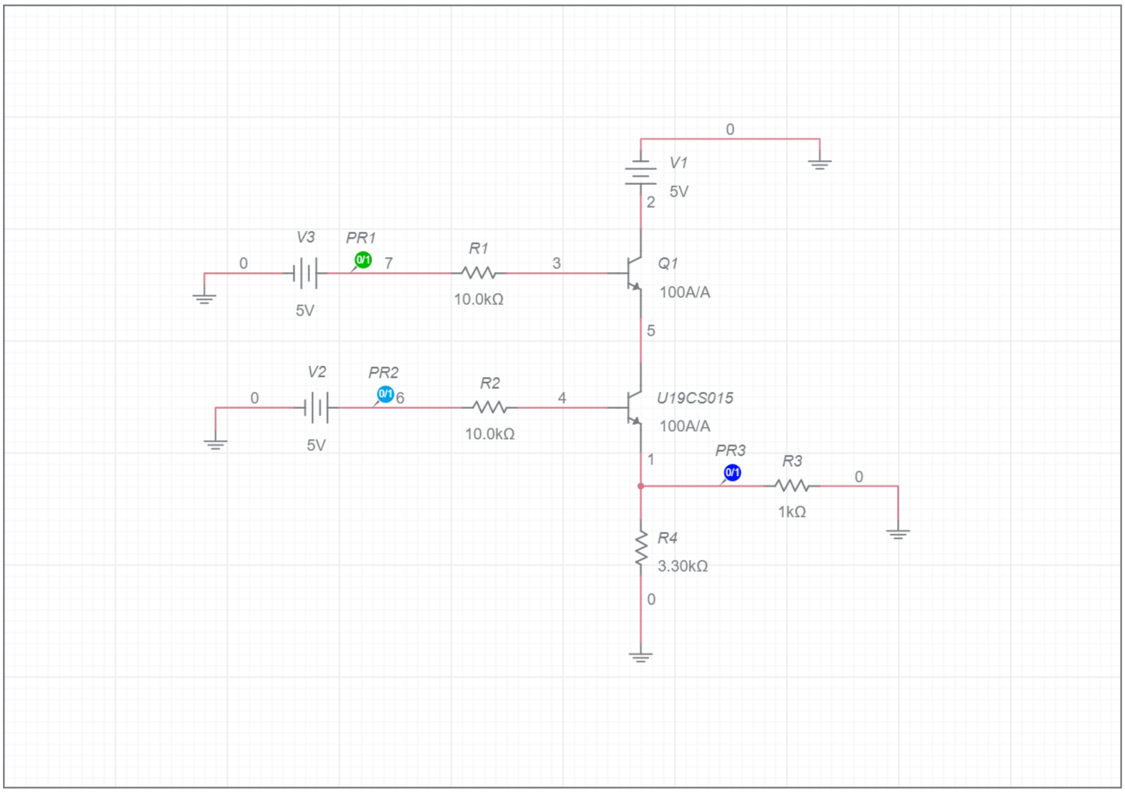

Transient 1
PR2: D(6)
PR3: D(1)
PR1: D(0)
Digital
1
0
1
0
1
0
0
100μ
200μ
300μ
400μ
500μ
600μ
700μ
800μ
900μ
1m
Time (s)

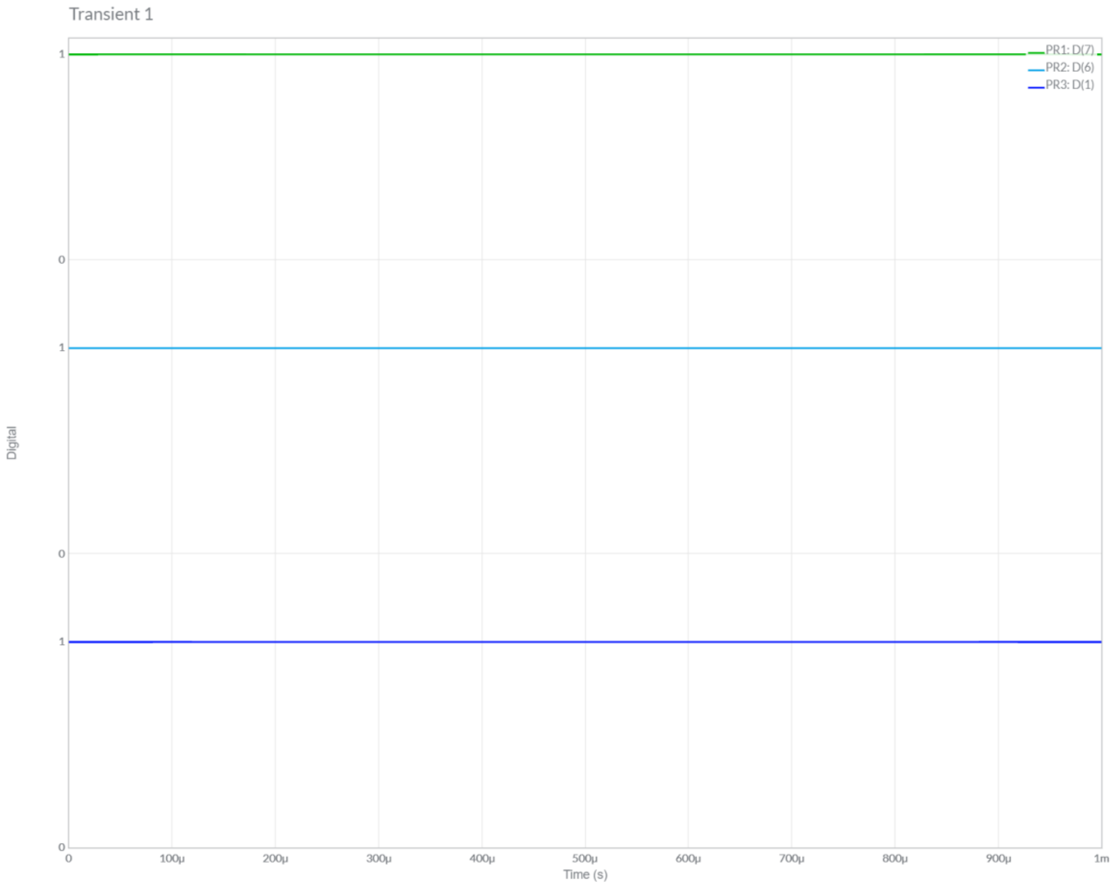
Circuit 3:


0
V1
5V
2
V3
PR1
0
7
R1
3
Q1
10.0kΩ
100A/A
5V
5
PR2
R2
0
4
U19CS015
10.0kΩ
100A/A
1
PR3
R3
0
1kΩ
R4
3.30kΩ
0


Transient 1
PR1: D(7)
PR3: D(1)
PR2: D(0)
Digital
1
0
1
0
1
0
0
100μ
200μ
300μ
400μ
500μ
600μ
700μ
800μ
900μ
1m
Time (s)

Circuit 4:





By looking at graphs, the given circuit represents an AND GATE.