SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY, SURAT
ELECTRONICS ENGINEERING DEPARTMENT

Expt. No:	10	Common Emitter Characteristics & Common Emmiter Amplifier
Date:	29-10-2020	

AIM: To study, the Input-Output characteristics of a BJT in Common Emitter Configuration. Also implement Common Emitter Amplifier.

SOFTWARE TOOLS / OTHER REQUIREMENTS:

1. Multisim Simulator/Circuit Simulator

THEORY:

The most frequently encountered transistor configuration appears in Fig.10.1 for the pnp and npn transistors. It is called the common-emitter configuration because the emitter is common to both the input and output terminals (in this case common to both the base and collector terminals). Two sets of characteristics are again necessary to describe fully the behavior of the common-emitter configuration: one for the input or base–emitter circuit and one for the output or collector–emitter circuit. Both are shown in Fig. 10.2 (a) and 10.2 (b) respectively.

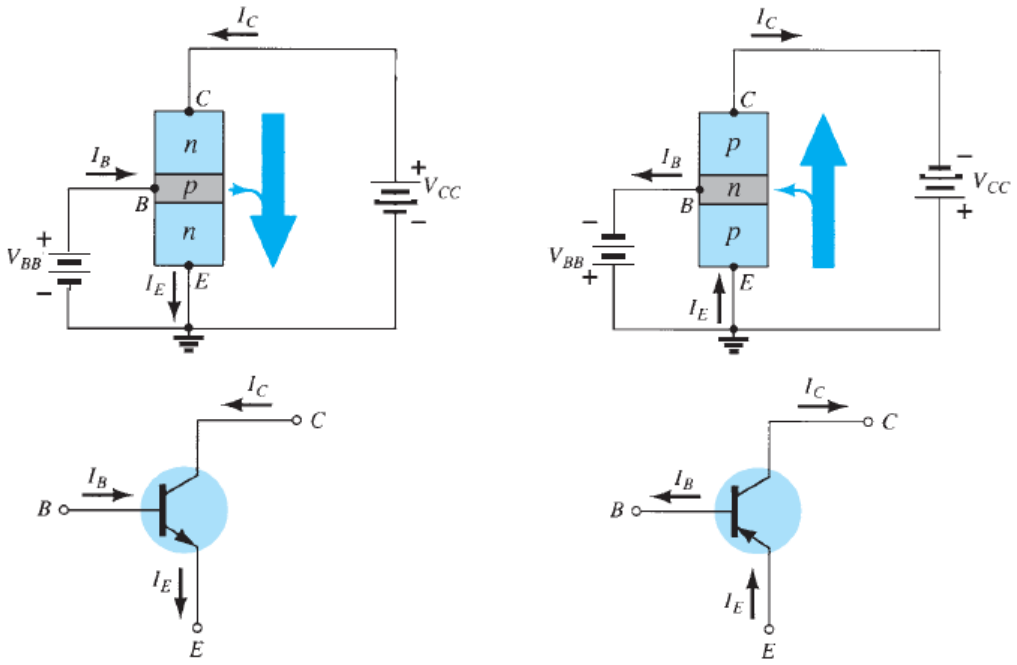


Fig. 10.1

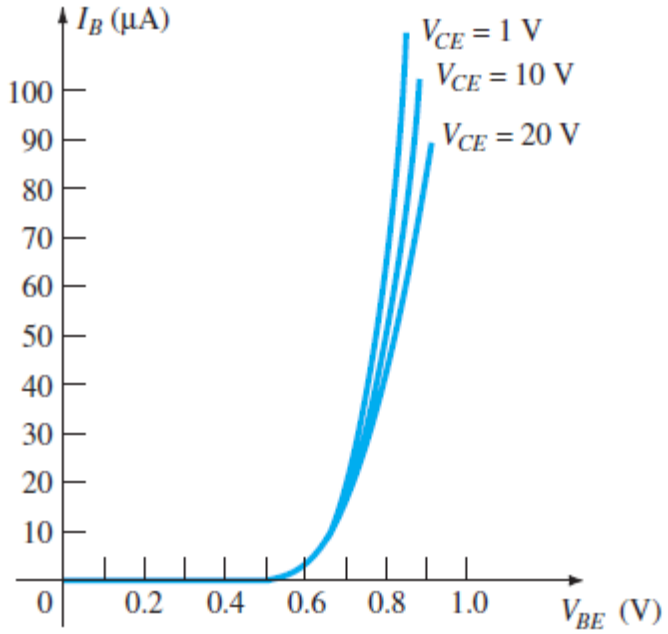


Fig. 10.2 (a) CE Input Characterisitcs

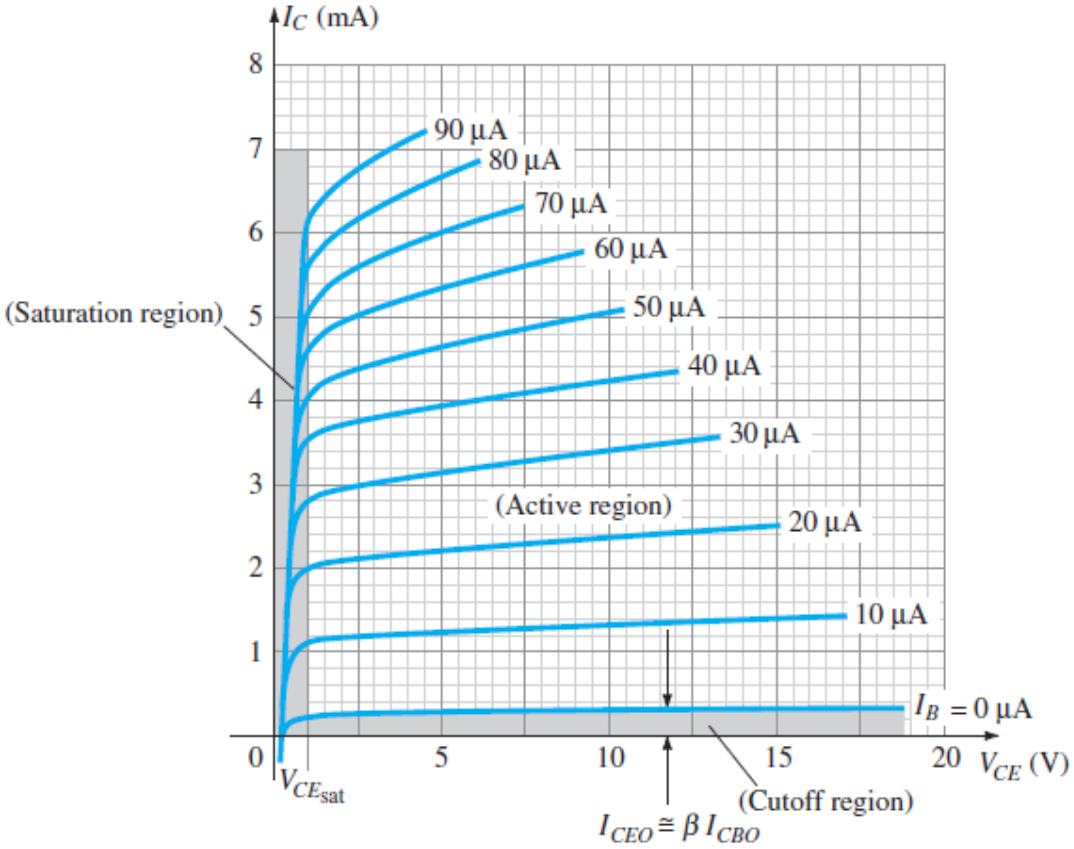


Fig. 10.2 (b) CE Output Characterisitcs

INPUT CHARACTERISTICS

The input characteristics are a plot of the input current (*IB*) versus the input voltage (*VBE*) for a range of values of output voltage (*VCE*). The curve describes the changes in the values of input current with respect to the values of input voltage keeping the output voltage constant.

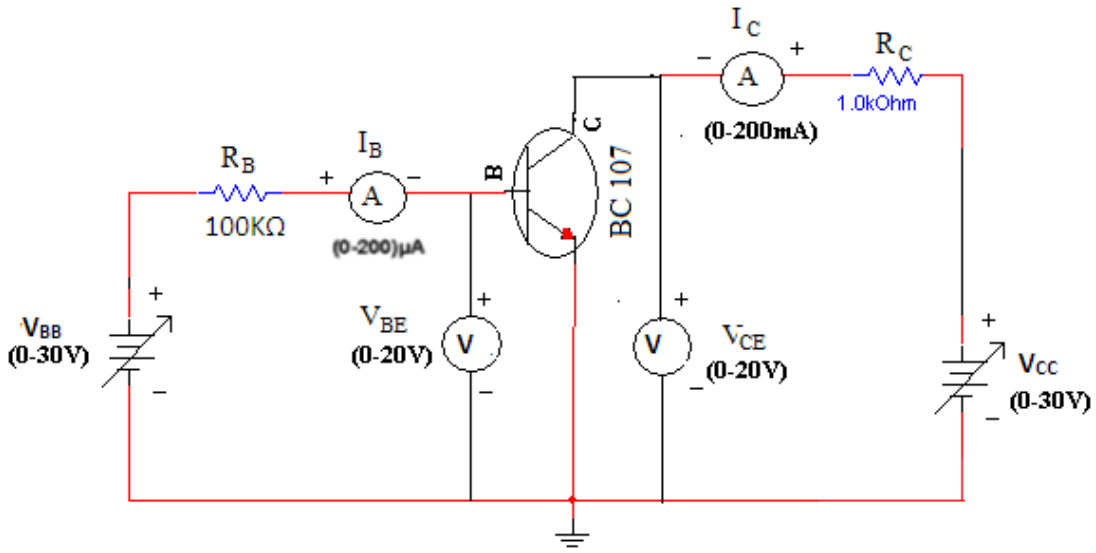


Fig. 10. 3 Circuit Diagram to obtain CE Input/Output Characteristics

PROCEDURE

1. **CONNECT THE CIRCUIT AS SHOWN IN THE CIRCUIT DIAGRAM.**
2. **KEEP OUTPUT VOLTAGE V_{CE} = 0V BY VARYING V_{CC}.**
3. **VARYING V_{BB} GRADUALLY, NOTE DOWN BASE CURRENT I_B AND BASE-EMITTER VOLTAGE V_{BE}.**
4. **STEP SIZE IS NOT FIXED BECAUSE OF NON LINEAR CURVE. INITIALLY VARY V_{BB} IN STEPS OF 0.1V. ONCE THE CURRENT STARTS INCREASING VARY V_{BB} IN STEPS OF 1V UP TO 5V.**
5. **REPEAT ABOVE PROCEDURE (STEP 3) FOR V_{CE} = 3V.**

OUTPUT CHARACTERISTICS

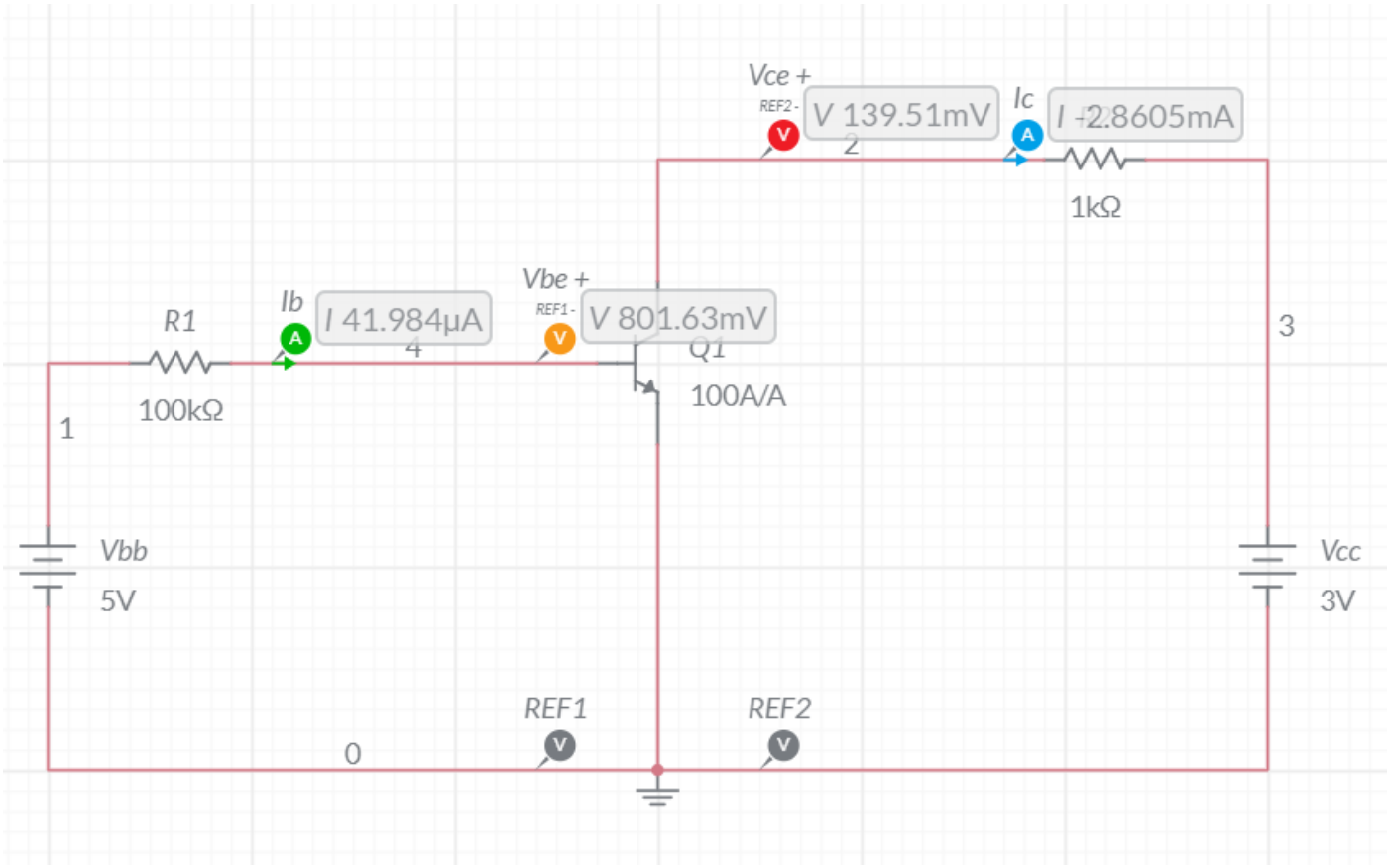
The output characteristics are a plot of the output current (*I C*) versus output voltage (*V CE*) for a range of values of input current (*I B*). The curve describes the changes in the values of output current against output voltage keeping the input current constant.

PROCEDURE

1. **CONNECT THE CIRCUIT AS SHOWN IN THE CIRCUIT DIAGRAM.**
2. **KEEP EMITTER CURRENT I_B = 0µA BY VARYING V_{BB}.**
3. **VARYING V_{CC} GRADUALLY IN STEPS OF 1V UP TO 5V AND NOTE DOWN COLLECTOR CURRENT I_C AND COLLECTOR-EMITTER VOLTAGE(V_{CE}).**
4. **REPEAT ABOVE PROCEDURE (STEP 3) FOR I_B = 20µA AND 60µA.**

INPUT CHARACTERISTICS

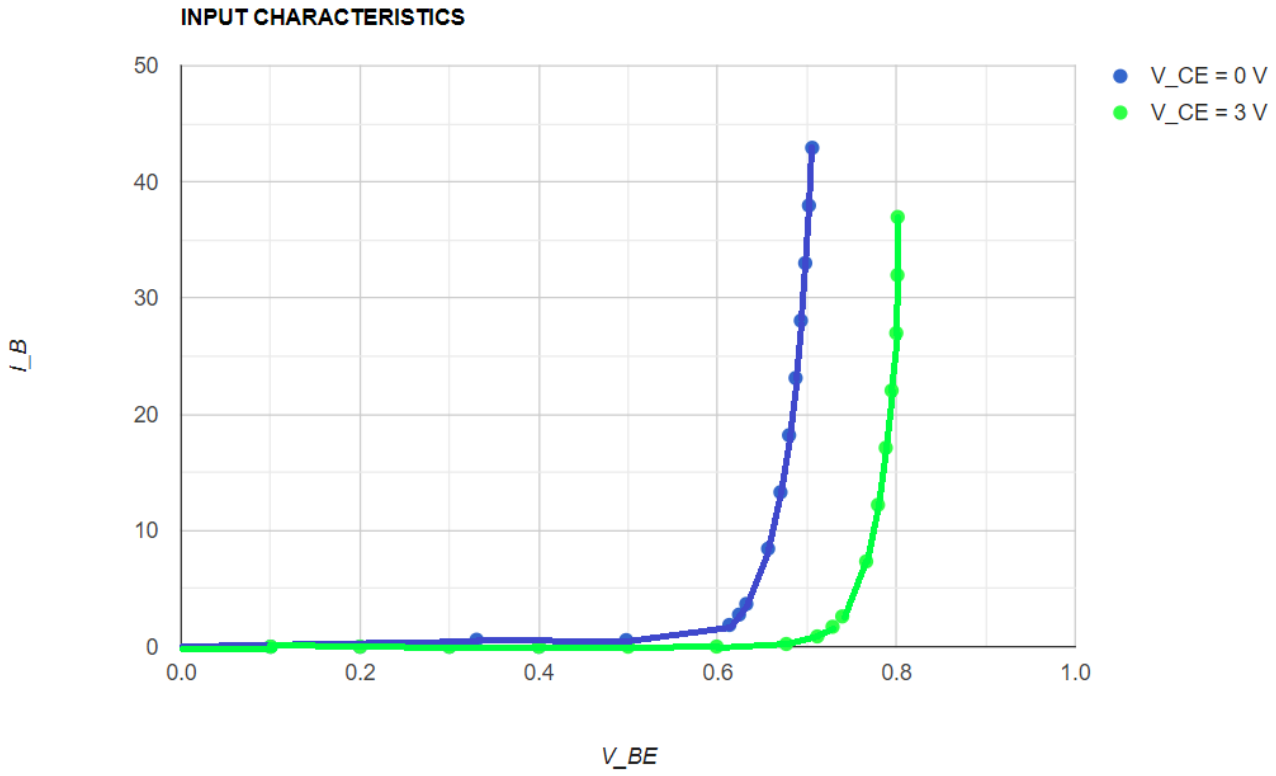
CIRCUIT DIAGRAM (FROM MULTISIM)



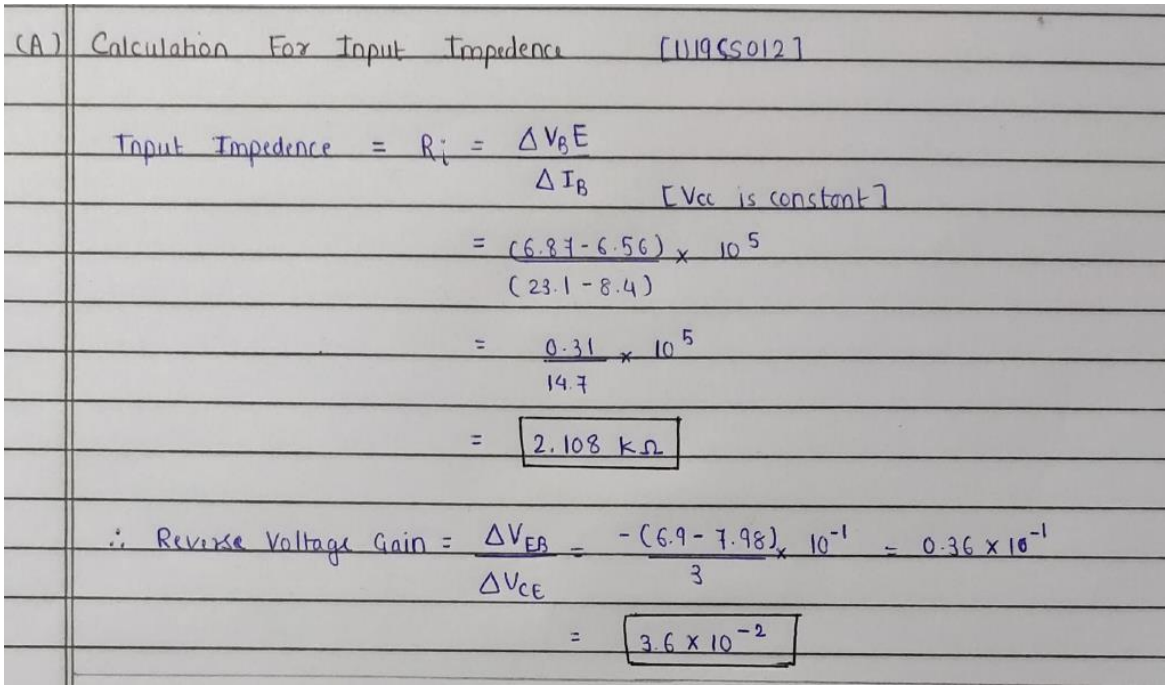
OBSERVATION TABLE

V_{BB}	V_{CE} = 0V		V_{CE} = 3V	
	V_{BE} (IN VOLTS)	I_B (IN µA)	V_{BE} (IN VOLTS)	I_B (IN µA)
0	0	0	0	0
0.1	0.1	0	0.1	0
0.2	0.2	0	0.2	0
0.3	0.3	0	0.3	0
0.4	0.39995	0	0.4	0
0.5	0.49770	0.22965	0.49998	0
0.6	0.56696	0.33038	0.59886	0.011367
0.7	0.597	1.0298	0.67683	0.23169
0.8	0.61316	1.8684	0.71150	0.88505
0.9	0.62398	2.7602	0.72859	1.7141
1	0.63211	3.6789	0.73942	2.6058
1.5	0.65648	8.4352	0.76620	7.3380
2	0.67033	13.297	0.77936	12.206
2.5	0.67995	18.200	0.78811	17.119
3	0.68727	23.127	0.79466	22.053
3.5	0.69314	28.069	0.79988	27.001
4	0.69801	33.020	0.80116	31.988
4.5	0.70218	37.978	0.80144	36.986
5	0.70580	42.942	0.80163	41.984

GRAPH



CALCULATIONS

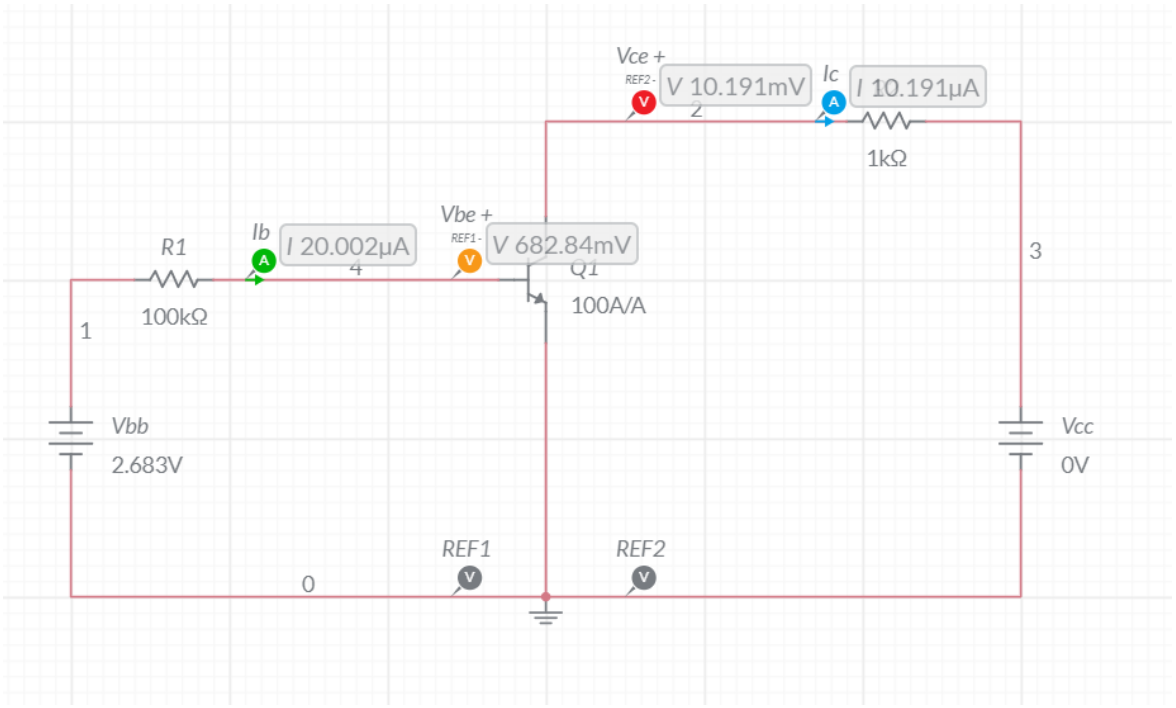


Input impedance = hie = Ri = $\Delta V_{BE} / \Delta I_B$ (V_{CE} = constant) = ***2.108 kΩ***
Reverse voltage gain = hre = $\Delta V_{EB} / \Delta V_{CE}$ (IB = constant) = ***3.6×10^{-2}***

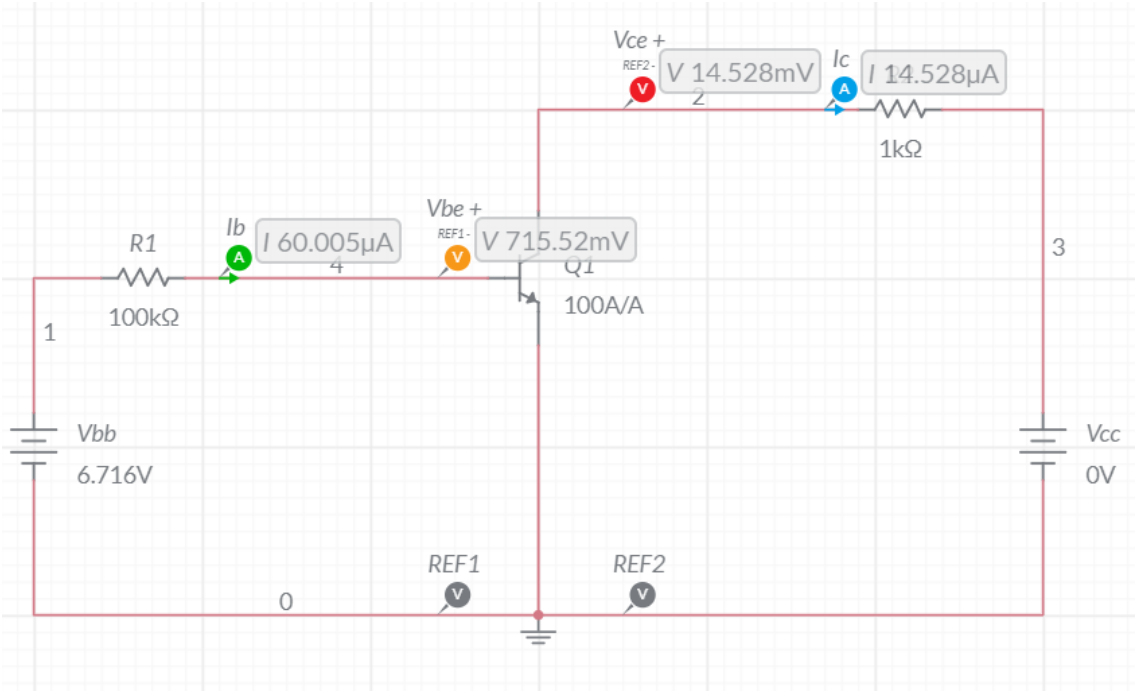
OUTPUT CHARACTERISTICS

CIRCUIT DIAGRAM (FROM MULTISIM)

20 UA



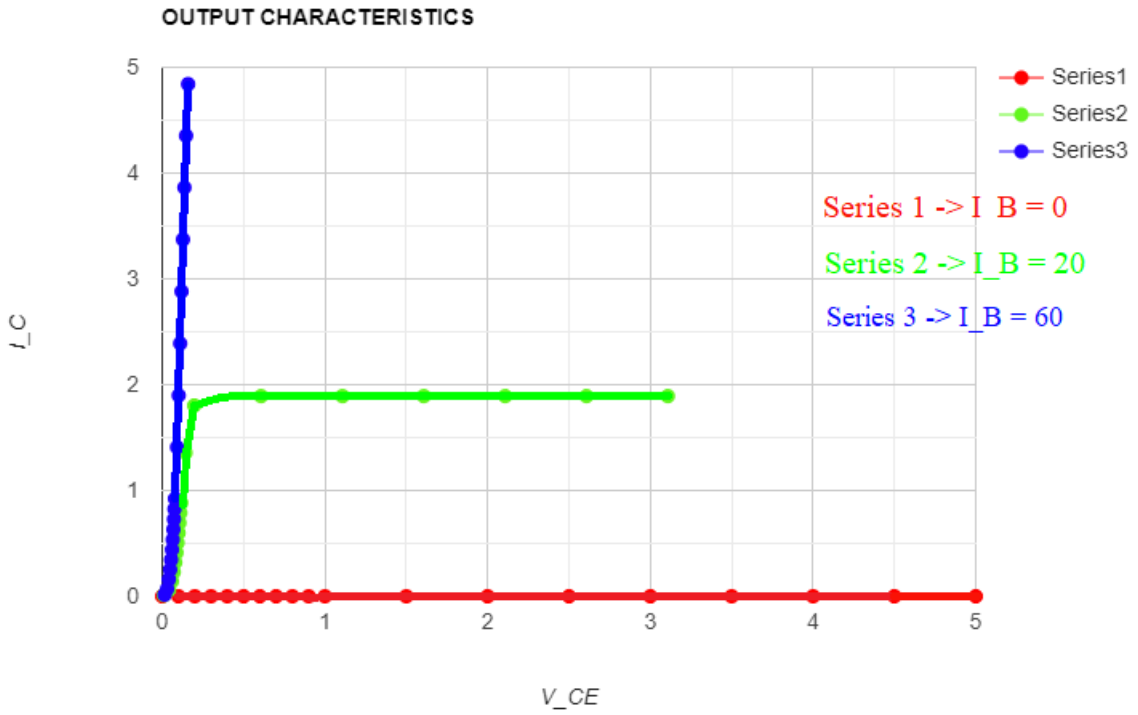
60 UA



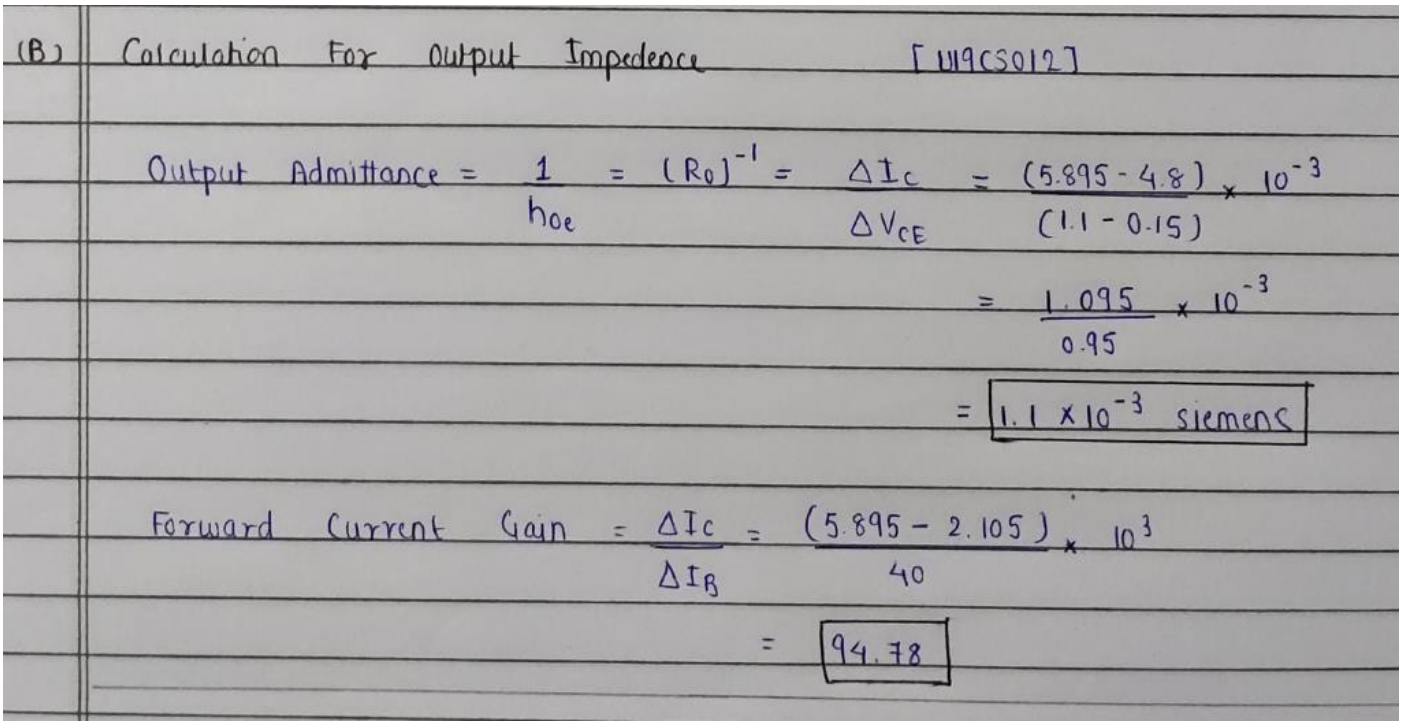
OBSERVATION TABLE

V_{CC}	I_B =0 µA		I_B =20 µA		I_B =60 µA	
	V_{CE} (IN VOLTS)	I_C (IN MA)	V_{CE} (IN VOLTS)	I_C (IN MA)	V_{CE} (IN VOLTS)	I_C (IN MA)
0	0	0	0.0102	0.0102	0.014528	0.014528
0.1	0.1	0	0.0421	0.0579	0.030123	0.069877
0.2	0.2	0	0.05933	0.14067	0.040552	0.15945
0.3	0.3	0	0.07108	0.22891	0.048373	0.25163
0.4	0.4	0	0.08016	0.31983	0.054647	0.34535
0.5	0.5	0	0.08772	0.41228	0.059905	0.4401
0.6	0.6	0	0.09431	0.5057	0.064448	0.53555
0.7	0.7	0	0.1003	0.59971	0.068464	0.63154
0.8	0.8	0	0.10585	0.69415	0.072076	0.72792
0.9	0.9	0	0.11115	0.78885	0.075369	0.82463
1	1	0	0.1163	0.8837	0.078405	0.92159
1.5	1.5	0	0.14345	1.3566	0.091037	1.4090
2	2	0	0.19702	1.8030	0.10124	1.8988
2.5	2.5	0	0.6077	1.8923	0.11028	2.3897
3	3	0	1.1077	1.8923	0.11882	2.8812
3.5	3.5	0	1.6077	1.8923	0.12736	3.3726
4	4	0	2.1077	1.8923	0.13637	3.8636
4.5	4.5	0	2.6077	1.8923	0.14651	4.3535
5	5	0	3.1077	1.8923	0.15902	4.841

GRAPH



CALCULATIONS



Output admittance 1/hoe = $(Ro)^{-1}$ = $\Delta I_C / \Delta V_{CE}$ (IB is constant) = ***1.1 x 10^{-3} ℧***

Forward current gain = hfe = $\Delta I_C / \Delta I_B$ (V_{CE} = constant) = ***94.78***

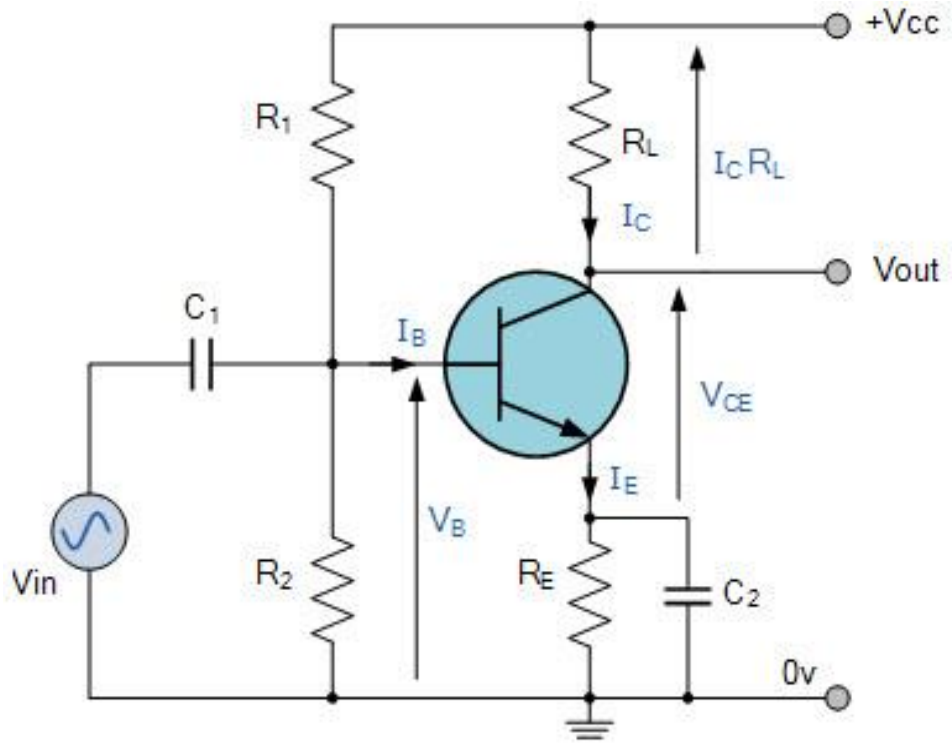
PART – B

COMMON EMITTER AMPLIFIER

All types of transistor amplifiers operate using AC signal inputs which alternate between a positive value and a negative value so some way of "presetting" the amplifier circuit to operate between these two maximum or peak values is required. This is achieved using a process known as Biasing. Biasing is very important in amplifier design as it establishes the correct operating point of the transistor amplifier ready to receive signals, thereby reducing any distortion to the output signal.

The aim of any small signal amplifier is to amplify all of the input signal with the minimum amount of distortion possible to the output signal, in other words, the output signal must be an exact reproduction of the input signal but only bigger (amplified).

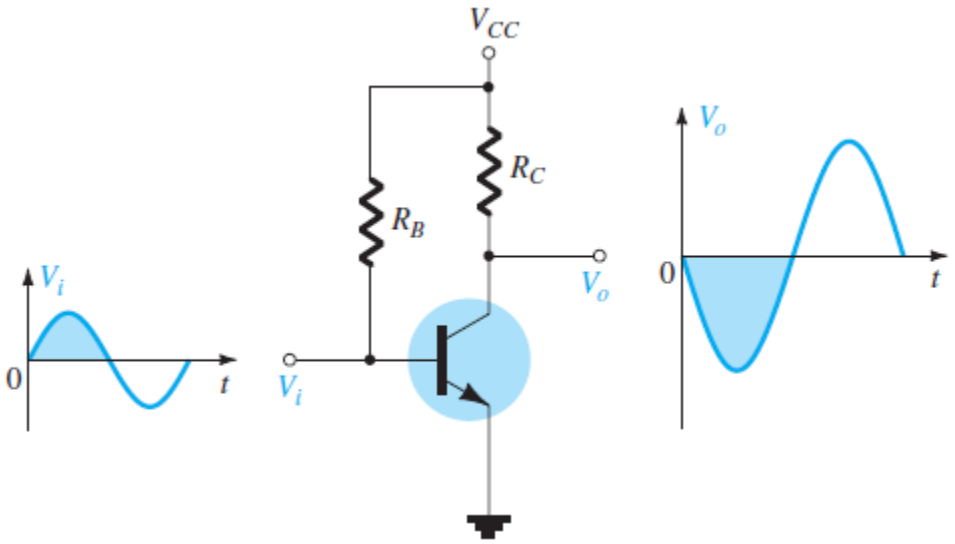
To obtain low distortion when used as an amplifier the operating quiescent point needs to be correctly selected. This is in fact the DC operating point of the amplifier and its position may be established at any point along the load line by a suitable biasing arrangement. The best possible position for this Q-point is as close to the center position of the load line.



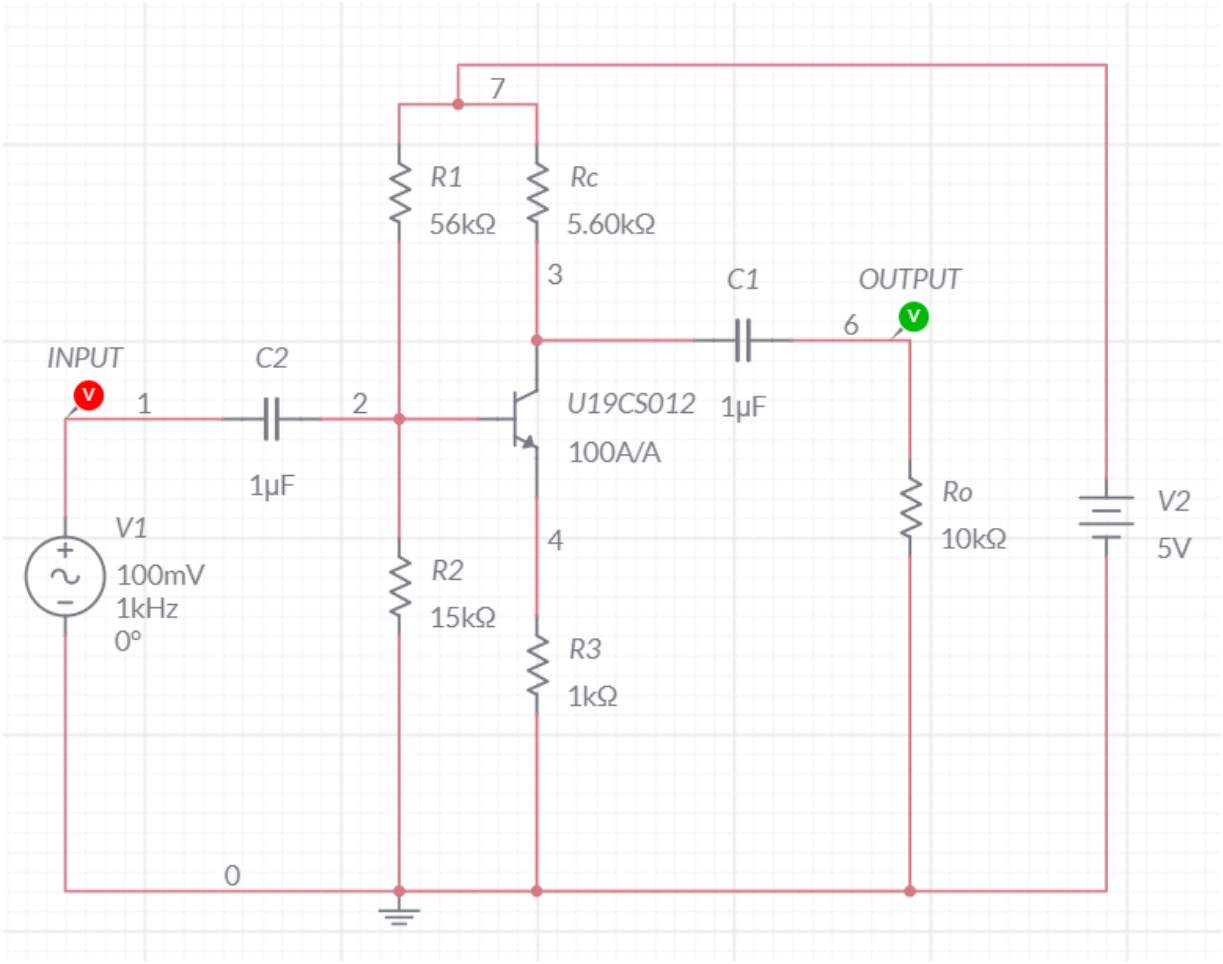
Common Emitter Amplifier Circuit

180 DEGREE PHASE SHIFT

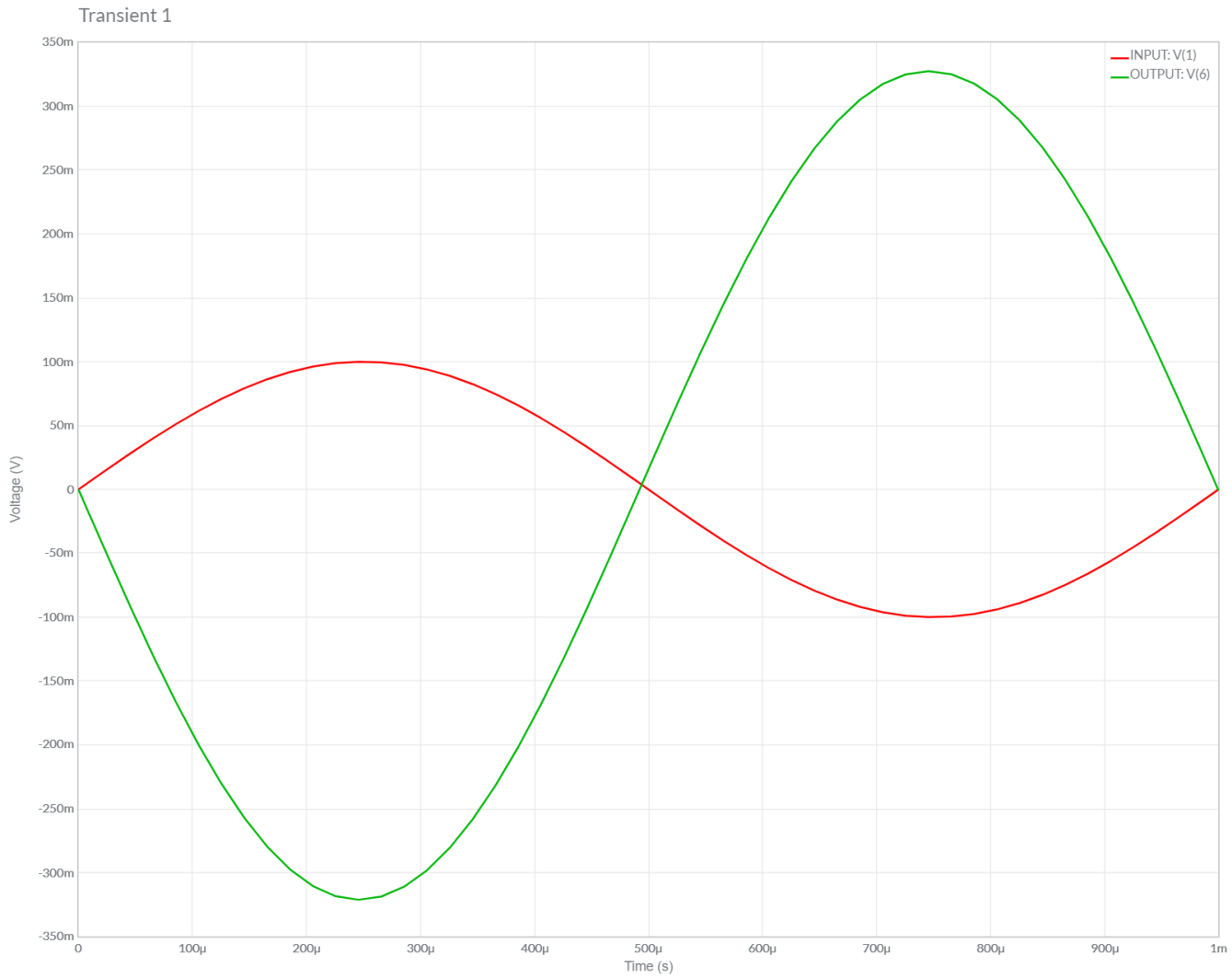
In CE amplifier configuration, there will always a phase-shift of 180 degrees between the input and output as described in figure below.



CIRCUIT DIAGRAM FROM MULTISIM



INPUT – OUTPUT WAVEFORMS



CONCLUSIONS

1.) In this Experiment, We have studied about Input and Output Characteristics of BJT in Common Emitter Configuration and also implemented it successfully on Multisim.

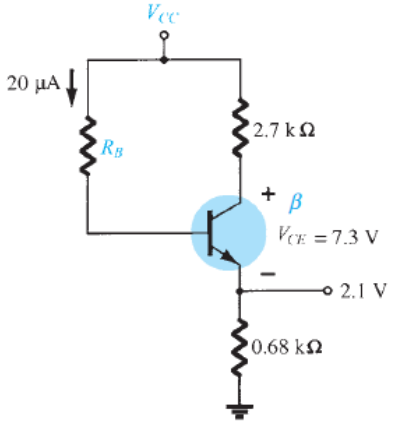
2.) We **Verified** the Theoretical Knowledge of Input and Output Characteristics of BJT in Common Emitter Configuration by *Plotting Input & Output Characteristic Graph*.

3.) We also Implemented Common Emitter *Amplifier* and Observed its Input and Output Waveforms.

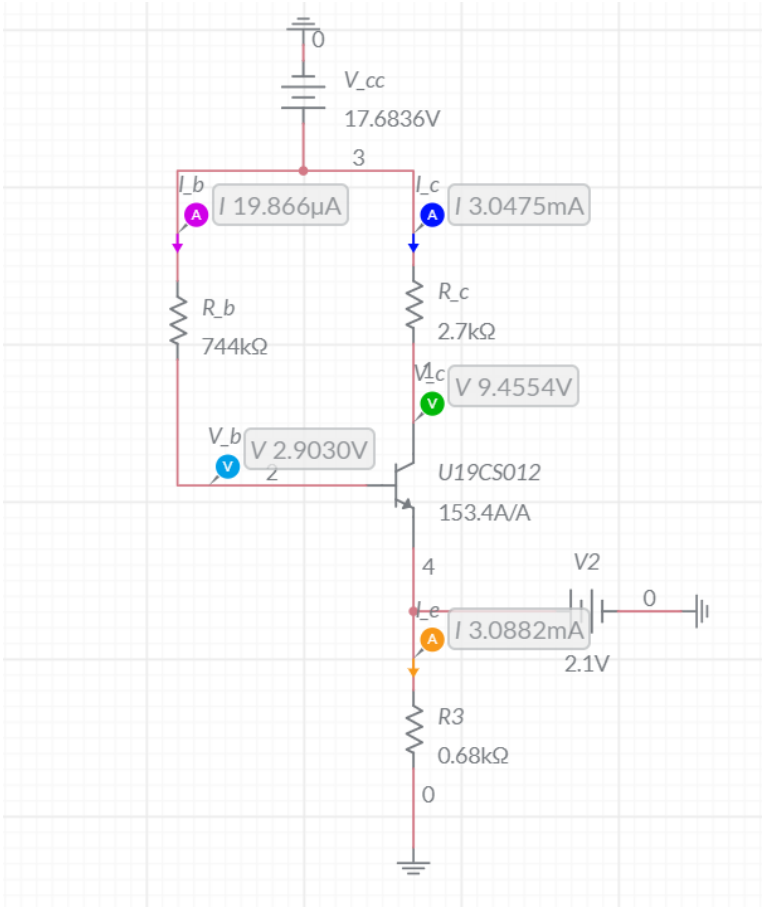
ASSIGNMENT-10

U19CS012

1.) Using the information provided in the figure below, determine the values of Beta, Vcc and Rb theoretically. Also compute and verify the values of Ic, Vb, and Vc by implementing the circuit on Multisim.



1.) Circuit Image:

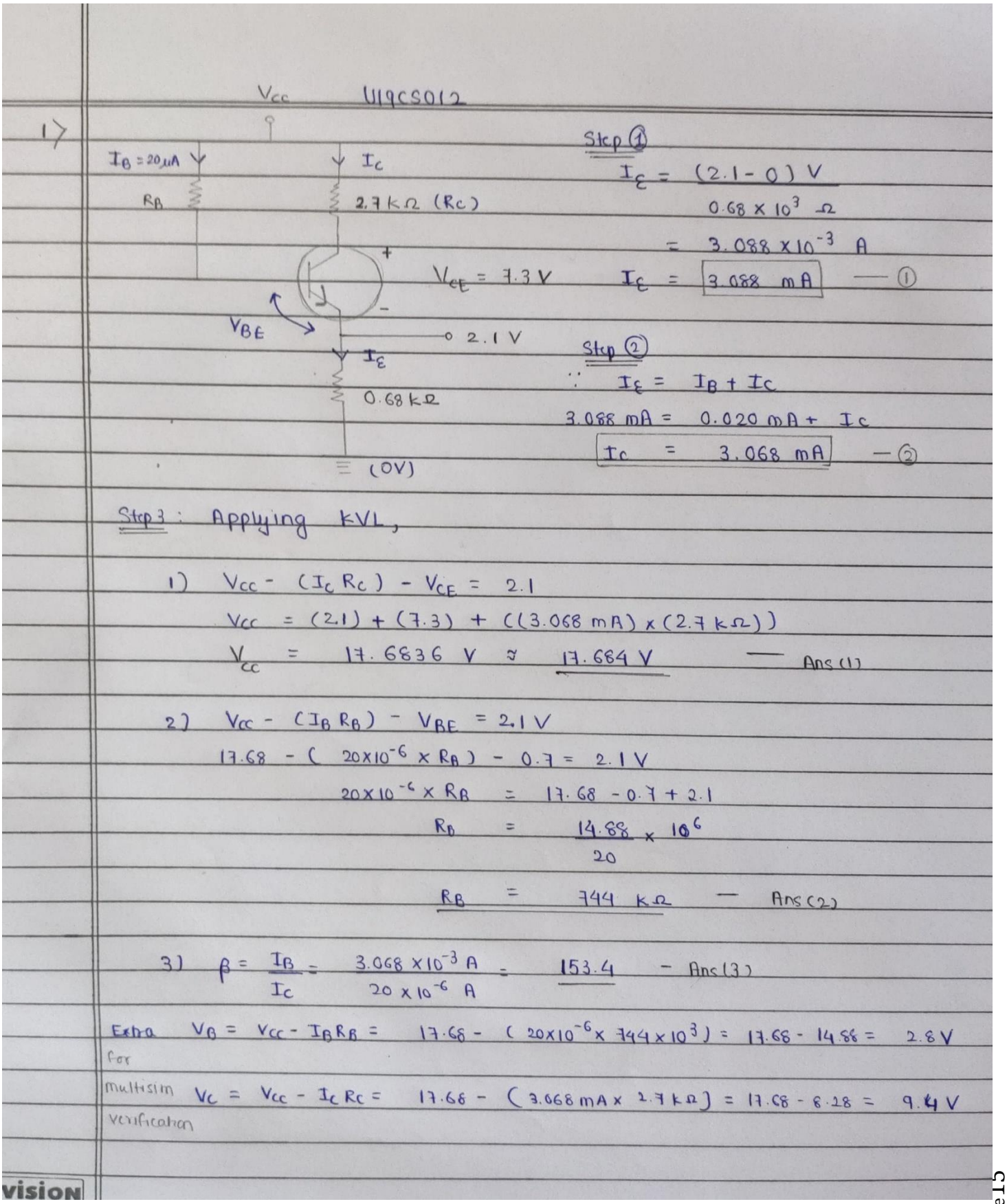


2.) Grapher Image:

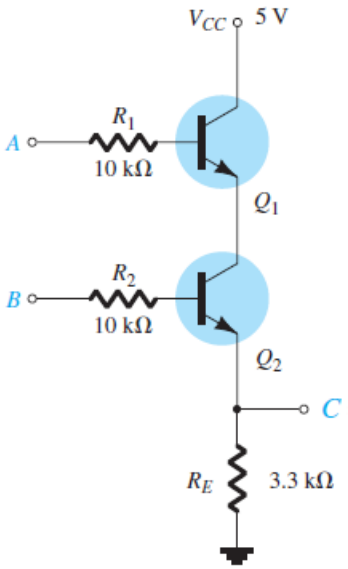
Parameter	Graph	Theoretical
V_b	2.9030 V	2.8 V
V_c	9.4554 V	9.4 V
I_b	0.019866 mA	0.020 mA
I_c	3.0475 mA	3.068 mA
I_e	3.0882 mA	3.088 mA

We can Clearly See Both the **Theoretical** and **Multisim Values** are *Approximately Equal*. Hence the Experiment was Performed Successfully and Circuit is verified.

3.) Calculations



2. Simulate the below given circuit on Multisim and predict the type of Digital Logic implemented by the same. Use the default transistor available in Multisim. Attach all the four screenshots (00, 05, 50 and 55).



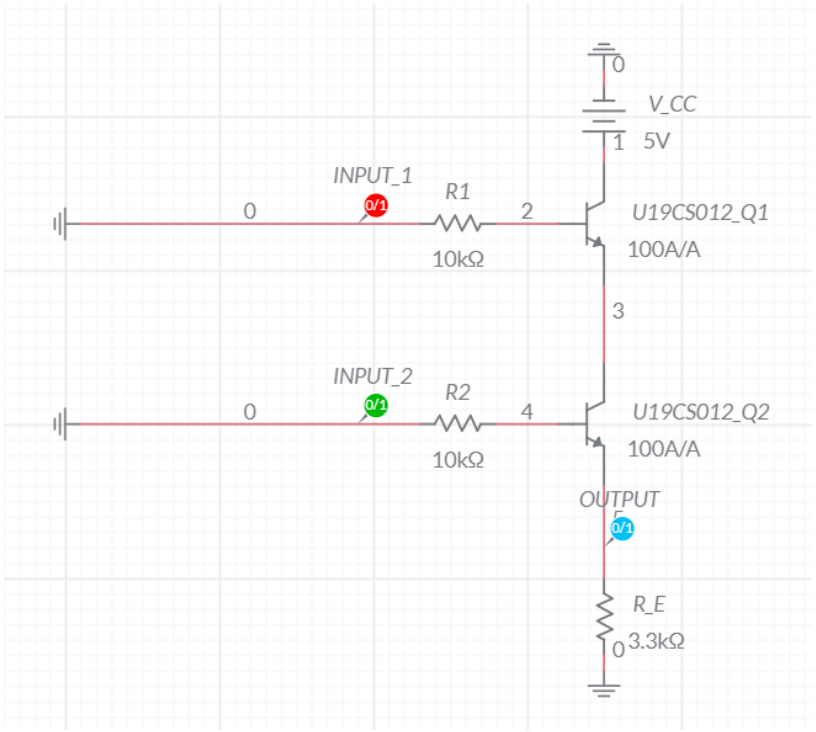
Answer:

By Observing the Truth Table Obtained from Multisim Simulation, We can clearly see that the Above Circuit [Equivalent to] represents the **Logical AND** Gate.

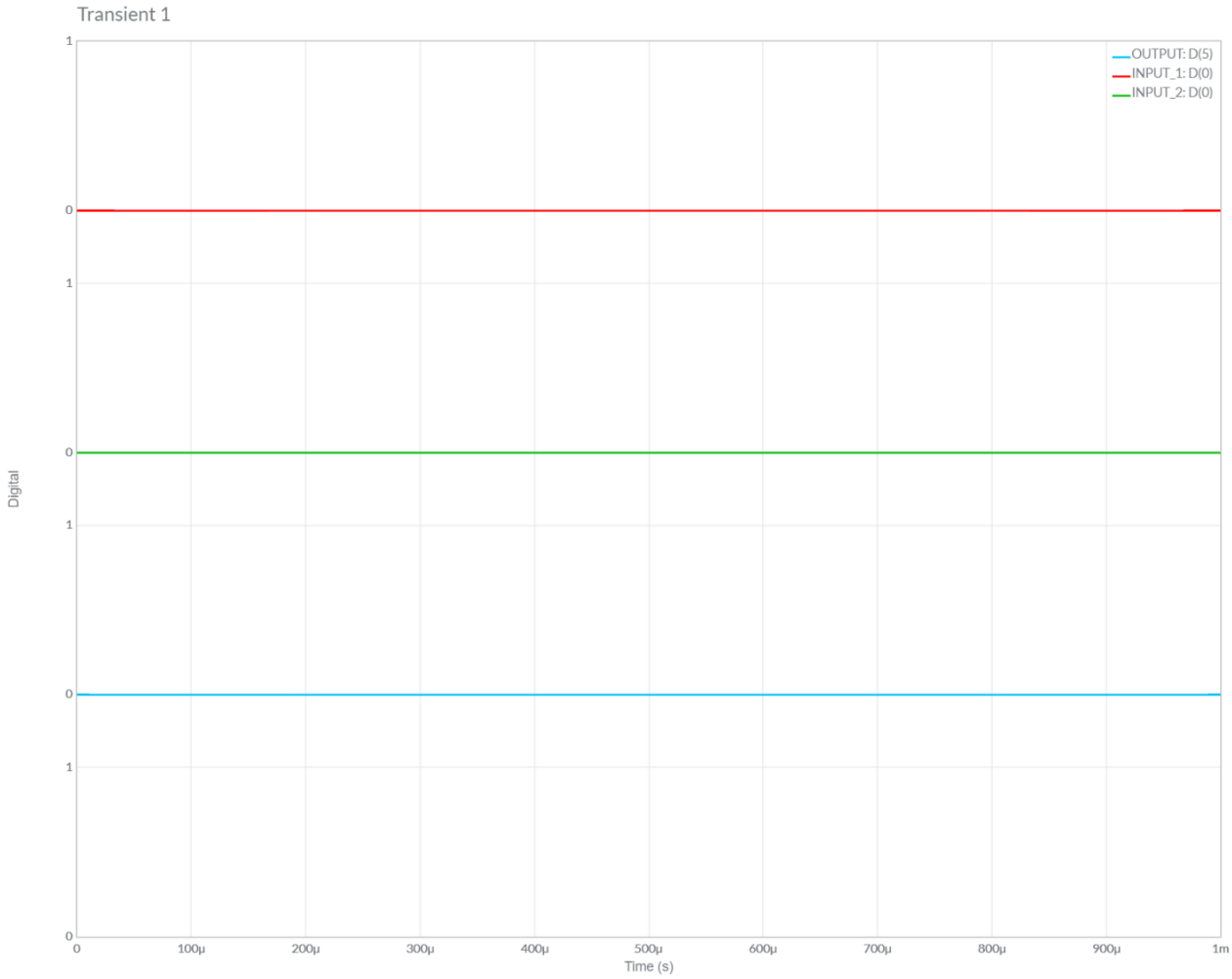
INPUT1	INPUT2	OUTPUT
0	0	0
0	1	0
1	0	0
1	1	1

A.) Case #1: 00

1.) Circuit Image:

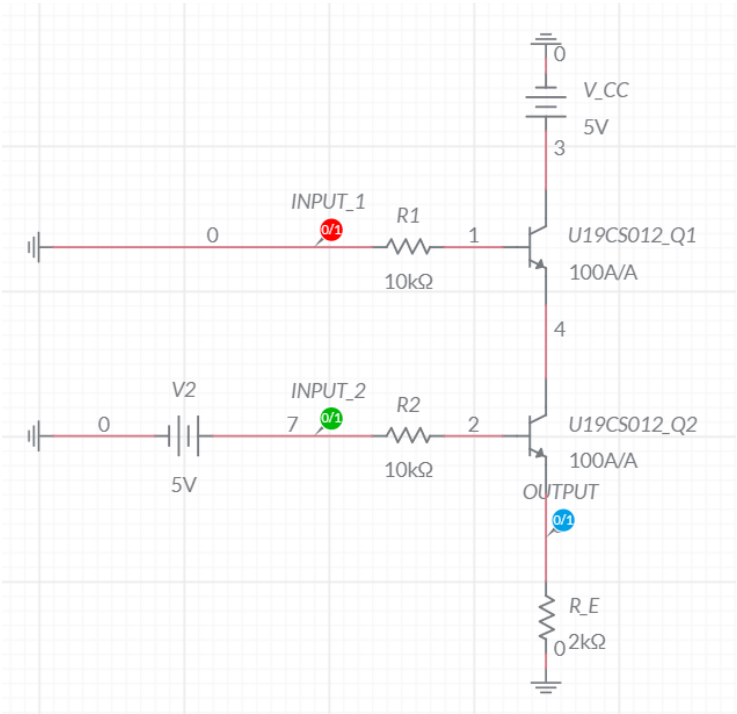


2.) Grapher Image:



B.) Case #2: 05

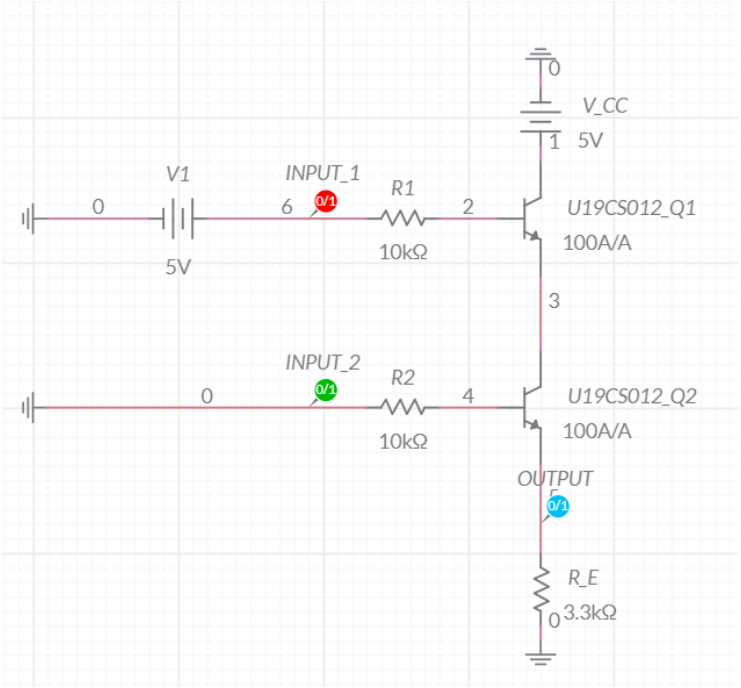
1.) Circuit Image:



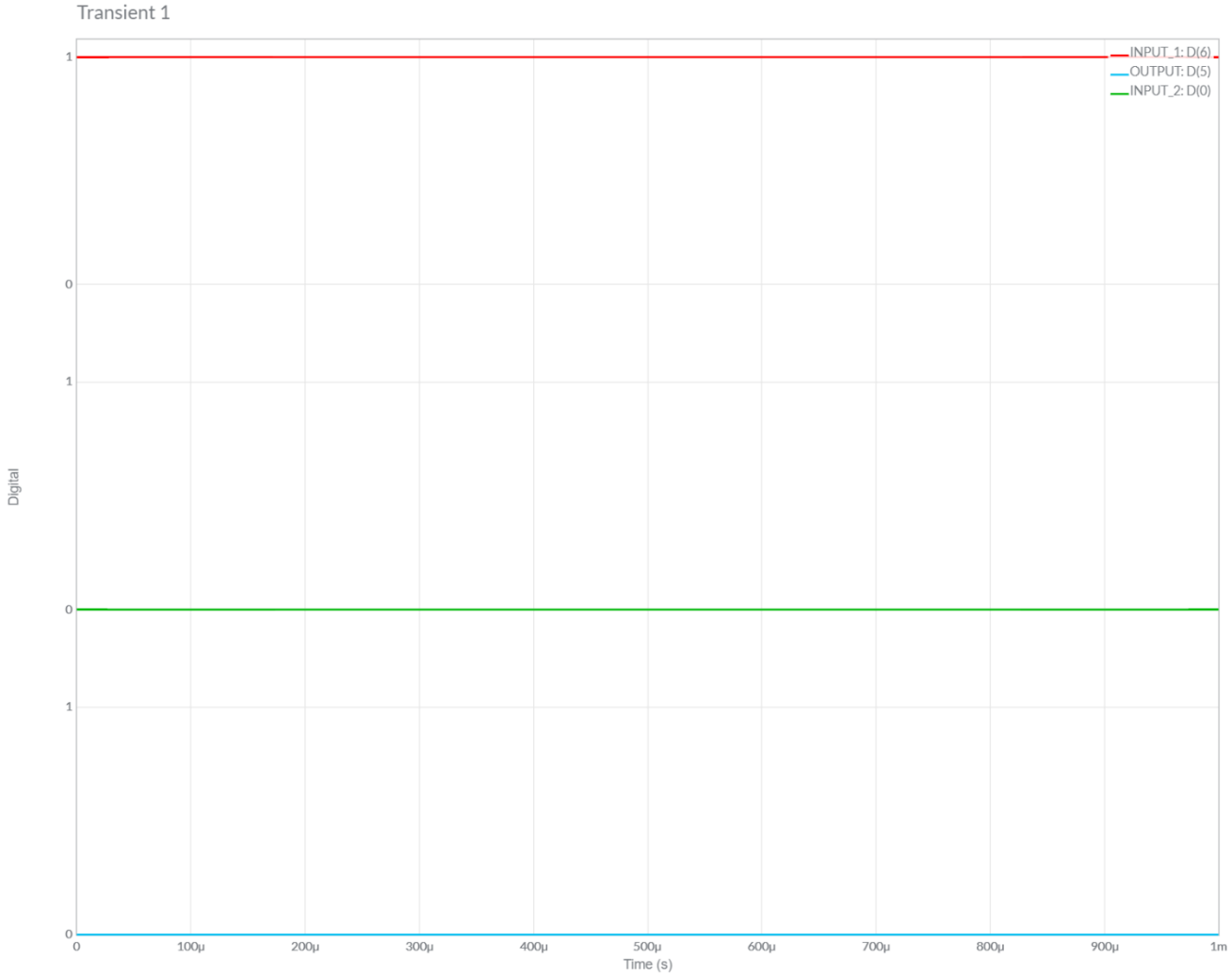
2.) Grapher Image:

C.) Case #3: 50

1.) Circuit Image:

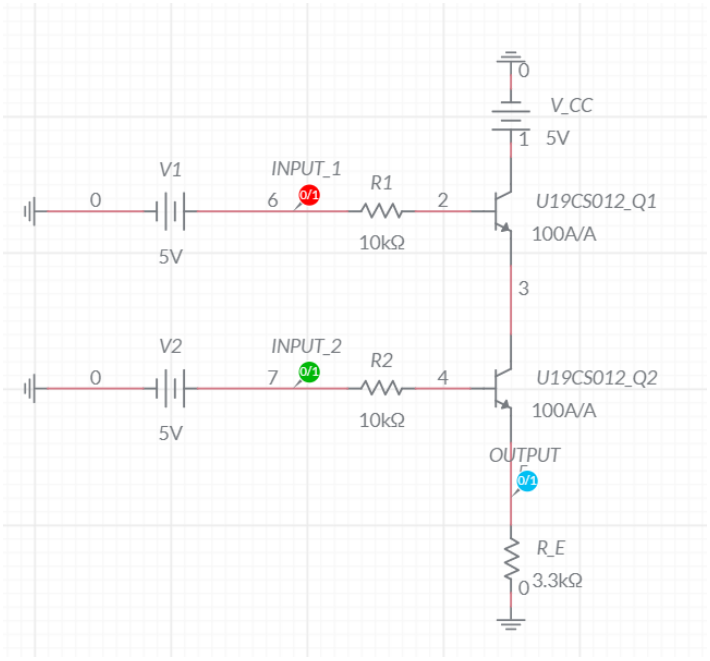


2.) Grapher Image:



D.) Case #4: 55

1.) Circuit Image:



2.) Grapher Image: