Sardar Vallabhbhai National Institute of Technology, Surat

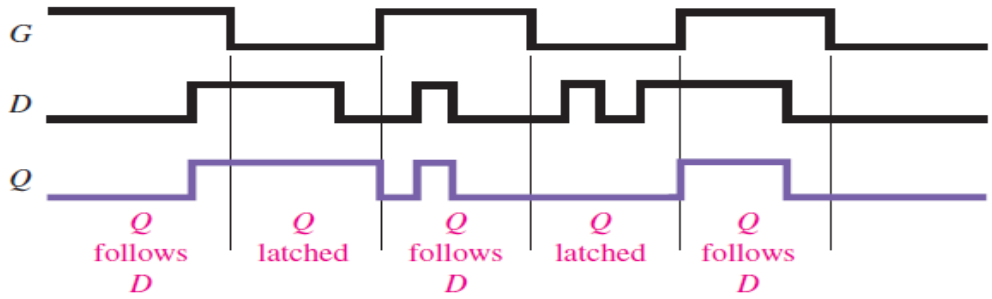
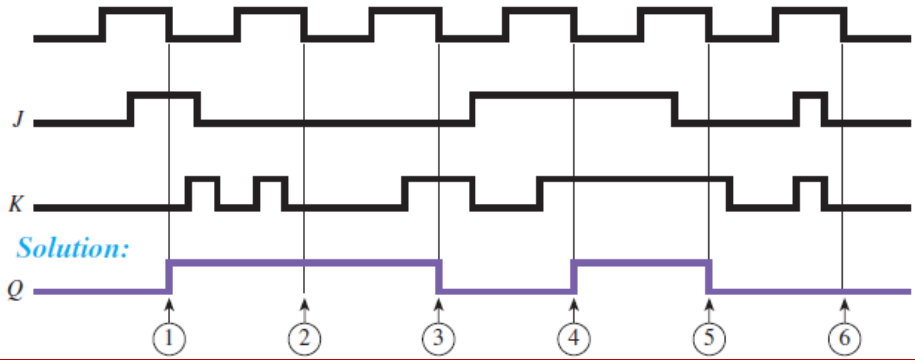
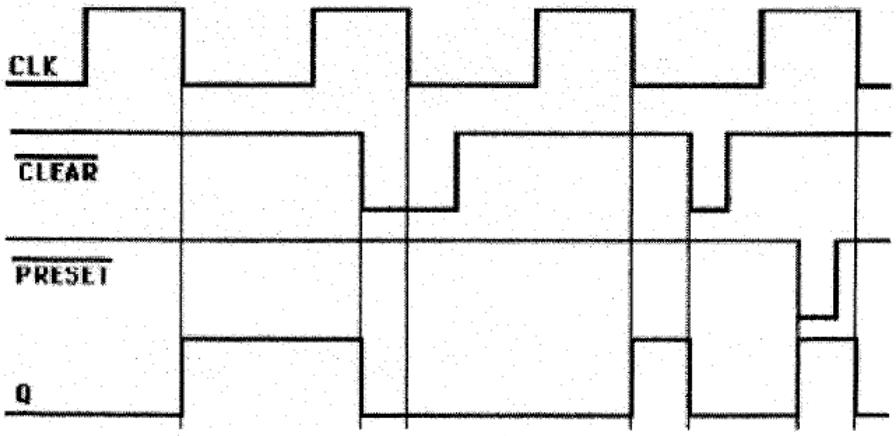
ECED Department

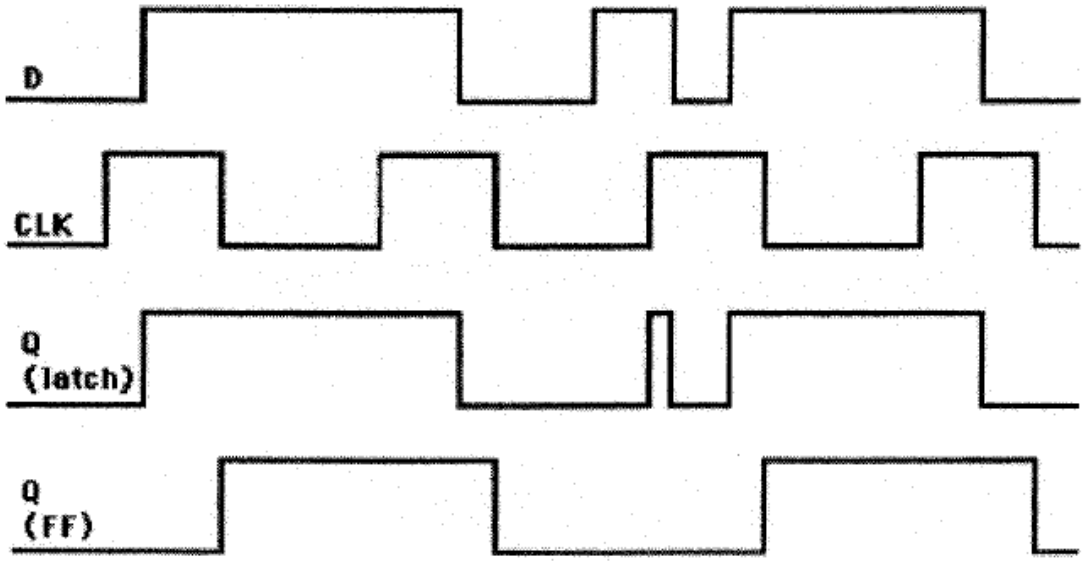
Subject: Digital Electronics & Logic Design (EC-207)

B.Tech Computer, Sem-III, Div – (A&B)

Date: 13-10-2020

Tutorial – 5 Hints/Solutions

1	Minterms: 0,5,7,9,12,14,15	2
2	Maxterms: 1,2,3,4,6,8,10,11,13	2
3		2
4		3
5	Since J=K=1, the output will toggle with every negative going clock pulse as long as preset and clear are held high. 	2

6		4