

# CO-Quiz 5 of 5

Total questions : 13

Max Marks : 13 (THE HIGHEST Marks will be MAPPED TO 10 Marks)

Time : 13 minutes

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\* Required

Logisim gives \_\_\_\_\_ color to wire whenever there are problems with incompatible bus width or conflicting value, \*

☒ Orange

☐ Brown

☒ Red

☒ Black

The following truth table is the implementation of \_\_\_\_\_. \*

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

☐  $Y = (A' + BC)$

☐  $Y = (B' + AC)$

☐  $Y = A + B + C$

☒  $B'$



\_\_\_\_\_ can combine multiple wires into a single wire with a wider bit width. \*

- ☒ Splitter
- ☐ Separator
- ☐ Combiner

The logical expression  $C=A+A'B$  is not equivalent to \*

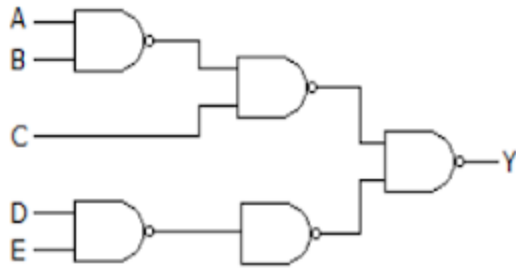
- ☒  $C=A'B$
- ☒  $C=AB$
- ☐  $C=A+B$
- ☒  $C=A'+B$

Once you ready with preparation of circuit in logisim circuit, none of your circuit wires should be \_\_\_\_\_ or \_\_\_\_\_. \*

- ☐ Brown
- ☒ Blue
- ☐ Black
- ☒ Gray



The following circuit in logisim is the implementation of \_\_\_\_\_.\*



- ☐  $Y = A' + B' + C' + D' + E'$
- ☒  $Y = (A' + B')C + (DE)'$
- ☐  $Y = AB + C + DE$
- ☐  $Y = AB + C(D+E)$

In logisim, both AND and OR gates can have only two inputs. \*

- ☒ True
- ☐ False

A full adder can be made using \_\_\_\_\_.\*

- ☒ two half adders
- ☐ three half adders
- ☐ two half adders and a OR gate
- ☐ two half adders and a NOT gate



The inputs of a NAND gate are connected together. The resulting circuit becomes of \_\_\_\_\_ gate. \*

- ☐ AND
- ☒ NOT
- ☐ OR
- ☐ NOR

The unconnected legs of the gate will be of color \_\_\_\_\_. \*

- ☐ Green
- ☐ Brown
- ☒ Blue
- ☐ Gray

The minimum number of 2-input NAND gates required to simulate the function  $S = (A + B)(C + D)$  is \_\_\_\_\_. \*

- ☐ 6
- ☐ 3
- ☐ 4
- ☒ 5



The output of the half adder is \_\_\_\_\_. \*

- ☐ carry
- ☐ none of these
- ☒ sum and a carry
- ☐ sum

In logisim, the circuit can also be made by the repeated use of \*

- ☐ NOT
- ☐ OR
- ☒ NAND
- ☐ NOR

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