



DEPARTMENT OF ELECTRONICS ENGINEERING SARDAR VALLABHBHAI NATIONAL INSTITUTE OF TECHNOLOGY

DLED LAB Practical-2

**Verification of truth table of basic logic gates.
Implementation of basic logic gates using NAND and
NOR gates.**

- ❑ Deals with binary variables that take 2 discrete values (0 and 1), and with logic operations
- ❑ Three basic logic operations: AND, OR, NOT

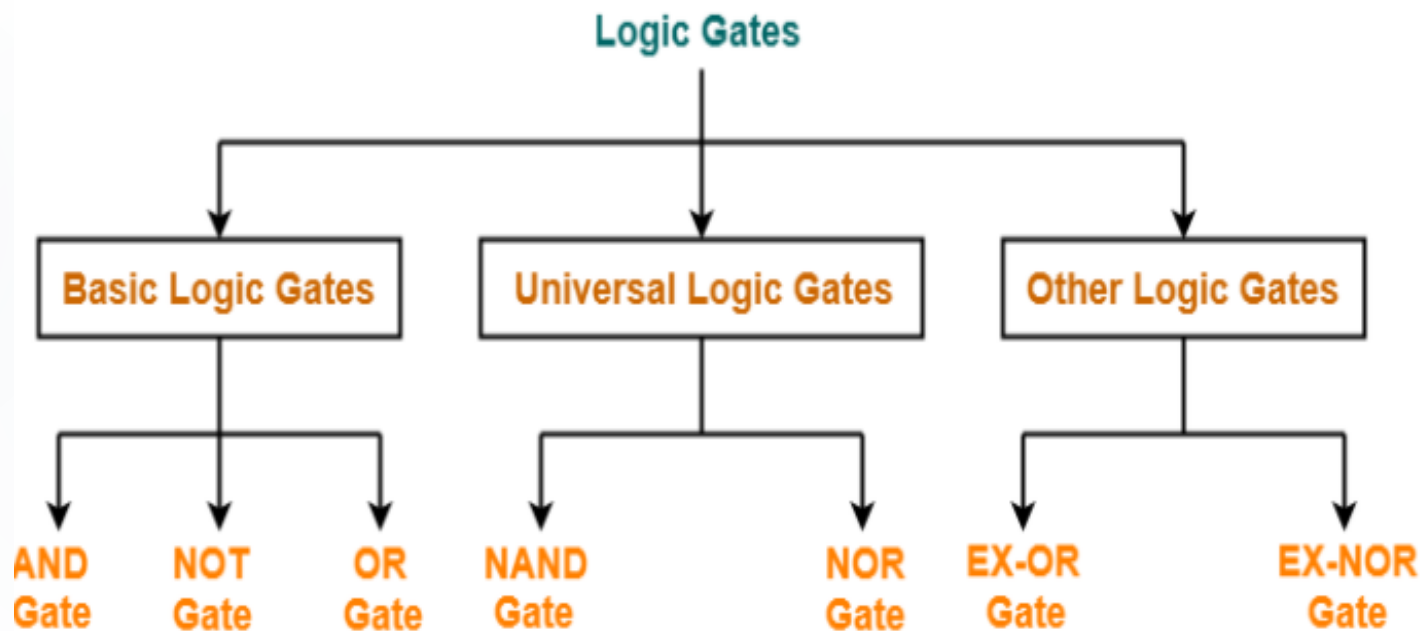
❑ $F(\text{variables}) = \text{Expression}$

↓
set of binary
variables

- Operators (+, •, ')
- Variables
- Constants (0, 1)
- Groupings (parenthesis)

❑ Example: $F(a,b) = a \bullet b$

- ❑ Logic gates are the switches that turn ON or OFF depending on the input conditions.
- ❑ They are the basic building blocks of computers.

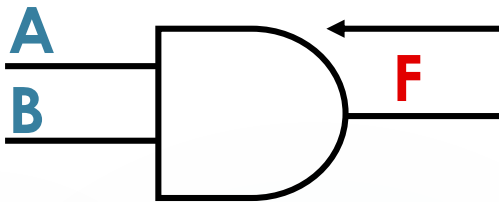


Basic Logic Gates:

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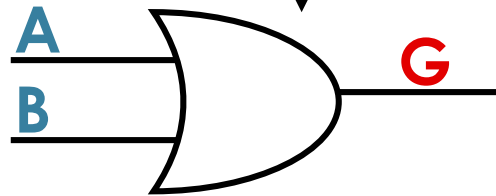
Symbols

2-Input AND



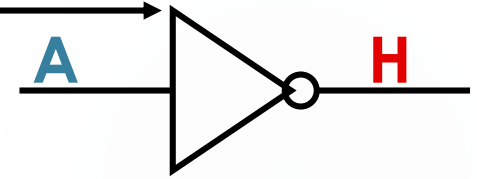
$$F = A \cdot B$$

2-Input OR



$$G = A + B$$

NOT (Inverter)



$$H = \bar{A} = A'$$

A	B	$F = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

A	B	$G = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

A	$F = \bar{A}$
0	1
1	0

Truth Tables

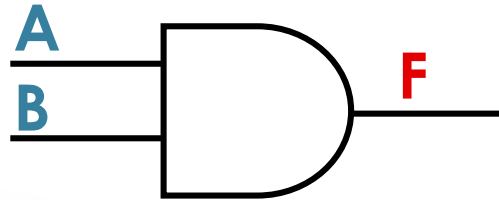
Basic Logic Gates:

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Timing Diagrams

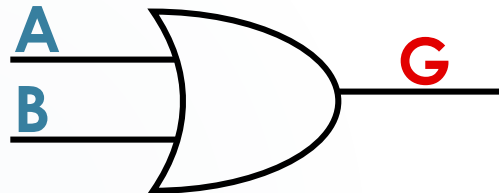
2-Input AND

$$F = A \cdot B$$



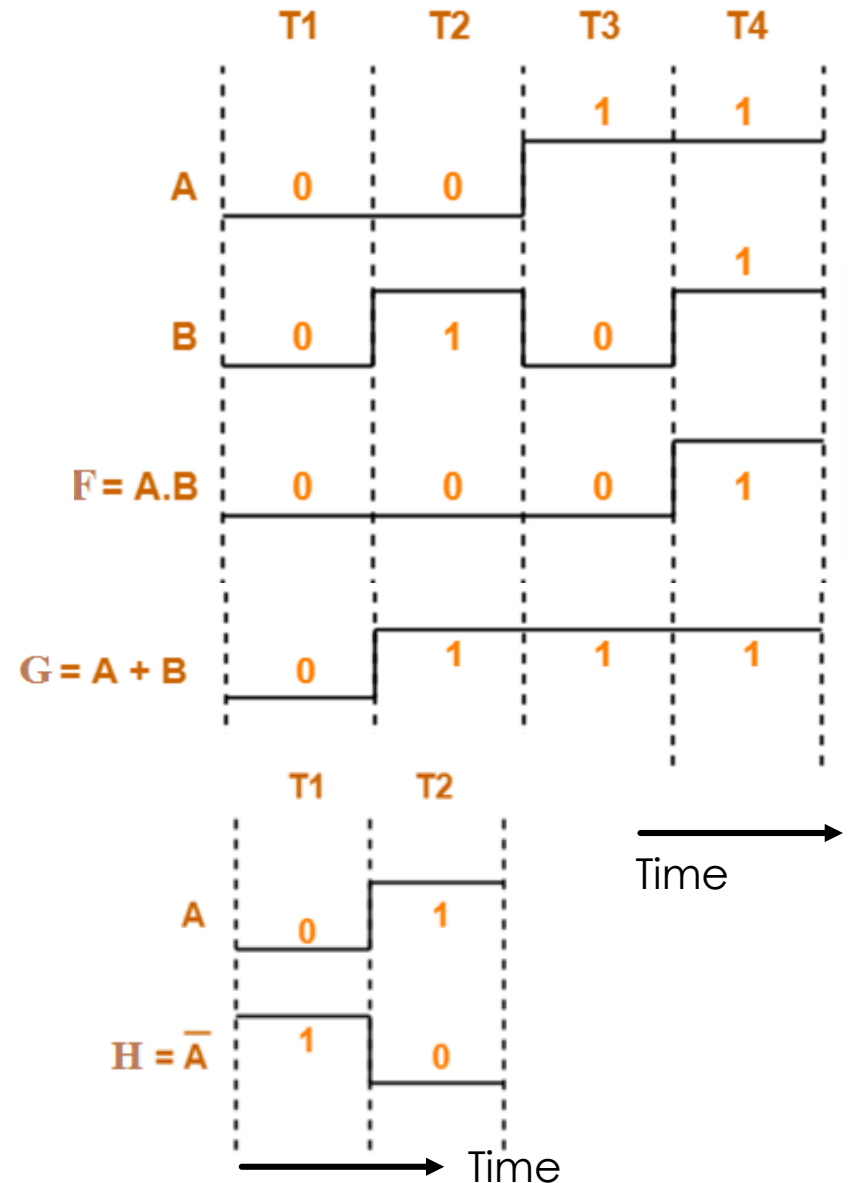
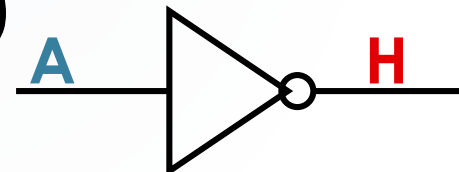
2-Input OR

$$G = A + B$$

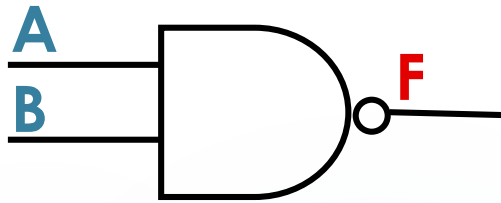


NOT (Inverter)

$$H = A'$$

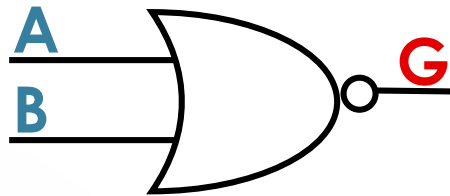


2-Input NAND



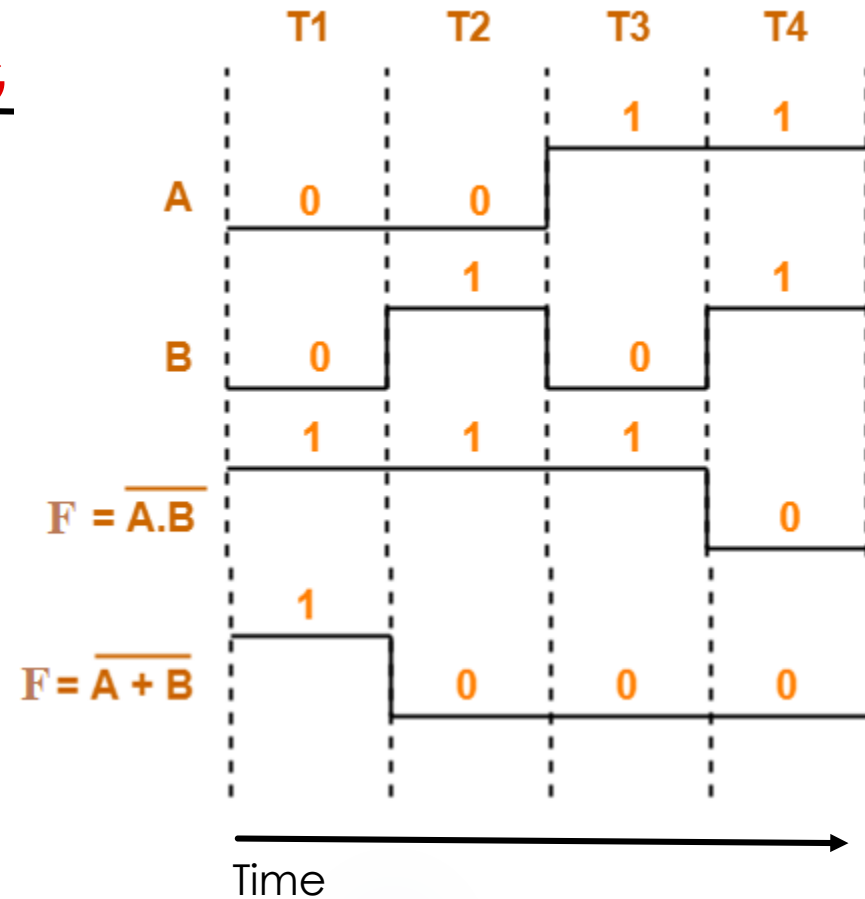
$$F = \overline{A \cdot B}$$

2-Input NOR

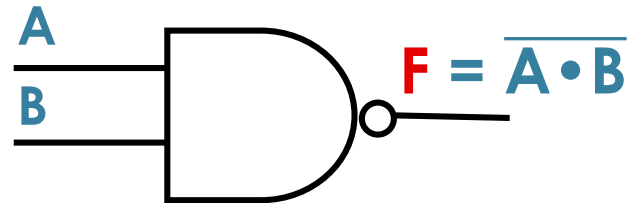


$$G = \overline{A + B}$$

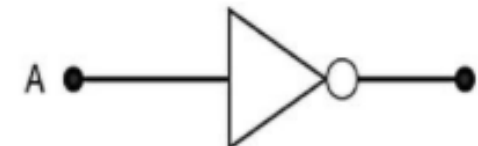
A	B	$F = \overline{A \cdot B}$	$G = \overline{A + B}$
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0



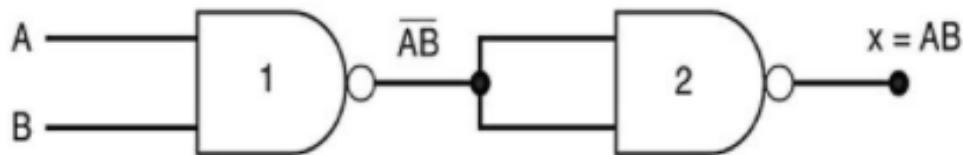
2-Input NAND



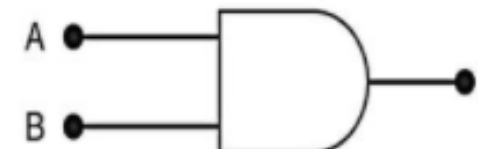
(a)



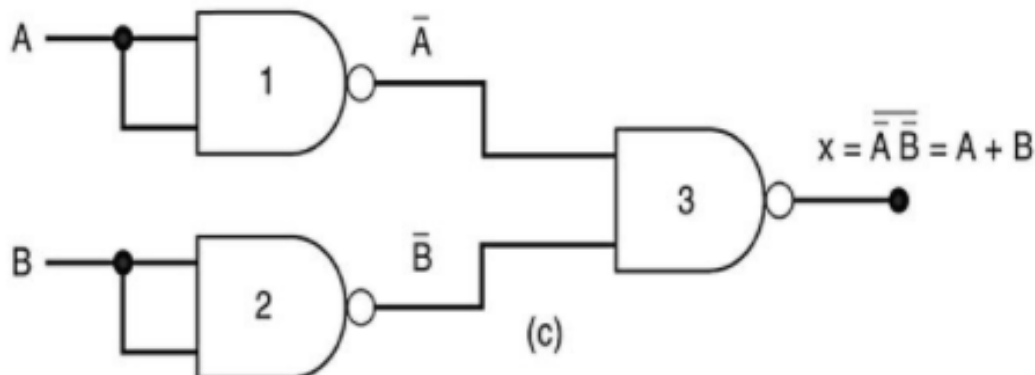
INVERTER



(b)



AND

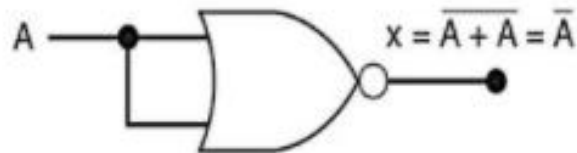
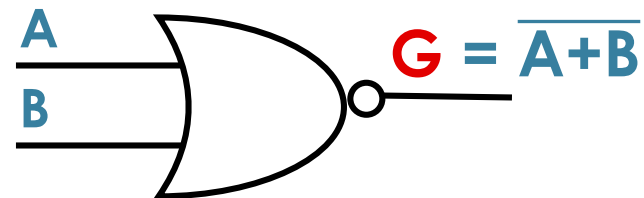


(c)

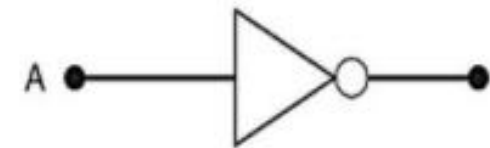


OR

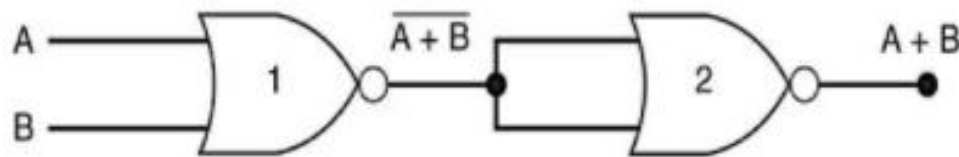
2-Input NOR



(a)



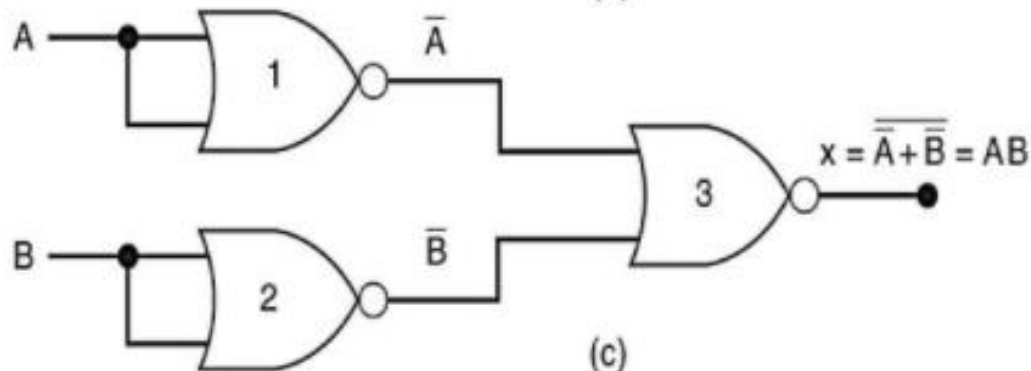
INVERTER



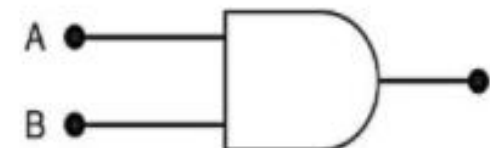
(b)



OR

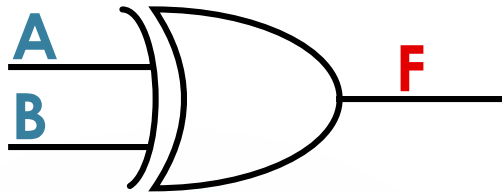


(c)



AND

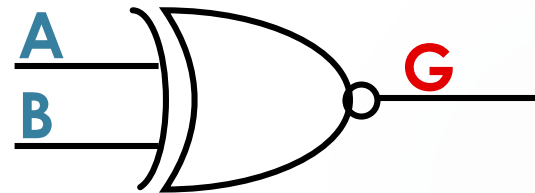
2-Input EX-OR



$$F = A \oplus B = A\bar{B} + \bar{A}B$$

A	B	$F = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

2-Input EX-NOR

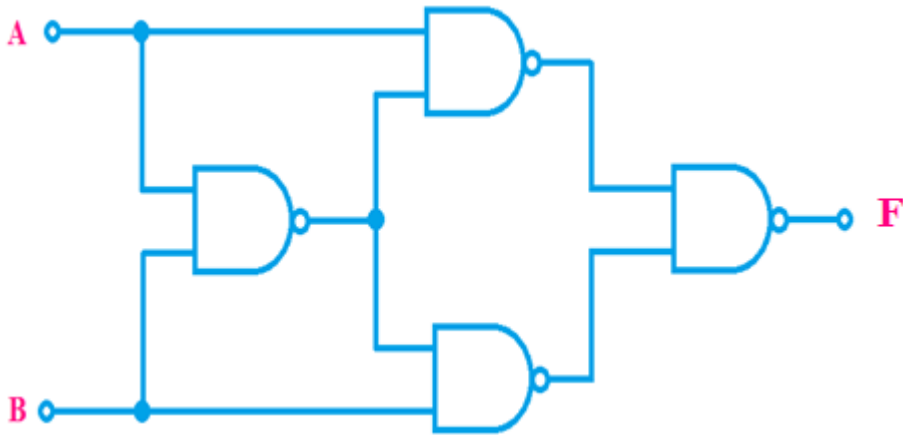


$$G = A \odot B = AB + \bar{A}\bar{B}$$

A	B	$G = A \odot B$
0	0	1
0	1	0
1	0	0
1	1	1

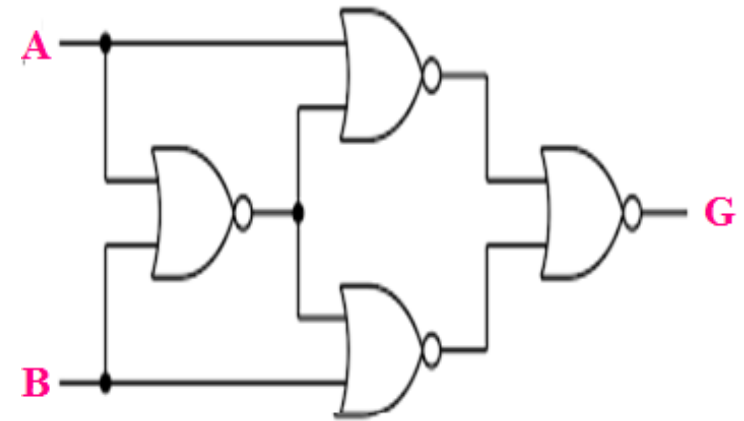
2-Input EX-OR using NAND

$$F = A \oplus B$$



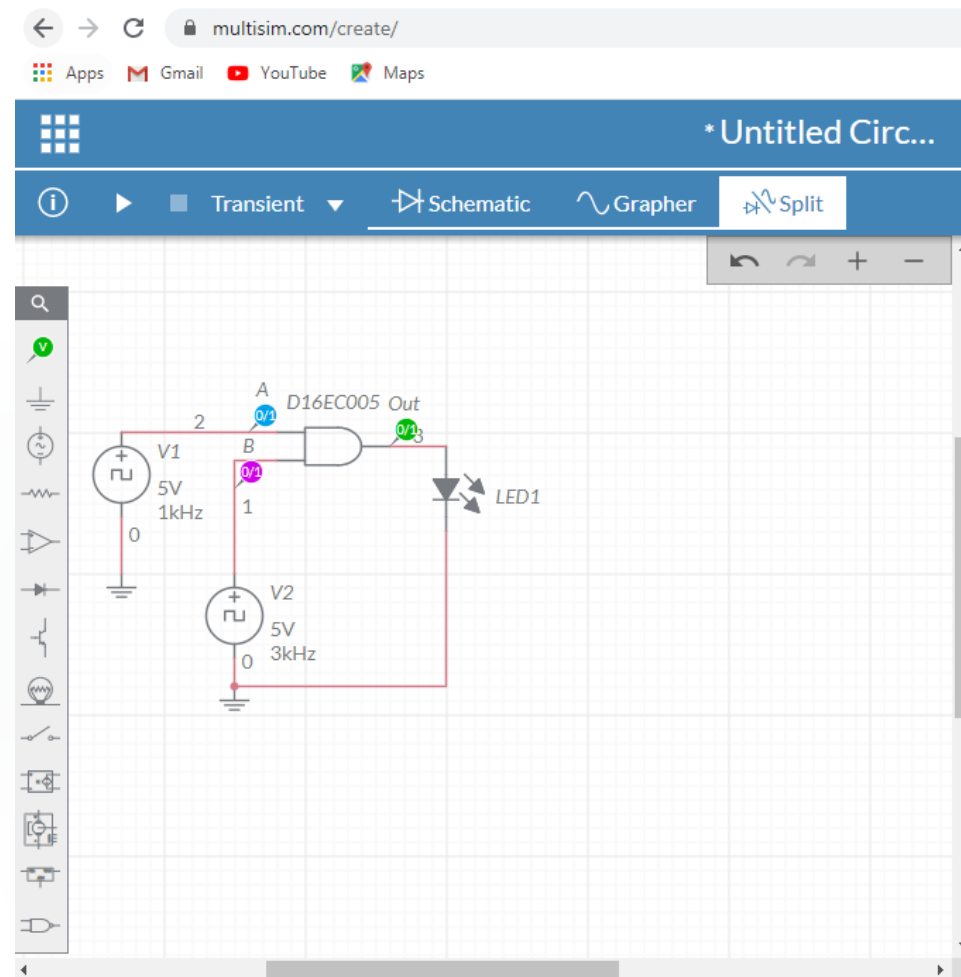
2-Input EX-NOR using NOR

$$G = A \odot B$$



Simulation of AND Gate in Multisim:

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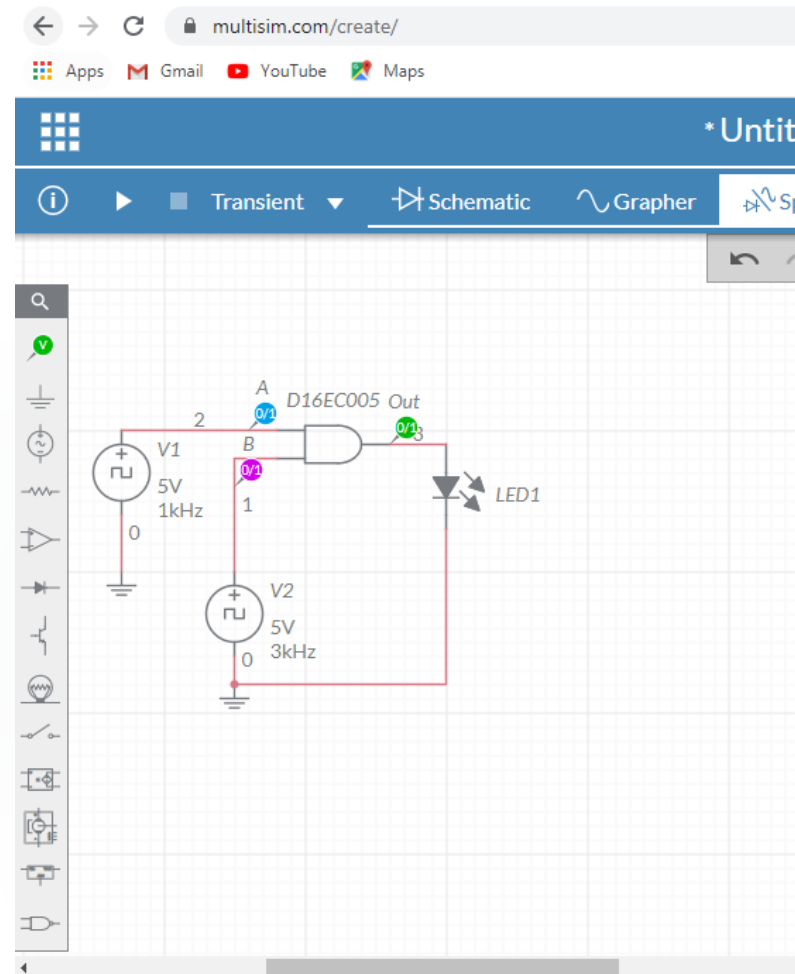
The image shows the component properties window for a 2-Input AND gate. The window is titled 'Item' and 'Document'. The component ID is 'D16EC005_AND', which is circled in red. The Type is '2-Input AND'. The Description states: 'Digital AND logic gate with 2 inputs. See [AND](#) for more information.' The Model is 'Digital_AND2'. The parameters are:

- rise_delay: 1e-9 s
- Output rise delay
- fall_delay: 1e-9 s
- Output fall delay
- Rise time: 0 s
- Fall time: 0 s

The Logic levels section is expanded, showing 'Use document settings' checked. The Use logic levels settings from section is partially visible.

Simulation of AND Gate in Multisim:

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Item Document

ID A

Type Probe

Probe type [?]

Function Digital

Logic levels [?]

☒ Use document settings

Mode 3.3V

Input low threshold 0.8 V

Input high threshold 2 V

Measurement labels [?]

Interactive simulation

☒ Instantaneous

Grapher plot [?]

☒ Show plots

Item Document

ID V1

Type Clock Voltage

Description

Clock voltage source. This component is a square wave generator.

Model [?]

CLOCK_SOURCE

VP 5 V

Voltage

Freq 1k Hz

Frequency

DC 50 %

Duty cycle

TR 1n s

Rise time

TF 1n s

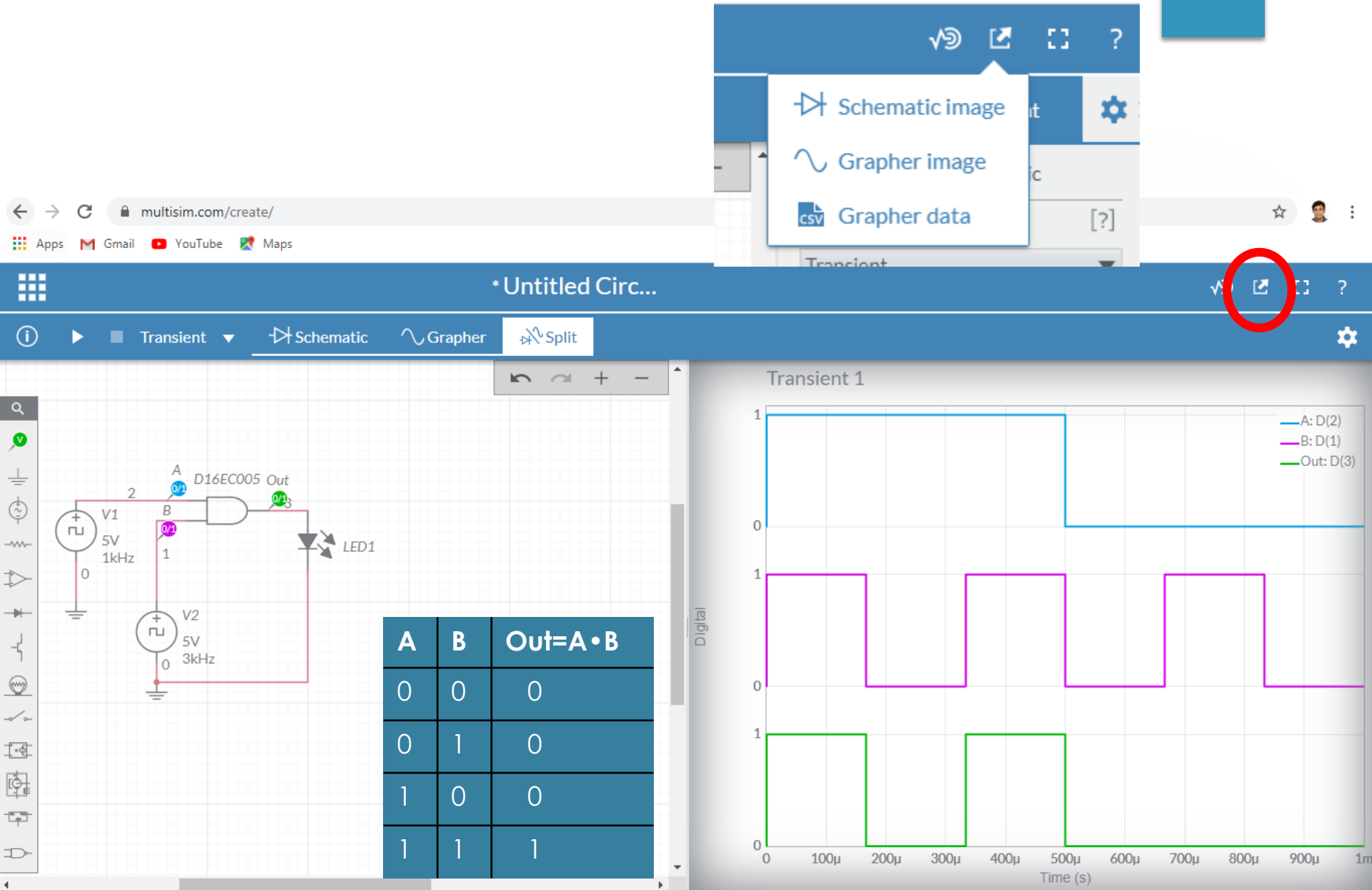
Fall time

Symbol

Details

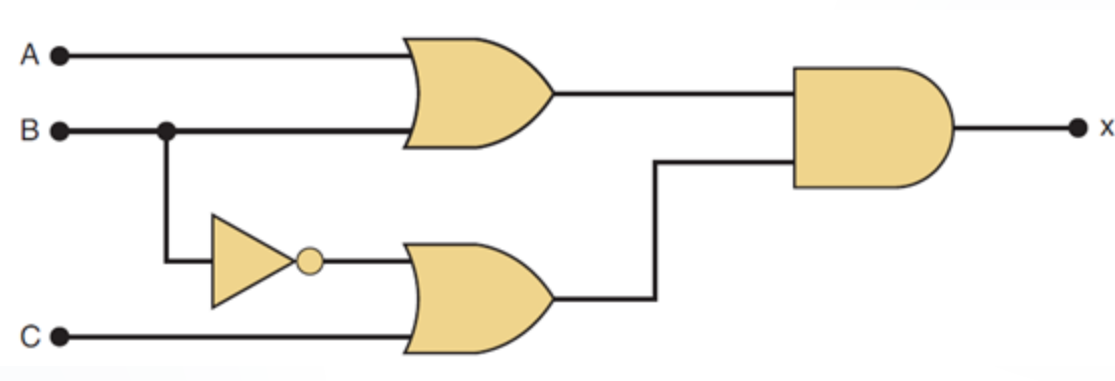
Simulation of AND Gate in Multisim:

13

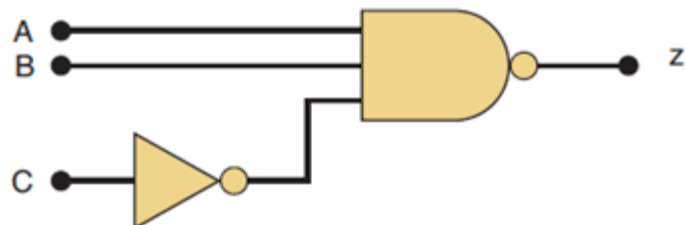


- ❑ Derive the logic expressions of following circuits and draw the truth table.
- ❑ Implement these circuits in Multisim and verify the truth table by from timing diagrams.

Circuit: 1



Circuit: 2



Circuit: 3

