Boolean Algebra

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The "WHY" Boolean Algebra

Algebra

When we learned numbers like 1, 2, 3, we also then learned how to add, multiply, etc. with them. Boolean Algebra covers operations that we can do with 0's and 1's. Computers do these operations ALL THE TIME and they are basic building blocks of computation inside your computer program.

Axioms, laws, theorems

We need to know some rules about how those 0's and 1's can be operated on together. There are similar axioms to decimal number algebra, and there are some laws and theorems that are good for you to use to simplify your operation.

How does Boolean Algebra fit into the big picture?

- It is part of the Combinational Logic topics (memoryless)
 - Different from the Sequential logic topics (can store information)

- Learning Axioms and theorems of Boolean algebra
 - Allows you to design logic functions
 - Allows you to know how to combine different logic gates
 - Allows you to simplify or optimize on the complex operations

Boolean algebra

- A Boolean algebra comprises...
 - A set of elements B
 - Binary operators {+, •} Boolean sum and product
 - A unary operation { ' } (or { \bar{ } })
 example: A' or A
- ...and the following axioms
 - 1. The set B contains at least two elements {a b} with a ≠ b
 - 2. Closure: a+b is in B a•b is in B
 - 3. Commutative: a+b=b+a $a \bullet b=b \bullet a$
 - 4. Associative: a+(b+c)=(a+b)+c $a \cdot (b \cdot c)=(a \cdot b) \cdot c$
 - 5. Identity: a+0 = a $a \cdot 1 = a$
 - 6. Distributive: $a+(b \cdot c)=(a+b) \cdot (a+c)$ $a \cdot (b+c)=(a \cdot b)+(a \cdot c)$
 - 7. Complementarity: a+a'=1 $a \cdot a'=0$

Digital (binary) logic is a Boolean algebra

Substitute

- {0, 1} for B
- AND for Boolean Product.
- OR for + Boolean Sum.
- NOT for 'Complement.

All the axioms hold for binary logic

Definitions

- Boolean function
 - Maps inputs from the set {0,1} to the set {0,1}
- Boolean expression
 - An algebraic statement of Boolean variables and operators

Logic Gates (AND, OR, Not) & Truth Table

AND $X \cdot Y$ $XY \cdot Y = \begin{bmatrix} X & Y & Z \\ \hline 0 & 0 & 0 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix}$ X+Y OR \overline{X} X' $X \longrightarrow Y$ NOT

Logic functions and Boolean algebra

• Any logic function that is expressible as a truth table can be written in Boolean algebra using +, ●, and '

| X | Υ | Z | Z=X•Y |
|---|---|---|-------|
| 0 | 0 | 0 | |
| 0 | 1 | 0 | |
| 1 | 0 | 0 | |
| 1 | 1 | 1 | |

| Χ | Υ | Χ' | Ζ | Z=X'∙Y |
|---|---|----|---|--------|
| 0 | 0 | 1 | 0 | - |
| 0 | 1 | 1 | 1 | |
| 1 | 0 | Ō | 0 | |
| 1 | 1 | 0 | 0 | |

| Χ | Υ | X' | Y' | X • Y | X' •Y' | Z | $Z=(X\bullet Y)+(X'\bullet Y')$ |
|---|---|----|----|-------|------------------|---|---------------------------------|
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | . , , , |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | |
| 1 | 1 | 0 | 0 | 1 | 1 0 0 0 | 1 | |
| | | | | | | | |

Two key concepts

- Duality (a meta-theorem— a theorem about theorems)
 - All Boolean expressions have logical duals
 - Any theorem that can be proved is also proved for its dual
 - Replace: with +, + with •, 0 with 1, and 1 with 0
 - Leave the variables unchanged

De Morgan's Theorem

- Procedure for complementing Boolean functions
- Replace: with +, + with •, 0 with 1, and 1 with 0
- Replace all variables with their complements

Universal Gate Implementation NAND Gate as Universal Gate

OR Gate using NAND Gate

NOR Gate using NAND Gate

EXOR using NAND Gate

NOR Gate as Universal Gate: TO DO

EX-OR Gate Using NOR gate

Boolean Functions

- Boolean function is described by an a algebraic expression called Boolean expressions which consists of binary variables and logic operation symbols.
- Mathematical functions can be expressed in two ways:

An expression is finite but not unique

$$f(x,y) = 2x + y$$

= $x + x + y$
= $2(x + y/2)$
= ...

A function table is unique

| × | У | f(x,y) |
|--------|--------|--------|
| 0 | 0 | 0 |
| 2 | 2 | 6 |
| 23 | 41 | 87 |
| ••• | | ••• |

We can represent logical functions in two analogous ways too:

- A finite, but non-unique Boolean expression.
- A truth table, which will turn out to be unique.

Boolean expressions

We can use these basic operations to form more complex expressions:

$$f(x,y,z) = (x + y')z + x'$$

- f is the name of the function.
- (x, y, z) are the input variables, each representing 1 or 0. Listing the inputs is optional, but sometimes helpful.
- A literal is any occurrence of an input variable or its complement. The function above has four literals: x, y', z, and x'.
- Precedence is important, but not too difficult.
 - NOT has the highest precedence, followed by AND, and then OR.
 - Fully parenthesized, the function above would be kind of messy:

$$f(x,y,z) = (((x + (y'))z) + x')$$

Useful laws and theorems

Identity: X + 0 = X Dual: $X \cdot 1 = X$

Null: X + 1 = 1 Dual: $X \bullet 0 = 0$

Idempotent: X + X = X Dual: $X \bullet X = X$

Involution: (X')' = X

Complementarity: X + X' = 1 Dual: $X \cdot X' = 0$

Commutative: X + Y = Y + X Dual: $X \bullet Y = Y \bullet X$

Associative: (X+Y)+Z=X+(Y+Z) Dual: $(X \bullet Y) \bullet Z=X \bullet (Y \bullet Z)$

Distributive: $X \bullet (Y+Z)=(X \bullet Y)+(X \bullet Z)$ Dual: $X+(Y \bullet Z)=(X+Y) \bullet (X+Z)$

Uniting: $X \bullet Y + X \bullet Y' = X$ Dual: $(X+Y) \bullet (X+Y') = X$

Proof of law with Truth table

$$(A \cdot B) \cdot C = A \cdot (B \cdot C)$$
 $(A+B)+C=A+(B+C)$

$$(A+B)+C=A+(B+C)$$

Useful laws and theorems (con't)

Absorption: $X+X \bullet Y=X$ Dual: $X \bullet (X+Y)=X$

Absorption (#2): $(X+Y') \bullet Y = X \bullet Y$ Dual: $(X \bullet Y') + Y = X + Y$

 $x + \overline{x}y = x + y$

(x+y)(x+z) = x + yz

de Morgan's: (X+Y+...)'=X'•Y'•... Dual: (X•Y•...)'=X'+Y'+...

Duality: $(X+Y+...)^D=X\bullet Y\bullet...$ Dual: $(X\bullet Y\bullet...)^D=X+Y+...$

Multiplying & factoring: (X+Y) • (X'+Z)=X • Z+X' • Y

Dual: $X \bullet Y + X' \bullet Z = (X + Z) \bullet (X' + Y)$

Consensus: $(X \circ Y) + (Y \circ Z) + (X' \circ Z) = X \circ Y + X' \circ Z$

Dual: $(X+Y) \bullet (Y+Z) \bullet (X'+Z) = (X+Y) \bullet (X'+Z)$

Proofing the theorems using axioms

• Idempotency: x + x = xProof: $x + x = (x + x) \cdot 1$ by identity $= (x + x) \cdot (x + x')$ by complement $= x + x \cdot x'$ by distributivity = x + 0 by complement = x by identity

• Idempotency: x • x = x Proof:

$$x \bullet x = (x \bullet x) + 0$$
 by identity
 $= (x \bullet x) + (x \bullet x')$ by complement
 $= x \bullet (x + x')$ by distributivity
 $= x \bullet 1$ by complement
 $= x$ by identity

Theorems

Prove the uniting theorem-- X•Y+X•Y'=X

```
Distributive X \cdot Y + X \cdot Y' = X \cdot (Y + Y')
Complementarity = X \cdot (1)
Identity = X
```

Prove the absorption theorem-- X+X•Y=X

```
Identity X+X \bullet Y = (X \bullet 1)+(X \bullet Y)
Distributive = X \bullet (1+Y)
Null = X \bullet (1)
Identity = X
```

To Prove

$$A + \bar{A}B = A + B$$

$$(A+B)(A+C)=A+BC$$

More proves

$$(A+\overline{B}+AB)(A+\overline{B})(\overline{A}B)=0$$

$$Y = (\overline{AB} + \overline{A} + AB)$$

Theorems

Prove the consensus theorem--

$$(XY)+(YZ)+(X'Z)=XY+X'Z$$

Complementarity
$$XY+YZ+X'Z = XY+(X+X')YZ + X'Z$$

Distributive $= XYZ+XY+X'YZ+X'Z$

Use absorption {AB+A=A} with A=XY and B=Z

$$= XY + X'YZ + X'Z$$

Rearrange terms

$$= XY+X'ZY+X'Z$$

Use absorption {AB+A=A} with A=X'Z and B=Y

$$XY+YZ+X'Z = XY+X'Z$$

Logic simplification

Example:

$$Z = A'BC + AB'C' + AB'C + ABC' + ABC$$

```
= A'BC + AB'(C' + C) + AB(C' + C) distributive

= A'BC + AB' + AB complementary

= A'BC + A(B' + B) distributive

= A'BC + A complementary

= BC + A absorption #2 Duality

(X \bullet Y') + Y = X + Y \text{ with } X = BC \text{ and } Y = A
```

Algebraic manipulation

```
x'y' + xyz + x'y

= x'(y' + y) + xyz [Distributive; x'y' + x'y = x'(y' + y)]

= x' \cdot 1 + xyz [ Axiom 5; y' + y = 1]

= x' + xyz [ Axiom 2; x' \cdot 1 = x']

= (x' + x)(x' + yz) [ Distributive ]

= 1 \cdot (x' + yz) [ Axiom 5; x' + x = 1]

= x' + yz [ Axiom 2; x' \cdot 1 = x']
```

More Problems:

$$A\bar{B} + \bar{A}B + \bar{A}\bar{B} + AB$$

 $(AB+C)(AB+D)$
 $AB+ABC+A\bar{B}=A$ (Prove)

De Morgan's Theorem

Use de Morgan's Theorem to find complements

Example: $F=(A+B) \bullet (A'+C)$, so $F'=(A' \bullet B')+(A \bullet C')$

| <u>A</u> | В | C | <u> </u> |
|----------|---|---|----------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

| Α | В | С | _ F ′ |
|---|---|---|--------------|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Complement of a function

- The complement of a function always outputs 0 where the original function outputted 1, and 1 where the original produced 0.
- In a truth table, we can just exchange 0s and 1s in the output column(s)

$$f(x,y,z) = x(y'z' + yz)$$

| X | У | Z | f(x,y,z) | × | У | Z | f'(x,y,z) |
|---|---|---|----------|---|---|---|-----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

Complementing a function algebraically

```
f(x,y,z) = x(y'z' + yz)

f'(x,y,z) = (x(y'z' + yz))' [complement both sides]

= x' + (y'z' + yz)' [because (xy)' = x' + y']

= x' + (y'z')' (yz)' [because (x + y)' = x' y']

= x' + (y + z)(y' + z') [because (xy)' = x' + y', twice]
```

- You can use DeMorgan's law to keep "pushing" the complements inwards
- You can also take the dual of the function, and then complement each literal
 - If f(x,y,z) = x(y'z' + yz)...
 - ...the dual of f is x + (y' + z')(y + z)...
 - ...then complementing each literal gives x' + (y + z)(y' + z')...
 - ...so f'(x,y,z) = x' + (y + z)(y' + z')

Canonical Forms

- Any boolean function that is expressed as a sum of minterms or as a product of maxterms is said to be in its canonical form.
- A minterm is a special product of literals, in which each input variable appears exactly once.
- A function with n variables has 2^n minterms (since each variable can appear complemented or not) A three-variable function, such as f(x,y,z), has $2^3 = 8$ minterms:

Minterms

• Each minterm is true for exactly one combination of inputs:

| Minterm | Is true when Sh | northanc |
|---------|-----------------|----------|
| x'y'z' | x=0, y=0, z=0 | m_0 |
| x'y'z | x=0, y=0, z=1 | m_1 |
| ×'yz' | x=0, y=1, z=0 | m_2 |
| x'yz | x=0, y=1, z=1 | m_3 |
| ×y'z' | x=1, y=0, z=0 | m_4 |
| ×y'z | x=1, y=0, z=1 | m_5 |
| ×yz' | x=1, y=1, z=0 | m_6 |
| ×yz | x=1, y=1, z=1 | m_7 |

Sum of minterms form

- Every function can be written as a sum of minterms, which is a special kind of sum of products form
- The sum of minterms form for any function is unique
- If you have a truth table for a function, you can write a sum of minterms expression just by picking out the rows of the table where the function output is 1 (1-minterm).

| X | У | Z | f(x,y,z) | f'(x,y,z) |
|---|---|---|----------|-----------|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |

$$f = x'y'z' + x'y'z + x'yz' + x'yz + xyz'$$

$$= m_0 + m_1 + m_2 + m_3 + m_6$$

$$= \Sigma(0,1,2,3,6)$$

$$f' = xy'z' + xy'z + xyz$$

$$= m_4 + m_5 + m_7$$

$$= \Sigma(4,5,7)$$

$$f' \text{ contains all the minterms not in } f$$

Sum of minterms: practise

F = x + yz, how to express this in the sum of minterms?

```
= x(y + y')(z + z') + (x + x')yz

= xyz + xyz' + xy'z + xy'z' + xyz + x'yz

= x'yz + xy'z' + xy'z + xyz' + xyz

= \Sigma(3,4,5,6,7)
```

or, convert the expression into truth-table and then read the minterms from the table

Maxterms

• A maxterm is a sum of literals, in which each input variable appears exactly once.

• A function with n variables has 2ⁿ maxterms

$$x' + y' + z'$$
 $x' + y' + z$ $x' + y + z'$ $x' + y + z$
 $x + y' + z'$ $x + y' + z$ $x + y + z'$ $x + y + z$

• The maxterms for a three-variable function f(x,y,z):

| Maxterm | Is false when | Shorthand | |
|--------------|---------------|--------------------|--------------|
| x + y + z | x=0, y=0, z=0 | M_0 | m_{∞} |
| x + y + z' | x=0, y=0, z=1 | M_1 | |
| x + y' + z | x=0, y=1, z=0 | M_2 | |
| x + y' + z' | x=0, y=1, z=1 | M_3 | minterm |
| x' + y + z | x=1, y=0, z=0 | M_4 | Mox Term |
| x' + y + z' | x=1, y=0, z=1 | $M_{\overline{5}}$ | |
| x' + y' + z | x=1, y=1, z=0 | M_6 | |
| x' + y' + z' | x=1, y=1, z=1 | M7. 11 | K |

• Each maxterm is *false* for exactly one combination of inputs:

Product of maxterms form

• Every function can be written as a unique product of maxterms

• If you have a truth table for a function, you can write a product of maxterms expression by picking out the rows of the table where the function output is 0 (0-maxterm).

| | | | | OP | So; | کی میں ر | f = (x' + y + z)(x' + y + z')(x' + y' + z') Max |
|------|-------|---|---|----------|-----------|----------|---|
| | × | У | Z | f(x,y,z) | f'(x,y,z) | | $= M_4 M_5 M_7 = \Pi(4,5,7)$ |
| , | 0 | 0 | 0 | / 1 | 0 | | |
| | 0 | 0 | 1 | 1 | 0 | FTT MI | f' = (x + y + z)(x + y + z')(x + y' + z) |
| | 0 | 1 | 0 | 1 | 0 | | (x + y' + z')(x' + y' + z) |
| | 0 | 1 | 1 | 1 | 0 | \sim | $= M_0 M_1 M_2 M_3 M_6$ $= \Pi(0,1,2,3,6)$ |
| XXX | 1 | 0 | 0 | 0 | 1 — | My | - 11(0,1,2,3,0) |
| 1477 | 1 | 1 | | 1 | - 1 | 5 | f' contains all the maxterms not in f |
| | 1 1 _ | 1 | 1 | 0 | 1 | - M7 | |

Product of maxterms: practise

• F = x'y' + xz, how to express this in the product of maxterms? Canonical = (x'y' + x)(x'y' + z)= (x' + x)(y' + x)(x' + z)(y' + z)Sor = (x + y')(x' + z)(y' + z)= (x + y' + zz')(x' + z + yy')(xx' + y' + z)= (x + y' + z)(x + y' + z')(x' + y + z)(x' + y' + z)(x + y' + z)(x' + y' + z)= (x + y' + z)(x + y' + z')(x' + y + z)(x' + y' + z)

or, convert the expression into truth-table and then read the minterms from the table

Minterms and maxterms are related

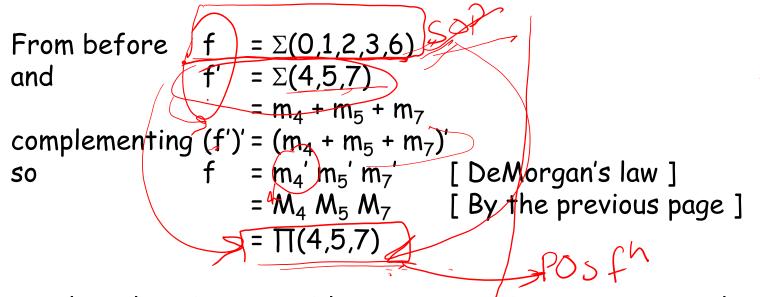
Any minterm m_i is the complement of the corresponding maxterm M_i

| Minterm | Shorthand | Maxterm | Shorthand | |
|---------|-----------|--------------|---------------------|---------------------------------------|
| x'y'z' | m_0 | x + y + z | M_{O} | $\left(\chi \gamma' \gamma' \right)$ |
| x'y'z | m_1 | x + y + z' | M_1 | $(\ \ \ \ \ \ \ \)$ |
| x'yz' | m_2 | x + y' + z | M_2 | |
| x'yz | m_3 | x + y' + z' | M_3 | X + 1 + Z |
| xy'z' | m_4 | x + y + z | \rightarrow M_4 | |
| xy'z | m_5 | X' + Y + Z' | M_5 | 1 20 2 |
| xyz' | m_6 | x' + y' + z | M_6 | (M_4) $= M_6$ |
| xyz | m_7 | x' + y' + z' | M_7 | 7 |

• For example, $m_4' = M_4$ because (xy'z')' = x' + y + z

Converting between canonical forms

• We can convert a sum of minterms to a product of maxterms



• In general, just replace the minterms with maxterms, using maxterm numbers that don't appear in the sum of minterms:

$$f = \Sigma(0,1,2,3,6)$$

= $\Pi(4,5,7)$

• The same thing works for converting from a product of maxterms to a sum of minterms

Standard Forms

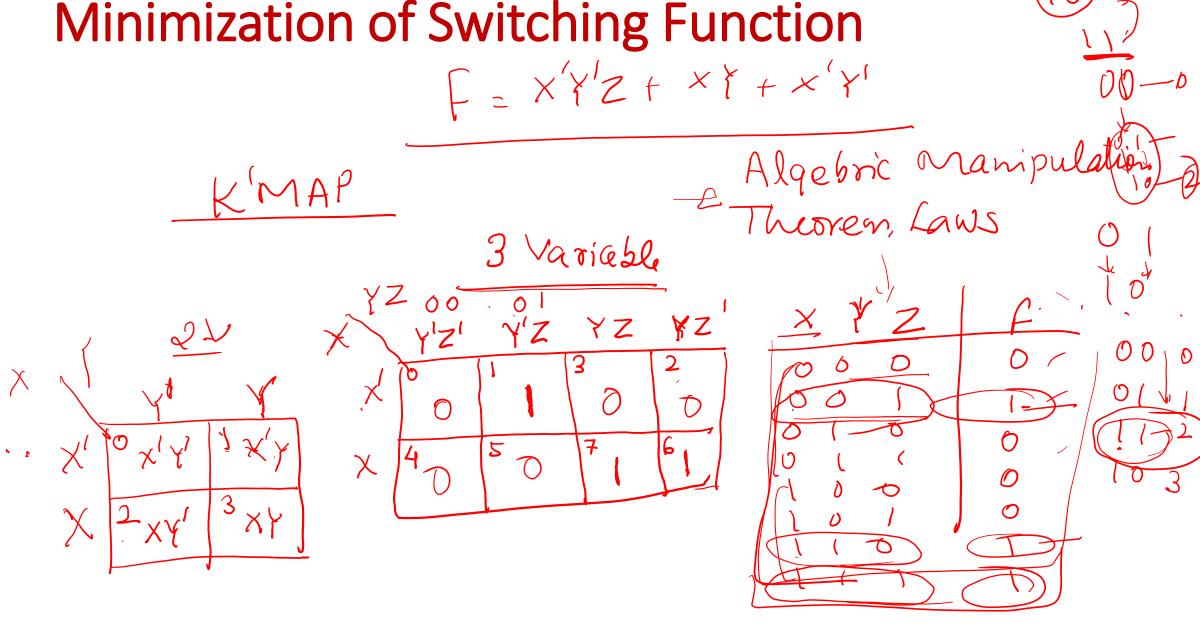
- Any boolean function that is expressed as a sum of products (SOP) or as a product of sums (POS), where each product-term or sum-term may require fewer than (n-1) operations, is said to be in its standard form.
- Standard forms are not unique, there can be several different SOPs and POSs for a given function.
- A SOP expression contains:
 - Only OR (sum) operations at the "outermost" level
 - Each term (implicant) must be a product of literals

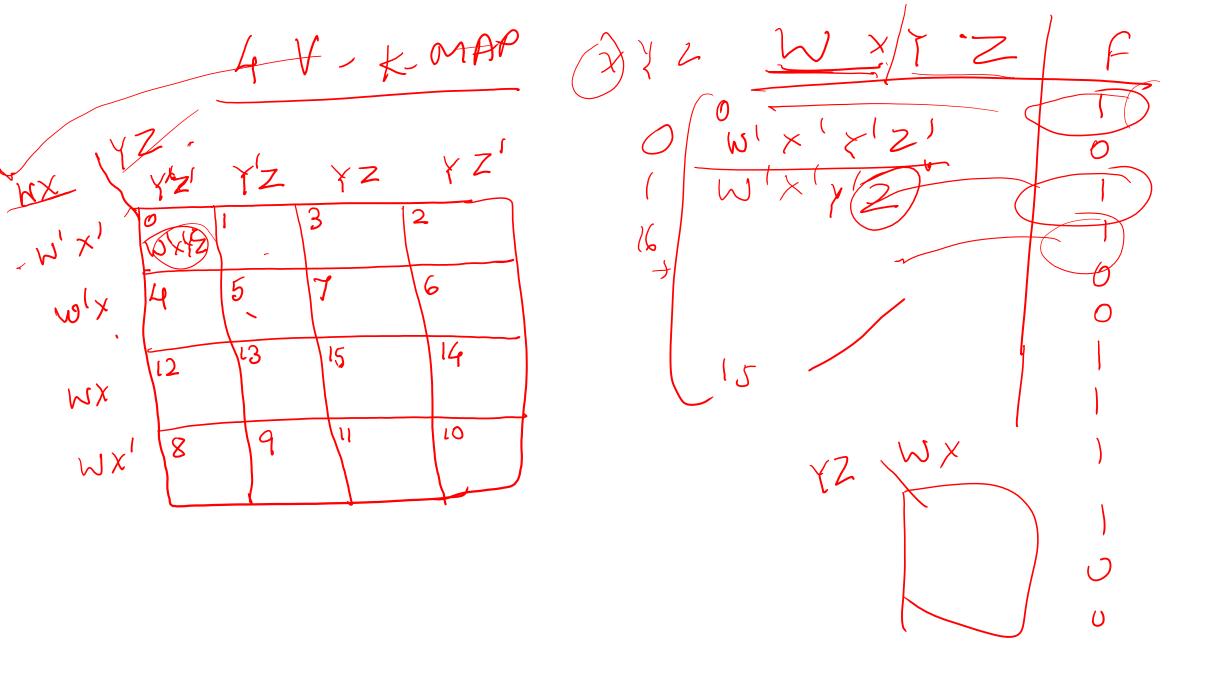
$$f(x,y,z) = xy + x'yz + xy'z$$

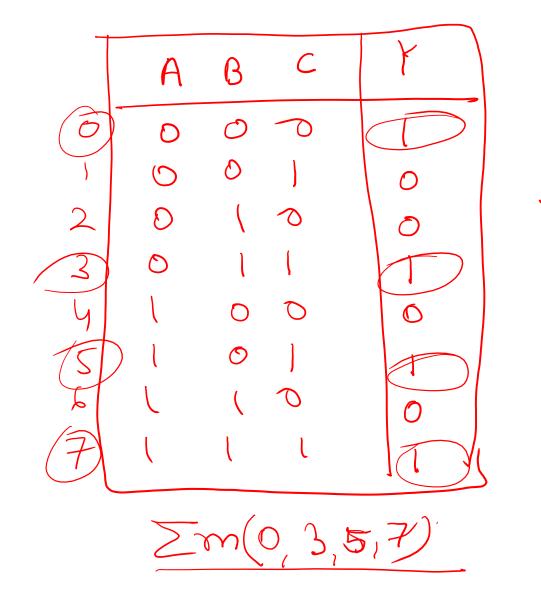
- A POS expression contains:
 - Only AND (product) operations at the "outermost" level
 - Each term (implicate) must be a sum of literals

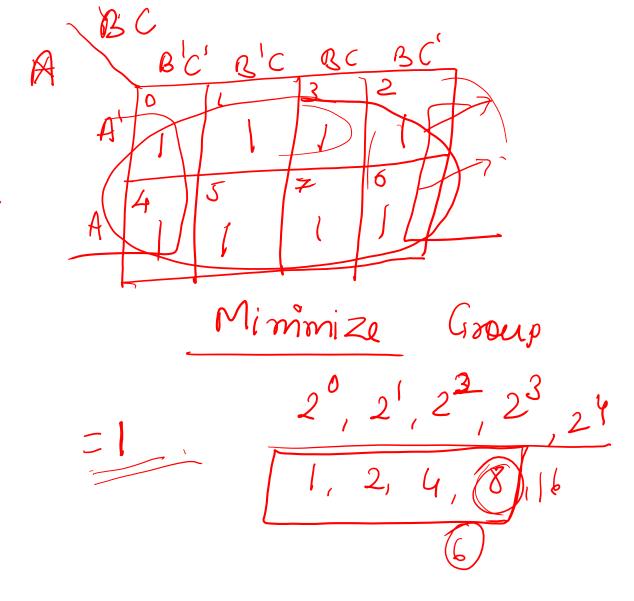
$$f(x,y,z) = (x' + y')(x + y' + z')(x' + y + z')$$

Minimization of Switching Function

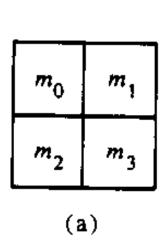


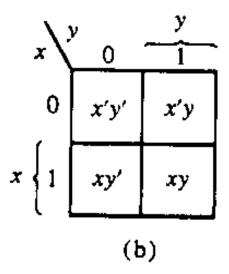


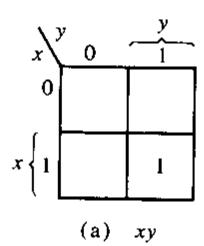


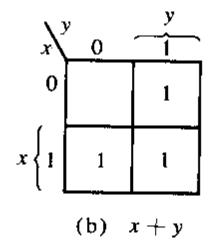


Two variable K Map







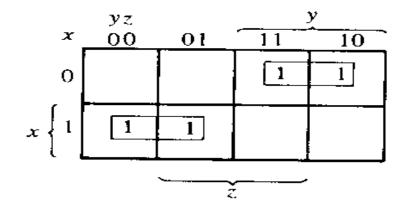


3- variable K-Map

| m ₀ | <i>m</i> 1 | m ₃ | m ₂ |
|----------------|----------------|----------------|----------------|
| m ₄ | m ₅ | m ₇ | m ₆ |

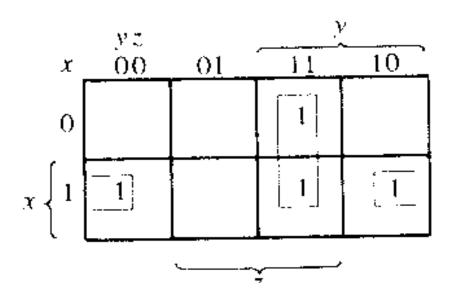
| χ^y | ζ. | | | y ~ |
|------------------------|--------|-------|-------------|--------|
| x \ | 00 | 01 | 11 | 10 |
| 0 | x'y'z' | x'y'z | x'yz | x'yz' |
| $x \left\{ 1 \right\}$ | xy'z' | xy'z | x yz | xyz' |
| . , | | | , | • |

$$F(x, y, z) = \Sigma(2, 3, 4, 5)$$

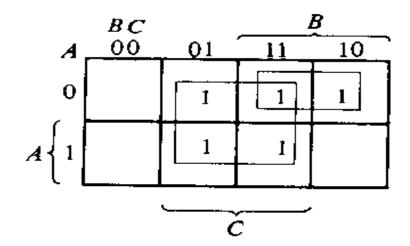


Simplify the Boolean function

$$F(x, y, z) = \Sigma(3, 4, 6, 7)$$

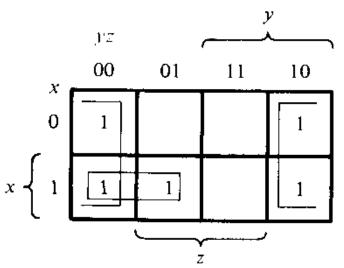


$$F = A'C + A'B + AB'C + BC$$



Simplify the Boolean function

$$F(x, y, z) = \Sigma(0, 2, 4, 5, 6)$$



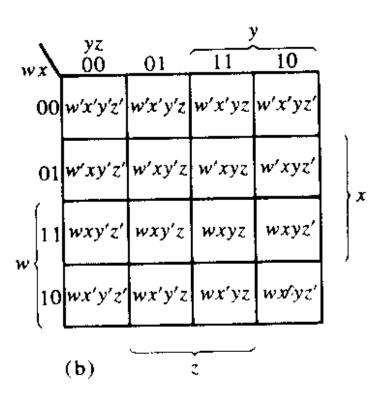
$$\Sigma$$
 (0, 2, 4, 5, 6) = $z' + xy'$

$$A'C + A'B + AB'C + BC = C + A'B$$

4- Variable K-Map

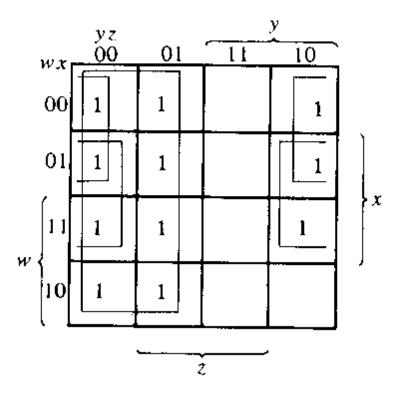
| <i>m</i> ₀ | <i>m</i> ₁ | <i>m</i> ₃ | <i>m</i> ₂ |
|-----------------------|-----------------------|-----------------------|-----------------------|
| ^m 4 | m ₅ | m 7 | <i>m</i> 6 |
| m 12 | m ₁₃ | m 15 | m ₁₄ |
| m 8 | m 9 | m ₁₁ | ^m 10 |

(a)



Simplify the Boolean function

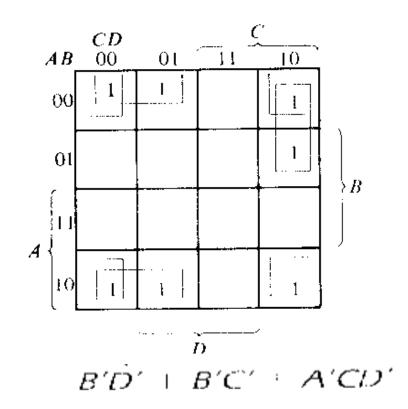
$$F(w, x, y, z) = \Sigma(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$$



$$y' + w'z' + xz'$$

Simplify the Boolean function

$$F = A'B'C' + B'CD' + A'BCD' + AB'C'$$



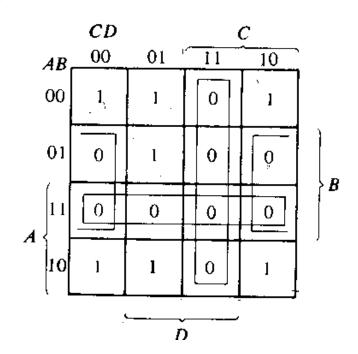
PRODUCT OF SUMS SIMPLIFICATION

Simplify the following Boolean function in (a) sum of products and (b) product of sums.

$$F(A, B, C, D) = \Sigma(0, 1, 2, 5, 8, 9, 10)$$

$$F = B'D' + B'C' + A'C'D$$

$$F = B'D' + B'C' + A'C'D$$
 $F = (A' + B')(C' + D')(B' + D)$



Completely and Incompletely Specified Logic Functions

Logical functions are of two types:

- 1. completely specified logical function
- 2. incompletely specified logical function

A logical function whose output is specified for all possible input combination called completely specified logical function.

A logical function whose output may not be specified for certain input combinations/conditions or for which a certain input combinations may never occur is called incomplete specified logical function.

| Inpu | ıts | | Output |
|------|-----|---|--------|
| Α | В | С | F |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | X |
| 1 | 1 | 1 | X |

Minimization of Incompletely Specified Logic Functions

• For a four bit binary 9's complementary circuit input > 9 is not possible or output for input > 9 is do not care. So, we put the do not care conditions for all WXYZ in the O/P.

$$w = \sum m(0,1) + \sum d(10,11,12,13,14,15) = f(A,B,C,D)$$

$$X = \sum m(2,3,4,5) + \sum d(10,11,12,13,14,15) = f(A,B,C,D)$$

$$Y = \sum m(2,3,6,7) + \sum d(10,11,12,13,14,15) = f(A,B,C,D)$$

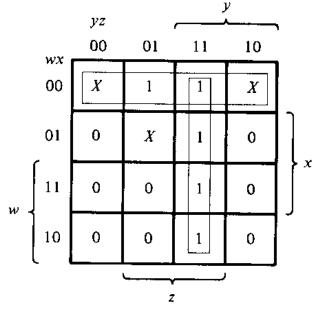
$$Z = \sum m(0,2,4,6,8) + \sum d(10,11,12,13,14,15)$$

Simplify the Boolean function

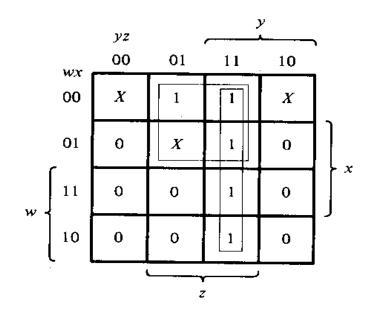
$$F(w, x, y, z) = \Sigma(1, 3, 7, 11, 15)$$

that has the don't-care conditions

$$d(w, x, y, z) = \Sigma(0, 2, 5)$$

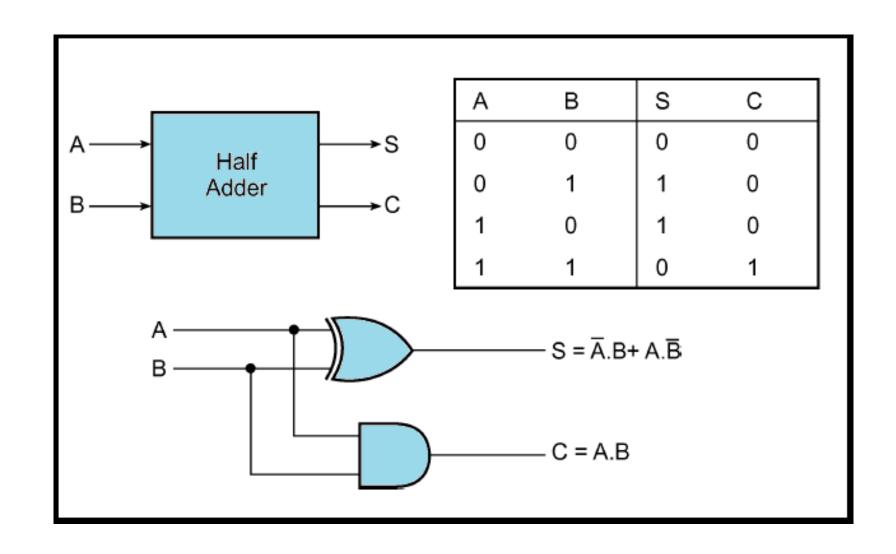


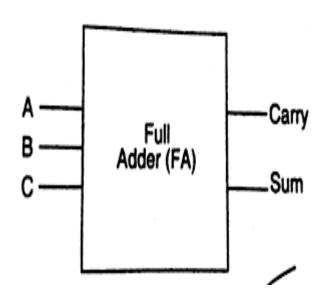
(a)
$$F = yz + w'x'$$



(b)
$$F = yz + w'z$$

Combinational Logic



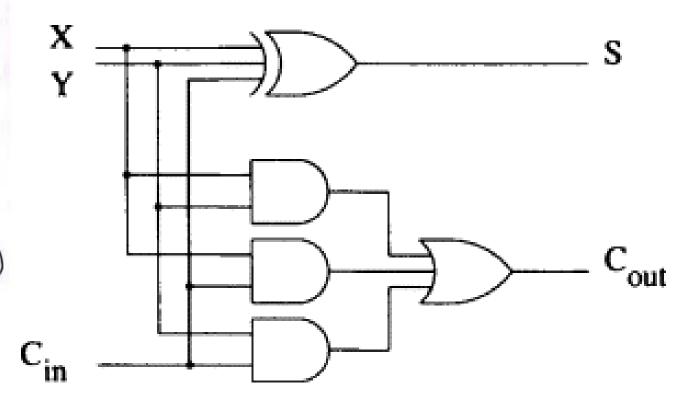


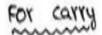
| | Inputs | | | puts |
|---|--------|-----|-----|-------|
| Α | В | Cin | Sum | Carry |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

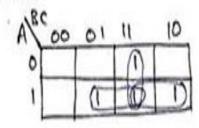


| V/RC | 00 | 01 | 11 | 10 |
|------|----|----|----|----|
| 0 | | 0 | | 0 |
| 1 | 0 | / | 0 | |

$$= \overline{A}(B \oplus c) + A(\overline{B \oplus c}) \qquad (: \overline{X} + X \overline{Y} = X \oplus Y)$$

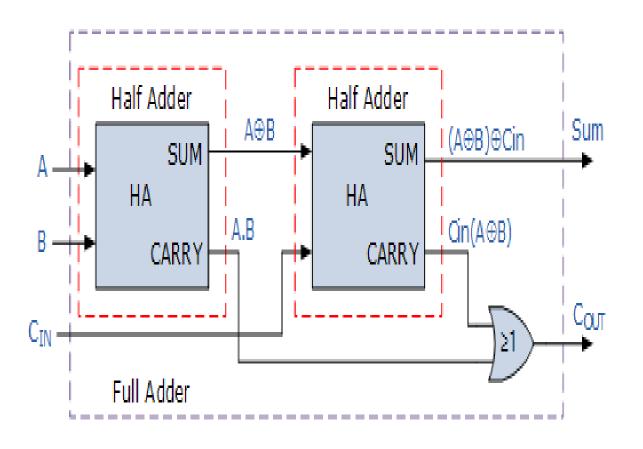


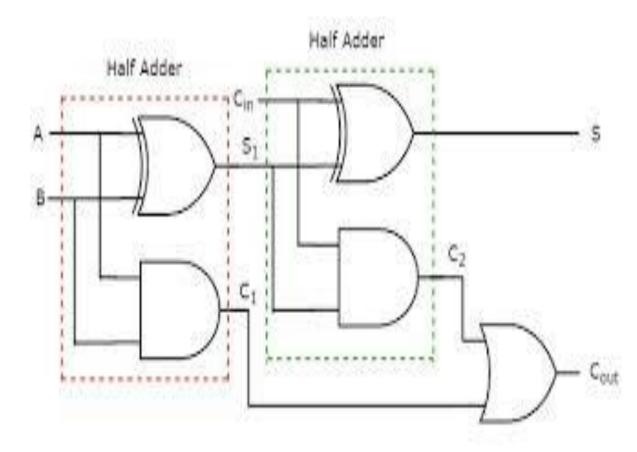




Carry = AB+BC+AC

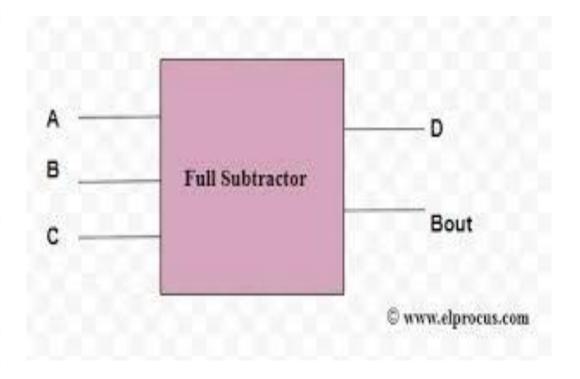
FULL ADDER Using HALF ADDERS





Full Subtractor

| | INPUT | | OUT | PUT |
|---|-------|-----|-----|------|
| A | В | Bin | D | Bout |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |



A O O O O

.. Difference = A @ 0.0 8m

Difference = ABBIN + ABBIN + ABBIN + ABBIN

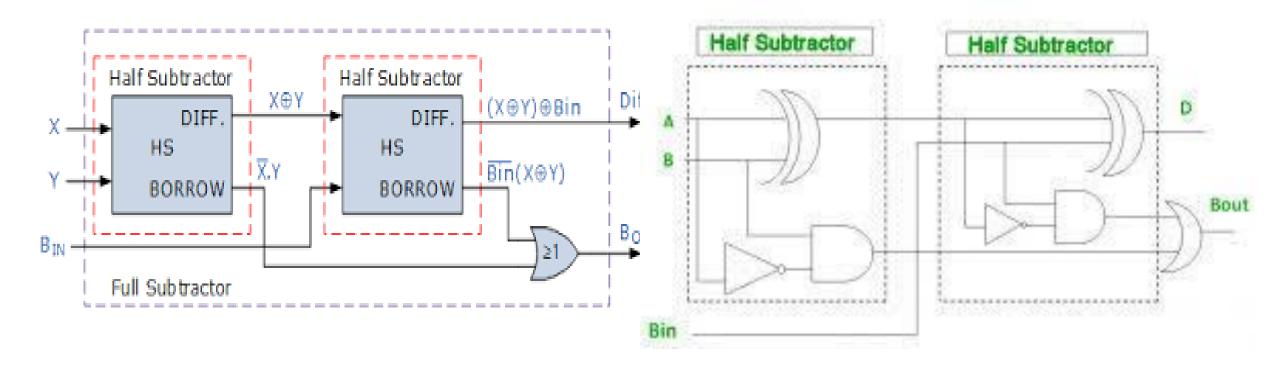
= A(BEIn+BEID) + A(BEIn+BEID)

 $= \overline{A}(B \oplus B_m) + A(B \oplus B_m) = \overline{A}(B \oplus B_m) + A(B \oplus B_m)$

= AGRESIA = AGRESIA

| FOX | Bout | 400 |
|-----|------|-----|
| 4.7 | - | |

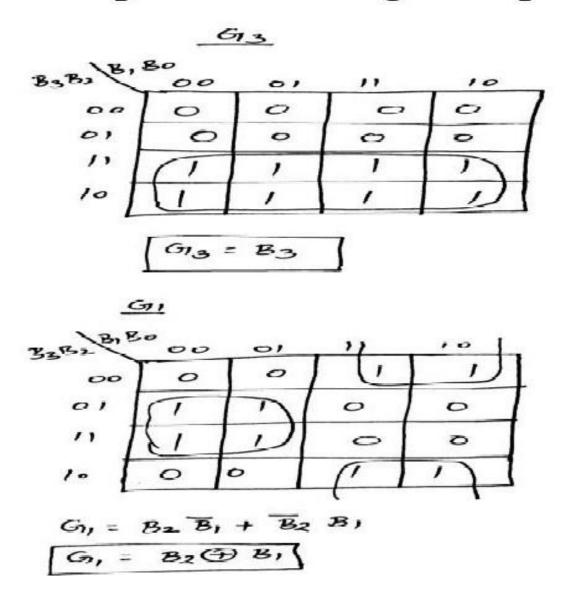
| ABR | 200 | E 0,0 | tt Gin | 880 |
|------|-----|-------|--------|-----|
| A OL | | G | (A) | D |
| A 1 | | | W | |

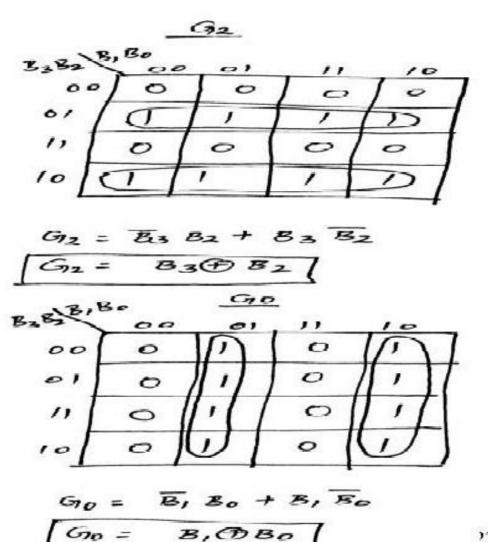


Binary to Gray Code Conversion

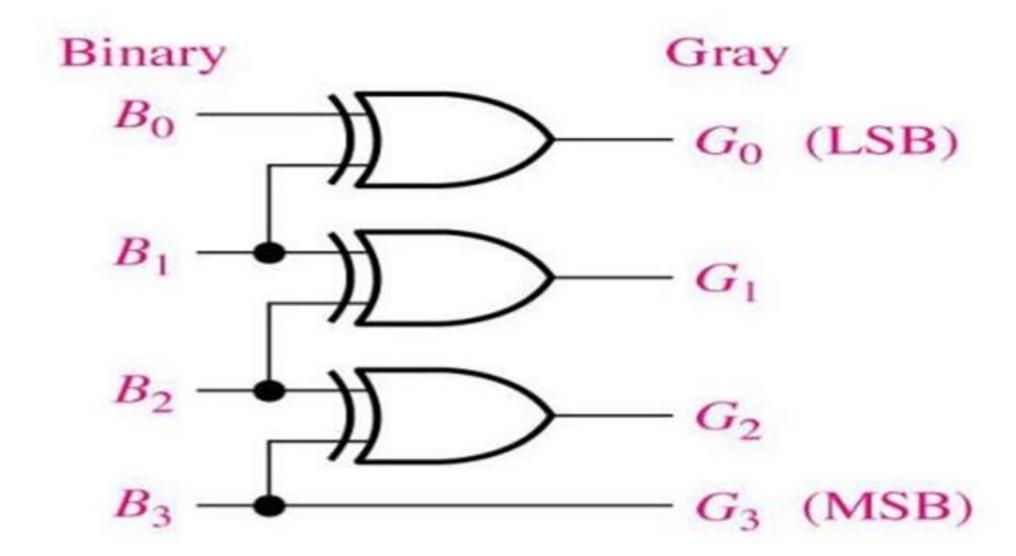
| Decimal Number | 4 bit Binary Number | 4 bit Gray Code |
|----------------|------------------------|--------------------|
| | ABCD | $G_1G_2G_3G_4$ |
| О | 0000 | 0000 |
| 1 | 0001 | 0001 |
| 2 | 0010 | 0011 |
| 3 | 0011 | 0010 |
| 4 | 0100 | 0110 |
| 5 | 0101 | 0111 |
| 6 | 0110 | 0101 |
| 7 | 0111 | 0100 |
| 8 | 1000 | 1100 |
| 9 | 1001 | 1101 |
| 10 | 1010 | 1111 |
| 11 | 1011 | 1110 |
| 12 | 1100 | 1010 |
| 13 | 1101 | 1011 |
| 14 | 1110 | 1001 |
| 15 | 1111 | 1000 |

Simplification using K-maps:





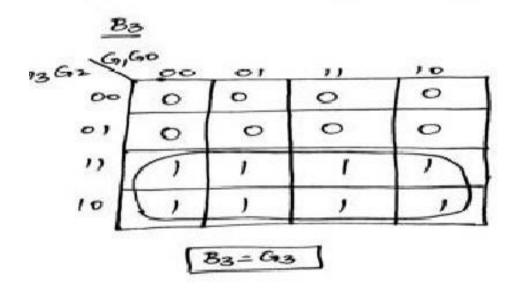
Logic Diagram:



Gray Code to Binary Code Conversion

| Truth | Table: | | | | ļ_ | ↓ ↓ | Binary |
|--------------------|--------|----|---------|----------|-----------|------------|--------|
| INPUT (GRAY CODE) | | | OUTPUTS | (BINARY) | _ o _ o - | | |
| G3 | G2 | G1 | G0 | В3 | B2 | BI | B0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | C |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 |]] |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | C |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | - 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | C |

Simplification using K-Maps:



| 00 | 0 | 10 | 0 | 10 |
|----|---|----|---|----|
| 01 | 0 | , | 1 | 1 |
| " | 0 | 0 | 0 | 0 |
| 10 | 0 | , | 1 | 0 |

| | 8, | | | | | |
|------|----|----|----|----|--|--|
| 6362 | 00 | 01 | ,, | 10 | | |
| 00 | 0 | 0 | Œ | | | |
| 01 | Q | 10 | 0 | 0 | | |
| " | 0 | 0 | C | | | |
| 10 | 0 | 0 | 0 | 0 | | |

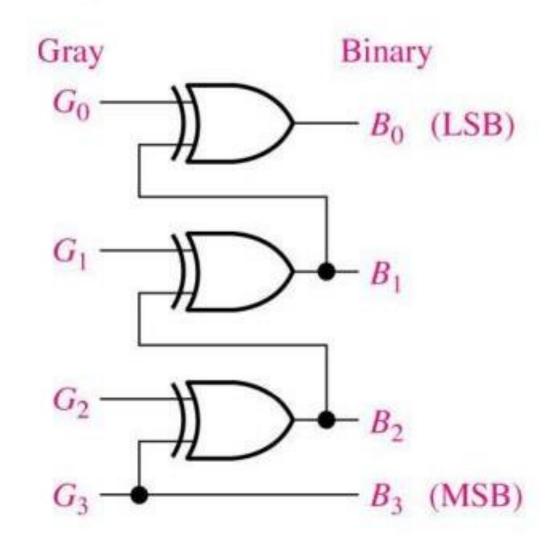
$$B_1 = \overline{G_3} \, \overline{G_2} \, G_1 + G_3 G_2 G_3 + \overline{G_3} G_2 \, \overline{G_3}$$
 $+ G_3 \, \overline{G_2} \, \overline{G_3} \, \overline{G_2} + G_3 \, \overline{G_2} \, \overline{G_3}$
 $= G_1 \, (\, \overline{G_3} \, \overline{G_2} \,) + G_3 \, \overline{G_2} \,)$
 $= G_1 \, (\, \overline{G_3} \, \bigoplus \, G_2 \,) + \overline{G_3} \, (\, \overline{G_3} \, \bigoplus \, G_2 \,)$
 $= G_1 \, (\, \overline{G_3} \, \bigoplus \, G_2 \,) + \overline{G_3} \, (\, \overline{G_3} \, \bigoplus \, G_2 \,)$
 $= G_1 \, \bigoplus \, G_3 \, \bigoplus \, G_2 \,$
 $= G_1 \, \bigoplus \, G_3 \, \bigoplus \, G_2 \,$
 $= G_1 \, \bigoplus \, G_3 \, \bigoplus \, G_2 \,$

Simplification using K-Maps:

Bo

| 12 | 00 | . 01 | . ,, | /(|
|------|----|------|------|----|
| 200 | 0 | , | 0 | 1, |
| », [| , | 0 | , | 0 |
| , [| 0 | , | 0 | , |
| > t | , | 0 | , | 0 |

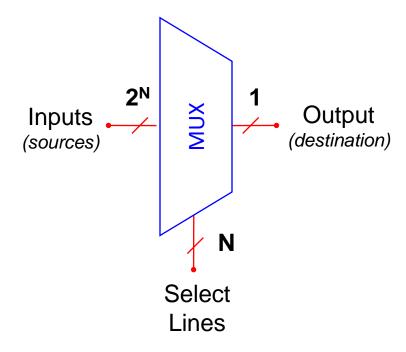
Logic Diagram:



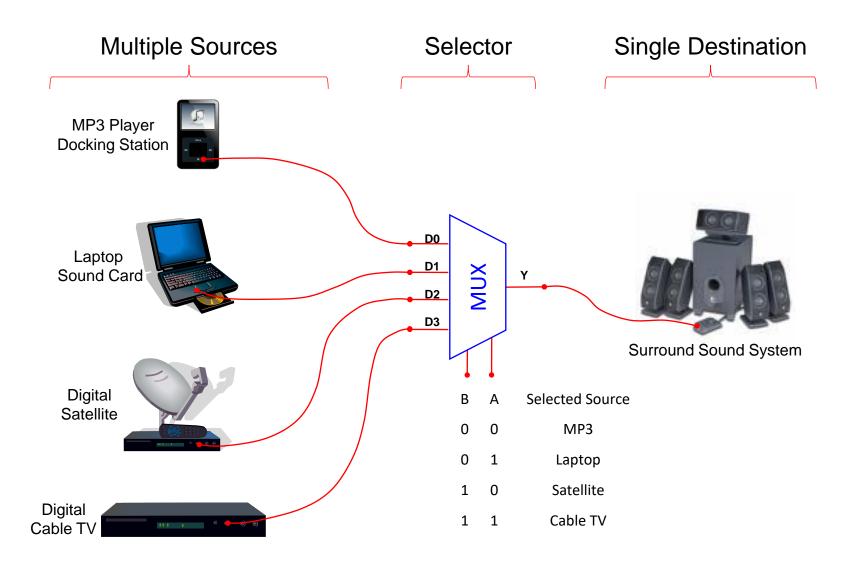
What is a Multiplexer (MUX)?

- A MUX is a digital switch that has multiple inputs (sources) and a single output (destination).
- The select lines determine which input is connected to the output.
- MUX Types
 - \rightarrow 2-to-1 (1 select line)
 - \rightarrow 4-to-1 (2 select lines)
 - → 8-to-1 (3 select lines)
 - → 16-to-1 (4 select lines)

Multiplexer Block Diagram

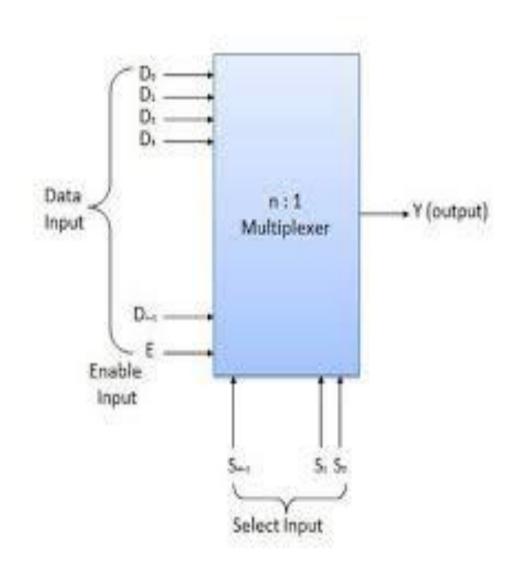


Typical Application of a MUX



Multiplexer/Demultiplexers

- Multiplexing means Generally a (n : 1) multiplexer or a data selector contains the following:
- 1. *n* number of inputs of the multiplexer
- 2. only one output of the multiplexer
- 3. m select/Address lines
- 4. one strobe/enable input (optional)



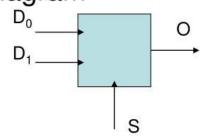
All inputs and outputs should be purely logical or binary input.

For n:1 multiplexer, each input will be selected at the single output at any instant of time, depends upon the input applied to the select/address inputs. Switching circuit connects a particular input to the output.

Here m and n are related by $2^m = n$

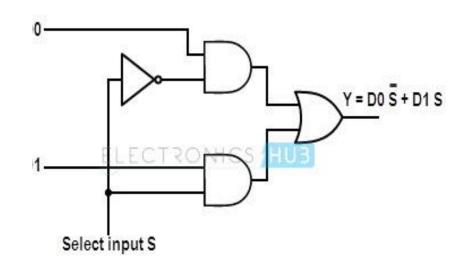
Design of a 2/1 Mux

 2/1 mux Block Diagram

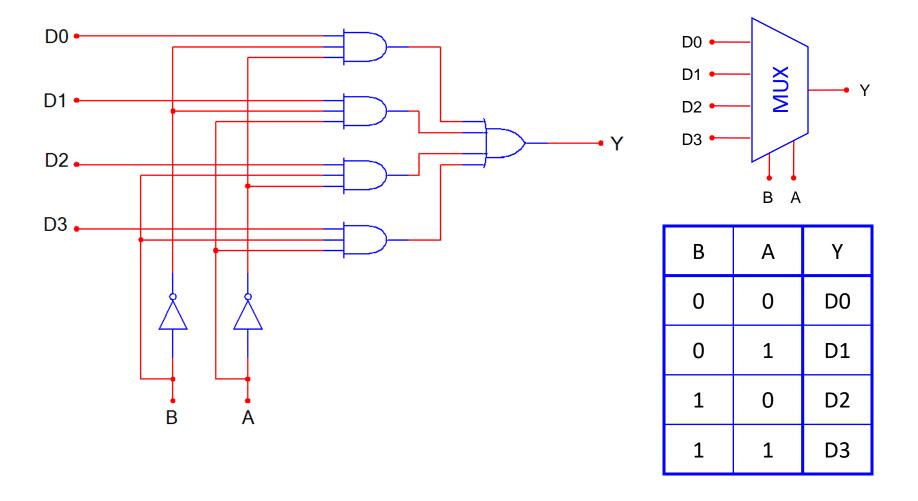


Truth Table

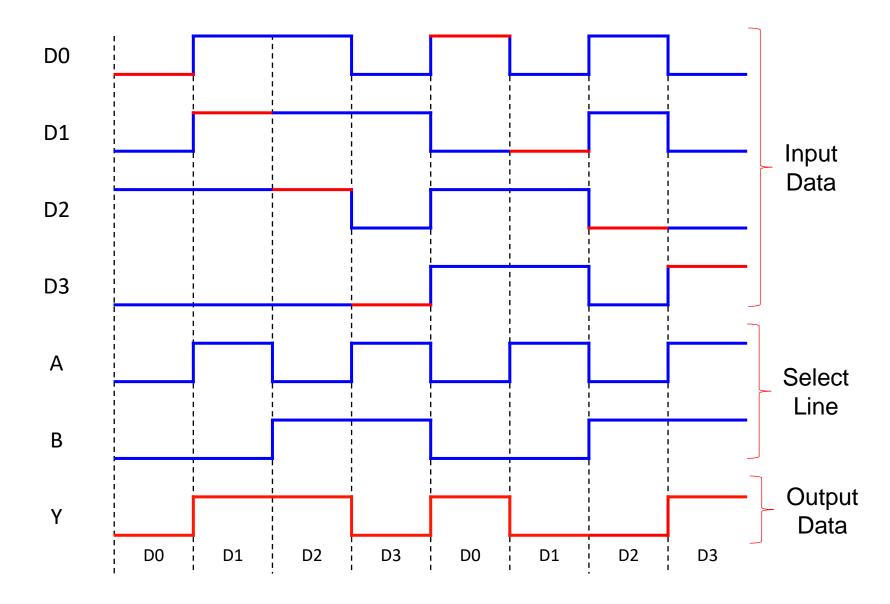
| S | D_1 | D_0 | 0 |
|---|-------|-------|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 4 | 1 | 1 |



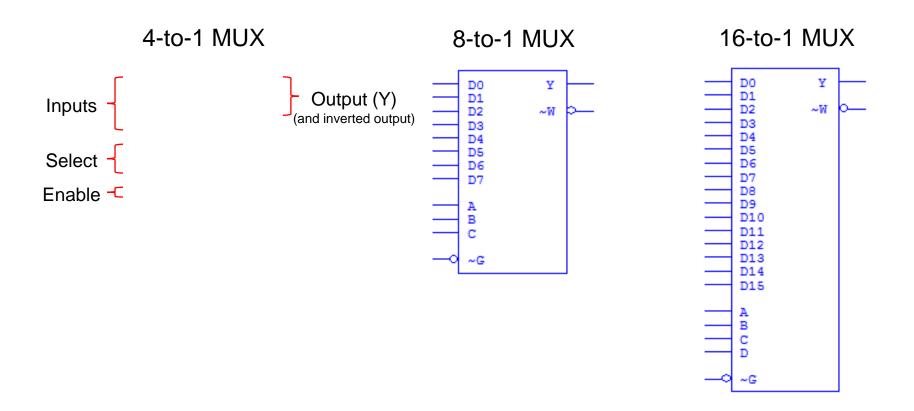
4-to-1 Multiplexer (MUX)



4-to-1 Multiplexer Waveforms



Medium Scale Integration MUX

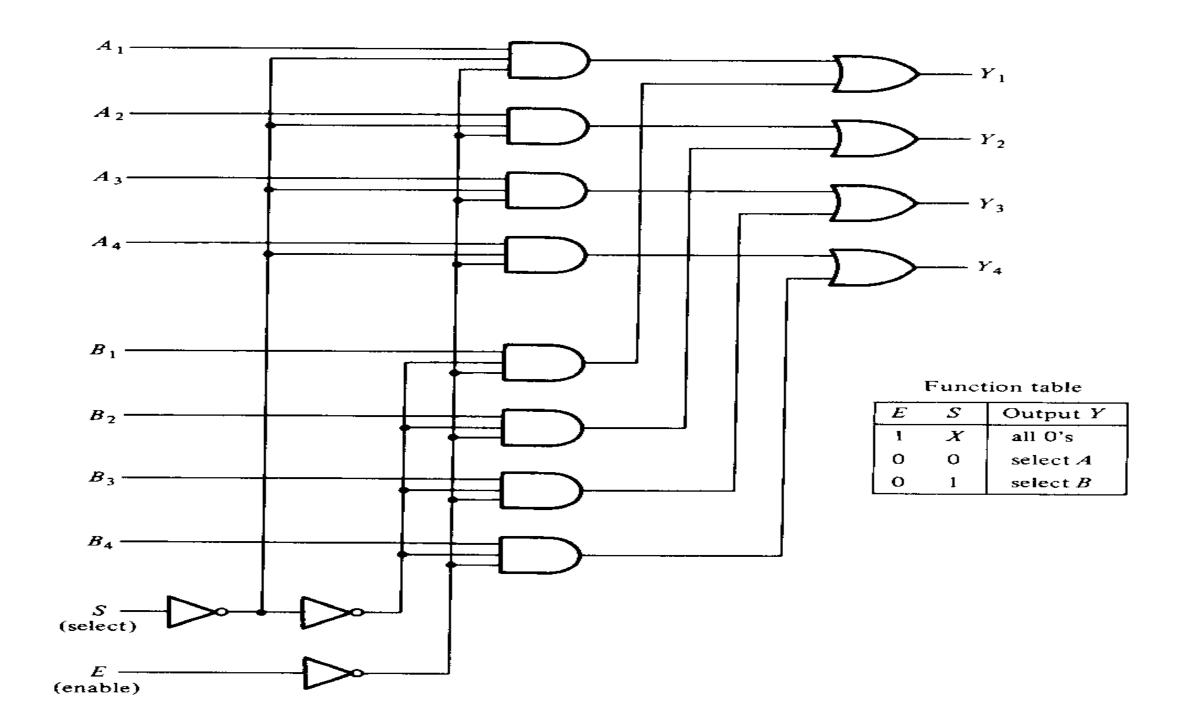


When two or more MUX are enclosed with in single chip

Selection and enable inputs in multiple unit IC may be common to all multiplexers. A Quadruple 2 to 1 line multiplexer IC is shown here.

It has 4 MUX each capable of selecting one of 2 input lines.

O/P Y1 can be selected to be equal to either A1 or B1..similarly others



Boolean Function Implementation

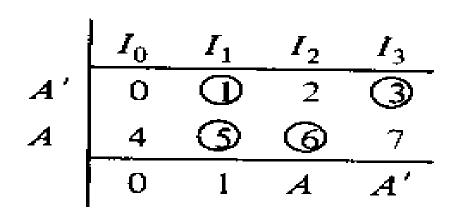
For implementing any Boolean function of n variable with 2ⁿ to 1 MUX is possible. However more optimize way is also there.

If we have Boolean function of n+1 variable then out of it 1 is used for input data and rest n are used as select I/P.

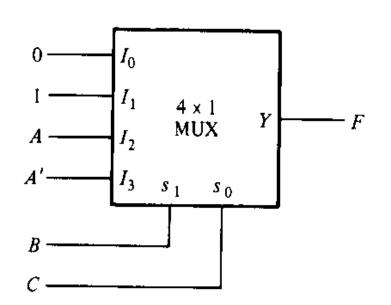
If A is a single variable then input of MUX are to be chosen either A or A' or 1 or 0.

By judicious use of these four values to inputs and others as select I/P variables one can implement any Boolean function of n+1 variables using 2ⁿ to 1 MUX.

$$F(A, B, C) = \Sigma(1, 3, 5, 6)$$



(c) Implementation table



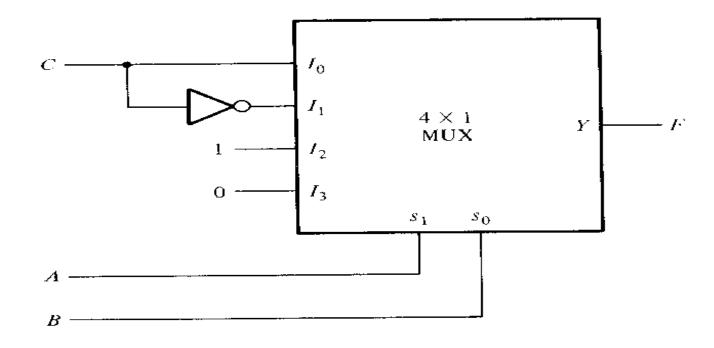
| Minterm | A | В | С | F |
|---------|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 1 | l | 1 |
| 4 | l | 0 | 0 | 0 |
| 5 | 1 | 0 | 1 | 1 |
| 6 | 1 | 1 | 0 | 1 |
| 7 | 1 | l | 1 | 0 |

(a) Multiplexer implementation

(b) Truth table

$$F(A, B, C) = \Sigma(1, 2, 4, 5)$$

| A | B | C | F | |
|---|---|---|---|--------------|
| 0 | 0 | 0 | 0 | F = C |
| О | 0 | 1 | 1 | <i>F</i> C |
| 0 |] | 0 | 1 | F = C' |
| 0 | 1 | 1 | O | <i>r</i> = 0 |
| 1 | 0 | 0 | 1 | F = 1 |
| 1 | O | 1 | ì | F - 1 |
| 1 | 1 | O | 0 | F = 0 |
| l | 1 | 1 | 0 | <i>I</i> = 0 |



(a) Truth table

(b) Multiplexer implementation

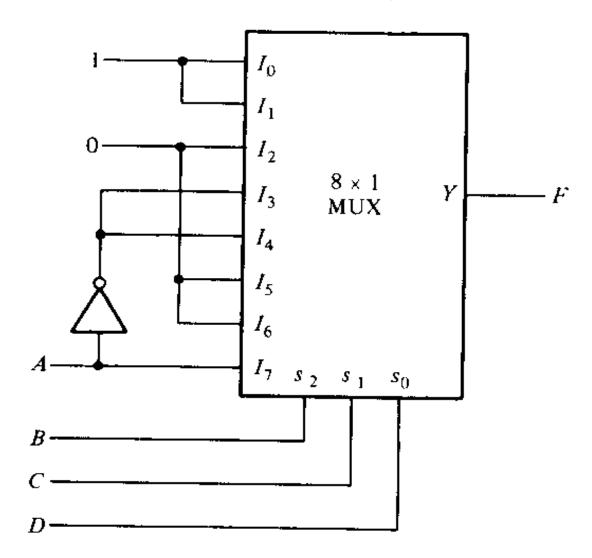
| | I_0 | I_1 | I_2 | I_3 |
|----|-------|-------|-------|-------|
| C' | 0 | 2 | 4 | 6 |
| C | 1 | 3 | 5 | 7 |
| | С | C' | 1 | 0 |

(c) Implementation table

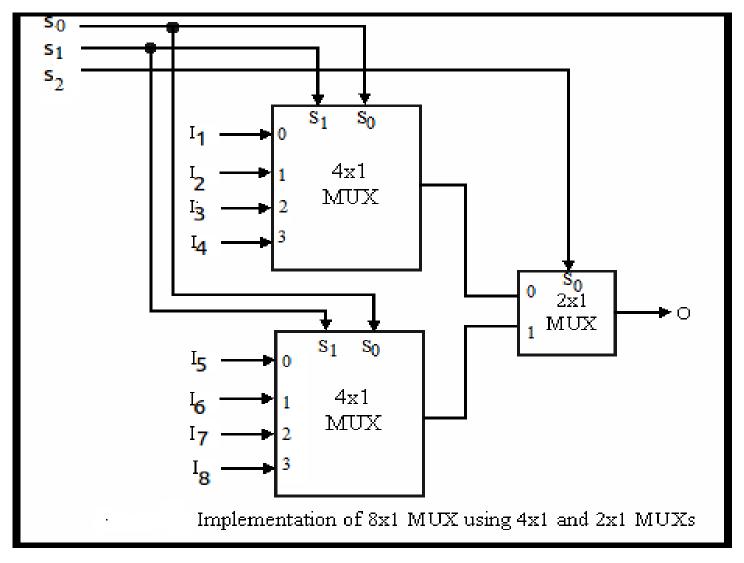
Implement the following function with a multiplexer:

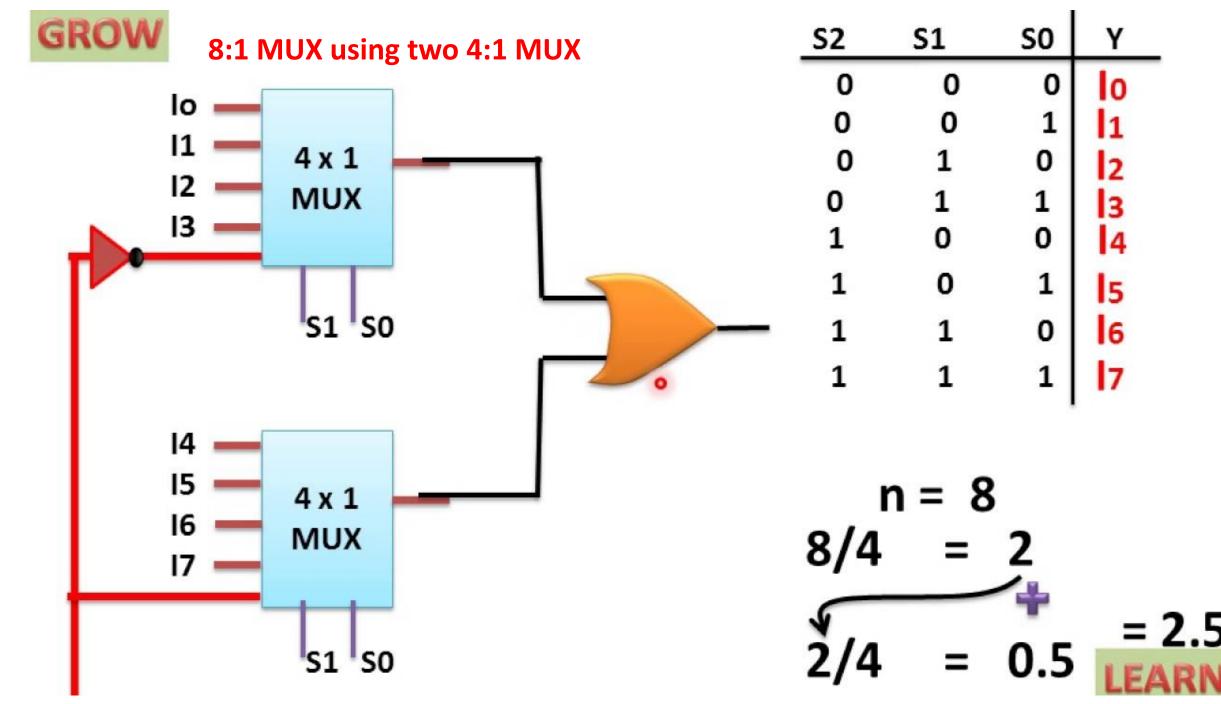
$$F(A, B, C, D) = \Sigma(0, 1, 3, 4, 8, 9, 15)$$

| | I_0 | 1 ₁ ① ③ | I_2 | I_3 | I_4 | I_5 | I_6 | I_7 |
|----|-------|--------------------|-------|-------|-----------------|-------|-------|-------|
| A' | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| A | 8 | 9 | 10 | 11 | 12 | 13 | 14 | (3) |
| | 1 | 1 | 0 | A' | $\overline{A'}$ | 0 | 0 | Ā |



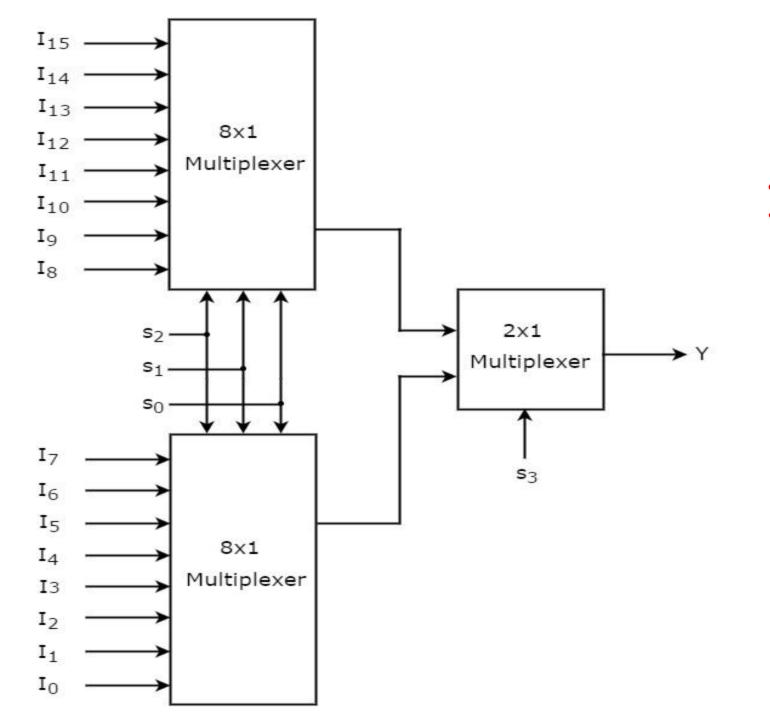
Higher order MUX 8:1 MUX using 4:1 MUXs





16:1 MUX using 4:1 MUX

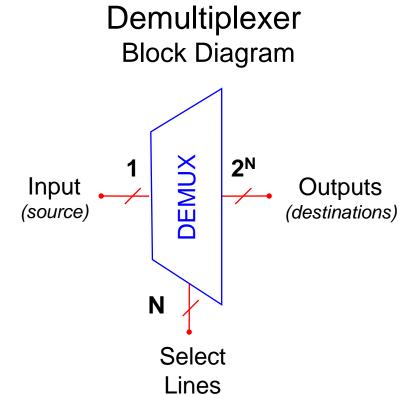
Inputs 11 -**4X1** MUX 12 -13 -**S**1 so 14 -4X1 15 -MUX 17 -**4X1** Output SO **S1** MUX (f) 18 S3 **S2 4X1** 19 MUX 110 111-SO **S1** 112-113-**4X1** MUX 114 115-**S**1 SO



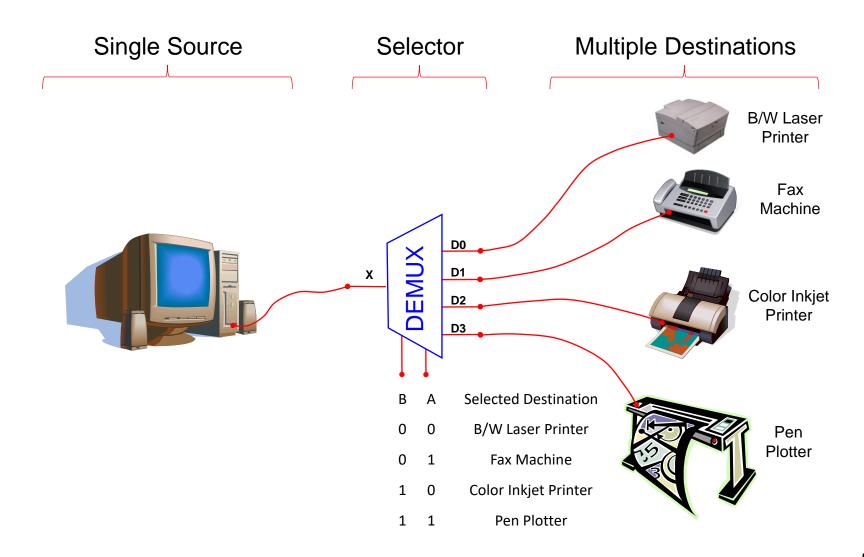
16:1 MUX using 8:1 MUX

What is a Demultiplexer (DEMUX)?

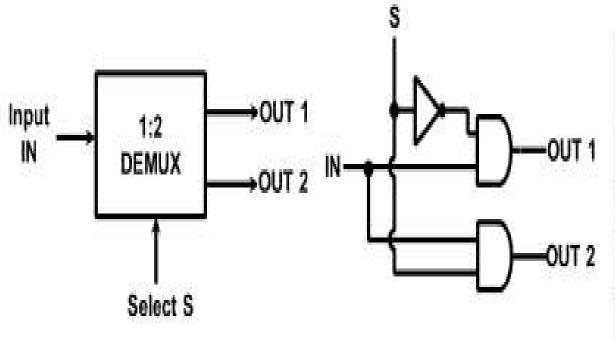
- A DEMUX is a digital switch with a single input (source) and a multiple outputs (destinations).
- The select lines determine which output the input is connected to.
- DEMUX Types
 - \rightarrow 1-to-2 (1 select line)
 - \rightarrow 1-to-4 (2 select lines)
 - \rightarrow 1-to-8 (3 select lines)
 - \rightarrow 1-to-16 (4 select lines)



Typical Application of a DEMUX



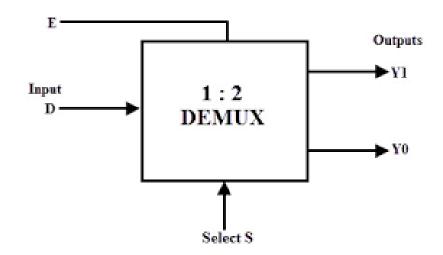
1: 2 Demux

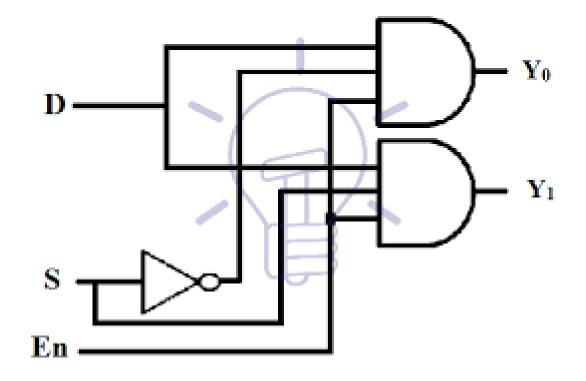


| Select (S) | Input (IN) | Out 1 | Out 2 |
|---------------|---------------|-------|-------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 |

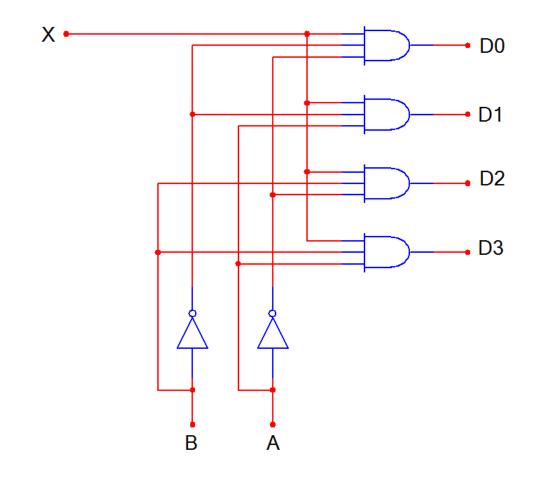
| Enable | Select | Out | out |
|--------|--------|-----|-----|
| E | S | YO | Y1 |
| 0 | x | 0 | 0 |
| 1 | 0 | 0 | Din |
| 1 | 1 | Din | 0 |

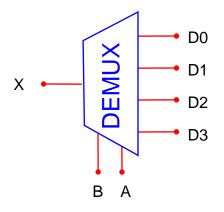
x = Don't care





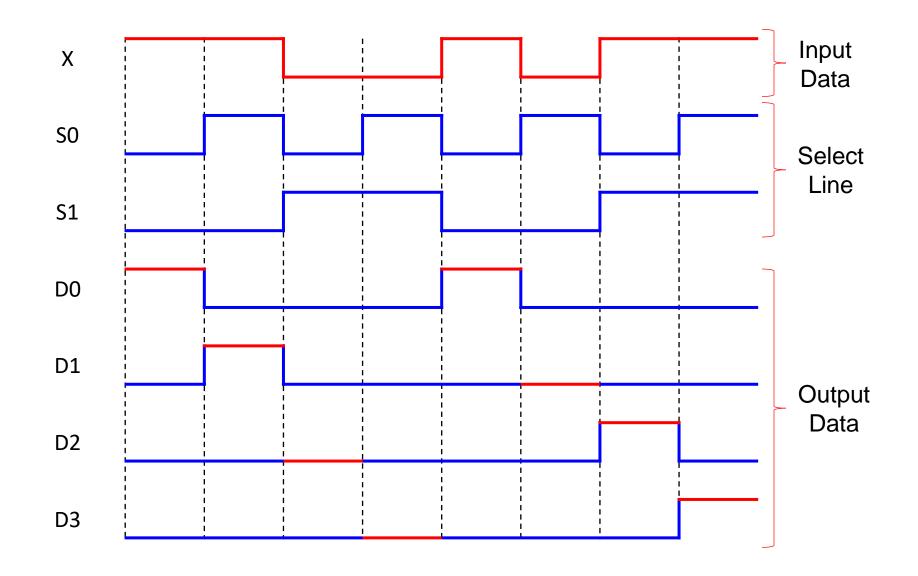
1-to-4 Demultiplexer (DeMUX)



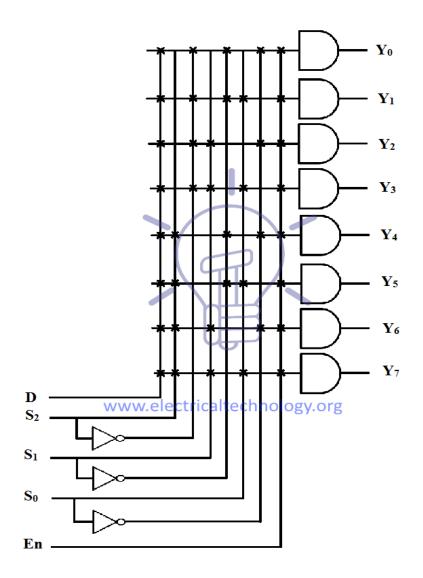


| В | А | D0 | D1 | D2 | D3 |
|---|---|----|----|----|----|
| 0 | 0 | Х | 0 | 0 | 0 |
| 0 | 1 | 0 | Х | 0 | 0 |
| 1 | 0 | 0 | 0 | Х | 0 |
| 1 | 1 | 0 | 0 | 0 | Χ |

1-to-4 De-Multiplexer Waveforms

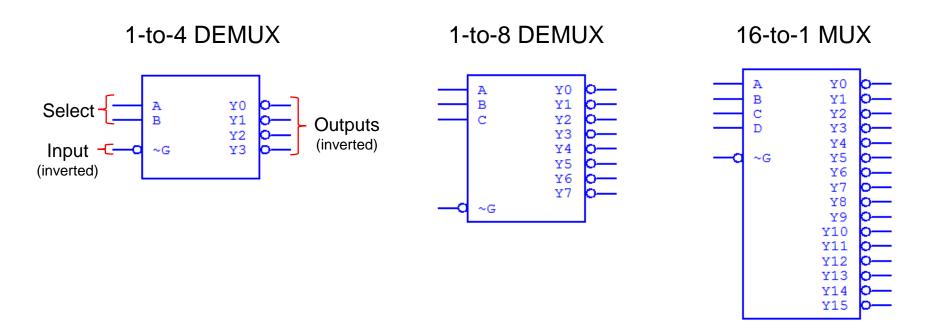


1:8 Demux with Enable Input



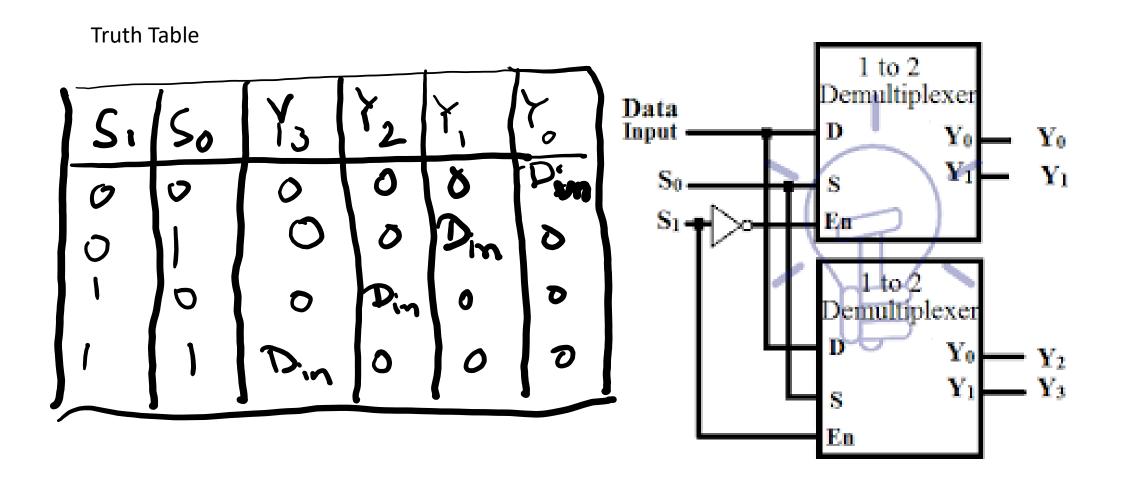
| | INPUT OUTPUT | | | | | | OUTP | | | | | |
|----|--------------|------|----------------|----------------|----|--------------|----------------|-------|----------------|----|----------------|-----------------------|
| En | D | S2 | S ₁ | So | Yo | Υ1 | Y ₂ | Y_3 | Y ₄ | Ys | Y ₆ | Y ₇ |
| 0 | Х | Х | Х | Х | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | Х | 0 | 0 | 0~ | Þ | 0 | 10- | -0 | 0 | 0 | 0 | 0 |
| 1 | Х | 0 | 0 | 1 | 0_ | _ D] | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | Х | 0 | 1 | 0 | 0 | 0 | D | 0 | 0 | 0 | 0 | 0 |
| 1 | Х | 0 | 1 | 1 | Ò | 0 | 0 | D | 0 | 0 | 0 | 0 |
| 1 | Х | 1 | 0 | 0 | 0 | 0 | 0 | 0 | D | 0 | 0 | 0 |
| 1 | Х | 1,,, | 0 | ai l ic | 0. | 0. | Q.l | Q., | 0 | D | 0 | 0 |
| 1 | Х | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | D | 0 |
| 1 | Х | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | D |

Medium Scale Integration DEMUX

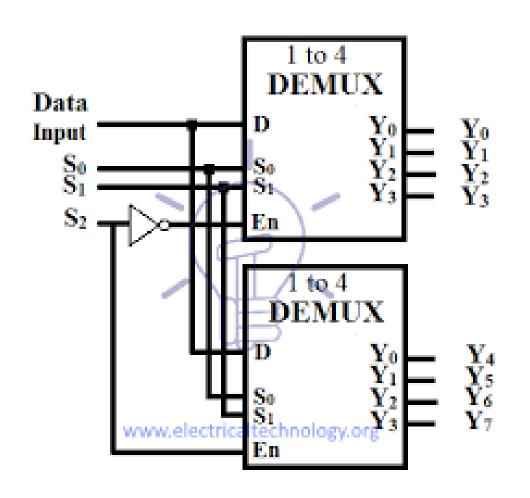


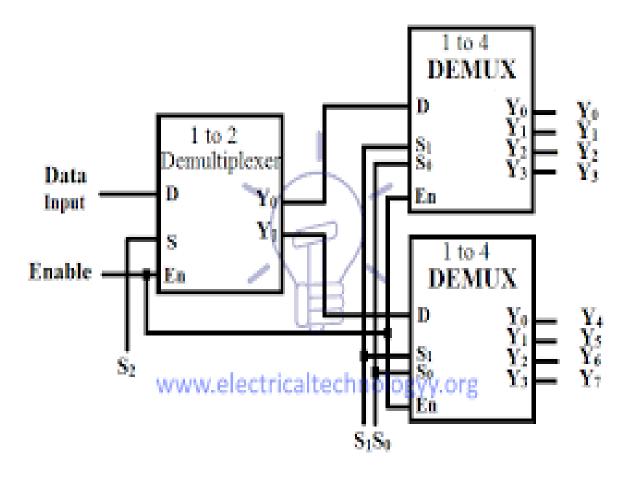
Note: Most Medium Scale Integrated (MSI) DEMUXs, like the three shown, have outputs that are inverted. This is done because it requires few logic gates to implement DEMUXs with inverted outputs rather than no-inverted outputs.

Demultiplxer Tree 1:4 using 1:2 Demux

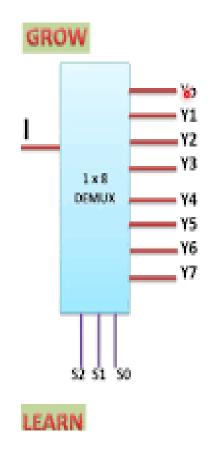


1:8 DeMUX Using 1:4





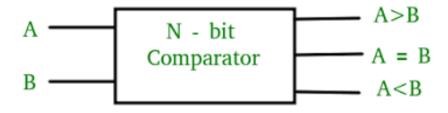
Full Adder using 1:8 De MUX



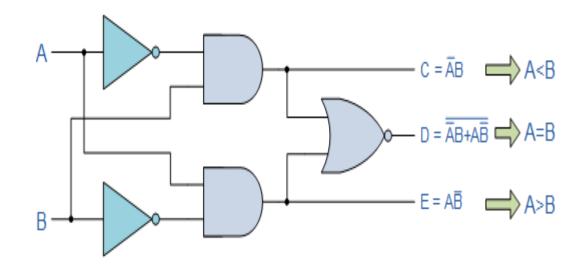
 $D(x,y,z) = \Sigma m(1,2,4,7)$ $B(x,y,z) = \Sigma m(1,2,3,7)$ Y0 Y1 **Y2** 1:8 **Y3** DEMUX Din = 1**Y4** Bout Y7 S1 S2 S0

Draw 1:64 demultiplexer using 1:16 demux and 1:4 demux

Comparator



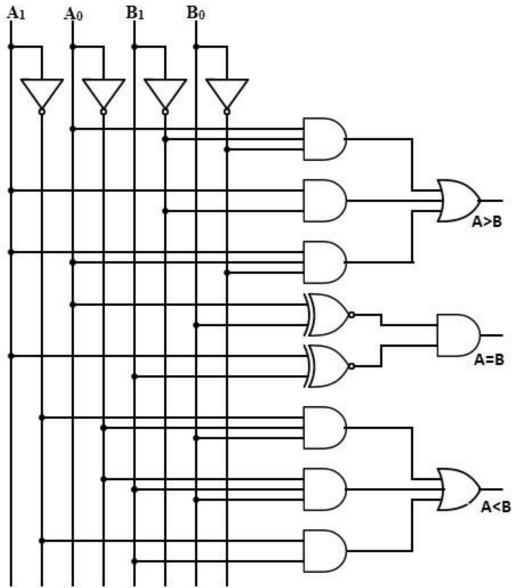
| A | В | A <b< th=""><th>A=B</th><th>A>B</th></b<> | A=B | A>B |
|---|---|--|-----|-----|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |

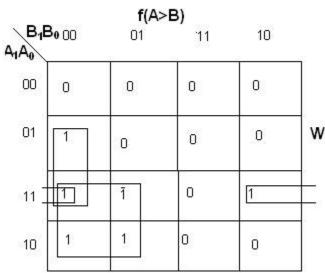


2-Bit Magnitude Comparator

Table 1. Truth Table of 2-Bit Magnitude Comparator

| INPL | T | | OUTE | TU | | |
|------|----|----|------|-----|-----|-------------------|
| A1 | A0 | B1 | В0 | A>B | A=B | A <b< th=""></b<> |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |



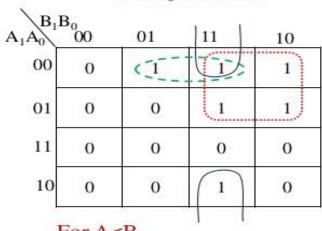


We get the equation as f(A>B)

$$= A_1 \overline{B}_1 + A_0 \overline{B}_1 \overline{B}_0 + A_1 A_0 \overline{B}_0$$

K-Map for A<B:

K-Map for A=B:



| $A \rightarrow B_1 I$ | 30 | | | |
|-----------------------|----|----|----|----|
| $A_1 A_0 B_1 I$ | 00 | 01 | 11 | 10 |
| 00 | 1 | 0 | 0 | 0 |
| 01 | 0 | 1 | 0 | 0 |
| 11 | 0 | 0 | 1 | 0 |
| 10 | 0 | 0 | 0 | 1 |

For A<B

$$\mathbf{Y}_{\scriptscriptstyle 1} = \overline{\mathbf{A}_{\scriptscriptstyle 1}} \; \overline{\mathbf{A}_{\scriptscriptstyle 0}} \; \mathbf{B}_{\scriptscriptstyle 0} + \overline{\mathbf{A}_{\scriptscriptstyle 1}} \; \mathbf{B}_{\scriptscriptstyle 1} + \overline{\mathbf{A}_{\scriptscriptstyle 0}} \; \mathbf{B}_{\scriptscriptstyle 1} \; \mathbf{B}_{\scriptscriptstyle 0}$$

For A=B

$$Y_2 = \overline{A_1} \; \overline{A_0} \; \overline{B_1} \; \overline{B_0} + \overline{A_1} \; A_0 \; \overline{B_1} \; B_0 + A_1 A_0 B_1 B_0 + A_1 \; \overline{A_0} \; B_1 \; \overline{B_0}$$

Binary Serial Adder

Let Register-1 hold the first number and register 2 holds the other no.

The D FF is cleared initially so Q=0 and Cin= 0.

The serial o/p (SO) of the two registers will provide the LSBs of the two number.

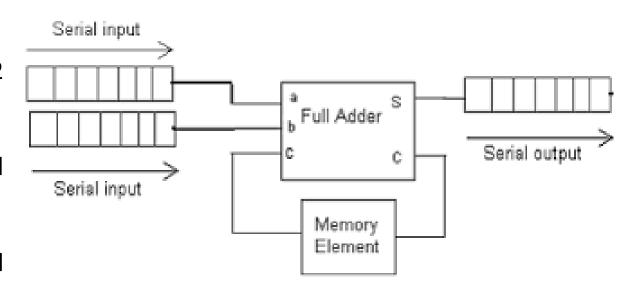
They will act bits a and b for full adder.

The FA will add these bits and produce sum and carry out Co.

Thus addition of LSB is complete.

Now a clock pulse is applied to both the shift registers.

Hence the two numbers are right shifted by one bit each.



The clock pulse gets applied to the D FF also and Q= Cin = Cout =0. The adder adds the two bits available at the SO outputs of the two registers

Advantages

The addition of a pair of bits only takes place at any instant of time

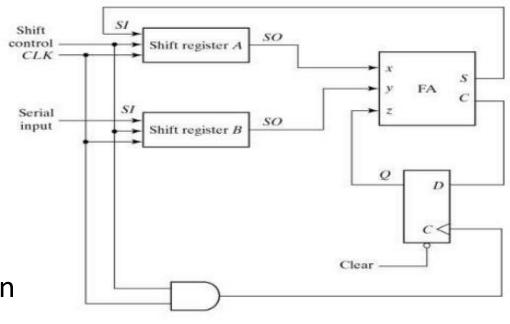
(n-1) number of clock cycles are required to complete the addition

The process of addition continues until the shift right control is disabled
Sum is available in the serial form

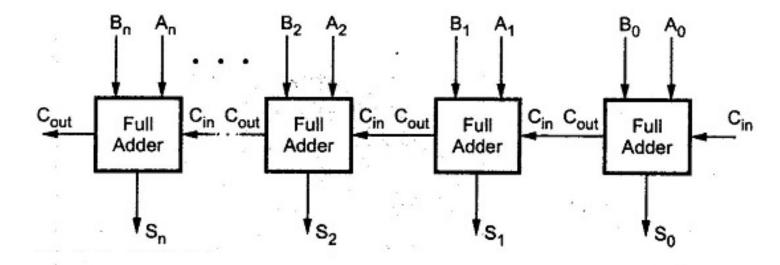
Drawback

- i) More time is required to complete the addition
- ii) A complicated ckt is required
- iii) The ckt contains more no of components
- iv) The Sum and Carry are available in the serial form hence result can't be observed at once.

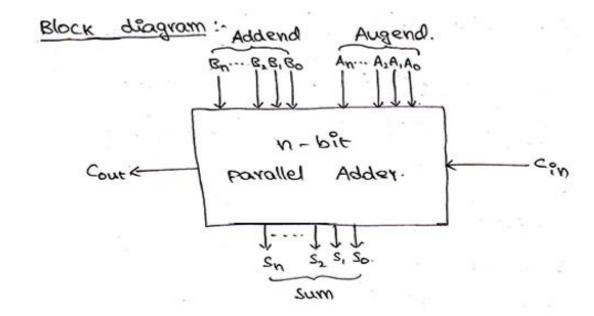
Fig: Serial Adder



Binary Parallel Adder



N-Bit Parallel Adder



Cascading of Adders

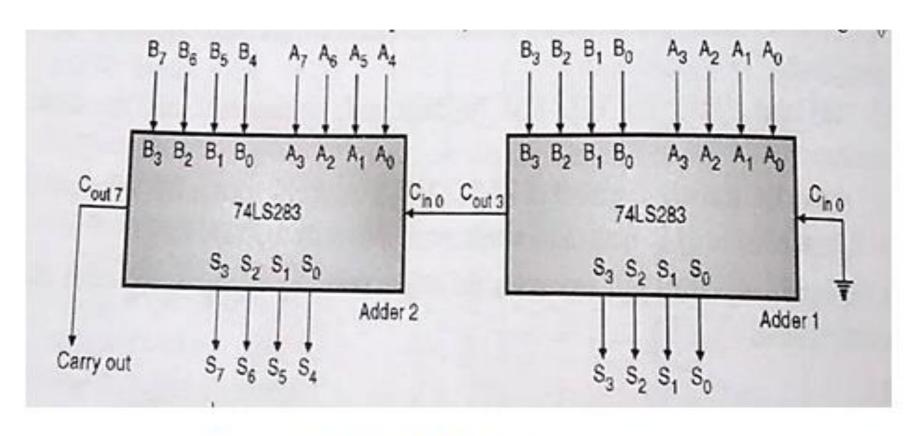
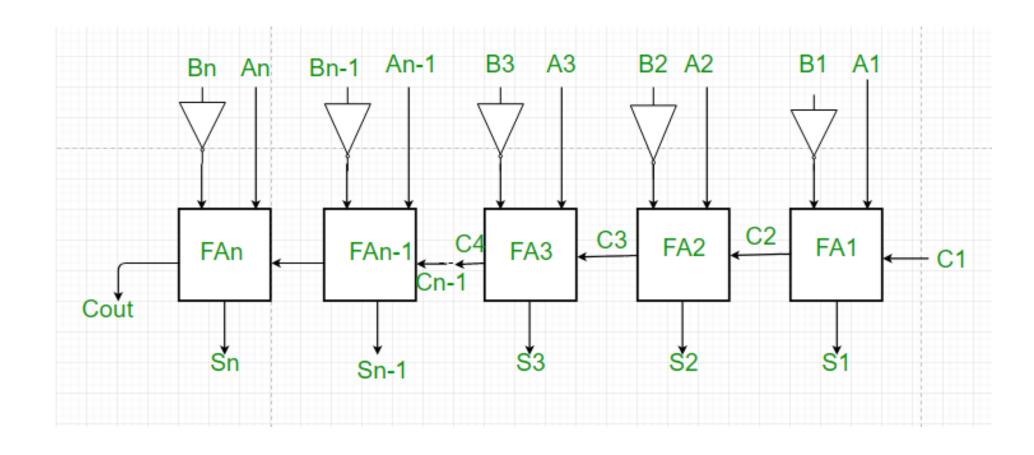


Fig2. Cascading of two IC 7483s

Binary Parallel Subtractor



Propagation delay in Parallel adder