ASSIGNMENT-11

U19CS012

1.) Design and Implement *MOD-12 Counter* in Multisim using JK Flip-Flops.

A.) Solution:

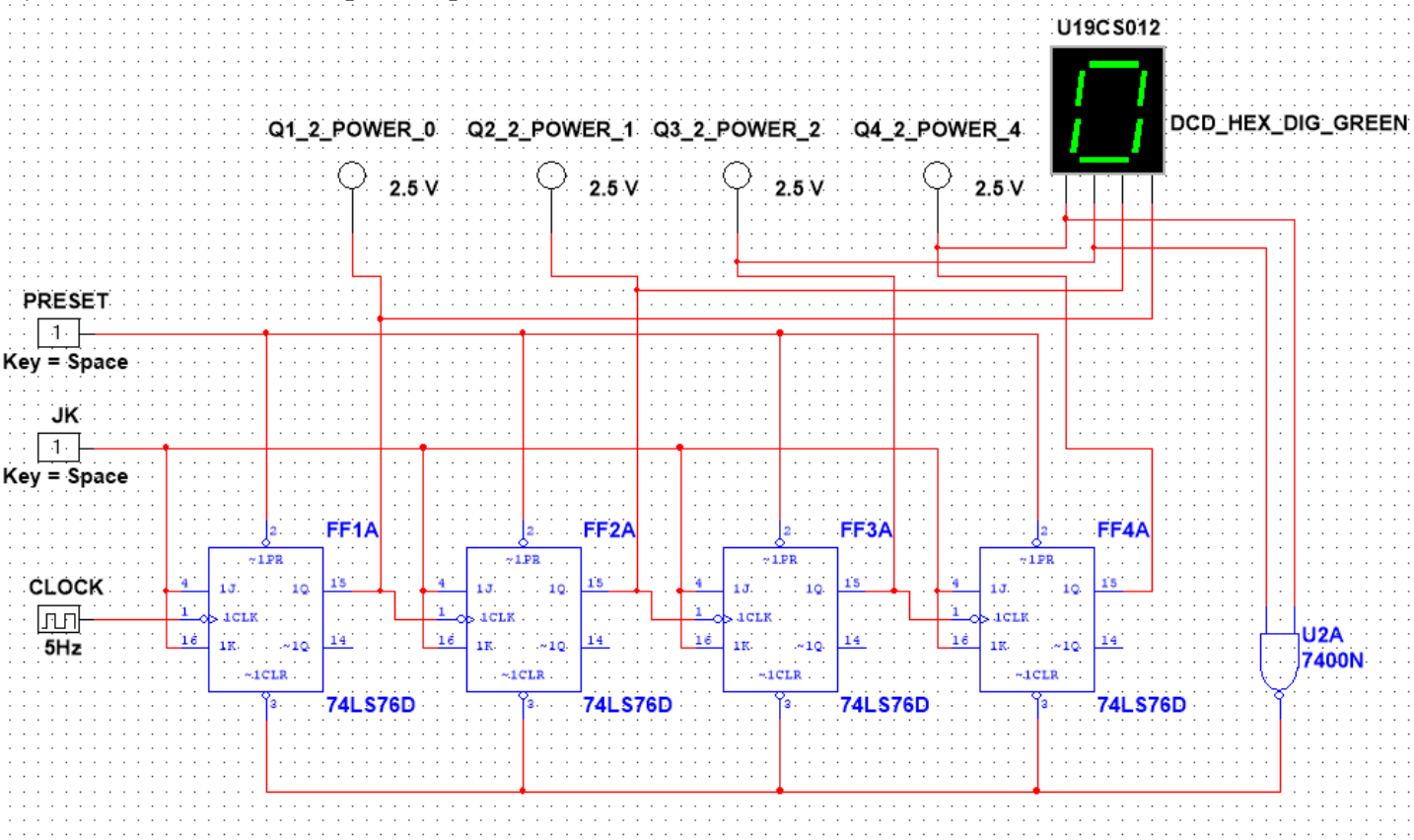
A MOD-12 Counter would be having **12** Valid States from 0 [0000] to 11 [1011].

We will make 4-Bit Full Counter [0-15] and Try to Reduce Valid States to **12**[0-11] using Additional NAND Gate that will take *Clear All Bits* as the Value in Counter turns out to be 12 [1100] i.e. When *First Two Bits Become One*, we will Clear all Bits.

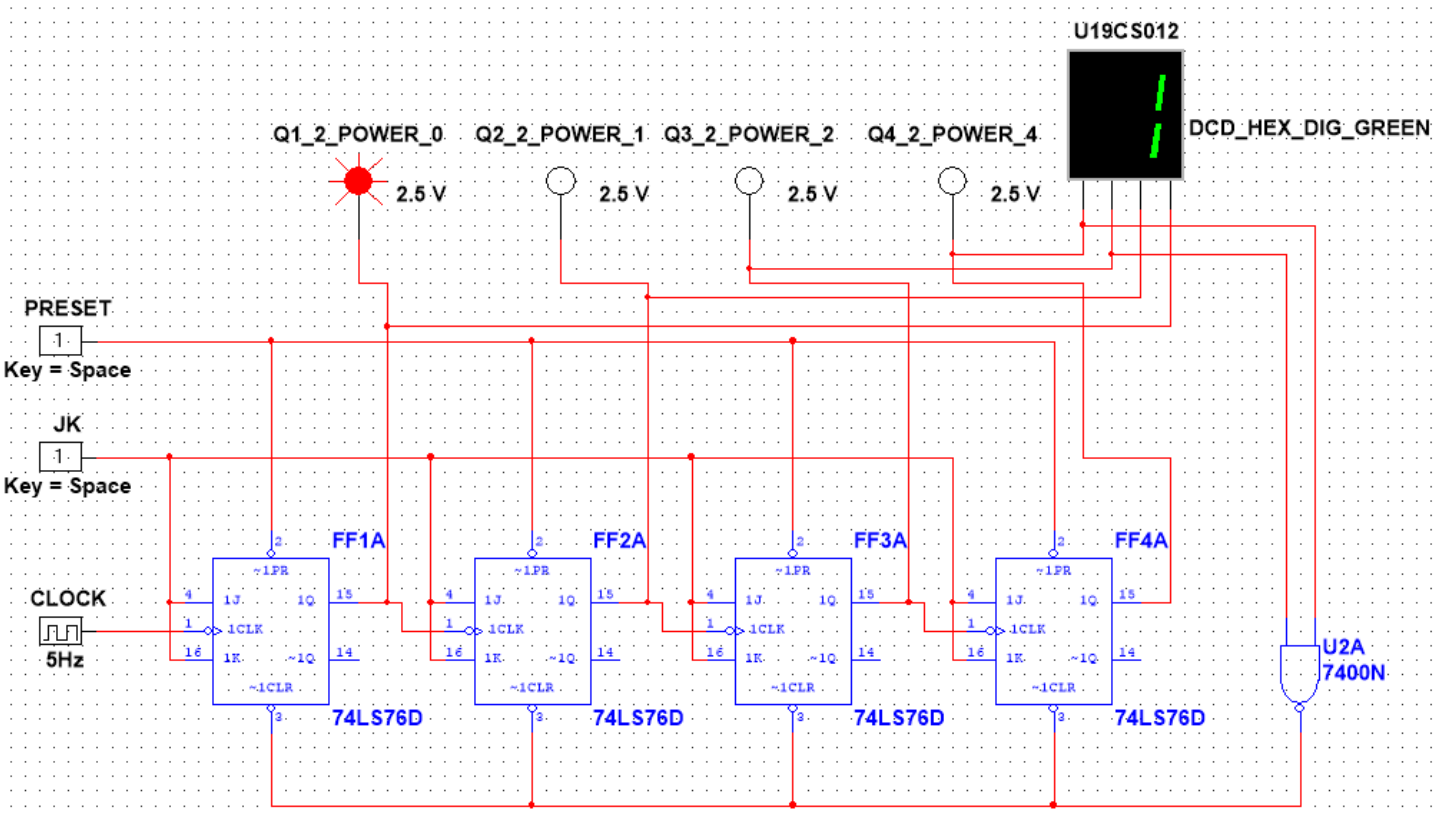
The Concept is Similar to MOD-7 Counter Implemented Earlier in Practical 11.

B.) Implementation:

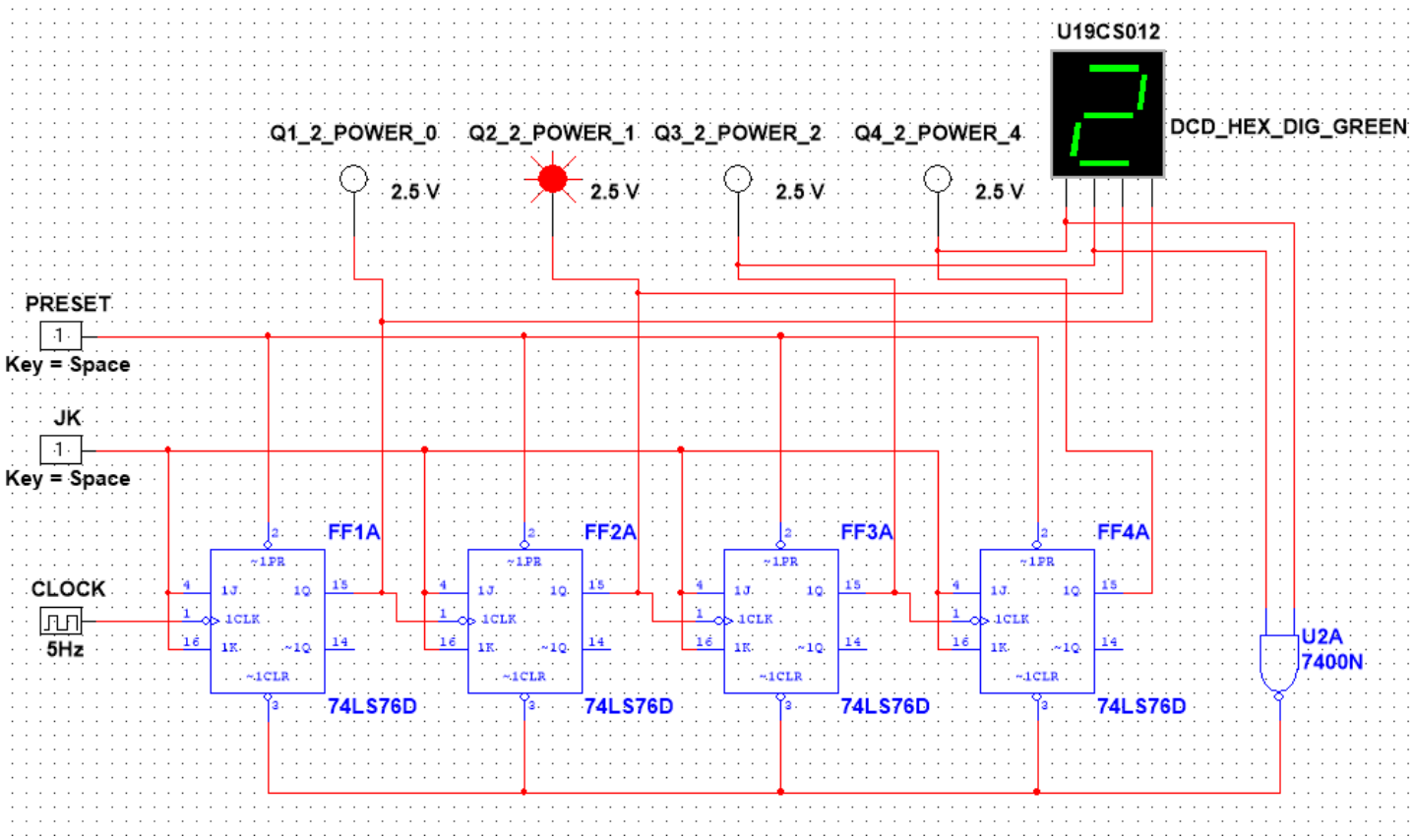
1.) Valid State: 0 [0000]



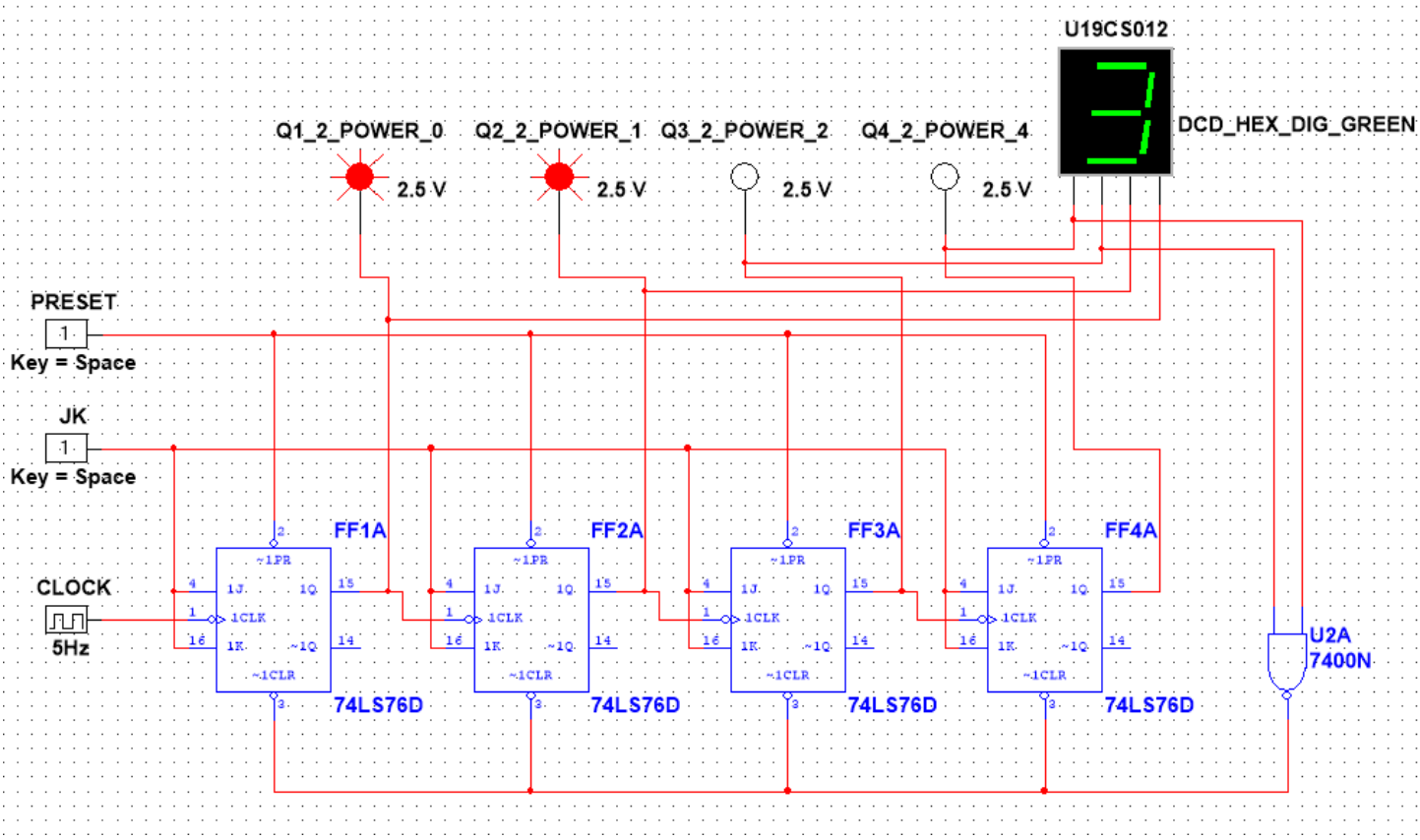
2.) Valid State: 1 [0001]



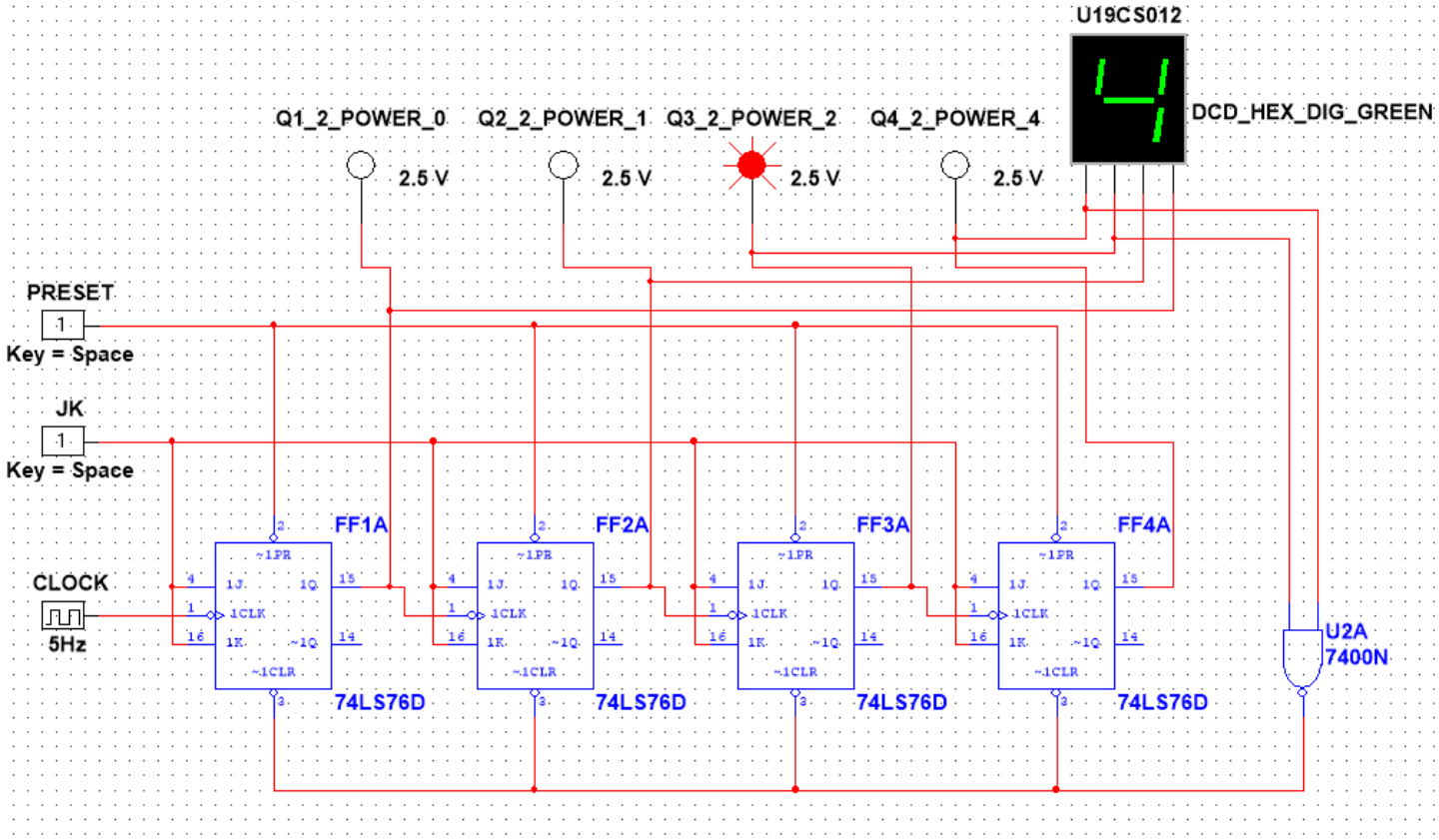
3.) Valid State: 2 [0010]



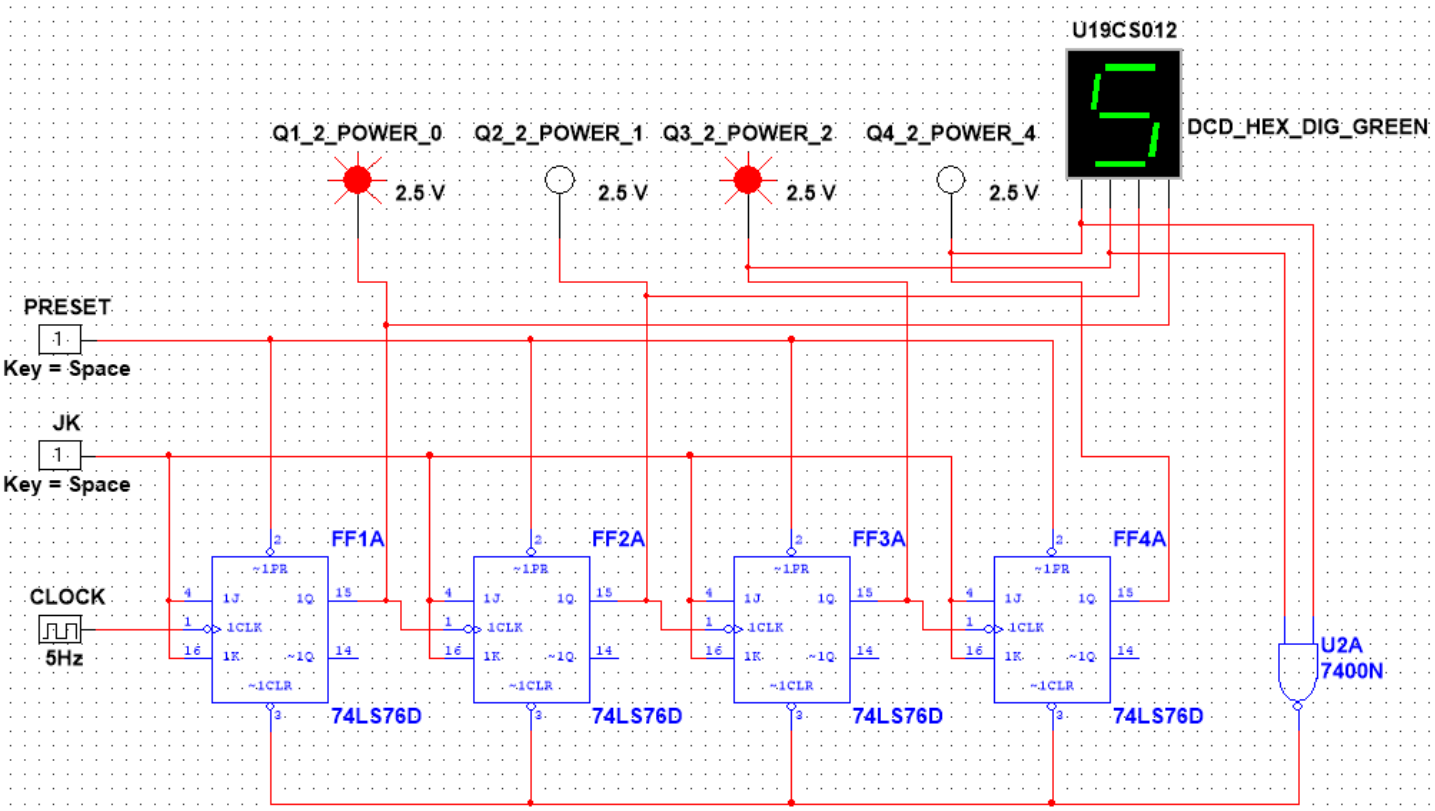
4.) Valid State: 3 [0011]



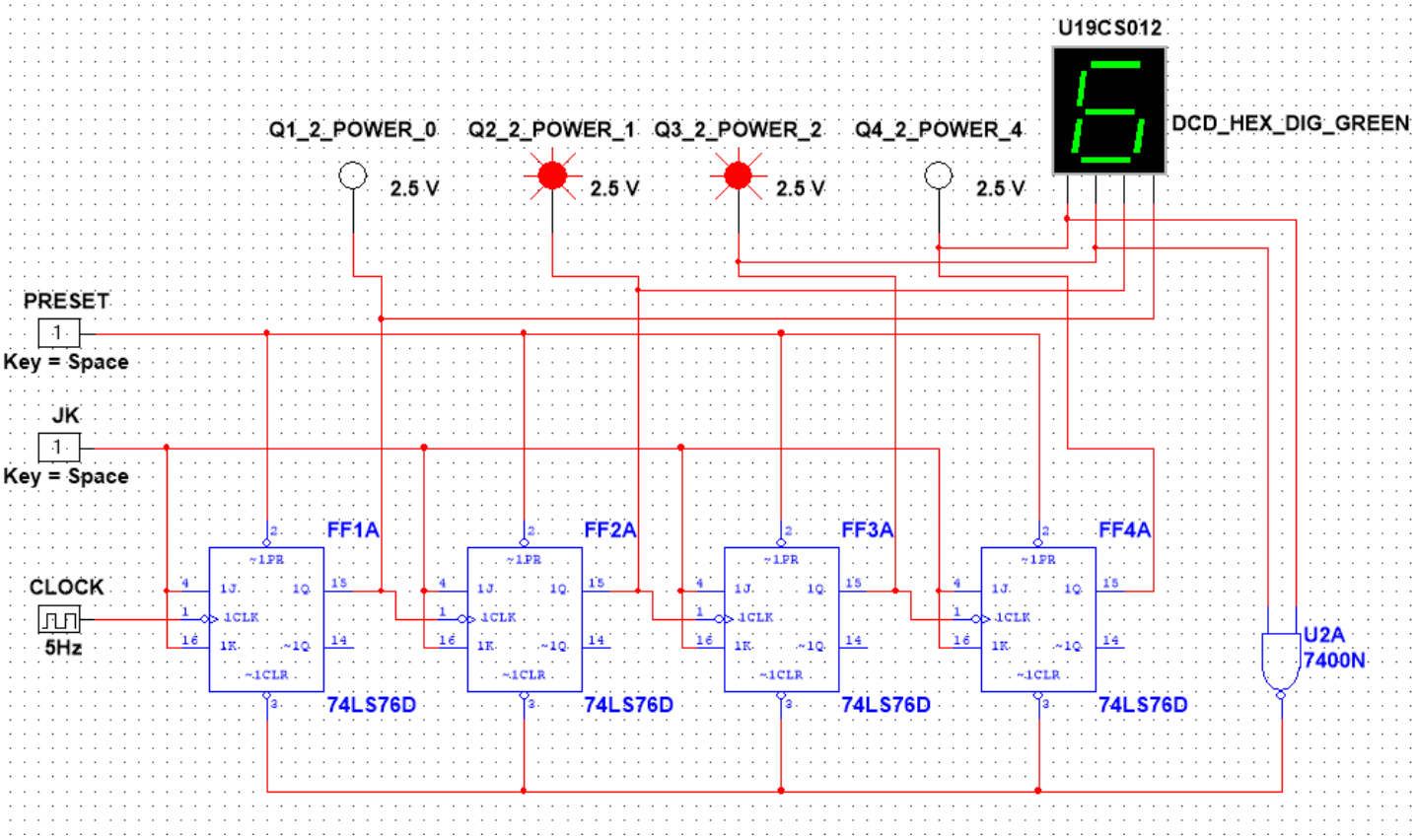
5.) Valid State: 4 [0100]



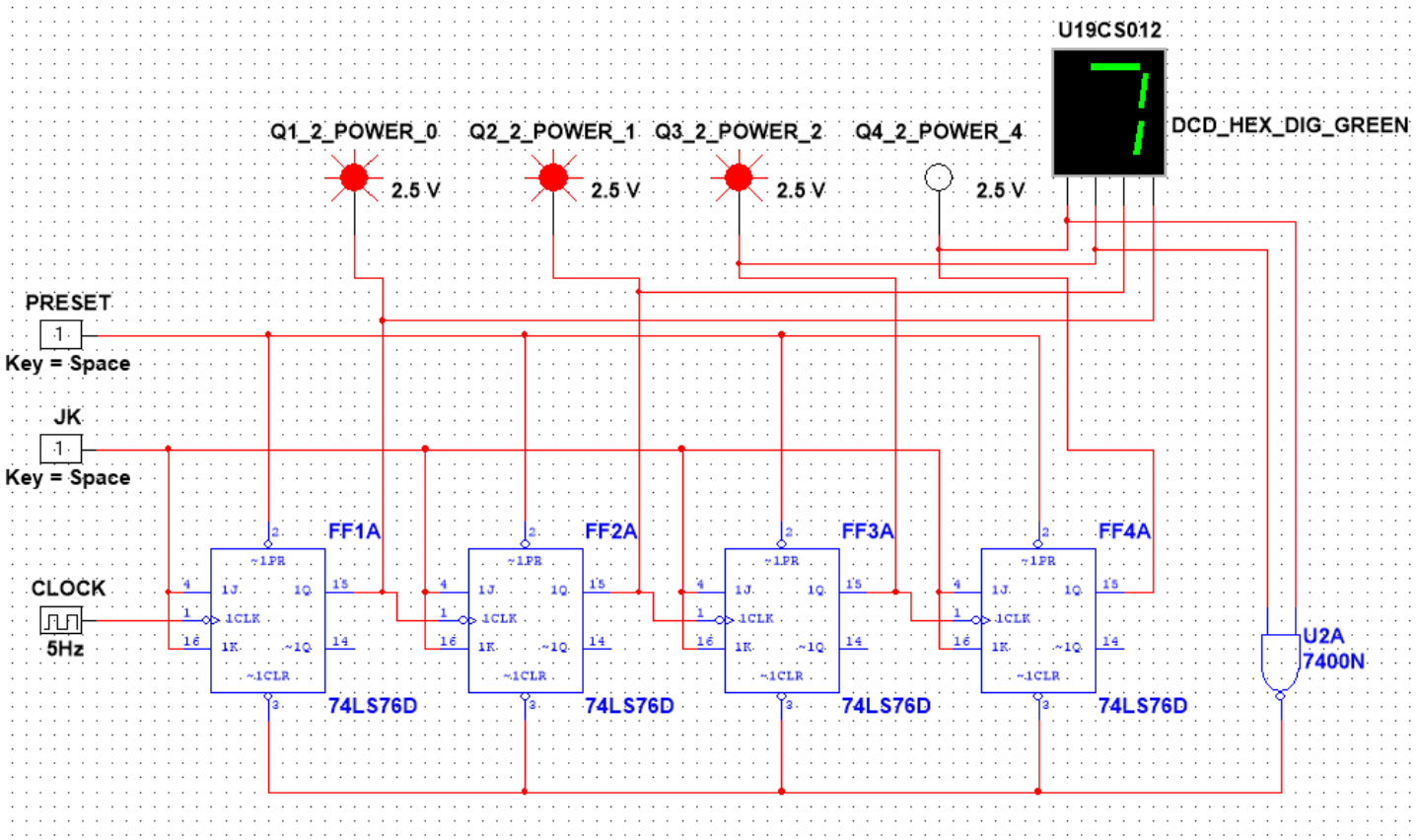
6.) Valid State: 5 [0101]



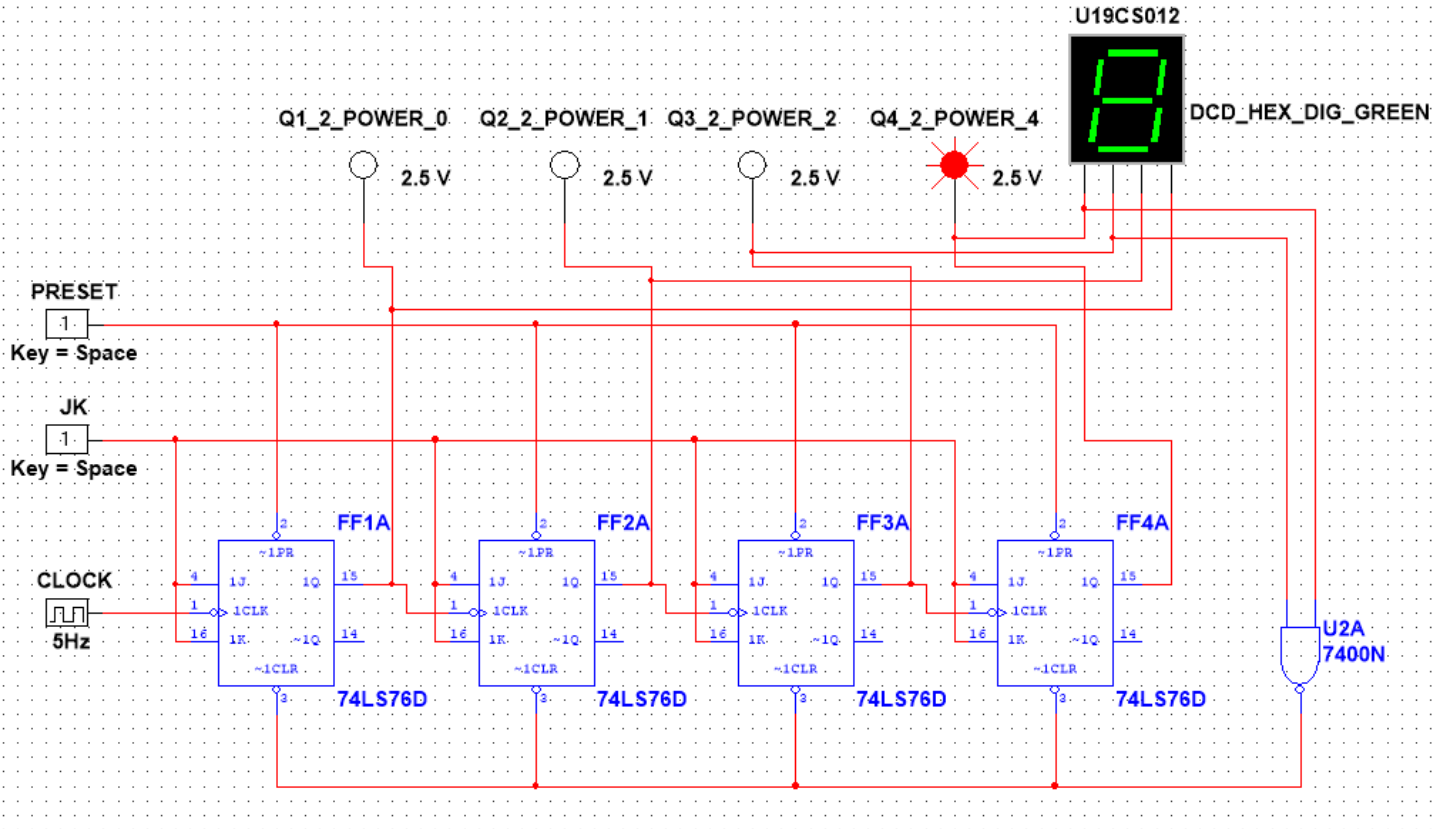
7.) Valid State: 6 [0110]



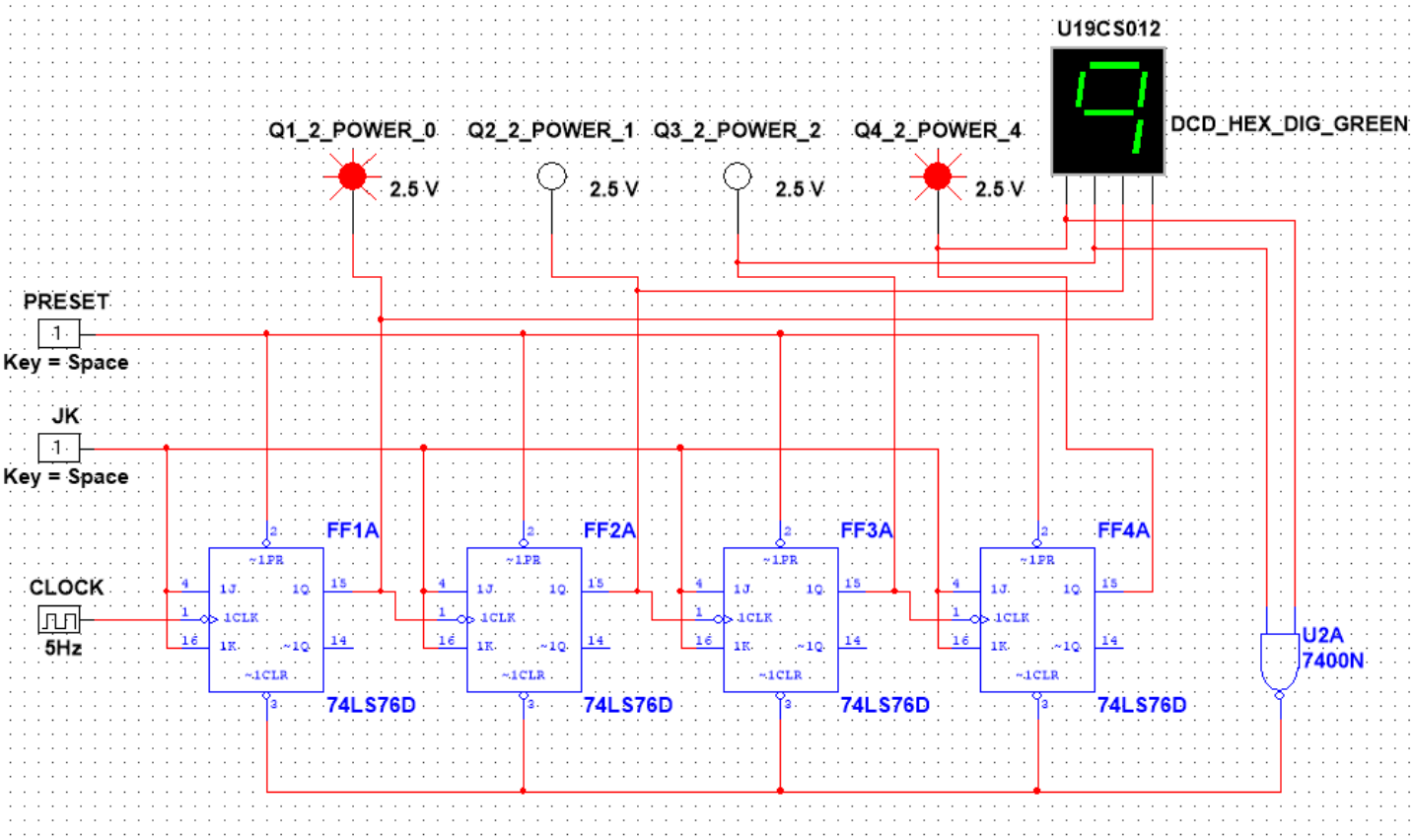
8.) Valid State: 7 [0111]



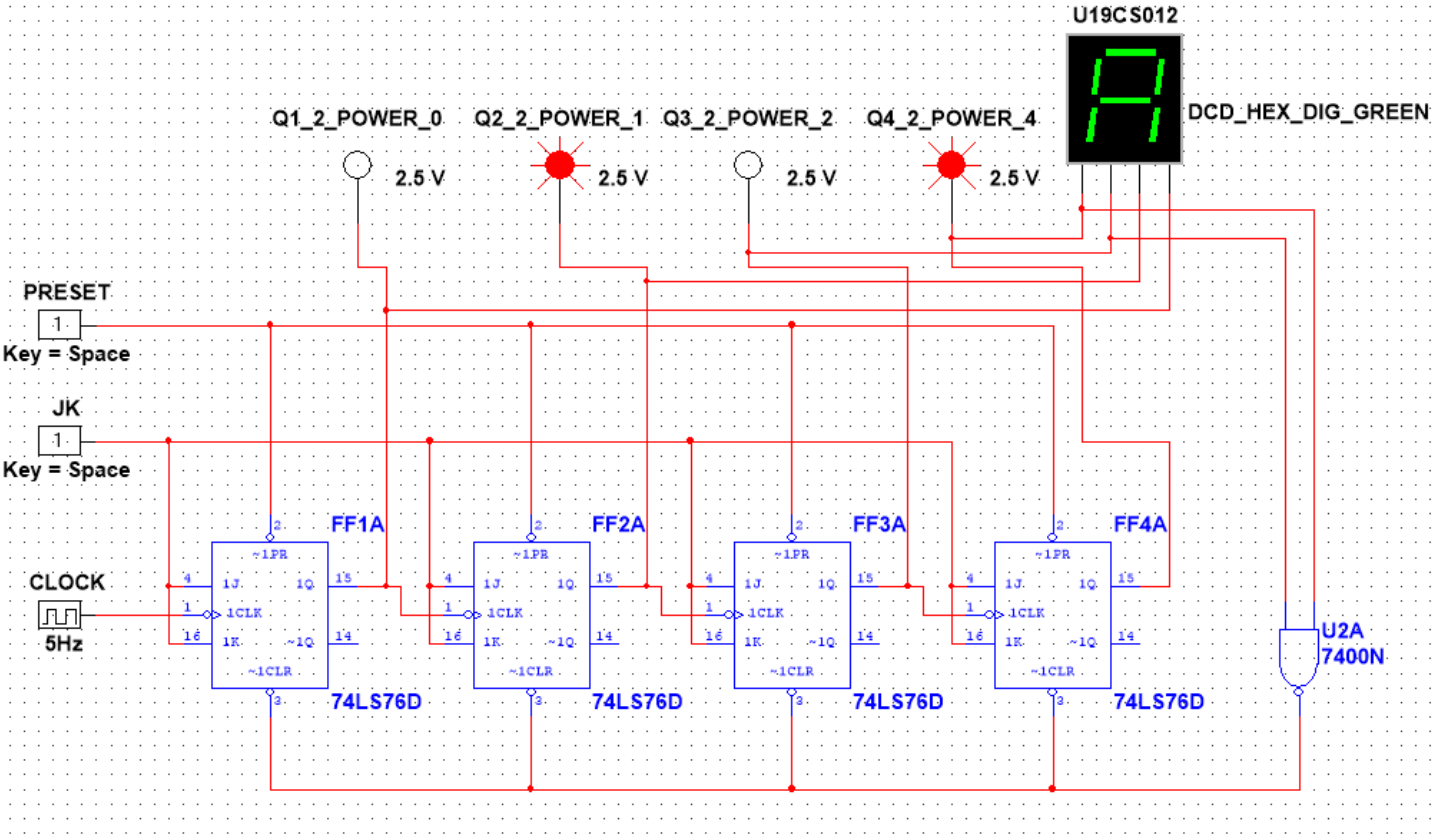
9.) Valid State: 8 [1000]



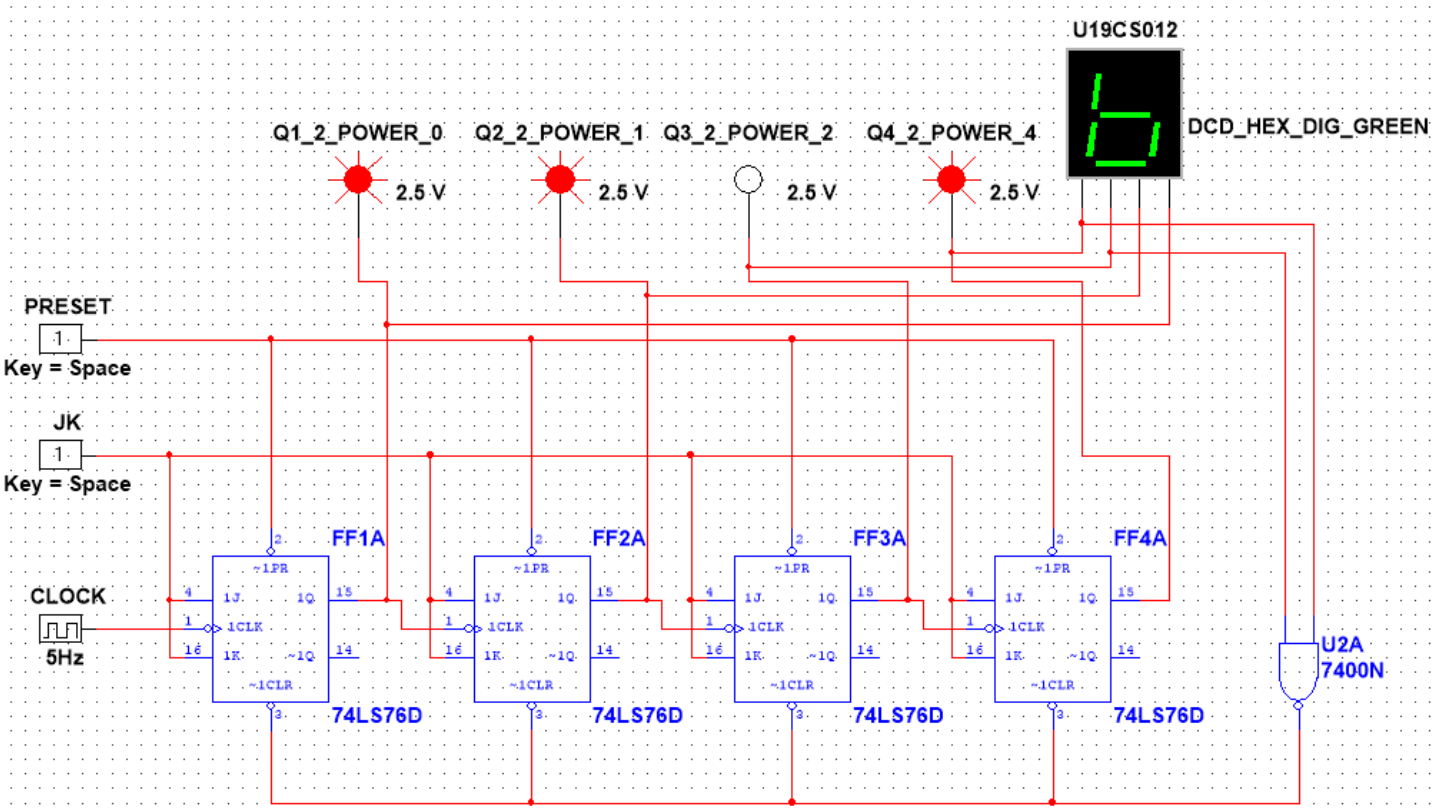
10.) Valid State: 9 [1001]



11.) Valid State: 10 [1010]

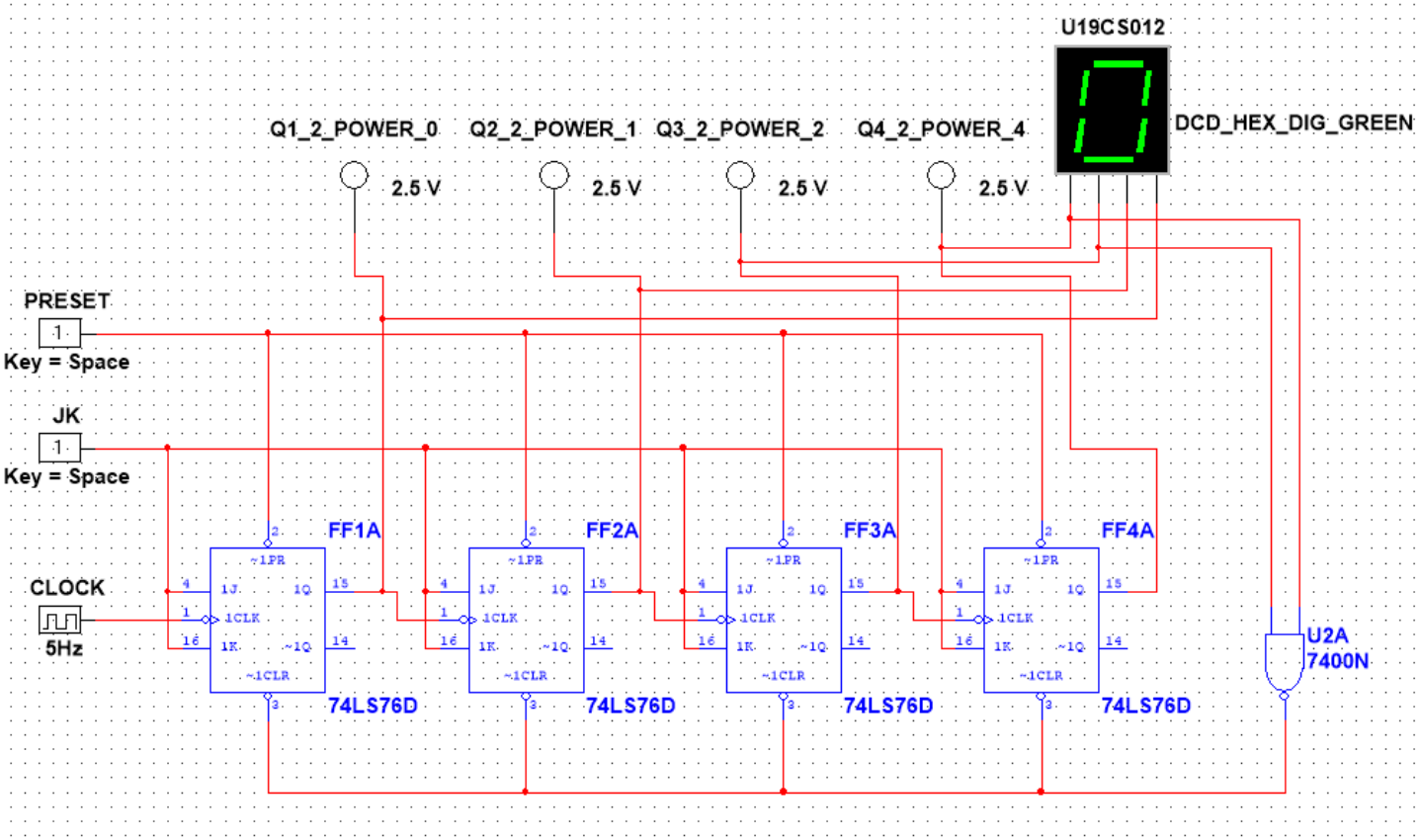


12.) Valid State: 11 [1011]

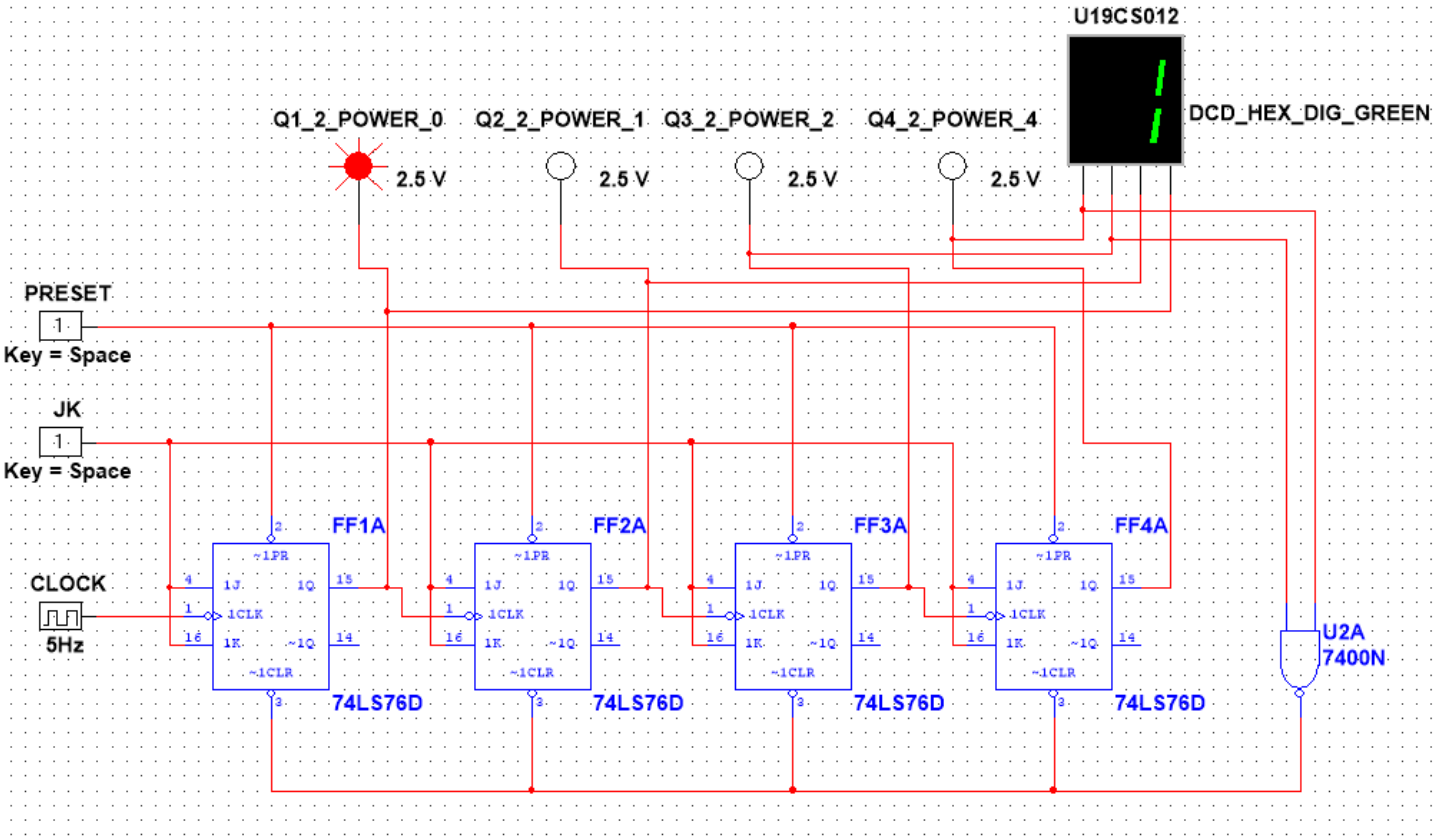


Cycle Starts Repeating Again

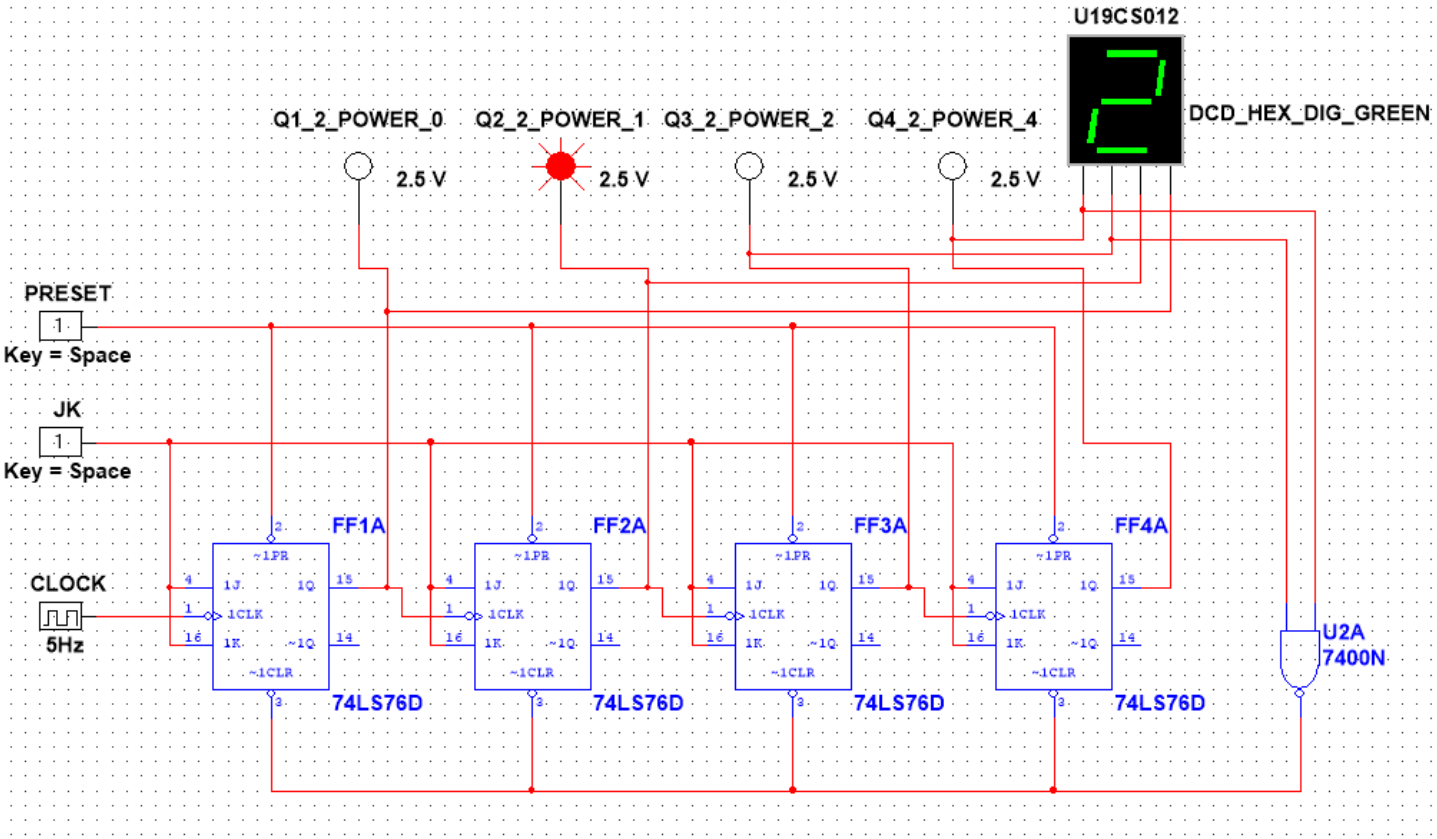
13.) Valid State: 12 [1100] -> 0 [0000]



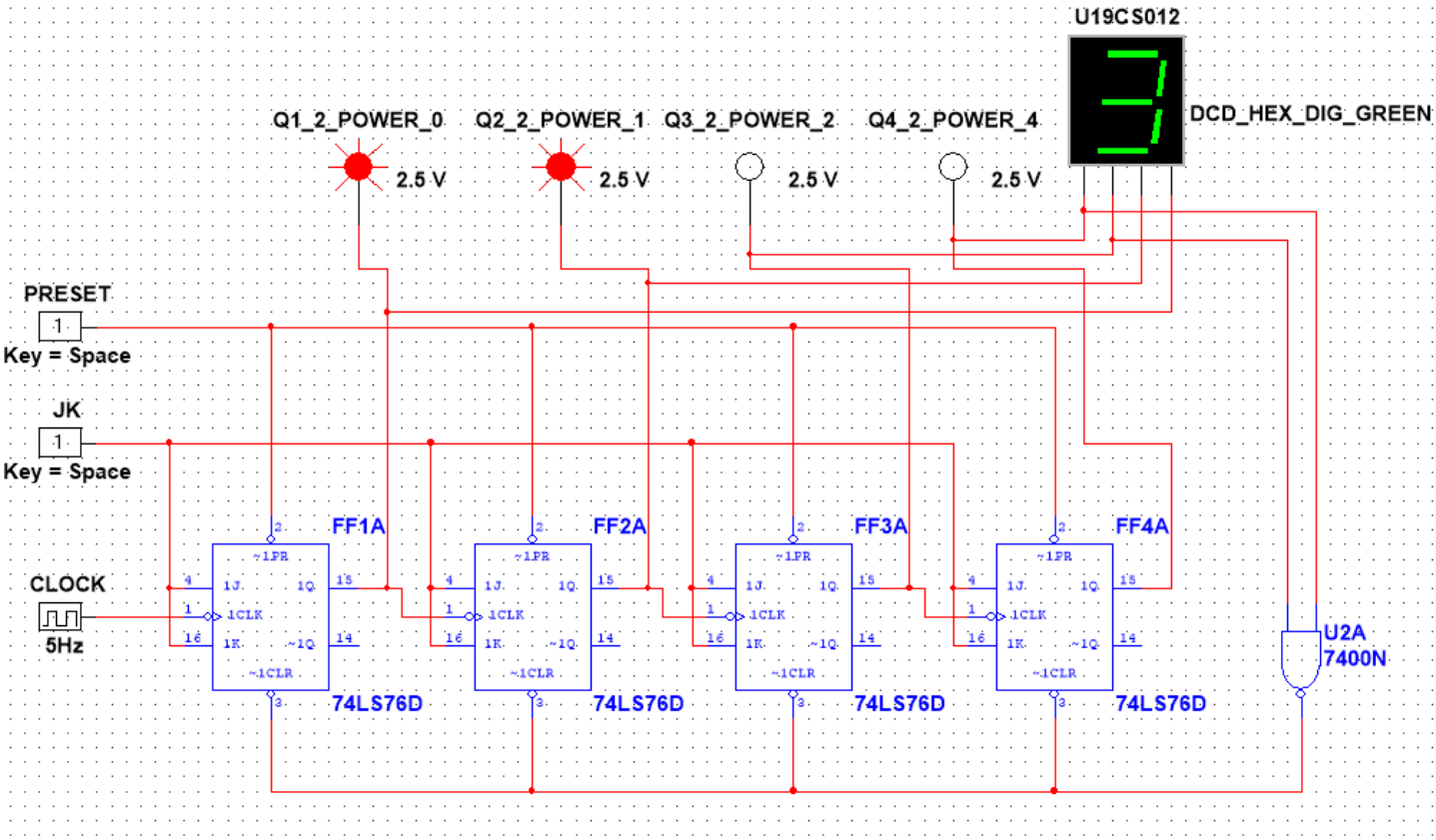
14.) Valid State: 13 [1101] -> 1 [0001]



15.) Valid State: 14 [1110] -> 2 [0010]

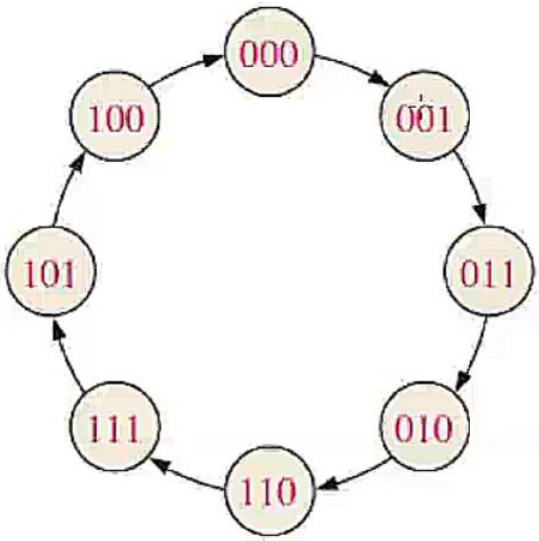


16.) Valid State: 15 [1111] -> 3 [0011]

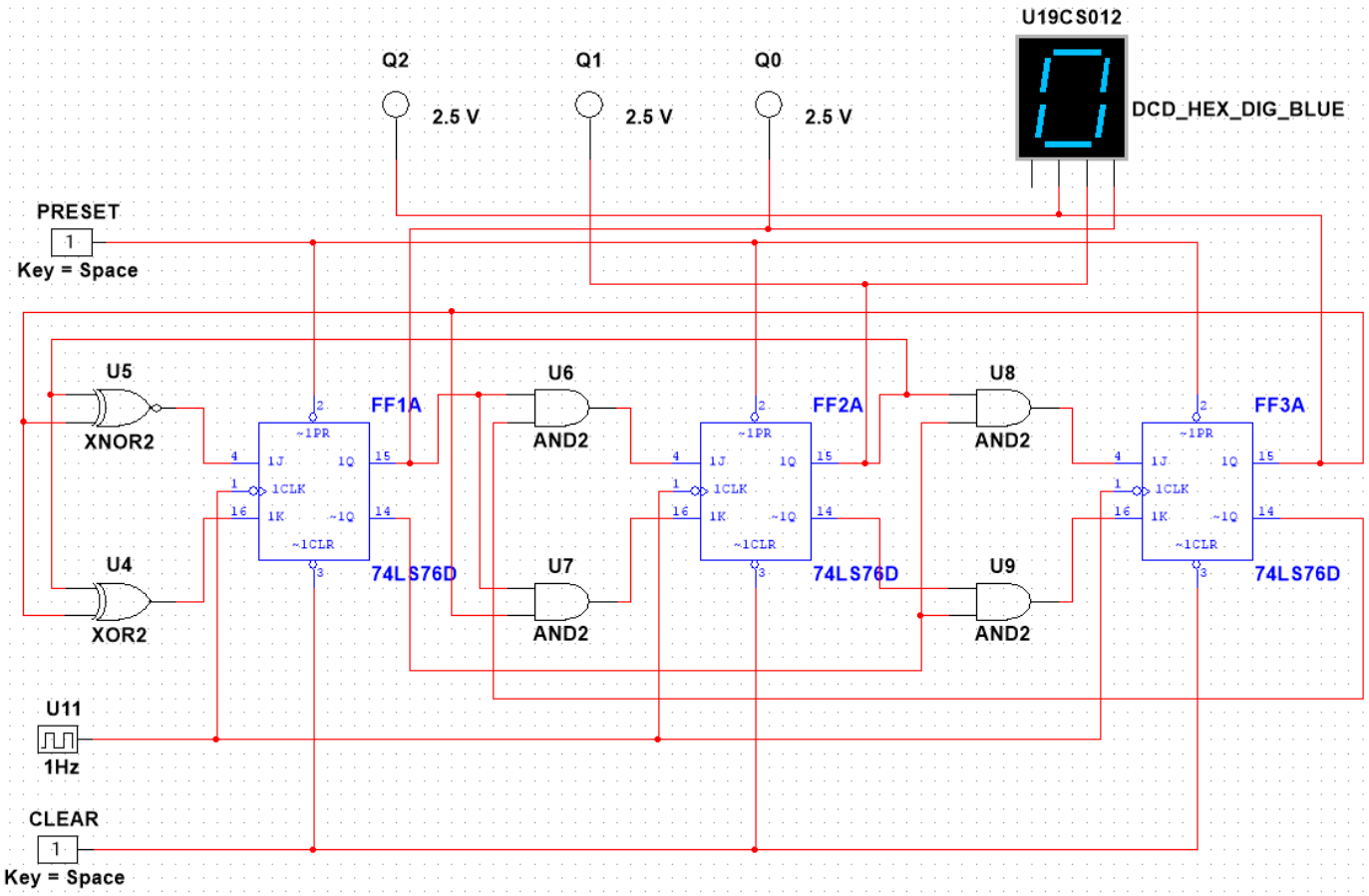


And the Loop Continues…

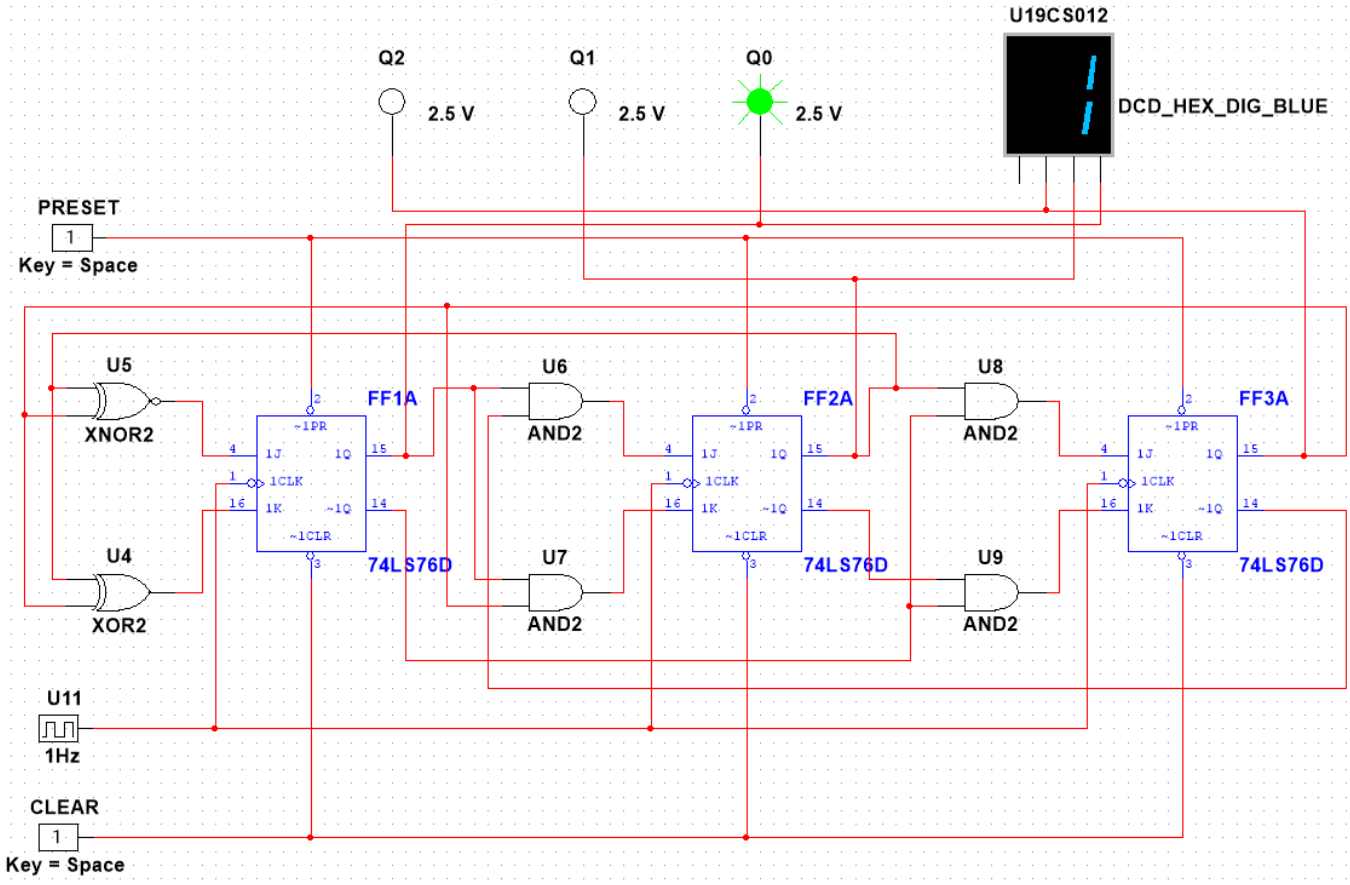
2.) Design and Implement *3-BIT Gray Code UP Synchronous Counter* in Multisim using JK Flip-Flops and Logic Gates.



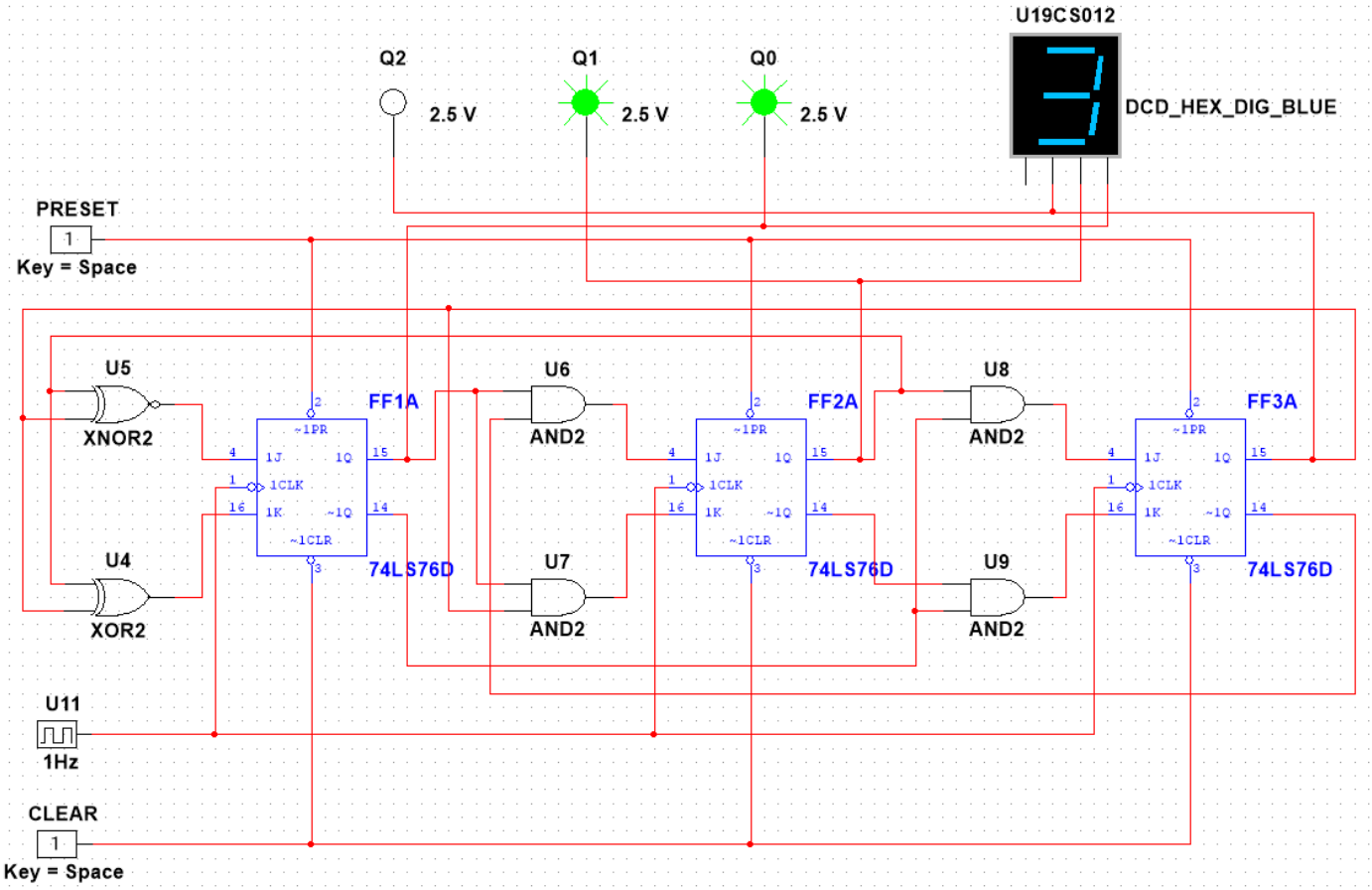
1.) Gray Code State: 000 [0]



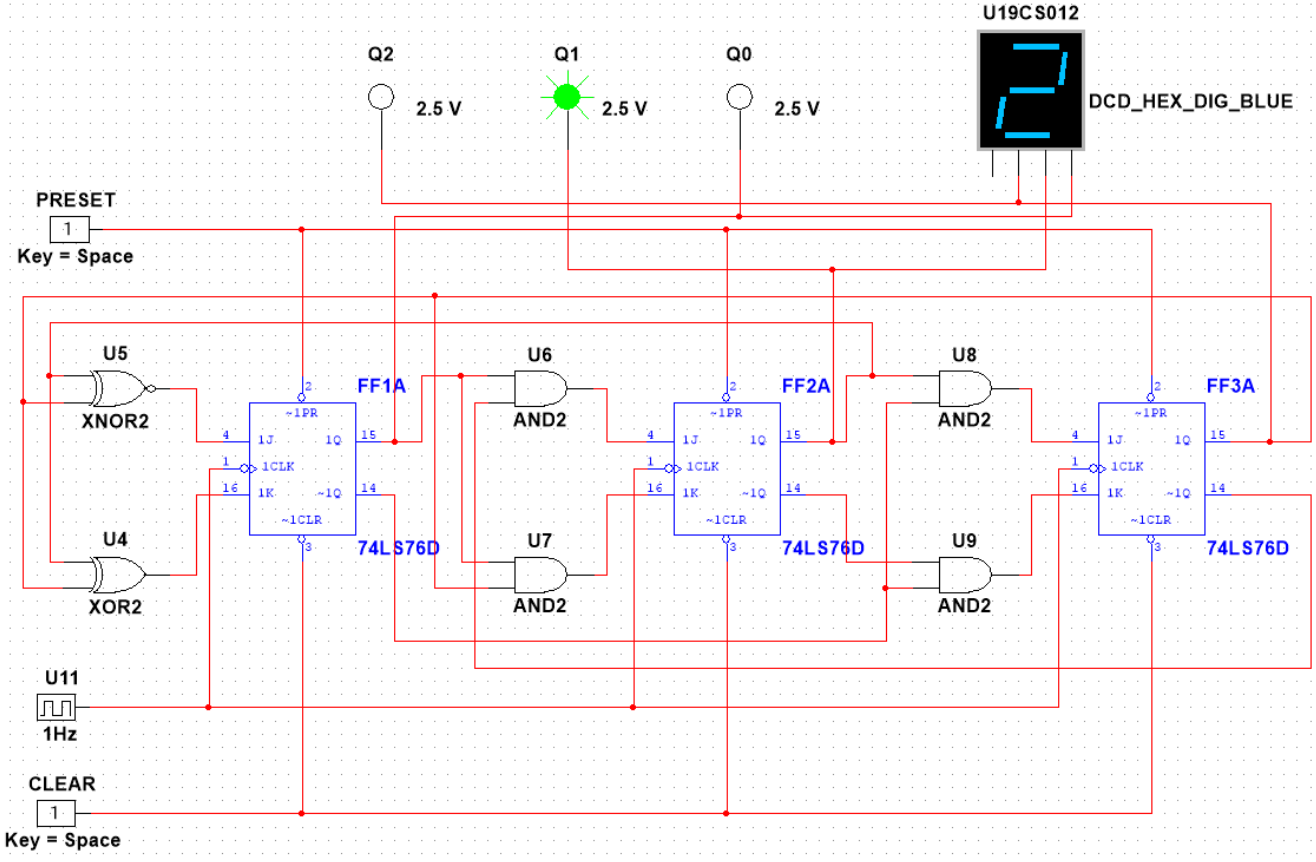
2.) Gray Code State: 001 [1]



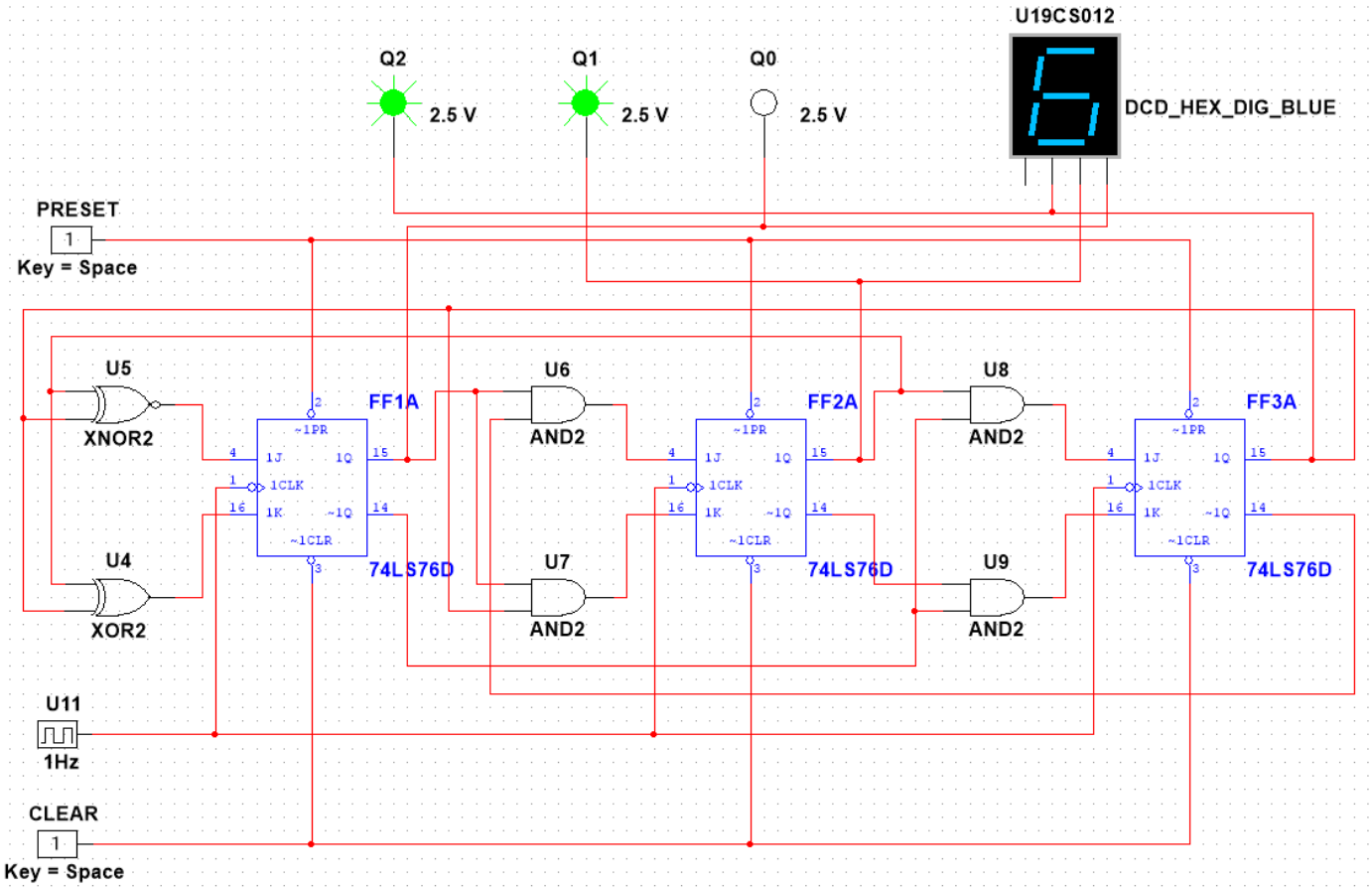
3.) Gray Code State: 011 [3]



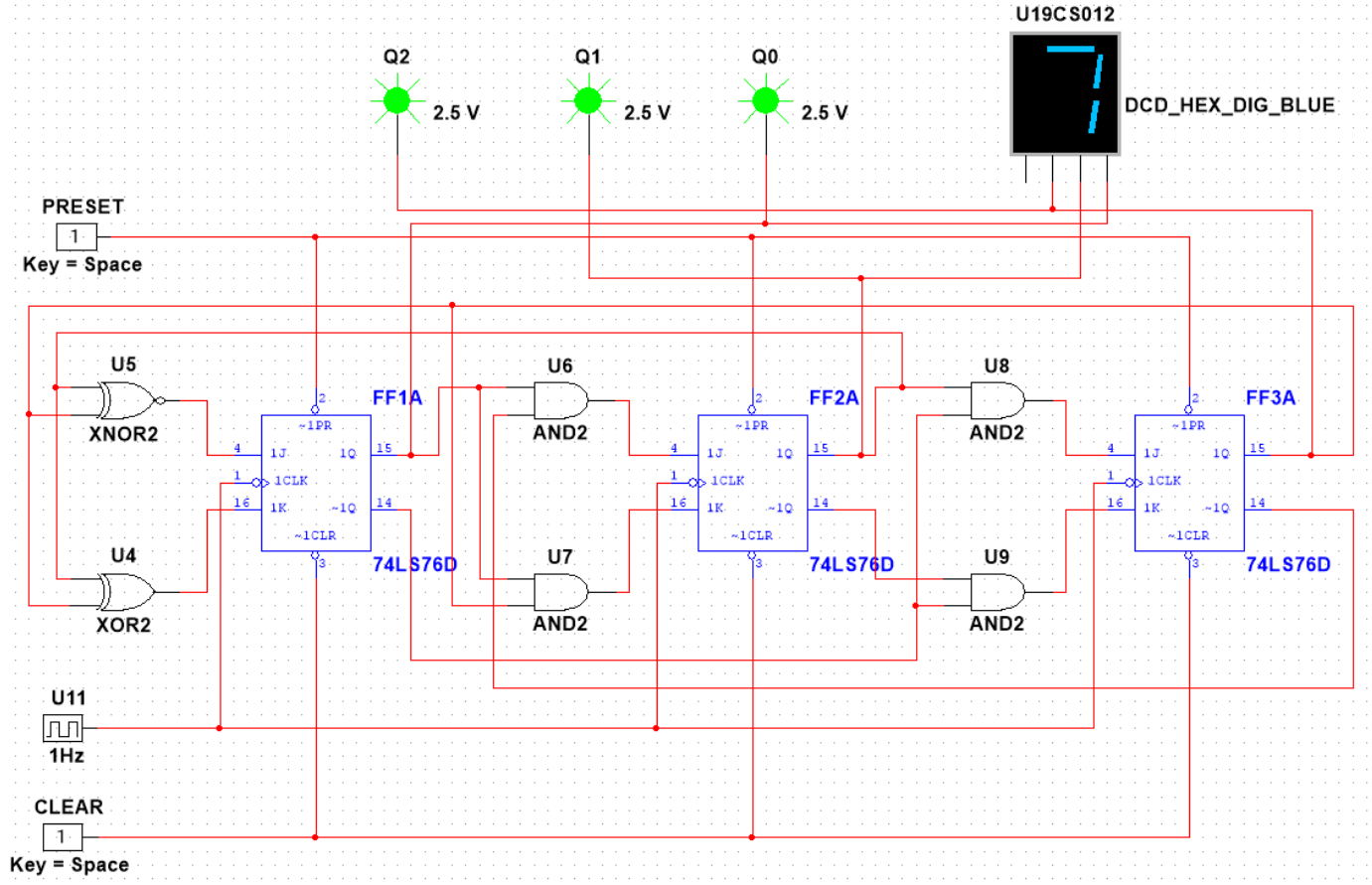
4.) Gray Code State: 010 [2]



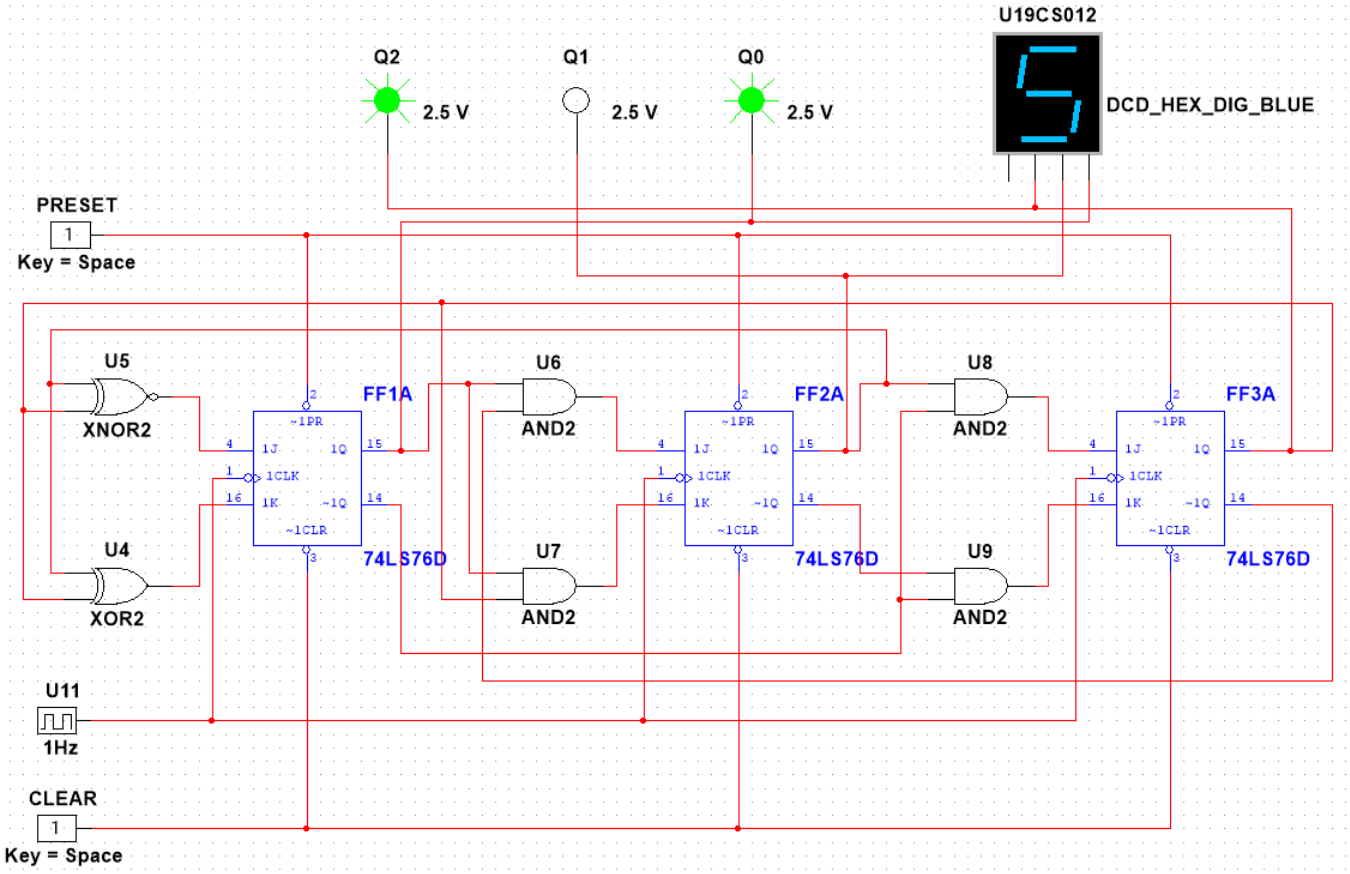
5.) Gray Code State: 110 [6]



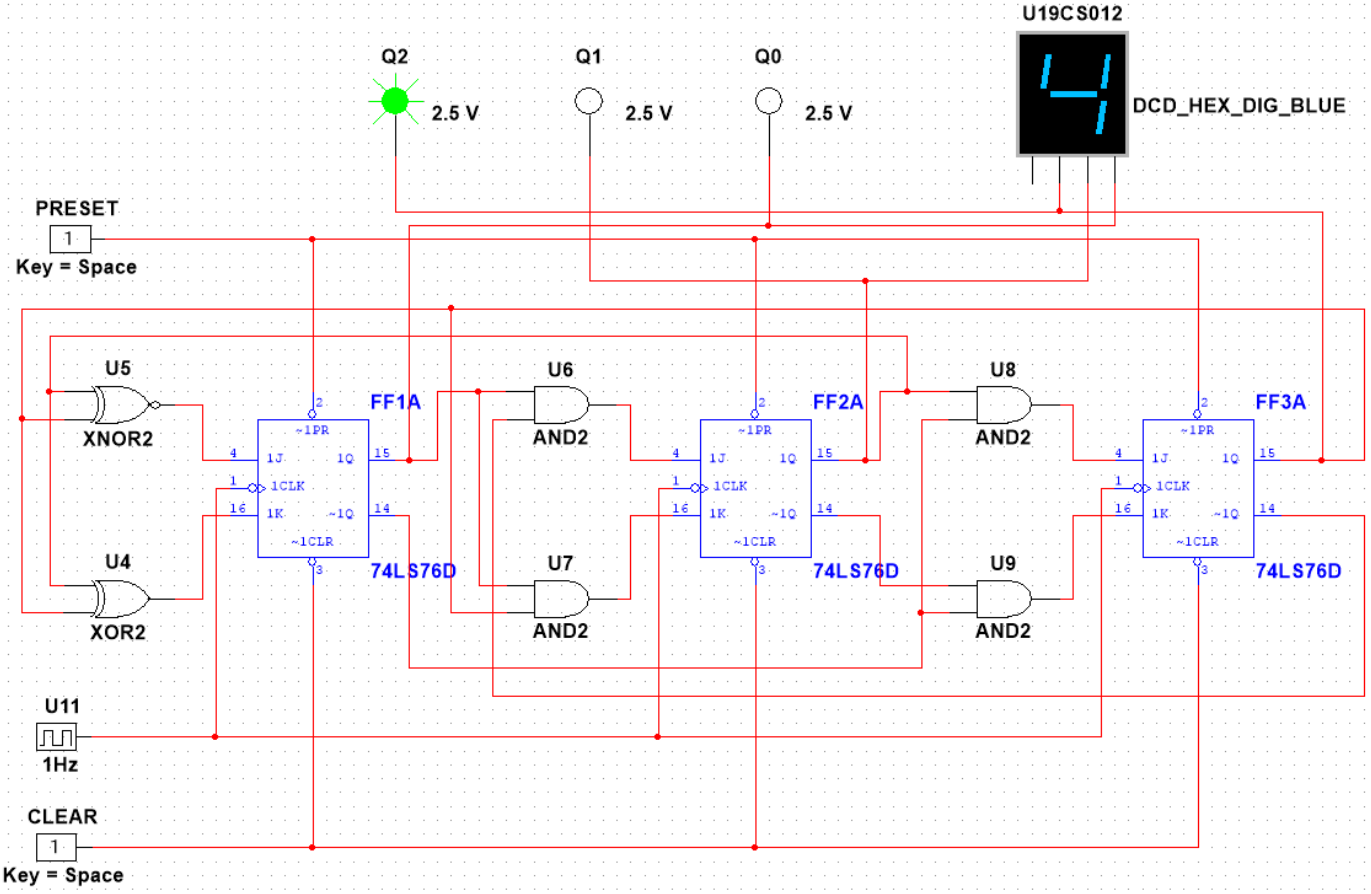
6.) Gray Code State: 111 [7]



7.) Gray Code State: 101 [5]



8.) Gray Code State: 100 [4]

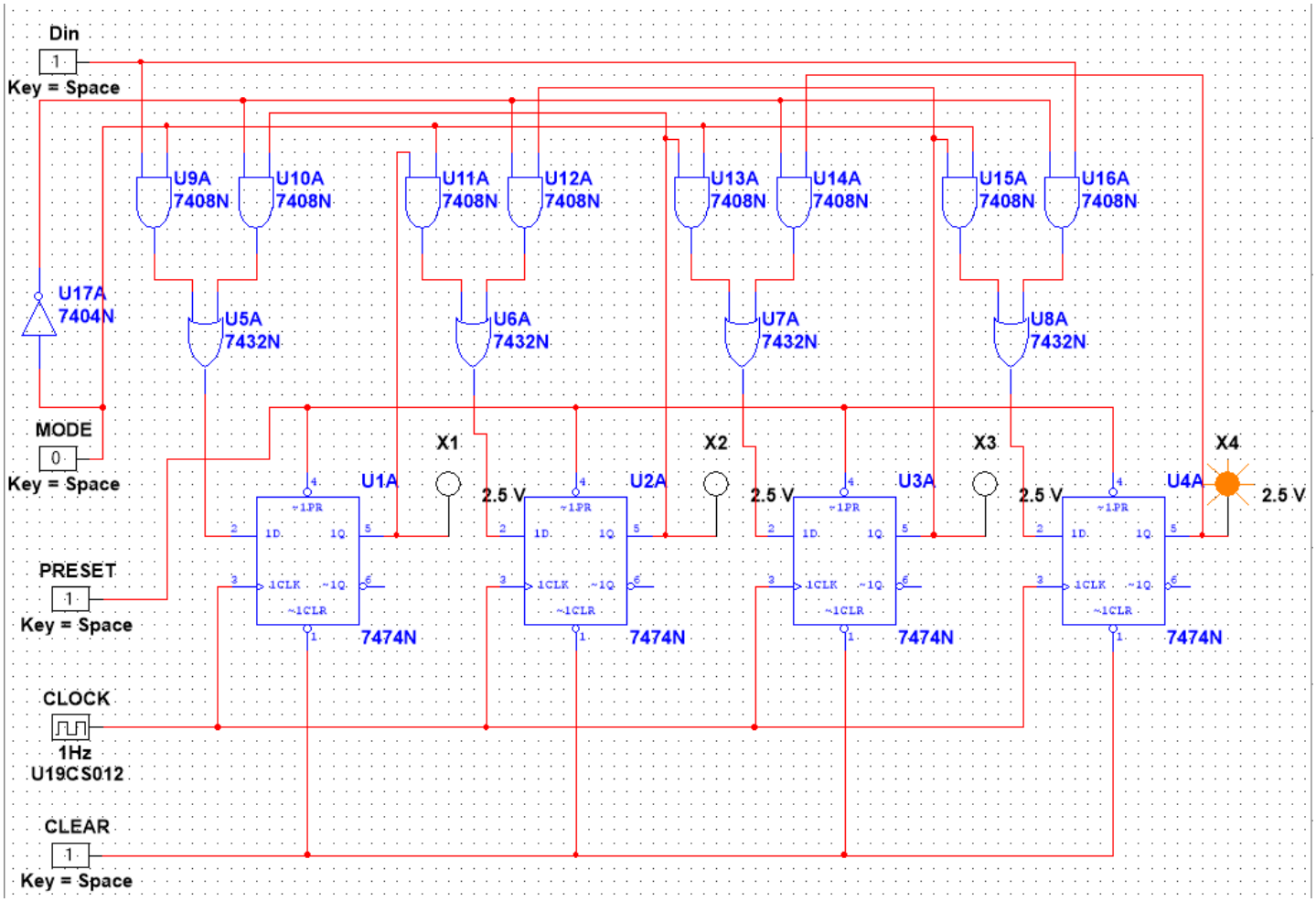


3.) Design and Implement *Bidirectional Shift Registers Using Mode Control* in Multisim using JK Flip-Flops and Logic Gates.

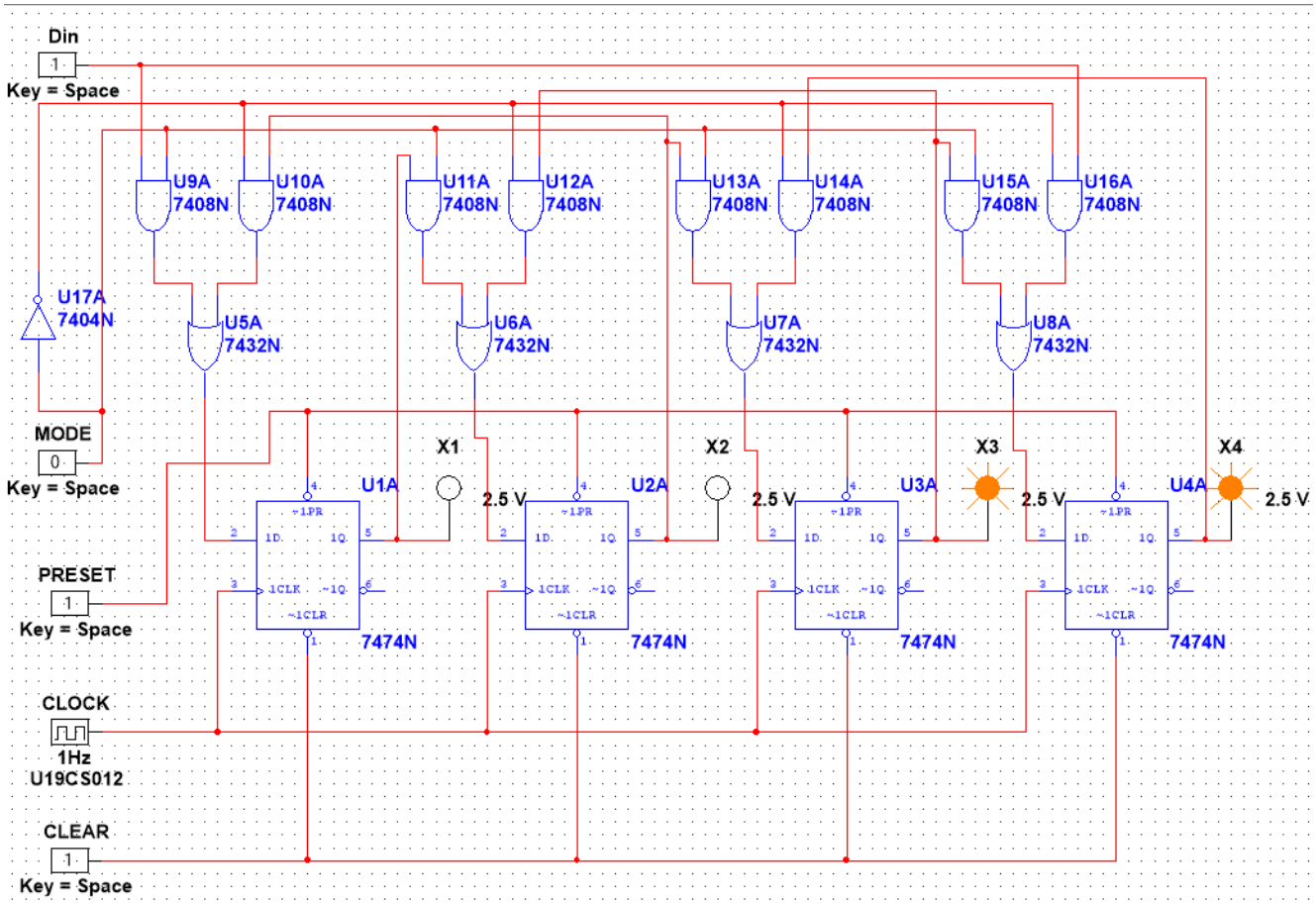
A1.) Implementation:

Mode Control: ***0 -> Shift LEFT Register***

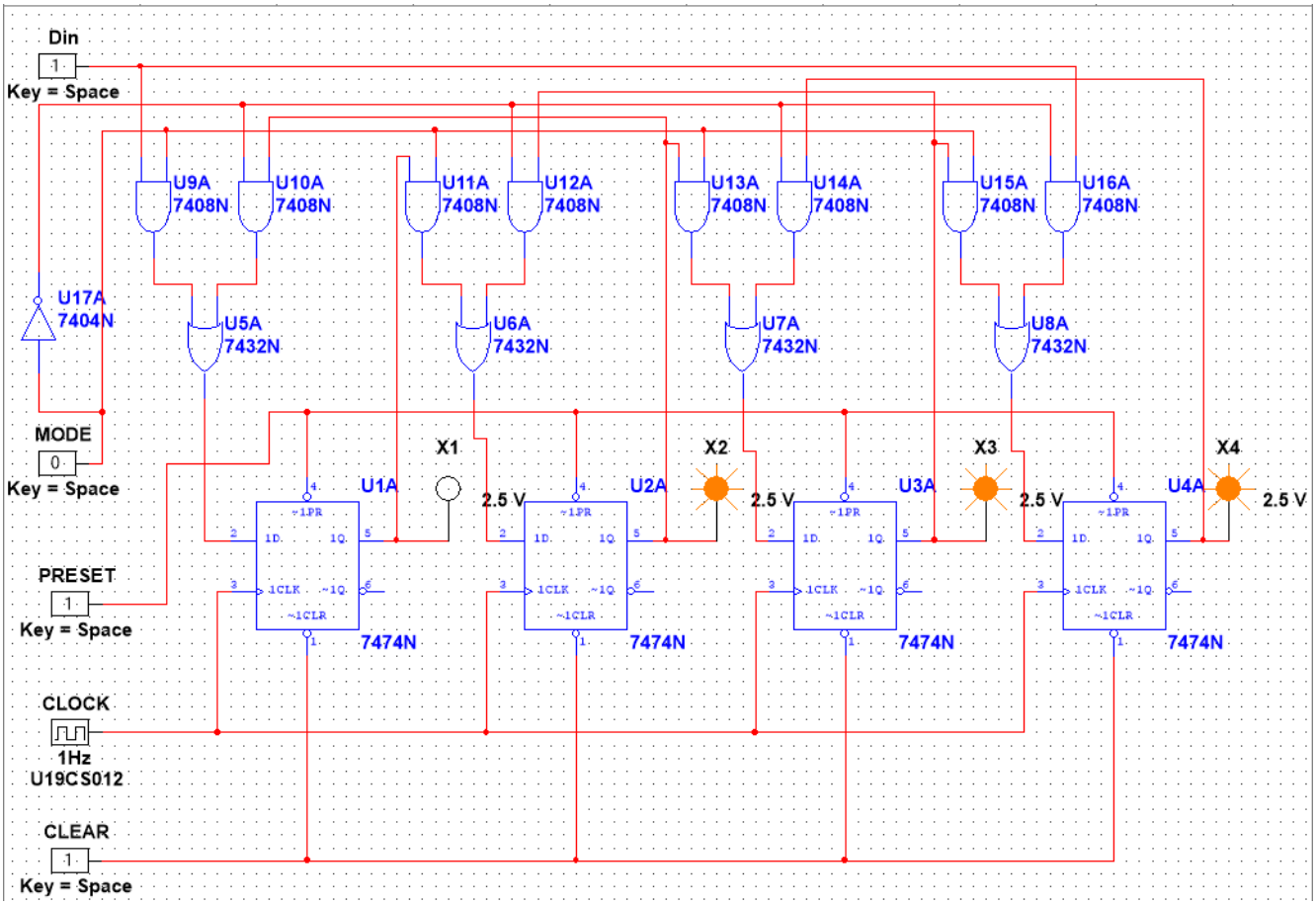
1.) State 1: 0001



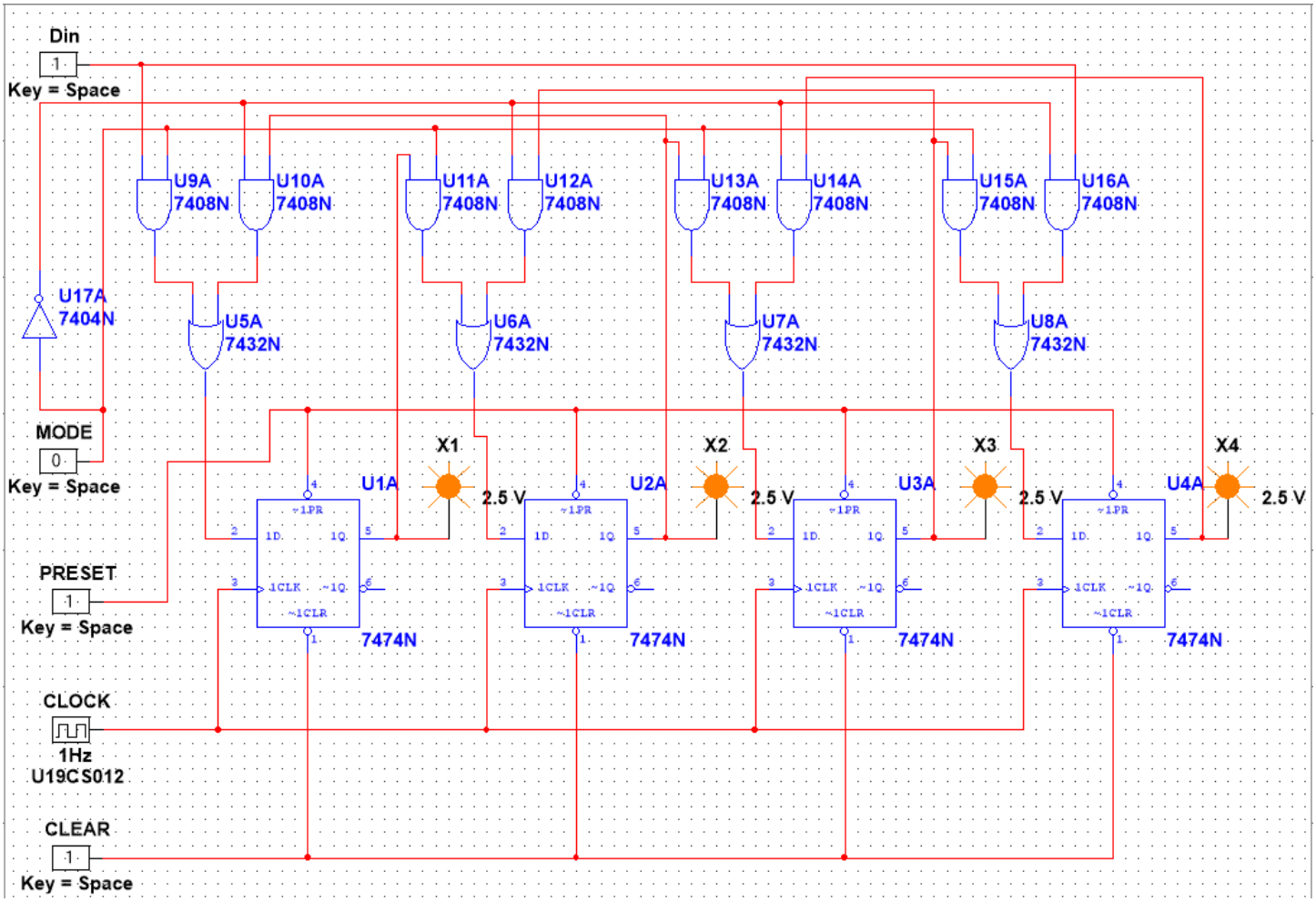
2.) State 2: 0011



3.) State 3: 0111



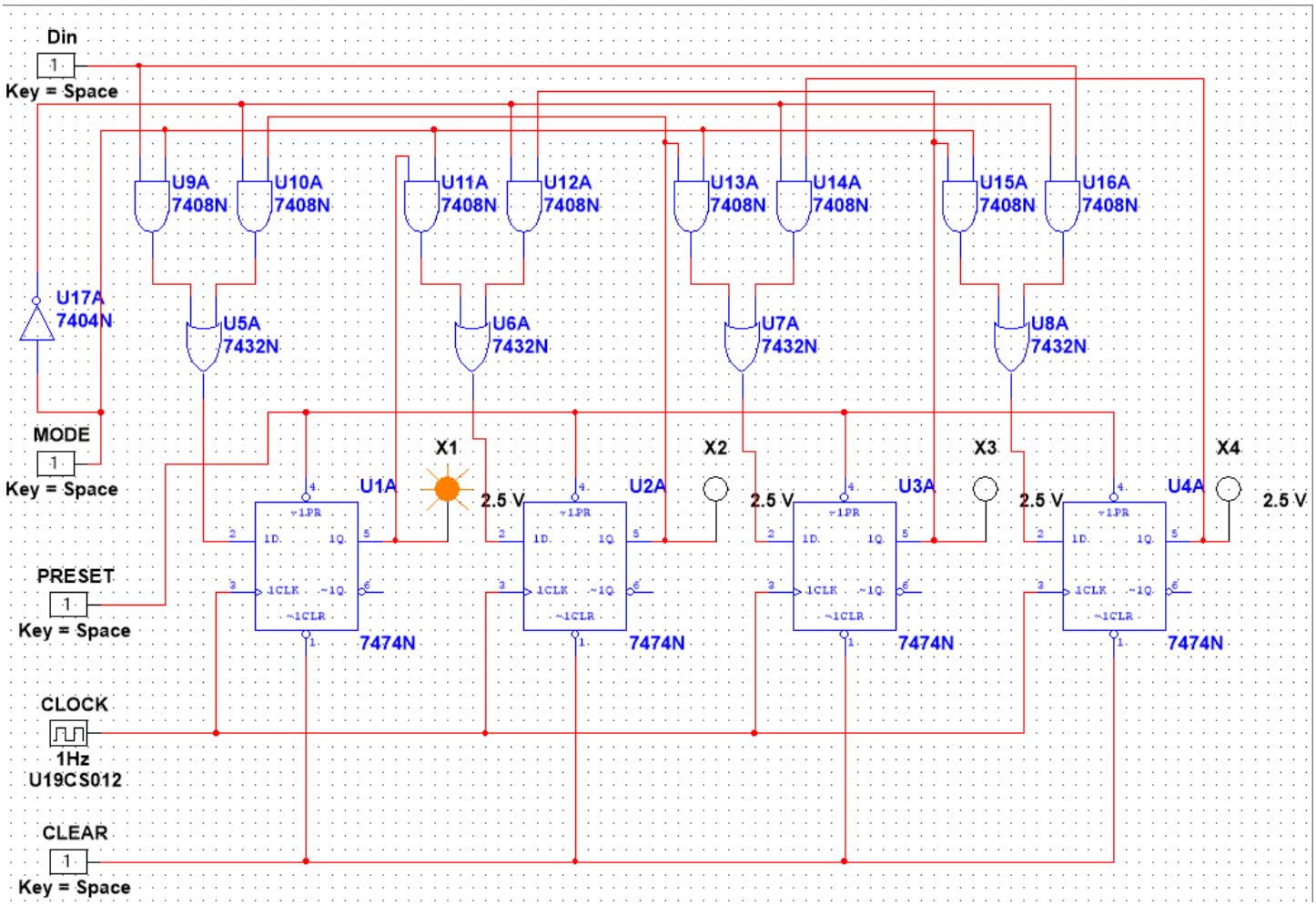
4.) State 4: 1111



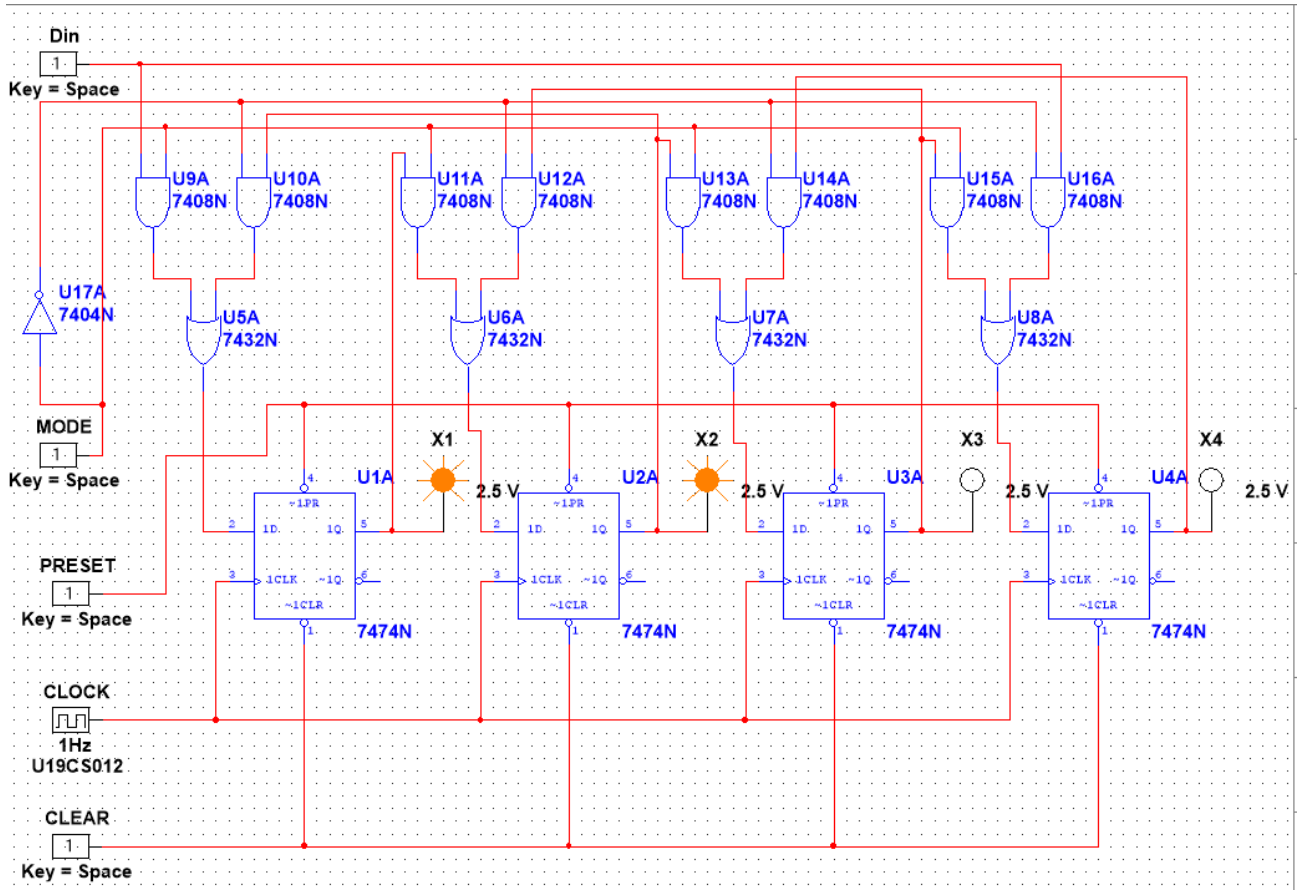
A2.) Implementation:

*Mode Control: **1** -> Shift Right Register*

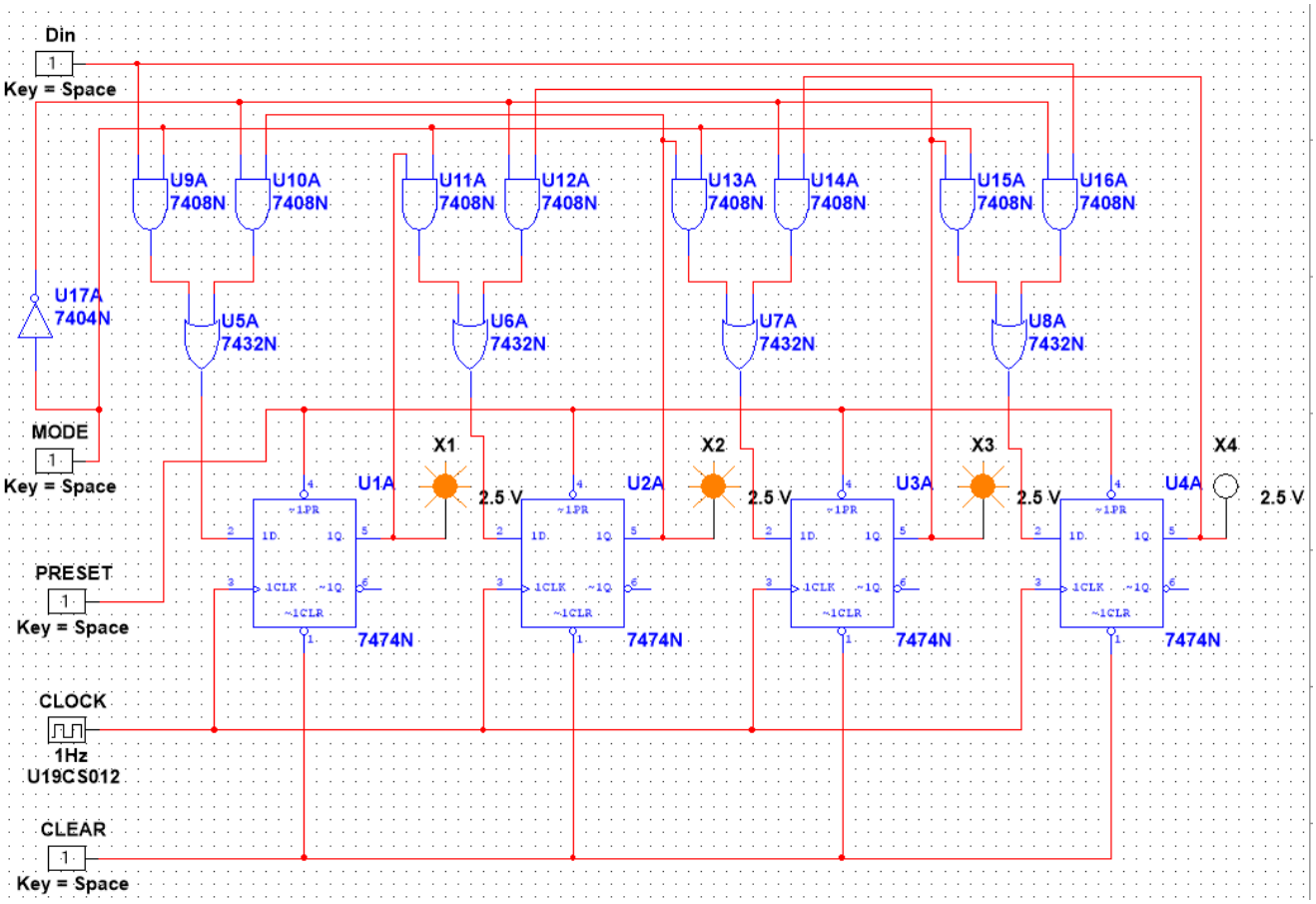
1.) State 1: 1000



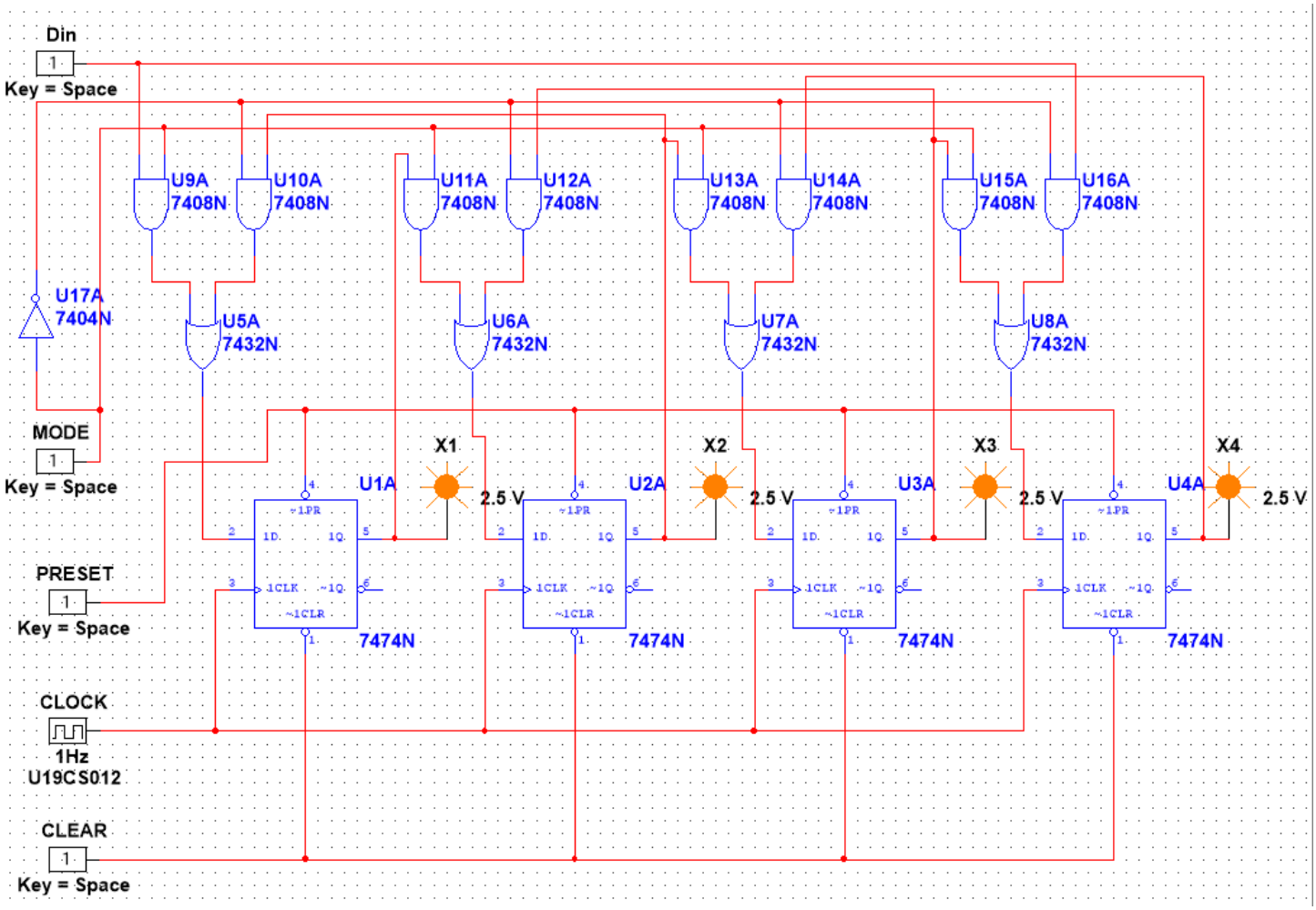
2.) State 2: 1100



3.) State 3: 1110



4.) State 4: 1111



D.) *CONCLUSION*:

We have Successfully Implemented *MOD-12 Counter, Synchronous Gray Counter and Bi-directional Shift Registers [Using Mode Control]* with the Help of JK Flip-flop and Logic Gates and **verified** our **MULTISIM Outputs** and **Results** from *Theoretical Knowledge of these Circuits taught in DELD Classes.*