Sardar Vallabhbhai National Institute of Technology, Surat

Electronics Engineering Department

End Semester Examination, December – 2020, AY-20/21

Subject: Digital Electronics and Logic Design (EC-207)

Date: 09-12-2020 **Time:** 3 Hrs **Maximum Marks:** 50

Instructions:

1. **This Question Paper Comprises of Five questions.**
2. **Figures to the right indicate the Maximum Marks assigned to the question.**
3. **Assume suitable data wherever necessary.**
4. **The Total time of 3 Hrs includes the time for scanning and uploading.**
5. **Use A4 Sheets to write answers. Mention your Admission No, Full Name and Sign on each page.**

Q.1 **A** Propose and draw a circuit/circuits that can produce the waveform in Fig.1(b) from Fig.1(a). Assume non-ideal Si diodes. **4**

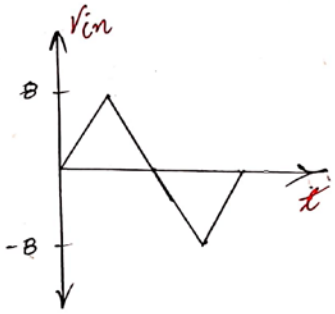


Fig. 1(a)

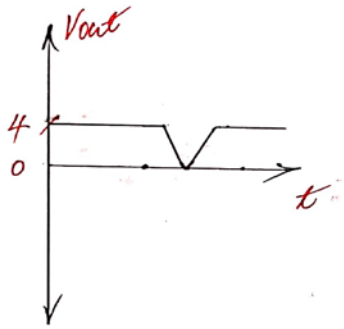
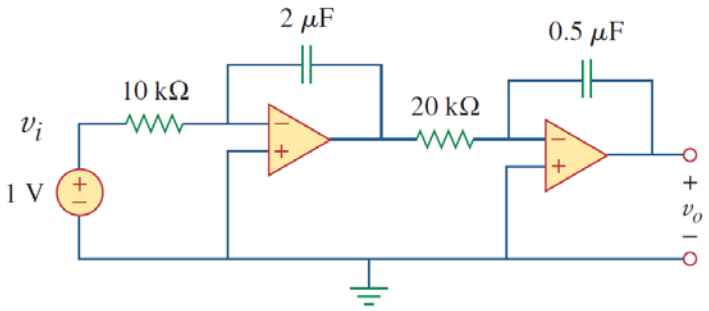
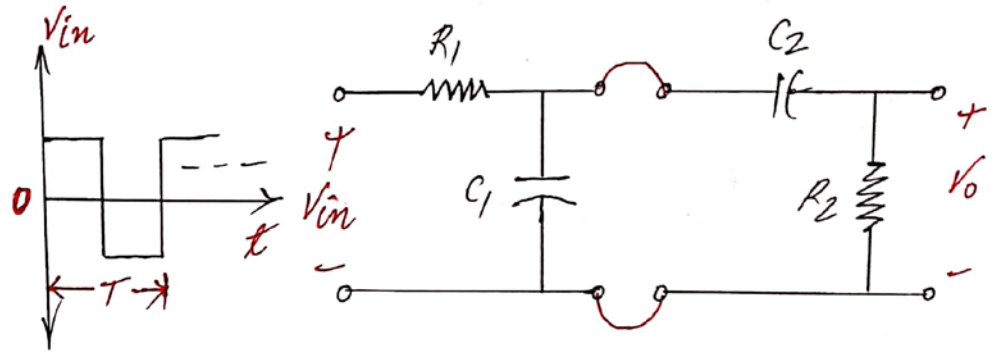


Fig. 1(b)

B For the circuit shown below, derive the relation between input and output. Also calculate the output voltage Vo at t = 6 milli second. **3**



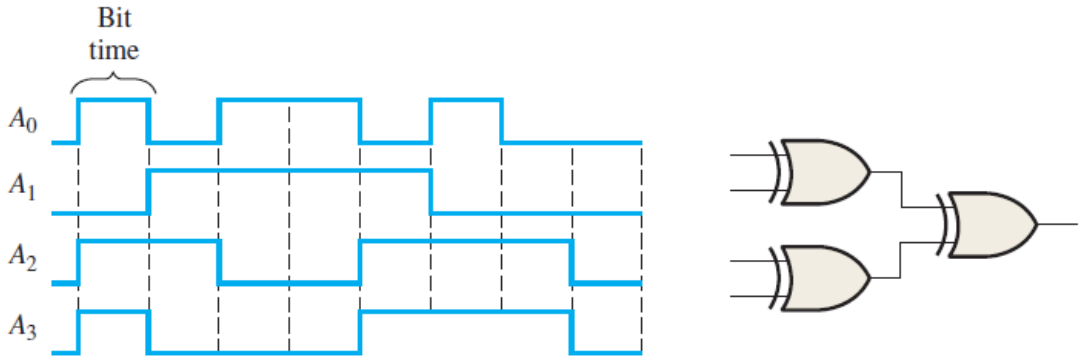
C Predict the task performed by each stage of a two stage circuit shown below. Note that the two stages are connected using connectors. Also draw the output waveform. Given (R1C1 >> T) and (R2C2 << T). **3**



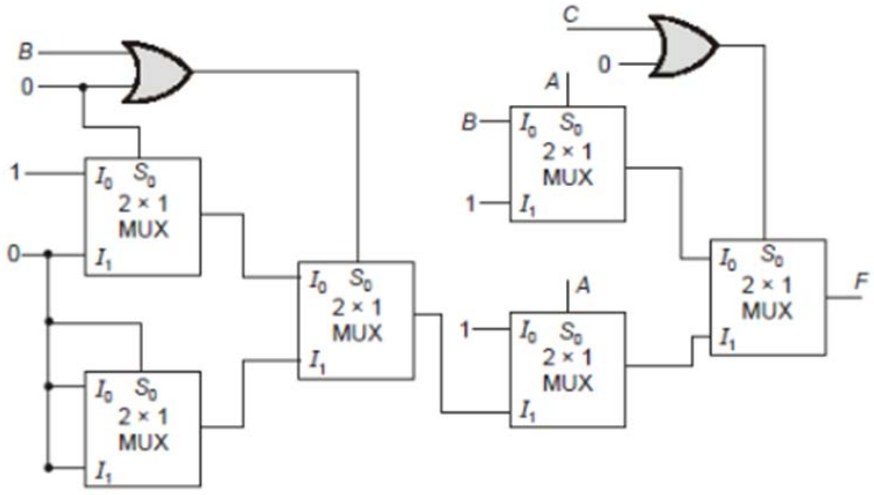
Q.2 **A** A 4 – Bit BCD Logic circuit is to be designed which can distinguish the digits that are greater than or equal to 5 from those that are less than 5. Considering the inputs as BCD numbers, design and implement the circuit (using basic logic gates) which will perform the said task. Use K-Map to simplify the expressions. **4**

OR

A Assuming A3,A2,A1,A0 as inputs applied to a Parity Logic Circuit shown in figure below. Predict how many times even parity occurs? The timing diagram includes 8-bit intervals. Append the Parity bit with A3A2A1A0P (P-Parity) for all the eight input combinations. **4**

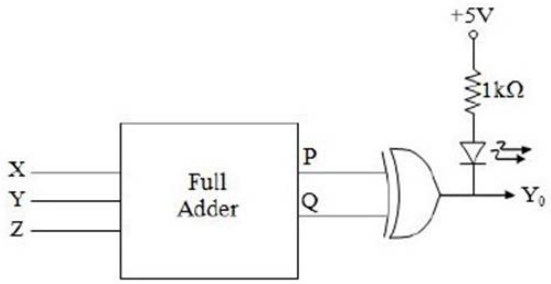


B Determine the output expression for F in the below given circuit. Also predict the number of input combinations for which the output will be high. Draw Truth Table. **4**



C Assuming Functions P and Q represent the Sum and Carry outputs of a Full – Adder, predict the number of input combinations for which the LED will glow. Assume Logic '0' – 0 Volts and Logic '1' – 5 Volts. **2**

X	Y	Z	P	Q
0	0	0		
0	1	0		
0	1	1		
1	0	0		
1	1	0		
1	1	1		
0	0	1		



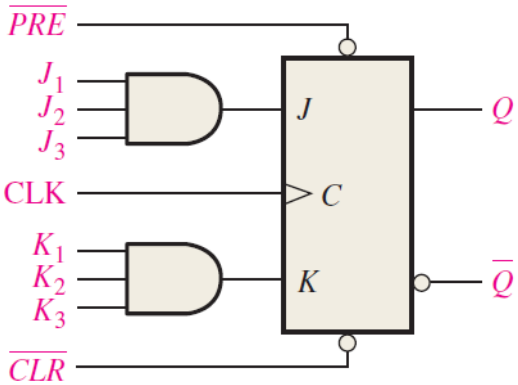
Q.3 **A** Design an Universal Shift Register to perform Shifting/Loading as per the following select inputs: **4**

S1	S0	Operation
0	0	Shift Right
0	1	Parallel Shift
1	0	No Change
1	1	Shift Left

B The following serial data are applied to the flip-flop through via AND gates as indicated in Figure below. Determine the resulting bit-pattern data that appears on the *Q* output. Predict and draw the output waveform for (6 Clock-Pulses). There is one clock pulse for each bit time. Assume that *Q* is initially 0 and that *PRE'* and *CLR'* are HIGH. Also that the, rightmost bits are applied first. **4**

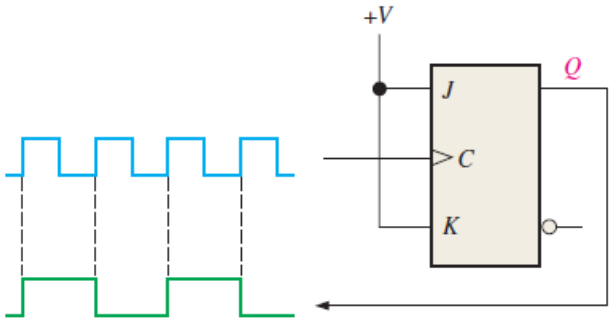
*J*1: 1 0 1 0 0 1 1; *J*2: 0 1 1 1 0 1 0; *J*3: 1 1 1 1 0 0 0

*K*1: 0 0 0 1 1 1 0; *K*2: 1 1 0 1 1 0 0; *K*3: 1 0 1 0 1 0 1

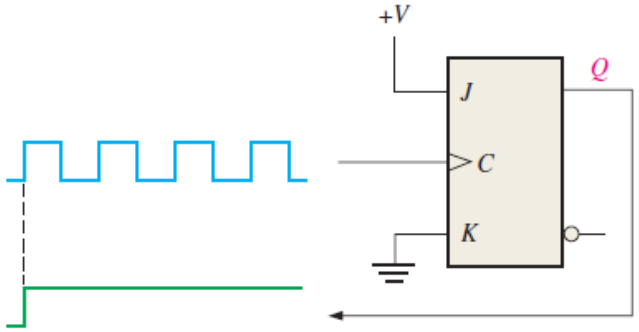


C The Flip-Flop below is tested for following four conditions. Is it working correctly or has a Fault? Describe your conclusion in detail. If faulty, write down what could be the possible reasons behind the fault? **2**

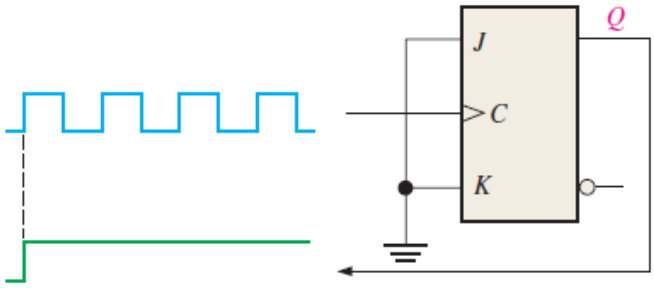
Condition - 1



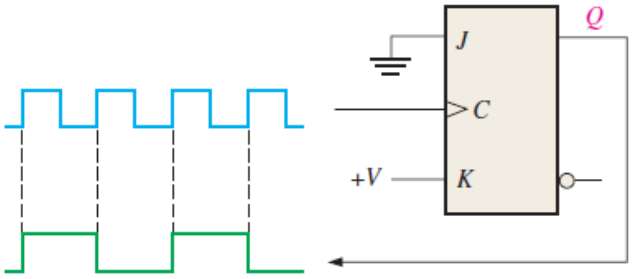
Condition - 2



Condition - 3



Condition - 4



Q.4 **A** Design an Asynchronous Down Counter using T-Flip Flops which will count the following sequence 0 – 14 – 10 – 8 – 7 – 5 – 3 - 0…..Also draw the connection diagram. **5**

B Based on the waveforms in Fig. 4(a), what can be the most likely problem with the register circuit in Fig. 4(b)? Describe in detail. **3**

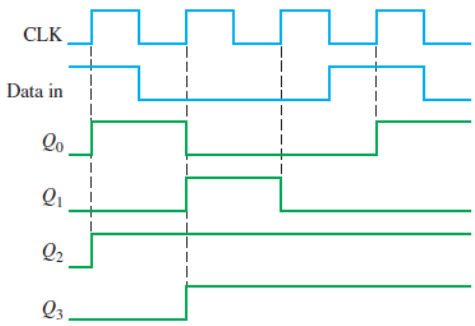


Fig. 4(a)

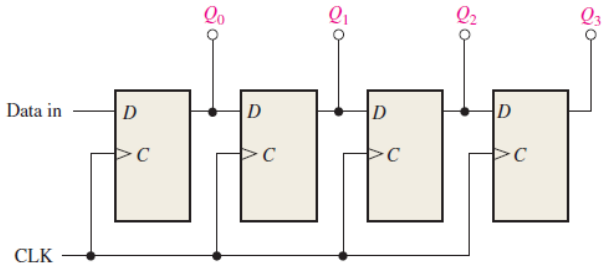


Fig. 4(b)

C Using a single opamp, design a circuit to produce the following ouput voltage. Assume C=2 micro Faraday. **2**

$$v_o = -\int_0^t (v_1 + 4v_2 + 10v_3)\,dt$$

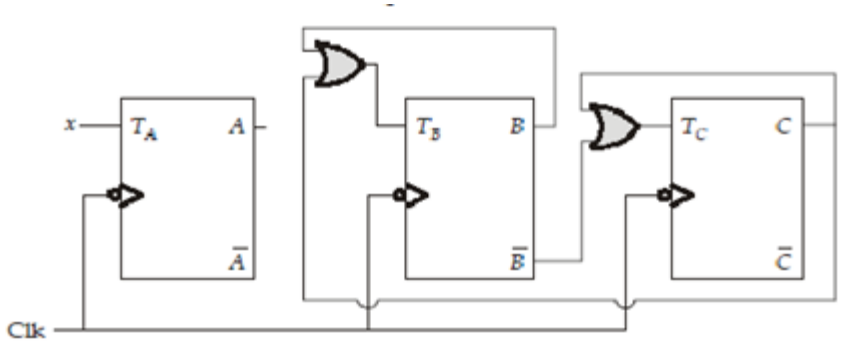
Q.5 **A** The following sequence of operations is performed in the Accumulator: **6**

$$\begin{aligned} p_3&: \quad A \leftarrow \overline{A} \\ p_9&: \quad A \leftarrow A + 1 \\ p_1&: \quad A \leftarrow A + B \\ p_3&: \quad A \leftarrow \overline{A} \\ p_9&: \quad A \leftarrow A + 1 \end{aligned}$$

a. Determine the content of A after each micro-operation, if initially A=1101 and the input B = 0110.
b. Repeat for A = 0110 and B = 1101.
c. Predict the operation performed by the stated sequence of micro-operations.

B For the below circuit, considering x=B(A+C'), **4**

a. Write down Present State and Next State Table
b. Determine the Modulus M



---------- All The Best ----------