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END SEMESTER EXAM

[U19CS012]

SUBJECT : DIGITAL ELECTRONICS & LOGIC DESIGN (EC207)
ROLL NO : U19CS012
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DIVISION : A
BRANCH : COMPUTER SCIENCE ENGINEERING (CSE)
No. of Pages :
Sign : Bhagya

Q1.) (A)

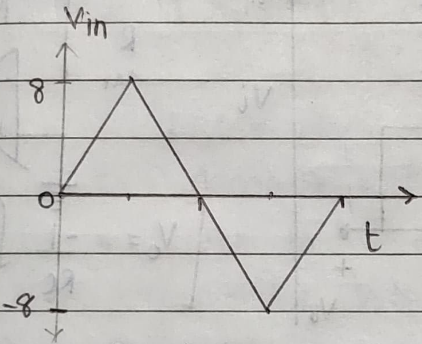
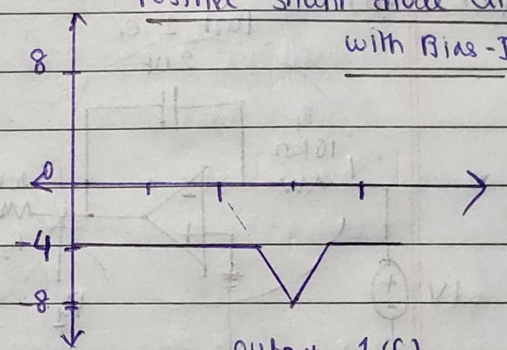


Fig 1(a)

Step ① →

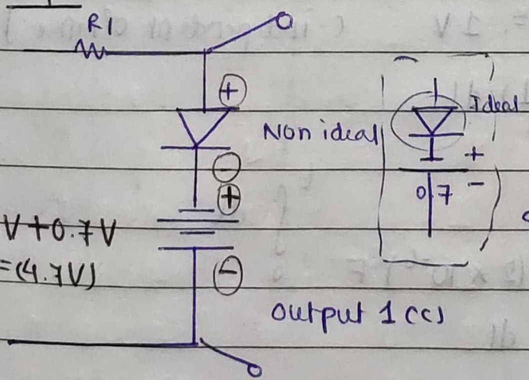
Positive shunt diode Clipper with Bias - II



output 1(C)

↓ Step ② Positive Clamper with Positive Bias

Step 1 :



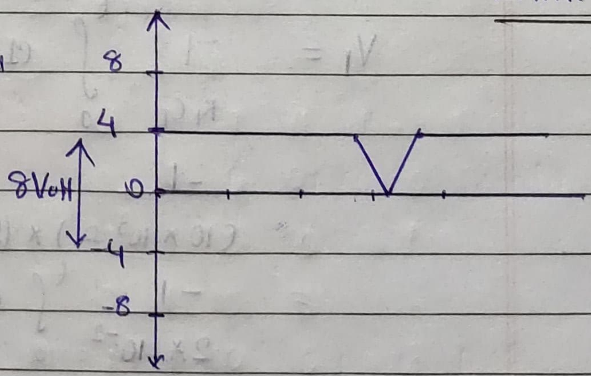
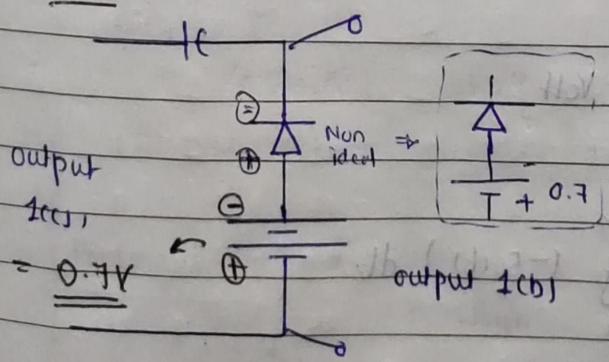


Fig 1(b)

Step 2 :



Combined circuit drawn on Next page →

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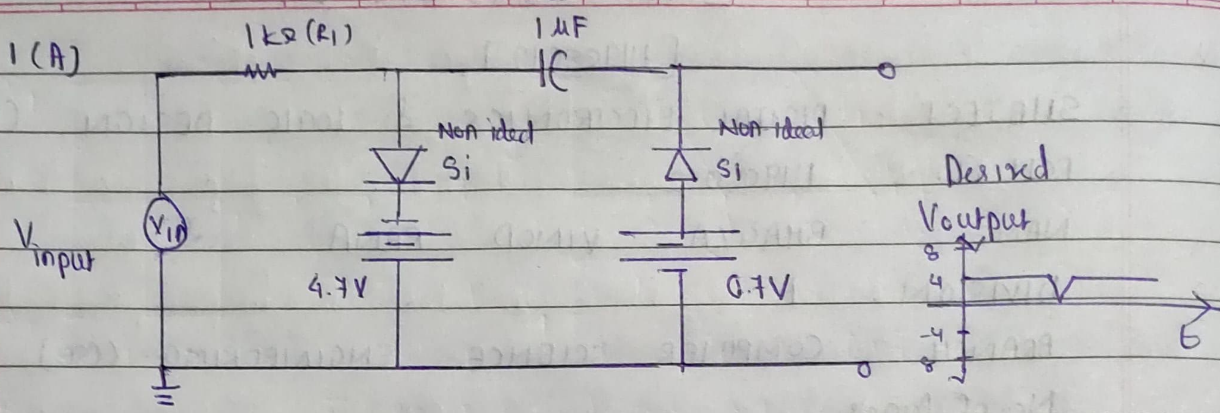
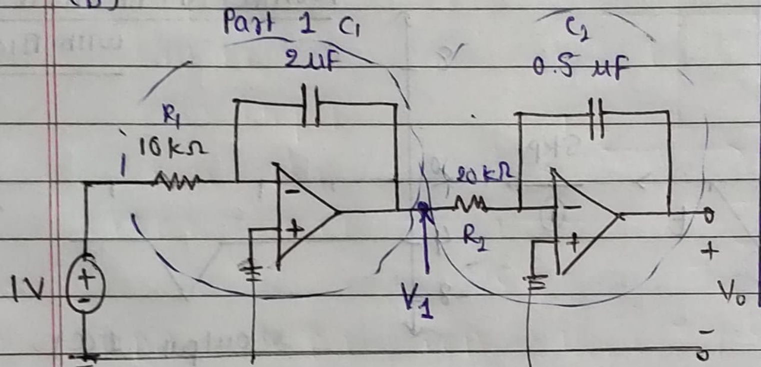
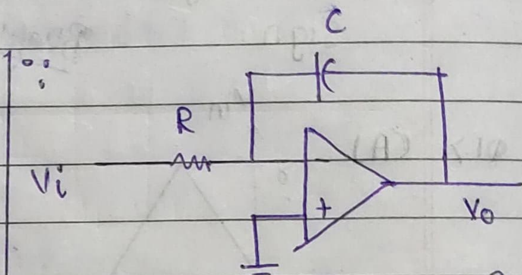
Ans 1 (A)



(Q1) (B)





$$\left[V_o = \frac{-1}{RC} \int V_i(t)\,dt \right]$$

After part 1

$V_i = 1V$ (independent of time)

$$V_1 = \frac{-1}{R_1 C_1} \int_0^t (1)\,dt$$

$$= \frac{-1}{(10 \times 10^3 \,\Omega) \times (2 \times 10^{-6})\,F} \int_0^t dt$$

$$= \frac{-1}{2 \times 10^{-2}} \int_0^t dt$$

$$= -50\,(t)_0^t$$

$$(V_1) = -50(t) \text{ Volt}$$

After part 2,

$$V_o = \frac{-1}{R_2 C_2} \int_0^t (-50(t))\,dt$$

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$$V_o = \frac{50}{(20\times10^3)\,\Omega \times (0.5\times10^{-6})\,F} \int_0^t (t)\,dt$$

$$= \frac{50}{20\times0.5\times(10^{-3})} \int_0^t (t)\,dt$$

$$= \frac{\cancel{50}^{10}}{\cancel{20}} \times \frac{\cancel{10}^{5}}{\cancel{5}} \times (1000) \left.\frac{t^2}{(2)}\right|_0^t$$

$$V_o = \boxed{2500\,(t^2)}$$

at time = 6 mill seconds $= (6\times10^{-3})$ S

$$= 2500 \times (6\times10^{-3})^2$$

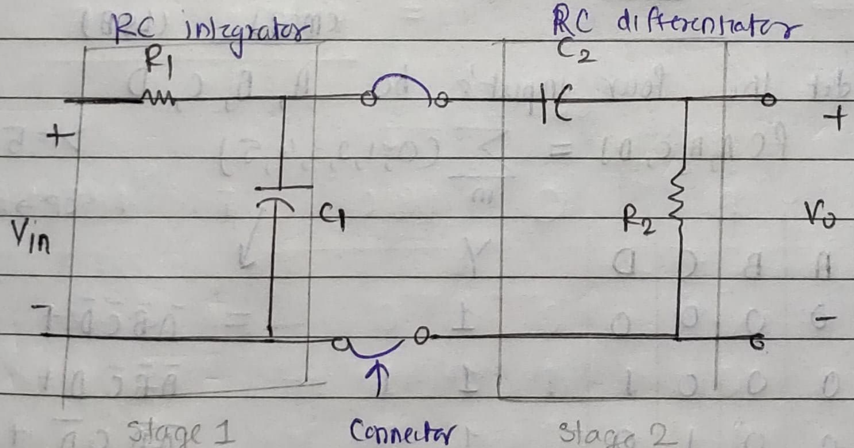
$$= 90000 \times 10^{-6}$$

$$= 9\times10^{-2} \text{ volt}$$

Ans: $= 0.09$ Volt

(I(B)) $= 90$ mill volt

(1) (C)



Low Pass RC circuit — High Pass RC circuit

if $R_1C_1 >> T$ (Given) Stage 1

Then, Low Pass ckt → $\boxed{\text{Integrator}}$

$\because R_2C_2 << T$ (Given) Stage 2

RC High Pass circuit $\xrightarrow{\text{act as}}$ $\boxed{\text{Differentiator}}$

$\int$ Rectangular ⟶ Triangle waveform

diff (triangular) = (Square wave)

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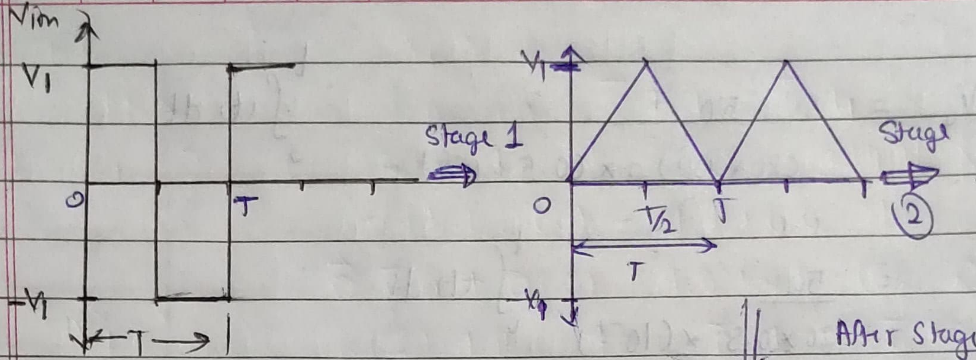
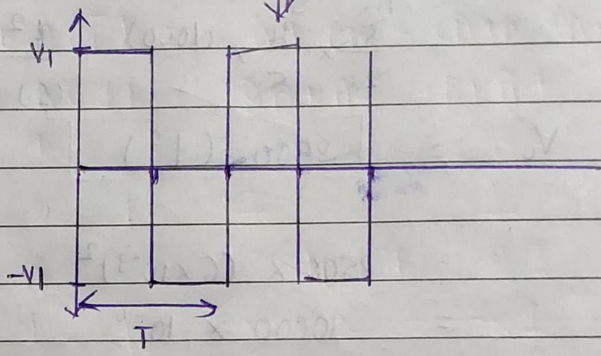


Ans:
Output = will be same input circuit



Q2.

2.) (A) 4-Bit BCD Logic

(MSB) (LSB)

Let the four input's be A, B, C, D

$$f(A,B,C,D) = \sum_m (0,1,2,3,4,5)$$

$>=5$

SOP → ①

Decimal	A	B	C	D	Y
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	0

$= \bar{A}\bar{B}\bar{C}\bar{D} +$
$\bar{A}\bar{B}\bar{C}D +$
$\bar{A}\bar{B}C\bar{D} +$
$\bar{A}\bar{B}CD +$
$\bar{A}B\bar{C}\bar{D} +$
$\bar{A}B\bar{C}D$

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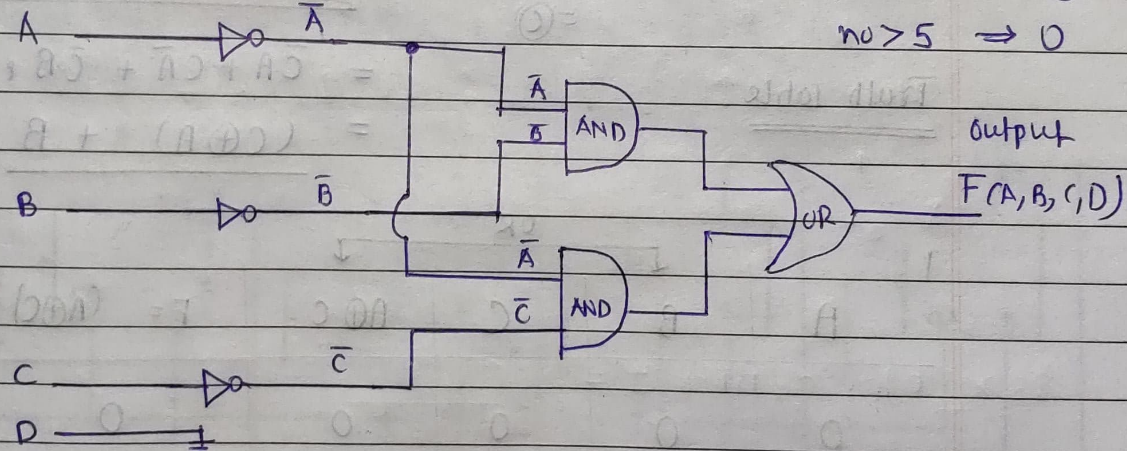
AB \ CD	$\bar{C}\bar{D}$ 00	$\bar{C}D$ 01	CD 11	$C\bar{D}$ 10
$\bar{A}\bar{B}$ 00	1 (0)	1 (1)	1 (3)	1 (2)
$\bar{A}B$ 01	1 (4)	1 (5)	(7)	(6)
AB 11	(12)	(13)	(15)	(14)
$A\bar{B}$ 10	(8)	(9)	(11)	(10)

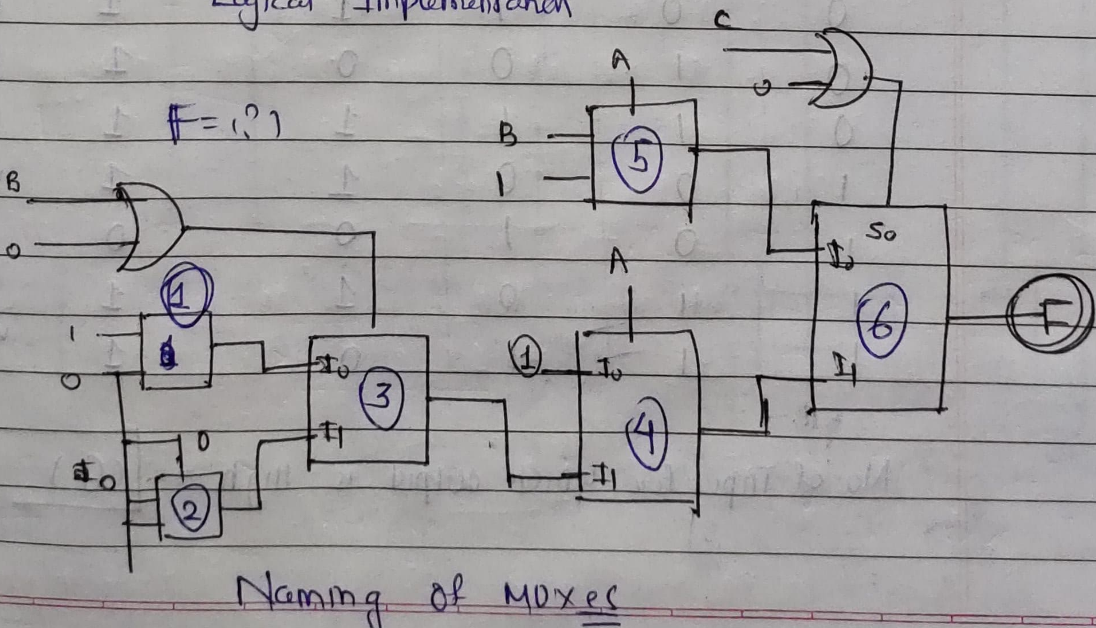
$F(A,B,C,D) = \bar{A}\bar{B} + \bar{A}\bar{C}$

Output
If no <= 5 ⇒ 1
no > 5 ⇒ 0



Logical Implementation

(b)(2) (B)   F = (?)



Naming of MUXes

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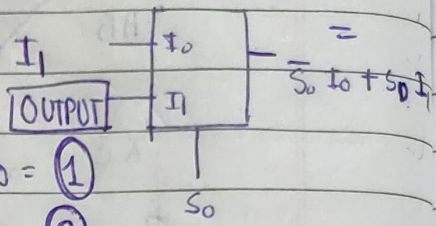
MUX   Expression = $\bar{S_0} I_0 + S_0 I_1$



I_0 I_1

1 $\bar{0}(1) + 0(0) = 1.1 + 0.0 = 1$

2 $\bar{0}\,0 + 0(0) = 1.0 + 0.0 = 0$

3 $\bar{B}(1) + B(0) = \bar{B}.1 = \bar{B}$

$\boxed{1}$ $\boxed{\bar{B}}$ ← 4 $\bar{A}(1) + A(\bar{B}) = \bar{A} + A\bar{B} = (\bar{A}+A)(\bar{A}+B) = \bar{A}+B$

$\boxed{B}$ $\boxed{1}$ 5 → $\bar{A}(B) + A(1) = \bar{A}B + A = (B+A)$

6

For Last mux

I_0	I_1	S_0	output (F)
↓	↓	↓	
$(B+A)$	$(\bar{A}+B)$	$C+0 = C$	$\boxed{\bar{C}(B+A) + C(\bar{A}+B)}$

$= \bar{C}A + C\bar{A} + \bar{C}B + CB$

$= (C \oplus A) + B \quad (C+\bar{C}=1)$

Truth Table

OR

A	B	C	$A \oplus C$	$F = (A \oplus C) + B$	
0	0	0	0	0	
0	0	1	1	1	✓
0	1	0	0	1	✓
0	1	1	1	1	✓
1	0	0	1	1	✓
1	0	1	0	0	
1	1	0	1	1	✓
1	1	1	0	1	✓

No. of Input for which output is High = $\boxed{(6)}$

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Q2.> (C) LED will Light in Forward Bias

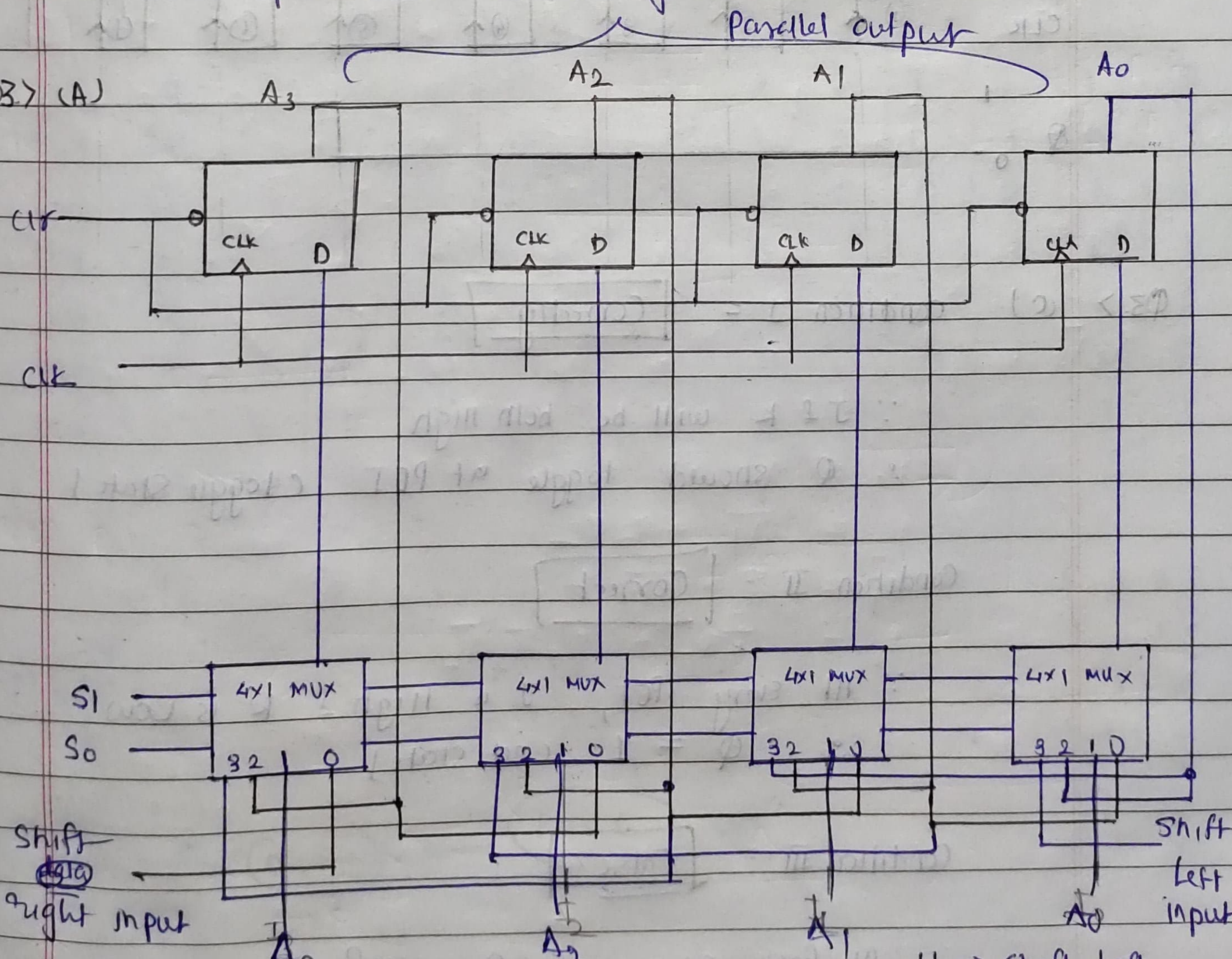
Led glow if $\boxed{P \oplus Q = 0}$

X	Y	Z	Sum $P = A \oplus B \oplus C_{in}$ $X \oplus Y \oplus Z$	carry q $XY + YZ + XZ$	$P \oplus Q$
0	0	0	0	0	0 ← ✓
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	1
1	0	0	1	0	1
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	1	1	0 ← ✓

Ans:

No. of input comb. LED will glow = (2)

Q3.> (A)



11 → shift Left

00 → shift Right 01 → Parallel shift 10 → No change

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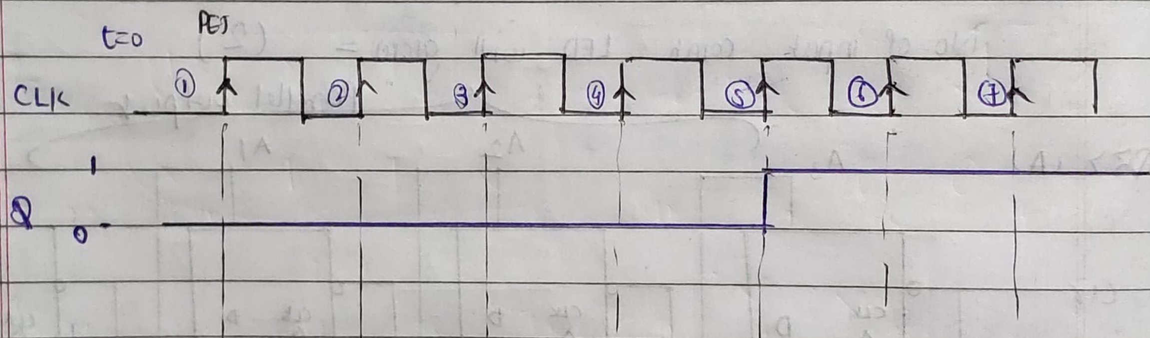
Q3.> (B)

	J_1	J_2	J_3	K_1	K_2	K_3	J (set)	K (re)	Q	State
t=0									0	
CLK=1	1	0	0	0	0	1	0	0	0	Hold
CLK=2	1	1	0	1	0	0	0	0	0	Hold
CLK=3	0	0	0	1	1	1	0	1	0	(Reset)
CLK=4	0	1	1	1	1	0	0	0	0	Hold
CLK=5	1	1	1	0	0	1	1	0	1	Set
CLK=6	0	1	1	0	1	0	0	0	1	Hold
CLK=7	1	0	1	0	1	1	0	0	1	Hold



Q3.> (C) Condition I = $\boxed{\text{Correctly}}$

∵ J & K will be both high

∴ Q should toggle at PET (Toggle State)

Condition II = $\boxed{\text{Correct}}$

∵ At every PET, J is High & K is Low

∴ Q = 1 (Set State)

Condition III = $\boxed{\text{False}}$

∵ At first Edge, Q = 0, J & K = both are LOW

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∴ JK FF is in hold state
∴ Q → no change
But it showed changes

Condition 4 : J = 0 K = 1 ⇒ Reset state

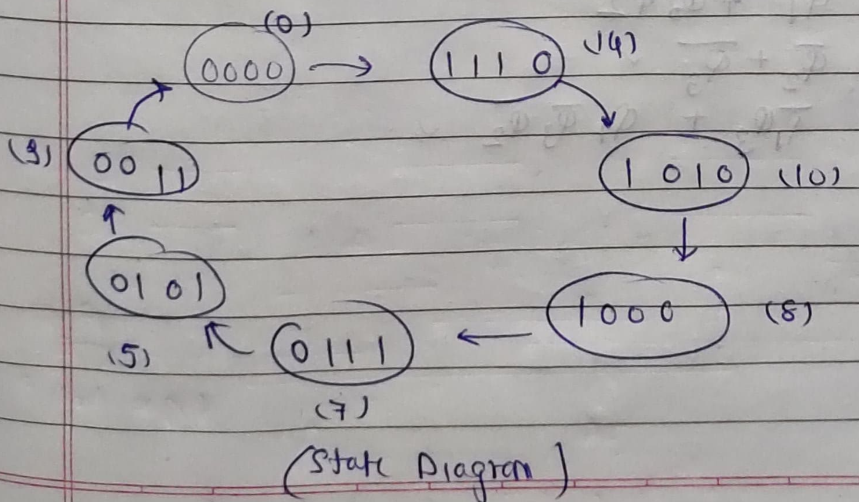
$\boxed{\text{FALSE}}$

∴ J is Low & K is High
∴ Q → 0 (Reset)
But waveform toggles, ∴ Incorrect

[$Q_n \oplus Q_{n+1}$]
(using Excitation)

Q4.) (A)

		Present State				Next State							
		Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+	T_3	T_2	T_1	T_0
t_n	0	0	0	0	0	1	1	1	0	1	1	1	0
t_{n+1}	14	1	1	1	0	1	0	1	0	0	1	0	0
t_{n+2}	10	1	0	1	0	1	0	0	0	0	0	1	0
t_{n+3}	8	1	0	0	0	0	1	1	1	1	1	1	1
t_{n+4}	7	0	1	1	1	0	1	0	1	0	0	1	0
t_{n+5}	5	0	1	0	1	0	0	1	1	0	1	1	0
t_{n+6}	3	0	0	1	1	0	0	0	0	0	0	1	1



(State Diagram)

8 4 2 1
1 1 1 0
1 0 1 0
1 0 0 0
0 1 1 1
1 0

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$[T_3 = \overline{Q_1}\,\overline{Q_0}]$

$Q_3Q_2 \backslash Q_1Q_0$	00 ($\overline{Q_1}\,\overline{Q_0}$)	01	11	10
00	1		0	
01	X	0	0	0
11	X			0
10	1			

$T_2 = \boxed{\overline{Q_1}} + Q_3Q_2$

$Q_3Q_2 \backslash Q_1Q_0$	00 ($\overline{Q_1}\,\overline{Q_0}$)	01 ($\overline{Q_1}Q_0$)	11	10
00	1	X	0	
01	X	1	0	
11	X	X	X	1
10	1	X		0

$T_1 = \overline{Q_3} + \overline{Q_2}$

$Q_3Q_2 \backslash Q_1Q_0$	00 ($\overline{Q_1}\,\overline{Q_0}$)	01	11	10
00 ($\overline{Q_3}\,\overline{Q_2}$)	1	X	1	X
01 ($\overline{Q_3}Q_2$)	X	1	1	X
11 (Q_3Q_2)				0
10 ($Q_3\overline{Q_2}$)	1	X	X	1

$T_0 = Q_3\overline{Q_1} + Q_1\overline{Q_3}\,\overline{Q_2}$

$Q_3Q_2 \backslash Q_1Q_0$	00 ($\overline{Q_1}\,\overline{Q_0}$)	01 ($\overline{Q_1}Q_0$)	11 (Q_1Q_0)	10 ($Q_1\overline{Q_0}$)
00	0		1	X
01		0	0	
11 (Q_3Q_2)	X	X		0
10 ($Q_3\overline{Q_2}$)	1	X		0

$T_3 = \overline{Q_0}\,\overline{Q_1}$

$T_2 = \overline{Q_1} + Q_3Q_2$

$T_1 = \overline{Q_2} + \overline{Q_3}$ ✓

$T_0 = \overline{Q_1}Q_3 + Q_1\overline{Q_3}\,\overline{Q_2}$ ✓

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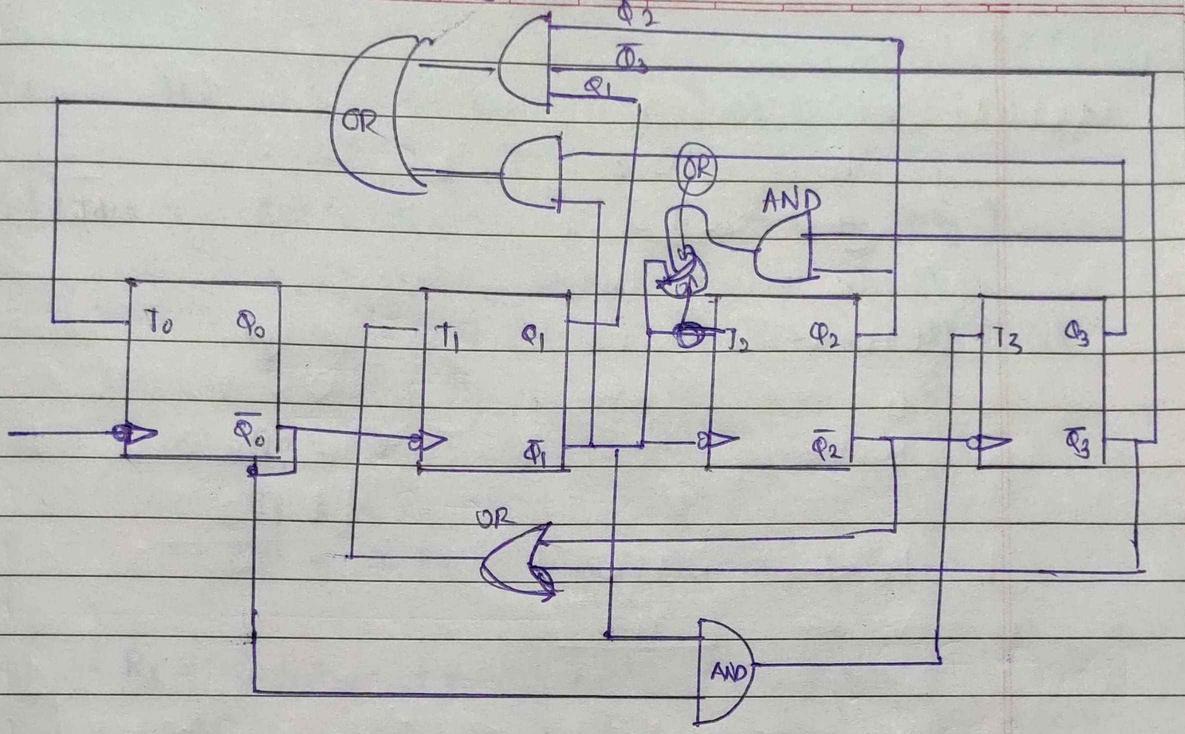

Asyn Down counter of 0-14-10-8-7-5-3-0

(4) (B)

Synchronous circuit → ~~A~~ All clock ~~to~~ same

Two shift ~~of~~ right register has a problem in q_3's D flip-flop that is the input value of Q_3's D terminal has been shorted with power line. Thus we have D of Q_3 as always high.

All other flipflops are working fine.

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(Q4) (c) $V_o = -\int_0^t (V_1 + 4V_2 + 10V_3)\,dt$

① Idea ⇒ first make = $(-V_1 - 4V_2 - 10V_3)$
using summer circuit

$$V_1' = -\frac{R_f}{R_1}(V_1) + -\frac{R_f}{R_2}(V_2) + -\frac{R_f}{R_3}(V_3)$$

$R_f = 1 R_1$

$R_f = 4 R_2$

$R_f = 10 R_3$ let $R_f = \boxed{20}$ kΩ

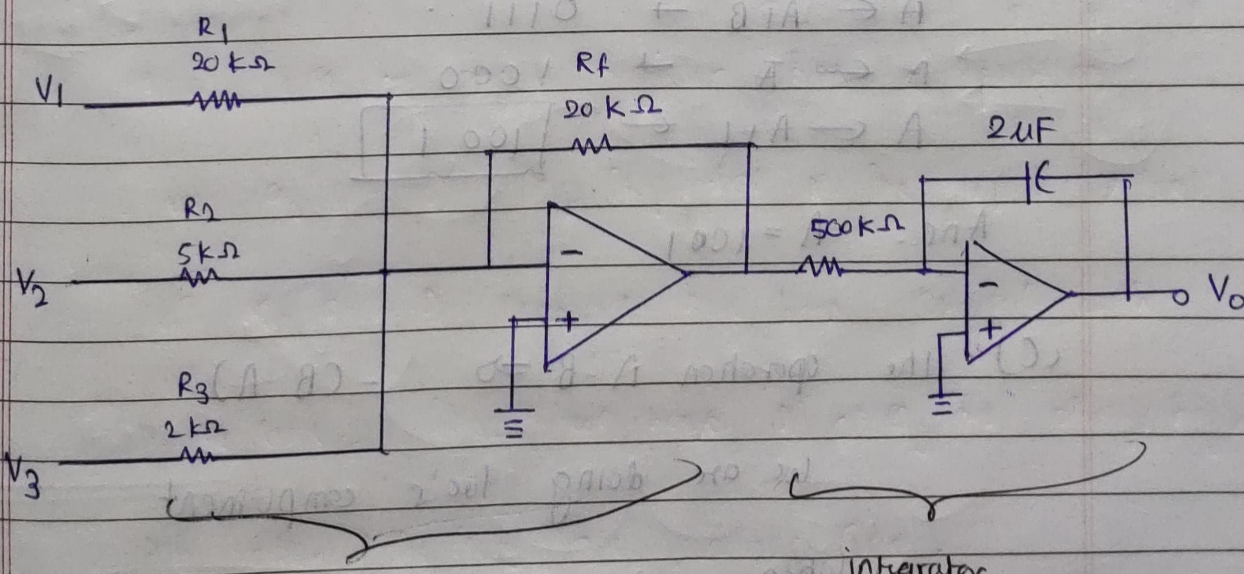
$R_1 = 20$ kΩ $R_2 = 5$ kΩ $R_3 = 2$ kΩ

② for integrating $RC = 1$ $C = 2\,\mu F$

$$R = \frac{1}{2\times 10^{-6}} = \frac{10^6}{2} = 5\times 10^5\ \Omega$$

$$= \boxed{500\ k\Omega}$$

FINAL circuit



∴ $\left[V_o = \int_0^t (-V_1 + -4V_2 - 10V_3)\,dt \right]$

(Q5) (A)

$A = 1101 \qquad B = 0110$

$\overline{A} = 0010$

(1) $A \leftarrow 0010$

$A+1 \leftarrow 0011$

$A \leftarrow A+B$

1001

$$\begin{array}{r} 0011 \\ +\ 0110 \\ \hline \boxed{1001} \end{array}$$

$\overline{A}$

$A \leftarrow 0110$

$A \leftarrow \boxed{0111}$

Ans: content of A after micro op = $\boxed{0111}$

(B) A initially → 0110

$A \leftarrow \overline{A}$ → 1001

$A \leftarrow A+1$ → 1010

$A \leftarrow A+B$ → 0111

$A \leftarrow \overline{A}$ → 1000

$A \leftarrow A+1$ ← $\boxed{1001}$

Ans: $A = 1001$

(C) The operation $A - B \Rightarrow -(B - A)$

we are doing two's complement

when $A \leftarrow \overline{A}$

$A \leftarrow A+1$

(Q5) (a) $X = B(A+\bar{C}) = T_A$ — ①

$T_B = B + C$

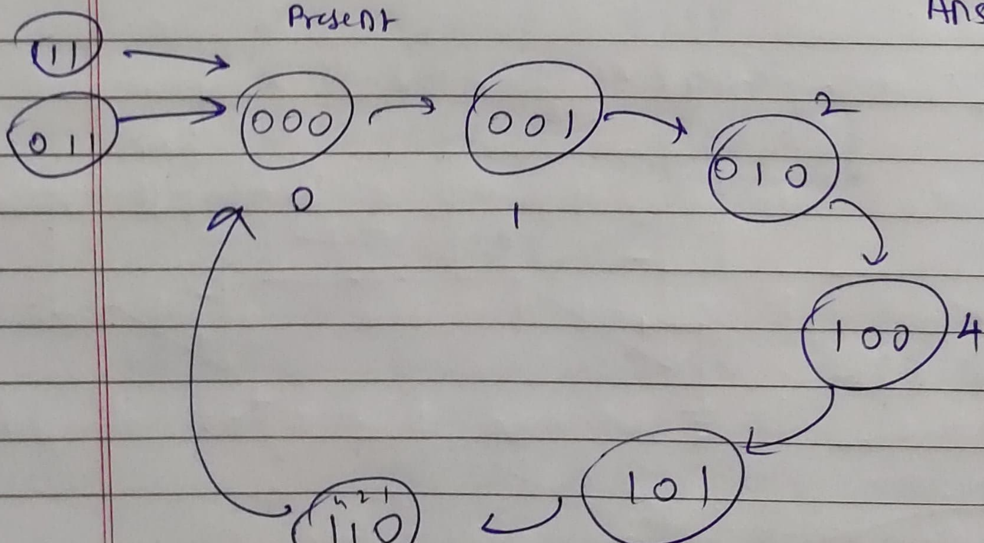
$T_C = \bar{B} + C$

T	Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

	Present State					Toggle			Next State		
$A+\bar{C}$	A	B	C	$\bar{B}$	$\bar{C}$	T_A	T_B	T_C	A	B	C
1	0	0	0	1	1	0	0	1	0	0	1
0	0	0	1	1	0	0	1	1	0	1	0
1	0	1	0	0	1	1	1	0	1	0	0
0	0	1	1	0	0	0	1	1	0	0	0
1	1	0	0	1	1	0	0	1	1	0	1
1	1	0	1	1	0	0	1	1	1	1	0
1	1	1	0	0	1	1	1	0	0	0	0
1	1	1	1	0	0	1	1	1	0	0	0

Present

Answer → Next



6 Valid States

0 → 1 → 2 → 4 → 5 → 6

(b) ∴ It is Mod "6" counter (3 not in case)