Computer Science and Engineering Department, SVNIT, Surat
B. Tech. II CSE (3rd Sem) & B. Tech. II CSE (Minor) (3rd Sem)
End Semester Exam: December 2020
Computer Organization (CS201)
Date: 17th Dec. 2020 Marks:15 Section B

Writing Time: 4:30pm - 5:15 pm Uploading Time: 5:15 to 5:30 pm Instructions:

1. Copy from any book or online material or other answer-book is strictly prohibited. There is NO marks for copied work 2. Use your own examples for explaining the theories.
3. Submit Section A before starting the Section B.
4. Timely uploading of each section is mandatory, late receipt will not be considered in any condition/situation (Each section to be uploaded separately).
5. Answers to be hand written on Answer-sheet like pages.
6. Answers must be uploaded in sequential order of the questions.
7. It is compulsory to mention **Admission No. : Question Number** on each page left top corner and **Page Number** on bottom right corner. Also write **Total Number of Pages on first page left top corner clearly**.

Q.2 MIPS 32-bit processor processes following code on two integer arrays A and B and **[10]**

produces a result in register $s0. Each array consists of 100 words. The base addresses of the arrays A and B are stored in $s1 and $s2 respectively. **Consider this code to answer the following questions:**

Line No. 1		ori $t0, $zero, 100
2		sub $s0, $s0, $s0
3	loop:	lw $s3, 0 ($s1)
4		lw $s4, 0 ($s2)
5		add $s5, $s3, $s4
6		add $s0, $s0, $s5
7		addi $s1, $s1, 4
8		addi $s2, $s2, 4
9		addi $t0, $t0, -1
10		bne $t0, $zero, loop

1. a) Write 'c' language code for this code, and describe what is produced in register $s0. [02]

b) Explain the addressing mode of line no. 10 and calculate the address offset required for [02]

loop in it. Consider the PC for line no. 1 is as your birth year.

c) Write the instruction formats used in this code for different instructions. Calculate the [02]

total clock cycles required for this code, if executed on multi cycle processor. 2. Identify the data hazard(s) which may affect the execution of the above code. Also, with [04]

the help of pipeline diagram, explain the solution for the data hazards.

OR

Identify the control hazard(s), if any present(s) in the above code. Explain different

solutions to resolve and provide one detailed solution for this code. Also discuss the execution time affected in terms of clock cycles before and after of your solution.

Q.3 Answer the following questions: [05] 1) List the levels of computer which are only machine dependent. [01] 2) Explain the hierarchical bus and its need. [02]

3) Which is the best way to design the circuit using ASIC or FPGA? Justify your answer. [02]

* * *