MICROPROCESSOR AND INTERFACING TECHNIQUES
B.TECH - II (IV SEMESTER)

Total Marks : 30 **TIME : 45 Min. (including UPLOAD time)**

1	Draw timing diagram for following instruction:(assume CALL was placed at 2500H and SP is set to 4000H) ***3405 RNC***	03
2	Determine physical address for the following 8086 instruction: (i) MOV AL, CS:[BX+0400], (ii) MOV AL, [BX+SI+FF] , ASSUME CS =4000H, IP 2300H, BX= 3500, SI = 2300H and DS =5000H	02
3	Write two separate ALP in 8085 to calculate the 1's and 2's complement of two successive memory locations 8500H and 8501H and store them in four consecutive memory locations starting from 8600H	04
4	Write a program to generate a square wave using 8255.	03
5	Calculate the total time delay for the following:(consider 5MHz clock frequency) ***MVI B, 80H*** ***LOOPII : MVI C,FFH*** ***LOOPI : DCR C*** ***JNZ LOOPI*** ***DCR B*** ***JNZ LOOPII***	04
6	In 8086, what instruction is most similar to (i) CMP (ii) TEST	02
7	Enlist parameter passing techniques in 8086. Discuss with example(code) any one.	04
8	Write results after execution of following instructions: (ii) MOV CL,2F ; MOV AL,1D ; SUB AL, CL (ii) MOV AX,8796 ; MOV CL,2 ; ROR AX, CL	02
9	Write 8085 ALP to read the count value of the counter while counting is going on. Assume counter 0 in Mode 0 with count value 7000H	03
10.	Write a control word for counter 1 of 8253 / 8254 for the following options: load least significant byte only, mode 5 of operation and binary counting. Write an instruction sequence that will load the control word into 8253 / 8254 that is located at address 0100H. Assume that 8253 / 8254 is attached to the I/O bus of the CPU and the address inputs A_0 and A_1 are supplied by A_2 and A_3 respectively.	03