DELD

Unit 3

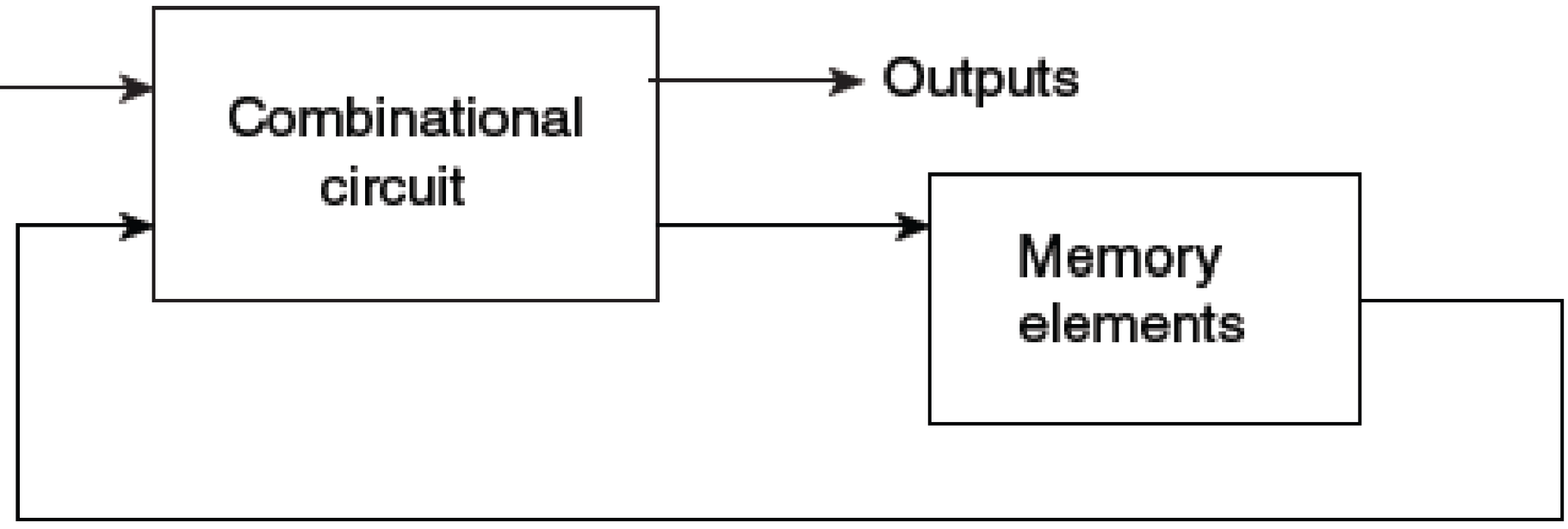
Sequential Circuits

Electronics Engineering Department

Comparison

COMBINATIONAL CIRCUITS	SEQUENTIAL CIRCUITS
Output depends only on the present value of the inputs.	Output depends on both the present and previous state values of the inputs
These circuits will not have any memory as their outputs change with the change in the input value.	Sequential circuits have some sort of memory as their output changes according to the previous and present values.
There are no feedbacks involved.	In a sequential circuit the outputs are connected to it as a feedback path.
Used in basic Boolean operations.	Used in the designing of memory devices.
Implemented in: Half adder circuit, full adder circuit, multiplexers, de-multiplexers, decoders and encoders.	Implemented in: RAM, Registers, counters and other state retaining machines.

Block Diagram



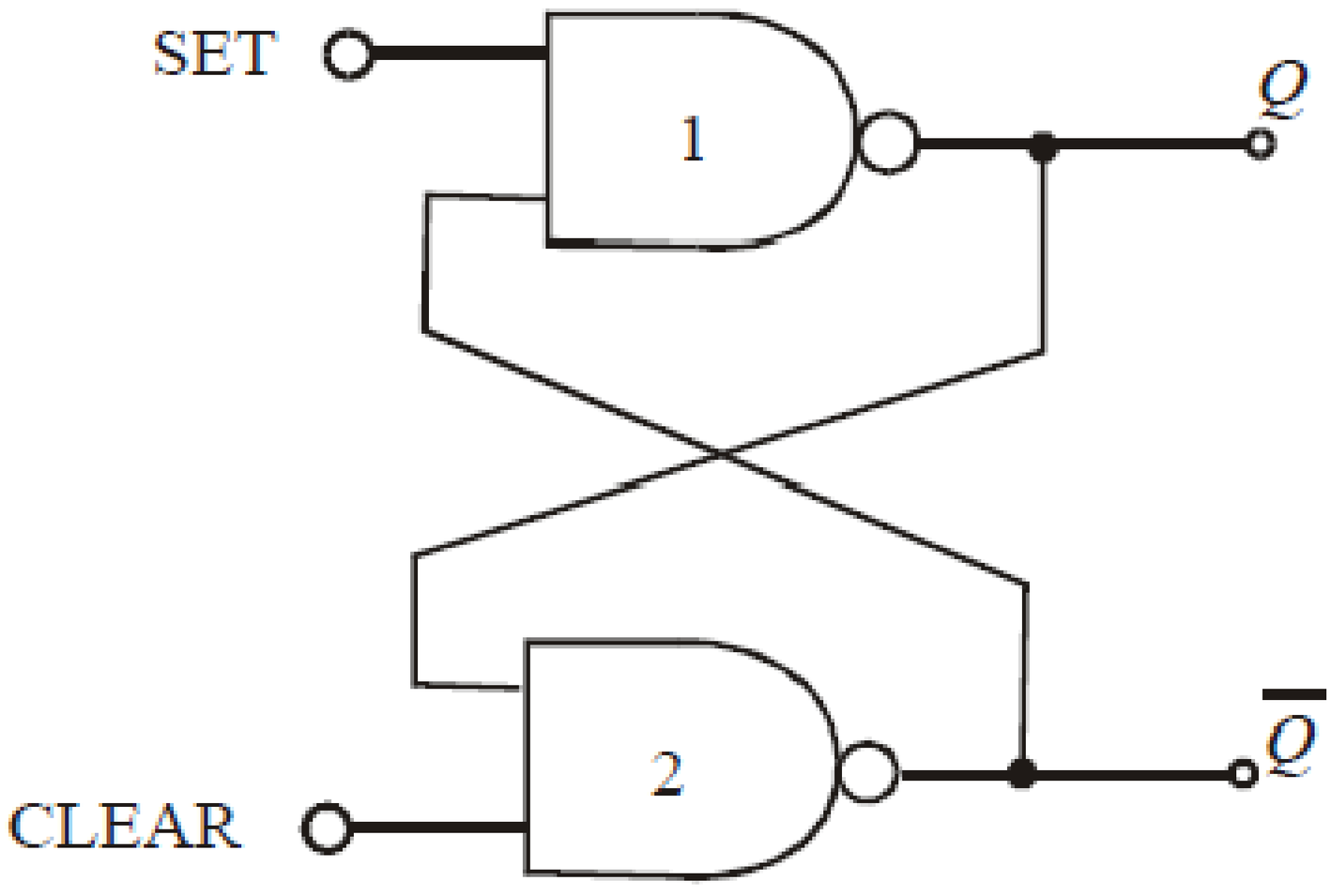
Flip – Flops and its Types

- Basic Memory element of a Digital Computer
- Stores 1 bit of information
- It’s a Bistable device
- Has two outputs, one complement of another (Q and Q’)
- Four Types
  - SR
  - D
  - JK
  - T

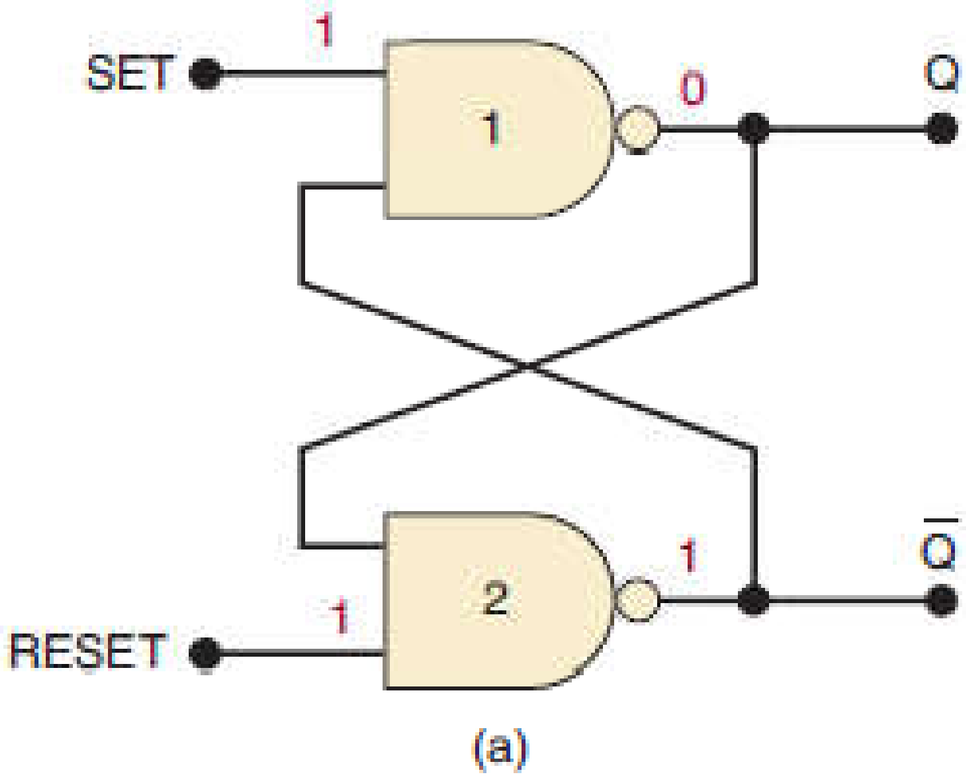
Concept of Latch

- Most basic type of FF circuit
- Can be constructed using NAND or NOR Gates
- These circuits latch to ‘1’ or ‘0’ immediately upon application of inputs
- Two types
  - NAND Gate Latch (Active Low)
  - NOR Gate Latch (Active High)

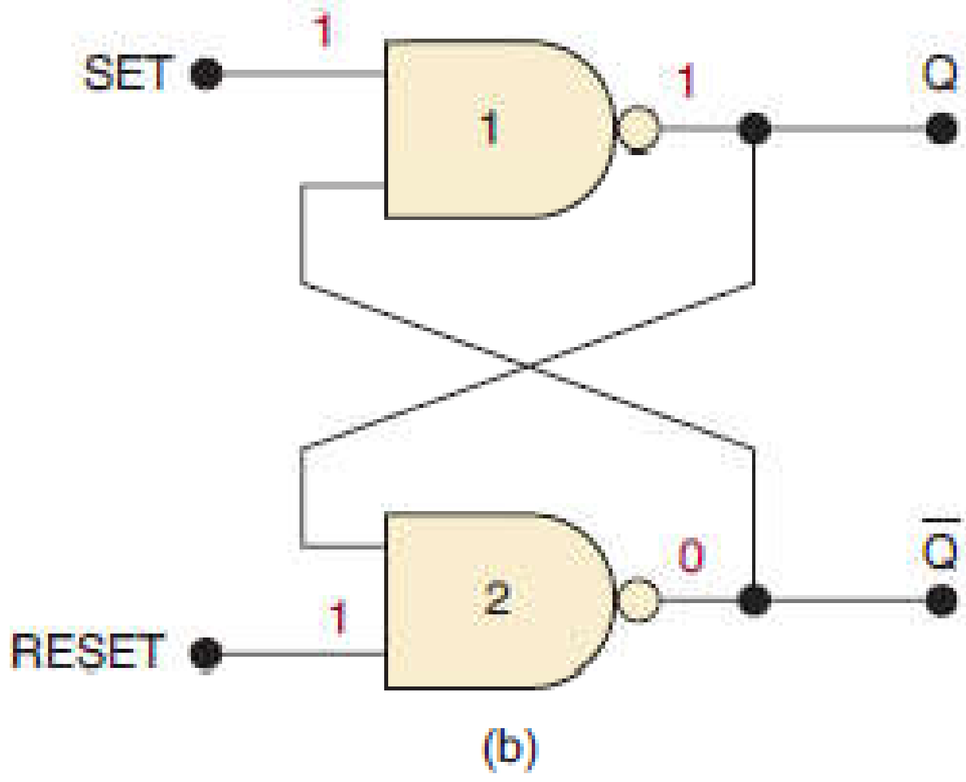
NAND Gate SR Latch



Two Stable States

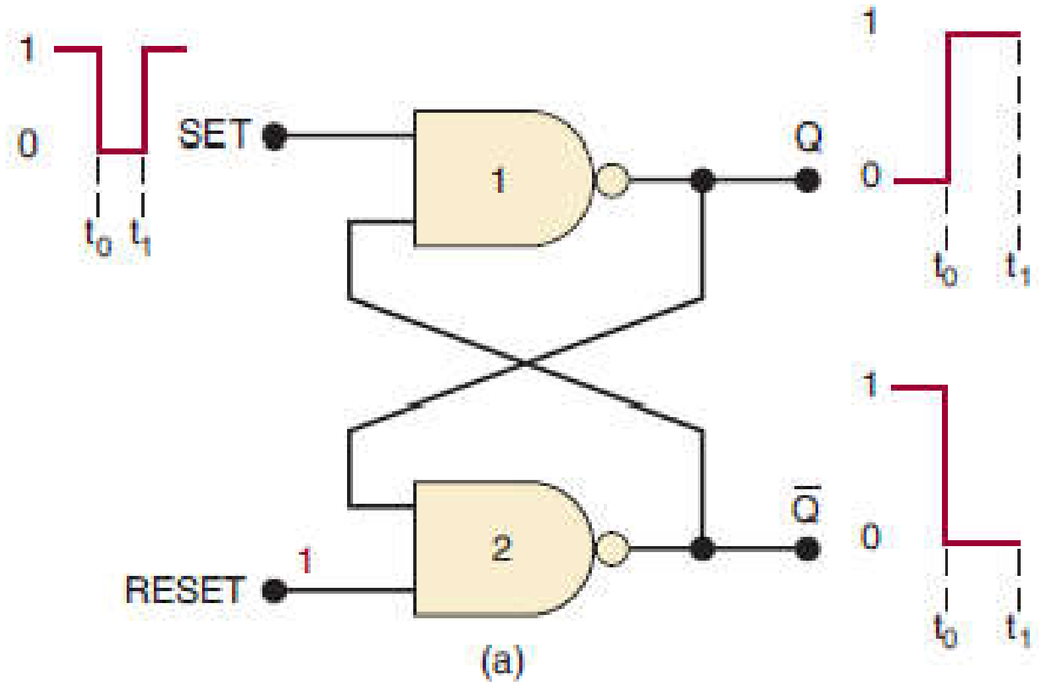


(a)

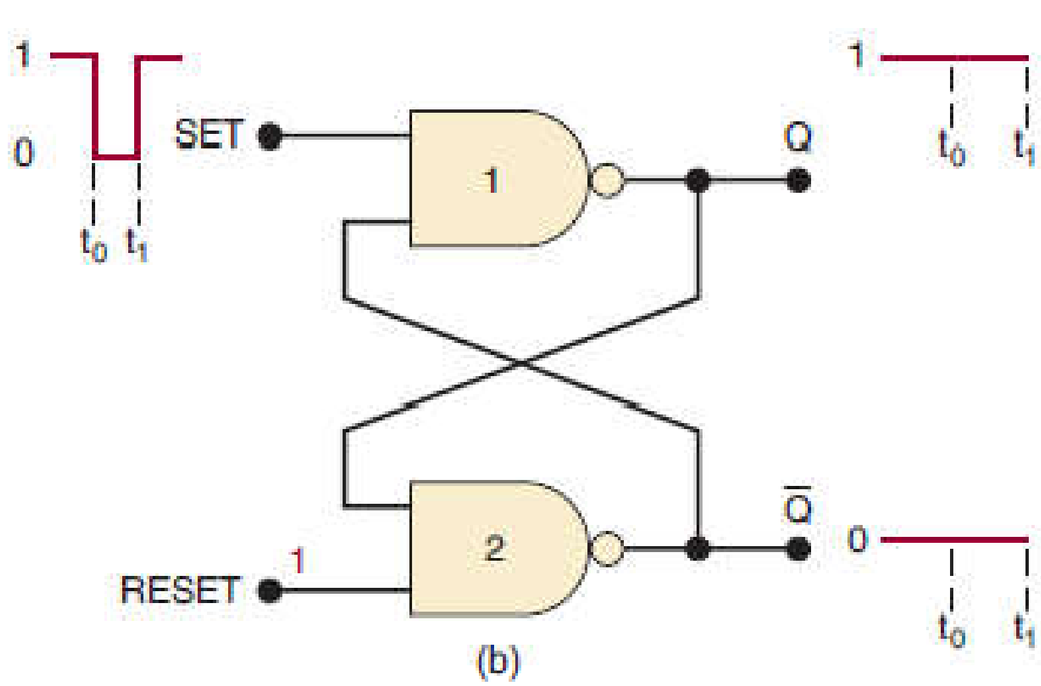


(b)

SET (Q=1)

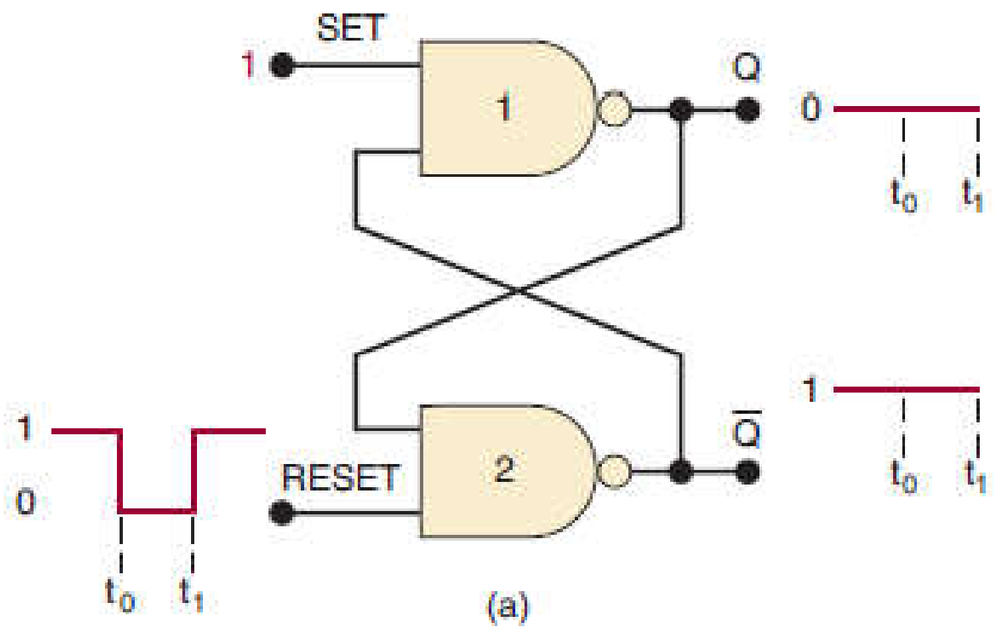

1
0
SET
Q
1
t_0 t_1
1
0
t_0 t_1
$\overline{Q}$
2
1
RESET
1
0
t_0 t_1

(a)

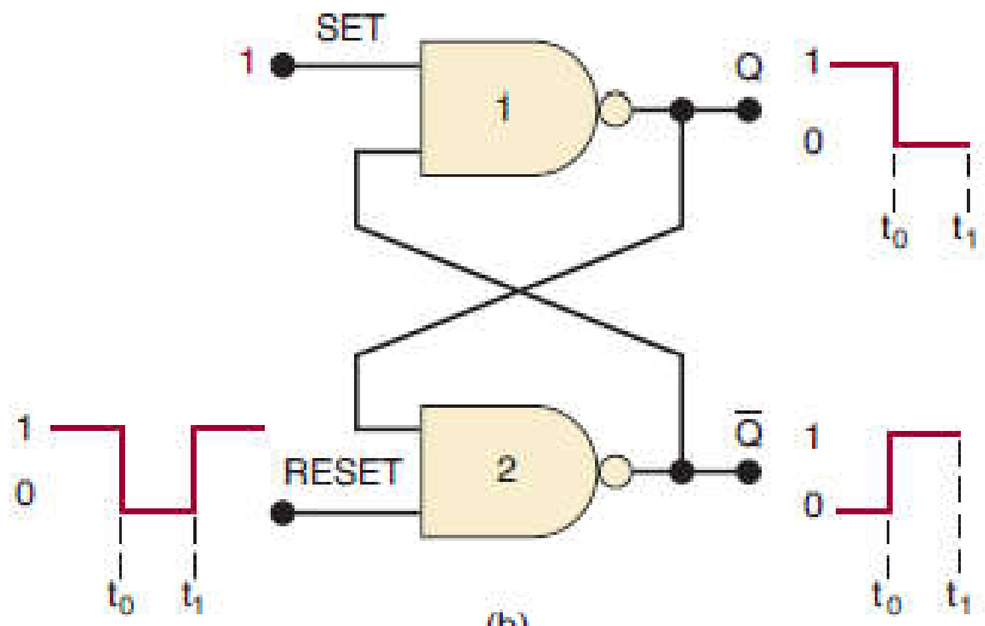

1
0
SET
Q
1
t_0 t_1
$\overline{Q}$
2
1
RESET
1
0
t_0 t_1

(b)

RESET (Q=0)


SET
1
1
Q
0
t_0 t_1
1
0
t_0 t_1
RESET
2
$\overline{Q}$
1
t_0 t_1

(a)

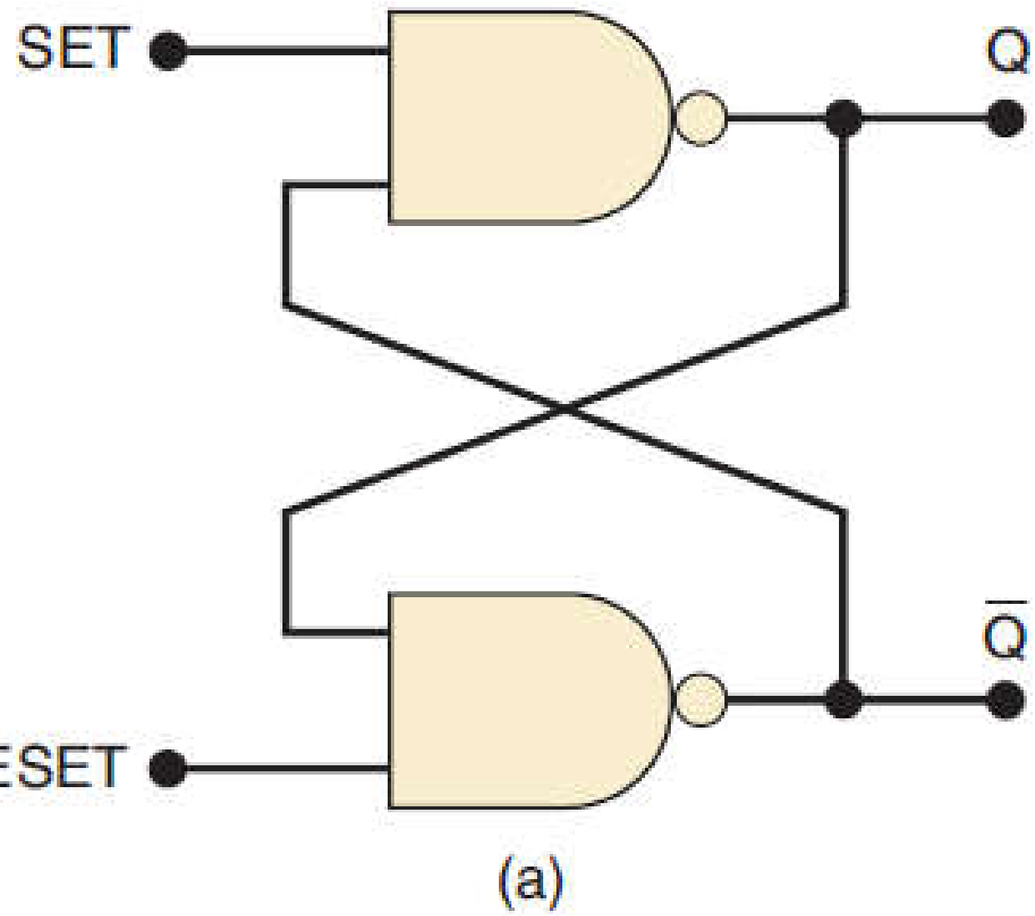

SET
1
1
Q
1
0
t_0 t_1
1
0
t_0 t_1
RESET
2
$\overline{Q}$
1
0
t_0 t_1

(b)

Summary

1. SET = RESET = 1. This condition is the normal resting state, and it has no effect on the output state. The Q and $\overline{Q}$ outputs will remain in whatever state they were in prior to this input condition.
2. SET = 0, RESET = 1. This will always cause the output to go to the $Q = 1$ state, where it will remain even after SET returns HIGH. This is called *setting* the latch.
3. SET = 1, RESET = 0. This will always produce the $Q = 0$ state, where the output will remain even after RESET returns HIGH. This is called *clearing* or *resetting* the latch.
4. SET = RESET = 0. This condition tries to set and clear the latch at the same time, and it produces $Q = \overline{Q} = 1$. If the inputs are returned to 1 simultaneously, the resulting state is unpredictable. This input condition should not be used.

Truth Table



(a)

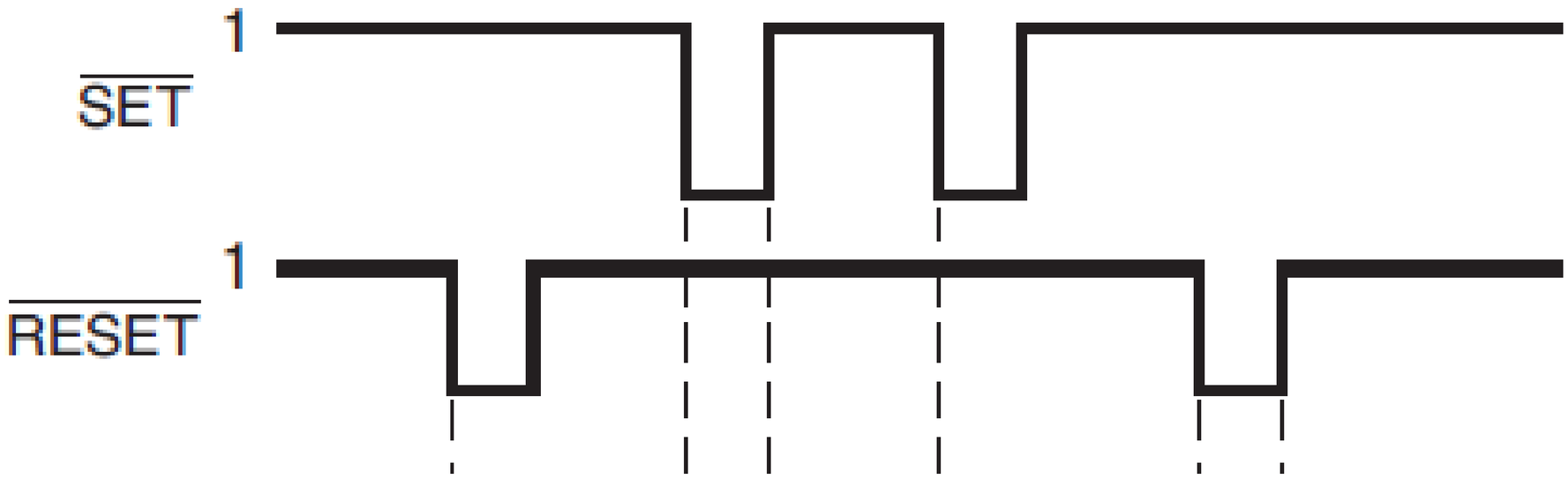
Set	Reset	Output
1	1	No change
0	1	Q = 1
1	0	Q = 0
0	0	Invalid *

*Produces $Q = \overline{Q} = 1$.

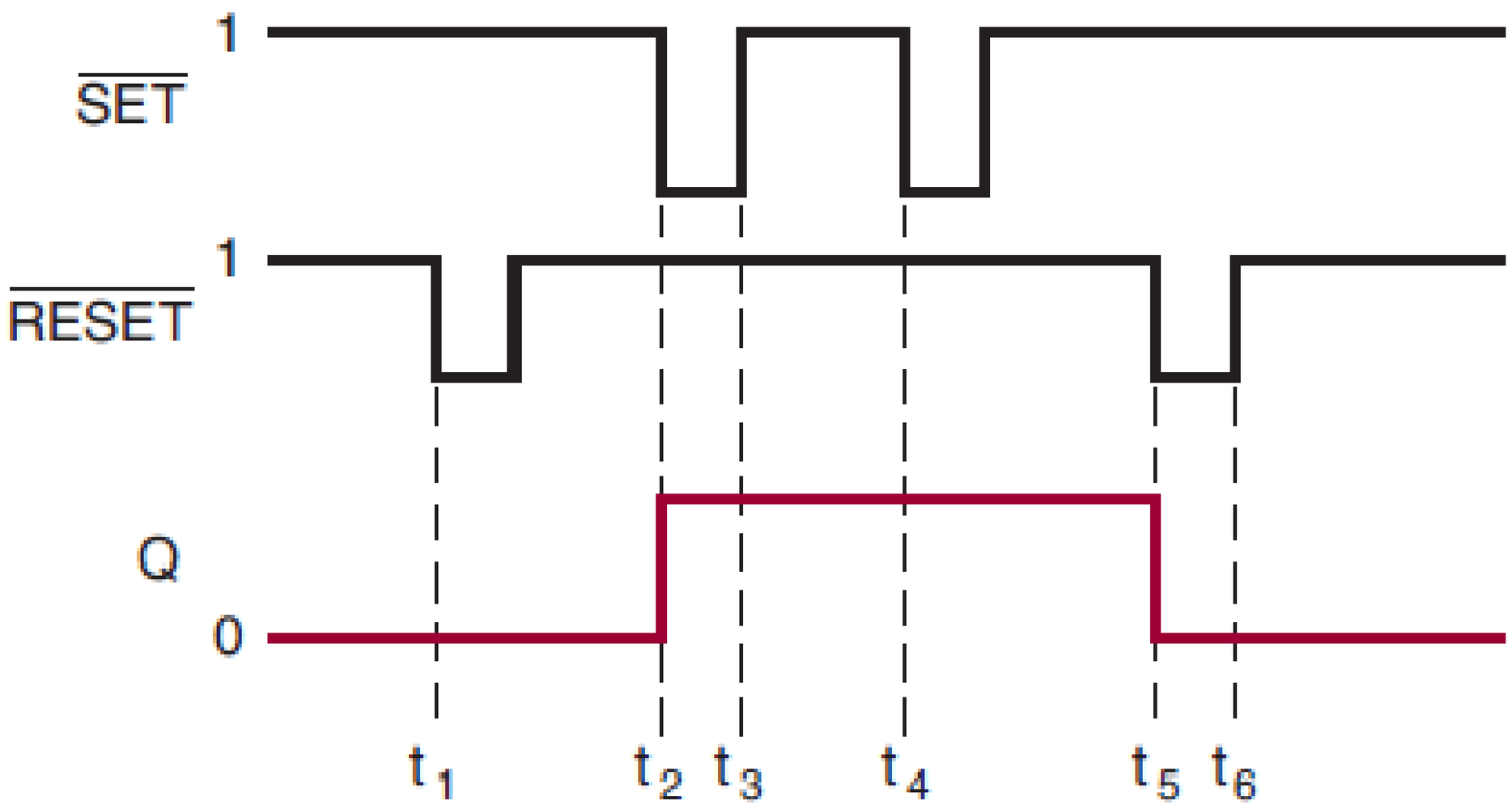
(b)

Concept Check

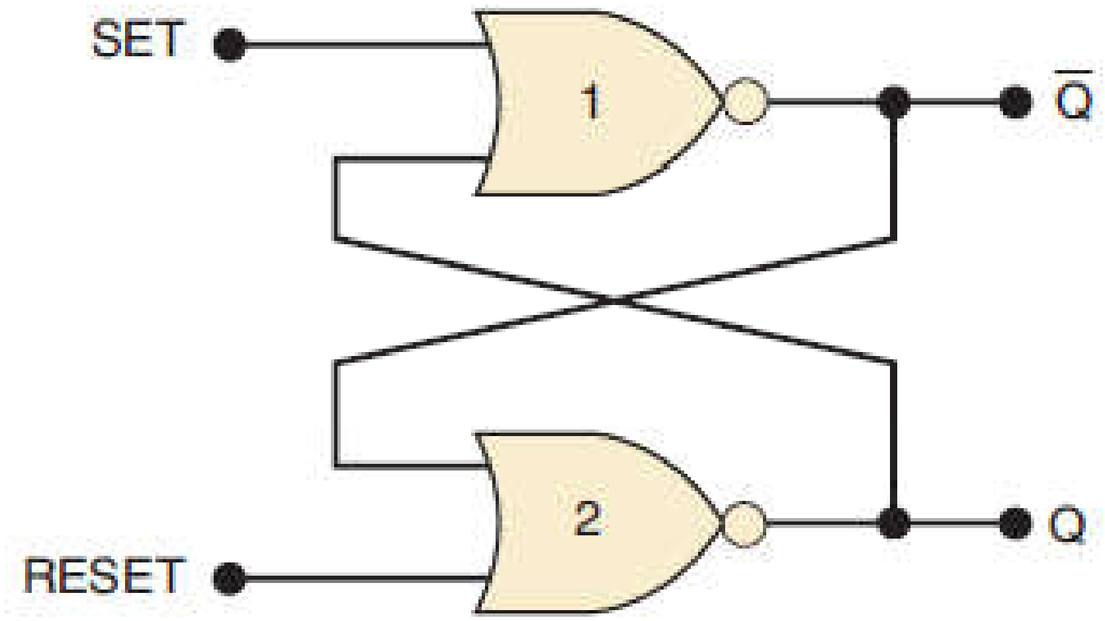
Assuming the Q=0 initially, determine the Q waveform for the NAND Latch



Solution

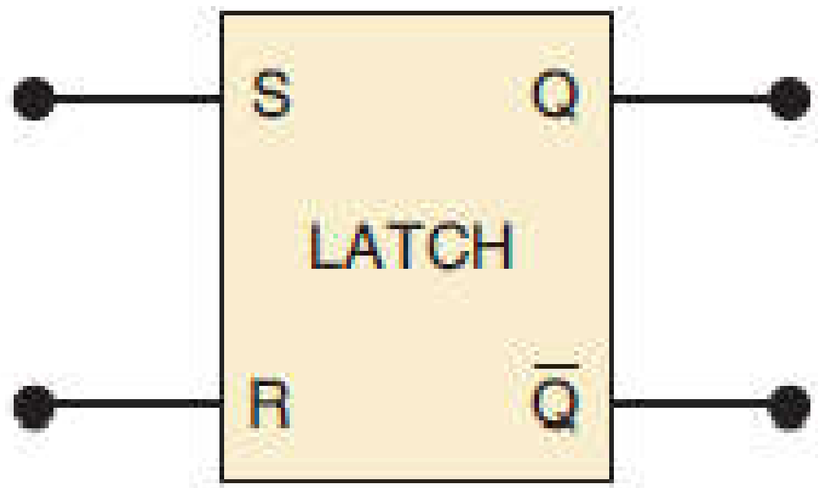


NOR Gate SR Latch



Set	Reset	Output
0	0	No change
1	0	Q = 1
0	1	Q = 0
1	1	Invalid*

*Produces $Q = \overline{Q} = 0$.



Description

1. SET = RESET = 0. This is the normal resting state for the NOR latch, and it has no effect on the output state. Q and $\overline{Q}$ will remain in whatever state they were in prior to the occurrence of this input condition.
2. SET = 1, RESET = 0. This will always set $Q = 1$, where it will remain even after SET returns to 0.
3. SET = 0, RESET = 1. This will always clear $Q = 0$, where it will remain even after RESET returns to 0.
4. SET = 1, RESET = 1. This condition tries to set and reset the latch at the same time, and it produces $Q = \overline{Q} = 0$. If the inputs are returned to 0 simultaneously, the resulting output state is unpredictable. This input condition should not be used.

To be Continued...