Necessity of 8259A

In a system, microprocessor may need to perform the following tasks in an efficient way using interrupt:

- ✓ Read ASCII characters from a keyboard on an interrupt basis.
- ✓ Count interrupts from a timer to produce a real time clock of seconds, minutes and hours.
- ✓ Communicate with an A/D converter.
- ✓ Communicate with a display or printer.
- ✓ Detect several emergency signal like power failure etc on an interrupt basis.

Each of these interrupt applications requires a separate interrupt pin. But, the 8086 has only two interrupt inputs: NMI and INTR. If we use NMI for a power failure interrupt, this leaves only one interrupt input for all other applications.

The solution is to use an external device called a priority interrupt controller (PIC) such as Intel 8259A.

Function of 8259A

- ✓ The Programmable Interrupt Controller (PIC) functions as an overall manager in an interrupt-driven system environment.
- ✓ It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced and issues an interrupt to the CPU based on this determination.
- ✓ Each peripheral device or structure usually has a special program or, routine that is associated with its specific functional or operational requirements; that is referred to as a service routine or service procedure.
- ✓ The 8259A PIC, after issuing an interrupt to the CPU, must somehow input information (interrupt vector number) into the CPU that can point the program counter to the service procedure associated with the requesting device .

Connection of 8259A with 8086 microprocessor (Single Mode)

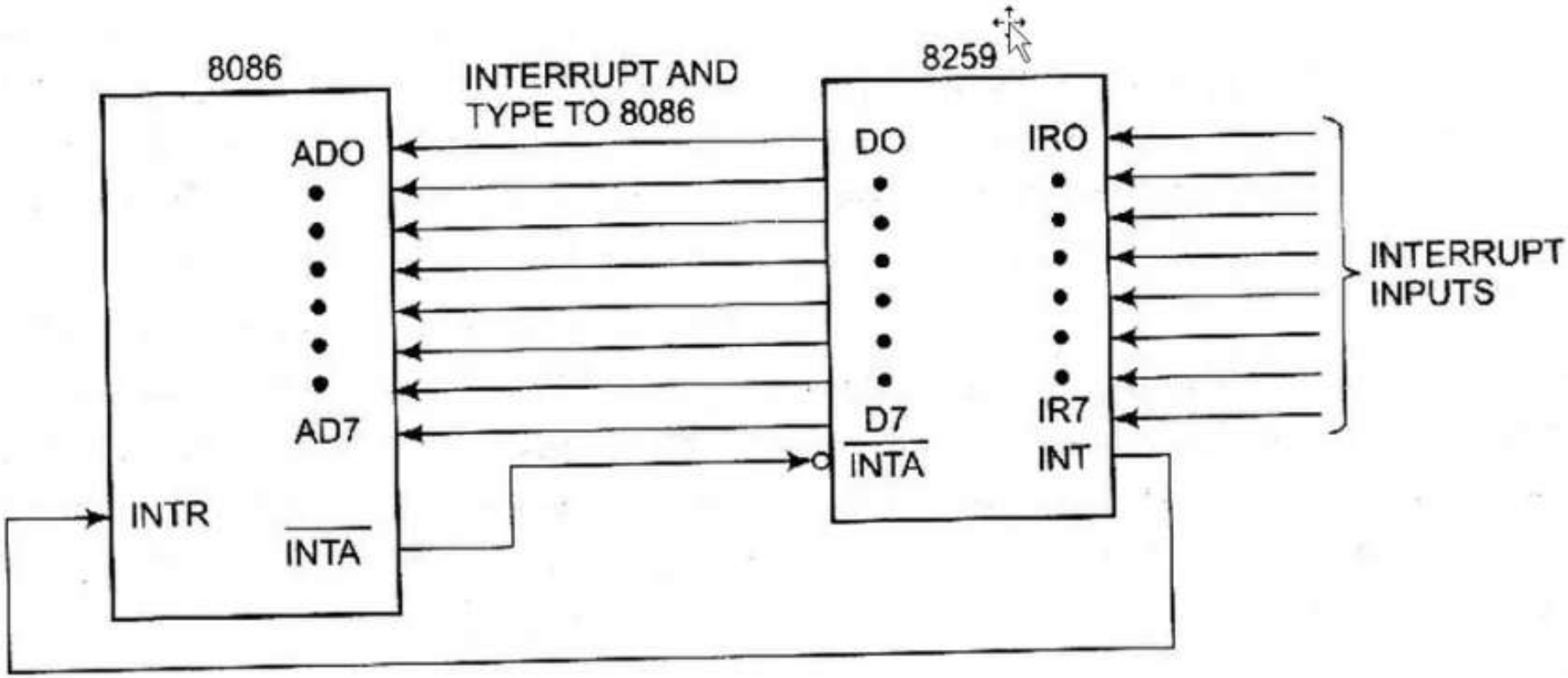

Fig. 1 Block Diagram showing an 8259 connected to an 8086

Connection of 8259A with 8086 microprocessor (Cascade Mode)

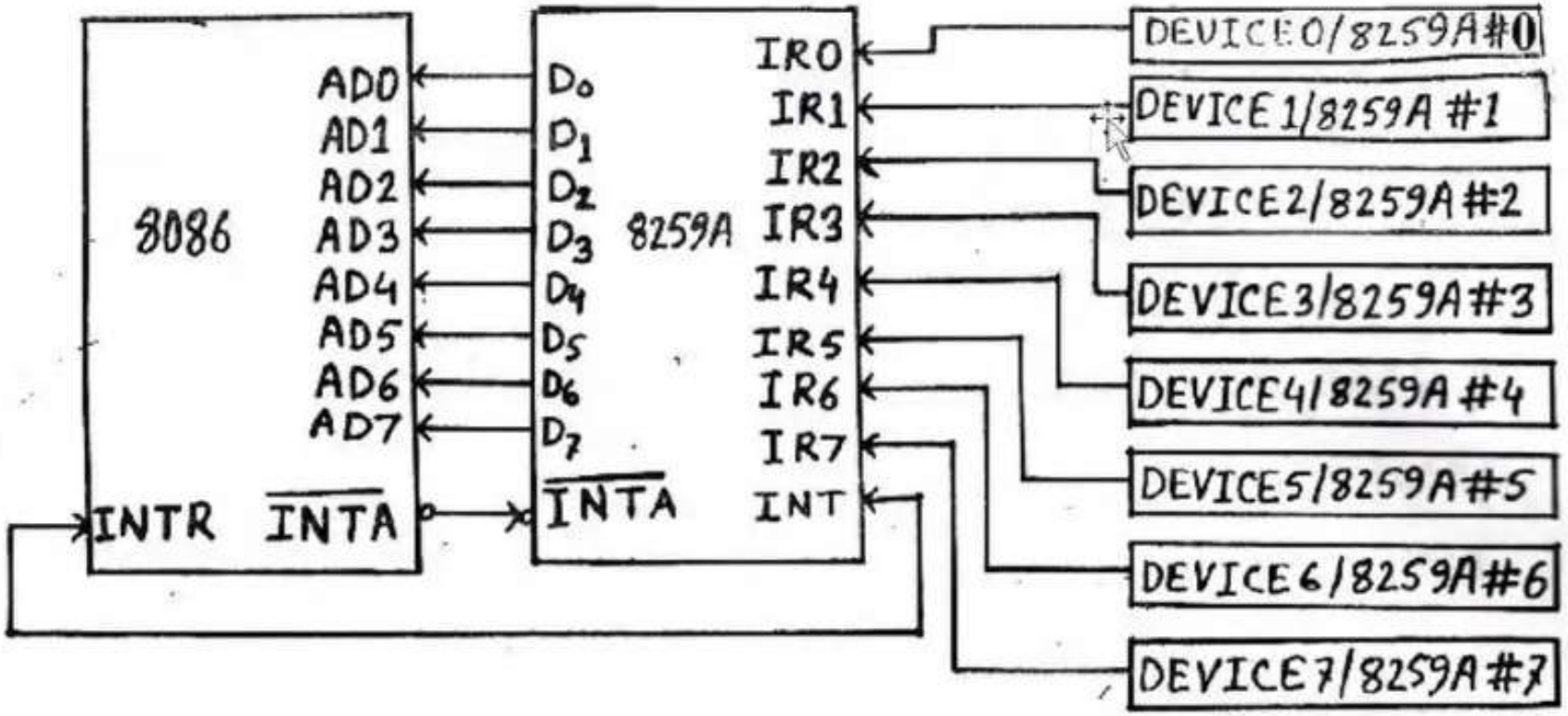

Fig. 2 Block Diagram showing an 8259 connected to an 8086

The 8259A PIC adds eight vectored priority encoded interrupts to the microprocessor. This controller can be expanded without additional hardware, to accept up to 64 interrupt requests. This require a master 8259A and eight 8259A slaves.

Internal Block Diagram of 8259A

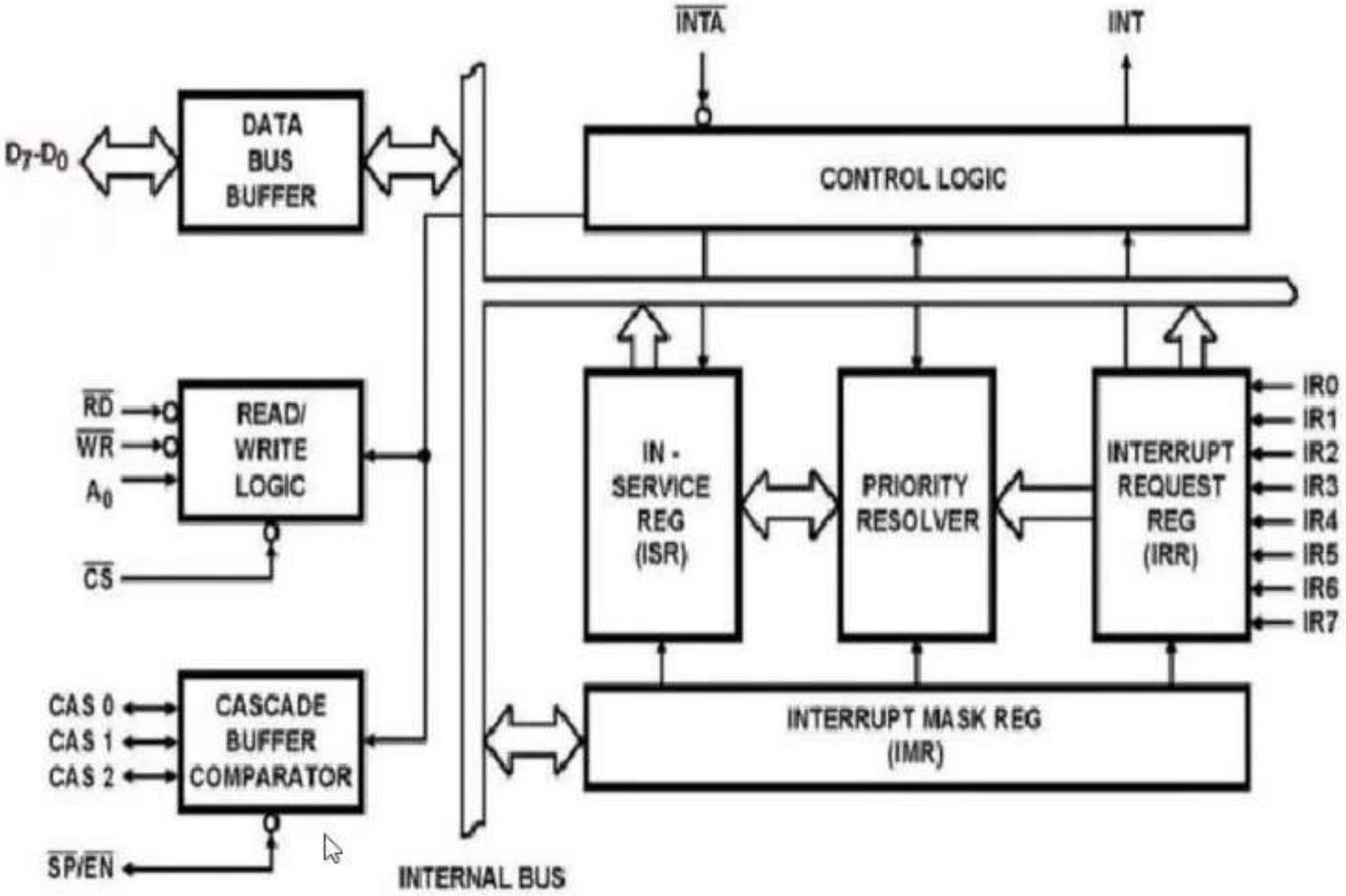

Fig. 3 Internal Block Diagram

Fig. 4 Pin Diagram

Internal Block Diagram of 8259A (Cont.)

8-bit data bus:

The 8-bit data bus ($D_7 - D_0$) allows the 8086-

* to send control words to the 8259A and read a status word from the 8259A.

* to send interrupt types to the 8086.

The eight data lines are always connected to the lower half of the 8086 data bus because the 8086 expects to receive interrupt types on lower 8-bit data lines.

$\overline{RD}, \overline{WR}$ and $\overline{CS}$:

The $\overline{RD}$ and $\overline{WR}$ inputs control data transfer when the device is selected by asserting its chip select ($\overline{CS}$) input low. Usually $\overline{RD}$ and $\overline{WR}$ pins are connected to the system $\overline{RD}$ and $\overline{WR}$ lines. $\overline{CS}$ may be connected to address decoder's output.

Address pin A_0:

A_0 input of 8259A is used to select one of the two internal addresses in the device. This pin may be connected to any of the system address lines.

Internal Block Diagram of 8259A (Cont.)

Cascade lines (CAS2-CAS0):

The cascade lines (CAS2-CAS0) are used as outputs from the master to the slaves for cascading multiple 8159As in a system. The master outputs a 3-bit slave identification number on these lines. Each slave in a system is assigned a 3-bit ID as part of its initialization. Sending this 3-bit ID number enables the slave.

Slave program/Enable buffer ($\mathbf{SP/\overline{EN}}$):

This pin is a dual function pin, when the 8259A is in buffered mode, this is an output that controls the data bus transceivers in a large microprocessor based system. When the 8259A is not in the buffered mode, this pin programs the device as a master (1) or a slave(0). When we use only one 8159A in our system, the $\mathbf{SP/\overline{EN}}$ pin is tied high (1).

INT Pin:

The interrupt output (INT) pin of 8259A is connected to the INTR pin on the microprocessor (8086) when there is only one 8259A in the system. In a system with master and slaves, only master's INT pin is connected to 8086. The slave's INT pins are connected to different IR pins of the master.

Internal Block Diagram of 8259A (Cont.)

Interrupt acknowledge ($\overline{INTA}$) pin:

This input pin of 8259A is connected to the $\overline{INTA}$ output of the 8086.

Interrupt request inputs(IR7 – IR0) :

The eight interrupt request inputs (IR7-IR0) are used to request an interrupt by the external devices in case of single 8159A system. In case of multiple 8259A system these input pins (IR7-IR0) of the master is connected to output INT pins of the slaves. Unused IR inputs should be tied to ground so that a noise pulse can not accidentally cause an interrupt. An interrupt signal must remain high on an IR input until after the falling edge of the first $\overline{INTA}$ pulse.

The interrupt Mask Register (IMR):

This register is used to disable (mask) or enable (unmask) individual interrupt inputs. Each bit in this register corresponds to the interrupt input with the same number. We can unmask an interrupt input by sending a command word with a 0 in the bit position that corresponds to that input.

Internal Block Diagram of 8259A (Cont.)

The Interrupt Request Register (IRR):

The IRR keeps track of which interrupt inputs are asking for service. If an interrupt input has an interrupt signal on it, then the corresponding bit in the IRR will be set.

The In Service Register (ISR):

The ISR keeps track of which interrupt inputs are currently being serviced. For each input that is currently being serviced, the corresponding bit will be set in the ISR.

The Priority Resolver:

The Priority Resolver acts as a "judge" that determines if and when an interrupt request on one of the IR inputs gets serviced.

8259A Interrupt Operation

To implement interrupt, **the interrupt enable flip-flop in the microprocessor should be enabled by writing the EI instruction** and the **8259A should be initialized by writing control words** in the control register. The 8259A requires two types of control words:

(a) Initialization Command Words (ICWS)

(b) Operational Command Words (OCWs)

ICWs are used to set up the proper conditions and specify RST vector address.

The OCWs are used to perform functions such as masking interrupts, setting up status-read operations etc.

Step-1: The IRR of 8259A stores the request.

Step-2: The priority resolver checks 3 registers-

* The IRR for interrupt requests. * IMR for masking bits and *the ISR for interrupt request being served.

It resolves the priority and sets the INT high when appropriate.