

LABORATORY JOURNAL

Submitted in fulfillment of the requirement

For the Subject

“DIGITAL ELECTRONICS AND LOGIC DESIGN”

(EC 207)

Prepared & Submitted By

Mr. BHAGYA VINOD RANA

(Admission No. U19CS012)

B. TECH. II (CSE) 3rd Semester

(Academic Year: 2020-21 [Aug-Dec 2020])

ONLINE MODE

Laboratory Teachers

Manoj Sir

Dr. Shilpi Gupta Mam

Sudhanshu Sir

Certificate

This is to Certify That

**Mr. BHAGYA VINOD RANA of B.Tech IInd
Computer Admission No. U19CS012 has
Satisfactorily Completed His course work in
**Digital Electronics and Logic Design
Laboratory** during the 3rd Semester Session
of Academic Year 2020-2021 and Submitted
on 03-December' 2020.**

Dr. Shilpi Gupta
Subject Co-ordinator

Director



Sardar Vallabhbhai National Institute of Technology, Surat

INDEX

Expt. No.	Experiment Name	Page No.
1	Introduction to Multisim	13/08/2020 [4]
2	Study of Basic and Universal Gates	20/08/2020 [23]
3	Half Adder and Half Subtractor	27/08/2020 [56]
4	Full Adder and Full Subtractor	03/09/2020 [69]
5	V-I Characteristics of PN – Junction Diode	10/09/2020 [83]
6	Diode Clipper Circuits (Series – Configuration)	17/09/2020 [91]
7	Diode Clipper Circuits (Shunt – Configuration)	24/09/2020 [115]
8	Diode Clamper Circuits	22/10/2020 [139]
9	Full Wave Rectifier	22/10/2020 [152]
10	Common Emitter Characteristics & Common Emitter Amplifier	29/10/2020 [158]
11	Registers and Counters	07/11/2020 [178]
12	Multiplexers and Code Converters	11/11/2020 [220]
13	High Pass and Low Pass Filters	26/11/2020 [255]