

Certificate

This is to Certify That

*Mr./Ms. BHAGYA VINOD RANA of B.Tech
IInd Computer Admission No. U19C0012 has
Satisfactorily Completed His course work in
Digital Electronics and Logic Design
Laboratory during the 3rd Semester Session of
Academic Year 2020-2021 and Submitted on
03-December' 2020.*

Dr. Shilpi Gupta
Subject Co-ordinator

Director



Sardar Vallabhbhai National Institute of Technology, Surat

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Expt. No.	Experiment Name	Date
1	Introduction to Multisim	13/08/2020
2	Study of Basic and Universal Gates	20/08/2020
3	Half Adder and Half Subtractor	27/08/2020
4	Full Adder and Full Subtractor	03/09/2020
5	V-I Characteristics of PN – Junction Diode	10/09/2020
6	Diode Clipper Circuits (Series – Configuration)	17/09/2020
7	Diode Clipper Circuits (Shunt – Configuration)	24/09/2020
8	Diode Clamper Circuits	22/10/2020
9	Full Wave Rectifier	22/10/2020
10	Common Emitter Characteristics & Common Emitter Amplifier	29/10/2020
11	Registers and Counters	07/11/2020
12	Multiplexers and Code Converters	11/11/2020
13	High Pass and Low Pass Filters	26/11/2020