ECE-6913 : CSA

Phase 2 Report

NetID : bvs9764

Name: Bhairavi Sawantdesai

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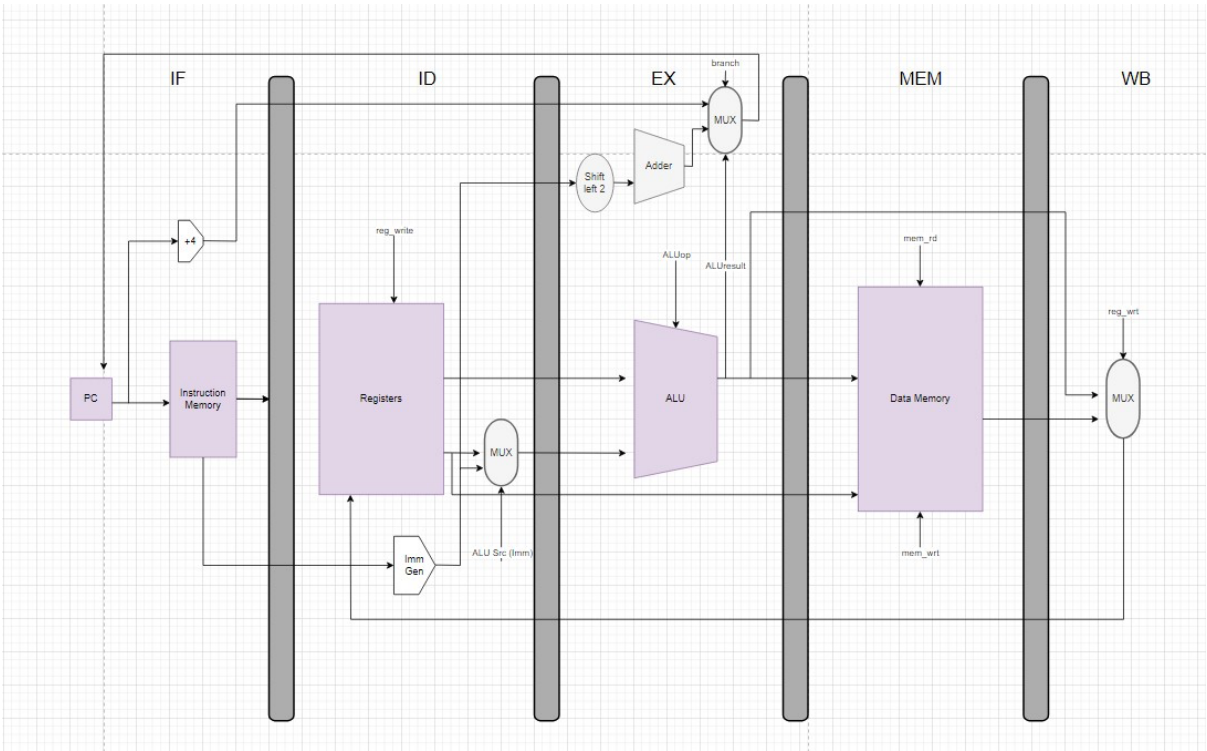
1) Schematic Diagram for five stage processor



2) Performance metrics:

Testcase 0:

Single Stage Core Performance Metrics

Total execu<on cycles = 6

Average CPI = 1.2

Instruc<ons per cycle = 0.833333

```
Single Stage Core Performance Metrics-----------------------------
Number of cycles taken: 6
Cycles per instruction: 1.2
Instructions per cycle: 0.833333
```

Five Stage Core Performance Metrics

Number of cycles taken: 10

Cycles per instruc<on: 2.0

Instruc<ons per cycle: 0.5

```
Five Stage Core Performance Metrics-----------------------------
Number of cycles taken: 10
Cycles per instruction: 2.0
Instructions per cycle: 0.5
```

Testcase 1:

Single Stage Core Performance Metrics

Total execu<on cycles = 40

Average CPI = 1.02564

Instruc<ons per cycle = 0.975001

output_ds7675 > testcase1 > PerformanceMetrics_Result.txt

```
1   Single Stage Core Performance Metrics-----------------------
2   Number of cycles taken: 40
3   Cycles per instruction: 1.02564
4   Instructions per cycle: 0.975001
5
```

Five Stage Core Performance Metrics

Number of cycles taken= 46

Cycles per instruc<on= 1.17949

Instruc<ons per cycle= 0.847824

```
Five Stage Core Performance Metrics-----------------------------
Number of cycles taken: 46
Cycles per instruction: 1.17949
Instructions per cycle: 0.847824
```

Testcase 2:

Single Stage Core Performance Metrics

Total execu<on cycles = 7

Average CPI = 1.75

Instruc<ons per cycle = 0.571429

```
Single Stage Core Performance Metrics----------
Number of cycles taken: 7
Cycles per instruction: 1.75
Instructions per cycle: 0.571429
```

Five Stage Core Performance Metrics

Number of cycles taken= 10

Cycles per instruc<on= 2.5

Instruc<ons per cycle= 0.4

```
Five Stage Core Performance Metrics----------
Number of cycles taken: 10
Cycles per instruction: 2.5
Instructions per cycle: 0.4
```

Testcase 3:

Single Stage Core Performance Metrics

Total execu<on cycles = 28

Average CPI = 2.54

Instruc<ons per cycle = 0.392858

```
Single Stage Core Performance Metrics----------
Number of cycles taken: 28
Cycles per instruction: 2.54545
Instructions per cycle: 0.392858
```

Five-Stage Core Performance Metric

Number of cycles taken=38

Cycles per instruc<on= 3.45455

Instruc<ons per cycle = 0.289473

```
Five Stage Core Performance Metrics-----------------------------
Number of cycles taken: 38
Cycles per instruction: 3.45455
Instructions per cycle: 0.289473
```

3. To enhance the performance of the single-stage processor further, we can employ the following methods:

a. Multiple Issue: To increase instruction-level parallelism, this approach involves replicating the internal components of the computer, allowing the launch of multiple instructions in each pipeline stage.

b. Speculation: In this method, the compiler or processor predicts the outcome of an instruction to eliminate it as a dependency in the execution of other instructions.

c. Superscalar: This advanced pipelining technique enables the processor to execute more than one instruction per clock cycle by selecting them during execution.

d. Caches and Memory Hierarchy: Utilizing cache memories with appropriate organization and size can significantly reduce memory access latency. Techniques like cache prefetching, cache associativity, and multi-level caching can further enhance performance by reducing memory stalls and improving data locality.

e. Instruction and Data Prefetching: Prefetching techniques fetch instructions or data from memory ahead of their actual use, reducing the latency caused by memory access. Prefetching can take advantage of spatial and temporal locality to improve performance.

f. SIMD and Vector Processing: Single Instruction, Multiple Data (SIMD) and vector processing architectures enable parallel processing of data elements using a single instruction. These architectures are particularly effective for tasks that involve a large amount of data parallelism, such as multimedia and scientific computing.

4. The performance of a five-stage processor surpasses that of a single-stage processor due to the utilization of pipelining. The five-stage processor achieves higher throughput by executing instructions in parallel. Although the time taken to execute a single instruction remains unchanged, the overall performance of the processor improves.