

Date
5/8/19

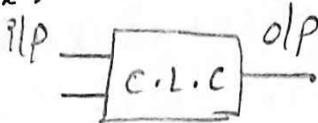
Unit - V

Synchronous Sequential Logic

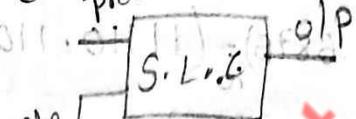
Logic Circuit (ckt)

Combinational logical ckt Sequential logic ckt

Ex:



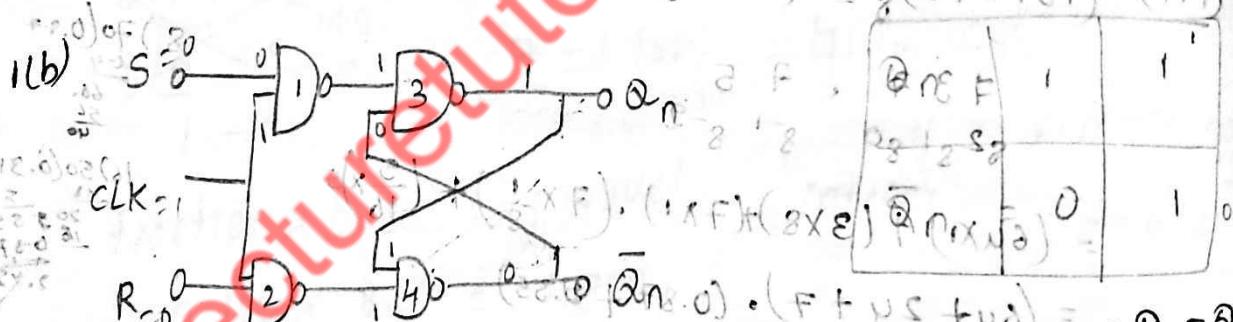
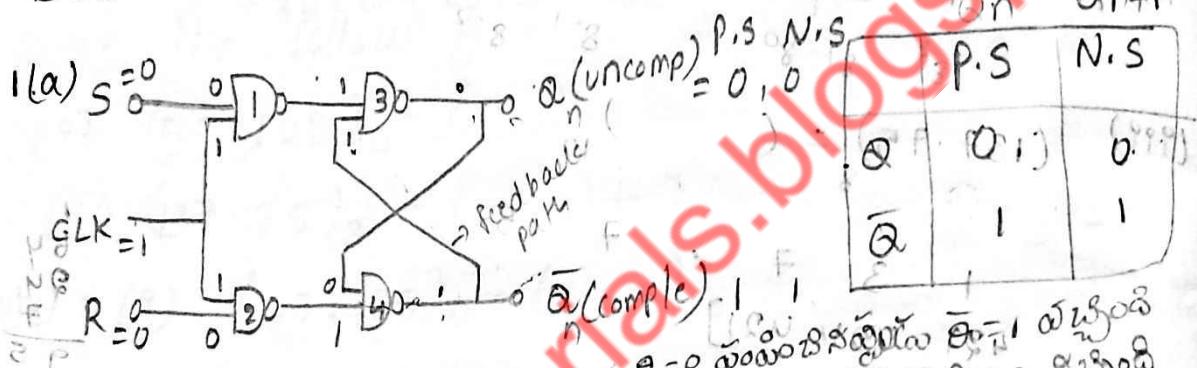
Ex: previous



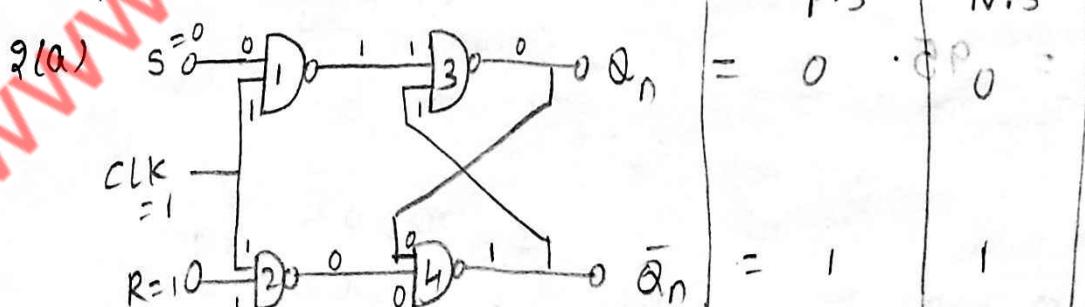
present

(NAND)

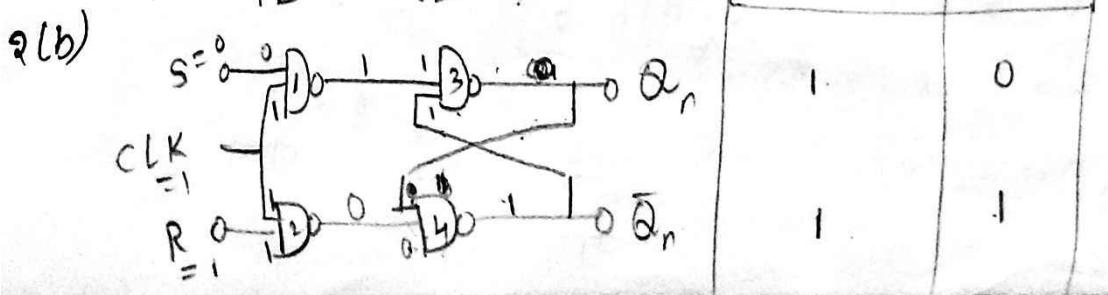
Basic Construction of S-R Flip Flop

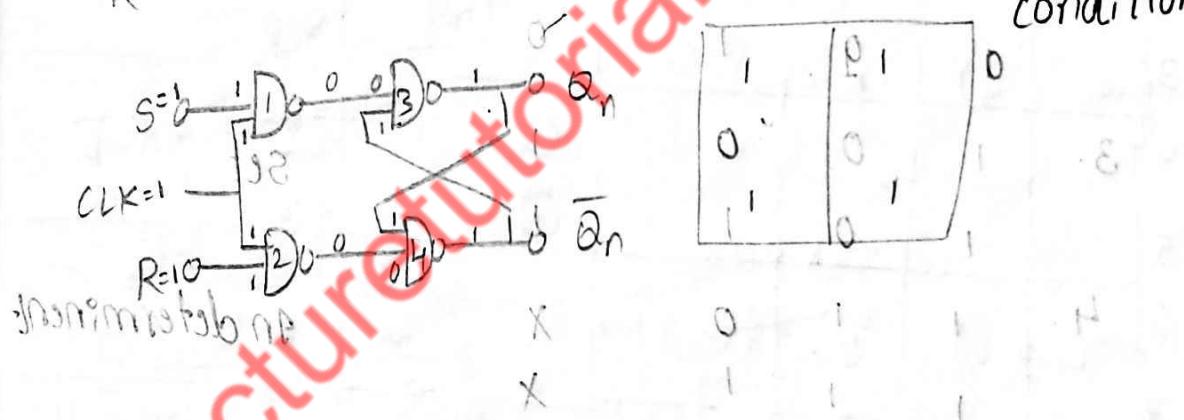
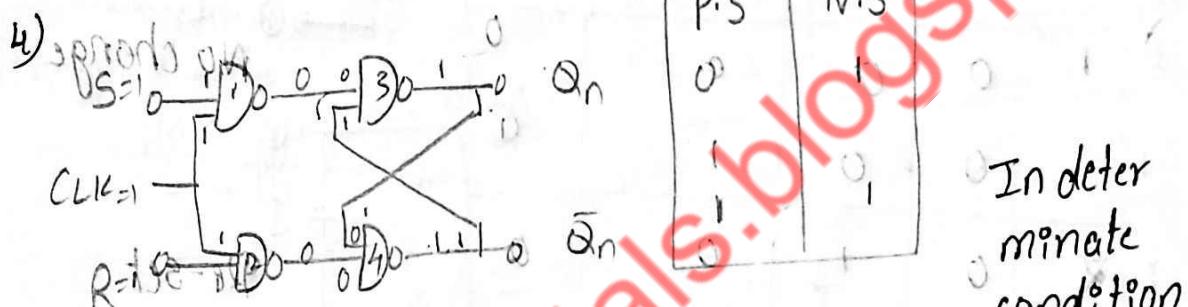
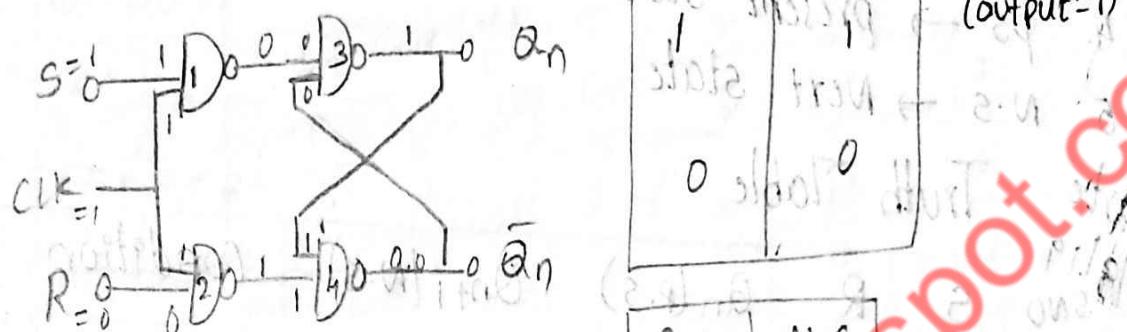
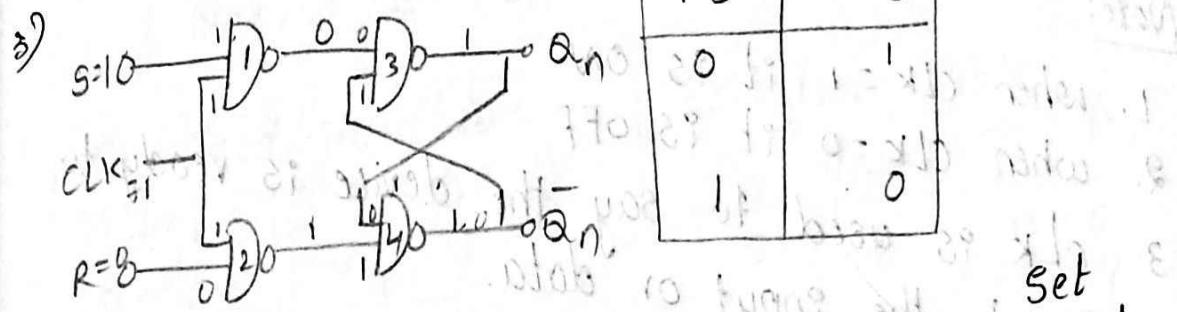


1(a) & 1(b) are no change condition $P.S = N.S \Rightarrow Q_n = Q_{n+1}$



Reset condition (output=0)





Flip flop:

- flip flop is a single bit storage device
- flip flop (SR, J-K, T, D) are four types of flip flop [Set, Reset]

* S-R flip flop [Set, Reset]

NAND			
A	B	AB	$\bar{A} \cdot \bar{B}$
0	0	0	1

NAND			
A	B	AB	$\bar{A} \cdot \bar{B}$
0	0	0	1

NAND			
A	B	AB	$\bar{A} \cdot \bar{B}$
0	1	0	1

NAND			
A	B	AB	$\bar{A} \cdot \bar{B}$
1	0	0	1

NAND			
A	B	AB	$\bar{A} \cdot \bar{B}$
1	1	1	0

Note:

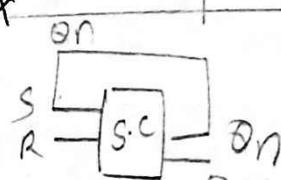
1. when $CLK = 1$ it is ON
2. when $CLK = 0$ it is OFF
3. CLK is used to say the device is ready to accept the input or data.
4. $PS \rightarrow$ present state
5. $N.S \rightarrow$ Next state

Date Truth Table

8/8/19

SNO	S	R	Q_n (P.S)	Q_{n+1} (N.S)	Condition
0	1	0	0	0	→ ① No change
1	0	0	1	1	→ ②
2	0	1	0	0	→ ① Re-set
3	0	1	1	0	→ ③
4	1	0	0	1	→ ② Set
5	1	0	1	1	→ ④
6	1	1	0	X	In determinent
7	1	1	1	X	

Characteristic Eq^n

SR Qn goes \rightarrow Qn+1

Guard (6, 4, 7, 5)

$$(S\bar{R} + \bar{S}R) \cdot (\bar{Q}_n + Q_n)S.R$$

Row. col

$$\begin{array}{|c|c|c|c|c|} \hline & & & & \text{Qn+1} \\ \hline & & & & \text{Qn} \\ \hline \text{Qn} & 0 & 1 & 0 & 1 \\ \hline \bar{S}R & 0 & 0 & 1 & 1 \\ \hline S.R & 1 & 1 & 0 & 0 \\ \hline \end{array}$$

$$S(R + \bar{R}) \text{ gof } \bar{S}R \text{ gof }$$

$$(S\bar{R} + \bar{S}R) \text{ gof } \bar{S}R \text{ gof }$$

$$\bar{R}(S + \bar{S}) \text{ gof } \bar{R} \text{ gof }$$

pair (1, 5)

$$(\bar{S}R + S\bar{R}) \text{ gof } \bar{S}R \text{ gof }$$

$$\bar{R}(S + \bar{S}) \text{ gof } \bar{R} \text{ gof }$$

X	6	X	7
1	4	1	5
X	2	3	X

$$Q_{n+1} = S + \bar{R} Q_n$$

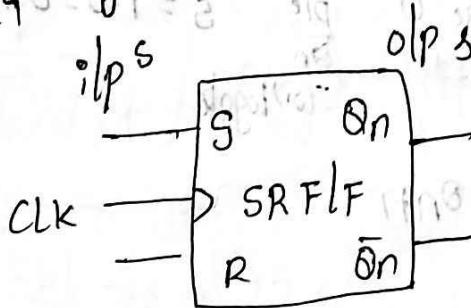
Minimized Truth Table

S	R	$Q_{n+1} =$
0	0	Q_n
0	1	0
1	0	1
1	1	X

Excitation Table

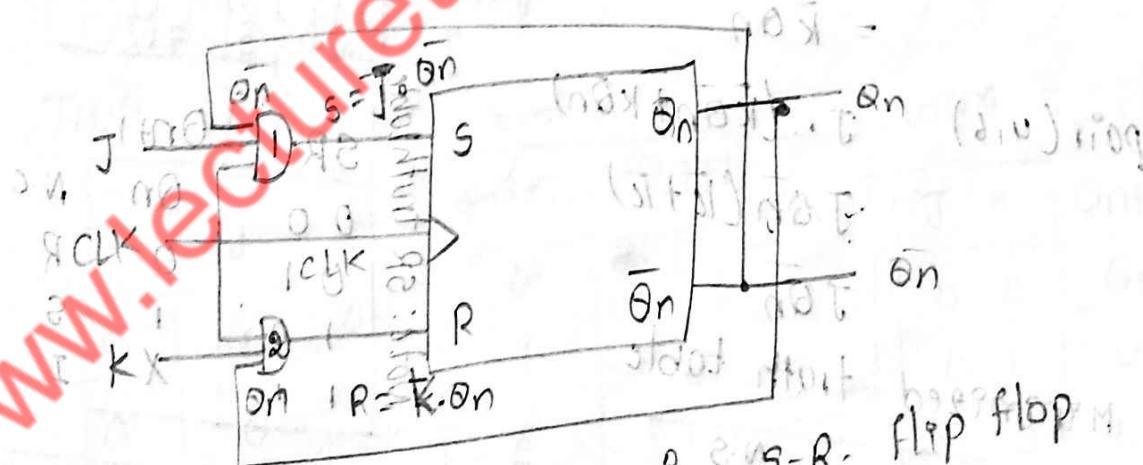
Q_n	Q_{n+1}	S	R
0	0	0	0
0	0	0	1
			X
0	1	1	0
1	0	0	1
1	1	0	0
		1	0
		X	0

Date 18/11/19 Symbol



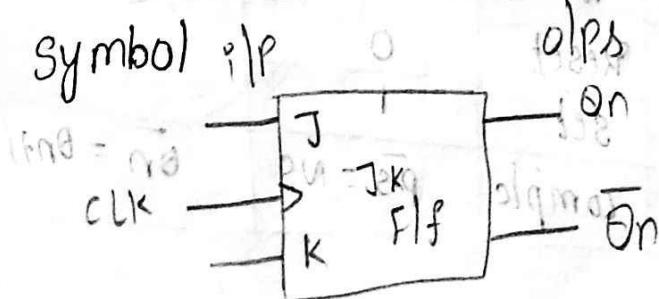
J-K- flip flop

AND Gate



circuit diagram for S-R flip flop

Symbol



Truth Table

J	K	S	R	P.S $Q_n = \bar{Q}_n$	N.S Q_{n+1}	C	$S = J\bar{Q}_n + RQ_n$	$R = K\bar{Q}_n$
0	0	0	0	0	1	0	$S = 0 \cdot 1 = 0$ R = 0 · 0 = 0	$R = 0 \cdot 0 = 0$
1	0	0	0	1	0	<u>1</u> N.C Reset	$S = 0 \cdot 0 = 0$ R = 0 · 1 = 0	$R = 0 \cdot 1 = 0$
0	1	0	0	0	1	<u>0</u> N.C Set	$S = 0 \cdot 1 = 0$ R = 1 · 0 = 0	$R = 1 \cdot 0 = 0$
3	0	1	0	1	0	<u>1</u> OR.S Set	$S = 0 \cdot 0 = 0$ R = 1 · 1 = 1	$R = 1 \cdot 1 = 1$
4	1	0	1	0	0	<u>1</u> N.C Reset	$S = 1 \cdot 1 = 1$ R = 0 · 0 = 0	$R = 0 \cdot 0 = 0$
5	1	0	0	1	0	<u>1</u> N.C Set	$S = 1 \cdot 0 = 0$ R = 0 · 1 = 0	$R = 0 \cdot 1 = 0$
6	1	1	1	0	0	<u>1</u> Com ple on	$S = 1 \cdot 1 = 1$ R = 1 · 0 = 0	$R = 1 \cdot 0 = 0$
7	1	1	0	1	1	<u>0</u> R.C on	$S = 1 \cdot 0 = 0$ R = 1 · 1 = 1	$R = 1 \cdot 1 = 1$

characteristic equation

$$J_K Q_n \text{ if } p.s \rightarrow Q_{n+1}$$

pair(1, 5) rows, cols

$$(\bar{J} + J) \cdot \bar{K} Q_n$$

$$= \bar{K} Q_n$$

pair(4, 6) $J \cdot (\bar{K} \bar{Q}_n + K Q_n)$

$$J \bar{Q}_n (\bar{K} + K)$$

$$J \bar{Q}_n$$

Minimized truth table

J	K	$\bar{Q}_{n+1} =$
0	0	\bar{Q}_n
0	1	0
1	0	1
1	1	\bar{Q}_n

SR	\bar{Q}_{n+1}	
0 0	\bar{Q}_n	
0 1	0	R
1 0	1	S
1 1	X	I

J	K	\bar{Q}_{n+1}
0 0	0 1	1 0
0 1	1 1	1 1
1 0	1 1	0 1
1 1	0 0	0 0

SR		\bar{Q}_{n+1}	
0 0		\bar{Q}_n	
0 1		0	R
1 0		1	S
1 1		X	I

and function
border
conditions
present
state

Exciation Table

K	0	-	X	0	-	X	-	-	-	0	0	0
J	0	0	0	1	-	-	0	-	X	0	1	X
Qn	0			1			0			1		
Qnti	0			1			0			1		

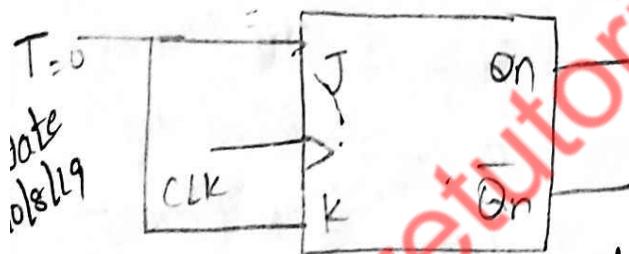
T Fl/f / Toggle flip flop

T flip flop

ilp olp

1 2
T Qn, \bar{Q}_n

outputs



It has single input and we get two outputs

Truth table

Assumption

using J-K Fl/f

T	J	K	Qn	Qnti
0	0	0	0	{ 0 } \rightarrow ① N.C
0	0	0	1	{ 1 } \rightarrow ② comp
1	1	1	1	{ 0 }
1	1	1	0	

J	K	Qn	Qnti
0	0	Qn NC	
0	1	Q R	
1	0	1 S	
1	1	\bar{Q}_n comp	

Minimized truth table

q/p N.S
T Q_{n+1}

q/p	N.S		
0	0	i/p	N.S
0	1	T	Q _{n+1}
1	0	0	Q _n N.C
1	T	1	Q _n comp

Excitation table

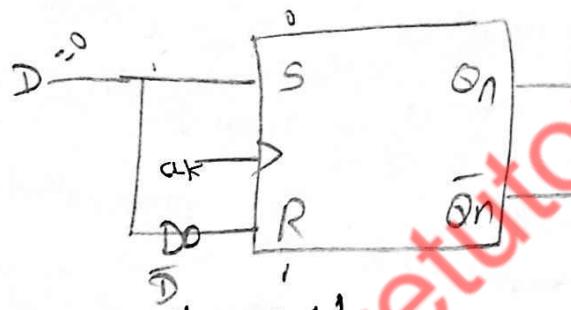
i/p	o/p
0	0
0	1
1	0
1	1

Characteristic equation

$$Q_{n+1} = \bar{T}Q_n + T\bar{Q}_n$$

Q	0	0	0	Q _{n+1}
T	0	0	1	
0	0	0	1	
1	1	1	0	

D flip flop (or) delay flip flop



Truth Table

This D flip flop can be constructed by using S-R flip flop

D i/p	S=D	R=̄D	(P.S) Q _n	(N.S) Q _{n+1}
0	0	1	0	0] Reset
0	0	1	1	0]
1	1	0	0	1] Set
1	1	0	1	1]

S.R. f/p Truth table

Minimized truth table

S	R	Qn+1	
		Qn	N.C
0	0	Qn	
0	1	0	R
1	0	1	S
1	1	X	inde

Excitation table

Qn	Qn+1	D
0	0	0
0	1	1
1	0	0
1	1	1

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13/8/19

Conversion of flip flops

(1) Convert S-R flip flop to D-flip flop (or)

1. convert S-R flip flop to D-flip flop using S-R flip flop.

construct D flip flop using S-R flip flop.

solu 1. which flip flop is going to construct

truth table of that flip flop

2. which flip flop is going to use for the construction

truth table of that flip flop

D	Qn	Qn+1 cond	SR	X
0	0	0	Reset	X0
0	1	0		01
1	0	1	Set	10
1	1	1		X0

Truth table of D flip flop

D	Qn	Qn+1
0	0	0
1	1	1

characteristic equation:

D	Qn	Qn+1
0	0	0
1	0	1
2	1	0
3	1	1

Qn	Qn+1	SR
0	0	0X0
0	1	10
1	0	01
1	1	X0

excitation table of SR flip flop

S-R flip flop \rightarrow D flip flop

S K-map

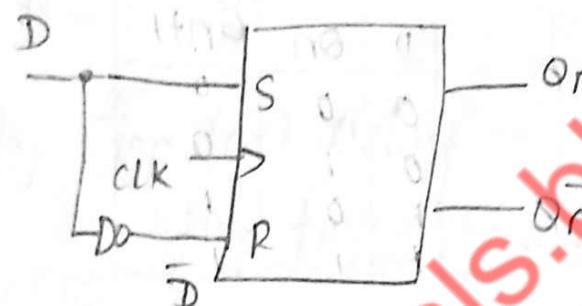
D	Qn	$\bar{Q}n$	Qn
Qn	0	1	
Qn	1	0	X
Qn	1	X	0

R - K-map

D	Qn	$\bar{Q}n$	Qn
D	0	1	
D	1	0	1
D	1	1	2

$$R = \bar{D} (\bar{Q}n + Qn)$$

$$= \bar{D}$$



2. Convert S-R flip flop to J-K flip flop
present (S R) flip flop \rightarrow JK flip flop (construct)
Excitation table Truth table
Truth table of J-K flip flop Excitation table of S-R flip flop

J	K	present Qn	next's Qn	condi- tion	S R
0	0	0	0	N.C	0 X
1	0	1	1		X 0
2	0	0	0		0 X
3	1	1	0	Reset	0 1
4	1	0	1	Set	1 0
5	1	0	1		X 0 X
6	1	1	0	Comp	1 0
7	1	1	0		0 1 X

Qn	On+1	S R
0	0	0 X
0	1	1 0
1	0	0 1
1	1	X 0

$$S = \sum_m (U, 6) + d(1, 5) \quad R = \sum_m (3, 7) + d(0, 2)$$

S K-map

		K-Qn			
		K̄Qn 00	KQn 01	K̄Qn 11	KQn 10
		J	J̄	J	J̄
	0		X		
	1	1	1	3	2
J	0	0	1	3	2
J̄	1	1	X	7	6

pair(U, 6)

$$= J \cdot (\bar{K}Qn + K\bar{Q}n)$$

$$= J\bar{Q}n(\bar{K} + K)$$

$$S = J\bar{Q}n$$

pair(3, 7)

$$= (\bar{J} + J) \bar{Q}n K$$

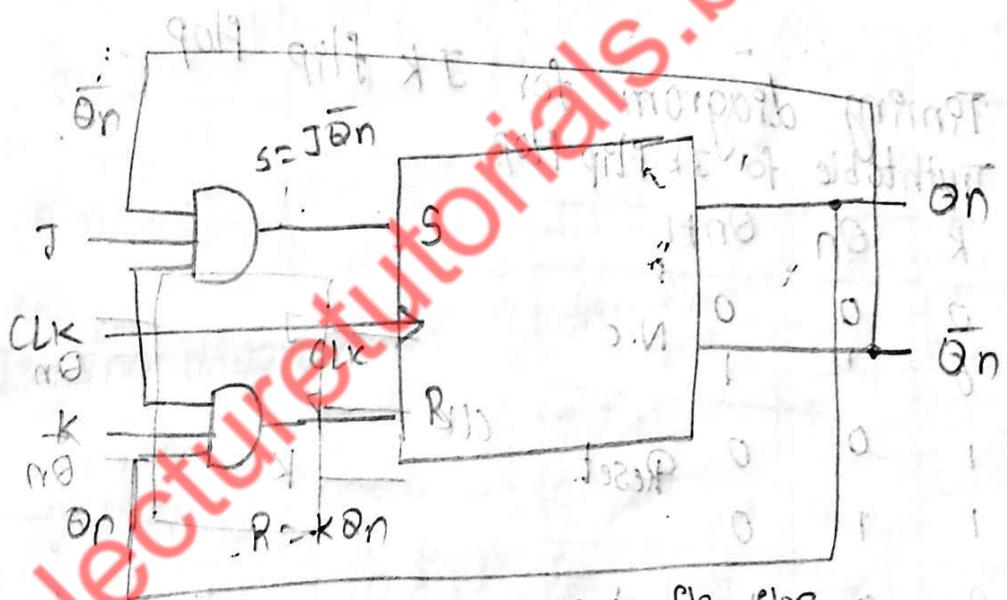
$$R = K\bar{Q}n$$

		K-Qn			
		K̄Qn 00	KQn 01	K̄Qn 11	KQn 10
		J	J̄	J	J̄
	0		X		
	1	1	1	3	2
J	0	0	1	3	2
J̄	1	1	X	7	6

pair(3, 7)

$$= (\bar{J} + J) \bar{Q}n K$$

$$R = K\bar{Q}n$$



Timing Diagrams

⇒ S-R flip flop (or) edge trigger flop flop

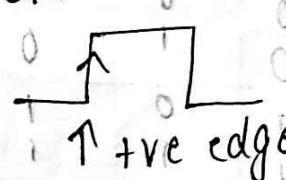
start

CLK $\xrightarrow{\text{konst}}$

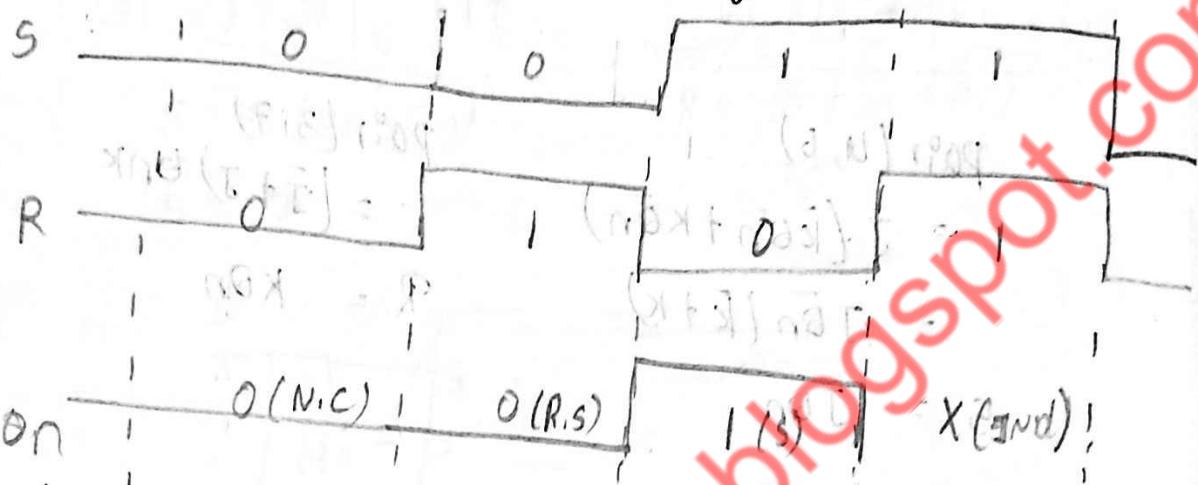
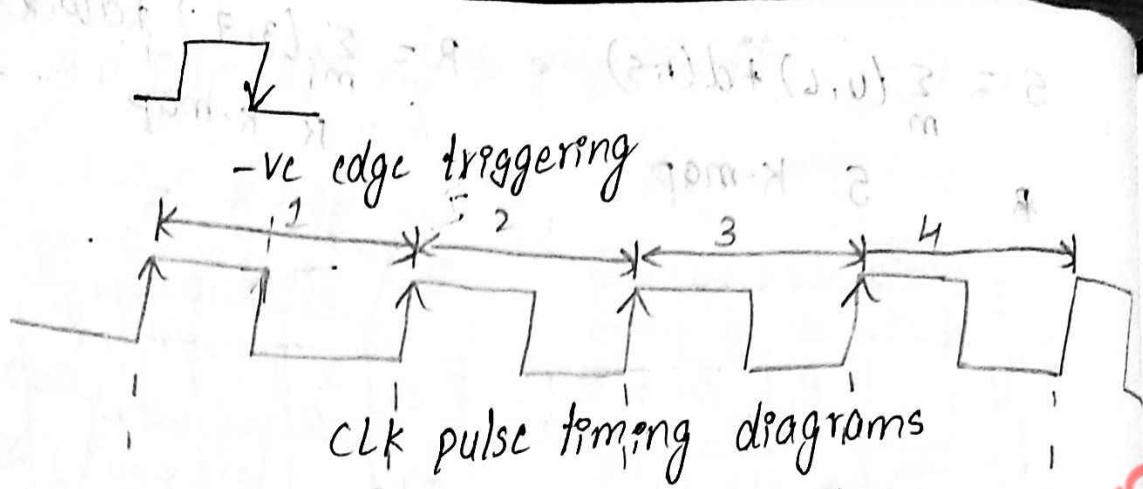
OFF → ON (triggering)

S	R	Qn(t)
0	0	Qn(t)
0	1	0
1	0	1
1	1	X

minimized truth table

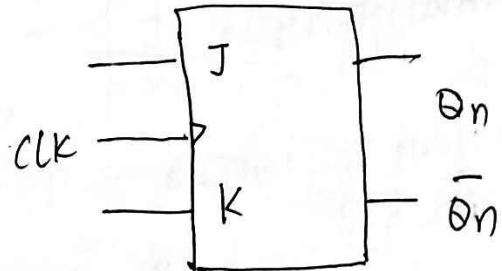


+ve edge triggering



Date : 14/8/19 Timing diagram for JK flip flop
 Truth table for JK flip flop

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

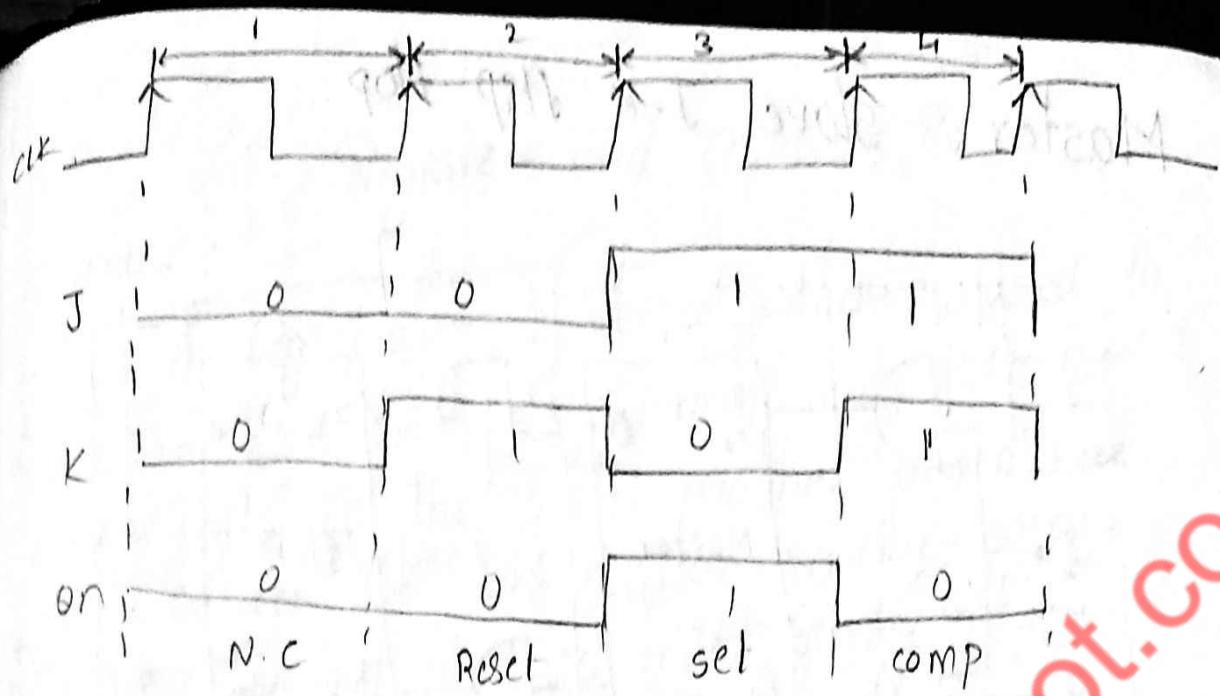


Minimized truth table for D-Flop Flop

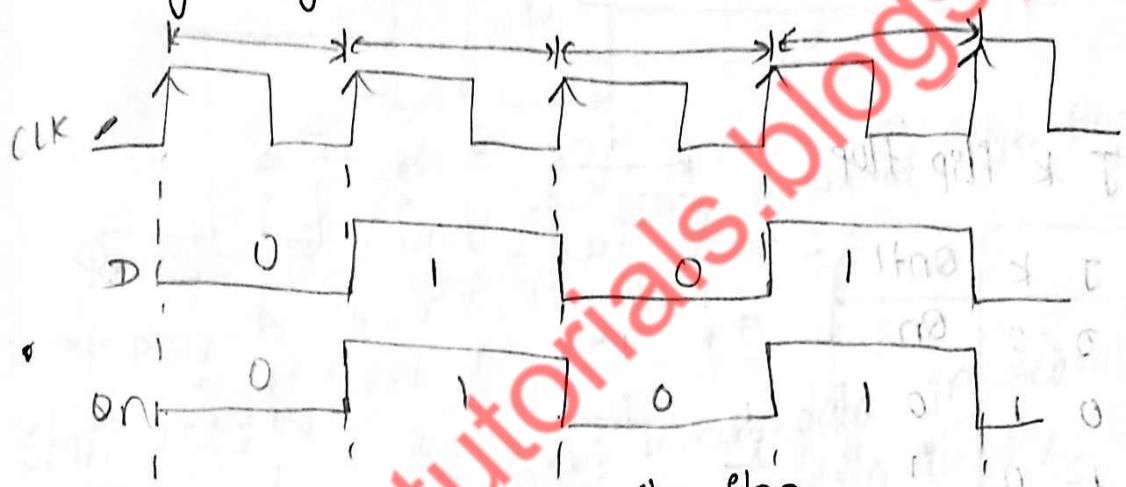
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Reset is $Q_{n+1} = 0$

Set



Timing diagram for D flip flop

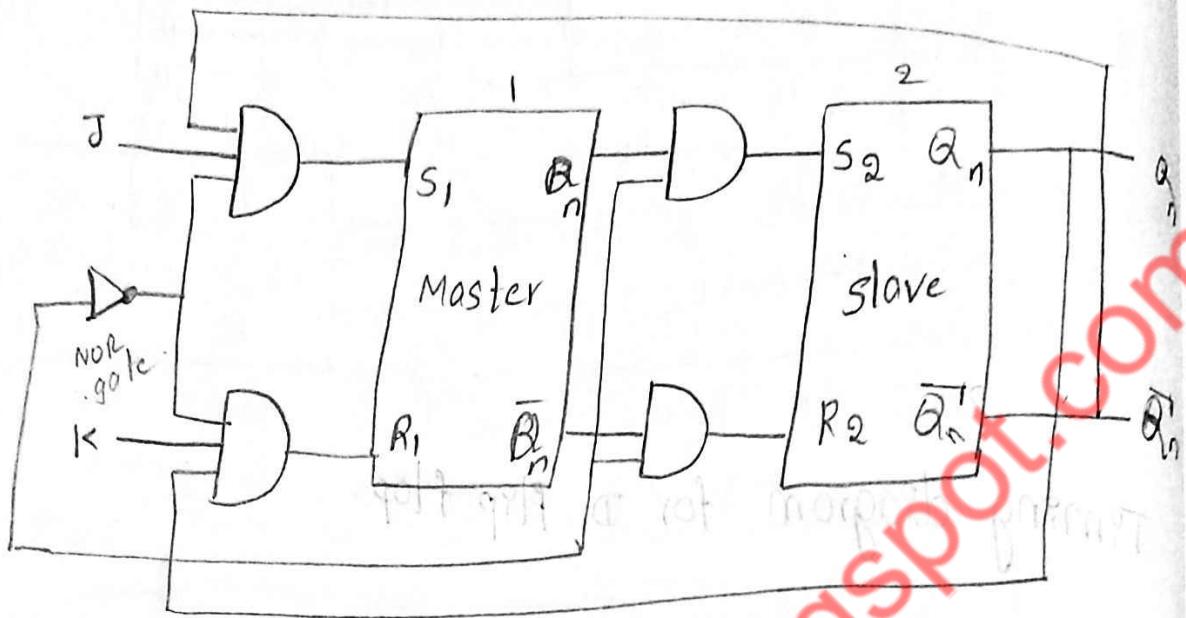


Timing diagram for T flip flop

T	Qn	Qnti	P-S	N-S
0	0	0	0	N.C
0	1	1	1	0
1	0	0	0	1 comp
1	1	1	1	0

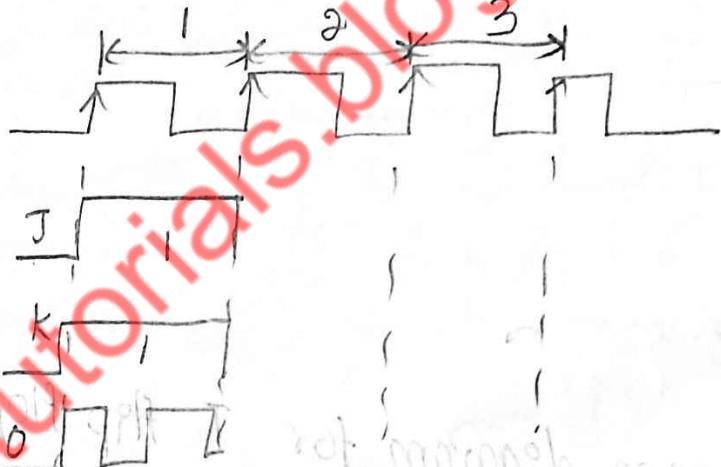
minimized truth table

Master's slave J-K flip flop



J K flip flop

J	K	Qn
0	0	Qn
0	1	0
1	0	1
1	1	\bar{Q}_n



Race around problem

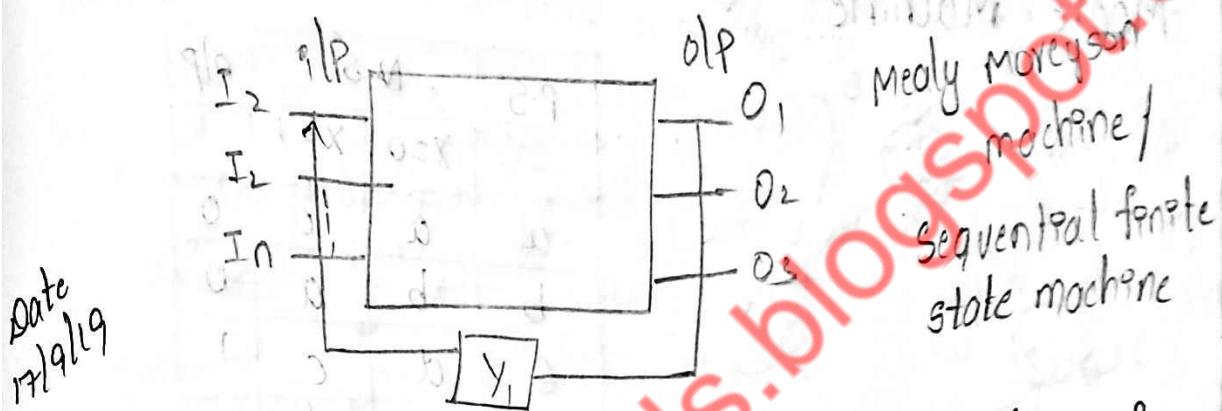
Here when the values of J K are both "1" we get the toggle or complement as output

while occurring this output an error race around problem occurred to avoid this "Master slave JK flip flop is used".

Unit - V

Finite State Machine

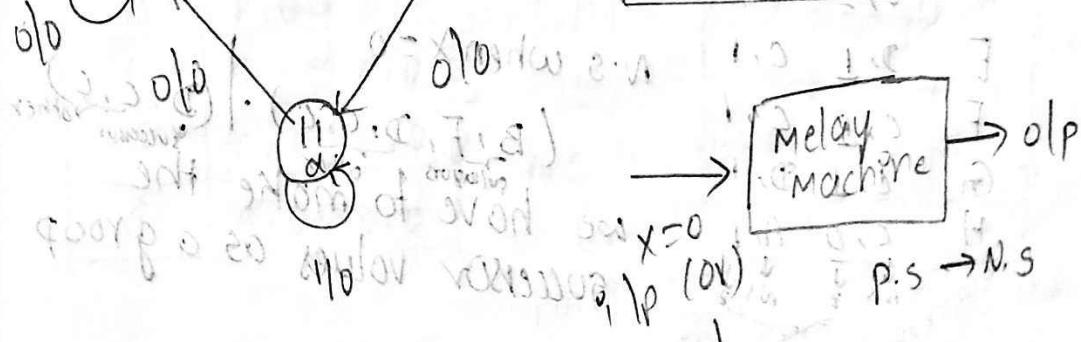
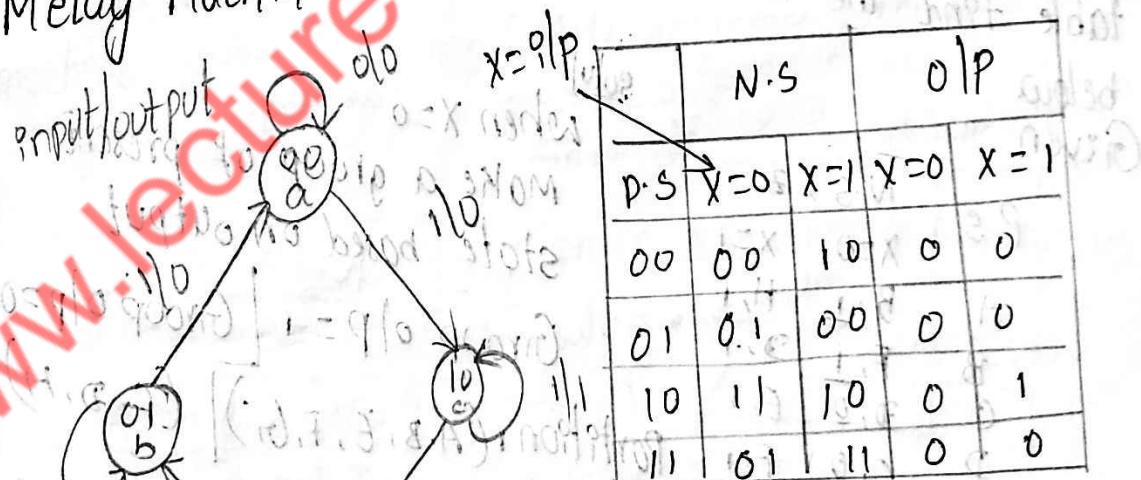
Finite state machine is a model which is used to describe the synchronous sequential machine. It is a machine with fixed no. of states i_1, i_2, \dots, i_n input variables; $o_1, o_2, o_3, \dots, o_n$ = output variables $y_1, y_2, y_3, \dots, y_n$ are state variables



State Diagrams

State diagram is the pictorial representation of states, present state \Rightarrow next state

Mealy Machine



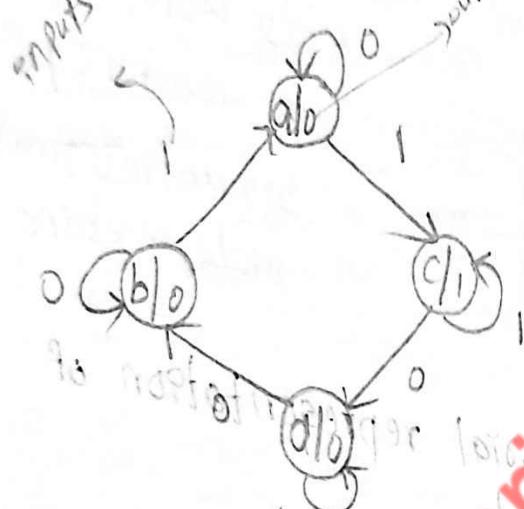
Excitation table

N.S		output		Q.O.P
P.S	X=0	X=1		
00	00	0	10	00P
01	01	0	00	0
10	11	0	10	1
11	01	0	11	0

Note

If they didn't mention any model it is melay
otherwise moore

Moore Machine



State table

P.S	N.S		Q.O.P
	X=0	X=1	
a	a	c	0
b	b	a	0
c	d	c	1
d	b	d	0

What are the conditions to minimize the state table found the minimized state table for the given below.

Given

P.S	N.S, Z	
	X=0	X=1
A	B, 1	H, 1
B	F, 1	D, 1
C	D, 0	E, 1
D	C, 0	F, 1
E	D, 1	C, 1
F	C, 1	C, 1
G	C, 1	D, 1
H	C, 0	A, 1

when X=0

make a group of present state based on output

Group Q.O.P = 1 Group Q.O.P = 0

Partition: (A, B, E, F, G) (C, D, H)

N.S when X=0

(B, F, D, C, C) . | (D, C, C)

we have to make the successor values as a group

partition 2

$$(A, B) (E, F, G) (c) \cdot (DH) \quad [\because B \text{ is successor of } A]$$

F is a successor of B

N.S when $X=1$

$$(HD) \underbrace{(CCD)}_{\text{successor}} (E) \underbrace{(FA)}_{\text{other successors}}$$

HD are successors of AB
 E is not successor of c

partition 3

$$(AB) (EFG) (x) (DH) (CD) (H)$$

minimized state table

P.S	N.S, Z	
	X=0	X=1
A	B, 1	H, 1
B	F, 1	D, 1
C	D, 0	E, 1
E	D, 1	C, 1
H	C, 0	A, 1

Date
19/9/2019

Derive a circuit that realizes the finite state machine defined by the state assignment table below using J-K flip flop.

when $X=0$

Group 0/p = 1

Group 0/p = 0

P.S	N.S, Z	
	X=0	X=1
A	B, 0	E, 0
B	E, 0	D, 0
C	D, 1	A, 0
D	C, 1	E, 0
E	B, 0	D, 0

partition 1 (C, D)

N.S when $X=0$

(D, C)

(A, B, E)

(B, E, B)

partition 2

(E) (D) (C)

N.S when $X=1$

(A, E)

(AB) E

(E, D, D)

partition 3

D, C

(AB) E

Minimized truth table

P.S	N.S, Z	
	X=0	X=1
A	B, 0	C, 0
C	D, 1	A, 0
D	C, 1	E, 0
E	B, 0	D, 0

Implement the finite state machine using J-K flip flops [the given state table is reduced state table for the above reduced table]

Q ₁ P ₀	X	P.S	N.S		Q ₁ P ₀	J _P	K _P	J _Q	K _Q
			Q ₁	P ₀					
0	0	A, 00	B, 01	0	0	0	X	1	X
1	0	B, 01	B, 01	0	0	X	X	0	
2	0	C, 10	D, 11	1	X	0	1	1	X
3	0	D, 11	C, 10	1	X	0	X	1	X
4	1	A, 00	B, 01	0	0	0	X	1	X
5	1	B, 01	D, 11	0	1	X	X	0	
6	1	C, 10	A, 00	0	X	1	0	X	
7	1	D, 11	B, 01	0	X	1	X	0	

Given minimized table

Q _n	Q _{n+1}	J K		P.S	N.S, Z	
		X	X		X=0	X=1
0	0	0	X	A	B, 0	B, 0
0	1	1	X	B	B, 0	D, 0
1	0	X	1	C	D, 1	A, 0
1	1	X	0	D	C, 1	B, 0

Excitation table of JK flip flop

		00	01	11	10
		X	X	1	
		0	(1) X	X	1
0	0				
	1	1	X	X	1

$$Jq = \bar{x} + \bar{p}$$

		00	01	11	10
		X	1	(1) X	
		0	0	1	2
0	0				
	1	X			

$$Kq = \bar{x} \cdot p$$

		00	01	11	10
				X	X
		0	1	3	2
0	0				
	1	(1) X	X		

$$Jp = xq$$

		00	01	11	10
		X	X		
		0	1	3	2
0	0				
	1	X	X	1	1

$$Kp = x$$

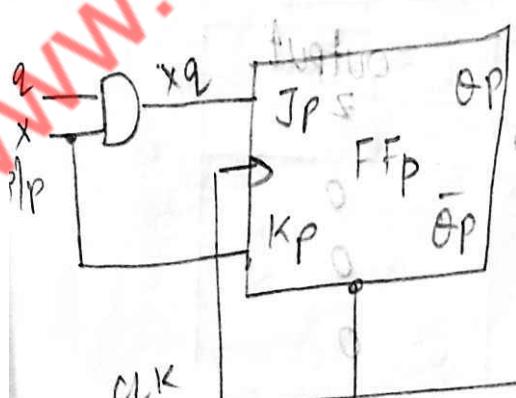
olp: z

Here x, p, q are inputs.

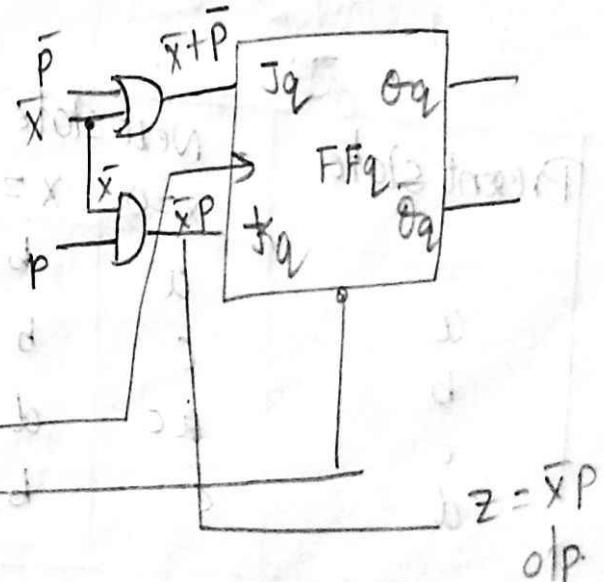
		00	01	11	10
				(1) 1	2
		0	1	3	2
0	0				
	1	4	5	3	6

$$z = \bar{x}p$$

logic circuit



clear
pulse



$$z = \bar{x}p$$

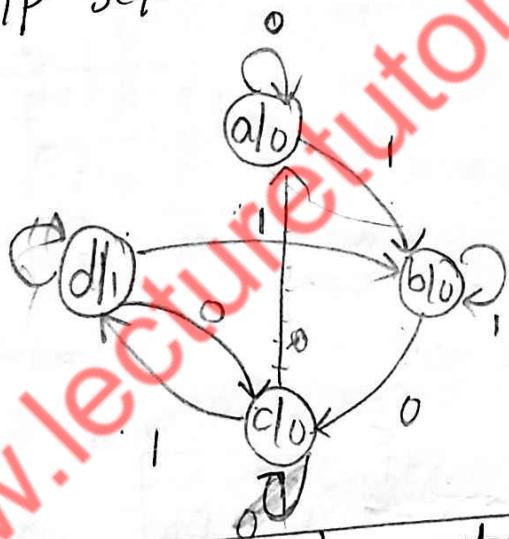
olp

- Assignment**
1. If the simple example explain the difference between melay and Moore type machine (unit-II)
 2. Draw the diagram of moore type FSM (finite state machine) for serial adder (unit-IV).
 3. draw the diagram of melay type state machine for serial adder and explain its operation (unit IV)
 4. what are the capabilities and limitations of finite state machine explain (unit II)

Date 2019 Sequence Detector

Design a moore type sequence detector to detect a serial input sequence of 101

o/p sequence 101
 $s_1 s_2 s_3$



excitation table of d

on	on + 1	D
0	0	0
0	1	1
1	0	0
1	1	1

Present state	Next state		output z
	$x=0$	$x=1$	
a	a	b	0
b	c	b	0
c	ac	d	0
d	c	b	1

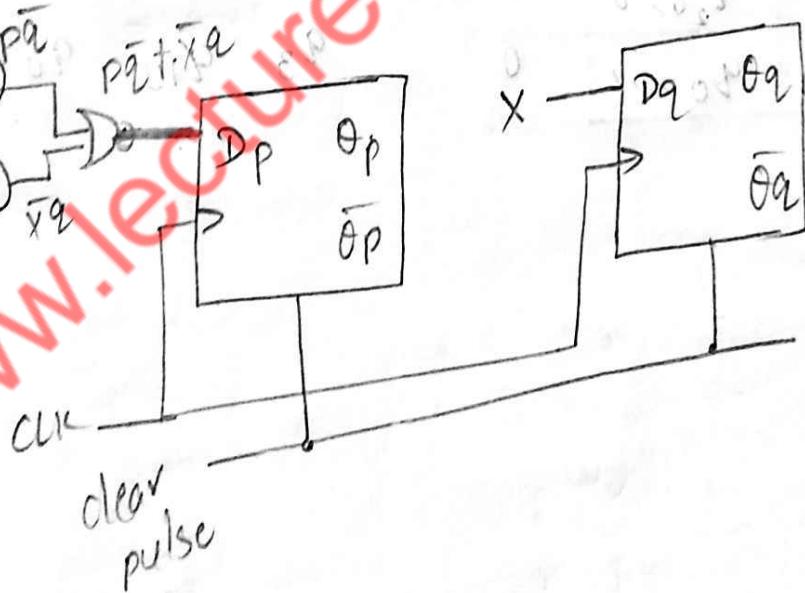
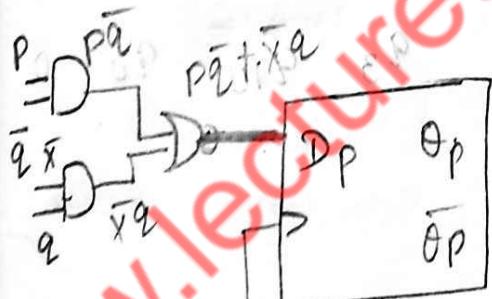
XQ/P	$P \cdot S$	$N \cdot S$	D_P	D_Q
	$P \cdot Q$	$P+1 \cdot Q+1$		
0	0	a	00	a
1	0	b	01	c
2	0	c	10	c
3	0	d	11	c
4	1	a	00	b
5	1	b	01	b
6	1	c	10	d
7	1	d	11	b

$X \cdot P \cdot Q$	00	01	11	10
0	1	1	1	2
1	0	1	3	2
	4	5	7	6

$X \cdot P \cdot Q$	00	01	11	10
0	0	1	3	2
1	1	2	7	13

$$D_P = P \cdot \bar{Q} + \bar{X} \cdot Q$$

$$D_Q = X$$



Date
21/9/19 Melay to Moore Machine

P.S	N.S , z	
	X=0	X=1
q ₀	q _{3,0}	q _{11,1}
q ₁	q _{0,1}	q _{3,10}
q ₂	q _{2,11}	q _{2,10}
q ₃	q _{1,10}	q _{0,1}

q _{0,1}	q _{1,1}	q _{11,1}
q _{0,1}	q _{1,0}	q _{10,0}
No change		
q _{3,0}	q _{2,11}	q _{21,}
q _{3,0}	q _{2,10}	q _{20,1}
No change		

State table

P.S	N.S , z		O/P
	X=0	X=1	
q ₀	q _{3,0}	q _{11,1}	1
q ₁₀	q _{0,1}	q _{3,0}	0
q ₁₁	q _{0,1}	q _{3,0}	1
q ₂₀	q _{21,1}	q _{20,0}	0
q ₂₁	q _{21,1}	q _{20,0}	1
q ₃	q _{10,0}	q _{0,1}	0

Moore Machine

P.S	X=0	X=1	O/P
q ₀	q ₃	q ₁₁	1
q ₁₀	q ₀	q ₃	0
q ₁₁	q ₀	q ₃	1
q ₂₀	q ₂₁	q ₂₀	0
q ₂₁	q ₂₁	q ₂₀	1
q ₃	q ₁₀	q ₀	0