Date
16/8/19

Unit - VI

Registers and Counters

Register

A register is a device which is used to store the data in binary format and shifts the binary bits in the serial manner and also we can collect the information in the same binary format. It is called bit by bit.

→ store the binary data

$\boxed{\text{Register}}$

temporary

Register is formed by using the no.of flip flops it may be D or T flip flop.

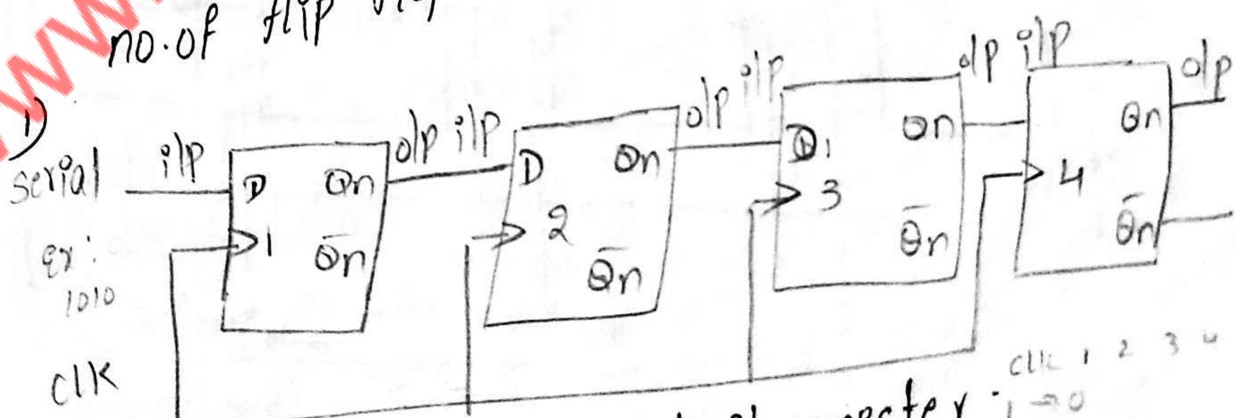
shift register

It shifts the given binary data in serial manner and we can collect the data in the same binary manner

4 bit register

no.of flip flops = 4 ; we may use "D" flip flop

1)

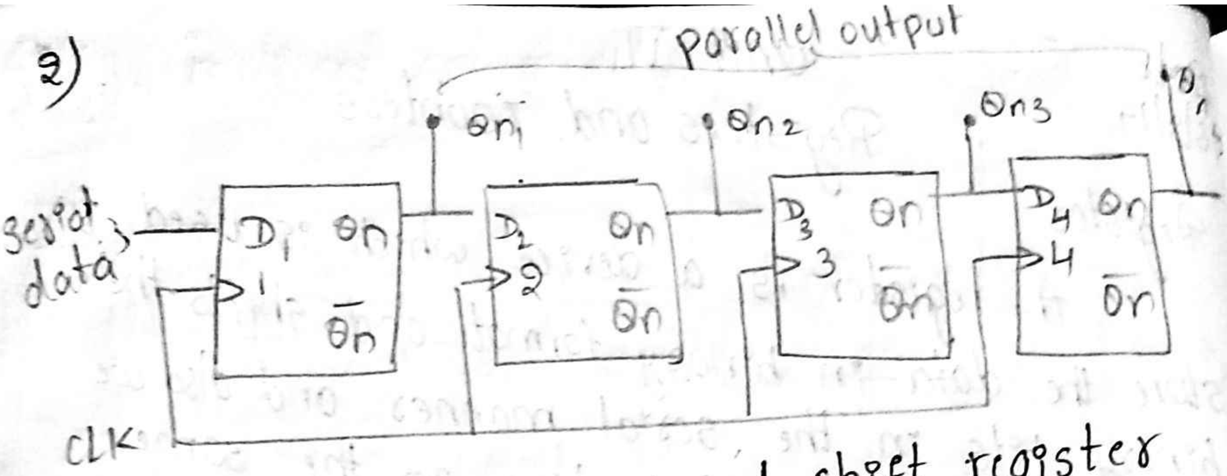


clk	1	2	3	4
1	→ 0			
2	1 →	0		
3	0	1 →	0	
	1	0	1 →	0

Serial in - serialout shift register :

∵ in means = entry of data

2)



Serial-in-parallel-out shift register

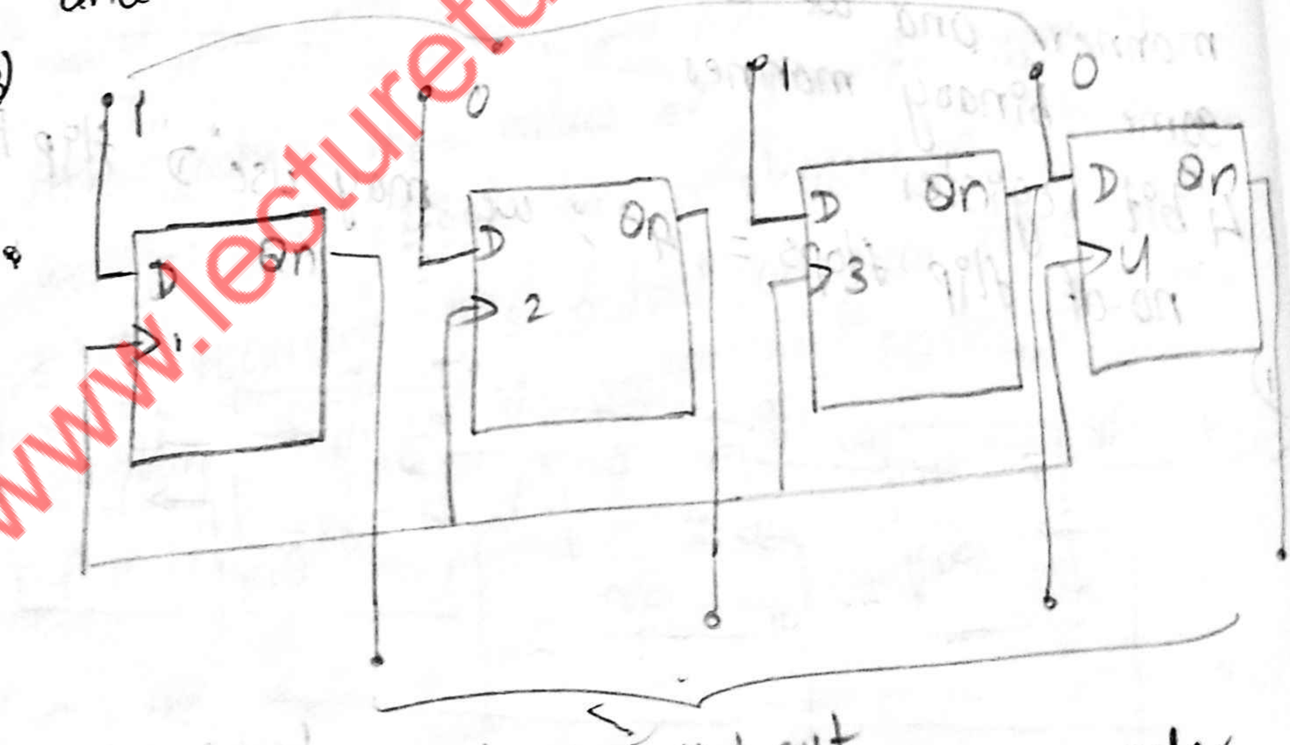
4 3 2 1
1 0 1 0

1010 →

	ops across f/f			
CLK	D_1	D_2	D_3	D_4
0	-	-	-	-
1	0	-	-	-
2	1	0	-	-
3	0	1	0	-
4	1	0	1	0

In this register the data entered in serial and collected in parallel out

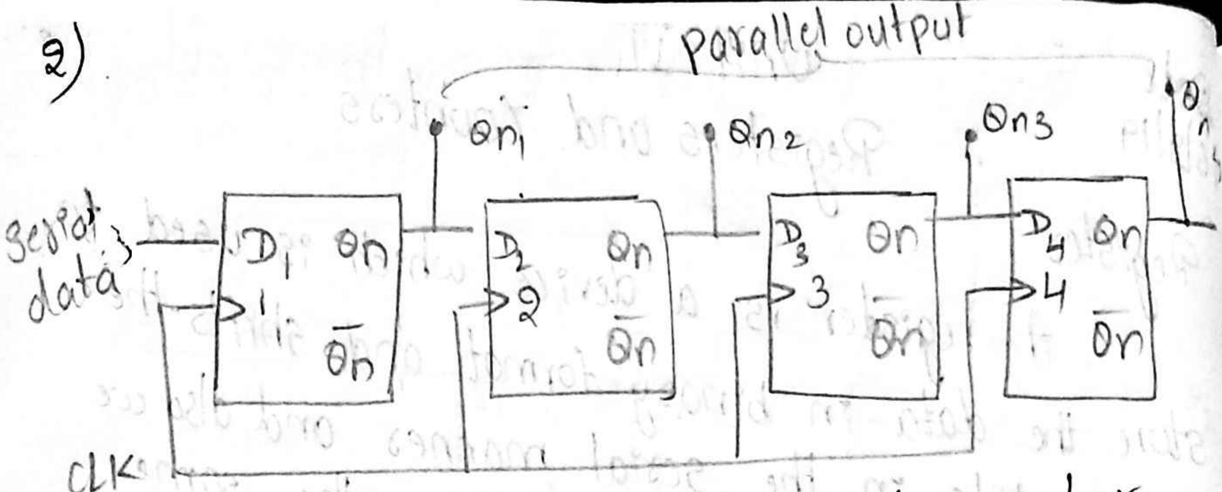
3)



Parallel-in-parallel-out shift register

4) Para

2)



Serial - in - parallel - out shift register

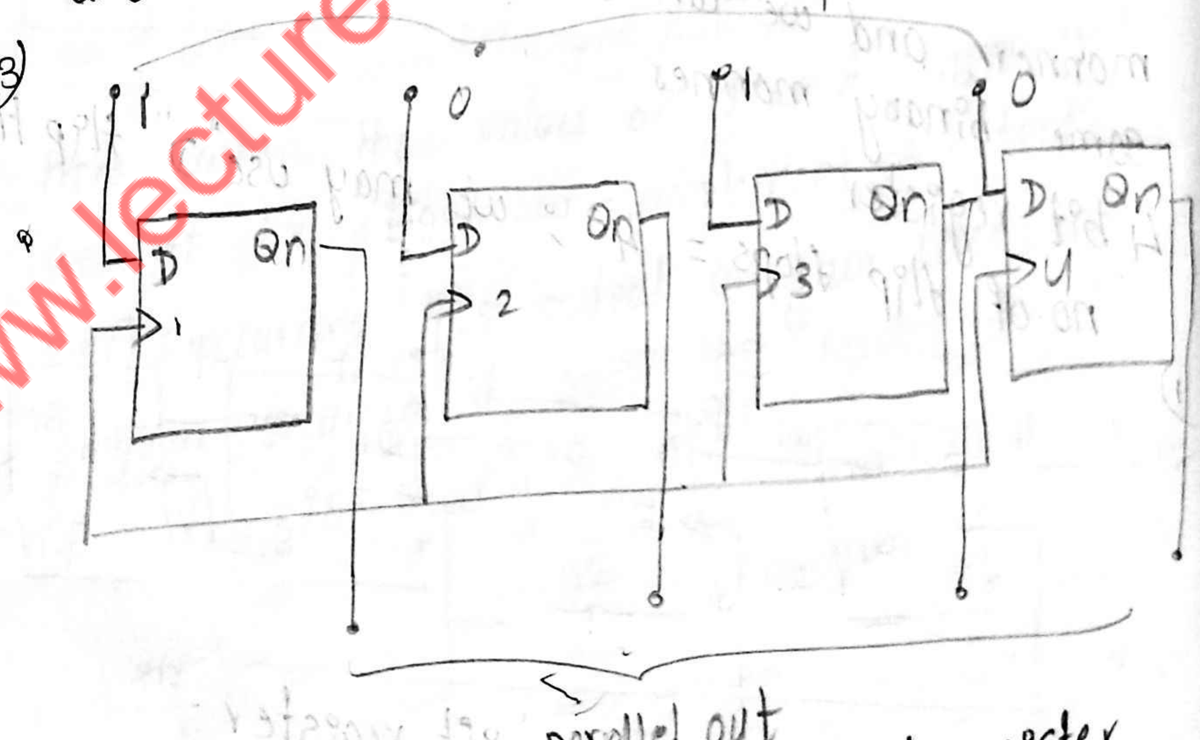
4 3 2 1
1 0 1 0

1010 →

	ops across f/f			
CLK	D_1	D_2	D_3	D_4
0	–	–	–	–
1	0	–	–	–
2	1	0	–	–
3	0	1	0	–
4	1	0	1	0

In this register the data entered in serial and collected in parallel out

3)

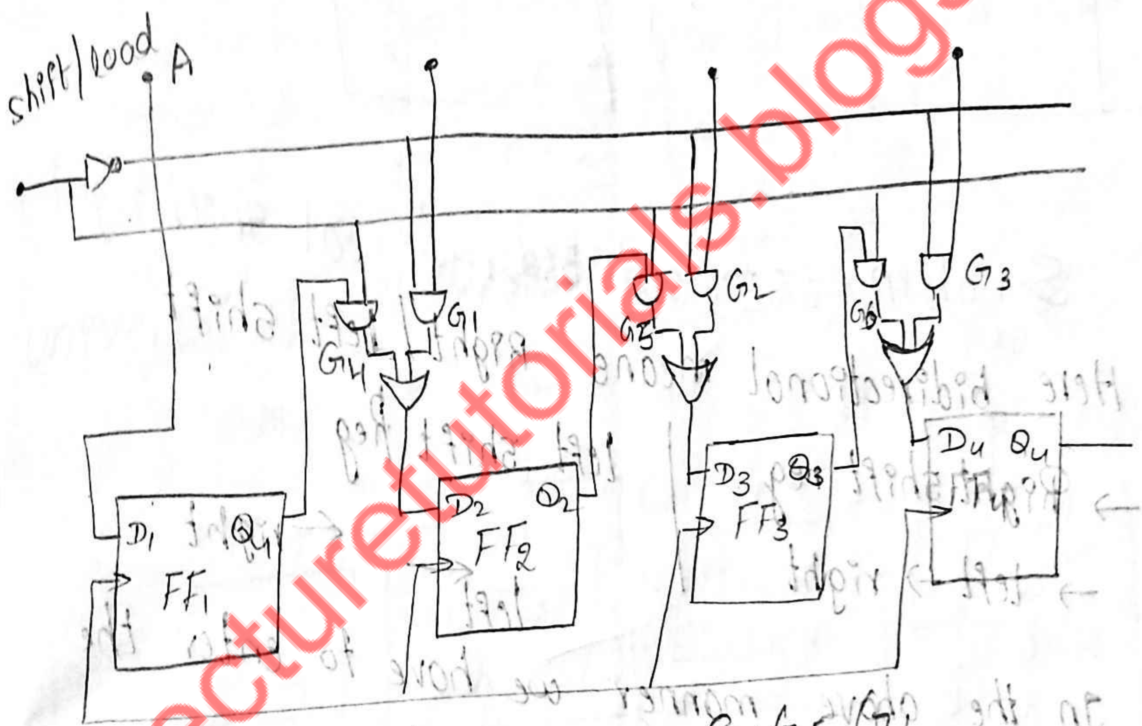


Parallel - in - parallel - out shift register

CLK	D_1	D_2	D_3	D_4
0	-	-	-	-
1	1	0	1	0
2	Q_1	Q_2	Q_3	Q_4
	1	0	1	0

Note: The input in parallel and collected the output parallel

4) Parallel-in serial out shift register



$G_1 G_2 G_3$ $G_4 G_5 G_6$

shift/load = 1 0 0 0 enable

Disable load

shift/load = 0 shift 0 0 0

1 1 1

G_1 G_2 G_3

A B C D

G_4 G_5 G_6

Q_1 Q_2 Q_3

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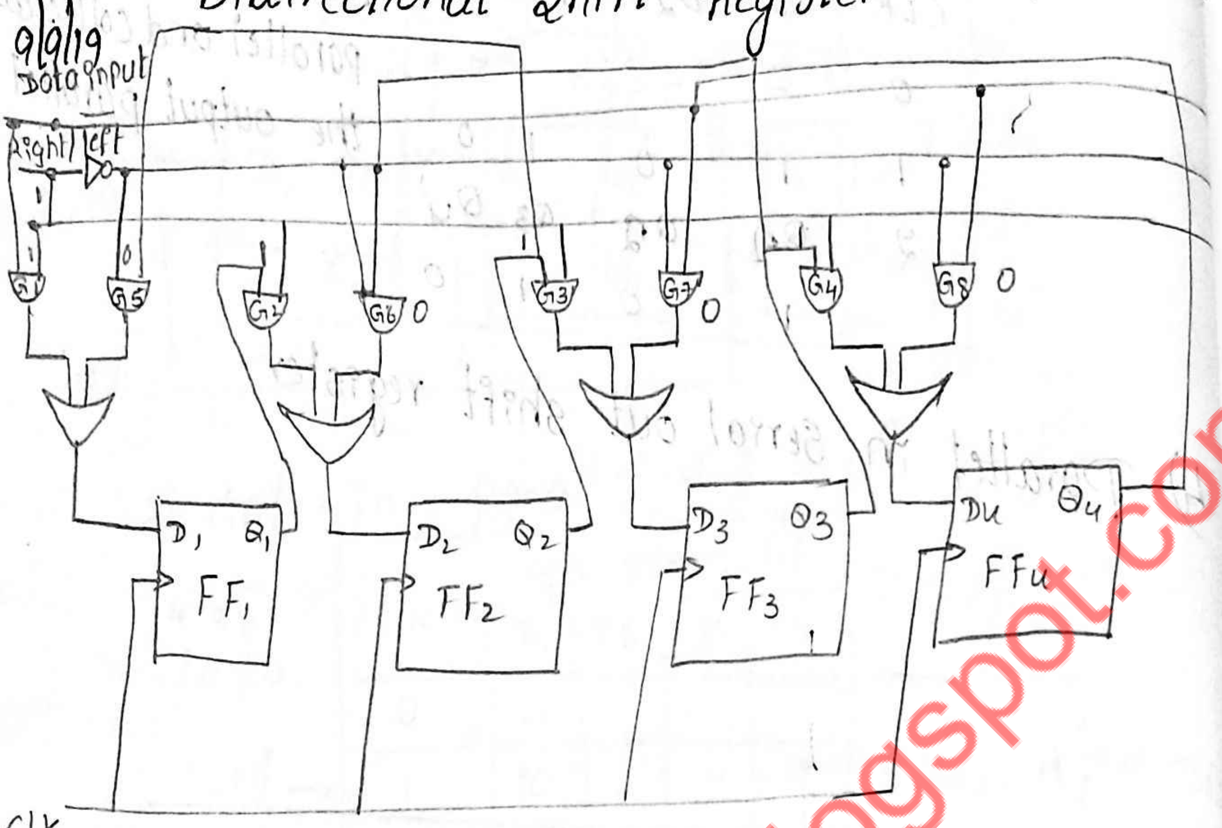
Bidirectional Shift Register (D- flip flop)



Serial-in - serial out Bidirectional shift register

Here bidirectional means Right / left shift

→ Right shift reg | left shift Reg

→ left → right | ← right left

In the above manner we have to enter the data according to arrow 'marks'

① Right/left = 1

G_1	G_2	G_3	G_4	G_5	G_6	G_7	G_8
1	1	1	1	0	0	0	0
enabled state				disabled-state			

Example

Data input 1111 left

CLK	D_1	D_2	D_3	D_4	
	0	0	0	0	→ initial state
0	0	0	0	0	→ (out)
1 →	1 →	0 →	0 →	0	
2 →	1 →	1 →	0 →	0	
3 →	1 →	1 →	1 →	0	
4 →	1 →	1 →	1 →	1	

(2)

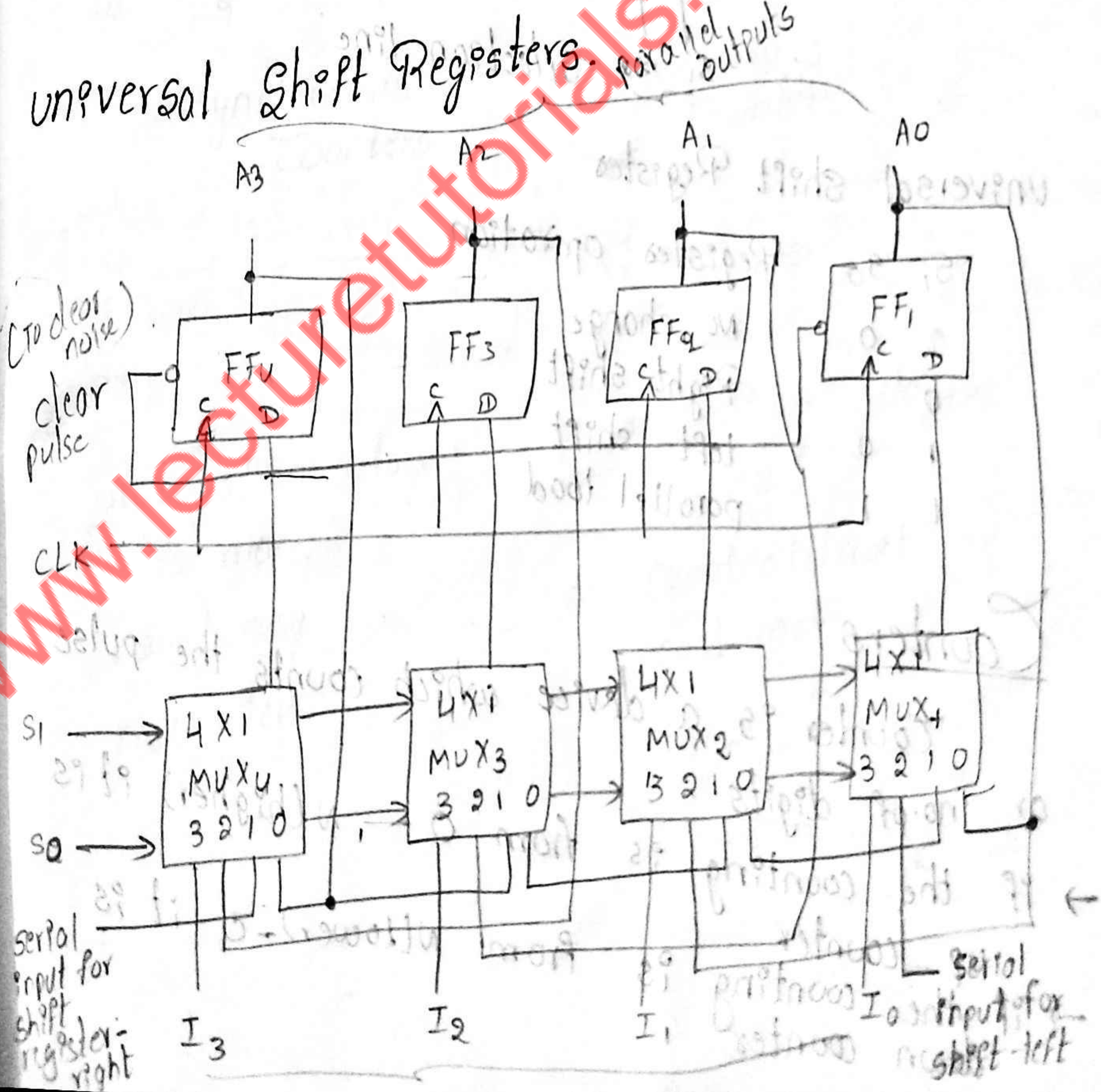
right/$\overline{left}$ = 0

G_1	G_2	G_3	G_4	G_5	G_6	G_7	G_8
0	0	0	0	1	1	1	1
disabled				enabled			

example

CLK	G_5 D_1	G_6 D_2	G_7 D_3	G_8 D_4	
0	0 ←	0 ←	0 ←	0	
1	0 ←	0 ←	0 ←	1	← data input right 1111
2	0 ←	0 ←	1 ←	1	
3	0 ←	1 ←	1 ←	1	
4	1 ←	1 ←	1 ←	1	

Universal Shift Registers.

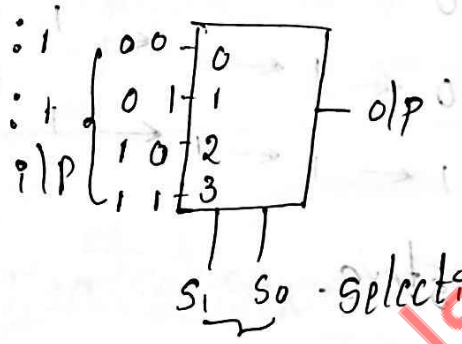


* Enter the data in serial and collecting the data in parallel called universal shift registers.
* universal shift register consists of 'D' flip flops and multiplexers
* Multiplexer: which has 2^n inputs and 1 output is called multiplexer

$2^n : 1$ where n = no. of selection line.
i/p o/p

Ex:- 4:1

$2^2 : 1$



00 - 0
01 - 1
11 - 2
10 - 3

Universal shift Register

S_1	S_0	Register operation
0	0	No change
0	1	Right shift
1	0	left shift
1	1	parallel load

Counters

Counter is a device which counts the pulse or no. of digits

→ if the counting is from 0 — N(higher) it is up counter

→ if the counting is from N(lower) - 0 it is down counter

Counters are of two types

→ synchronus counters

→ Asynchronus counters

CLK	decimal count
1	0
2	1
3	2
4	3
5	4
6	5
7	6
8	7
9	8
10	9

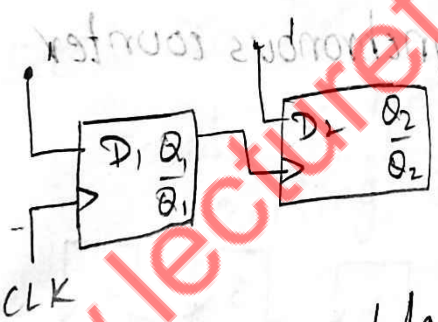
Asynchronus counters

In asynchronous counters, the output of first flip flop is given to the clk as second flip flop and propagation delay is occured

Synchronous Counters

In synchronous counters, the clk pulse is same and no propagation delay

Asynchronous Counters

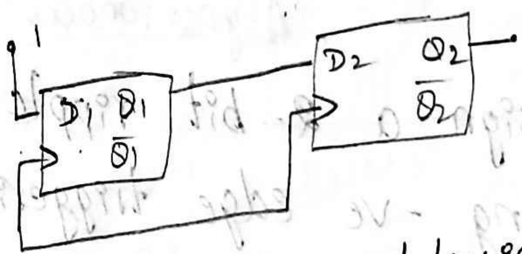


propagation delay is more

count easy

cost less

Synchronous Counters



propagation delay is less

count difficult

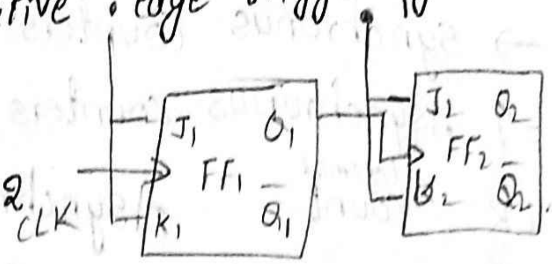
cost more

1. Design a two bit ripple up-counter using J-K flip flop by negative edge triggering

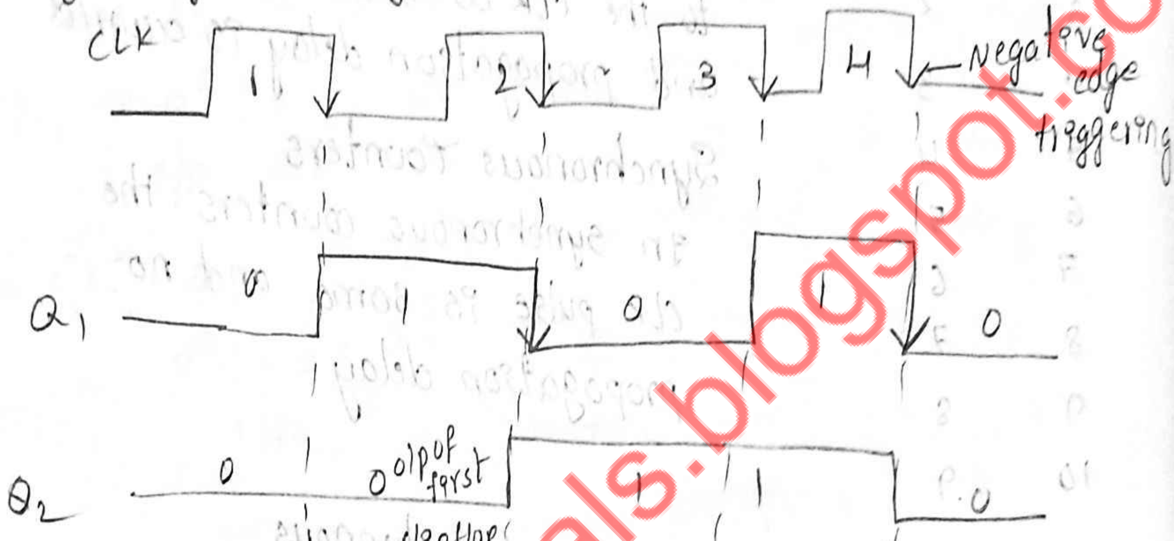
no. of bits $n = 2$

no. of flip flops $= 2$

(J K F/F)

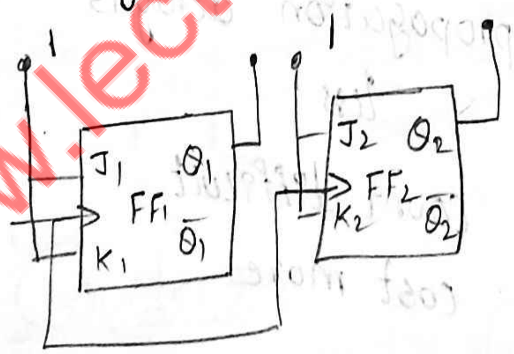


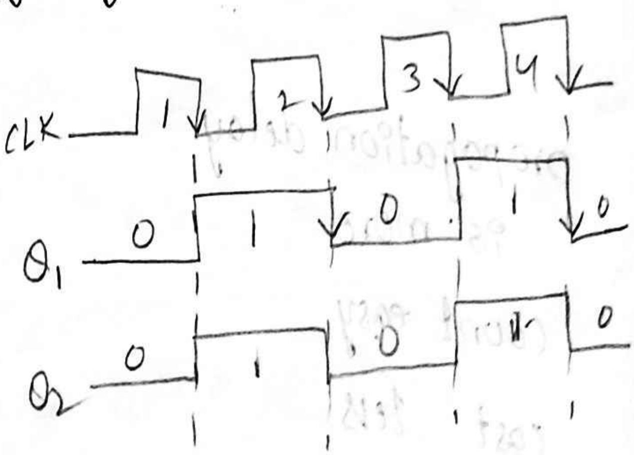
By using '-ve' edge triggering



Asynchronous counter

2. Design a 2-bit ripple up-synchronous counter using -ve edge triggering





$n =$ no. of bits $= 2$

no. of F/F $= 2$

(J K F/F)

synchronous counter by -ve edge triggering

Design of Synchronous Counters

It is represented as bit counter or divide by or ~~nth~~ counter or modulo ~~nth~~ countor or mod ~~nth~~ counter.

Design a decade counter or mod 10 counter using T flip flop.

Counters.

n bit counter

Modulo - N counter

MOD - N counter

Divide by N counter

· N = no. of counter.

N = 0 to N-1

Ex: N = 10

MOD = 10 counter

N = 10 (0-9)

counting sequence

no. of f/fs are n.

Decade Counter

Count the numbers = N = 10

counting sequence (0-(N-1))

(0-9)

no. of f/f required to construct the counter

n = no. of f/fs.

n = 4

$2^n \geq N$

n=0 $2^0 \ngeq 10$

n=1 $2^1 \ngeq 10$

n=2 $2^2 \ngeq 10$

n=3 $2^3 \ngeq 10$

n=4 $2^4 \geq 10$

CLK	Dc no		Present state Q_D	Q_C	Q_B	Q_A		Next state Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_D	T_C	T_B	T_A
1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1
2	1	1	0	0	0	1	2	0	0	1	0	0	0	1	1
3	2	2	0	0	1	0	3	0	0	1	1	0	0	0	1
4	3	3	0	0	1	1	4	0	1	0	0	0	1	1	1
5	4	4	0	1	0	0	5	0	1	0	1	0	0	0	1
6	5	5	0	1	0	1	6	0	1	1	0	0	0	1	1
7	6	6	0	1	1	0	7	0	1	1	1	0	0	0	1
8	7	7	0	1	1	1	8	1	0	0	0	1	1	1	1
9	8	8	1	0	0	0	9	1	0	0	1	0	0	0	1
10	9	9	1	0	0	1	0	0	0	0	0	1	0	0	1

Excitation table of T F/F

P.S Q_n	N.S Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

T_A

Q_DQ_C \ Q_BQ_A	00	01	11	10
00	1_0	1_1	1_3	1_2
01	1_4	1_5	1_7	1_6
11	X_{12}	X_{13}	X_{15}	X_{14}
10	1_8	1_9	X_{11}	X_{10}

double octent

$T_A = 1$

T_B

Q_DQ_C \ Q_BQ_A	00	01	11	10
00	0	1_1	1_3	2
01	4	1_5	1_7	6
11	X_{12}	X_{13}	X_{15}	X_{14}
10	8	9	X_{11}	X_{10}

quard

$$\text{quard} = (\bar{Q_D}\,\bar{Q_C} + \bar{Q_D}Q_C)(Q_BQ_A + \bar{Q_B}Q_A)$$

$$= \bar{Q_D}(\bar{Q_C} + Q_C) \cdot Q_A(Q_B + \bar{Q_B})$$

$$= \bar{Q_D}\,Q_A$$

T_C

Q_DQ_C \ Q_BQ_A	00	01	11	10
00	0	1	1_3	2
01	4	5	1_7	6
11	X_{12}	X_{13}	X_{15}	X_{14}
10	8	9	X_{11}	10

$T_C = Q_BQ_A$

T_D

Q_DQ_C \ Q_BQ_A	00	01	11	10
00	0	1	3	2
01	4	5	1_7	6
11	X_{12}	X_{13}	X_{15}	X_{14}
10	8	1_9	X_{11}	X_{10}

quard $= Q_DQ_A$

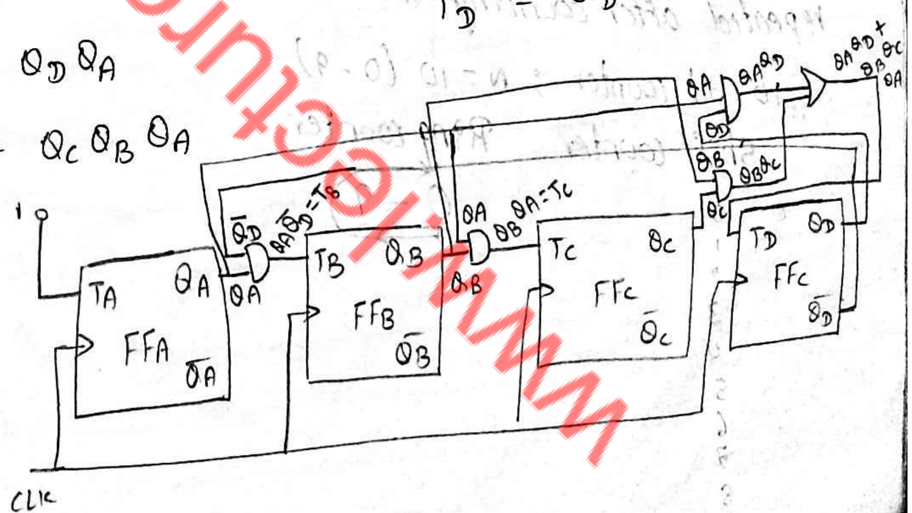
Pair $= Q_CQ_BQ_A$

$T_A = 1$

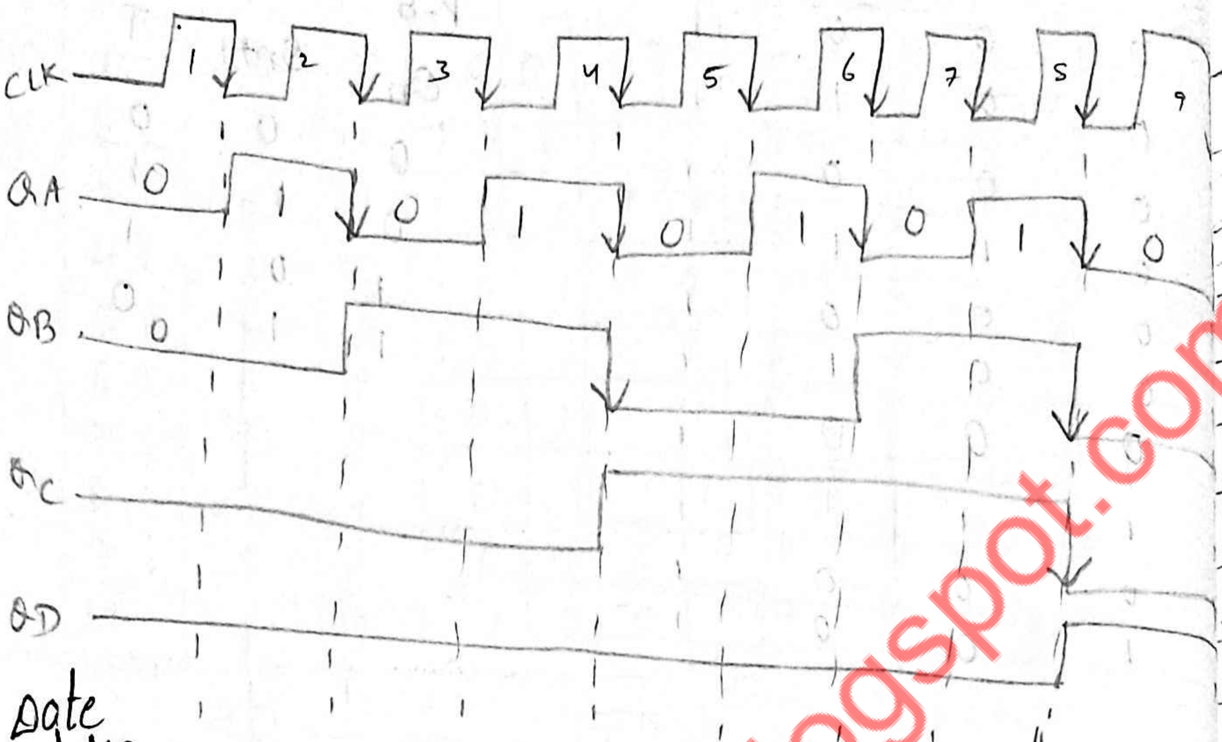
$T_B = \bar{Q_D}\,Q_A$

$T_C = Q_BQ_A$

$T_D = Q_DQ_A + Q_CQ_BQ_A$



Timing Diagram



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Design a 10 bit ring and shift counter with D flip flops

10 bit shift and ring counter

It is called shift counter because it shifts the value from present to next

It is called ring counter when the cycle is repeated after counting the maximum value

10 bit counter ; N = 10 (0 - 9)

Shift counter   Ring counter

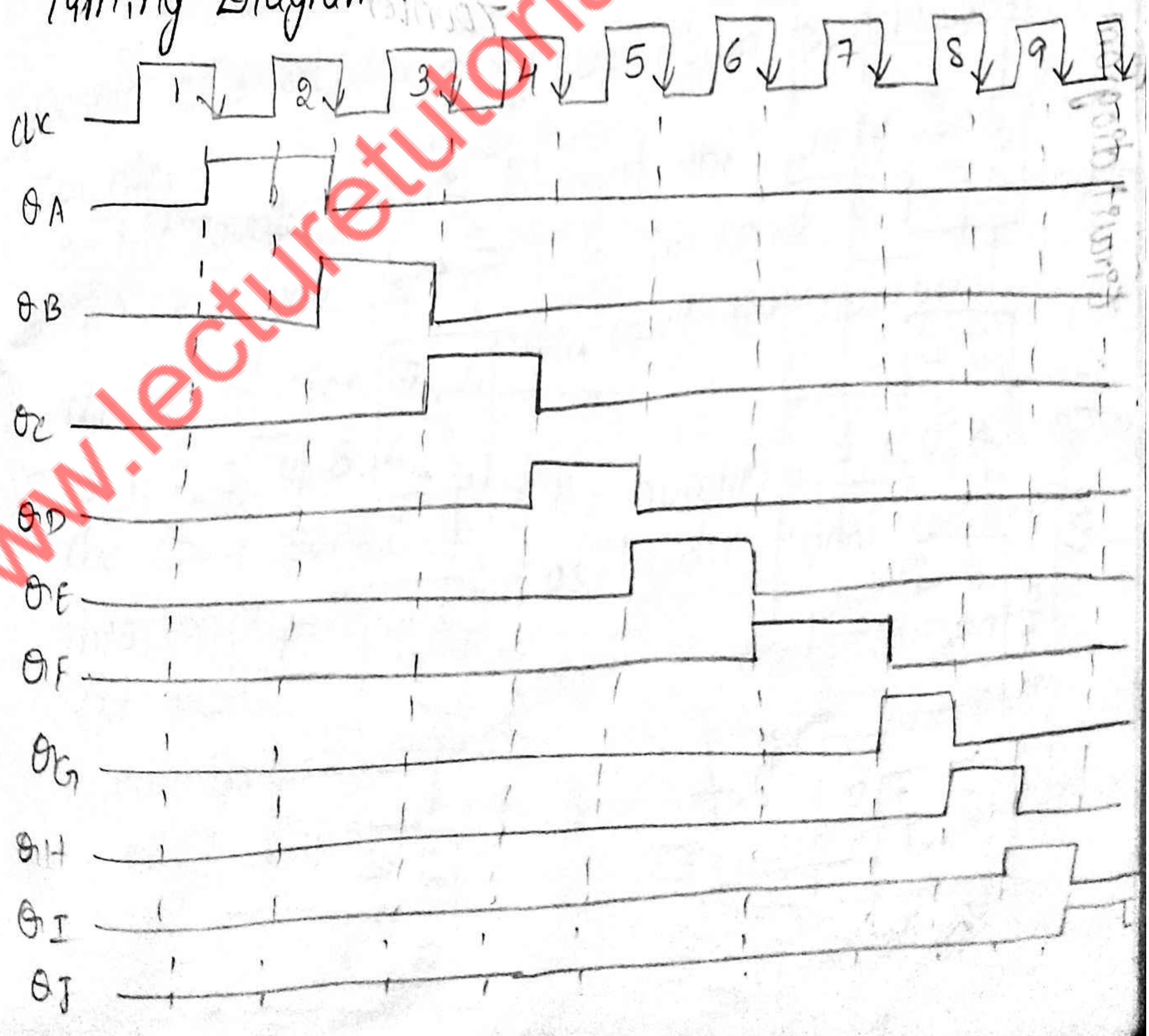
0 – 0
1
2
3
4
5
6
7
8
9

0 – 9

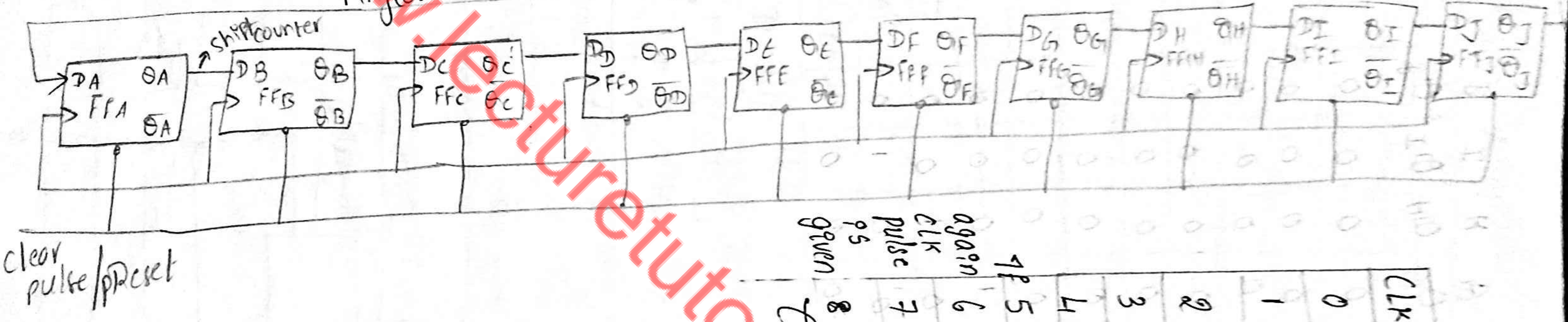
Truth table

		A	B	C	D	E	F	G	H	I	J
CLK	Decimal number	Q_A	Q_B	Q_C	Q_D	Q_E	Q_F	Q_G	Q_H	Q_I	Q_J
0		0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0
2	1	0	1	0	0	0	0	0	0	0	0
3	2	0	0	1	0	0	0	0	0	0	0
4	3	0	0	0	1	0	0	0	0	0	0
5	4	0	0	0	0	1	0	0	0	0	0
6	5	0	0	0	0	0	1	0	0	0	0
7	6	0	0	0	0	0	0	1	0	0	0
8	7	0	0	0	0	0	0	0	1	0	0
9	8	0	0	0	0	0	0	0	0	1	0
10	9	0	0	0	0	0	0	0	0	0	1

Timing Diagram



Circuit diagram for shift and ring counter

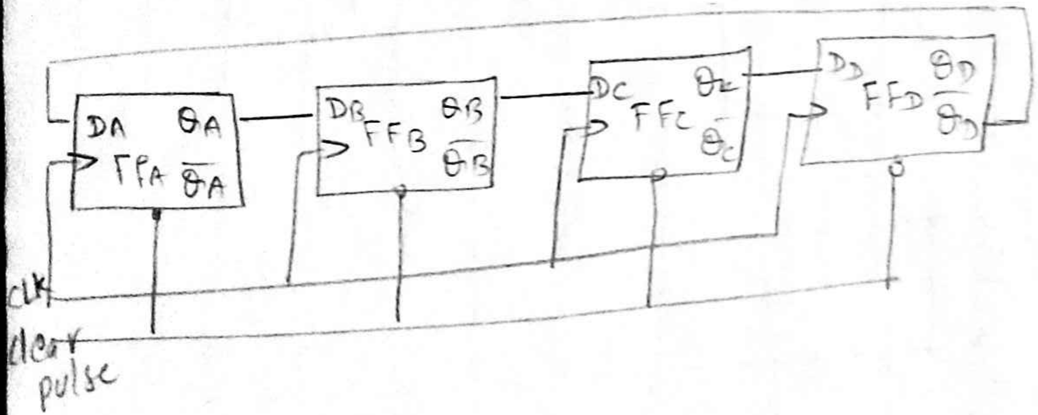


Twisted ring counter

CLK	QA	QB	QC	QD	$\overline{Q_D}$
0	0	0	0	0	1
1	1	0	0	0	1
2	1	1	0	0	1
3	1	1	1	0	1
4	1	1	1	1	0
5	0	1	1	1	0
6	0	0	1	1	0
7	0	0	0	1	0
8					

If again CLK pulse is given

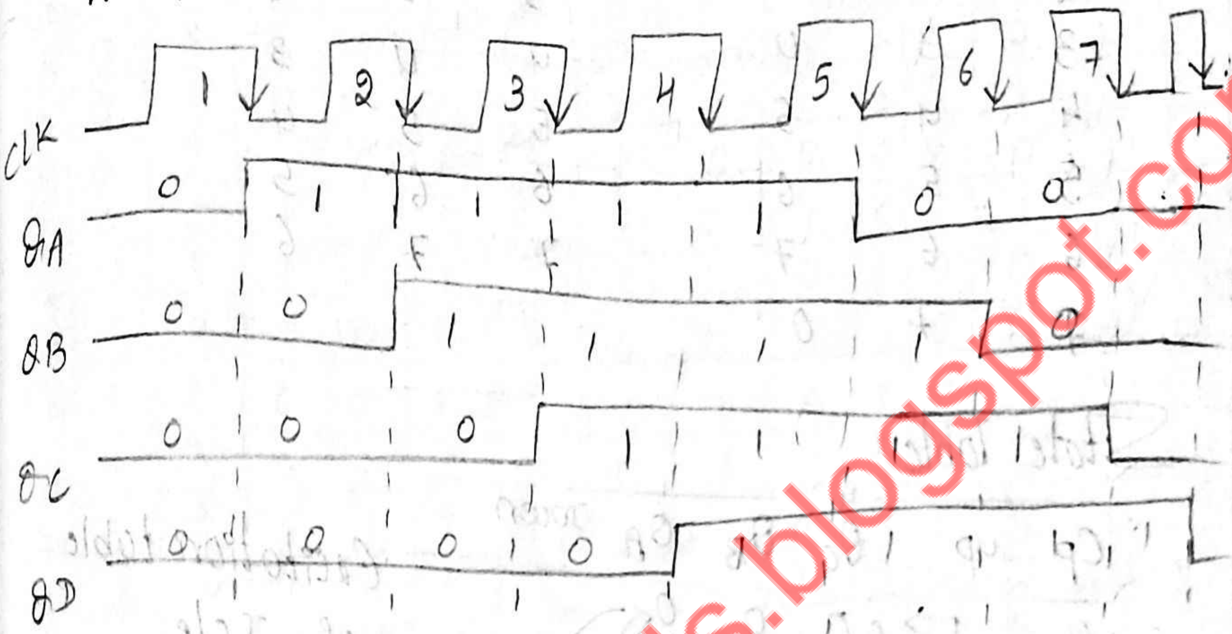
Circuit diagram for Johnson counter



Design a 4-bit Johnson counter or a 4-bit shift and twisted ring counter with D flip flops

4 bit Johnson counter / 4 bit and twisted ring counter

N = 4 (0 - 3) [4+4 = 8 (0 - 7)]



Timing Diagram

Design a 3-bit [down-5] up-down synchronous counter

3-bit counter enable to count the numbers as $2^n = N$

$2^3 = 8$ you can be able to count 8 i.e., (0 - 7)

The up-counter can able to count the numbers 0, 1, 2, 3, 4, 5, 6, 7, 0..

The down counter count the numbers 7, 6, 5, 4, 3, 2, 1, 0

This counter is known as bi-directional counter (up-down)

counting = N. sequence

no. of flip flops = n = 3

Mode signal

up / $\overline{DOWN}$ = 1 → 1 0 ON OFF	UP counter
up / $\overline{down}$ = 0 → 0 1 OFF ON	down counter

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Up Counter

	P.S	N.S
0	0	1
1	1	2
2	2	3
3	3	4
4	4	5
5	5	6
6	6	7
7	7	0

Down Counter

	P.S	N.S
0	0	7
1	1	0
2	2	1
3	3	2
4	4	3
5	5	4
6	6	5
7	7	6

State Table

Cp	up	Q_C	Q_B	Q_A	Down
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

Excitation table of T F/F

P.S Q_n	N.S Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

For K-map

$$T_A = \sum_m (0, 1, 2, --- 15)$$

$$T_B = \sum_m (0, 2, 4, 6, 9, 11, 13, 15)$$

$$T_C = \sum_m (0, 4, 11, 15)$$

Excitation table

	$U/\overline{D}$		present state Q_C	Q_B	Q_A	No. need	next state Q_{C+1}	Q_{B+1}	Q_{A+1}		T_C	T_B	T_A
0	0	0	0	0	0	0	1	1	1	7	1	1	1
1	0	1	0	0	1	1	0	0	0	0	0	0	1
2	0	2	0	1	0	2	0	0	1	1	0	1	1
3	0	3	0	1	1	3	0	1	0	2	0	0	1
4	0	4	1	0	0	4	0	1	1	3	1	1	1
5	0	5	1	0	1	5	1	0	0	4	0	0	1
6	0	6	1	1	0	6	1	0	1	5	0	1	1
7	0	7	1	1	1	7	1	1	0	6	0	0	1
8	1	0	0	0	0	8	0	0	1	1	0	1	1
9	1	1	0	0	1	9	0	1	0	2	0	1	1
10	1	2	0	1	0	10	0	1	1	3	0	0	1
11	1	3	0	1	1	11	1	0	0	4	1	1	1
12	1	4	1	0	0	12	1	0	1	5	0	0	1
13	1	5	1	0	1	13	1	1	0	6	0	1	1
14	1	6	1	1	0	14	1	1	1	7	0	0	1
15	1	7	1	1	1	15	0	0	0	0	1	1	

T_A

$U/\overline{D}Q_C$ \ Q_BQ_A	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

T_B

$U/\overline{D}Q_C$ \ Q_BQ_A	00	01	11	10
00	1			1
01	1			1
11		1	1	
10		1	1	

T_C

$U/\overline{D}Q_C$ \ Q_BQ_A	00	01	11	10
00	1			
01	1			
11				1
10				1

$T_A = 1$

$q_1 \rightarrow U/D\, Q_A$

$q_2 \rightarrow \overline{U/D}\,\overline{Q_A}$

$p_1 \rightarrow \overline{U/D}\,\overline{Q_B}\,\overline{Q_A}$

$p_2 \rightarrow U/D\, Q_B Q_A$

$T_B = U/D\, Q_A + \overline{U/D}\,\overline{Q_A}$

$T_C = \overline{U/D}\,\overline{Q_B}\,\overline{Q_A} + U/D\, Q_B Q_A$

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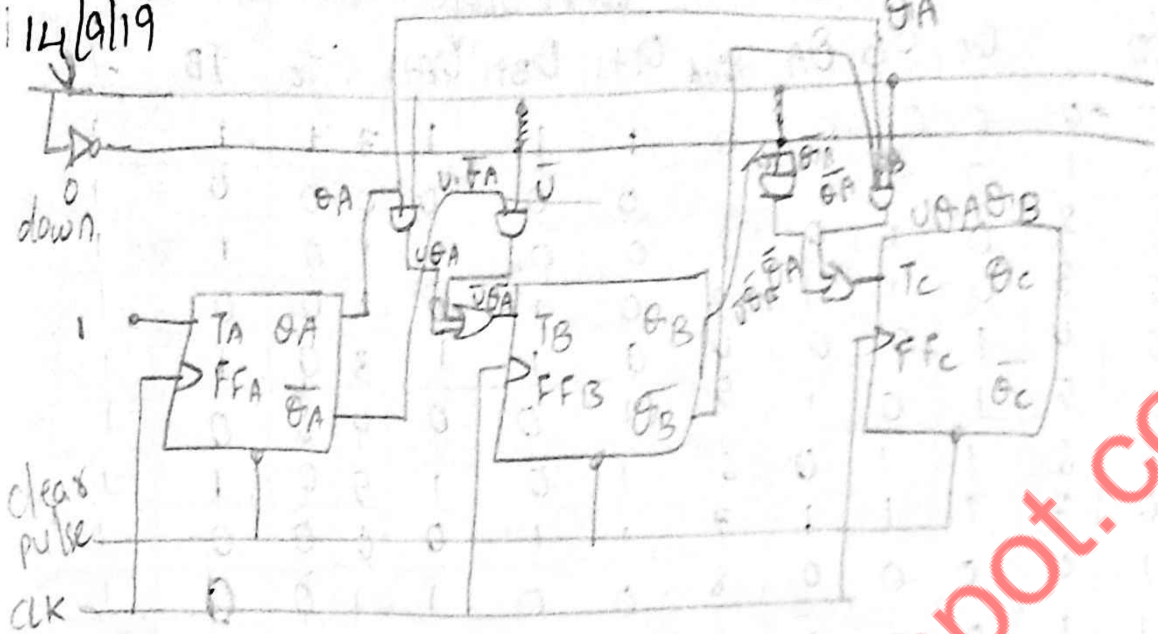


logic diagram

Design divide by "6" counter using T flip flop
Mod 6 counter

Divide by 6 counter (or) MOD 6 - counter

no. of counts = 6 ; counting range 0 - (N-1)
(0 - 5)

n = no. of flip flops $\quad 2^n \geq N$

$n=1 \quad 2^1 \ngeq 6$

$n=2 \quad 2^2 \ngeq 6$

$n=3 \quad 2^3 \geq 6$

No. of flip flops = 3

No. of bits = no. of flip flops = 3

Note

MOD - 6 (0 - 5) ; n = 3 (0 - 7)
6, 7 or don't care

- 5 (0 - 4) ; n = 3 (0 - 7)
(5, 6, 7) don't care

P.S	N.S
0	1
1	2
2	3
3	4
4	5
5	0

CLK	D.no	Q_C (P.S)	Q_B (P.S)	Q_A (P.S)		Q_{C+1} (N.S)	Q_{B+1} (N.S)	Q_{A+1} (N.S)	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1	0	0	1
1	1	0	0	1	2	0	1	0	0	1	1
2	2	0	1	0	3	0	1	1	0	0	1
3	3	0	1	1	4	1	0	0	1	1	1
4	4	1	0	0	5	1	0	1	0	0	1
5	5	1	0	1	0	0	0	0	1	0	1
6	6	X	X	X							
7	7	X	X	X							

Excitation table of T f/f

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

$$T_A = \sum_m (0, 1, 2, 3, 4, 5)$$

$$T_B = \sum_m (1, 3)$$

$$T_C = \sum_m (3, 5)$$

T_A

$Q_C \backslash Q_BQ_A$	00	01	11	10
0	1 (0)	1 (1)	1 (3)	1 (2)
1	1 (4)	1 (5)	X (7)	X (6)

T_B

$Q_C \backslash Q_BQ_A$	00	01	11	10
0	0	1	1 (3)	(2)
1	(4)	(5)	X (7)	X (6)

T_C

$Q_C \backslash Q_BQ_A$	00	01	11	10
0	(0)	(1)	1 (3)	(2)
1	(4)	1 (5)	X (7)	X (6)

P_2, P_1

$T_A = 1$

$T_B = \bar{Q}_C \cdot Q_A$

$T_C = \cancel{\bar{Q}_C Q_B Q_A +}$

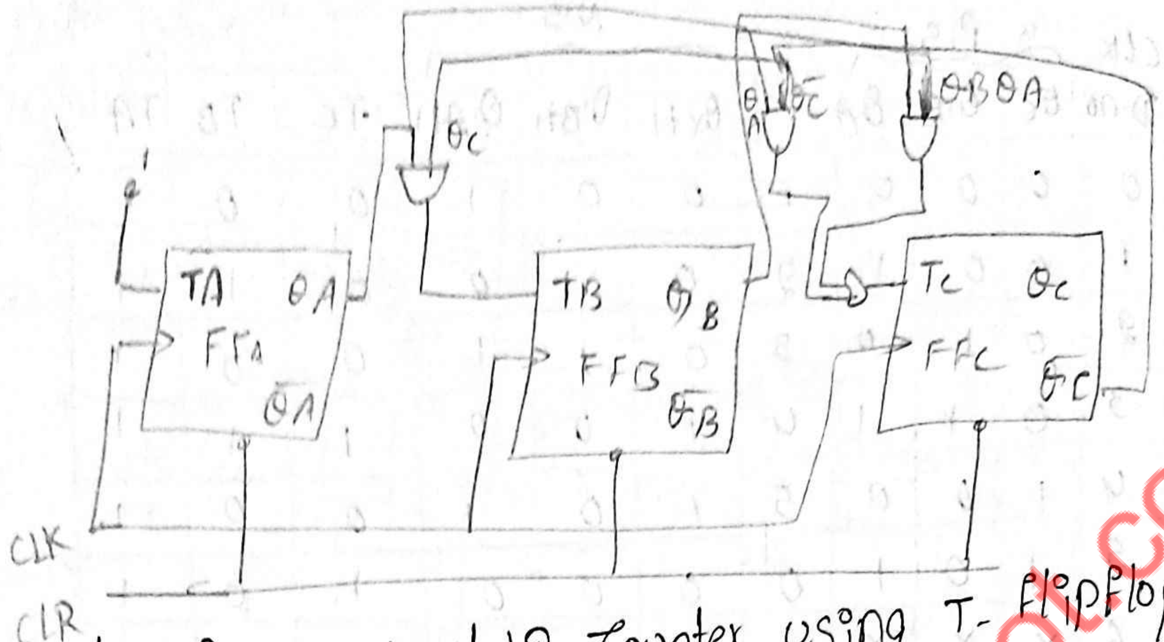
$\cancel{\bar{Q}_C Q_B Q_A}$

$P_1(\bar{Q}_C \cdot Q_A) + P_2($

$(\bar{Q}_C + Q_C)(Q_B Q_A)$

$\bar{Q}_C Q_A + Q_B Q_A$

$T_C = P_2 + P_1 \rightarrow (\bar{Q}_C Q_A + Q_B Q_A)$



Date 16/9/19 **Design Mod-12 Counter using T-flipflops**

The total no of counts $N = 12$

Counting sequence - 0 to $N-1$

0 to $(12-1)$

0 to 11 (12, 13, 14, 15) don't cares

T flip flop

P.S Q_n	N.S Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

No.of flip flops - n $\quad 2^n \geq N$

n	
1	$2^1 \ngeq 12$
2	$2^2 \ngeq 12$
3	$2^3 \ngeq 12$
4	$2^4 \geq 12$

No.of flip flops = No.of binary bits

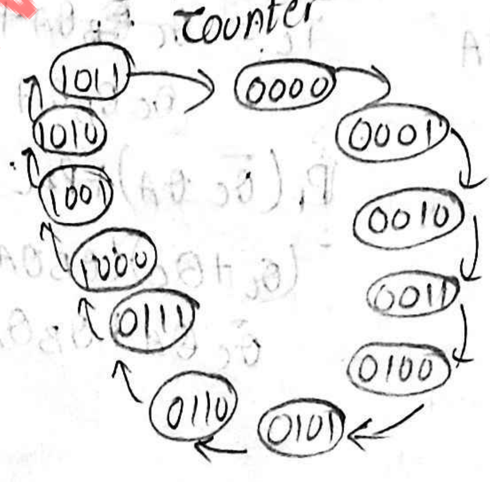
$n = 4$; $0 - (2^n - 1)$

$0 - (2^4 - 1)$

$0 - (16 - 1)$

$0 - 15$

Counter



P.S	N.S
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	10
10	11
11	0

D.NO	Q_D (8)	Q_C (4)	Q_B (2)	Q_A (1)		Q_{D+1} (8)	Q_{C+1} (4)	Q_{B+1} (2)	Q_{A+1} (1)	T_D	T_C	T_B	T_A
	P.S.					N.S.				T flipflop			
0	0	0	0	0	1	0	0	0	1	0	0	0	1
1	0	0	0	1	2	0	0	1	0	0	0	1	1
2	0	0	1	0	3	0	0	1	1	0	0	0	1
3	0	0	1	1	4	0	1	0	0	0	1	1	1
4	0	1	0	0	5	0	1	0	1	0	0	0	1
5	0	1	0	1	6	0	1	1	0	0	0	1	1
6	0	1	1	0	7	0	1	1	1	0	0	0	1
7	0	1	1	1	8	1	0	0	0	1	1	1	1
8	1	0	0	0	9	1	0	0	1	0	0	0	1
9	1	0	0	1	10	1	0	1	0	0	0	1	1
10	1	0	1	0	11	1	0	1	1	0	0	0	1
11	1	0	1	1	0	0	0	0	0	1	0	1	1

$T_A = \sum_m (0, 1, 2, \ldots 11)$

$T_B = \sum_m (1, 3, 5, 7, 9, 11)$

$T_C = \sum_m (3, 7)$; $T_D = \sum_m (7, 11)$

T_A

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	1_0	1_1	1_3	1_2
01	1_4	1_5	1_7	1_6
11	X_{12}	X_{13}	X_{15}	X_{14}
10	1_8	1_9	1_{11}	1_{10}

octent (1)

$T_A = 1$

T_B

$Q_DQ_C \backslash Q_BQ_A$	00	01 ($\bar{Q}_BQ_A$)	11 (Q_BQ_A)	10 ($Q_B\bar{Q}_A$)
00 ($\bar{Q}_D\bar{Q}_C$)	0	1_1	1_3	2
01 ($\bar{Q}_DQ_C$)	4	1_5	1_7	6
11 (Q_DQ_C)	X_{12}	X_{13}	X_{15}	X_{14}
10 ($Q_D\bar{Q}_C$)	8	1_9	1_{11}	10

octent $T_B = Q_A$

T_C

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	0	1	1_3	2
01	4	5	1_7	6
11	X_{12}	X_{13}	X_{15}	X_{14}
10	8	9	11	10

Pair (3,7) ; $T_C = \bar{Q}_D Q_B Q_A$

T_D

$Q_DQ_C \backslash Q_BQ_A$	00	01	11	10
00	0	1	3	2
01	4	5	1_7	6
11	X_{12}	X_{13}	X_{15}	X_{14}
10	8	9	1_{11}	10

pair (7,5) ; pair (15,11)

$T_D = Q_C Q_B Q_A + Q_D Q_B Q_A$

$T_A = 1$; $T_B = Q_A$; $T_C = \overline{Q_D} Q_B Q_A$; $T_D = Q_C Q_B Q_A + Q_D Q_B Q_A$