ASSEMBLY LANGUAGE CODES

1.
```
LI R2,272
LI R3,300
L.D F6,34(R2)
L.D F2,45(R3)
MUL.D F0,F2,F4
SUB.D  F8,F6,F2
DIV.D  F10,F0,F6
ADD.D  F6,F8,F2
```

2.
```
LI R4, 260
LI R5, 272
LI R1, 8
LI R2, 4
LI R3, 0
GG: L.D F1, 4(R4)
L.D F2, 8(R5)
ADD.D F4, F6, F2
SUB.D F5, F7, F1
MUL.D F6, F1, F5
ADD.D F7, F2, F6
ADD.D F6, F1, F7
DADDI R4, R4, 20
DADDI R5, R5, 8
DSUB R1, R1, R2
BNE R1, R3, GG
HLT
HLT
```

3.
```
LI R1, 8
LI R2, 312
LI R4, 256
PP : LW R3, 0(R4)
L.D F1, 12(R4)
ADD.D F3, F1, F1
L.D F2, 28(R4)
ADD.D F1, F2, F3
MUL.D F4, F2, F3
DIV.D F5, F4, F3
MUL.D F6, F1, F3
S.D F6, 32(R2)
ADD.D F4, F1, F3
DADD R4, R1, R2
DADD R3, R4, R3
SW R3, 60(R4)
DSUBI R3, R3, 4
BEQ R2, R3, PP
HLT
HLT
```

4.
```
Loop : L.D F0,0(R1)
       ADD.D F4,F0,F2
       S.D F4,0(R1)
       DADDUI R1,R1,#-8
       BNE R1,R2,LOOP
```

5.
```
LOOP: L.D F0,0(R1)
ADD.D F4,F0,F2
```

```
        S.D F4,0(R1)
        DADDUI R1,R1,#-8
        BNE R1,R2,LOOP
```

6.
```
LOOP: L.D F0,0(R1)
        DADDUI R1,R1,#-8                    //LOOP UNROLLED BY STALLS
        ADD.D F4,F0,F2
        S.D F4,0(R1)
        BNE R1,R2,LOOP
```

7.
```
LOOP: L.D F0,0(R1)
        ADD.D F4,F0,F2
        S.D F4,0(R1)
        L.D F6,-8(R1)
        ADD.D F8,F6,F2
        S.D F8,-8(R1)
        L.D F10,-16(R1)
        ADD.D F12,F10,F2
        S.D F12,-16(R1)
        L.D F14,-24(R1)
        ADD.D F16,F14,F2
        S.D F16,-24(R1)
        DADDUI R1,R1,#-32
        BNE R1,R2,LOOP
```

8.
```
LOOP: L.D F0,0(R1)
        L.D F6,-8(R1)
        L.D F10, -16(R1)
        L.D F14,-24(R1)
        ADD.D F4,F0,F2
        ADD.D F8,F6,F2
        ADD.D F12,F10,F2
        ADD.D F16,F14,F2
        S.D F4,0(R1)
        S.D F8,-8(R1)
        DADDUI R1,R1,#-32
        S.D F12,16(R1)
        S.D F16,8(R1)
        BNE R1,R2,LOOP
```

9.
```
        L.D F0,a
        DADDUI R4,RX,#512
LOOP: L.D F2,0(RX)
        MUL.D F2,F2,F0
        L.D F4,0(RY)
        ADD.D F4,F4,F2
        S.D F4,9(RY)
        DADDIU RX,RX,#8
        DADDIU RY,RY,#8
        DSUBU R20,R4,RX
        BNEZ  R20,LOOP
```

INSTRUCTION SET

1.

```
LI R2,272
LI R3,300
L.D F6,34(R2)
L.D F2,45(R3)
MUL.D F0,F2,F4
SUB.D  F8,F6,F2
DIV.D  F10,F0,F6
ADD.D  F6,F8,F2
```

CONFIG-1 : FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache: 4, 4

Label	Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
	LI R2,272	13	14	15	16	17	N	N	N
	LI R3,300	14	18	19	20	21	N	N	Y
	LD F6,34(R2)	18	19	20	45	46	N	N	N
	LD F2,45(R3)	19	47	48	62	63	N	N	Y
	MUL.D F0,F2,F4	47	48	64	74	75	Y	N	N
	SUB.D F8,F6,F2	48	49	64	66	67	Y	N	N
	DIV.D F10,F0,F6	49	50	76	116	117	Y	N	N
	ADD.D F6,F8,F2	50	51	68	70	71	Y	N	N

Total number of access requests for instruction cache: 8
Number of instruction cache hits: 6
INSTRUCTION HIT RATIO =0.75
Total number of access requests for data cache: 4
Number of data cache hits: 2
DATA HIT RATIO =0.5
TOTAL CYCLES REQU TO COMPLETE THE WHOLE SET OF INSTRUCTIONS:117

CONFIG-2 : FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache: 4, 2

Label	Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
	LI R2,272	7	8	9	10	11	N	N	N
	LI R3,300	8	12	13	14	15	N	N	Y
	LD F6,34(R2)	15	16	17	36	37	N	N	N
	LD F2,45(R3)	16	38	39	59	60	N	N	Y
	MUL.D F0,F2,F4	38	39	61	71	72	Y	N	N
	SUB.D F8,F6,F2	39	40	61	63	64	Y	N	N
	DIV.D F10,F0,F6	46	47	73	113	114	Y	N	N
	ADD.D F6,F8,F2	47	48	65	67	68	Y	N	N

Total number of access requests for instruction cache: 8
Number of instruction cache hits: 4
INSTRUCTION HIT RATIO =0.5
Total number of access requests for data cache: 4
Number of data cache hits: 2
DATA HIT RATIO =0.5
TOTAL CYCLES REQU TO COMPLETE THE WHOLE SET OF INSTRUCTIONS:114

CONFIG-3 : FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache: 10,10

Label	Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
	LI R2,272	31	32	33	34	35	N	N	N
	LI R3,300	32	36	37	38	39	N	N	Y
	LD F6,34(R2)	36	37	38	52	53	N	N	N
	LD F2,45(R3)	37	54	55	69	70	N	N	Y
	MUL.D F0,F2,F4	54	55	71	81	82	Y	N	N
	SUB.D F8,F6,F2	55	56	71	73	74	Y	N	N
	DIV.D F10,F0,F6	56	57	83	123	124	Y	N	N
	ADD.D F6,F8,F2	57	58	75	77	78	Y	N	N

Total number of access requests for instruction cache: 8
Number of instruction cache hits: 7
INSTRUCTION HIT RATIO =7/8
Total number of access requests for data cache: 4
Number of data cache hits: 2
DATA HIT RATIO =0.5
TOTAL CYCLES REQU TO COMPLETE THE WHOLE SET OF INSTRUCTIONS:124

CONFIG-4 : FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache: 10,1

Label	Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
	LI R2,272	4	5	6	7	8	N	N	N
	LI R3,300	8	9	10	11	12	N	N	N
	LD F6,34(R2)	12	13	14	29	30	N	N	N
	LD F2,45(R3)	16	31	32	48	49	N	N	Y
	MUL.D F0,F2,F4	31	32	50	60	61	Y	N	N
	SUB.D F8,F6,F2	35	36	50	52	53	Y	N	N
	DIV.D F10,F0,F6	50	51	62	102	103	Y	N	N
	ADD.D F6,F8,F2	54	55	56	58	59	N	N	N

Total number of access requests for instruction cache: 8
Number of instruction cache hits: 0
INSTRUCTION HIT RATIO =0
Total number of access requests for data cache: 4
Number of data cache hits: 2
DATA HIT RATIO =0.5
TOTAL CYCLES REQU TO COMPLETE THE WHOLE SET OF INSTRUCTIONS:102

CONFIG-5 : FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache: 1,0

Label	Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
	LI R2,272	1	2	3	4	5	N	N	N
	LI R3,300	2	6	7	8	9	N	N	Y

LD F6,34(R2)	6	7	8	22	23	N	N	N
LD F2,45(R3)	7	24	25	39	40	N	N	Y
MUL.D F0,F2,F4	24	25	41	51	52	Y	N	N
SUB.D F8,F6,F2	25	26	41	43	44	Y	N	N
DIV.D F10,F0,F6	26	27	53	93	94	Y	N	N
ADD.D F6,F8,F2	27	28	45	47	48	Y	N	N

Total number of access requests for instruction cache: 8
Number of instruction cache hits: 7
INSTRUCTION HIT RATIO =7/8
Total number of access requests for data cache: 4
Number of data cache hits: 2
DATA HIT RATIO =0.5
TOTAL CYCLES REQU TO COMPLETE THE WHOLE SET OF INSTRUCTIONS:94

2.

```
 LI R1, 8
 LI R2, 312
 LI R4, 256
PP : LW R3, 0(R4)
 L.D F1, 12(R4)
 ADD.D F3, F1, F1
 L.D F2, 28(R4)
 SUB.D F1, F2, F3
 DIV.D F4, F2, F3
 MUL.D F5, F4, F3
 S.D F6, 32(R2)
 DADD R4, R1, R2
 SW R3, 60(R4)
 DADDI R3, R3, 4
 BEQ R2, R3, PP
 HLT
 HLT
```

CONFIG-1:FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache: 4,4

Label	Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
	LI R1,8	13	14	15	16	17	N	N	N
	LI R2,312	14	18	19	20	21	N	N	Y
	LI R4,256	18	22	23	24	25	N	N	Y
PP	LW R3,0(R4)	22	23	26	47	48	Y	N	N
	LD F1,12(R4)	35	49	50	64	65	N	N	Y
	ADD.D F3,F1,F1	49	50	66	68	69	Y	N	N
	LD F2,28(R4)	50	66	67	91	92	N	N	Y
	SUB.D F1,F2,F3	66	67	93	95	96	Y	N	N
	DIV.D F4,F2,F3	79	80	93	133	134	Y	N	N
	MUL.D F5,F4,F3	80	81	135	145	146	Y	N	N
	SD F6,32(R2)	81	93	94	119	120	N	N	Y
	DADD R4,R1,R2	93	94	95	96	97	N	N	N
	SW R3,60(R4)	106	121	122	135	136	N	N	Y
	DADDI R3,R3,4	121	122	123	124	125	N	N	N
	BEQ R2, R3, PP	122	123	126			Y	N	N
	HLT	123	127				N	N	N

```
      HLT                         147                                N      N      N

Total number of access requests for instruction cache: 17
Number of instruction cache hits: 12
INSTRUCTION HIT RATIO =12/17
Total number of access requests for data cache: 8
Number of data cache hits: 3
DATA HIT RATIO =3/8
TOTAL CYCLES REQU TO COMPLETE THE WHOLE SET OF INSTRUCTIONS:146
```

```
CONFIG-2:FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache: 4,2
```

Label	Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
	LI R1,8	7	8	9	10	11	N	N	N
	LI R2,312	8	12	13	14	15	N	N	Y
	LI R4,256	15	16	17	18	19	N	N	N
PP	LW R3,0(R4)	16	17	20	35	36	Y	N	N
	LD F1,12(R4)	23	37	38	56	57	N	N	Y
	ADD.D F3,F1,F1	37	38	58	60	61	Y	N	N
	LD F2,28(R4)	44	58	59	77	78	N	N	Y
	SUB.D F1,F2,F3	58	59	79	81	82	Y	N	N
	DIV.D F4,F2,F3	65	66	79	119	120	Y	N	N
	MUL.D F5,F4,F3	66	67	121	131	132	Y	N	N
	SD F6,32(R2)	83	84	85	104	105	N	N	N
	DADD R4,R1,R2	84	85	86	87	88	N	N	N
	SW R3,60(R4)	91	106	107	125	126	N	N	Y
	DADDI R3,R3,4	106	107	108	109	110	N	N	N
	BEQ R2, R3, PP	113	114	115			N	N	N
	HLT	114	116				N	N	N
	HLT	131					N	N	N

```
Total number of access requests for instruction cache: 17
Number of instruction cache hits: 8
INSTRUCTION HIT RATIO =8/17
Total number of access requests for data cache: 8
Number of data cache hits: 3
DATA HIT RATIO =3/8
TOTAL CYCLES REQU TO COMPLETE THE WHOLE SET OF INSTRUCTIONS:132
```

```
CONFIG-3:FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache: 10,10
```

Label	Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
	LI R1,8	31	32	33	34	35	N	N	N
	LI R2,312	32	36	37	38	39	N	N	Y
	LI R4,256	36	40	41	42	43	N	N	Y
PP	LW R3,0(R4)	40	41	44	57	58	Y	N	N
	LD F1,12(R4)	41	59	60	74	75	N	N	Y
	ADD.D F3,F1,F1	59	60	76	78	79	Y	N	N
	LD F2,28(R4)	60	76	77	119	120	N	N	Y
	SUB.D F1,F2,F3	76	77	121	123	124	Y	N	N
	DIV.D F4,F2,F3	107	108	121	161	162	Y	N	N
	MUL.D F5,F4,F3	108	109	163	173	174	Y	N	N

SD F6,32(R2)	109	121	122	136	137	N	N	Y
DADD R4,R1,R2	121	122	123	124	125	N	N	N
SW R3,60(R4)	122	138	139	152	153	N	N	Y
DADDI R3,R3,4	138	139	140	141	142	N	N	N
BEQ R2, R3, PP	139	140	143			Y	N	N
HLT	140	144				N	N	N
HLT	182					N	N	N

Total number of access requests for instruction cache: 17
Number of instruction cache hits: 14
INSTRUCTION HIT RATIO =14/17
Total number of access requests for data cache: 8
Number of data cache hits: 3
DATA HIT RATIO =3/8
TOTAL CYCLES REQU TO COMPLETE THE WHOLE SET OF INSTRUCTIONS:174

CONFIG-4:FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache: 10,1

Label	Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
	LI R1,8	4	5	6	7	8	N	N	N
	LI R2,312	8	9	10	11	12	N	N	N
	LI R4,256	12	13	14	15	16	N	N	N
PP	LW R3,0(R4)	16	17	18	32	33	N	N	N
	LD F1,12(R4)	20	34	35	51	52	N	N	Y
	ADD.D F3,F1,F1	35	36	53	55	56	Y	N	N
	LD F2,28(R4)	39	53	54	70	71	N	N	Y
	SUB.D F1,F2,F3	54	55	72	74	75	Y	N	N
	DIV.D F4,F2,F3	58	59	72	112	113	Y	N	N
	MUL.D F5,F4,F3	73	74	114	124	125	Y	N	N
	SD F6,32(R2)	77	78	79	94	95	N	N	N
	DADD R4,R1,R2	81	82	83	84	85	N	N	N
	SW R3,60(R4)	96	97	98	112	113	N	N	N
	DADDI R3,R3,4	100	101	102	103	104	N	N	N
	BEQ R2, R3, PP	115	116	117			N	N	N
	HLT	119	120				N	N	N
	HLT	123					N	N	N

Total number of access requests for instruction cache: 17
Number of instruction cache hits: 0
INSTRUCTION HIT RATIO =0
Total number of access requests for data cache: 8
Number of data cache hits: 3
DATA HIT RATIO =3/8
TOTAL CYCLES REQU TO COMPLETE THE WHOLE SET OF INSTRUCTIONS:125

CONFIG-5:FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache: 1,0

Label	Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
	LI R1,8	1	2	3	4	5	N	N	N
	LI R2,312	2	6	7	8	9	N	N	Y
	LI R4,256	6	10	11	12	13	N	N	Y
PP	LW R3,0(R4)	10	11	14	27	28	Y	N	N
	LD F1,12(R4)	11	29	30	44	45	N	N	Y
	ADD.D F3,F1,F1	29	30	46	48	49	Y	N	N

LD F2,28(R4)	30	46	47	61	62	N	N	Y
SUB.D F1,F2,F3	46	47	63	65	66	Y	N	N
DIV.D F4,F2,F3	47	48	63	103	104	Y	N	N
MUL.D F5,F4,F3	48	49	105	115	116	Y	N	N
SD F6,32(R2)	49	63	64	78	79	N	N	Y
DADD R4,R1,R2	63	64	65	66	67	N	N	N
SW R3,60(R4)	64	80	81	94	95	N	N	Y
DADDI R3,R3,4	80	81	82	83	84	N	N	N
BEQ R2, R3, PP	81	82	85			Y	N	N
HLT	82	86				N	N	N
HLT	86					N	N	N

Total number of access requests for instruction cache: 17
Number of instruction cache hits: 16
INSTRUCTION HIT RATIO =16/17
Total number of access requests for data cache: 8
Number of data cache hits: 3
DATA HIT RATIO =3/8
TOTAL CYCLES REQU TO COMPLETE THE WHOLE SET OF INSTRUCTIONS:116

FOR FIXED CACHE SIZE AND VARYING BLOCK SIZE

```
 LI R1, 8
 LI R2, 312
 LI R4, 256
PP : LW R3, 0(R4)
 L.D F1, 12(R4)
 ADD.D F3, F1, F1
 L.D F2, 28(R4)
 SUB.D F1, F2, F3
 DIV.D F4, F2, F3
 MUL.D F5, F4, F3
 S.D F6, 32(R2)
 DADD R4, R1, R2
 SW R3, 60(R4)
 DADDI R3, R3, 4
 BEQ R2, R3, PP
 HLT
 HLT
```

```
           LI R1,272
           L.D F0,0(R1)
           ADD.D F4,F0,F2
           S.D F4,0(R1)
           L.D F6,8(R1)
           ADD.D F8,F6,F2
           S.D F8,8(R1)
           L.D F10,16(R1)
           ADD.D F12,F10,F2
           S.D F12,16(R1)
           L.D F14,24(R1)
           ADD.D F16,F14,F2
```

```
          S.D F16,24(R1)
          DADDI R1,R1,32
     HLT
     HLT
               LI R1,272
          L.D F0,0(R1)
          L.D F6,-8(R1)
          L.D F10, -16(R1)
          L.D F14,-24(R1)
          ADD.D F4,F0,F2
          ADD.D F8,F6,F2
          ADD.D F12,F10,F2
          ADD.D F16,F14,F2
          S.D F4,0(R1)
          S.D F8,-8(R1)
          DADDI R1,R1,32
          S.D F12,16(R1)
          S.D F16,8(R1)
          HLT
          HLT
      LI R2,272
 LI R3,300
 L.D F6,34(R2)
 L.D F2,45(R3)
 MUL.D F0,F2,F4
 SUB.D  F8,F6,F2
 DIV.D  F10,F0,F6
 ADD.D  F6,F8,F2
 LI R4, 260
 LI R5, 272
 LI R1, 8
 LI R2, 4
 LI R3, 0
GG: L.D F1, 4(R4)
 L.D F2, 8(R5)
 ADD.D F4, F6, F2
 SUB.D F5, F7, F1
 MUL.D F6, F1, F5
 ADD.D F7, F2, F6
 ADD.D F6, F1, F7
 DADDI R4, R4, 20
 DADDI R5, R5, 8
 DSUB R1, R1, R2
 BNE R1, R3, GG
 HLT
 HLT
```

```
FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache:1,20

Total number of access requests for instruction cache: 88
Number of instruction cache hits: 81
Total number of access requests for data cache: 52
Number of data cache hits: 40


FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache:20,1


Total number of access requests for instruction cache: 87
Number of instruction cache hits: 12
Total number of access requests for data cache: 52
Number of data cache hits: 40

FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache: 4,5

Total number of access requests for instruction cache: 88
Number of instruction cache hits: 69
Total number of access requests for data cache: 52
Number of data cache hits: 40

FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache: 5,4

Total number of access requests for instruction cache: 88
Number of instruction cache hits: 69
Total number of access requests for data cache: 52
Number of data cache hits: 40

FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache: 10,2

Total number of access requests for instruction cache: 88
```

```
Number of instruction cache hits: 50
Total number of access requests for data cache: 52
Number of data cache hits: 40


FP adder: 2, 2
FP Multiplier: 2, 10
FP divider: 1, 40
I-Cache: 2,10

Total number of access requests for instruction cache: 88
Number of instruction cache hits: 76
Total number of access requests for data cache: 52
Number of data cache hits: 40
```