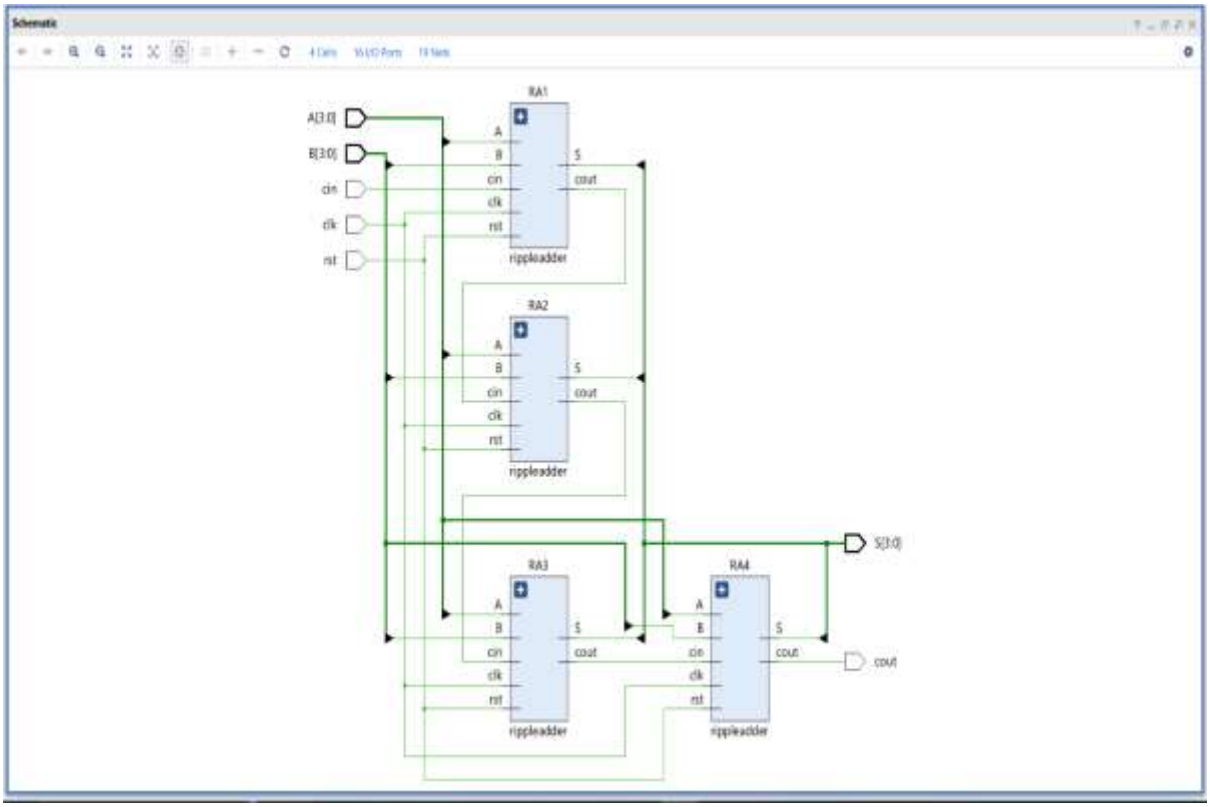
2) 4-bit adder with pipeline registers

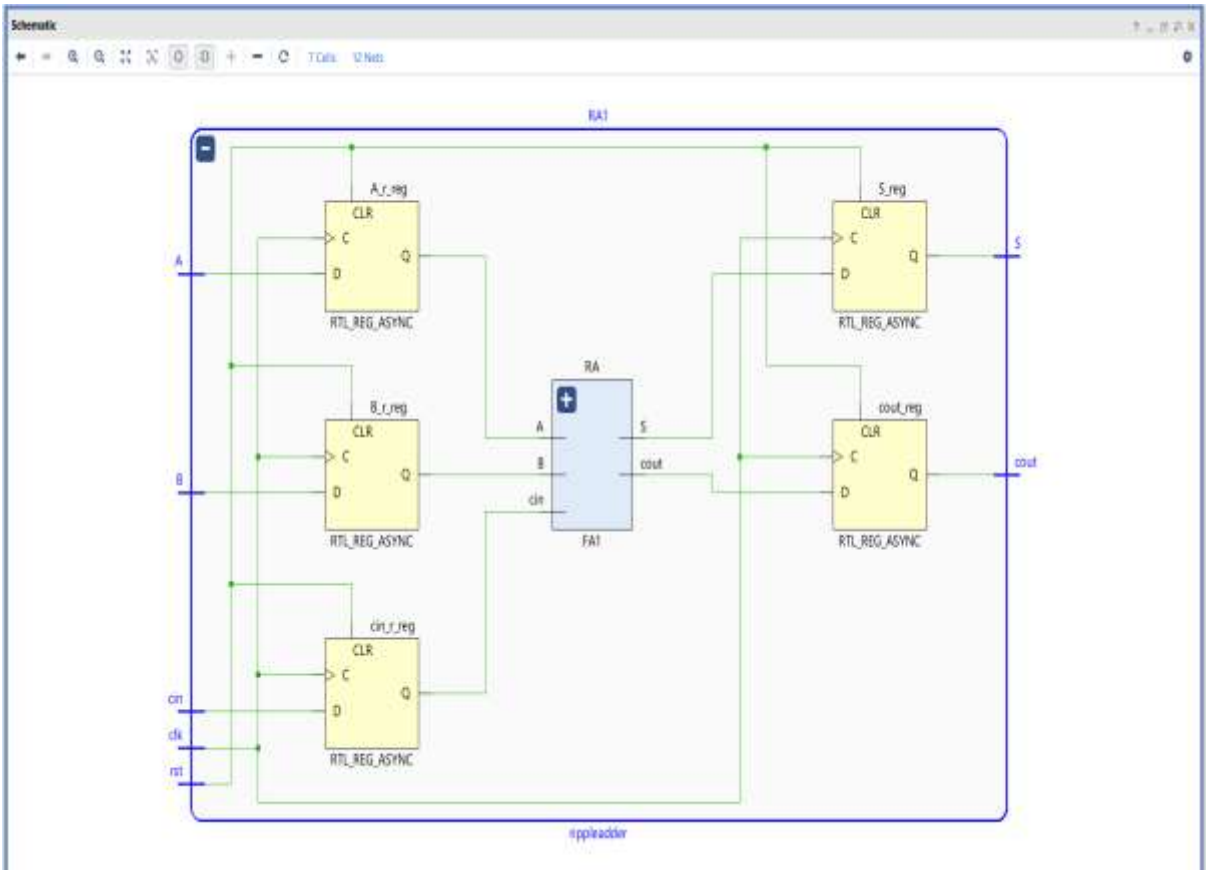
```
22
23  module ripple_adder_4bit(
24      input [3:0]A,
25      input [3:0]B,
26      input cin,
27      input clk,
28      input rst,
29      output [3:0] S,
30      output cout
31      );
32      wire c0,c1,c2,c3;
33      rippleadder RA1 (.A(A[0]),.B(B[0]),.cin(cin),.clk(clk),.rst(rst),.S(S[0]),.cout(c0));
34      rippleadder RA2 (.A(A[1]),.B(B[1]),.cin(c0),.clk(clk),.rst(rst),.S(S[1]),.cout(c1));
35      rippleadder RA3 (.A(A[2]),.B(B[2]),.clk(clk),.rst(rst),.cin(c1),.S(S[2]),.cout(c2));
36      rippleadder RA4 (.A(A[3]),.B(B[3]),.clk(clk),.rst(rst),.cin(c2),.S(S[3]),.cout(c3));
37
38      assign cout = c3;
39  endmodule
```

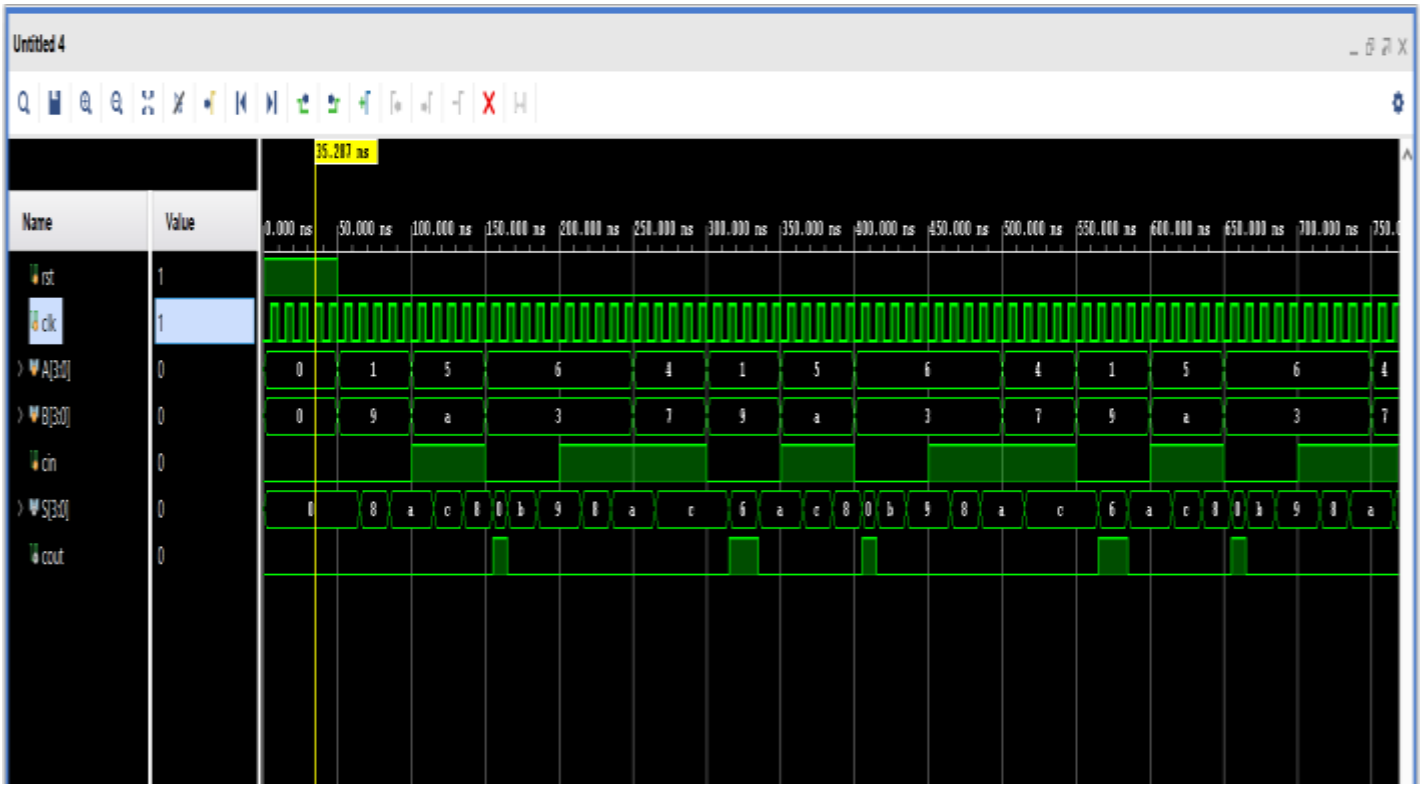
rippleadder.v

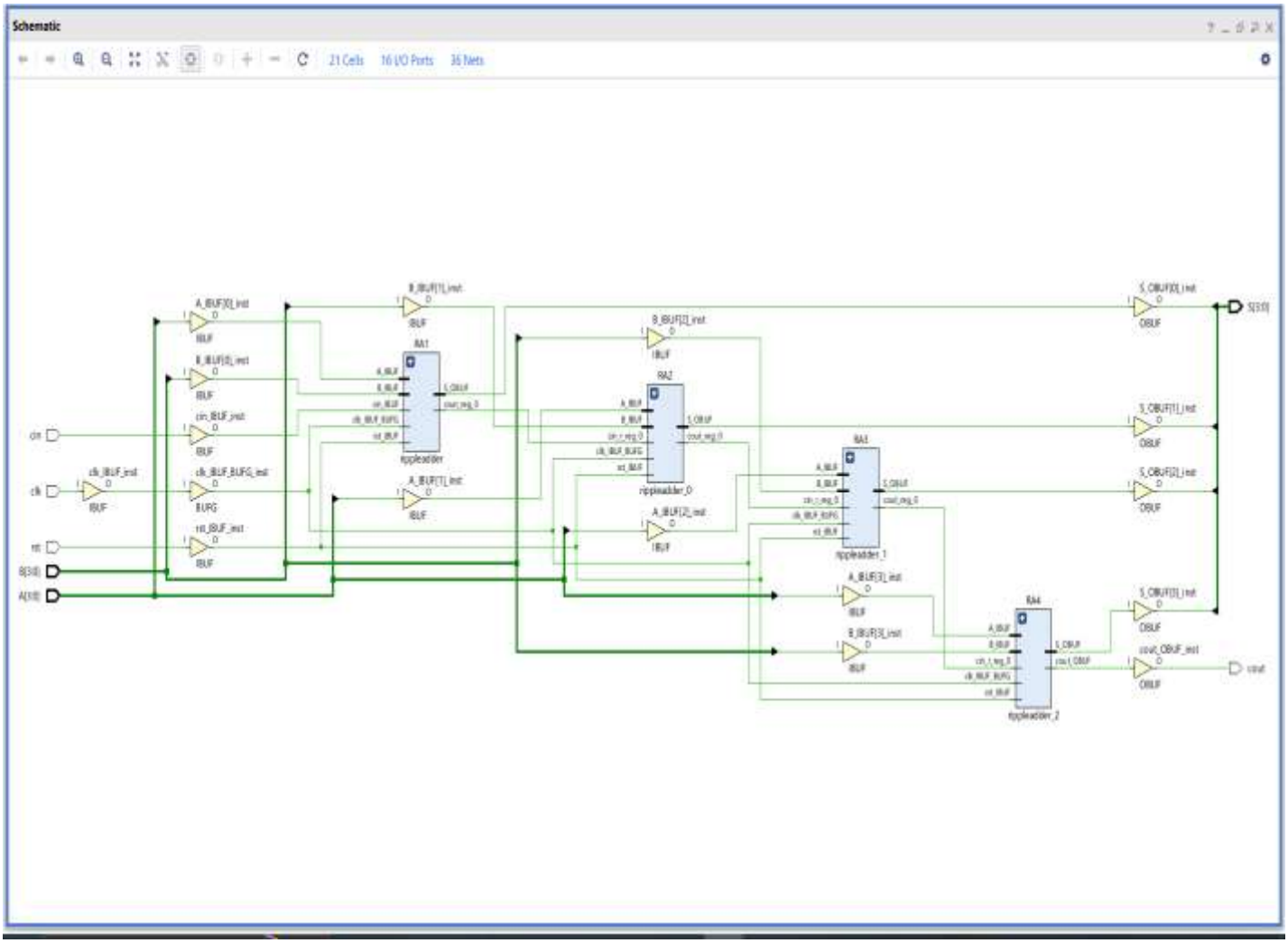
C:/Users/Bhanuprakash/4bitrippleadder/4bitrippleadder.srcs/sources_1/new/rippleadder.v

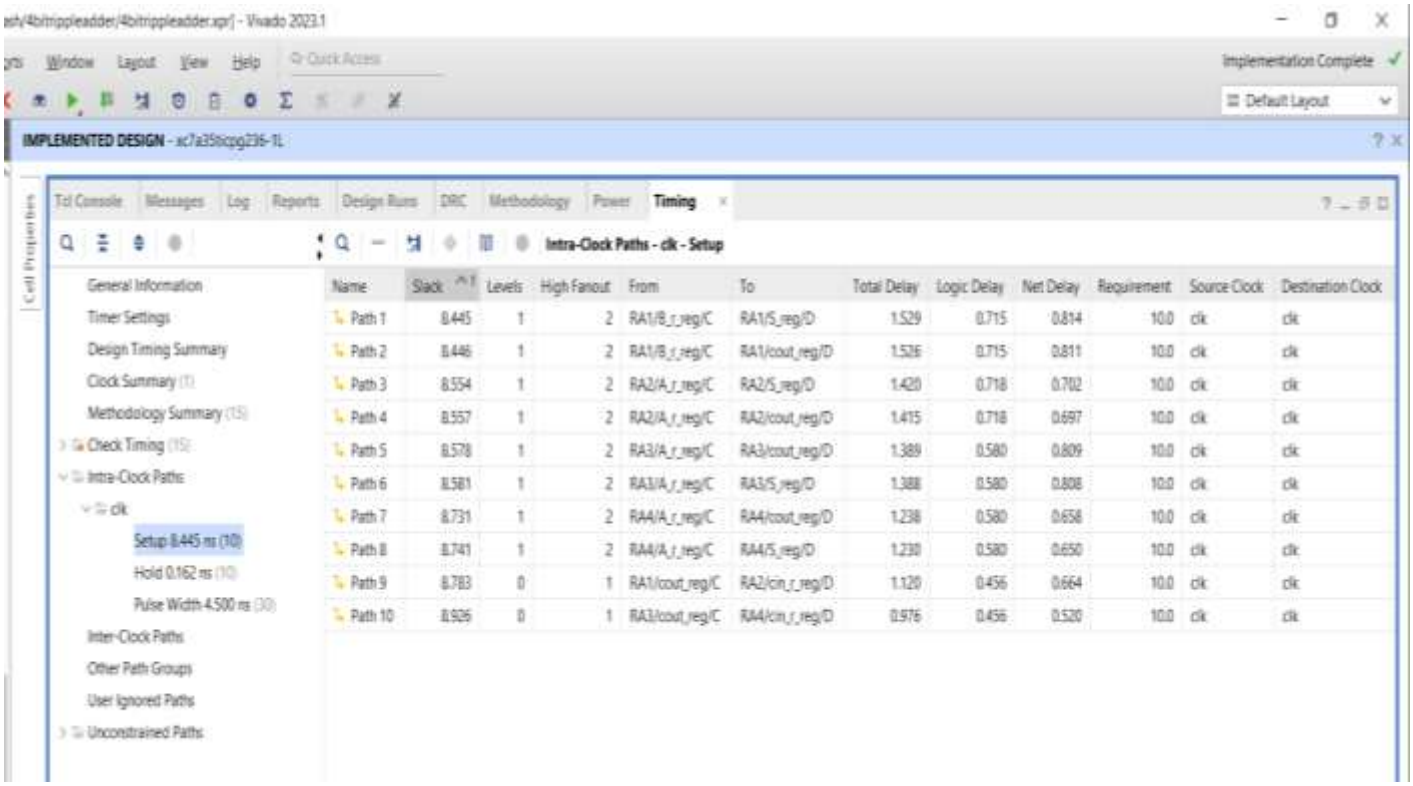
```
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21
22
23  module rippleadder(
24      input A,
25      input B,
26      input cin,
27      input clk,
28      input rst,
29      output reg S,
30      output reg cout
31      );
32      wire S_f,cout_f;
33      reg A_r,B_r,cin_r;
34     FA1 RA (.A(A_r),.B(B_r),.cin(cin_r),.S(S_f),.cout(cout_f));
35
36      always @(posedge clk,posedge rst)
37       begin
38       if(rst)
39          begin
40            A_r <= 1'b0;
41            B_r <= 1'b0;
42            cin_r <=1'b0;
43            S<=0;
44           cout<=0;
45          end
46        else
47          begin
48            A_r <= A;
49            B_r <= B;
50            cin_r <= cin;
51            S<=S_f;
52            cout<=cout_f;
53           end
54       end
55  endmodule
56
```

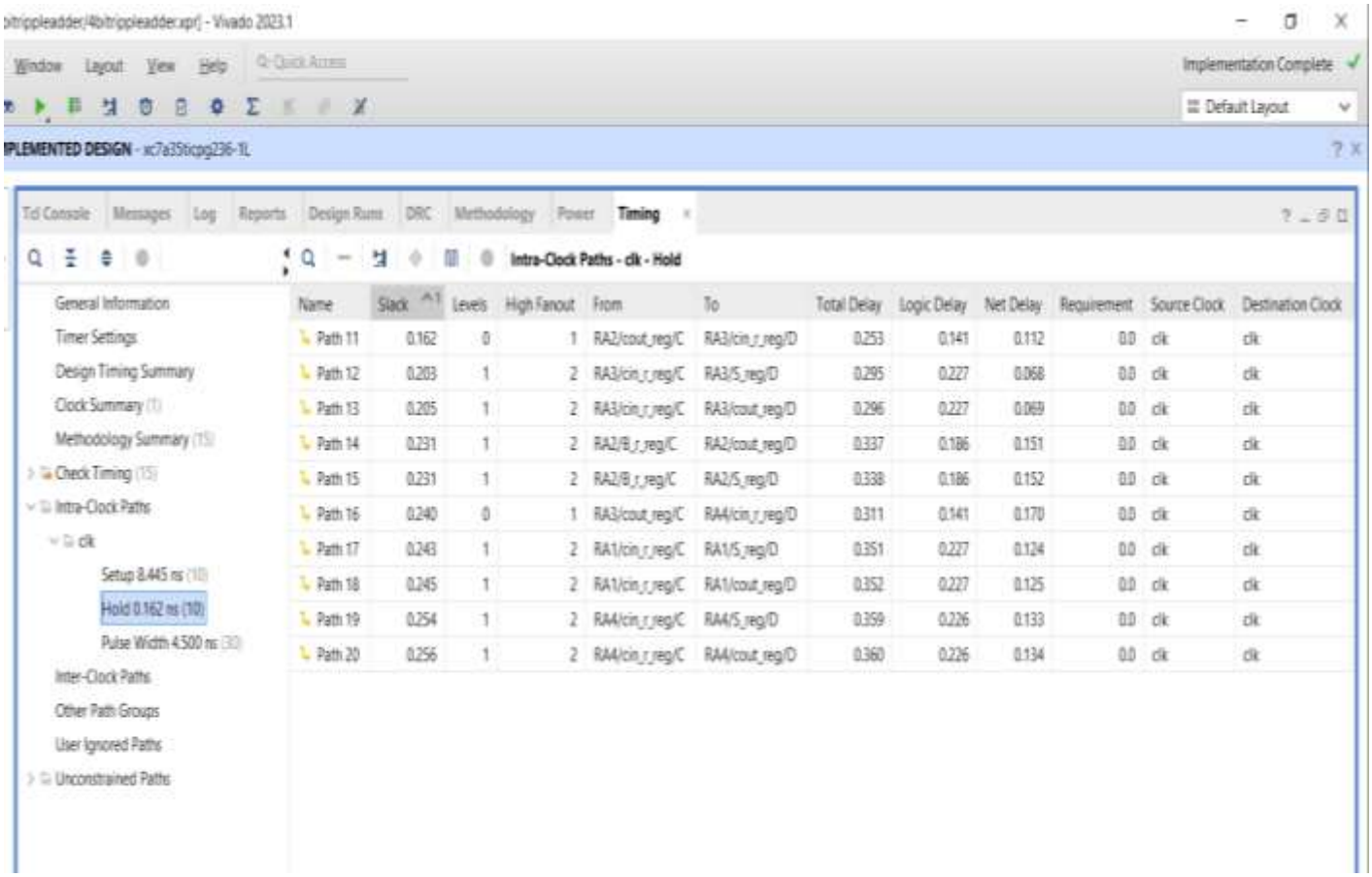

Schematic
RA1
A[3:0]
B[3:0]
cin
clk
rst
A
B
cin
clk
rst
S
cout
rippleadder
RA2
RA3
RA4
S[3:0]
cout


Schematic
RA1
A_r_reg
B_r_reg
cin_r_reg
S_reg
cout_reg
CLR
C
D
Q
RTL_REG_ASYNC
RA
A
B
cin
S
cout
FA1
A
B
cin
clk
rst
S
cout
rippleadder


Untitled 4
35.207 ns
Name
Value
rst
clk
A[3:0]
B[3:0]
cin
S[3:0]
cout


Schematic
21 Cells
16 I/O Ports
36 Nets


Implementation Complete
Default Layout
IMPLEMENTED DESIGN - xc7a35ticpg236-1L
Tcl Console | Messages | Log | Reports | Design Runs | DRC | Methodology | Power | Timing
Intra-Clock Paths - clk - Setup
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Methodology Summary (15)
Check Timing (15)
Intra-Clock Paths
clk
Setup 8.445 ns (10)
Hold 0.162 ns (10)
Pulse Width 4.500 ns (30)
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
Name | Slack | Levels | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock | Destination Clock
Path 1 | 8.445 | 1 | 2 | RA1/B_r_reg/C | RA1/S_reg/D | 1.529 | 0.715 | 0.814 | 10.0 | clk | clk
Path 2 | 8.446 | 1 | 2 | RA1/B_r_reg/C | RA1/cout_reg/D | 1.526 | 0.715 | 0.811 | 10.0 | clk | clk
Path 3 | 8.554 | 1 | 2 | RA2/A_r_reg/C | RA2/S_reg/D | 1.420 | 0.718 | 0.702 | 10.0 | clk | clk
Path 4 | 8.557 | 1 | 2 | RA2/A_r_reg/C | RA2/cout_reg/D | 1.415 | 0.718 | 0.697 | 10.0 | clk | clk
Path 5 | 8.578 | 1 | 2 | RA3/A_r_reg/C | RA3/cout_reg/D | 1.389 | 0.580 | 0.809 | 10.0 | clk | clk
Path 6 | 8.581 | 1 | 2 | RA3/A_r_reg/C | RA3/S_reg/D | 1.388 | 0.580 | 0.808 | 10.0 | clk | clk
Path 7 | 8.731 | 1 | 2 | RA4/A_r_reg/C | RA4/cout_reg/D | 1.238 | 0.580 | 0.658 | 10.0 | clk | clk
Path 8 | 8.741 | 1 | 2 | RA4/A_r_reg/C | RA4/S_reg/D | 1.230 | 0.580 | 0.650 | 10.0 | clk | clk
Path 9 | 8.783 | 0 | 1 | RA1/cout_reg/C | RA2/cin_r_reg/D | 1.120 | 0.456 | 0.664 | 10.0 | clk | clk
Path 10 | 8.926 | 0 | 1 | RA3/cout_reg/C | RA4/cin_r_reg/D | 0.976 | 0.456 | 0.520 | 10.0 | clk | clk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Setup 8.445 ns (10)
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Pulse Width 4.500 ns (30)
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
Name | Slack | Levels | High Fanout | From | To | Total Delay | Logic Delay | Net Delay | Requirement | Source Clock | Destination Clock
Path 11 | 0.162 | 0 | 1 | RA2/cout_reg/C | RA3/cin_r_reg/D | 0.253 | 0.141 | 0.112 | 0.0 | clk | clk
Path 12 | 0.203 | 1 | 2 | RA3/cin_r_reg/C | RA3/S_reg/D | 0.295 | 0.227 | 0.068 | 0.0 | clk | clk
Path 13 | 0.205 | 1 | 2 | RA3/cin_r_reg/C | RA3/cout_reg/D | 0.296 | 0.227 | 0.069 | 0.0 | clk | clk
Path 14 | 0.231 | 1 | 2 | RA2/B_r_reg/C | RA2/cout_reg/D | 0.337 | 0.186 | 0.151 | 0.0 | clk | clk
Path 15 | 0.231 | 1 | 2 | RA2/B_r_reg/C | RA2/S_reg/D | 0.338 | 0.186 | 0.152 | 0.0 | clk | clk
Path 16 | 0.240 | 0 | 1 | RA3/cout_reg/C | RA4/cin_r_reg/D | 0.311 | 0.141 | 0.170 | 0.0 | clk | clk
Path 17 | 0.243 | 1 | 2 | RA1/cin_r_reg/C | RA1/S_reg/D | 0.351 | 0.227 | 0.124 | 0.0 | clk | clk
Path 18 | 0.245 | 1 | 2 | RA1/cin_r_reg/C | RA1/cout_reg/D | 0.352 | 0.227 | 0.125 | 0.0 | clk | clk
Path 19 | 0.254 | 1 | 2 | RA4/cin_r_reg/C | RA4/S_reg/D | 0.359 | 0.226 | 0.133 | 0.0 | clk | clk
Path 20 | 0.256 | 1 | 2 | RA4/cin_r_reg/C | RA4/cout_reg/D | 0.360 | 0.226 | 0.134 | 0.0 | clk | clk