

## 1) 4-bit adder with pipeline registers only at the input and outputs of the 4-bit adder.

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pipelined_rippleadder.v

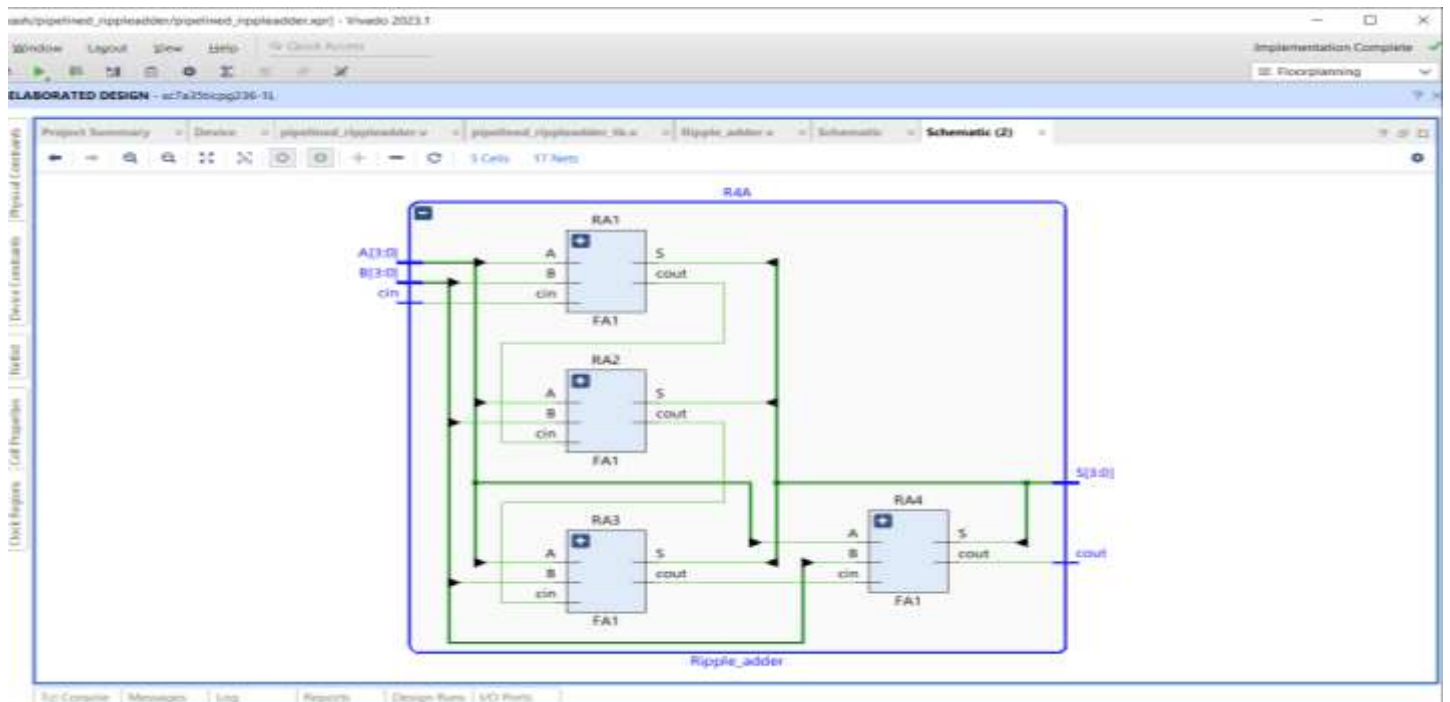
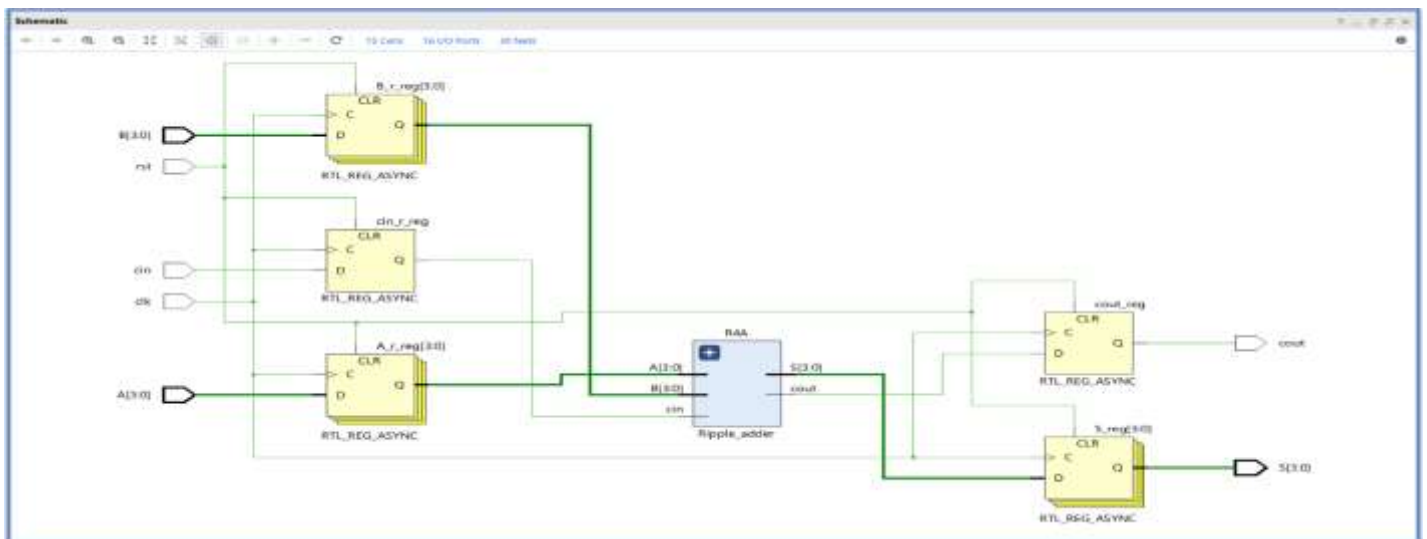
C:/Users/Bhanuprakash/pipelined_rippleadder/pipelined_rippleadder.srscs/sources_1/new/pipelined_rippleadder.v

19 //
20 //////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
21
22
23 module pipelined_rippleadder(
24     input [3:0]A,
25     input [3:0]B,
26     input cin,
27     input clk,
28     input rst,
29     output reg [3:0] S,
30     output reg cout,
31 );
32     wire [3:0] s_f;
33     wire cout_f;
34     reg [3:0]A_r,B_r;
35     reg cin_r;
36     Ripple_adder R4A (.A(A_r),.B(B_r),.cin(cin_r),.S(s_f),.cout(cout_f));
37
38     always @(posedge clk,posedge rst)
39     begin
40         if(rst)
41         begin
42             A_r <= 4'b0000;
43             B_r <= 4'b0000;
44             cin_r <= 1'b0;
45             S<=4'b0000;
46             cout<=0;
47         end
48         else
49         begin
50             A_r <= A;
51             B_r <= B;
52             cin_r <= cin;
53             S<=s_f;
54             cout<=cout_f;
55         end
56     end
57 endmodule
58
59
```

```

21
22
23 module Ripple_adder{
24     input [3:0]A,
25     input [3:0]B,
26     input cin,
27     output [3:0] S,
28     output cout
29 };
30 wire c0,c1,c2,c3;
31 FA1 RA1 (.A(A[0]),.B(B[0]),.cin(cin),.S(S[0]),.cout(c0));
32 FA1 RA2 (.A(A[1]),.B(B[1]),.cin(c0),.S(S[1]),.cout(c1));
33 FA1 RA3 (.A(A[2]),.B(B[2]),.cin(c1),.S(S[2]),.cout(c2));
34 FA1 RA4 (.A(A[3]),.B(B[3]),.cin(c2),.S(S[3]),.cout(c3));
35
36 assign cout = c3;
37 endmodule
38

```





IMPLEMENTS DESIGN - xc7a250tccg236-1L													
Timing													
Intra-Clock Paths - clk - Setup													
General Information	Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Excep
Timer Settings	Path 1	7.190	1	2	B_r_reg[1]/C	S_reg[1]/D	2.515	0.688	1.907	10.0	clk	clk	
Design Timing Summary	Path 2	7.507	2	3	B_r_reg[1]/C	S_reg[2]/D	2.465	0.704	1.761	10.0	clk	clk	
Clock Summary (1)	Path 3	7.517	2	3	B_r_reg[1]/C	S_reg[3]/D	2.457	0.704	1.753	10.0	clk	clk	
Methodology Summary (15)	Path 4	7.531	2	3	B_r_reg[1]/C	cout_reg/D	2.485	0.732	1.753	10.0	clk	clk	
Check Timing (15)	Path 5	8.554	1	3	A_r_reg[0]/C	S_reg[3]/D	1.420	0.718	0.702	10.0	clk	clk	
Intra-Clock Paths													
clk													

IMPLEMENTS DESIGN - xc7a250tccg236-1L													
Timing													
Intra-Clock Paths - clk - Hold													
General Information	Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Excep
Timer Settings	Path 6	0.234	1	3	cin_r_reg/C	S_reg[0]/D	0.326	0.226	0.100	0.0	clk	clk	
Design Timing Summary	Path 7	0.238	1	3	B_r_reg[2]/C	cout_reg/D	0.345	0.230	0.115	0.0	clk	clk	
Clock Summary (1)	Path 8	0.249	1	3	B_r_reg[2]/C	S_reg[3]/D	0.341	0.226	0.115	0.0	clk	clk	
Methodology Summary (15)	Path 9	0.249	1	3	B_r_reg[2]/C	S_reg[2]/D	0.340	0.226	0.114	0.0	clk	clk	
Check Timing (15)	Path 10	0.652	1	3	cin_r_reg/C	S_reg[1]/D	0.662	0.229	0.433	0.0	clk	clk	
Intra-Clock Paths													
clk													

The most critical path in this method is B\_r\_reg[1]/C to S\_reg[1]/D and the slack is 7.190ns