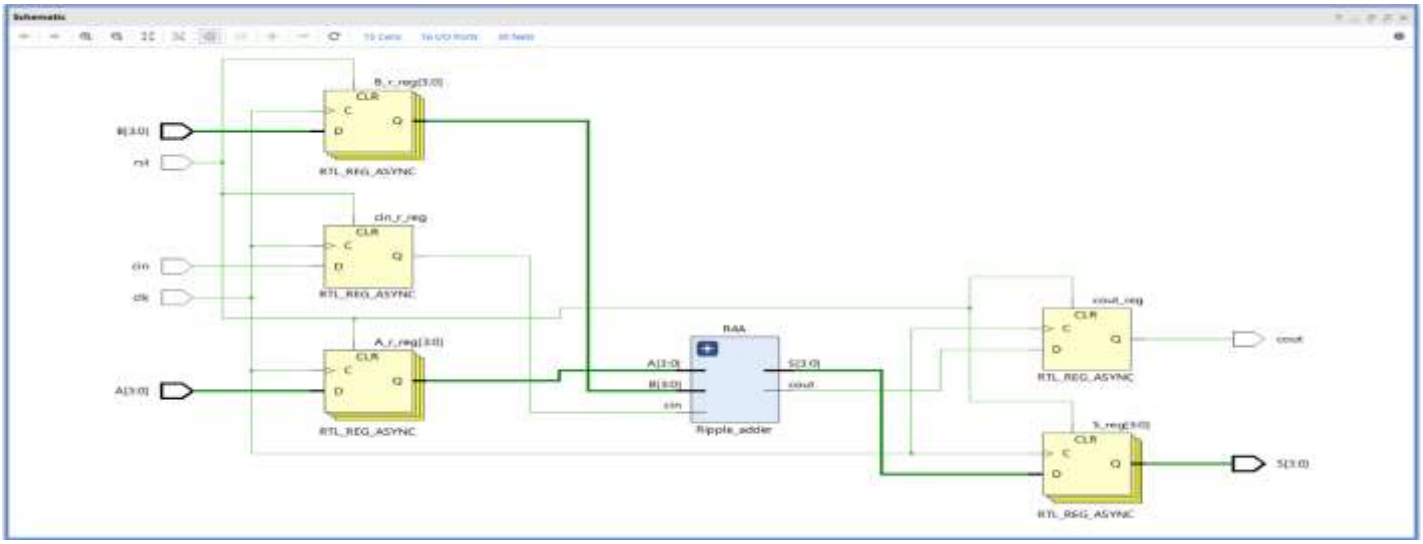
1) 4-bit adder with pipeline registers only at the input and outputs of the 4-bit adder.

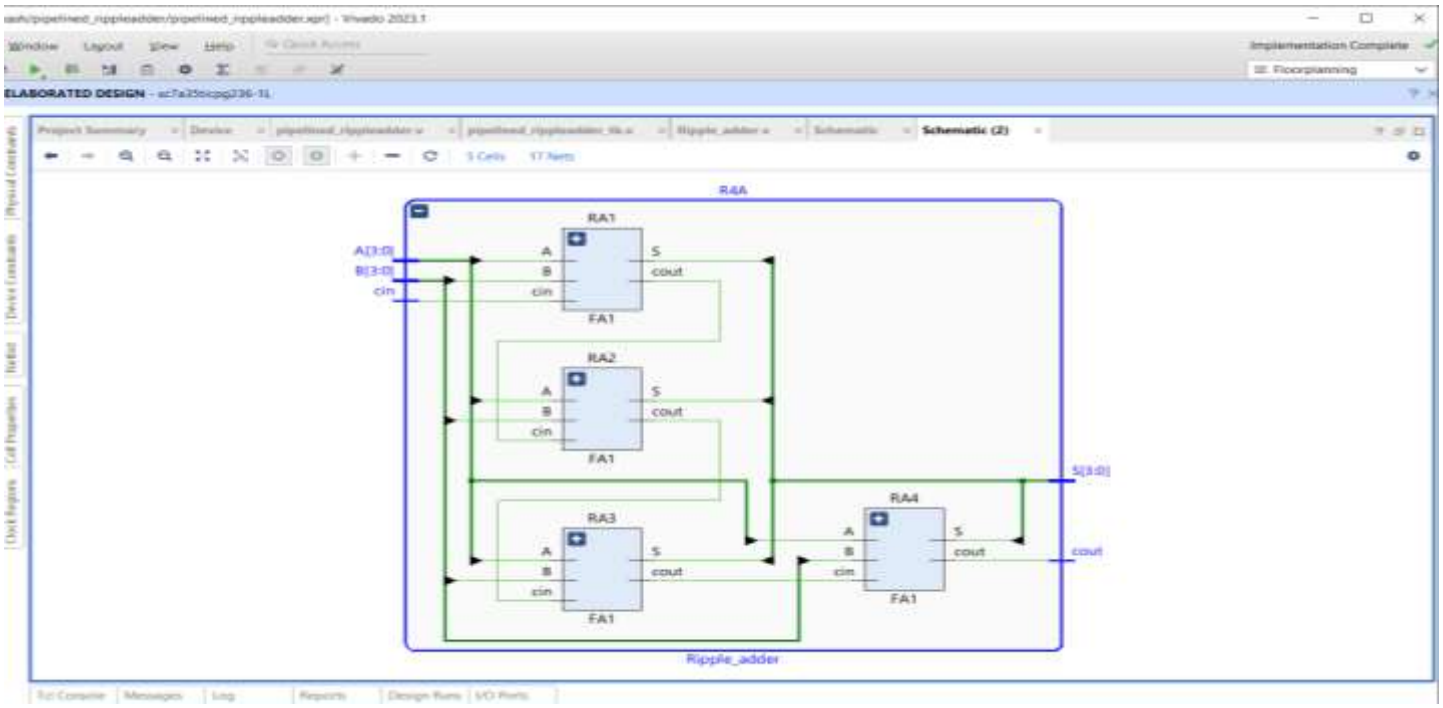
pipelined_rippleadder.v

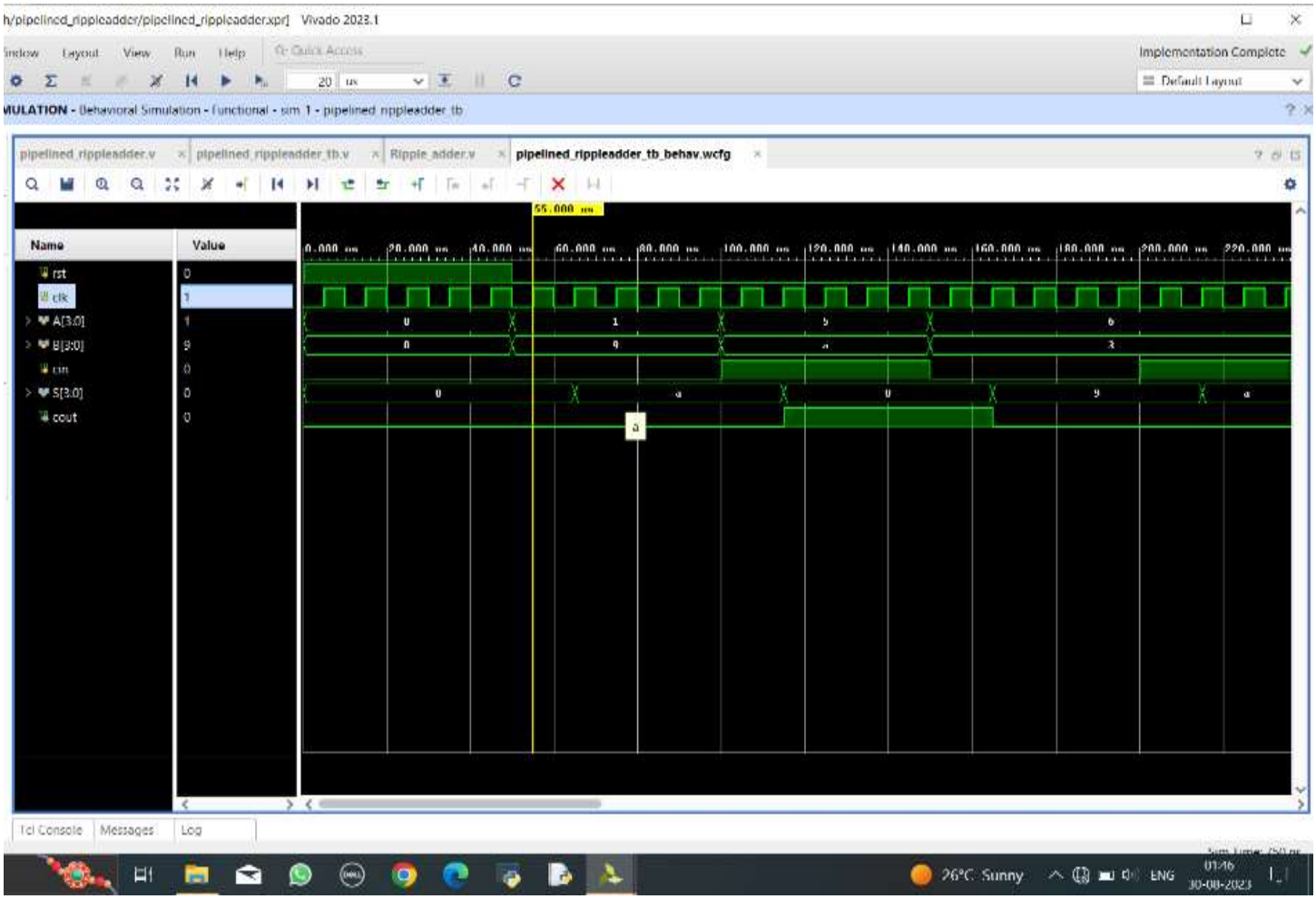
C:/Users/Bhanuprakash/pipelined_rippleadder/pipelined_rippleadder.srcs/sources_1/new/pipelined_rippleadder.v

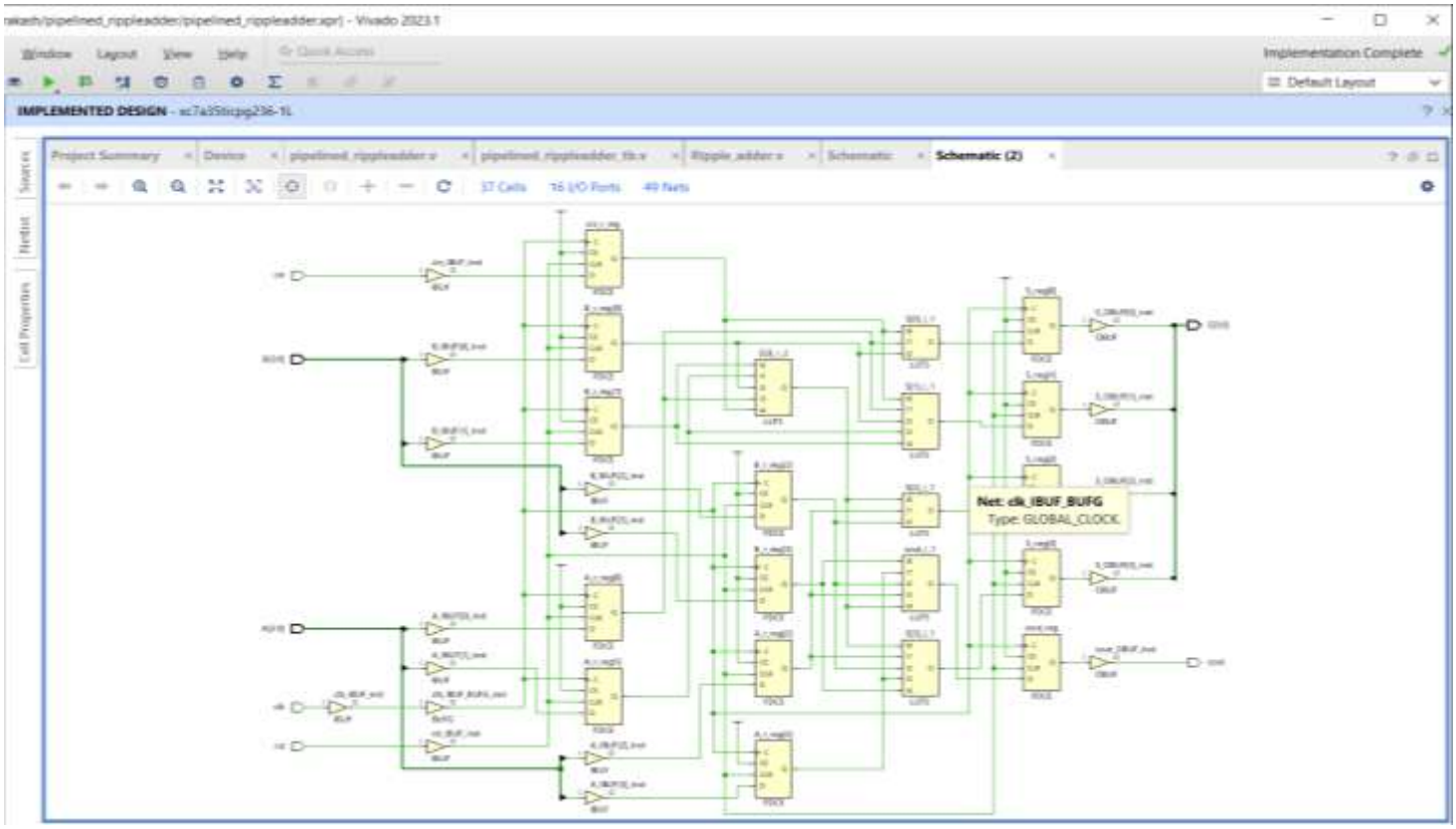
```
19      //
20      //////////////////////////////////////////////////////////////////////////////////
21
22
23      module pipelined_rippleadder(
24          input [3:0]A,
25          input [3:0]B,
26          input cin,
27          input clk,
28          input rst,
29          output reg [3:0] S,
30          output reg cout
31      );
32          wire [3:0] S_f;
33          wire cout_f;
34          reg [3:0]A_r,B_r;
35          reg cin_r;
36         Ripple_adder R4A (.A(A_r),.B(B_r),.cin(cin_r),.S(S_f),.cout(cout_f));
37
38          always @(posedge clk,posedge rst)
39           begin
40           if(rst)
41              begin
42                A_r <= 4'b0000;
43                B_r <= 4'b0000;
44                cin_r <=1'b0;
45                S<=4'b0000;
46               cout<=0;
47              end
48            else
49              begin
50                A_r <= A;
51                B_r <= B;
52                cin_r <= cin;
53                S<=S_f;
54                cout<=cout_f;
55               end
56           end
57      endmodule
58
59
```

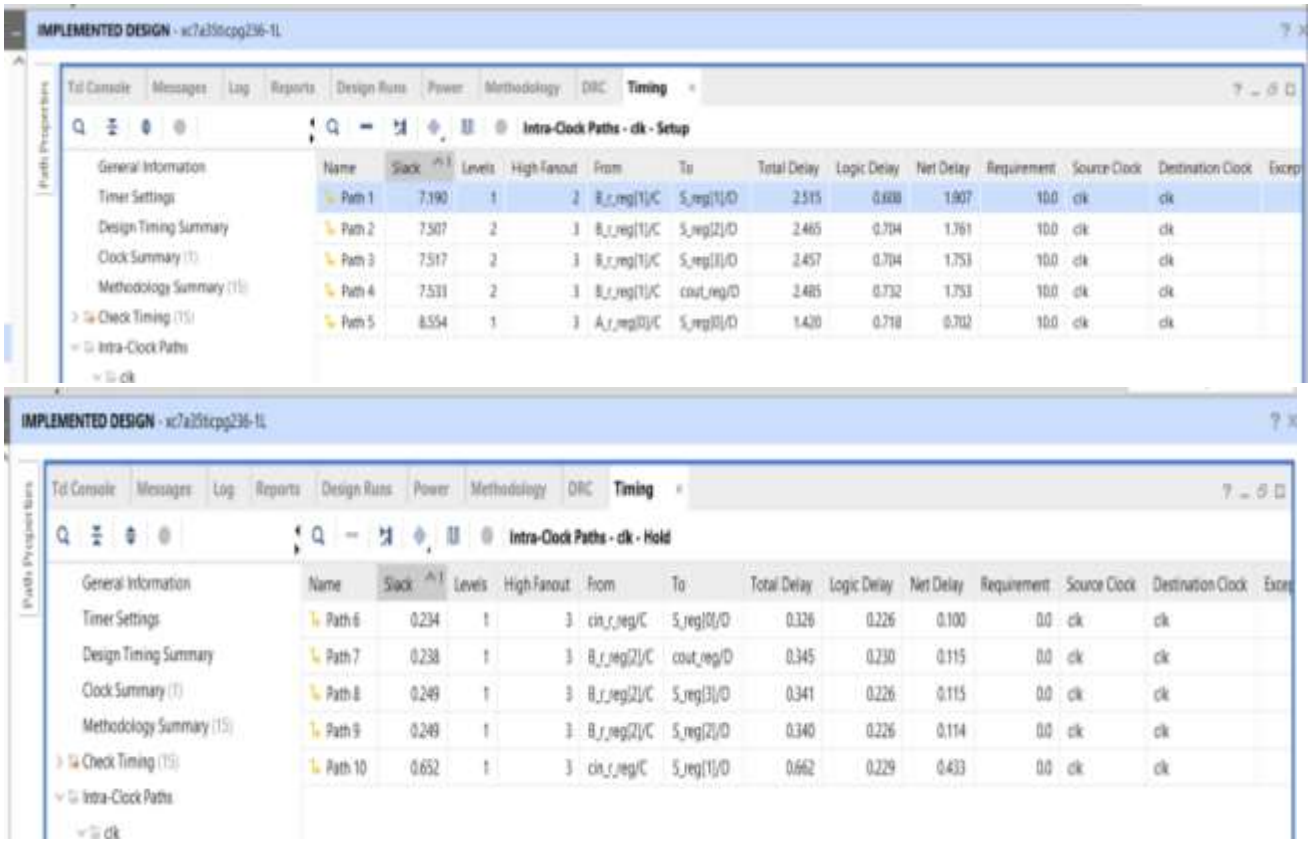
```
21
22
23  module Ripple_adder(
24      input [3:0]A,
25      input [3:0]B,
26      input cin,
27      output [3:0] S,
28      output cout
29      );
30      wire c0,c1,c2,c3;
31     FA1 RA1 (.A(A[0]),.B(B[0]),.cin(cin),.S(S[0]),.cout(c0));
32     FA1 RA2 (.A(A[1]),.B(B[1]),.cin(c0),.S(S[1]),.cout(c1));
33     FA1 RA3 (.A(A[2]),.B(B[2]),.cin(c1),.S(S[2]),.cout(c2));
34     FA1 RA4 (.A(A[3]),.B(B[3]),.cin(c2),.S(S[3]),.cout(c3));
35
36  0   assign cout = c3;
37  endmodule
38
```






Vivado 2023.1
Implementation Complete
Behavioral Simulation - Functional - sim 1 - pipelined_rippleadder_tb
pipelined_rippleadder_tb_behav.wcfg
Name
Value
rst
clk
A[3:0]
B[3:0]
cin
S[3:0]
cout
55.000 ns
Tcl Console
Messages
Log
26°C Sunny
ENG
30-08-2023


IMPLEMENTED DESIGN
Schematic (2)
Net: clk_IBUF_BUFG
Type: GLOBAL_CLOCK



The most critical path in this method is B_r_reg[1]/C to S_reg[1]/D and the slack is 7.190ns