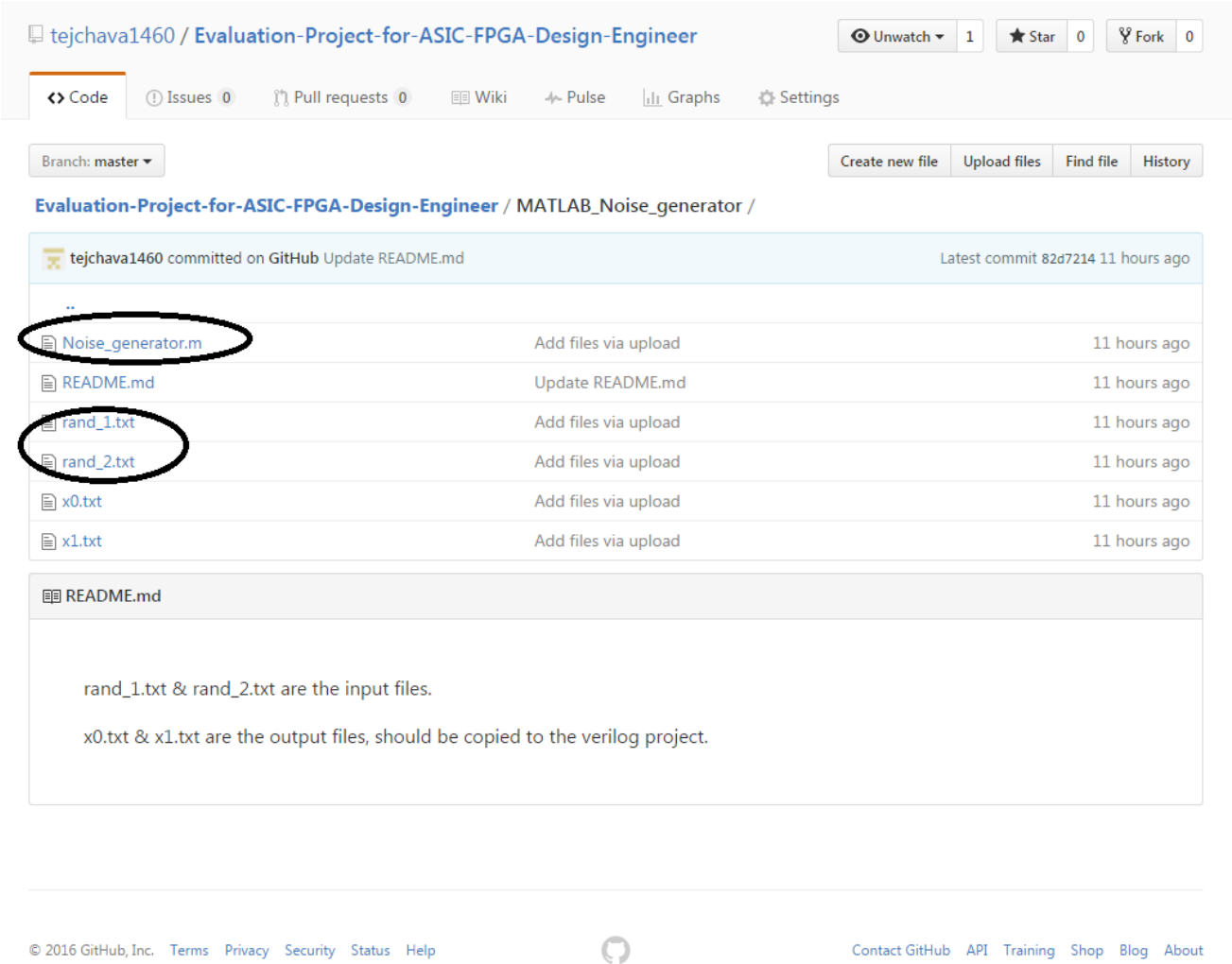
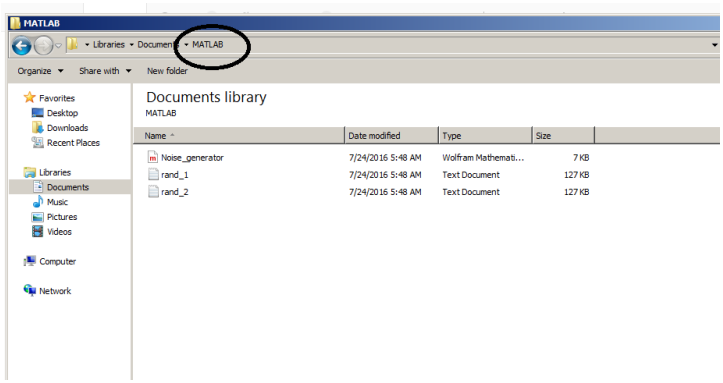
Follow the below steps in order to do the simulation:

a) Simulation steps for the Pre-defined urng_seed.
b) Simulation steps for the custom urng_seed.

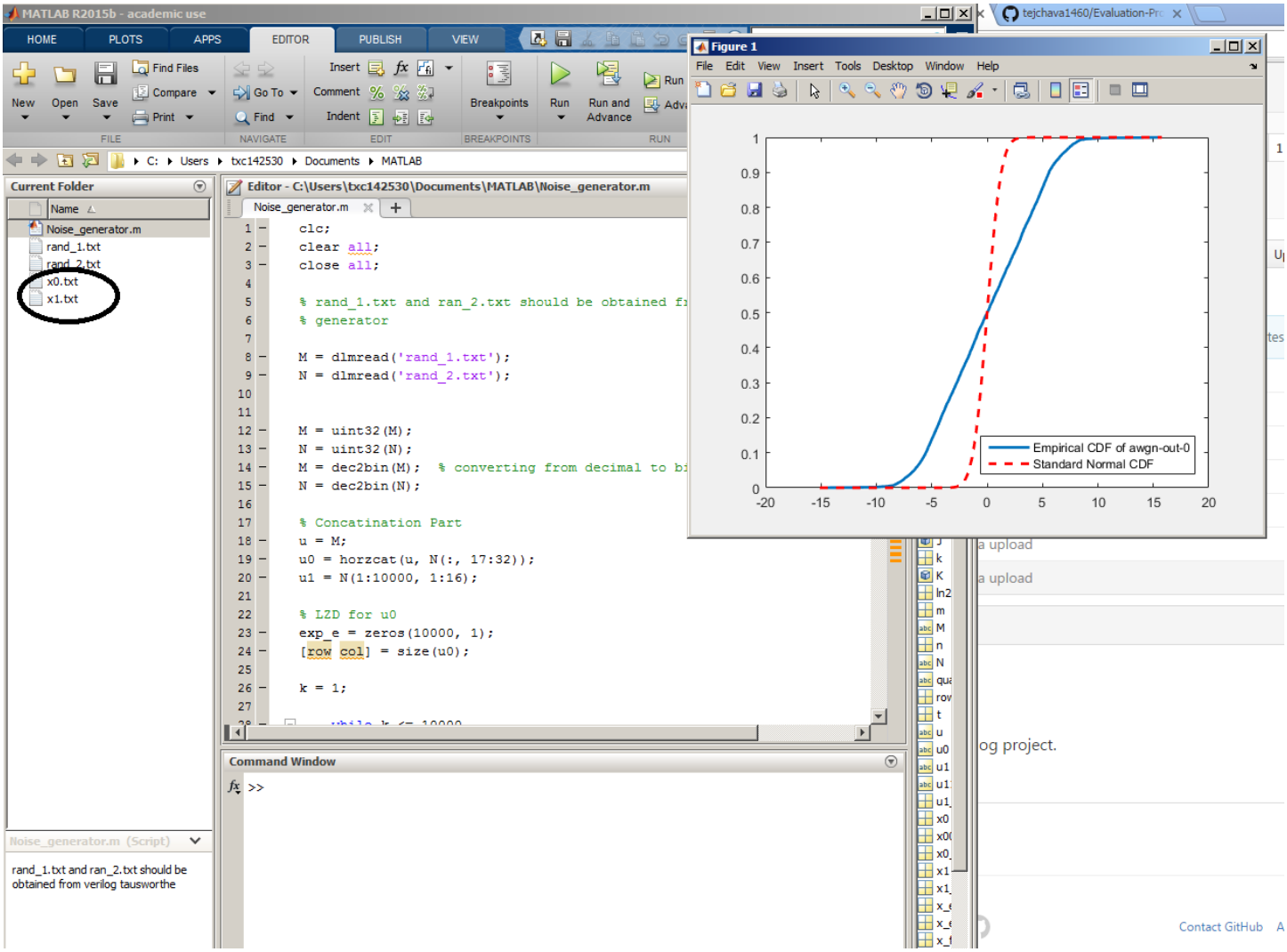
a) Simulation steps for the Pre-defined urng_seed:

i) Copy all the highlighted files into the MATLAB directory. It gives **'x0.txt' & 'x1.txt'.**



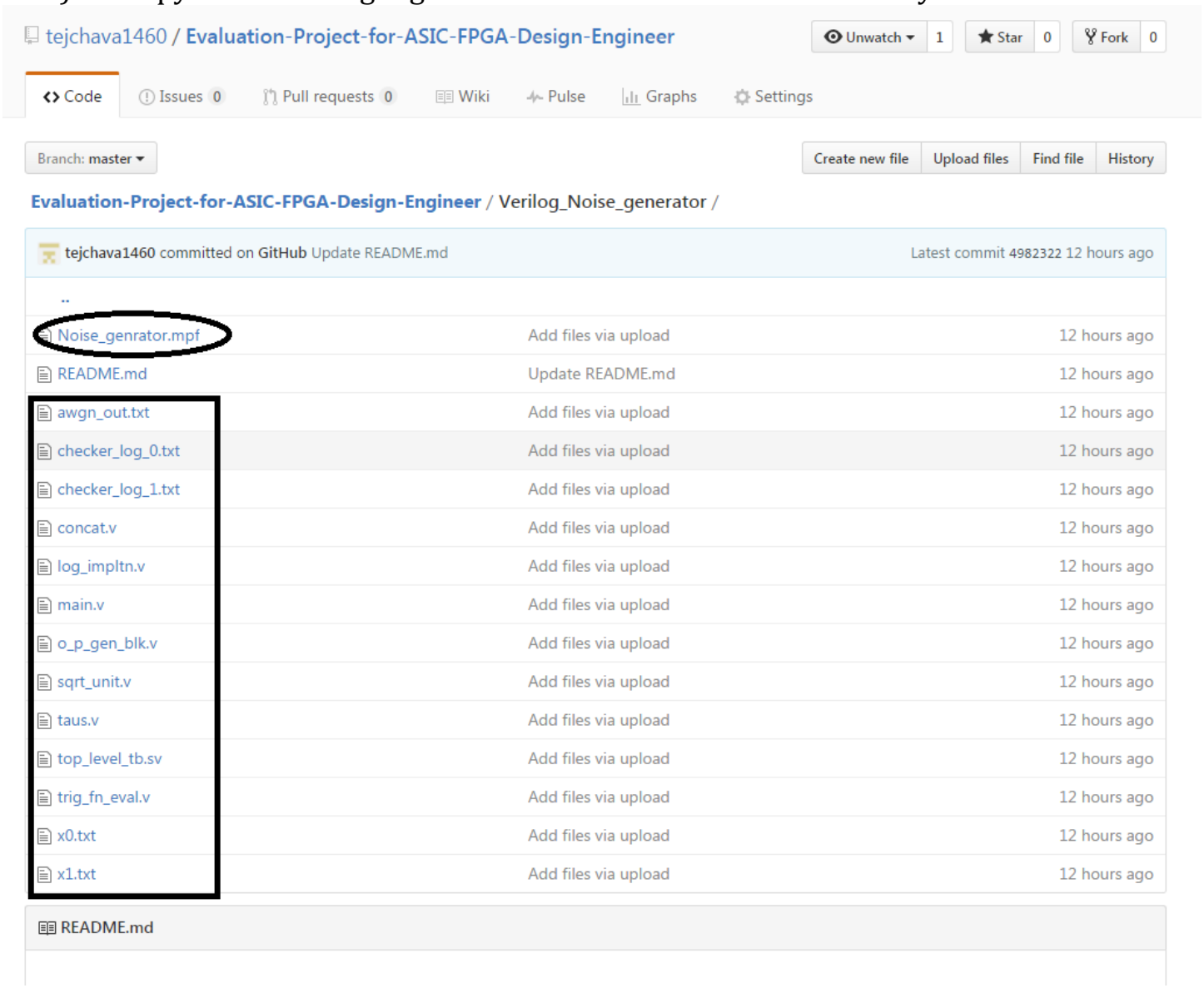


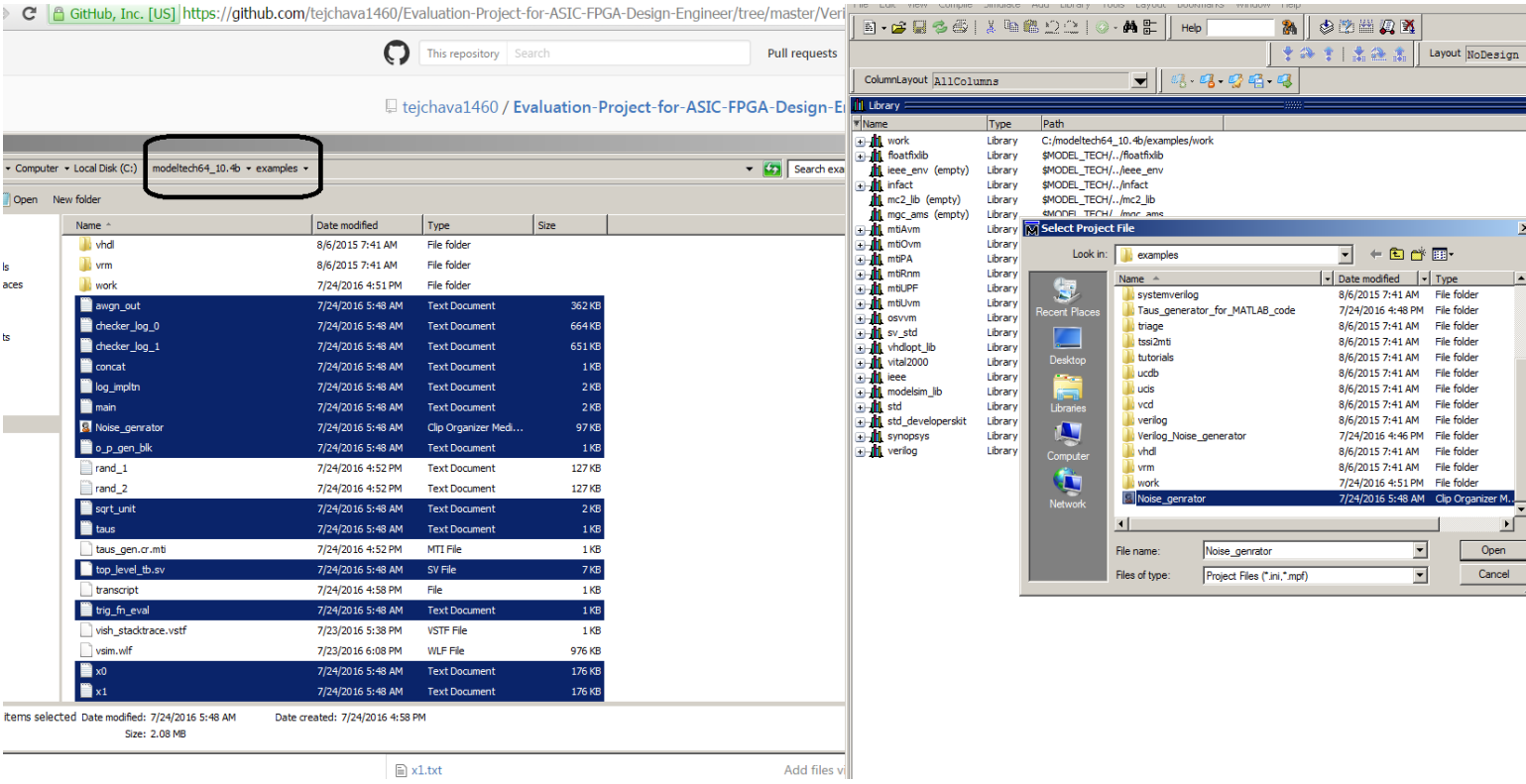
Result follows as



Copy the above **'x0.txt' & 'x1.txt'** into the **Verilog Noise generator** Project.

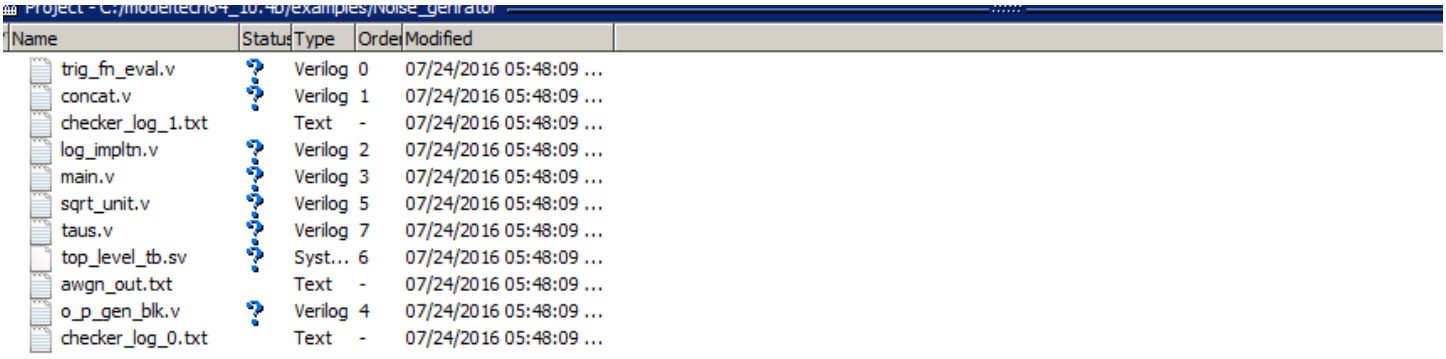
ii) Copy the below highlighted files into the **Modelsim** directory.

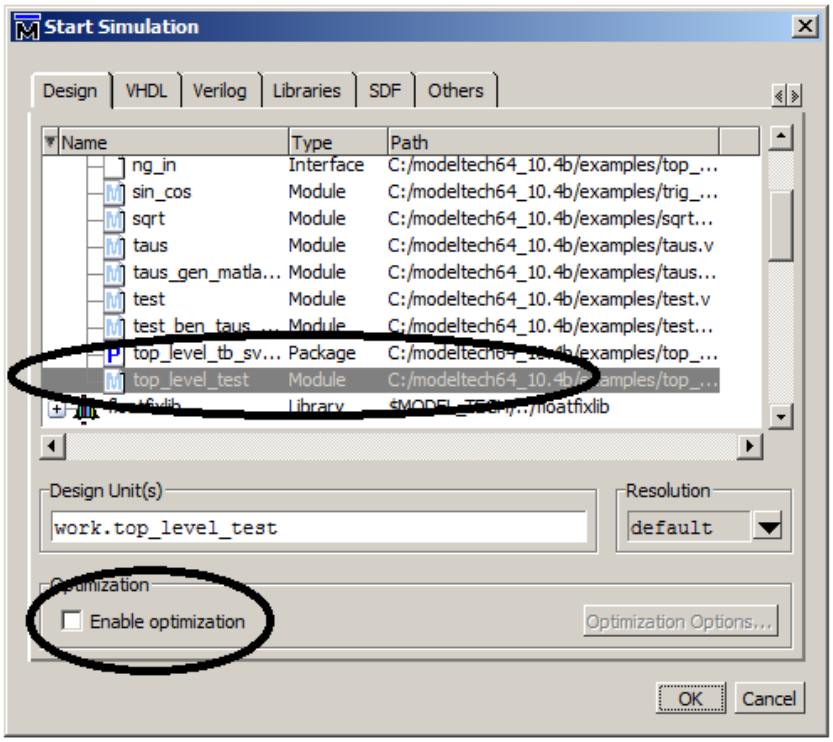



GitHub, Inc. [US] https://github.com/tejchava1460/Evaluation-Project-for-ASIC-FPGA-Design-Engineer/tree/master/Veri
This repository Search
Pull requests
tejchava1460 / Evaluation-Project-for-ASIC-FPGA-Design-E
Computer ▸ Local Disk (C:) ▸ modeltech64_10.4b ▸ examples ▸
Open New folder
Name Date modified Type Size
vhdl 8/6/2015 7:41 AM File folder
vrm 8/6/2015 7:41 AM File folder
work 7/24/2016 4:51 PM File folder
awgn_out 7/24/2016 5:48 AM Text Document 362 KB
checker_log_0 7/24/2016 5:48 AM Text Document 664 KB
checker_log_1 7/24/2016 5:48 AM Text Document 651 KB
concat 7/24/2016 5:48 AM Text Document 1 KB
log_impltn 7/24/2016 5:48 AM Text Document 2 KB
main 7/24/2016 5:48 AM Text Document 2 KB
Noise_genrator 7/24/2016 5:48 AM Clip Organizer Medi... 97 KB
o_p_gen_blk 7/24/2016 5:48 AM Text Document 1 KB
rand_1 7/24/2016 4:52 PM Text Document 127 KB
rand_2 7/24/2016 4:52 PM Text Document 127 KB
sqrt_unit 7/24/2016 5:48 AM Text Document 2 KB
taus 7/24/2016 5:48 AM Text Document 1 KB
taus_gen.cr.mti 7/24/2016 4:52 PM MTI File 1 KB
top_level_tb.sv 7/24/2016 5:48 AM SV File 7 KB
transcript 7/24/2016 4:58 PM File 1 KB
trig_fn_eval 7/24/2016 5:48 AM Text Document 1 KB
vish_stacktrace.vstf 7/23/2016 5:38 PM VSTF File 1 KB
vsim.wlf 7/23/2016 6:08 PM WLF File 976 KB
x0 7/24/2016 5:48 AM Text Document 176 KB
x1 7/24/2016 5:48 AM Text Document 176 KB
items selected Date modified: 7/24/2016 5:48 AM Date created: 7/24/2016 4:58 PM
Size: 2.08 MB
x1.txt
Add files
Help
Layout NoDesign
ColumnLayout AllColumns
Library
Name Type Path
work Library C:/modeltech64_10.4b/examples/work
floatfixlib Library $MODEL_TECH/../floatfixlib
ieee_env (empty) Library $MODEL_TECH/../ieee_env
infact Library $MODEL_TECH/../infact
mc2_lib (empty) Library $MODEL_TECH/../mc2_lib
mgc_ams (empty) Library
mtiAvm Library
mtiOvm Library
mtiPA Library
mtiRnm Library
mtiUPF Library
mtiUvm Library
osvvm Library
sv_std Library
vhdlopt_lib Library
vital2000 Library
ieee Library
modelsim_lib Library
std Library
std_developerskit Library
synopsys Library
verilog Library
Select Project File
Look in: examples
Recent Places
Desktop
Libraries
Computer
Network
Name Date modified Type
systemverilog 8/6/2015 7:41 AM File folder
Taus_generator_for_MATLAB_code 7/24/2016 4:48 PM File folder
triage 8/6/2015 7:41 AM File folder
tssi2mti 8/6/2015 7:41 AM File folder
tutorials 8/6/2015 7:41 AM File folder
ucdb 8/6/2015 7:41 AM File folder
ucis 8/6/2015 7:41 AM File folder
vcd 8/6/2015 7:41 AM File folder
verilog 8/6/2015 7:41 AM File folder
Verilog_Noise_generator 7/24/2016 4:46 PM File folder
vhdl 8/6/2015 7:41 AM File folder
vrm 8/6/2015 7:41 AM File folder
work 7/24/2016 4:51 PM File folder
Noise_genrator 7/24/2016 5:48 AM Clip Organizer M...
File name: Noise_genrator
Files of type: Project Files (*.ini,*.mpf)
Open
Cancel

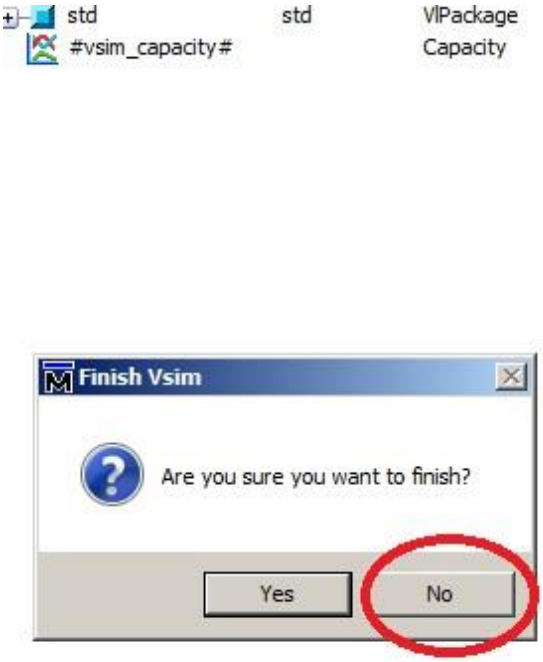
After copying the project, simulate the **top_level_test** module.

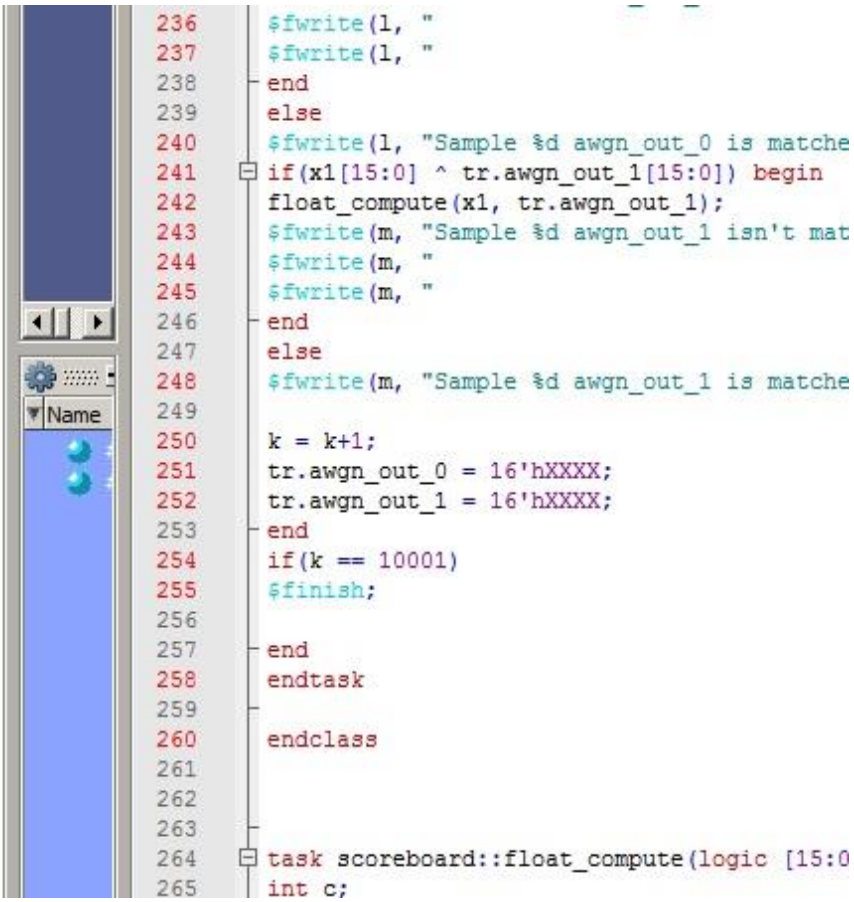
Uncheck the **Enable optimization** option.



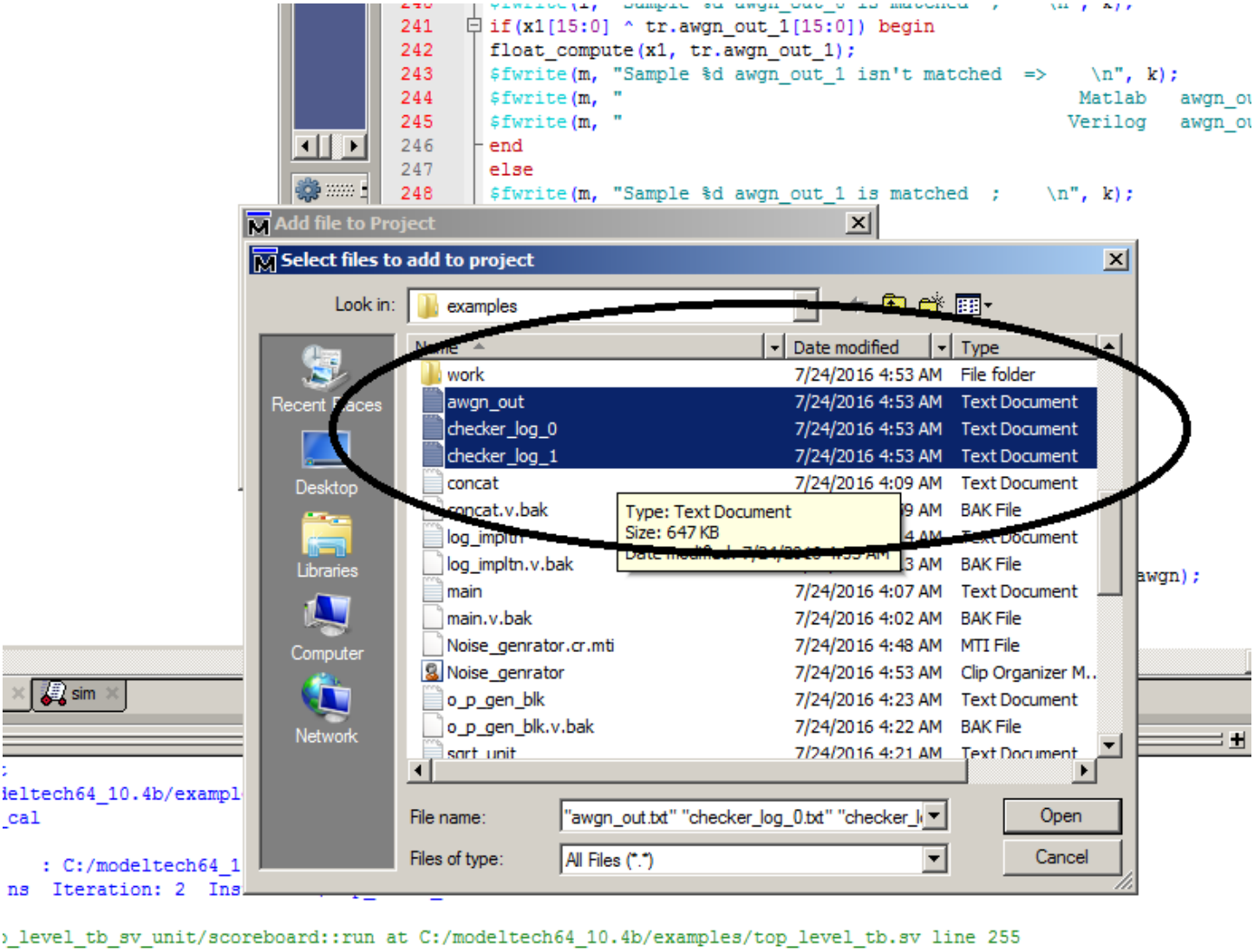


Wait for the **Finish Vsim** popup, and check the **'No'** option.



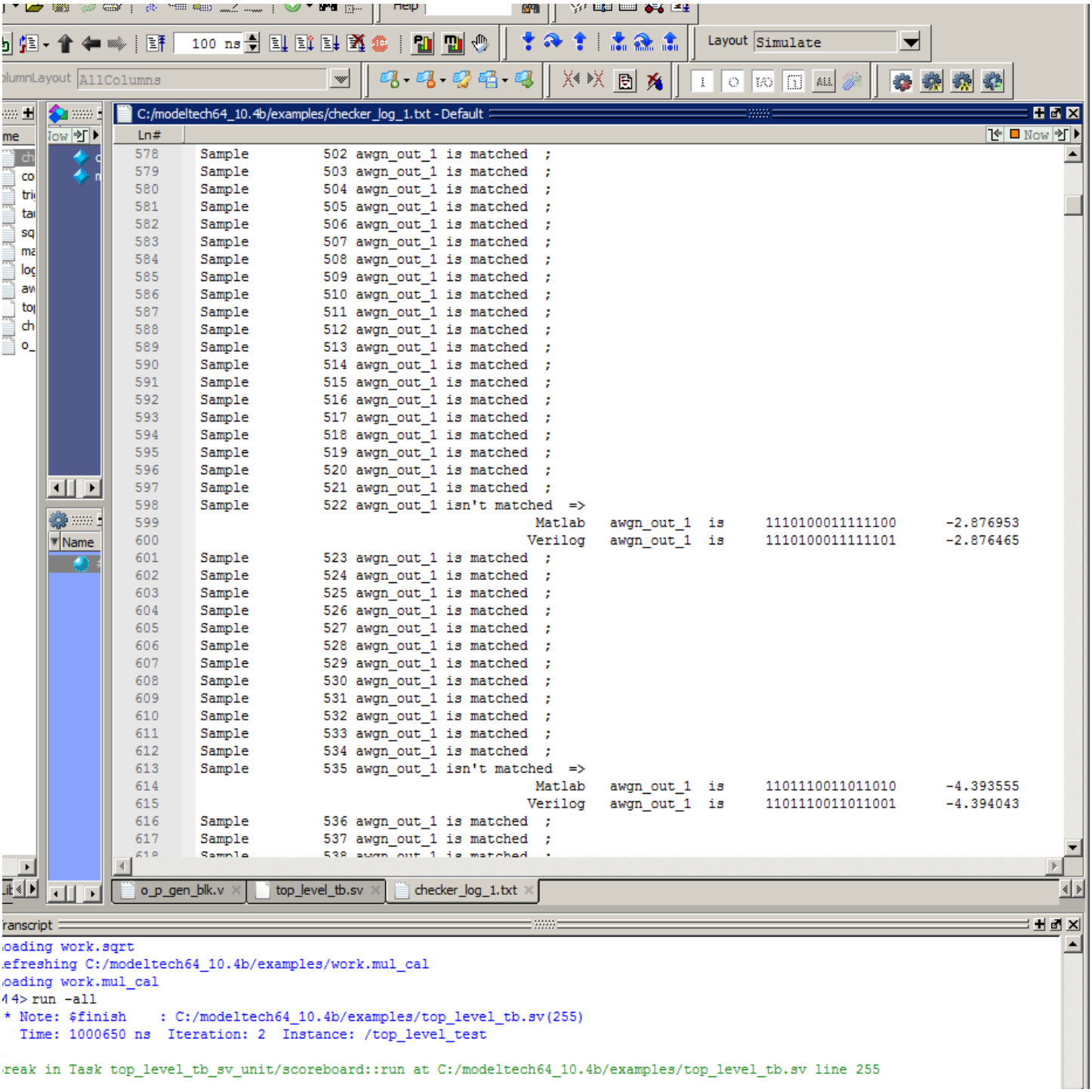


Highlighted files in the below picture are the output files of the **Verilog_Noise_generator**.



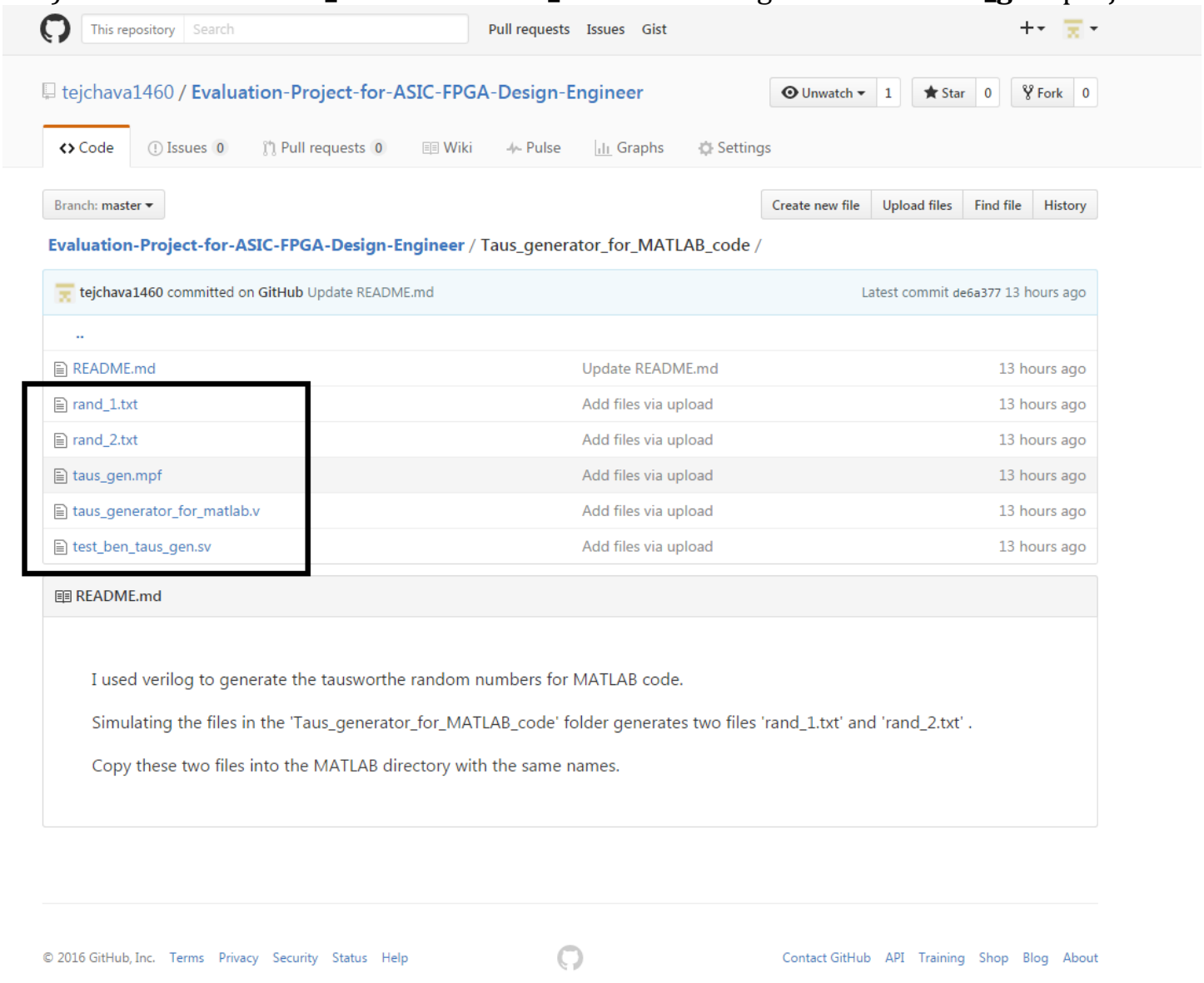
This is the format of the **'checker_log.txt'.**

For those **unmatched** samples the LSB bits not matched, this is because of various conversions between floating to binary and binary to floating conversions in the MATLAB.

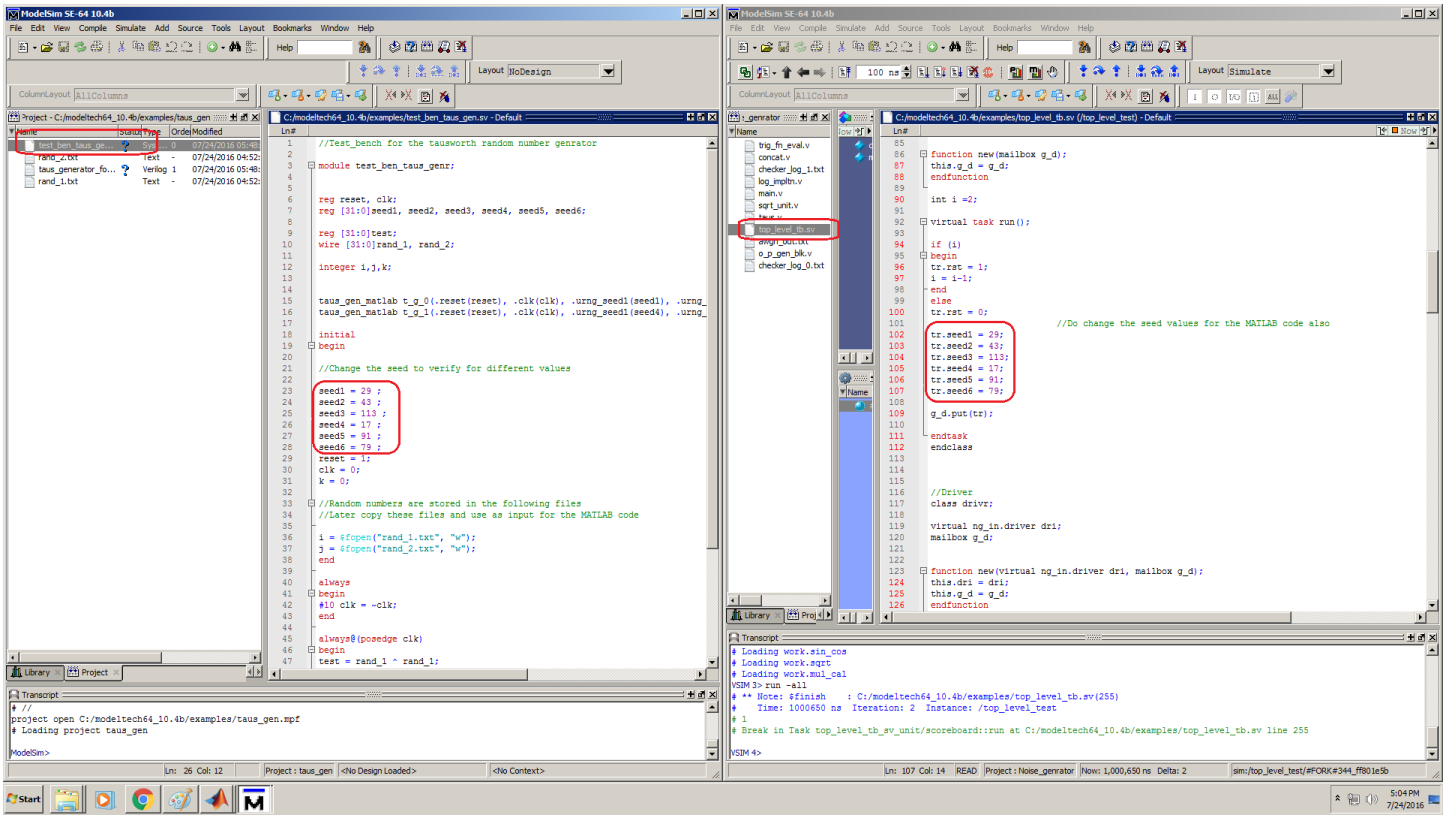


b) Simulation steps for the **custom urng_seed**.

i) Generate **'rand_1.txt'** and **'rand_2.txt'** files using the below **'taus_gen'** project



Before running simulation on the above project **change** the **seed** values in **'test_ben_taus_gen.sv'** & **'top_level_tb.sv'**



The seed values in the above boxes are **pre-defined**.

Change them to the **custom** values.

ii) Follow the steps in the **'Simulation steps for the Pre-defined urng_seed'** part.