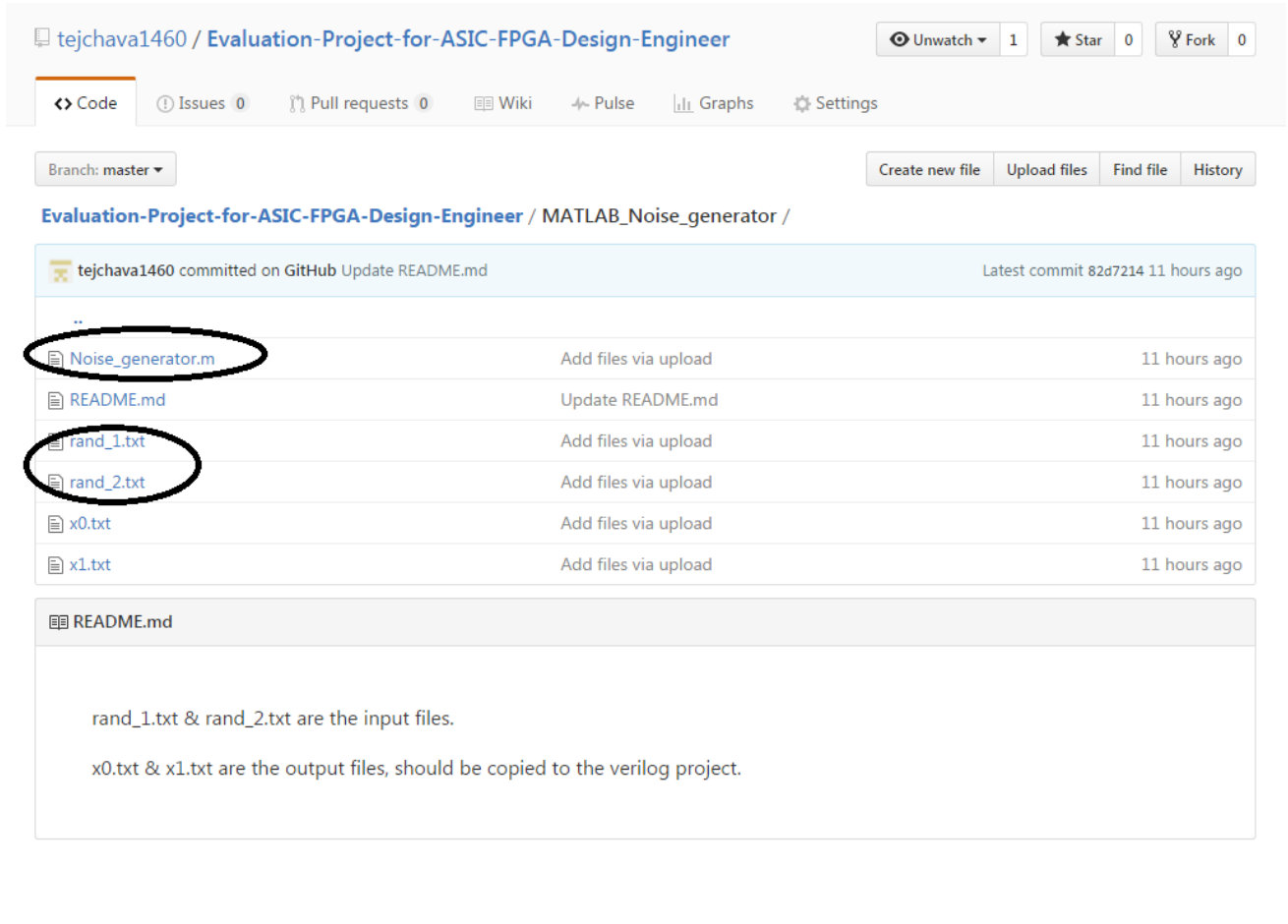


Follow the below steps in order to do the simulation:

- a) Simulation steps for the Pre-defined urng_seed.
- b) Simulation steps for the custom urng_seed.

a) Simulation steps for the Pre-defined urng_seed:

- i) Copy all the highlighted files into the MATLAB directory. It gives '**x0.txt**' & '**x1.txt**'.



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Evaluation-Project-for-ASIC-FPGA-Design-Engineer / MATLAB_Noise_generator /

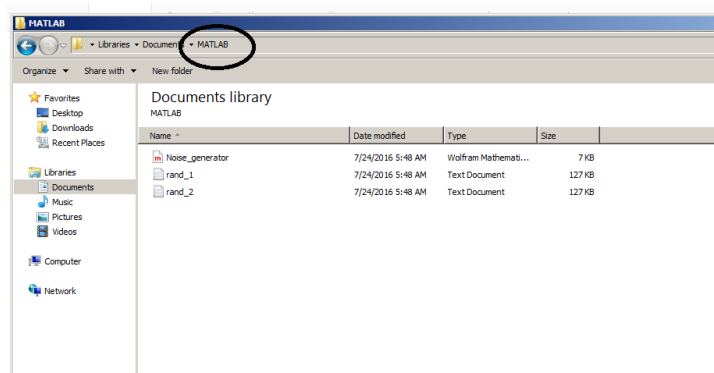
teychava1460 committed on GitHub Update README.md Latest commit 82d7214 11 hours ago

File	Action	Time
Noise_generator.m	Add files via upload	11 hours ago
README.md	Update README.md	11 hours ago
rand_1.txt	Add files via upload	11 hours ago
rand_2.txt	Add files via upload	11 hours ago
x0.txt	Add files via upload	11 hours ago
x1.txt	Add files via upload	11 hours ago

README.md

rand_1.txt & rand_2.txt are the input files.

x0.txt & x1.txt are the output files, should be copied to the verilog project.



MATLAB

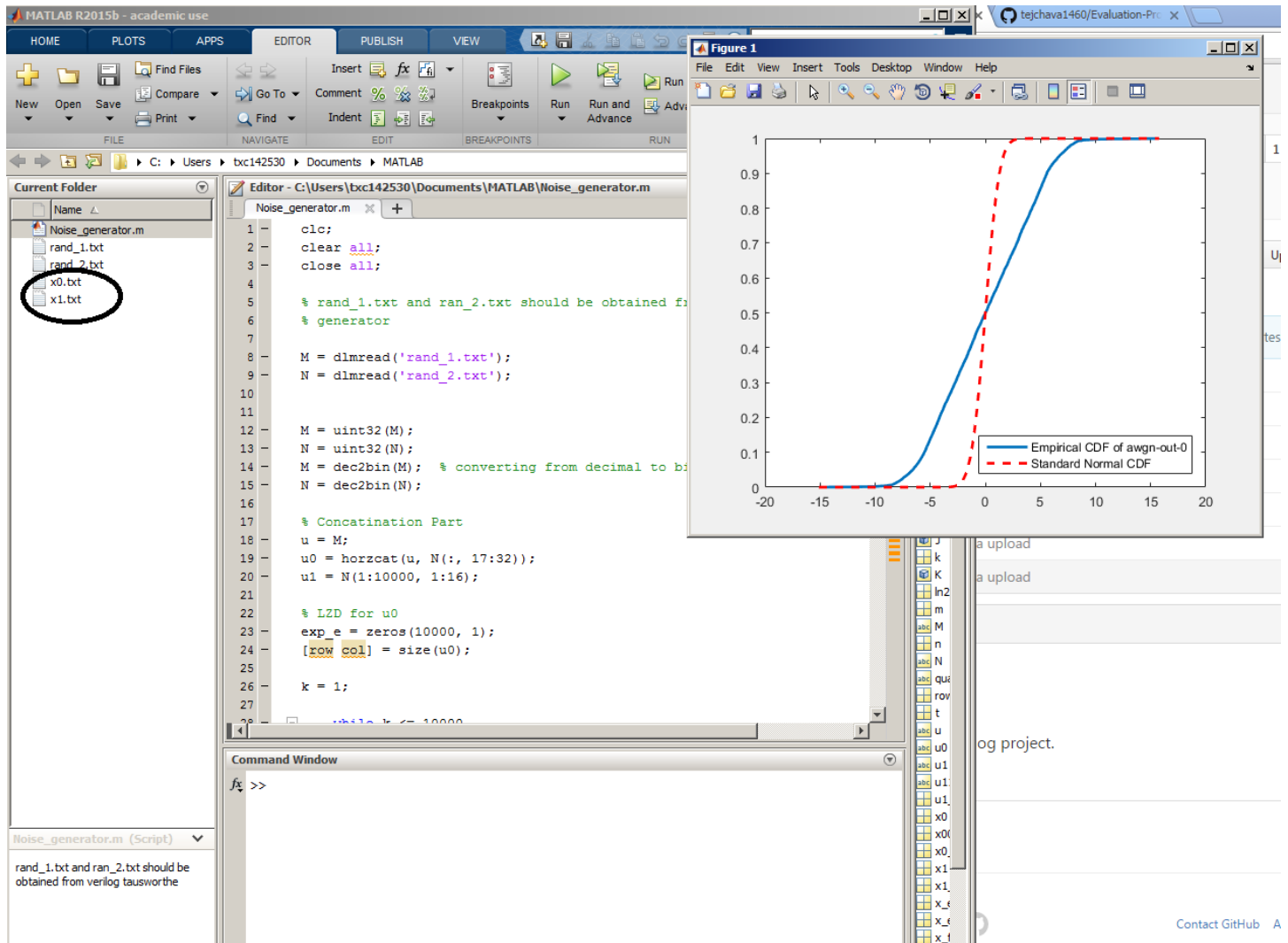
Libraries Documents MATLAB

Organize Share with New folder

Documents library

Name	Date modified	Type	Size
Noise_generator	7/24/2016 5:48 AM	Wolfram Mathemat...	7 KB
rand_1	7/24/2016 5:48 AM	Text Document	127 KB
rand_2	7/24/2016 5:48 AM	Text Document	127 KB

Result follows as



Copy the above 'x0.txt' & 'x1.txt' into the Verilog Noise generator Project.

ii) Copy the below highlighted files into the **Modelsim** directory.

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1

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0

Code

Issues 0

Pull requests 0

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Upload files

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History

Evaluation-Project-for-ASIC-FPGA-Design-Engineer / Verilog_Noise_generator /

tejchava1460 committed on GitHub Update README.md

Latest commit 4982322 12 hours ago

..		
Noise_genrator.mpf	Add files via upload	12 hours ago
README.md	Update README.md	12 hours ago
awgn_out.txt	Add files via upload	12 hours ago
checker_log_0.txt	Add files via upload	12 hours ago
checker_log_1.txt	Add files via upload	12 hours ago
concat.v	Add files via upload	12 hours ago
log_impltn.v	Add files via upload	12 hours ago
main.v	Add files via upload	12 hours ago
o_p_gen_blk.v	Add files via upload	12 hours ago
sqrtn_unit.v	Add files via upload	12 hours ago
taus.v	Add files via upload	12 hours ago
top_level_tb.sv	Add files via upload	12 hours ago
trig_fn_eval.v	Add files via upload	12 hours ago
x0.txt	Add files via upload	12 hours ago
x1.txt	Add files via upload	12 hours ago

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Computer Local Disk (C:) modeltech64_10_4b examples Search examples

Open New folder

Name	Date modified	Type	Size
vhdl	8/6/2015 7:41 AM	File folder	
verm	8/6/2015 7:41 AM	File folder	
work	7/24/2016 4:51 PM	File folder	
awgn_out	7/24/2016 5:48 AM	Text Document	362 KB
checker_log_0	7/24/2016 5:48 AM	Text Document	664 KB
checker_log_1	7/24/2016 5:48 AM	Text Document	651 KB
concat	7/24/2016 5:48 AM	Text Document	1 KB
log_impltn	7/24/2016 5:48 AM	Text Document	2 KB
main	7/24/2016 5:48 AM	Text Document	2 KB
Noise_generator	7/24/2016 5:48 AM	Clip Organizer Medi...	97 KB
o_p_gen_blk	7/24/2016 5:48 AM	Text Document	1 KB
rand_1	7/24/2016 4:52 PM	Text Document	127 KB
rand_2	7/24/2016 4:52 PM	Text Document	127 KB
sqr1_unit	7/24/2016 5:48 AM	Text Document	2 KB
taus	7/24/2016 5:48 AM	Text Document	1 KB
taus_gen.cr.mti	7/24/2016 4:52 PM	MTI File	1 KB
top_level_tb.sv	7/24/2016 5:48 AM	SV File	7 KB
transcript	7/24/2016 4:58 PM	File	1 KB
trig_fn_eval	7/24/2016 5:48 AM	Text Document	1 KB
vish_stacktrace.vstf	7/23/2016 5:38 PM	VSTF File	1 KB
vsim.wlf	7/23/2016 6:08 PM	WLF File	976 KB
x0	7/24/2016 5:48 AM	Text Document	176 KB
x1	7/24/2016 5:48 AM	Text Document	176 KB

Items selected Date modified: 7/24/2016 5:48 AM Date created: 7/24/2016 4:58 PM Size: 2.08 MB

x1.txt Add files via upload

ColumnLayout AllColumns

Library

Name	Type	Path
work	Library	C:/modeltech64_10_4b/examples/work
floatfixlib	Library	\$MODEL_TECH/./floatfixlib
ieee_env (empty)	Library	\$MODEL_TECH/./ieee_env
infact	Library	\$MODEL_TECH/./infact
mc2_lib (empty)	Library	\$MODEL_TECH/./mc2_lib
mgc_ams (empty)	Library	\$MODEL_TECH/./mgc_ams
mtAvm	Library	
mtbVmm	Library	
mtbPA	Library	
mtbRm	Library	
mtbUPF	Library	
mtbUvm	Library	
osvm	Library	
sv_std	Library	
vhdopt_lib	Library	
vital2000	Library	
ieee	Library	
modelsim_lib	Library	
std	Library	
std_developerskit	Library	
synopsys	Library	
verilog	Library	

Select Project File

Look in: examples

Name	Date modified	Type
systemverilog	8/6/2015 7:41 AM	File folder
Taus_generator_for_MATLAB_code	7/24/2016 4:48 PM	File folder
trig	8/6/2015 7:41 AM	File folder
tsi2mtb	8/6/2015 7:41 AM	File folder
tutorials	8/6/2015 7:41 AM	File folder
ucdb	8/6/2015 7:41 AM	File folder
ucd	8/6/2015 7:41 AM	File folder
vcd	8/6/2015 7:41 AM	File folder
verilog	8/6/2015 7:41 AM	File folder
Verilog_Noise_generator	7/24/2016 4:46 PM	File folder
vhdl	8/6/2015 7:41 AM	File folder
verm	8/6/2015 7:41 AM	File folder
work	7/24/2016 4:51 PM	File folder
Noise_generator	7/24/2016 5:48 AM	Clip Organizer Medi...

File name: Noise_generator Open

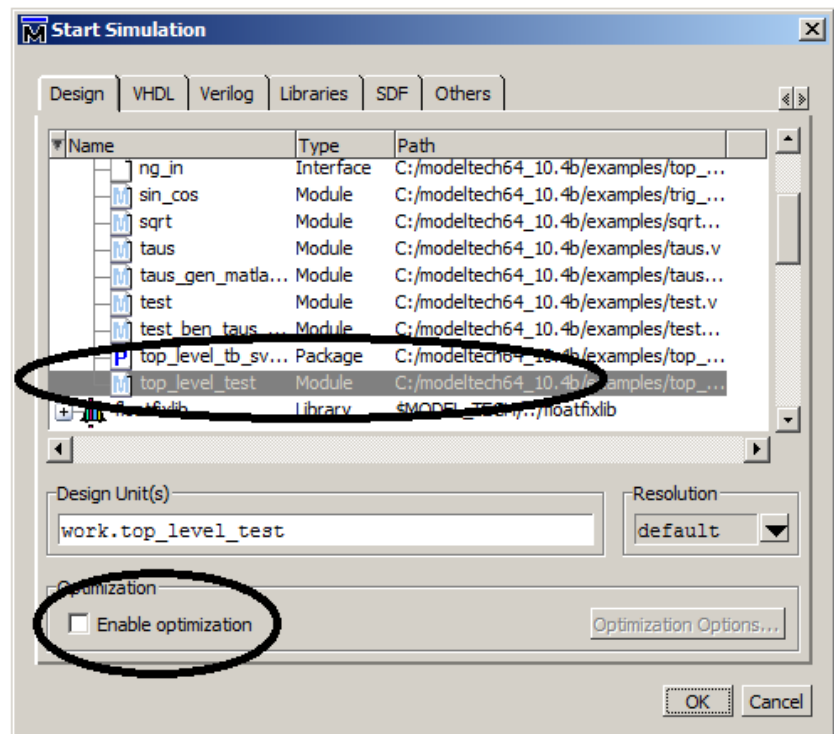
Files of type: Project Files (*.ini;.mpf) Cancel

After copying the project, simulate the **top_level_test** module.

Uncheck the **Enable optimization** option.

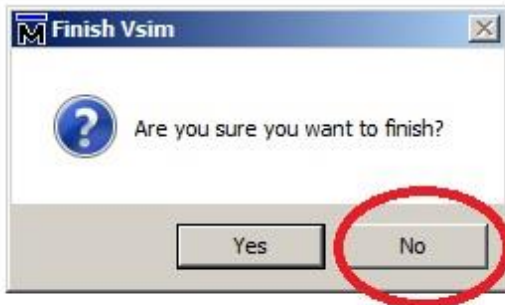
Project - C:/modeltech64_10.4b/examples/Noise_Generator

Name	Status	Type	Order	Modified
trig_fn_eval.v	?	Verilog	0	07/24/2016 05:48:09 ...
concat.v	?	Verilog	1	07/24/2016 05:48:09 ...
checker_log_1.txt		Text	-	07/24/2016 05:48:09 ...
log_impltn.v	?	Verilog	2	07/24/2016 05:48:09 ...
main.v	?	Verilog	3	07/24/2016 05:48:09 ...
sqrt_unit.v	?	Verilog	5	07/24/2016 05:48:09 ...
taus.v	?	Verilog	7	07/24/2016 05:48:09 ...
top_level_tb.sv	?	Syst...	6	07/24/2016 05:48:09 ...
awgn_out.txt		Text	-	07/24/2016 05:48:09 ...
o_p_gen_blk.v	?	Verilog	4	07/24/2016 05:48:09 ...
checker_log_0.txt		Text	-	07/24/2016 05:48:09 ...



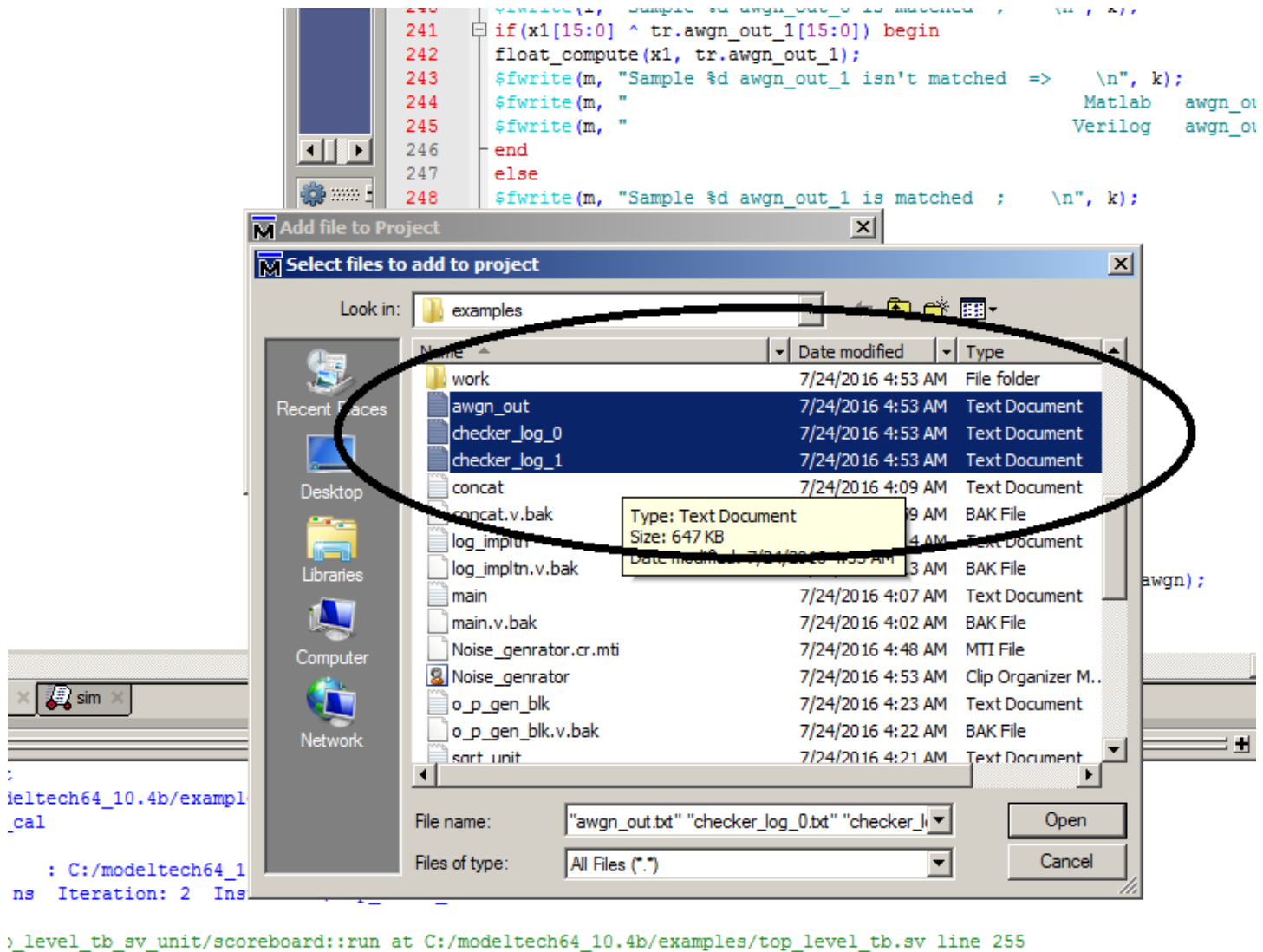
Wait for the **Finish Vsim** popup, and check the '**No**' option.

std std VIPackage
#vsim_capacity# Capacity



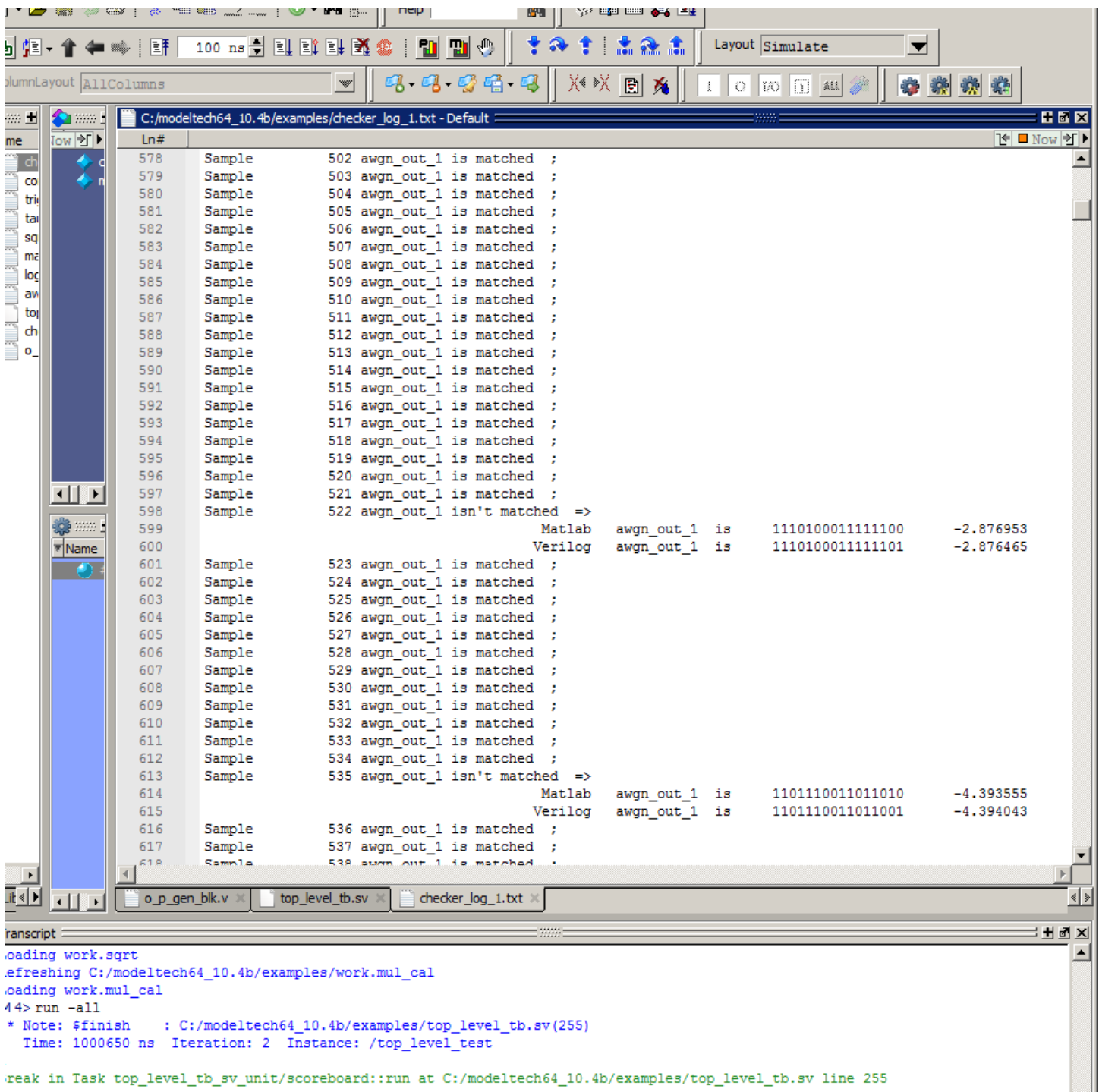
```
236 $fwrite(1, "  
237 $fwrite(1, "  
238 end  
239 else  
240 $fwrite(1, "Sample %d awgn_out_0 is matche  
241 if(x1[15:0] ^ tr.awgn_out_1[15:0]) begin  
242 float_compute(x1, tr.awgn_out_1);  
243 $fwrite(m, "Sample %d awgn_out_1 isn't mat  
244 $fwrite(m, "  
245 $fwrite(m, "  
246 end  
247 else  
248 $fwrite(m, "Sample %d awgn_out_1 is matche  
249  
250 k = k+1;  
251 tr.awgn_out_0 = 16'hXXXXX;  
252 tr.awgn_out_1 = 16'hXXXXX;  
253 end  
254 if(k == 10001)  
255 $finish;  
256  
257 end  
258 endtask  
259  
260 endclass  
261  
262  
263  
264 task scoreboard::float_compute(logic [15:0]  
265 int c;
```

Highlighted files in the below picture are the output files of the **Verilog_Noise_generator**.



This is the format of the 'checker_log.txt'.

For those **unmatched** samples the LSB bits not matched, this is because of various conversions between floating to binary and binary to floating conversions in the MATLAB.



```
C:/modeltech64_10.4b/examples/checker_log_1.txt - Default
Ln#
578 Sample 502 awgn_out_1 is matched ;
579 Sample 503 awgn_out_1 is matched ;
580 Sample 504 awgn_out_1 is matched ;
581 Sample 505 awgn_out_1 is matched ;
582 Sample 506 awgn_out_1 is matched ;
583 Sample 507 awgn_out_1 is matched ;
584 Sample 508 awgn_out_1 is matched ;
585 Sample 509 awgn_out_1 is matched ;
586 Sample 510 awgn_out_1 is matched ;
587 Sample 511 awgn_out_1 is matched ;
588 Sample 512 awgn_out_1 is matched ;
589 Sample 513 awgn_out_1 is matched ;
590 Sample 514 awgn_out_1 is matched ;
591 Sample 515 awgn_out_1 is matched ;
592 Sample 516 awgn_out_1 is matched ;
593 Sample 517 awgn_out_1 is matched ;
594 Sample 518 awgn_out_1 is matched ;
595 Sample 519 awgn_out_1 is matched ;
596 Sample 520 awgn_out_1 is matched ;
597 Sample 521 awgn_out_1 is matched ;
598 Sample 522 awgn_out_1 isn't matched =>
599 Matlab awgn_out_1 is 1110100011111100 -2.876953
600 Verilog awgn_out_1 is 1110100011111101 -2.876465
601 Sample 523 awgn_out_1 is matched ;
602 Sample 524 awgn_out_1 is matched ;
603 Sample 525 awgn_out_1 is matched ;
604 Sample 526 awgn_out_1 is matched ;
605 Sample 527 awgn_out_1 is matched ;
606 Sample 528 awgn_out_1 is matched ;
607 Sample 529 awgn_out_1 is matched ;
608 Sample 530 awgn_out_1 is matched ;
609 Sample 531 awgn_out_1 is matched ;
610 Sample 532 awgn_out_1 is matched ;
611 Sample 533 awgn_out_1 is matched ;
612 Sample 534 awgn_out_1 is matched ;
613 Sample 535 awgn_out_1 isn't matched =>
614 Matlab awgn_out_1 is 1101110011011010 -4.393555
615 Verilog awgn_out_1 is 1101110011011001 -4.394043
616 Sample 536 awgn_out_1 is matched ;
617 Sample 537 awgn_out_1 is matched ;
618 Sample 538 awgn_out_1 is matched ;

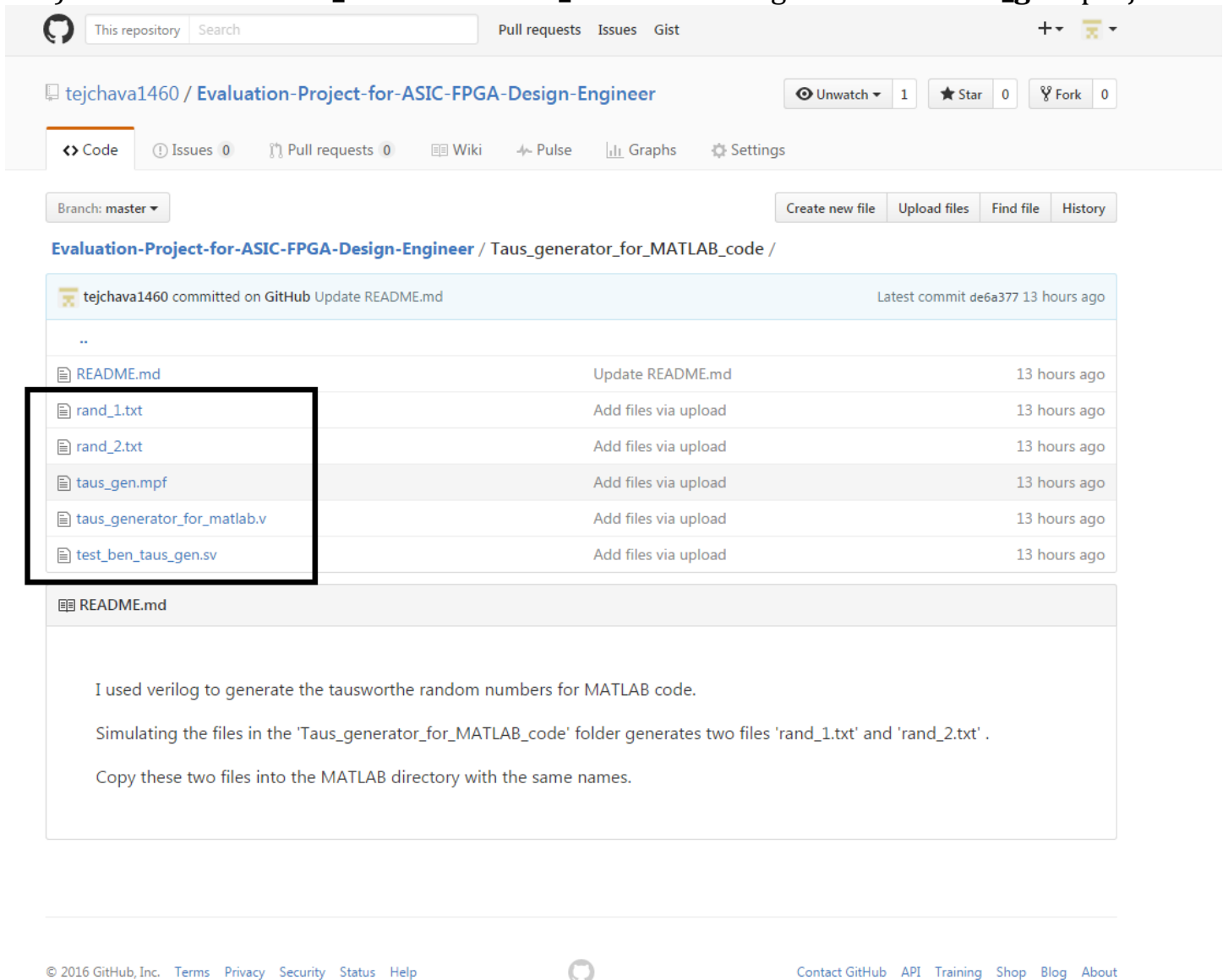
o_p_gen_blk.v x top_level_tb.v x checker_log_1.txt x

transcript
loading work.sqrt
refreshing C:/modeltech64_10.4b/examples/work.mul_cal
loading work.mul_cal
44> run -all
* Note: $finish : C:/modeltech64_10.4b/examples/top_level_tb.v(255)
Time: 1000650 ns Iteration: 2 Instance: /top_level_test

reak in Task top_level_tb_sv_unit/scoreboard::run at C:/modeltech64_10.4b/examples/top_level_tb.v line 255
```


b) Simulation steps for the **custom urng_seed**.

i) Generate '**rand_1.txt**' and '**rand_2.txt**' files using the below '**taus_gen**' project



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tejkava1460 committed on GitHub Update README.md Latest commit de6a377 13 hours ago

File	Commit Message	Time
..		
README.md	Update README.md	13 hours ago
rand_1.txt	Add files via upload	13 hours ago
rand_2.txt	Add files via upload	13 hours ago
taus_gen.mpf	Add files via upload	13 hours ago
taus_generator_for_matlab.v	Add files via upload	13 hours ago
test_ben_taus_gen.sv	Add files via upload	13 hours ago

README.md

I used verilog to generate the tausworthe random numbers for MATLAB code.

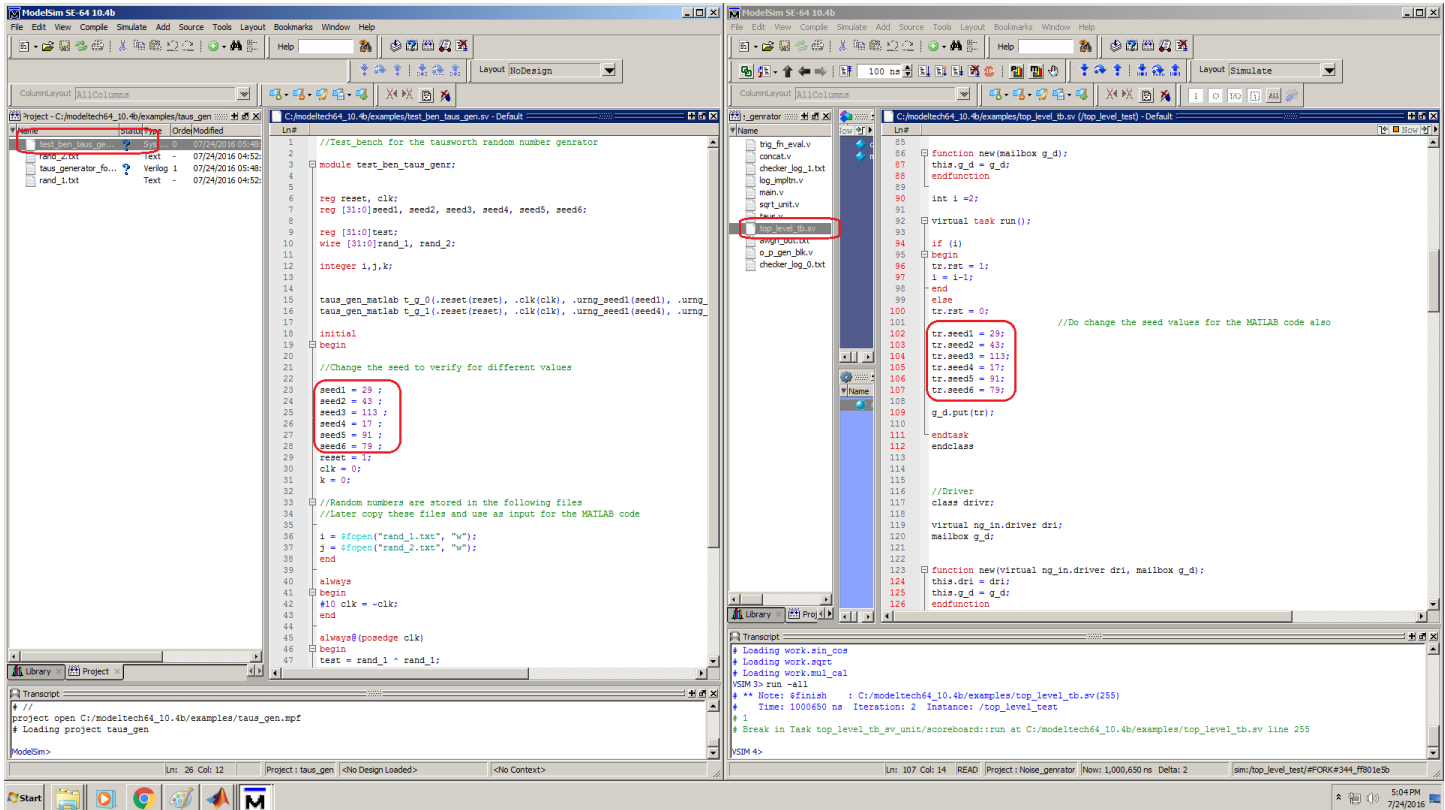
Simulating the files in the 'Taus_generator_for_MATLAB_code' folder generates two files 'rand_1.txt' and 'rand_2.txt'.

Copy these two files into the MATLAB directory with the same names.

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Before running simulation on the above project **change** the **seed** values in 'test_ben_taus_gen.sv' & 'top_level_tb.sv'



The seed values in the above boxes are **pre-defined**.

Change them to the **custom** values.

- ii) Follow the steps in the 'Simulation steps for the Pre-defined urng_seed' part.