Vinutha S Mallya

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About Me

Currently pursuing B.E at **Dayananda Sagar College of Engineering** in the department of **Electronics and Communication Engineering**. Passionate to learn new technologies and to excel innovative technology applications. The main objective of my career is to work for a firm where I will be able to apply my VLSI knowledge, skills and talent as a Design and Verification Engineer which would motivate me as a fresh graduate along with fulfilling the organizational goals.

Education

Qualification	Institution	University	Grades/Percentage	Year of passing
BE(ECE)	Dayananda Sagar College of Engineering, Bengaluru	VTU	8.61(CGPA)	2023(Pursuing)
12th	Sri Siddaganga PU Science College, Davanagere	KSEEB	96.16%	2019
10th	Sri Siddaganga High School , Davanagere	ICSE	97.76%	2017

Professional Experience

Trainee at Maven Silicon

Currently undergoing the course titled “Advanced VLSI Design and Verification”. Completed the Digital Design using Verilog. Gained knowledge about Advanced Verilog and Code Coverage. Completed the Verification concepts using System Verilog, SV assertions and UVM .

Projects

Router 1x3 RTL Design *Aug 2022*

- Worked on the design and verification of each module which combine together to form the router.
- The router accepts data packets on a single 8-bit port and routes them to respective desired channel.
- Totally the design consisted of four major blocks as FSM, Register, Synchronizer, FIFO blocks
- Tools used :- ModelSim(Verilog Simulation).
- HDL:- Verilog.

Alarm Clock RTL design *March 2023*

- Developed the RTL code for each of the sub-blocks used in the block level architecture of the Alarm clock.
- Verified each sub-block using task-based Verilog Testbench.
- Finally verified the top-level RTL using Verilog Testbench.
- Tools used :- ModelSim(Verilog Simulation).
- HDL:- Verilog , Quartus prime.

Implementation of Palm Vein Image Processing and Enhancement on FPGA *Sept 2022(ongoing)*

- Will be able to build a system on FPGA for the image processing and enhancement of the Palm Veins
- As palm veins are not visible to our naked eyes and hence cannot be forged easily.
- Show the difference of the processing power between FPGA and the other CPU’s.
- Tools used:- ModelSim, Intel Quartus Prime, Matlab, Linux.
- HDL:- Verilog, C.

Technical Skills

Course Studied	Digital Electronics**,** Fundamentals of VLSI , Verilog Programming, STA, Advanced Verilog and Code Coverage, System Verilog and assertions, UVM.
HVL\HDL	Verilog, System Verilog
Programming Languages	C, Python.
Scripting languages	Perl, Tcl
Simulation Tools	Intel Quartus Prime, ModelSim, Cadence, Synopsis-IC Compiler ,MATLAB, Multisim.
Operating System	Windows, Linux.
FPGA Used	DE-10Lite, DE1-SoC.
Microsoft Office	Word, Excel, PowerPoint.

Achievements & Extra-Curricular

- **Rank Holder** of both 10th and 12th Grade and with a **KCET ranking of 5164**.
- **Volunteer** at the ARCC Davanagere , an Organization working towards animal welfare.
- **Coordinator** for the **Project Open Day** conducted by the Dept. of ECE of DSCE in June 2022.
- Volunteer at **Youth For Parivarthan**, a registered non-profit organisation working towards “Swachha Bengaluru”.

Behavioral Skills

- Public Speaking
- Teamwork
- Leadership
- Creativity

Hobbies

- Cooking different kinds of cuisines
- Gardening
- Exploring about mythology
- Painting and Sketching

Languages Known

- ***English***
- ***Kannada***
- ***Hindi***
- ***Konkani***

Declaration

I certify that the particulars given above are correct and complete to the best of my knowledge and believe that nothing has been concealed by me.

Date :- 29 March 2023
Place:- Bengaluru

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