Bharamu S K
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EDUCATIONAL QUALIFICATION

Year	Degree	Institution/ School	Performance
2018	B.E (Electronics and Communication Eng.)	J.S.S Academy of Technical Education Bangalore	67.5%
2015	Diploma(Electronics and Communication Eng.)	B.V.V.S Polytechnic Bagalkot	77.44%
2012	Class X	S.S.S.B.V.V.S Hi-School Halingali	82.72%

PROFESSIONAL TRAINING

- **Advance VLSI Design and Verification training.** [Jan'18 – Jun'18]
  Maven Silicon Bangalore.

PROFESSIONAL SKILLS

UVM | SV | SVA | OOPS Concept | Verilog | STA | Digital Electronics | Perl | Embedded C.

TOOLS

Linux | GVIM | Cadence SimVision | Vmanger | SVN |Questasim | Modelsim | Quartus Prime | EDA Playground

PROFESSIONAL EXPERIENCE

Senior Design Verification Engineer, ExcelMax Bangalore [Jun'2018 – Present]

Profession Summary:

- Experience in developing Verification plan, Implementation test plan documents.
- Experience in developing System Verilog, UVM-based Verification environments and testbench components including agents, drivers and scoreboard.
- Experience in writing Tests and Sequences with Constrained-Random stimulus.
- Good Knowledge on UART and I2C Protocol.
- Good Knowledge on Assertion.
- Worked Code coverage.
- Debugging.

PROJECTS

Verification of TDM switch for Modem:

- TDM switch is used to make use of the bandwidth of channels with maximum efficiency via shared interface pipes. It Supports E1 bit rate and time slots (32 time slots or 32 DSO channels at bit rate 2.048Mbps).
- Created Verification plan.
- Developed SV-UVM based verification plug & play env.
- Created testcase sequences to verify various key features.
- Analyzed toggle coverage.
- Worked on code model.
- Closed Code coverage as 100%.

Verification of Real-Time Clock:

- A real-time clock (RTC) is an electronic device (most often in the form of an integrated circuit) that measures the passage of time.The term real-time clock is used to avoid confusion with ordinary hardware clocks which are only signals that govern digital electronics, and do not count time in human units.
- RTC module is capable of retrive system from standby mode.
- Wrote SV based testcases to verify RTC functionality.
- Covered use cases scenario.
- Created Verification Environment using UVM Methodology.
- Toggle coverage closure.

Verification of DSPI:

- SPI is a serial interfaced protocol used for communication in embedded systems. It's a four-pin protocol. Device is supposed to communicate with external world for data transfer to-and-from.
- Data transfer between Master and Slave is ensured.
- Created Verification plan.
- Created testcase sequences to verify various key features.

UART IP Verification:

- The UART IP core provides serial communication capabilities, which allows communication with modem or other external devices.
- Implemented an Baudrate generation block.

Verification:

- Verified the design using UVM TB Architecture blocks i.e. Agents, Environment and Tests.
- Verified the UART packet of 5,6,7,8bits. Prity and Different baudrate also verified using UVM TB.
- Verified the RTL module using Verilog TB.

I2C IP Verification:

- I2C is a popular serial communication protocol used to connect microcontrollers, sensors.
- Data transfer between Master and Slave is ensured.
- Prepared the Verification Plan & implemented test cases for verification of IP.
- Verified the the design using UVM TB Architecture.

AHB2APB Bridge:

- The AHB to APB bridge is an AHB slave, providing an interface between the high- speed. AHB and the low-power APB. Read and write transfers on the AHB are converted into equivalent transfers on the APB
- Analysis of AHB2APB Bridge specifications
- Created UVM based verification environment.
- Wrote the test-cases for single transfer, burst transfer.
- Worked on APB Controller logic.

APB VIP Verification :

- APB is designed for low bandwidth control accesses, for example peripheral interfaces on system. This bus has an address and data phase but a much reduced, low complexity signal list. Furthermore, it is an interface designed for a low frequency system with a low bit width (32 bits)
- AMBA-APB protocol specification.
- Created Verification Plan.
- Created Verification Environment using UVM Methodology
- Worked on Write & Read Sequence, Driver, Monitor, Scoreboard
- Performed read and write operations with and without wait states. Also, Slave Error Situation.

RAM Verification Project:

- 4096x64 Dual Port Ram can read and write data simultaneously with unidirectional data ports.
- Implemented the design with write and read enable signals using Verilog HDL and synthesized the circuit using Quartus Prime.
- Perform write to any memory location, read from the same memory location, read data should be the same as written data
- Assert reset in between write/read operation and check for default values.
- Verified the design using functional coverage by defining covergroups and coverpoints.

FIFO Verification :

- Develop a comprehensive testbench environment to verify the functionality and performance of the FIFO design.
- Perform functional simulation, checking for proper data flow, synchronization, and handling of empty and full conditions.
- Debug and resolve design or verification-related problems, ensuring the FIFO operates correctly according to the specifications.
- Created Verification Plan.
- Created Verification Environment using SV Test Bench.
- Worked on Testcase writing, Generator, Driver, Monitor.

HOBBIES

Cricket **I** Kabaddi **I** Cooking

LANGUAGES

Kannada **I** English **I** Hindi **I** Telugu.

DECLARATION

I, hereby declare that the information furnished above is correct to the best of my knowledge.

Date:

Place: Bangalore [Bharamu S K]