CONTACT

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OBJECTIVE

To obtain an entry-level position at a respected organization and utilize the educational knowledge.

EDUCATION

2020-2022

- **VELLORE INSTITUTE OF TECHNOLOGY (VIT -VELLORE)**
  VLSI design (MTech)
  7.09

2020

- **Hindustan institute of technology and science**
  Electronics and communication engineering (B.tech)
  8.92

2016

- **Narayana junior college**
  Intermediate board of education
  95.9%

2014

- **Narayana e-techno schools**
  School of secondary education
  10 Gpa

SKILLS

- Knowledge in C , python and basic of Linux
- Digital design , testing and verification PLC, SCADA manufacturing.
- HDL: verilog HDL , system verilog Tools used : cadance virtuoso, intel quartus prime, Modelsim, synopsis

PROJECTS

- **Fast FIR filter using compressor and carry select adder.**
  - Designed and implemented FIR filter using a modified Carry select adder and compressor in Intell quartus prime.
  - This design focusses on increasing speed and decrease area.
  - Modified Carry select adder consists of BEC (excees1 convertor in binary format) along with Ripple carry adder.

- **Ultra low voltage digital IC design techniques**
  - Design of modified Wilson mirror current based level shifter and implemented in cadance virtuoso using 90nm technology
  - This design focusses on reducing the power consumption.
  - Comparison of the design with different level shifters
- **Approximate Square Rooters for error resilient applications**
  - This project is based on designing the approximate square root circuit.The proposed design focusses on reducing the area and improve energy efficiency
  - The proposed design comprises of two methods, in first the exact subtractor cells which were substituted in the place of subtractor cells and the second method uses bit truncation for reducing the complexity
- **Complete Home automation using IOT**
  - Automated complete home electronics and electrical appliances and operated them using IOT.
  - New idea of Home automation with low cost.
  - Versatility to operate them using LAN or through cloud.
- **Low power dynamic comparator**
  To create a double tail type comparator with low power consumption
- **Design and verification of AMBA APB protocol using UVM**
  - Designing of APB protocol
  - Study of universal verification methodology
  - Verification of APB using UVM

ACHIEVEMENTS, CERTIFICATIONS, EXTRA CURRICULAR

- Basic telecommunication internship at BSNL
- IOT internship at Experts hub industrial training center
- Received best intern award from Experts hub industrial training
- PLC manufacturing training and SCADA programming in zenmaq technologies.

- Participated in many technical events and workshops

PERSONAL DETAILS

- Date of Birth : 01/08/1998
- Nationality : INDIAN
- Languages known : English, Hindi, Telugu , Tamil
- Hobbies : Listening to music and travelling
- Gender : Male

DECLARATION

- I here by declare that the details given by me are true to the best of my knowledge