



Jatin Jitendra Sharma

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CAREER OBJECTIVE/ ABOUT ME :

To enhance my professional skills, capabilities and knowledge in an organization which recognizes the value of hard work and trusts me with responsibilities and challenges. Seeking for Job/ Internship in RTL Design and Verification / Open to new opportunities in Semiconductor Industry

PROFESSIONAL TRAINING / CERTIFIED TRAINING /CERTIFICATION /HANDS ON TRAINING :

- **Advanced VLSI Design and Verification Course**
Maven Silicon VLSI Design and Training Centre, Bengaluru
May 2022 till date.
- **Pcb and Circuit Design**
Certified by CETPA INFOTECH PRIVATE LIMITED , Noida.
16th Oct 2021 to 12th Nov 2021.

EDUCATION

- | | |
|------|---|
| 2016 | • B. E in Electronics And Telecommunications
Sant Gadge Baba Amravati University
8.61 CGPA |
| 2013 | • Diploma in Electronics And Telecommunications
MSBTE, Pune
66.91% |
| 2010 | • 10th
Dyanmata High School, Amravati
70.91% |

TECHNICAL SKILLS

- **VLSI Domain Skills**
HDL: Verilog
HVL: SystemVerilog
Verification Methodologies : Constraint Random Coverage Driven Verification
Assertions Based Verification - SVA
TB Methodology : UVM
Protocols : AXI, AHB, UART, I2C, SPI
EDA tools: Mentor Graphics Questa Sim and Xilinx- Ise, Xilinx- Vivado.
Domain: ASIC/FPGA front-end Design and Verification.
- **Programming Skills**
C [Data type | Array | Pointers | Memory Allocation | List | Stacks and Queues.
C++, Good Knowledge of Oops concepts.
- **Core Skills**
RTL coding using synthesizable constructs of Verilog, FSM based design, Simulation, CMOS Fundamentals, Code Coverage, Functional Coverage, Synthesis, Static Timing

Analysis,
Assertions Based Verification using SVA.

- **Operating System**
Linux

VERIFICATION

- **System Verilog HVL:**
Memories - Dynamic array, Queue, Associative array, Task & Function - Pass by reference
Interface - Modport and clocking block
Basic and advanced object-oriented programming - Handle assignments, Copying the object contents, Inheritance, polymorphism, static properties and methods, virtual classes and parameterized classes.
Constraint Randomization - constraint overriding and inheritance, Distribution and conditional constraints, Soft, static and inline constraints.
Thread synchronization techniques - events, semaphores and Mailbox - built-in methods
Functional coverage - Cover groups, bins and cross-coverage, CRCOV and regression testing.
- **System Verilog Assertions:**
Types of assertions, assertion building blocks, sequences with edge definitions and logical relationship. Sequences with different timing relationships. Clock definitions, implication and repetition operators, different sequence compositions, inline and binding assertions, advanced SVA Features and assertion Coverage.
- **UVM:**
UVM Objects & Components
UVM Factory & overriding methods
Stimulus Modelling, UVM Phases, UVM Configuration, TLM, UVM Sequence, virtual sequence & sequencer, Introduction to RAL.

PROJECTS

- **Router 1x3**
Designed using Verilog. Implemented by various submodules like FIFO, FSM, Register, Synchronizer working together and communicating with each other. As the name 1x3 one Router connected between three networks sending and receiving data accordingly.
- **PC to PC OPTICAL FIBER COMMUNICATION SYSTEM**
Final Year Degree Project.

BEHAVIORAL SKILLS /HOBBIES

Team Leader, Team Player,
Punctual, Persistent, Time
management.



Numismatics



EXPERIENCE

13/09/21

-

13/09/22

- **Field Application Engineer**
Record Tech Electronics, Roorkee
 - Calibration and Testing of various instrumentation sensors such as LVDT's, Load Cell's, Earth Pressure Cell's.
 - Pcb fabrication including printing, etching, drilling, components mounting through hole as well as SMD.
 - Reports, Leading team to complete the project assigned.
 - Test Pile Load Test Data Monitoring in MAHSR Bullet Train Project.
 - Test Pile Installation in MAHSR Bullet Train Project.
 - Manufacturing and Designing LVDT's for NHPC Kishanganga Project.

- Installation of Data Monitoring system of Pandit Deendayal Upadhyay Cable Stayed Bridge (Surat) .

ACHIEVEMENTS & AWARDS

- 6 years Class Representative (3 Years in Diploma, Degree respectively.)
- Represented my school at District Level in Football.

ACTIVITIES

- Member Of Dream Foundation Group.

LANGUAGES

- English
- Hindi
- Marathi

DECLARATION

- “I hereby declare that the details and information given above are complete and true to the best of my knowledge.”

Place: Ghaziabad

Date:

Jatin Jitendra Sharma