# Shubham Dainiwal

Design and Verification Trainee

I am electronically savvy and passionate about working in Digital domains, constantly improving the skillset required to excel in VLSI Domain. Self-Motivated, Hardworking, and Conscientiousness person who thrives in a high-pressure working environment

dainiwalshubham@gmail.com

+91-8999-544-134

Maharashtra, India

www.linkedin.com/in/shubham-dainiwal-1b41a9214

github.com/Shubhamdainiwal

## PROFESSIONAL TRAINING

Advanced Digitial Design and Verification Course, Maven Silicon, Bangalore (Present)

# **EDUCATION**

# Bachelors of Engineering in Electronics and Tele-Communication

Government College of Engineering, Amravati

08/2018 - 08/2022, CGPA: 7.66

**HSC(+2)** 

Late Jyoti Janholkar Higher Secondary School, Akola

06/2017 - 05/2018, Percentage: 77.54%

SSC(10th)

Shri Bhausaheb Potey Vidyalaya, Akot

06/2015 - 05/2016. Percentage: 92.4%

# **TECHNICAL SKILLS**

**SUBJECTS KNOWN:** Digital Electronics TBMethodology: UV M

HDL: System Verilog Verilog HVL:

**Program ming** 

C, Python

Languages:

Mentor Graphics-Questa Sim, Xilinx-ISE **EDA Tools:** 

Timing Analysis:

and Model Sim

STA

Operating Systems:

Linux, Windows

# **PROJECTS**

### Router 1x3-RTL Design and Verification

- Implemented RTL using Verilog HDL and verified RTL using System Verilog Synthesized the design
- Generated functional and code coverage for RTL Verification Signoff.
- EDA Tools: Model Sim, Quartus Prime

### **MAC Unit**

- Implemented RTL using Verilog HDL and verified RTL using System Verilog HVL.
- Generated functional and code coverage for RTL Verification Signoff.
- EDA Tools: Mentor Graphics- Questa Sim.

<ul> <li>Smart Blind Stick Using Arduino and Python</li> <li>Voice Smart Home Assistant Using NodeMCU and Python</li> </ul>			
	E	XPERIENCE	
- Intern At Persistent System 01/2022-06/2022 - Intern At MBA Electrosoft, 05/2019-06/2019			
	S	OFT SKILLS	
Time Management	Team Work Problem So		
	<u> </u>	ITERESTS	
Chess/Sudoku	Reading Books	Travelling	Badminton/Cricket
	DEC	CLARATION	
I hereby declare that all	the particulars furnished above	are true to the best of my knowled	dge.

PROJECTS