ANNA DEVARAJU

VLSI Design and Verification Trainee

ABOUT ME: Quick Self learner, having 5 years of Professional Experience in various organizations with focused in reaching the goals of a company with adaptive nature.

Contact

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Interests

Reading

Travel

Languages

Telugu	●●●●● Advanced
Hindi	●●●○○ Intermediate
English	●●●●○ Upper intermediate

Work History

2022-03 - 2023-03
Area Business Manager
Diagnocare Lifesciences Pvt Ltd, Hyderabad

2018-09 - 2022-03
Sales & Service Engineer
Tulip Diagnostics Pvt Ltd, Hyderabad, TG

2016-02 - 2017-02
US IT Recruiter
Unique Key Resources, Warangal, TG

Education

2017-08 - 2019-07
M Tech: Digital Communication
Kakatiya University - Warangal
GPA: 75

2011-08 - 2015-06
B Tech: Electronics &communication Engineering
Vaagdevi College of Engineering - Warangal
GPA: 65

2009-06 - 2011-03
Intermediate
Board of Intermediate - Hanamkonda, TG
GPA: 94

Technical Skills

HDL: Verilog

HVL: System Verilog

TB Methodology: UVM

Verification Methodologies: Constraint Random coverage Driven Verification, Assertion Based Verification-SVA

Operating System: Linux, Windows

EDA Tools: Mentor Graphics- Questa sim and Xilinx -ISE, Xilinx Viv ado, Model Sim

Soft Skills

Time management

Interpersonal Communication

Team work

Adaptability

Marketing & negotiation

Certifications

2023-02
"Star of the month" from Maven Silicon in Professional Training

2022-11
"Star of the month" from Maven Silicon in Professional Training

2022-06
"Star of the month" from Maven Silicon in professional Training

2009-05
"Grama Rathna Award" for Best Academic performance & good conduct

STA: STA Basics, Comparison with DTA, Timing Path and Constraints, Different types of clocks Clock domain and Variations, Clock Distribution Networks, Fixing timing failure

Programing Languages: C, Python Basics

Domain: ASIC/FPGA front-end Design and Verification

Protocols: AXI, AHB, UART, I2C, SPI

Scripting Languages: Perl Scripting

Tools used in Engineering: MATLAB - Digital Signal Processing Keil MDK or Arduino IDE - Microcontroller Programming MASM or TASM - Assembly Language Programming (8085 or 8086) etc. LTSpice (Spice Simulator) - Circuit analysis NS2 - Network Simulator for Wireless communication. Cadence Virtuoso - Custom IC design and package/PCB design/analysis

Projects

Router [1x3] RTL Design & Verification
The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2. Architected the block level structure for the design

- Implemented RTL using Verilog HDL.
- Architected the Class based verification environment using System Verilog.
- Verified the RTL model using System Verilog.
- Generated functional and code coverage for the RTL verification sign-off.

Date:09/03/2023
Place: Hyderabad

Anna Devaraju