Bharamu S K
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EDUCATIONAL QUALIFICATION

Year	Degree	Institution/ School	Performance
2018	B.E (Electronics and Communication Eng.)	J.S.S Academy of Technical Education Bangalore	67.5%
2015	Diploma(Electronics and Communication Eng.)	B.V.V.S Polytechnic Bagalkot	77.44%
2012	Class X	S.S.S.B.V.V.S Hi-School Halingali	82.72%

PROFESSIONAL TRAINING

- **Advance VLSI Design and Verification training.** [May'22 - Present]
  Maven Silicon Bangalore.
- **Embedded Systems Trainee**. [Sep'18 – May'19]
  Cranes varsity a Training Division of Cranes Software International Ltd Bangalore.

PROFESSIONAL SKILLS

UVM | SV | SVA | OOPS Concept | Verilog | STA | Digital Electronics | Perl | C.

TOOLS

Questasim | Modelsim | Quartus Prime |EDA Playground | Linux.

PROFESSIONAL EXPERIENCE

Senior Embedded Engineer, M.S Technology Bangalore [July'19 - Dec'22]

Provides solutions and innovation for Energy Management and communication.

Achievements/Tasks:

- To Design, Develop, Implement and test the Embedded Software and Hardware.
- Strong knowledge of communication protocol **UART**, **I2C**, **RS232**, **RS485**, **SPI**
- Designed and developed the electronic zig for testing of PCB.

Tool Expertise: **Atollic** | **Arduino** | **ESP-IDF** | **Code Compos Studio** | **Altium** | **Ki cad** | **OrCad**.

PROJECTS

UART IP Verification: [Mar'23 - Apr'23]

- The UART IP core provides serial communication capabilities, which allows communication with modem or other external devices.
- Implemented an Baudrate generation block.

Verification:

- Verified the design using UVM TB Architecture blocks i.e. Agents, Environment and Tests in QuestaSim.
- Verified the UART packet of 5,6,7,8bits. Prity and Different baudrate also verified using UVM TB.
- Verified the RTL module using Verilog TB.

Router 1x3 Design and Verification: [Jan'23 - Feb'23]

- The router accepts data packets on a single 8-bit port and routes them to one of the three output channels - channel0, channel1, and channel2.It's a 3-layered network device as per the OSI reference model of the network.
- Implemented various submodules i.e. FSM, FIFO, Register and Synchronizer using Verilog HDL.
- Implemented the Synthesizable design circuit using Quartus Prime.

Verification:

- Verified the design using UVM TB Architecture blocks i.e. Agents, Environment and Tests in QuestaSim.
- Connected the design and verification environment using interface and virtual interface.

RAM Verification Project: [Feb'23 - Mar'23]

- Designed and Verified 16x8 synchronous dual port RAM memory and single RAM Memory. The Memory model is capable of storing and retrieving 16bits of data as per address location.
- Perform write to any memory location, read from the same memory location, read data should be the same as written data
- Assert reset in between write/read operation and check for default values.
- Verified the design using functional coverage by defining covergroups and coverpoints.

Energy Meter Reading Using Wi-Fi and BLE: [Aug'19 - Aug'21]

- Designed and Developed an end node to communicate with the meter using UART and then send the data to the Gateway through Wi-Fi or BLE.
- Gateway uses the 4G / 2G module to communicate with headend system.

GAS and Water Meter: [Sep'21 - Mar'22]

- This project used to collect the water meter data and Gas meter in Real time.
- In this project we read GAS and Water Meter data using LC sensor or Reed switch. And send the data using the RS485 protocol.

Smart Lock Dual Authentication: [Jan'18 - Mar'18]

- This project aims to enhance system securities.
- We used RFID to unlock the system and 4-digit Password for the next step authentication.

HOBBIES

Cricket **I** Kabaddi **I** Cooking

LANGUAGES

Kannada **I** English **I** Hindi **I** Telugu.

DECLARATION

I, hereby declare that the information furnished above is correct to the best of my knowledge.

Date:

Place: Bangalore [Bharamu S K]