CONTACTS

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Gujarat, India

TECHNICAL SKILLS

- Digital Circuit Design
- HDL: Verilog
- HVL: System Verilog
- Assertion Based Verification
- Code/Function Coverage
- TB Methodology: UVM
- Operating System: Linux
- Programming Language: C, C++
- Interconnect Protocols: AHB, APB
- SOC Interfaces: UART, I2C, SPI

EDA TOOLS

- Intel - Quartus Prime
- Modelsim Intel FPGA Starter Edition
- Mentor Graphics - Questasim

INTERNSHIPS

Plant Training at GSECL

- In plant training at thermal power plant, which includes understanding plant operation, working and maintenance of power plant.

MAVEN SILICON
Centre of Excellence in VLSI

Sumit Jaysingh Jadon

About me

A dedicated student and an individual who works hard to achieve organizational objectives and enhances skills and knowledge from practical experiences.

PROFESSIONAL TRAINING

ADVANCED VLSI DESIGN & VERIFICATION

MAVEN SILICON | March 2022 - till date

INDUSTRIAL EXPERIENCE

Vijay Flexible Containers Pvt. Ltd.

Electronic Engineer | Nov. 2021 - Feb. 2023

- Worked on fine settings, programming & modbus communication for SPM machines along with installation, commissioning & troubleshooting.
- Research & Development of medical ICU ventilator for adult & pediatric intensive care.
- Development of various control system, logic diagram, schematic diagram, flow chart, I/O list etc. using AutoCAD electrical.

EDUCATION

- **M.E. in Electrical Power Engineering**
  Maharaja Sayajirao University of Baroda | 2019-2021
  8.46
- **B.E. in Electrical Engineering**
  Government Engineering College Dahod | 2014 - 2018
  7.53
- **H.S.C in Gujarat State Education Board**
  Sarva Vidyalaya High School, Kadi | 2014
  64%
- **S.S.C in Gujarat State Education Board**
  A.G.P High School, Ambaji | 2012
  80.8%

PROJECTS

AHB to APB Bridge - Design and Verification

- AMBA specification defines on-chip communication standard for designing high performance embedded micro-controllers
- Bridge is an interface between IPs of two different protocols. It converts one standard bus interface signals to other standard bus interface signals.
- AMBA AHB to APB Bridge acts as an interface between high performance IP's and low power peripherals.
- HDL: Verilog, HVL: System Verilog, TB Methodology: UVM

Router 1x3 - RTL Design and Verification

- Architected the block level structure for the design.
- Implemented RTL using Verilog HDL.
- Architected the class based verification environment using SystemVerilog.
- Verified the RTL model using SystemVerilog.
- Generated functional and code coverage for the RTL verification sign-off.
- Synthesized the design.
- HDL: Verilog, HVL: System Verilog, TB Methodology: UVM

Verification of Dual Port RAM

- Designed and verified dual port RAM under constrained random testbench environment using SV.

Synchronous FIFO - Design and Verification

- FIFO is used for interfacing data transfer between two systems working with same clock but with different throughput.
- FIFO is also used to avoid overflow and underflow conditions.
- Implemented and verified using Verilog.

ACHIEVEMENTS

- Maven Silicon **STAR OF THE MONTH** (July-2022 & August 2022).
- Secure (1284.06642/1800) marks in TCS national Qualifer Test.
- Qualified the Graduate Aptitude Test in Engineering (GATE).
- Participated in Vadodara International Marathon 2018.
- Participated in the 39th State Level Science-Maths Exhibition 2011.

STRENGTHS

- Adaptive
- Multitasking
- Team player
- Leadership

HOBBIES

- Playing Chess
- Adventure Activities
- Travelling

LANGUAGES

- English
- Hindi
- Gujarati

DECLARATION

I hereby declare that the above information is correct up to my knowledge and I bear the responsibility for the correctness of the above-mentioned particulars.

Date :

Place : Ambaji,Gujarat **Signature**