Technical Topics

			Verification
1	Digital systems Vs Analog systems	1	Pass by reference or pass by value
2	History of VLSI and latest trends	2	Shallow and deep copy
3	IC Design Front Back End flow	3	Constraint_mode with static constraints
4	IC Design Front End flow	4	Code coverage Vs functional coverage
5	Digital systems Vs Analog systems	5	Semaphore
6	Logic Minimization techniques using Boolean Postulates	6	UVM_factory
7	"Logic Minimization techniques using K-Map	7	Clocking block
8	Different types of adder circuits	8	Polymorphism
9	Multiplexer and their applications	9	The constraint Inheritance and Overriding
10	Encoders and decoders	10	M_sequencer vs P_sequencer
11	Latches and flipflops	11	Task body of a sequence
12	SISO Shift Registers	12	Associative array
13	SIPO shift Register	13	Explain about dynamic array and Queues
14	PISO Shift Registers	14	$cast
15	PIPO Shift registers	15	Enum datatype with example
16	Counters	16	Reporting mechanisms and its uses
17	Counter Design Techniques	17	UVM_Phases
18	Mealy Vs Moore FSM	18	What is the significance of get_next_item?
19	Glitches and Hazards	19	Difference between immediate and concurrent assertions
20	FIFO Operation and applications.	20	$rose vs @posedge
21	FIFO Depth Calculation	21	Difference between ##N and implication operators
22	Frequency division using counters	22	Advantage of assertions
23	Synchronous vs asynchronous circuits	23	How to connect transactors in SV TB
24	Why HDL's? how they are different from Software development languages like C & C++?	24	How to connect transactors in UVM TB
25	Different Abstraction Levels in Verilog	25	Virtual interface connection with static interface in SV TB
26	Data Types in Verilog	26	Virtual interface connection with static interface in UVM TB

27	Operators in Verilog	27	UVM Configuration
28	Different types of Assignments in Verilog	28	Need of Virtual sequence & Virtual sequencer
29	Tasks and functions in Verilog		
30	How to write task-based TB in Verilog?		
31	Synthesis Coding Style		
32	Verilog Coding guidelines		
33	"System Tasks and Compiler directives in Verilog		
34	FSM coding in Verilog		
35	How to write TB for FSM's using Verilog?		
36	file i/o operations in Verilog		
37	Blocking assignments		
38	Non-blocking assignments		
39	Processes in Verilog		
40	Display system tasks		
41	Random system function		
42	Synthesis issues		
43	Mealey FSM coding styles to avoid glitch		
44	Parallel blocks		
49	5 more applications of AMP		
45	Sequential blocks		
46	Operation of BJT.		
47	Ideal Characteristics of OP-AMP		
48	5 applications of OP-AMP		
50	"Kirchoff's Current Law and Voltage Law		
51	Thevenin's Theorem		
52	Norton's Theorem		
53	How to solve a wheatsone bridge?		
54	Applications of wheatstone bridge		
55	"Monostable multivibrator		
56	Bistable multivibrator		
57	Astable Multivibrator		
58	Integrator and differentiator using OP-AMP		

59	Different logic families		
60	CMOS vs TTL		
61	different kinds of feedback systems		