## Assignment 1

## **AVVARU BHARAT**

Download all latex-tikz codes from

https://github.com/Bharat437/EE5803-FPGA-LAB/tree/main/Assignment-1

## 1 Problem

Draw the Logic Circuit for the following Boolean Expression: (X' + Y).Z + W'

## 2 Explanation

First we will simplify the given Boolean expression as below, so that NAND or NOR logic gates are used for designing logic circuit.

Using De Morgan's Law

$$(\overline{X} + Y).Z + \overline{W} = (\overline{X} + \overline{Y}).Z + \overline{W}$$

$$= \overline{X.\overline{Y}.Z} + \overline{W}$$

$$= (\overline{\overline{X.\overline{Y}.Z}}) + \overline{W}$$
(2.0.1)

$$\implies \left(\overline{X} + Y\right).Z + \overline{W} = \overline{\left(\overline{X.\overline{Y}.Z}\right).W}$$
 (2.0.2)

Now we will draw logic circuit according to the above simplified expression.

