Challenge Problem 1

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Download all latex-tikz codes from

https://github.com/Bharat437/EE5803−FPGA−LAB/tree/main/Challenge−1

1 Problem

Obtain and implement an algorithm to convert any truth table to NAND logic.

2 Algorithm

1. From Truth table we will have inputs array and ouput array. Implement a for loop along the length of the ouput array.
2. Inside for loop, when output array will be equal to 1 for that index read the inputs from input array.
3. If input is 0 then take Complement of that input and if input is 1 take Normal input. Like this form all min terms.
4. Take complement of each min term which is nothing but a NAND gate operation. These are the first level of NAND gates.
5. Now pass all the outputs of first level of NAND gates through another NAND gate and obtain required output.

3 Explanation

For example the given truth table is as below

X	Y	Z	G(X,Y,Z)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Table 1: Given Truth table

From truth table (1), consider the min terms for which $G = 1$ as shown in the below table.

X	Y	Z	G	Min term
0	1	0	1	$\overline{X}.Y.\overline{Z}$
1	0	0	1	X.$\overline{Y}.\overline{Z}$
1	0	1	1	X.$\overline{Y}.Z$
1	1	1	1	X.Y.Z

Table 2: Min terms for which $G = 1$

As algorithm says, now we take the complement of the Min terms which can be implemented using NAND gates. This can be seen in the circuit figure (1) below. And pass the ouputs of all these NAND gates through another NAND gate as shown below.

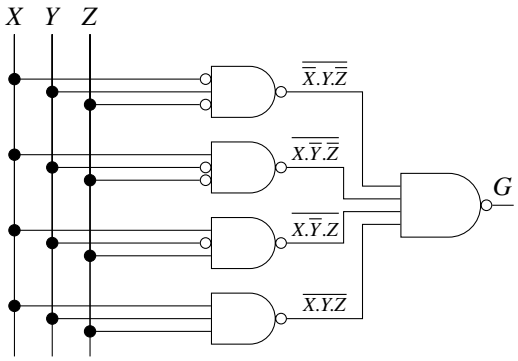

Figure 1: Logic Circuit using NAND gates

The same can be implemented using AND-OR logic i.e. SOP form is drawn as shown below.

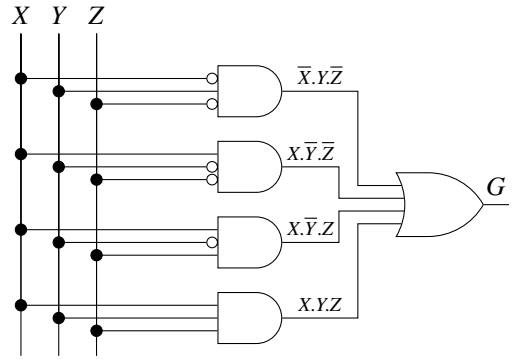

Figure 2: Logic Circuit in SOP form

4 Verification

Here we will verify whether NAND-NAND logic is equivalent to AND-OR logic or not by using De Morgan's law as below.

$$\begin{aligned}\overline{\left(\overline{X}.Y.\overline{Z}\right).\left(\overline{X.\overline{Y}.\overline{Z}}\right).\left(\overline{X.\overline{Y}.Z}\right).\left(\overline{X.Y.Z}\right)} &= \left(\overline{\overline{X}.Y.\overline{Z}}\right)+\left(\overline{\overline{X.\overline{Y}.\overline{Z}}}\right)+\left(\overline{\overline{X.\overline{Y}.Z}}\right)+\left(\overline{\overline{X.Y.Z}}\right) \\ &= \overline{X}.Y.\overline{Z}+X.\overline{Y}.\overline{Z}+X.\overline{Y}.Z+X.Y.Z\end{aligned} \tag{4.0.1}$$

5 Conclusion

From the above logic circuit figures (1) and (2) and also from 4.0.1, we can say that SOP form i.e. AND-OR logic is equivalent to NAND-NAND logic. The Verification is also done using a c code.