Assignment 1

AVVARU BHARAT

Download all latex-tikz codes from

https://github.com/Bharat437/EE5803−FPGA−LAB/tree/main/Assignment−1

1 Problem

Draw the Logic Circuit for the following Boolean Expression:
$\left(\mathbf{X}' + \mathbf{Y}\right).\mathbf{Z} + \mathbf{W}'$

2 Explanation

First we will simplify the given Boolean expression as below, so that NAND or NOR logic gates are used for designing logic circuit.
Using De Morgan's Law

$$\begin{aligned}\left(\overline{X} + Y\right).Z + \overline{W} &= \left(\overline{\overline{X}} + \overline{\overline{Y}}\right).Z + \overline{W} \\ &= \overline{\overline{X}.\overline{Y}}.Z + \overline{W} \\ &= \left(\overline{\overline{\overline{X}.\overline{\overline{Y}}.Z}}\right) + \overline{W}\end{aligned} \tag{2.0.1}$$

$$\implies \left(\overline{X} + Y\right).Z + \overline{W} = \overline{\left(\overline{\overline{\overline{X}.\overline{\overline{Y}}.Z}}\right).W} \tag{2.0.2}$$

Now we will draw logic circuit according to the above simplified expression.

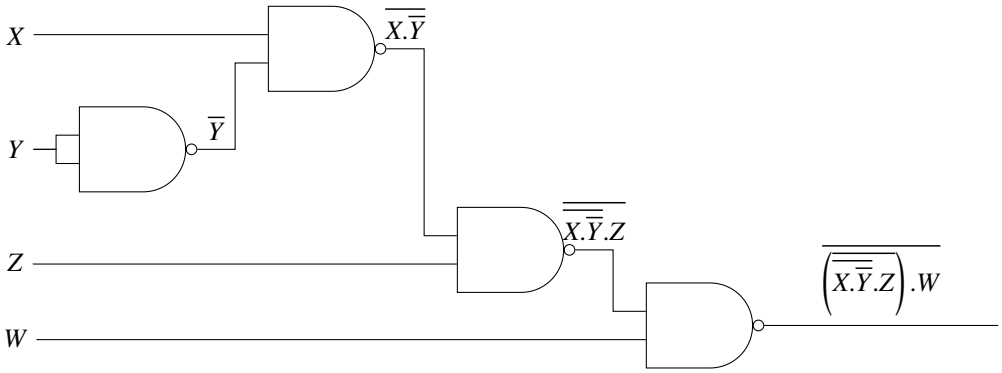

Figure 1: Logic circuit using NAND gate

X	Y	Z	W	Output
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Table 1: Truth table of above Logic circuit