VIT
Vellore Institute of Technology

Reg.No.:

Slot: B2 + TB2

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
FALL SEMESTER 2025-2026

Programme Name & Branch	: M. Tech – Embedded Systems
Course Code and Course Name	: MAEDS506 - System Design using FPGA
Faculty Name(s)	: Dr VIDHYAPATHI CM
Class Number(s)	: VL2025260105662
Date of Examination	: 18/8/25
Exam Duration	: 90 minutes Maximum Marks: 50

General instruction(s):

- **Answer All Questions**

CO1 - Develop and simulate combinational circuits using HDL and test benches.
CO2 - Develop and simulate sequential circuits using HDL and test benches.

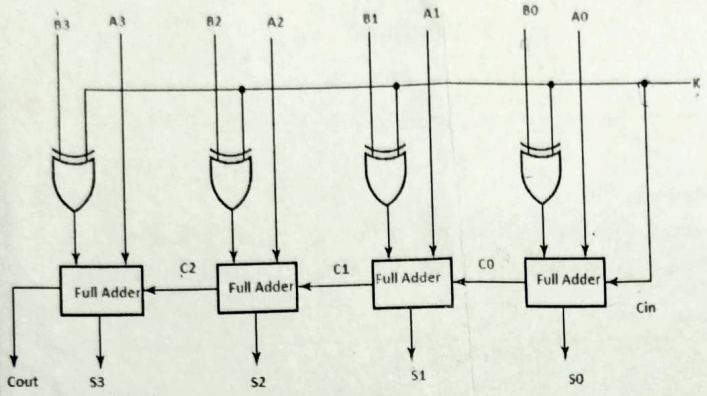
Q. No	Question	M	CO	BL
1.	Evaluate and contrast the following hardware platforms for embedded system development, considering factors such as execution methodology, performance, power efficiency, cost, ease of prototyping, time to market, and other relevant metrics. a) FPGA b) CPU c) ASIC d) GPU	10	CO1	2
2.	Discuss the following concepts in the context of system design using FPGA technology: a) The architecture of Zynq devices and the design flow for embedded systems b) The role of software reference designs and software profiling technique c) The principles of hardware-software co-design and methods for achieving hardware acceleration d) The distinction between hard-core IP and soft-core IP in FPGA-based systems	10	CO1	2
3	Develop a VHDL code and **Testbench** for an 8:1 MUX using the following modelling techniques. a) Concurrent b) Sequential	10	CO2	3
4.	Develop a VHDL code for an 4:16 Decoder using 2:4 Decoder.	10	CO1	3

VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Reg.No.:

Slot: B2 + TB2

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
FALL SEMESTER 2025-2026

5.	Develop a VHDL code to model the below 4-bit adder/subtractor circuit using Structural modelling. 	10	CO1	3

****

VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Reg.No.:

Slot: B2 + TB2

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

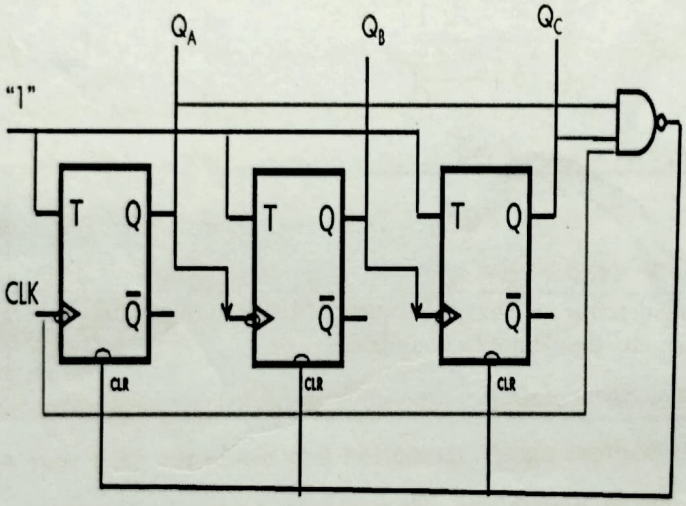
Programme Name & Branch	: M. Tech – Embedded Systems
Course Code and Course Name	: MAEDS506 - System Design using FPGA
Faculty Name(s)	: Dr VIDHYAPATHI CM
Class Number(s)	: VL2025260105662
Date of Examination	: 06/10/25
Exam Duration	: 90 minutes

Maximum Marks: 50

General instruction(s):

- **Answer All Questions**

CO2 - Develop and simulate sequential circuits using HDL and test benches.
CO3 - Build and integrate IP cores for an FPGA based system.

Q. No	Question	M	CO	BL
1.	Model a 3-bit asynchronous mod-6 up counter using VHDL and display the count value in SEVEN SEGMENT display. 	10	CO3	2
2.	Using VHDL, model a single Frequency Divider which accepts 50 MHz frequency and generates the following OUTPUT frequencies based on the INPUT selector as given in the below table.	10	CO2	2

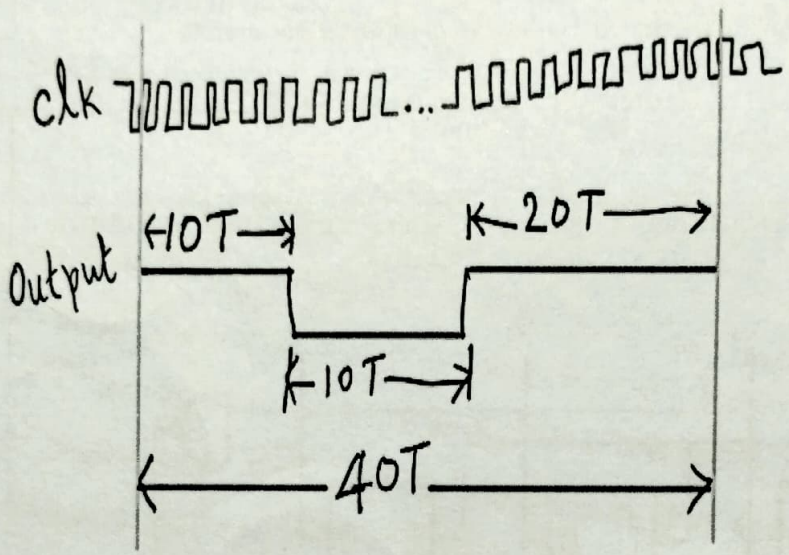
INPUT selector	OUTPUT
0	25 MHz
1	50 KHz
2	5 KHz
3	500 Hz

VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Reg.No.:

Slot: B2 + TB2

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

3	Develop a state machine for a Water Vending Machine which should accept ₹5, ₹10, ₹20 Rupee Coins/Notes and dispense 1 liter of water for ₹25 Rupee. The Vending machine should refund the extra money if any. Model the State Machine using VHDL code.	10	CO2	3
4.	Generate the following Output signal which changes only during positive edge using Finite State Machine (FSM) based VHDL programming approach. T is the basic one clock period. 	10	CO2	3
5.	Model a string detector to detect the sequence "10101" using VHDL. Note: Overlapping should not be considered.	10	CO2	3

****

T/K/TY

Reg. No: 25MES0023

Final Assessment Test – November 2025

VIT® Vellore Institute of Technology

Course: **MAEDS506 - System Design using FPGA**

Class NBR(s): **5661** Slot: **B2+TB2**

Time: **Three Hours** Max. Marks: **100**

- **KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE**
- **DON'T WRITE ANYTHING ON THE QUESTION PAPER**

COs	CO Statements
CO1	Develop and simulate combinational circuits using HDL and test benches.
CO2	Develop and simulate sequential circuits using HDL and test benches.
CO3	Build and integrate IP cores for an FPGA based system.
CO4	Apply a hardware-software co-design approach to accelerate real-world applications.
CO5	Simulate an IP-based system design using an FPGA.

BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Answer ALL Questions

(10 X 10 = 100 Marks)

1. Compare and contrast the execution models of Field Programmable Gate Arrays (FPGAs) and traditional processor-centric architectures such as CPUs and microcontrollers. Discuss how parallelism is achieved in FPGAs and how it differs from the sequential or limited parallel execution in CPUs and microcontrollers. Highlight the implications of these models on important metrics of system design. **CO4 BL3**

2. Map the embedded system design cycle onto a modern FPGA architecture. Explain how both top-down and bottom-up design methodologies are applied within this context. Highlight the advantages, challenges, and typical use cases of each approach in FPGA-based embedded system development. **CO4 BL3**

3. (i) Given the following part of VHDL code, fill in the table. **[5] CO1 BL3**

```
SIGNAL a: BIT;
SIGNAL b: BIT_VECTOR (7 DOWNTO 0);
SINGAL c: STD_LOGIC;
SIGNAL d: STD_LOGIC_VECTOR (7 DOWNTO 0);
SIGNAL e: INTEGER RANGE 0 TO 7;
```

OPERATION	Legal/Illegal
e<=d;	
d(0) <= c;	
a<=b(5);	
b<=d;	
b(0)<=a;	

(ii) Tabulate the differences between WHEN and CASE. **[5]**

4. Model the carry ripple adder given in Fig.1. in VHDL with the following style **CO1 BL3**

   a) Using **loop** VHDL construct **[5]**

   b) Using **generate** VHDL construct **[5]**

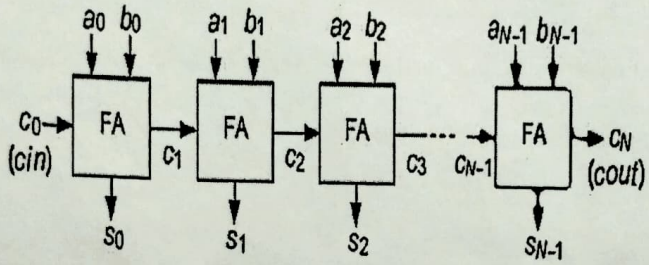
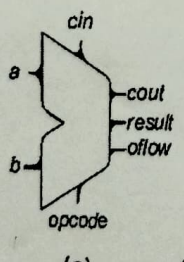


Fig.1. Carry Ripple adder

5. Develop a VHDL code to model a 64-bit Arithmetic and Logical Unit(ALU) as shown in Fig.2. **CO1 BL4**



(a) (b)

Unit	opcode	Instruction	result
Logic	0000	Complement *a*	not *a*
	0001	Complement *b*	not *b*
	0010	Logic and	*a* and *b*
	0011	Logic or	*a* or *b*
	0100	Logic nand	*a* nand *b*
	0101	Logic nor	*a* nor *b*
	0110	Logic xor	*a* xor *b*
	0111	Logic xnor	*a* xnor *b*
Arithmetic	1000	Transfer *a*	*a*
	1001	Transfer *b*	*b*
	1010	Increment *a*	*a* + 1
	1011	Increment *b*	*b* + 1
	1100	Decrement *a*	*a* – 1
	1101	Decrement *b*	*b* – 1
	1110	Add *a* and *b*	*a* + *b*
	1111	Add *a* and *b* with carry	*a* + *b* + *cin*

Fig.2. ALU

6. Write a Structural VHDL code to model Tapped delay line given below in Fig.3. **CO2** **BL4**

Note: 4-Stage SR means 4-bit SHIFT REGISTER.

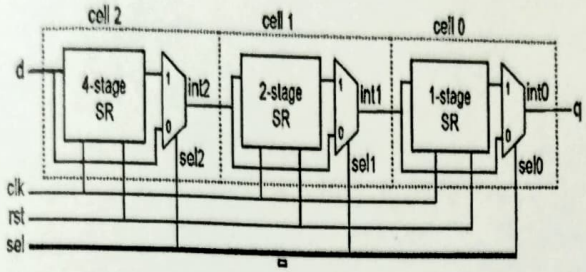
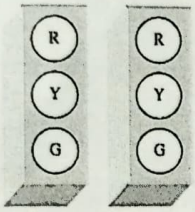


Fig.3. Tapped delay

7.(a) Develop a VHDL code to model the given Traffic Light Controller in Fig.4. **CO4** **BL4**

Assume the clock frequency is 60 Hz.



State	Operation Mode		
	REGULAR	TEST	STANDBY
	Time	Time	Time
RG	timeRG (30s)	timeTEST (1s)	—
RY	timeRY (5s)	timeTEST (1s)	—
GR	timeGR (45s)	timeTEST (1s)	—
YR	timeYR (5s)	timeTEST (1s)	—
YY	---	---	Indefinite

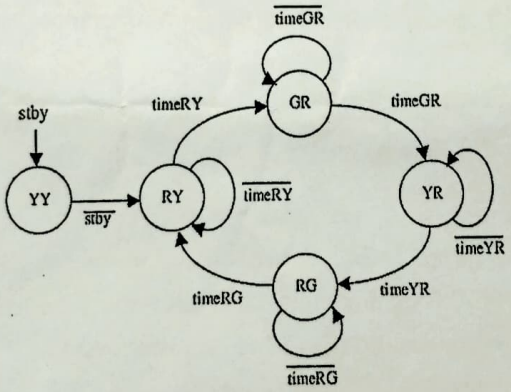


Fig.4. Traffic Light Controller

OR

7.(b) Develop a VHDL code to generate the following **outp** waveform given in Fig.5. **CO4** **BL4**

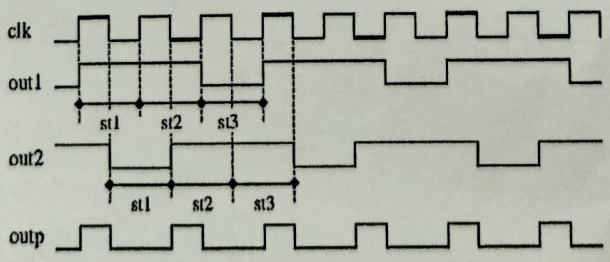


Fig.5. outp waveform

8.(a) Develop a VHDL code to implement a progressive 2-digit decimal counter (0 → 99 →0), with external asynchronous reset. Also map the binary coded decimal (BCD) output to seven segment display (SSD). CO4 BL4

OR

8.(b) Generate the following Output signal as shown in Fig.6 using Finite State Machine (FSM) based VHDL programming approach where T0 is the basic one clock period. Assume the clock frequency is 1 Hz and map the output to an LED. CO4 BL4

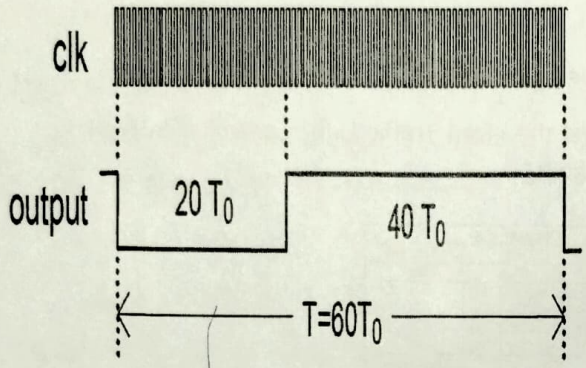


Fig.6. output waveform

9. (i) Explain the concept of Hardware acceleration and Partial Reconfiguration in FPGA design. [5] CO5 BL3

(ii) Explain the roles of bitstream encryption and tamper detection mechanisms in protecting FPGA-based systems from unauthorized access and physical attacks. [5]

10. Assume a design in which it has a mixed FPGA + ARM SoC system where custom hardware logic in the FPGA Programmable Logic (PL) must be controlled and accessed by software running on the ARM Processing System (PS). The communication is to be handled via AXI interconnects. CO3 BL3

(i) Describe the role and types of AXI interfaces (AXI4, AXI4-Lite, AXI4-Stream) in such a system.

(ii) Outline how to package a custom IP (hardware module) so that it can be accessed via AXI from the ARM side (i.e. how to wrap your logic). What are the key interface signals and metadata attributes needed?

⇔⇔⇔ T/K/TY⇔⇔⇔