VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

School of Electronics Engineering
CONTINUOUS ASSESSMENT TEST - 1
FALL SEMESTER 2025-2026

SLOT: A2+TA2+TAA2

Programme Name & Branch	:M.Tech Embedded Systems
Course Code and Course Name	: MAEDS501 - Embedded System Design
Faculty Name(s)	: Dr.S.Sundar
Class Number(s)	: VL2025260105663
Date of Examination	: 17/8/2025
Exam Duration	: 90 minutes

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes:
  CO1- Develop a typical embedded system using different modelling approaches
  CO2- Select the appropriate processors and memory architecture

Q. No	Question	M	CO	BL
1.	(i)Discuss in detail about the differences between general computing and Embedded computing (6marks) (ii) What are all the desirable features and general characteristics of Embedded systems? (4 Marks)	10	1	2
2.	Discuss about Embedded Product Development Life Cycle (EDLC)	10	1	2
3.	Design an automatic tea/coffee vending machine based on FSM model for the following requirement. • The tea/coffee vending is initiated by user inserting a 5-rupee coin. • After inserting the coin, the user can either select 'Coffee' or 'Tea' or press 'Cancel' to cancel the order and take back the coin.	10	1	3
4.	An Embedded system employs RAM chips of 16K x 8 and ROM chips of 32K x 8. The system needs 64K x 16 bytes of RAM, 128K x 16 bytes of ROM, Discuss the following: a. How many RAM and ROM chips are needed to implement this design? b. Draw a memory-address map for the system and the interfacing diagram.	10	2	3
5.	(i)Given 32bit data and 32-bit address in a direct mapped cache, find how many total bits are required for a cache with 64kB of data? (5 Marks) (ii) Assume for Direct Mapped Cache, find out the total miss and hits for the scenario below (5 Marks)	10	2	3

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TAA2

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CONTINUOUS ASSESSMENT TEST - 1

FALL SEMESTER 2025-2026

Memory		Cache (N = 5)		
			Address	Data
20	7	0	30 25	76 78
21	3	1	31 26	98 59
22	27	2		
23	32	3	25 28	56 56
24	101	4		
25	78			
26	59			
27	24			
28	56			
29	87			
30	36			
31	98			

Processor

1. Read 30
2. Read 31
3. Read 30
4. Read 26
5. Read 25
6. Read 28
7. Read 23
8. Read 25
9. Read 28

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SLOT: A2+TA2+TAA2

School of Electronics Engineering
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

Programme Name & Branch	:M.Tech Embedded Systems
Course Code and Course Name	: MAEDS501 - Embedded System Design
Faculty Name(s)	: Dr.S.Sundar
Class Number(s)	: VL2025260105663
Date of Examination	: 5/10/2025
Exam Duration	: 90 minutes

Maximum Marks: 50

General Instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 - Remember, 2 - Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes:
  CO1- Develop a typical embedded system using different modelling approaches
  CO3- Compare various wired and wireless protocols.
  CO4-Apply the concepts of RTOS for developing real-time embedded systems.

Q. No	Question	M	CO	BL
1.	Assume there are three actors (Passenger, admin, and Bank) for an airline reservation system. Develop an UML model for this system which represents different use cases (with include and extend relationships).	10	1	3
2.	Given below are the arrival and burst times of four processes P1, P2, P3 and P4. Draw the Gantt Chart using SJF pre-emptive and SJF non-pre-emptive Process / Arrival Time(msec) / Execution Time(msec) P1 / 0 / 8 P2 / 1 / 4 P3 / 2 / 9 P4 / 3 / 5 Calculate the average waiting time and average turnaround time.	10	4	3
3.	An industrial automation system uses multiple high-speed sensors connected to a central controller via serially. Propose and Design and a communication strategy that ensures data integrity, avoids bus contention, and supports future scalability. Justify your design choices.	10	3	3
4.	(i) A printing system has 3 printers shared among multiple users. Each user submits a print job that must wait until a printer is free. Discuss in detail about the solution to manage access the printer [5 Marks] (ii) In a hospital monitoring system, patient vitals are tracked in real-time. Multiple sensors feed data to a central dashboard. How do you ensure smooth multitasking and data integrity? [5 Marks]	10	4	3

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CONTINUOUS ASSESSMENT TEST - II

FALL SEMESTER 2025-2026

SLOT: A2+TA2+TAA2

5.	In a hospital management system, multiple medical devices (ECG, blood pressure monitors, ventilators) send status updates to a central monitoring server. The updates are not sent directly to a particular server thread but are stored in a shared communication area until a monitoring thread retrieves them. a) Identify which IPC mechanism (Mailbox, Queue, or Pipe) best suits this system. b) Justify your choice, comparing it with at least one other IPC method. c) How would the system handle the scenario where the mailbox/queue/pipe is full, but devices continue to send updates?	10	4	3

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Reg. No: 25MES0023

R/K/TY

Final Assessment Test – November 2025

VIT® Vellore Institute of Technology

Course: MAEDS501 - Embedded System Design

Class NBR(s): 5663

Slot: A2+TA2+TAA2

Time: Three Hours

Max. Marks: 100

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

COs	CO Statements
CO1	Develop a typical embedded system using different modelling approaches.
CO2	Select the appropriate processors and memory architecture.
CO3	Compare various wired and wireless protocols.
CO4	Apply the concepts of RTOS for developing real-time embedded systems.
CO5	Identify the need for hardware/software co-design approach for embedded system design.

BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Answer ALL Questions

(10 X 10 = 100 Marks)

1. Design an embedded system for a driver and passenger seat belt warning mechanism in an automotive application using a Finite State Machine (FSM) model. The system must fulfil the following functional requirements: **CO1 BL3**

   - When the vehicle ignition is turned on and the seat belt is not fastened within 10 seconds of ignition ON, the system generates an alarm signal for 5 seconds.
   - The Alarm is turned off when the alarm time (5 seconds) expires or if the driver/passenger fastens the belt or if the ignition switch is turned off, whichever happens first.

   Additionally, model the timer subsystem as a separate FSM, capturing its internal states and transitions.

2.(a) Let there are three actors (operator, customer, and Bank) of a cash dispenser or ATM. Develop an UML case diagram for this scenario with include and extend relationships. **CO1 BL3**

OR

2.(b) Let there be two producers (P1 and P2) and two consumers (C1 and C2), where consumer C1 has higher priority than consumer C2. Discuss how to construct a Petrinet model for this producer consumer system that incorporates the priority constraint. **CO1 BL3**

3.(a) A processor takes 100 ns to access the main memory. With cache memory in place, it takes only 20 ns for a cache hit, but a cache miss still results in a 100 ns main memory access. If the cache hit ratio is 90%, calculate the effective memory access time. Explain the impact of cache hit ratio on system performance and suggest two ways to improve cache efficiency. CO2 BL3

OR

3.(b) A processor based embedded system has 2 GB of Virtual memory. It has 8 MB of Main Memory. Considering a page size of 2 KB, Compute: CO2 BL3

i) The number of pages in Virtual and Main memory

ii) The size of the Page table

iii) Assuming a TLB size which contains 2048 pages, calculate the total size of TLB.

4. An embedded system has to be designed for 1024 × 8 - bit RAM using 256 × 8 - bit RAM Chips. For this design: CO2 BL3

(a) Compute total number of decoders those are needed for the system?

(b) Design a memory-address map for the system and

(c) Show the chip layout for the above design.

5. Describe the step-by-step process of data transmission in the I^2C protocol. Explain how a single master can communicate with multiple slave devices? And how multiple masters can share control over multiple slaves. Support your explanation with relevant diagrams and examples. CO3 BL2

6. Modern embedded and automotive systems often rely on robust communication protocols to ensure reliability and real-time performance. Explain how the CAN protocol addresses these needs. Illustrate the structure of a CAN data frame and discuss the significance of its various frame fields. CO3 BL2

7. A real-time embedded system must schedule the following periodic tasks: CO4 BL3

Task	Execution Time (C)	Period (T)
T1	1 ms	4 ms
T2	2 ms	5 ms
T3	3 ms	20 ms

Draw Gantt charts for the first 20 ms schedule under both RMS and EDF and analyse the differences in task execution and response.

8.	Discuss the concept of priority inversion in the context of real-time systems. Elaborate on how the Priority Ceiling Protocol (PCP) mitigates this issue. Use the following scenario to support your explanation: Four tasks T1, T2, T3, and T4 are scheduled with descending priority levels (T1 being the highest, T4 the lowest). Tasks T1 and T3 share access to resource R1, while tasks T2 and T4 share access to resource R2. Analyse how priority inversion could occur in this setup and demonstrate how PCP would prevent it.	CO4	BL3
9.	Discuss the advantages of adopting hardware/software co-design methodology in embedded systems. How does this approach differ from the conventional design flow?	CO5	BL2
10.	Provide a real-world example where hardware-software co-design is applied and explain the hardware-software partitioning.	CO5	BL3

⇔⇔⇔ R/K/TY⇔⇔⇔