Asynchronous FIFO Implementation Using FPGA

Yanjun Zhang[1,2],Chunli Yi[1] and Jinqi Wang[1]
[1] Key Laboratory of Instrumentation Science & Dynamic Measurement(North University of China)
[2] Ministry of Education and Science Technology on Electronic Test & Measurement Laboratory
North University of China
Taiyuan, Shanxi Province, China
zhangyanjun@nuc.edu.cn, yichunli1026@yeah.net
wangjinqi_0925@163.com

Jinye Zhang
Jin xi industrial group technology center
Taiyuan, Shanxi Province, China
shanxi_jinye@163.com

***Abstract*—We introduce a design of asynchronous FIFO on FPGA for the purpose of high-speed, steady data transmission between asynchronous clock domains. In the design , the memory address was organized into one ring list , using gray code as its address code, making uses of double jump technology to finish two asynchronous clock regions between address signals transmission, avoiding the meta-stability well.**

Keywords-FPGA; asynchronous FIFO; grey code; double jump technology

I. INTRODUCTION

With the development of integrated circuit technology, the scale of circuit design is increasing rapidly and the system clock is also used more and more often. Including the handling of many asynchronous clocks, they will cause conflict quasi-steady signals, which may lead to the design function of the system failure. Therefore, treatment of asynchronous clock has been difficulties in circuit design[1].There are many solutions to this problem, such as the phase control method, double jump technology. However, these methods are low efficiency, the best approach is to use asynchronous clock asynchronous FIFO, which passes signals between the clock regions is more flexible and commonly used in the standard bus interface to transfer data between the memory read and write burst. In this paper, we introduce a high-speed asynchronous FIFO method within the FPGA, according to the excellent control logic of FPGA, and low power consumption, high reliability, reconfigurability, short development cycle and lower development costs and so on[2]. The method is suitable for high frequency data acquisition system, such as video image acquisition pretreatment systems.

II. THE DESIGN OF ASYNCHRONOUS FIFO

We construct the FIFO in the FPGA using dual-port RAM. In the design, the difficult is to generate the empty and full flag, because the flag of input control is due to output, similarly the flag of output control is usually generated by input. Therefore, both the write address and read address must be re-synchronized when transfer to another area. Below is a simplified diagram of asynchronous FIFO. Including the following modules: dual-port ram, write and read address generator, Gray code counter and flag generation unit.

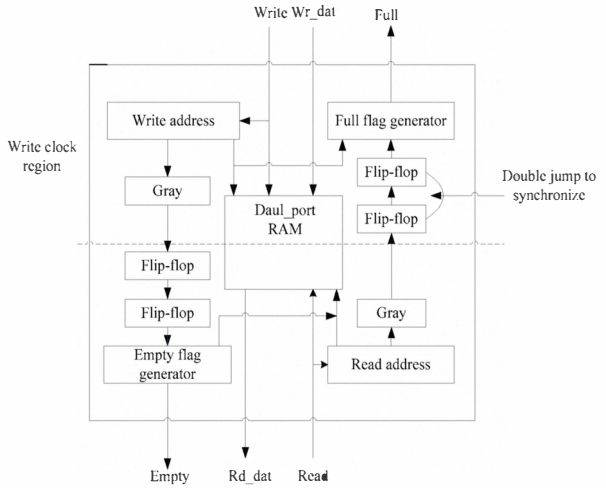

Figure 1. Simplified asynchronous FIFO

A. *Dual_port RAM*

Xilinx's Virtex and SpartanII series FPGA chip are integrated with "Select + Block RAM (block RAM), it can be configured into a real dual-port RAM. Therefore, select the block RAMB_S4_S4 as the storage body, the dual-port RAM's two ports A, B completely independent read and write clock frequency up to 100MHz, is not only fast and simple design. in the design, configure a port A write port, another port B configured as a read port, and then block the RAMB_S8_S8 connecting pin can be configured as a storage capacity of 512-byte in the FIFO, the FPGA to control the read and write its address and clock signals.

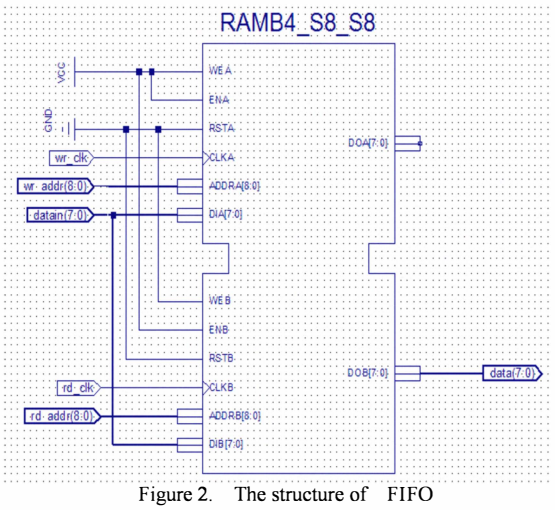

Figure 2. The structure of FIFO

B. *State Logic Module*

State logic module task is to provide FIFO empty and full flag signal, this signal tells the external circuit FIFO has reached a critical condition: if there is full signal, then the FIFO write operation for the critical state, that there is no space to store more data; if there is an empty signal, the FIFO read operation for the critical state that no more data FIFO can be read. So empty, FIFO full signal is a very important role to play, read and write it in order to achieve their own independent operation and management of obstructive data storage. We can list the memory organized into a ring, shown in Figure 3, for the empty or full of signs can be read, write, to get the relative position of the address.

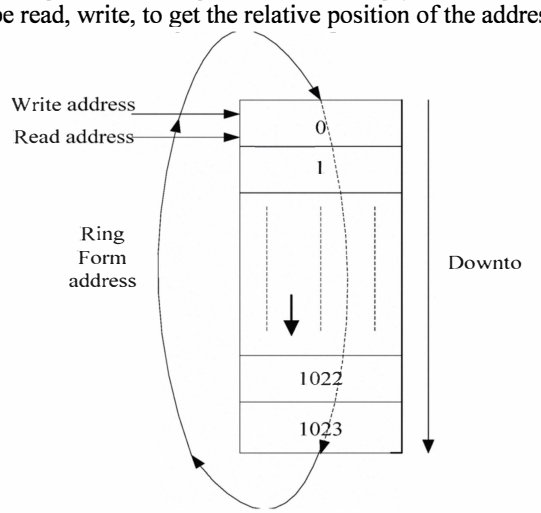

Figure 3. Ring address

System reset, read, write addresses are 0, which is FIFO empty status, not allowed to read. To the F IFO reading and writing data in the process, read, write, change of address was increasing, if the write address and read address difference is greater than 1 or more to be read until FIFO empty so far; the same token, if you write address and read address difference is greater than 1 or more to write, until the FIFO is full. Because memory is organized into a ring form, so when writing the address or read address 1023, the next read, write operation, read, write, will jump to address 0, this work ways are used to describe the structure of the unsigned critical state is very suitable.

C. Gray Counter

FPGA chip is the input and output modules (Input / Output Block, IOB), can be configured module (Configurable Logic Block, CLB) and programmable connection resources (Programmable Interconnect Array, PIA) 3 modules to form. PIA is located between the chip's logic blocks, underwent programmed into a network connection, internal logic for the connection between the chip and transfer information between them. As input to the logical block address the alignment may be different, so each bit of the address change counter can not be completely synchronized, the address data may be in a period of instability. If the asynchronous clock is just the address in the address instability in the comparison when sampling, then it may output the wrong result. Therefore, the design refers to Gray code, Gray code is only one among the adjacent count encoding changes, the address counter with a Gray code can be done to eliminate fuzziness in the circuit, so as to solve the above problems, and its implementation block diagram is shown below.

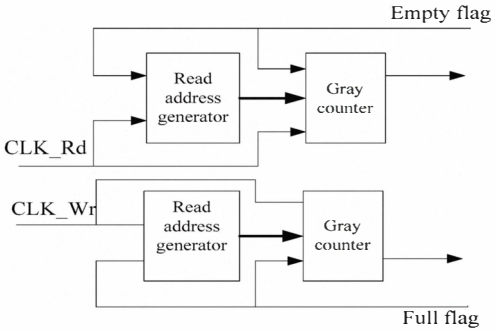

Figure 4. Conversion figure

Gray code can be achieved with a binary counter, which counts the clock the clock with the same binary, Gray code read address counter with a read clock CLK_Rd, write the address of the Gray code used to write the clock CLK_Wr; data input binary data of two adjacent Duanyou bit different or produce: Dgi = Db (i) XOR Db (i + 1). Here "Dg" said Gray code, "Db" said binary code, i on behalf of the counter digits. Read, write address generator and the Gray code transformation, shift, respectively, by empty and full flag control. When generating an empty flag to prohibit the read address generator and Gray code conversion, the shift operation; Similarly, when the full flag is generated to prohibit write address generator and Gray code conversion, the shift operation.

D. Synchronization Designs

In Figure 1, the use of write address and read address generating empty and full flag, the address must be passed to another clock in the region, but also to ensure that the address of the synchronization. During a number of addresses in the re-synchronization problems may occur, some other bits may be delayed a bit clock cycle, depending on the propagation characteristics of each respective lead. In other words, due to the asynchronous nature of the two clock

regions are likely to sample some of the first rising edge of the clock is captured, the other may be the next rising clock is captured, depending on whether the data to the first flip-flop before the arrival of the clock edge, After sufficient setup time and hold time. We use technology to complete the double jump between the regions address the two asynchronous clock signal transmission, and its schematic diagram is shown below.

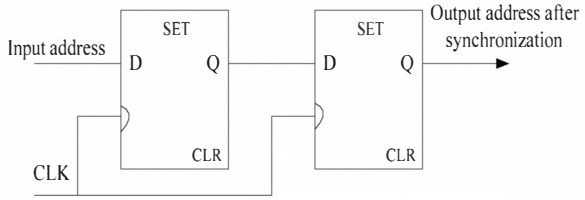

Figure 5. Double jump technical principle diagram

III. CONCLUSION

This paper presents a FPGA asynchronous FIFO using the method detailed in the empty, full signal generation, the use of Gray code to encode the address of the reading and writing, using technology to complete the double jump between the regions address the two asynchronous clock signals transmission. Click here to asynchronous FIFO design software simulation and hardware implementation have been validated by, and applied to practical circuit. Practice has proved that with this design of asynchronous F IFO high speed, small size, empty full status flags and reliability.

ACKNOWLEDGMENT

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