RECONFIGURABLE COMPUTING

PROJECT-1

NAME OF STUDENTS:

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OBJECTIVE:

Our objective was to build an FPGA based bank vault safety controller that has a safe inside for its customers to put their valuables.

VAULT MODULE:

To open the bank vault, authentication is required from the critical stakeholders along with security personnel. This is the first level of protection built as part of our project to build a robust safety system. Various cases as per the bank timings to open the vault are as follows:

1) During banking hours, the vault can only be opened if either President or VP has given authorization along with a guard.
2) During non-banking hours, the vault can be opened if either President or both VPs have given authorization along with a guard.

Programming done based on the above conditions makes our first authentication module.

The pins assigned are as follows:

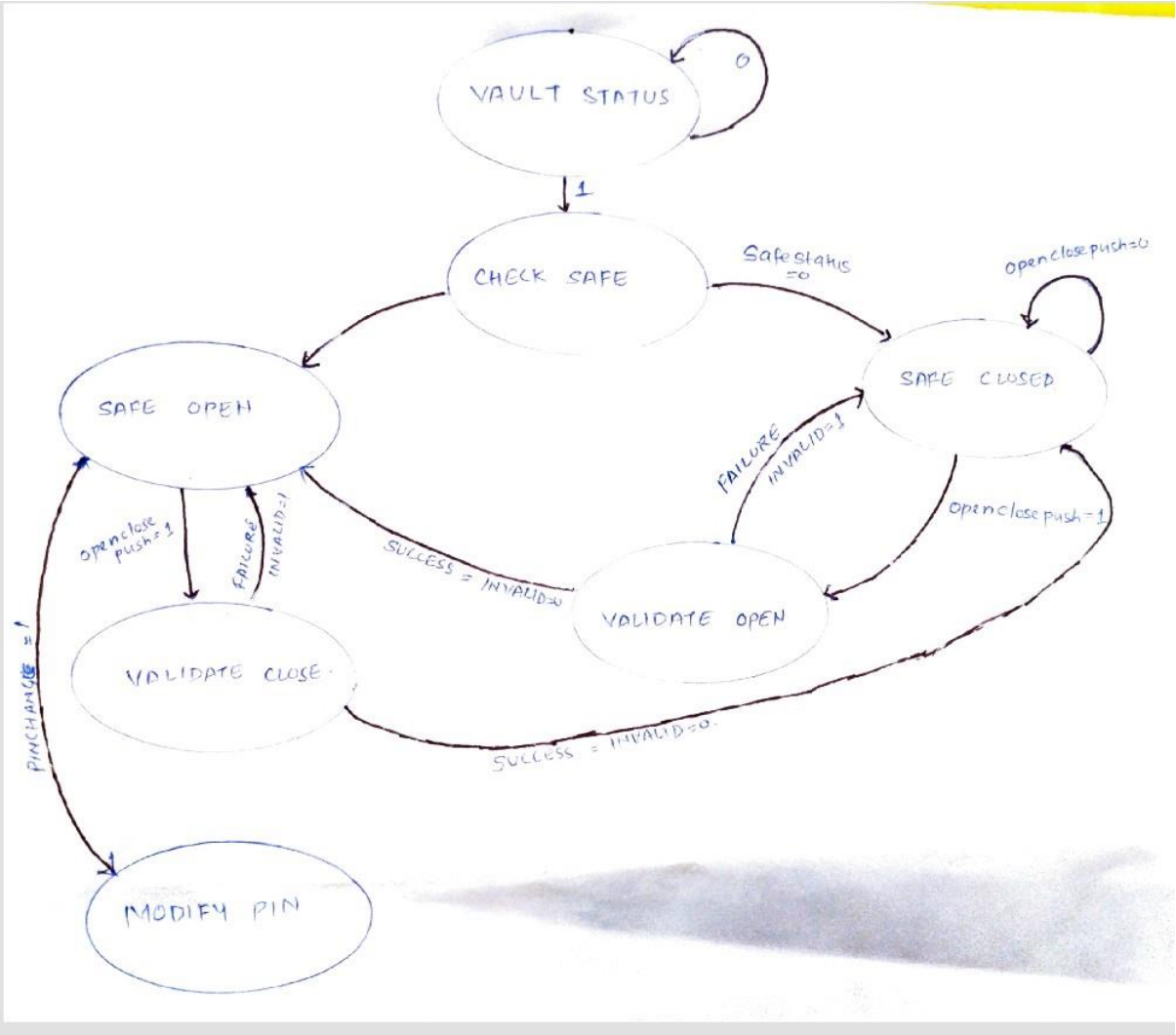
1) Guard: H19
2) VP1 Authentication: H18
3) VP2 Authentication: H17
4) President Authentication: M15
5) BankTiming: Input through VIO
6) VaultStatus: Output on VIO

SAFE MODULE:

So once the vault is open, next comes our safe module. The safe module is designed based on below mentioned conditions:

1) The customer can open the safe after entering the correct password only. Once the password is entered, the customer has to press an assigned open/close push button to unlock the safe.
2) If anyone tries to open the safe without entering the password, an LED will light up, indicating an invalid state.
3) Once the customer opens the safe after entering the correct password, the safe status indicates it as open, shown by an LED.
4) The customer also has the provision to change the password while the safe is open using an assigned change password push button. The changed password is displayed on the VIO window.
5) To enhance the safety standards, the customer can close the safe only if all the switches assigned to enter the password are reset. If a customer tries to close the safe without resetting, an LED indicating an invalid state lights up.
6) Closing the safe can be done using the same open/close push button.

Based on the above conditions, we have built an FSM with seven states. The state diagram is as follows:



PIN CONFIGURATION:

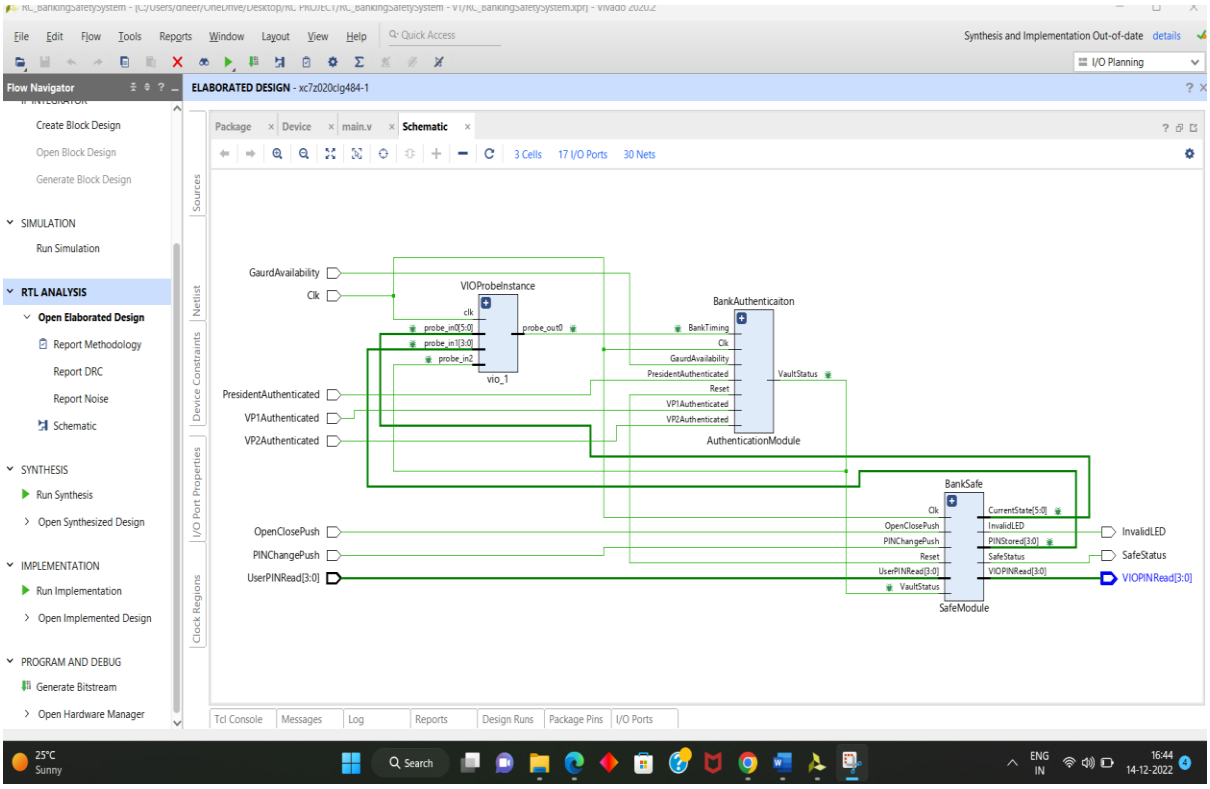
1) Clock: Y9
2) OpenClosePush: T18
3) PINChangePush: R16
4) UserPINRead [3:0]: F21,H22,G22,F22
5) VIOPINRead [3:0] : U21,U22,T21,T22
6) InvalidLED: U14
7) SafeStatus: U19

MAIN MODULE:

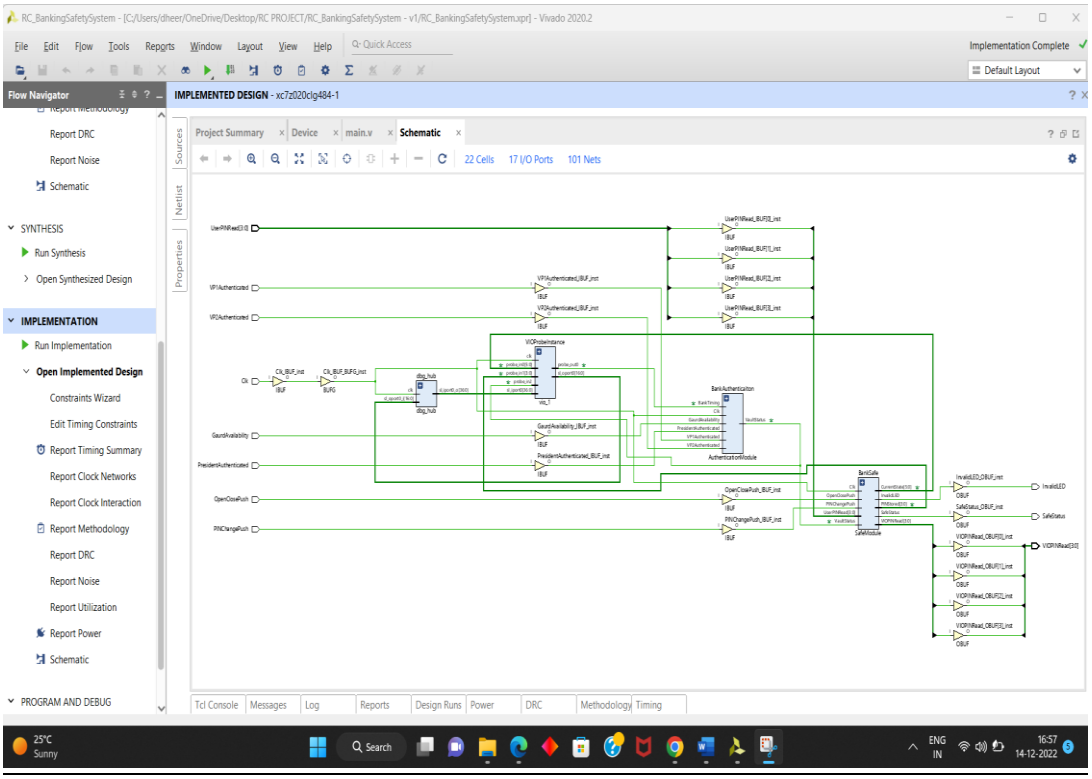
In the main module, we have instantiated above mentioned modules along with the VIO module that we have used here as an additional input/output. The main modules contain all the inputs we require from the board, mentioned exclusively as inputs and outputs, while those inputs/outputs taken from VIO are mentioned as wires.

The Elaborate design, implementation Design and utilisation status are as follows:

1) <u>Elaborate design:</u>



2) <u>Implementation Schematic:</u>



3) Utilization Report: