18CSC203J - COMPUTER ORGANIZATION AND ARCHITECTURE

1. A source program is usually in \_\_\_\_\_\_\_[L1]  
   a) Assembly language  
   b) Machine level language  
   c) High-level language  
   d) Natural language
2. \_\_\_\_\_\_ bus structure is usually used to connect I/O devices. [L1]  
   a) Single bus  
   b) Multiple bus  
   c) Star bus  
   d) Rambus
3. The decoded instruction is stored in \_\_\_\_\_\_[L1]  
   a) IR  
   b) PC  
   c) Registers  
   d) MDR
4. The registers, ALU and the interconnection between them are collectively called as [L1]  
   a) process route  
   b) information trail  
   c) information path  
   d) data path

5. When Performing a looping operation, the instruction gets stored in the \_\_\_\_\_\_[L1]

a) Registers

b) Cache

c) System Heap

d) System stack

6. To reduce the memory access time we generally make use of \_\_\_\_\_\_[L1]

a) Heaps

b) Higher capacity RAM’s

c) SDRAM’s

d) Cache’s

7. The time delay between two successive initiations of memory operation \_\_\_\_\_\_\_[L1]

a) Memory access time

b) Memory search time

c) Memory cycle time

d) Instruction delay

8. During the execution of a program which gets initialized first? [L1]

a) MDR

b) IR

c) PC

d) MAR

9. The internal components of the processor are connected by \_\_\_\_\_\_\_[L1]

a)Processor intra-connectivity circuitry

b)Processor bus

c)Memory bus

d) Rambus

10. In multiple Bus organisation, the registers are collectively placed and referred as [L1]

a) Set registers

b) Register file

c) Register Block

d) Map registers

12. When Performing a looping operation, the instruction gets stored in the \_\_\_\_\_\_[L1]

a) Registers

b) Cache

c) System Heap

d) System stack

13. By using which technique instruction set complexity can be reduced. [L1]

a)RISC

b)CISC

c)Compiler

d)clock rate

14. Which technique helps multiple instructions overlapped in execution[L1]

a) Pipeline

b) instruction execution

c) MAR

d) DMA

1. Which of the register/s of the processor is/are connected to Memory Bus? [L1]  
   a) PC  
   b) MAR  
   c) IR  
   d) Both PC and MAR
2. To reduce the memory access time we generally make use of \_\_\_\_\_\_[L1]  
   a) Heaps  
   b) Higher capacity RAM’s  
   c) SDRAM’s  
   d) Cache’s

17. Direct addressing mode is also called as [L1]

a).Absolute Mode

b). Immediate mode

c). Register mode

d). Relative mode

18. Which is used as part of the primary memory to store some fixed data that cannot be changed. [CLO1,L1]

a)RAM b)ROM c)Magnetic disk d)Flash memory

19. \_\_\_\_\_\_\_\_\_\_permits the CPU to perform memory load and store operation in a single clock cycle[L1]

(A)Cache memory

(B)Main Memory

(C)Secondary Memory

(D) Virtual Memory

20. What is the content of Stack Pointer (SP)?[L1]

(A) Address of the current instruction

(B) Address of the next instruction

(C) Address of the top element of the stack

(D) Size of the stack.

22. Lower byte addresses are used for the most significant bytes of the word

are used in which technique. [L1]

a)big endian b)little endian

c) addressing mode d)location register

22.  Program counter \_\_\_\_\_ [CLO1,L1]

a) Counts the total number of instructions present in a program.

b) Points to the current instruction that is being executed.

c) Points to the next instruction that is to be executed.

d) Stores the data of the current instruction that is being executed

23. Normal execution of programs may be preempted how it may be represented in

computer organization and architecture. [L1]

a) Interrupt b) instruction execution

c) MAR d) MDR

24. Content of the program counter is added to the address part of the instruction in order to obtain the effective address is called.[L1]

(A) relative address mode. (B) index addressing mode.

(C) register mode. (D) implied mode.

25 Which of the following is true? [CLO1,L1]

a) Central Processing Unit (CPU) consists of Control Unit, Arithmetic Logic Unit (ALU) and Primary Memory.

b)There are broadly two types of memory, primary memory and secondary memory.

c) The arithmetic and logic operations are performed in the control unit.

d) Control Unit is a part of main memory.

26. Two registers are initialized as R1=30 and R2 = 25. The instruction ADD R1, R2 is in memory location 2018H. If the size of an instruction is 4 byte, then after the execution of the instruction the value of PC, R1 and R2 will be. [CLO1,L2]

a) PC = 2018H, R1 = 55, R2 =25

b)PC = 2018H, R1 = 55, R2 =00

c) PC = 201CH, R1 = 55, R2 =00

d) PC = 201CH, R1 = 55, R2 =25

1. The special purpose registers[CLO1,L1]
2. MDR, Accumulator
3. MAR ,Accumulator
4. Accumulator, Instruction Register
5. MAR, MDR
6. Computer buses used to communicate with memory and I/O…. Which of the following is false statement? [CLO1,L1]
7. Uses 2 separate buses, one for memory and other for I/O
8. Uses one common bus for both memory and I/O,but separate control lines for memory and I/O
9. Use one common bus for control line but separate address bus for memory and I/O.
10. Use one common bus for memory and I/O with common control lines.
11. I/O interface is connected between[CLO1,L1]
12. Processor and I/O devices
13. Processor and memory
14. Memory and IO devices
15. Input and Output devices

30 \_\_\_\_\_\_ is issued to activate the peripheral and inform it what to do[CLO1,L1]

a. Control Command

b. Status Command

c. Input Command

d. Output Command

31. \_\_\_\_\_ causes the IO interface to receive data from the peripheral and places it in its buffer register[CLO1,L1]

a. Control Command

b. Status Command

c. Input Command

d. Output Command

32. \_\_\_\_\_\_ causes the IO interface to respond by transferring data from the bus into one of its register[CLO1,L1]

a. Control Command

b. Status Command

c. Input Command

d. Output Command

33. It synchronizes the data flow and supervises the transfer between peripheral and processor

a. memory interface[CLO1,L1]

b. I/O interface

c. I/O bus

b. Peripheral controller

34. The function of address decoder of I/O interface[CLO1,L1]

a. to identify the I/O device

b. to control the I/O device

c. to identify the status of I/O device

d. to activate the address bus

35. The data transfer rate of peripheral is \_\_\_\_\_\_ transfer rate of CPU[CLO1,L1]

a. Slower than

b. faster than

c.equal to

d. average of

36. A bus is a [CLO1,L1]

a. bunch of wires used to carry address.

b. bunch of wires used to carry address and data.

c. bunch of wires used to carry address ,data and control bits.

d. bunch of wires used to carry only data

37. ARM is a [CLO1,L1]

a. 16-bit microprocessor

b. 32-bit and 64-bit RISC multi-core processor

c. 64-bit microprocessor

d. 32-bit and 64-bit CISC multi-core processor

38. Three subfamilies within ARM cortex family are[CLO1,L1]

a. ARM Cortex Ax,Rx,Mx series

b. ARM Cortex Ax,Sx,Cx series

c. ARM Cortex Ax,Bx,Cx series

d. ARM Cortex Ax,Rx,Dx series

39. RISC instruction operates on[CLO1,L1]

a. operands present in processor register

b. operands present in memory

c. one operand in register and one operand in memory

d. operands present in cache memory

40. The ALU in ARM has[CLO1,L1]

a. two 32-bit inputs

b. two 64-bit inputs

c. two 16-bit inputs

d. two 8-bit inputs

41. The additional components of ARM are[CLO1,L1]

a. Barrel shifter and booth multiplier

b. Barrel shifter and booth divisor

c. Barrel shifter and booth adder

d. Barrel shifter and booth subtractor

42.It is a normal mode which has least number of registers and does not have SPSR[CLO1,L1]

a. user mode

b. FIQ mode

c. Monitor mode

d. SVC mode

43.Out of 37 registers in ARM Cortex M3[CLO1,L1]

a. 32 GPR and 5 status registers

b. 31 GPR and 6 status registers

c. 30 GPR and 7 status registers

d. 24 GPR and 13 status registers

44. In \_\_\_\_\_ mode the instructions can be either 16-bit or 32-bit and increases the performance of ARM cortex M3 microcontroller[CLO1,L1]

a. Thumb mode

b. Thumb1 mode

c. Thumb2 mode

d. SVC mode

45. The \_\_\_\_\_ mode traps when illegal instructions are executed[CLO1,L1]

a. Thumb mode

b. Undefined mode

c. Thumb2 mode

d. Trap mode

46. If ‘T’ Bit in Program Status Register of ARM is set to 1[CLO1,L1]

a. Processor in Thumb state

b. Processor in ARM state

c. Processor in idle state

d. Processor in Jazelle state

47. If ‘T’ Bit in Program Status Register of ARM is set to 0[CLO1,L1]

a. Processor in Thumb state

b. Processor in ARM state

c. Processor in idle state

d. Processor in Jazelle state

48. If ‘J’ Bit in Program Status Register of ARM is set to 1[CLO1,L1]

a. Processor in Thumb state

b. Processor in ARM state

c. Processor in idle state

d. Processor in Jazelle state

49. When the processor is executing ARM state[CLO1,L1]

a. All the instructions are 32-bit wide and word aligned

b. All the instructions are 16-bit wide and half word aligned

c. All the instructions are 8-bit wide and byte aligned

d. All the instructions are 64-bit wide and double word aligned

50. When the processor is executing Thumb state[CLO1,L1]

a. All the instructions are 32-bit wide and word aligned

b. All the instructions are 16-bit wide and half word aligned

c. All the instructions are 8-bit wide and byte aligned

d. All the instructions are 64-bit wide and double word aligned

51. When the processor is executing Jazelle state[CLO1,L1]

a. All the instructions are 32-bit wide and word aligned

b. All the instructions are 16-bit wide and half word aligned

c. All the instructions are 8-bit wide and byte aligned

d. All the instructions are 64-bit wide and double word aligned

52. Which flag bit will be tested if two operands are equal?

a. ‘Z’

b. ‘C’

c. ‘N’

d. ‘V’

53. Which registers are used for string manipulation in 8086?

a. CS:IP

b. ES:SI

c. DS:BP

d. SS:SP

54. \_\_\_\_\_\_\_ register is used in looping and rotation instructions

a. ax

b.bx

c.cx

d.dx

55. \_\_\_\_\_\_\_ is a major component used for pipelining operation in 8086

a. prefetch queue

b. CU

c. ALU

d. Memory

56. 8086 microprocessor is a \_\_\_\_\_\_\_ processor and has \_\_\_\_\_ address lines

a. 16-bit and 16-bit

b. 16-bit and 20-bit

c. 32-bit and 16-bit

d. 20-bit and 16-bit

57. 16-bit microprocessor belongs to

a. First generation

b. Second generation

c. Third generation.

d.Fourth generation

58. One of the characteristics of microcontroller is

a. CPU,RAM, ROM, I/O and timer are all on single chip.

b. Expansive

c.System design is complex

d. uses large number of instructions

59. Match the effective address calculation to relavent addressing modes

|  |  |  |
| --- | --- | --- |
| 1. | Content of PC + address part of the instruction | Indexed mode(2) |
| 2. | Content of index register + address part of the instruction | Auto increment mode(4) |
| 3. | Content of register | Relative mode(1) |
| 4. | Content of register+ step size | Register mode(3) |

60. Booth algorithm is a

a. Multiplication algorithmic rule for 2’s complement number

b. Multiplication algorithmic rule for 1’s complement number

c. Division algorithmic rule for 2’s complement number

d. Division algorithmic rule for 1’s complement number

61. Which component does not belong to 8086 processor?

a. Prefetch queue

b. Barrel shifter

c. Control Unit

d. ALU

62. Which component belongs to ARM processor?

a. Prefetch queue

b. barrel shifter

c. Bus Interface unit

d. Booth divisor

63. \_\_\_\_\_ is used for exchanging byte or word

a. LES

b. XGHG

c. XLAT

d. SAHF

61. .data represents

a. data segment

b. segment directive

c. extra segment

d. stack segment

62. In MOV instruction, register except \_\_\_\_\_ cannot be target register

a. IP

b. AX

c. DS

d. BX

63. The symbols cannot be redefined later in the program using \_\_\_\_\_ directive.

a. EQU

b. DB

c. DUP

d. DW

64. Which register tells about the status of a processor after any arithmetic or logical operations

a. IP

b. flag

c. SP

d. SI