

Intermediate Code generation.Lexical Analysis  $\rightarrow$  Syntax Analysis  $\rightarrow$  Semantic Analysis  
 $\downarrow$ 

Machine  $\leftarrow$  Code  $\leftarrow$  Intermediate Code  
code Generation Optimization Generation

Q.1  
Three  
Address  
Code

Various forms of Intermediate Code Generation

Q.1

① Linear form

- a. Prefix
- b. Postfix
- c. 3 address code.

② Tree form

- a. Syntax Tree
- b. DAG (Directly Acyclic) Graph

a. Prefix Notation

$$a + b \Rightarrow +ab$$

$$(a+b) * c \Rightarrow *(+ab)c$$

$$(a+b) * (c-d) \Rightarrow *(+ab)(-cd)$$

b. Postfix Notation

$$a + b \Rightarrow ab +$$

$$(a+b) * c \Rightarrow (ab+)c *$$

$$(a+b) * (c-d) \Rightarrow (ab+)(cd-) *$$

c. 3 address code :

$$x \text{ op } z \rightarrow (\text{variable equator variable})$$

$$\text{op } z \rightarrow \text{equator variable}$$

$$\text{ex} \rightarrow x = a + b * c + d$$

1.  $T_1 = b * c$

$$\Rightarrow a + T_1 + d$$

2.  $T_2 = a + T_1$

$$\Rightarrow T_2 + d$$

3.  $T_3 = T_2 + d$

4.  $x = T_3$

ex  $\rightarrow a = (b * -c) + (b * -c)$

1.  $T_1 = -c$   $\{ a = (b * T_1) + (b * -c) \}$
2.  $T_2 = b * T_1$
3.  $T_3 = -c$
4.  $T_4 = b * T_3$
5.  $T_5 = T_2 + T_4$
6.  $x = T_5$

### \* Implementation of 3 address code

$\hookrightarrow$  form of intermediate code

$\hookrightarrow$  representations are:

- ① Quadruples
- ② Triples
- ③ Indirect Triples.

#### ① Quadruples:

$\hookrightarrow$  has 4 fields

$\hookrightarrow$  op, arg 1, arg 2 and result.

#### ② Triples:

$\hookrightarrow$  has 3 fields

$\hookrightarrow$  op, arg 1, arg 2

#### ③ Indirect Triples:

uses pointers for representation

exple To find quadruples, triples, / indirect Triples.

S-1 convert to Three Address code

$$a = (b * - c) + (b * - c)$$

$$1. T_1 = -c$$

$$a = (b * T_1) + (b * - c)$$

$$2. T_2 = b * T_1$$

$$a = T_2 + (b * - c)$$

$$3. T_3 = -c$$

$$a = T_2 + (b * T_3)$$

$$4. T_4 = b * T_3$$

$$a = T_2 + T_4$$

$$5. T_5 = T_2 + T_4$$

$$6. \boxed{a = T_5}$$

6.

Three address code

① operand op<sub>1</sub> op<sub>2</sub>

② op<sub>1</sub> op<sub>2</sub>

Quadruples

#	op	arg 1	arg 2	result
(1)	-	c		T <sub>1</sub>
(2)	*	b	T <sub>1</sub>	T <sub>2</sub>
(3)	-	c		T <sub>3</sub>
(4)	*	b	T <sub>3</sub>	T <sub>4</sub>
(5)	+	T <sub>2</sub>	T <sub>4</sub>	T <sub>5</sub>
(6)	=	T <sub>5</sub>		a

leave blank (-)  
or (=)

Indirect Triples

Triples

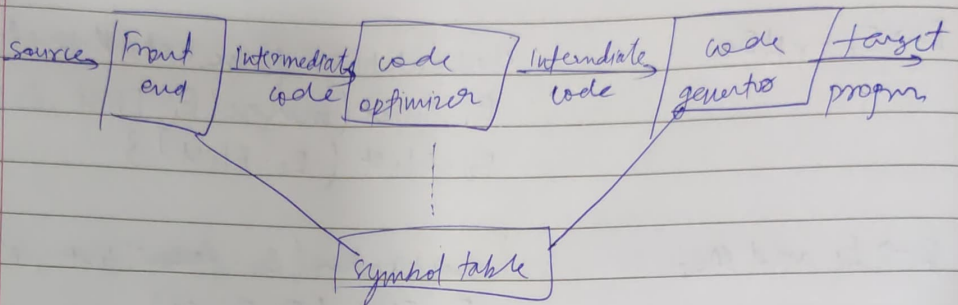
#	op	arg 1	arg 2
(1)	-	c	
(2)	*	b	(1)
(3)	-	c	
(4)	*	b	(3)
(5)	+	(2)	(4)
(6)	=	a	(5)

#	reference / start
(1)	13
(2)	14
(3)	15
(4)	16
(5)	17
(6)	18



## \* Code Generation

- Properties:
- (1) high performance
  - (2) correctness
  - (3) efficient
  - (4) quick code generation



### Issues:

- (1) Input target problems (Notations)
- (2) code generation
- (3) Memory management (Mapping values)
- (4) Instruction selection (Assembly code)
- (5) Register allocation (Use of registers)

Example

Q-

$$x = y + z$$

MOV y, R0

ADD z, R0

MOV R0, x

Q

$$a = b + c$$

$$d = a + e$$

MOV b, R0

ADD c, R0

MOV R0, a

MOV a, R0

ADD e, R0

MOV R0, d

MOV b, R0

ADD c, R0

ADD e, R0

MOV R0, d

## Code generation Algorithm:

Q

$$T = (a-b) + (a-c) + (a-c)$$

convert to three address code (Intermediate) Code.

$$T_1 \Rightarrow (a-b)$$

$$T = T_1 + (a-c) + (a-c)$$

$$T_2 \rightarrow (a-c)$$

$$T = T_1 + T_2 + (a-c)$$

$$T_3 \rightarrow (a-c)$$

$$T = T_1 + T_2 + T_3$$

$$T_4 \Rightarrow T_1 + T_2$$

$$T = T_4 + T_3$$

$$T_5 \rightarrow T_4 + T_3$$

$$T \rightarrow T_5$$

$$T_1 \rightarrow (a-b)$$

$$T_2 \rightarrow (a-c)$$

$$T_3 \rightarrow T_1 + T_2$$

$$T_4 \rightarrow T_3 + T_2$$

$$T \rightarrow T_5$$

### Assembly code

MOV a, R0

SUB b, R0

MOV a, R1

SUB c, R1

ADD R1, R0

ADD R1, R0

MOV R0, T

Stat

Code Generated

Register Descriptor

Addr. Descriptor

(1)  $T_1 = a - b$

MOV a, R0

R0 has  $T_1$

$T_1$  in R0

SUB b, R0

(2)  $T_2 = a - c$

MOV a, R1

R0 has  $T_1$

$T_1$  in R0

SUB c, R1

R1 has  $T_2$

$T_2$  in R1

(3)  $T_3 = T_1 + T_2$

ADD R1, R0

R0 has  $T_3$

$T_3$  in R0

R1 has  $T_2$

$T_2$  in R1

(4)  $T_4 = T_3 + T_2$

ADD R1, R0

R0 has  $T_4$

$T_4$  in R0

R1 has  $T_2$

$T_2$  in R1

(5)  $T = T_4$

MOV R0, T

# ① Backpatching

↳ A process which is used to fulfill the info. used during code generation

Rules:

Production Rule

Semantic Action

$B \rightarrow B_1 \parallel B_2$

{ backpatching( $E_1$ .flist,  $M$ .instr)  
 $E_1$ .Tlist(merge( $E_1$ .Tlist,  $E_2$ .Tlist))  
 $E_2$ .Flist( $E_2$ .Flist) }

$B \rightarrow B_1 \&\& B_2$

{ backpatching( $E_1$ .Flist,  $M$ .instr)  
 $E_1$ .Tlist( $E_2$ .Tlist)  
 $E_2$ .Flist(merge( $E_1$ .Flist,  $E_2$ .Flist)) }

Three Address Code Using Backpatching

$A < B \parallel C < D \&\& P < Q$

100 : if  $A < B$  go to 106

101 : else go to 102

102 : if  $C < D$  go to 104

103 : else go to 107

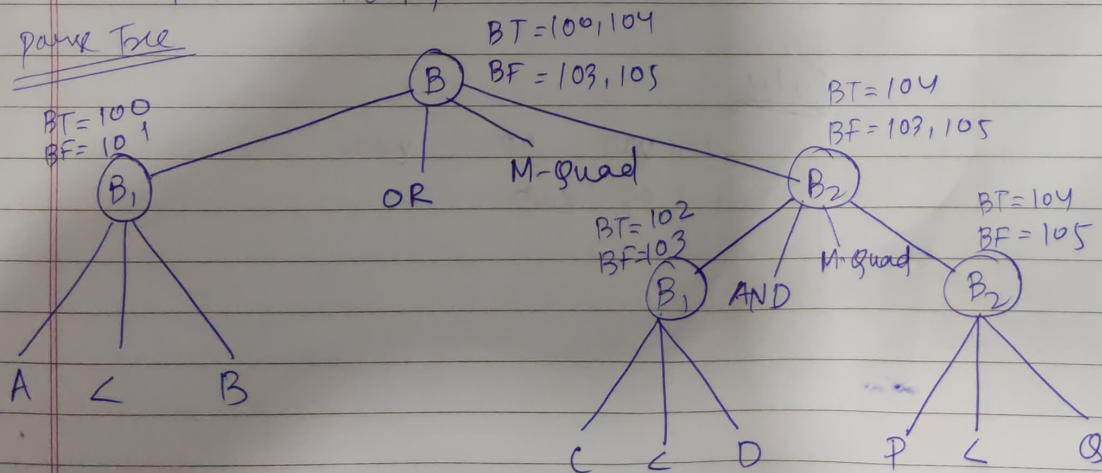
104 : if  $P < Q$  go to 106

105 : else go to 107

106 : True stmt

107 : False stmt

Parse Tree





4m

①  $x = a * - (b + c)$

①  $T_1 = b + c$   
 $x = a * - T_1$

②  $T_2 = -T_1$   
 $x = a * T_2$

③  $T_3 = a * T_2$

④  $x = T_3$

For Trnply

#	op	arg 1	arg 2
(1)	+	b	c
(2)	-	(1)	
(3)	*	a	(2)

②  $x = * y$

$a = \&x$

①  $T_1 = * y$

①  $T_1 = \&x$

②  $x = T_1$

②  $a = T_1$

Rules

- (1) var op. var
- (2) op var