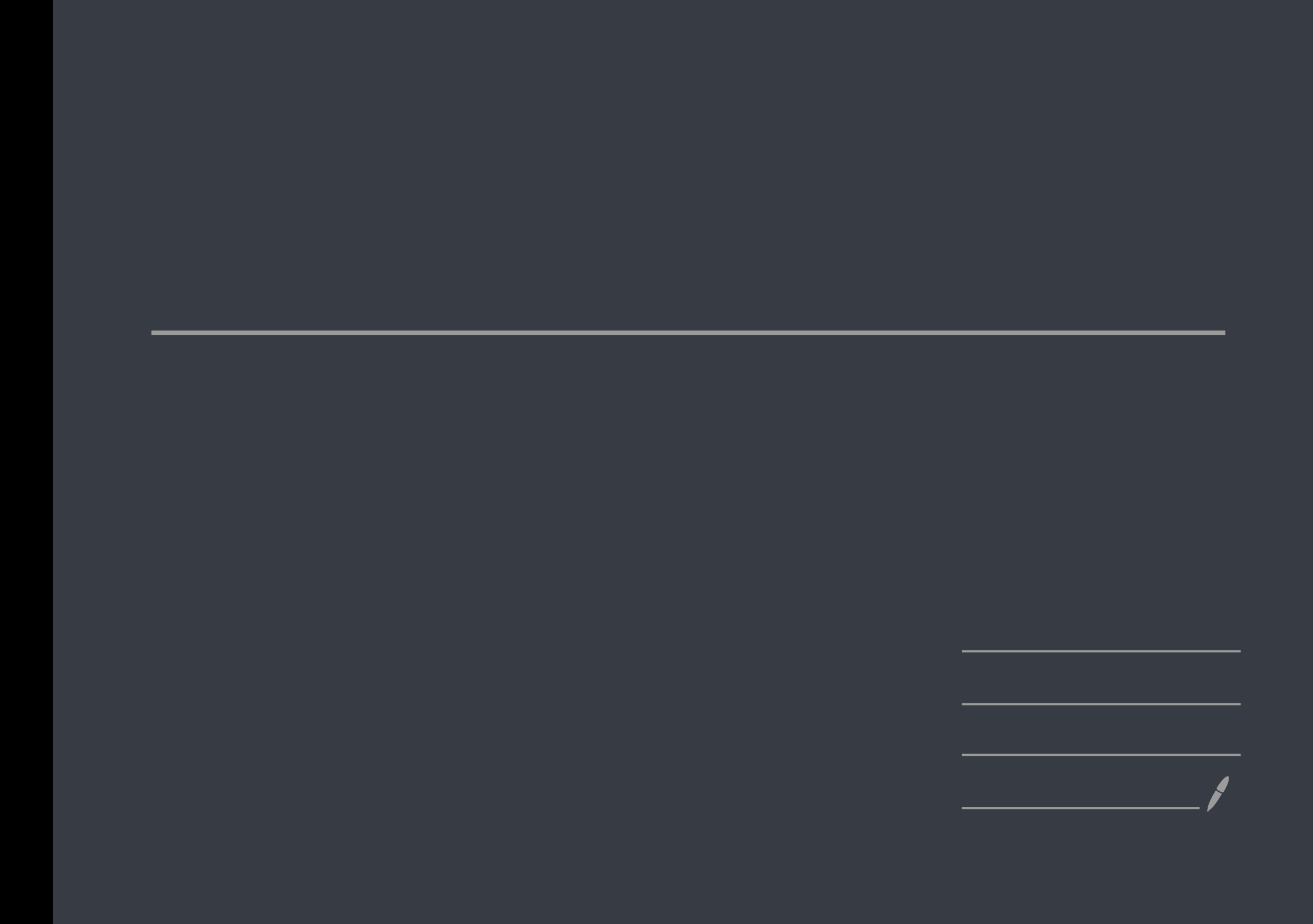
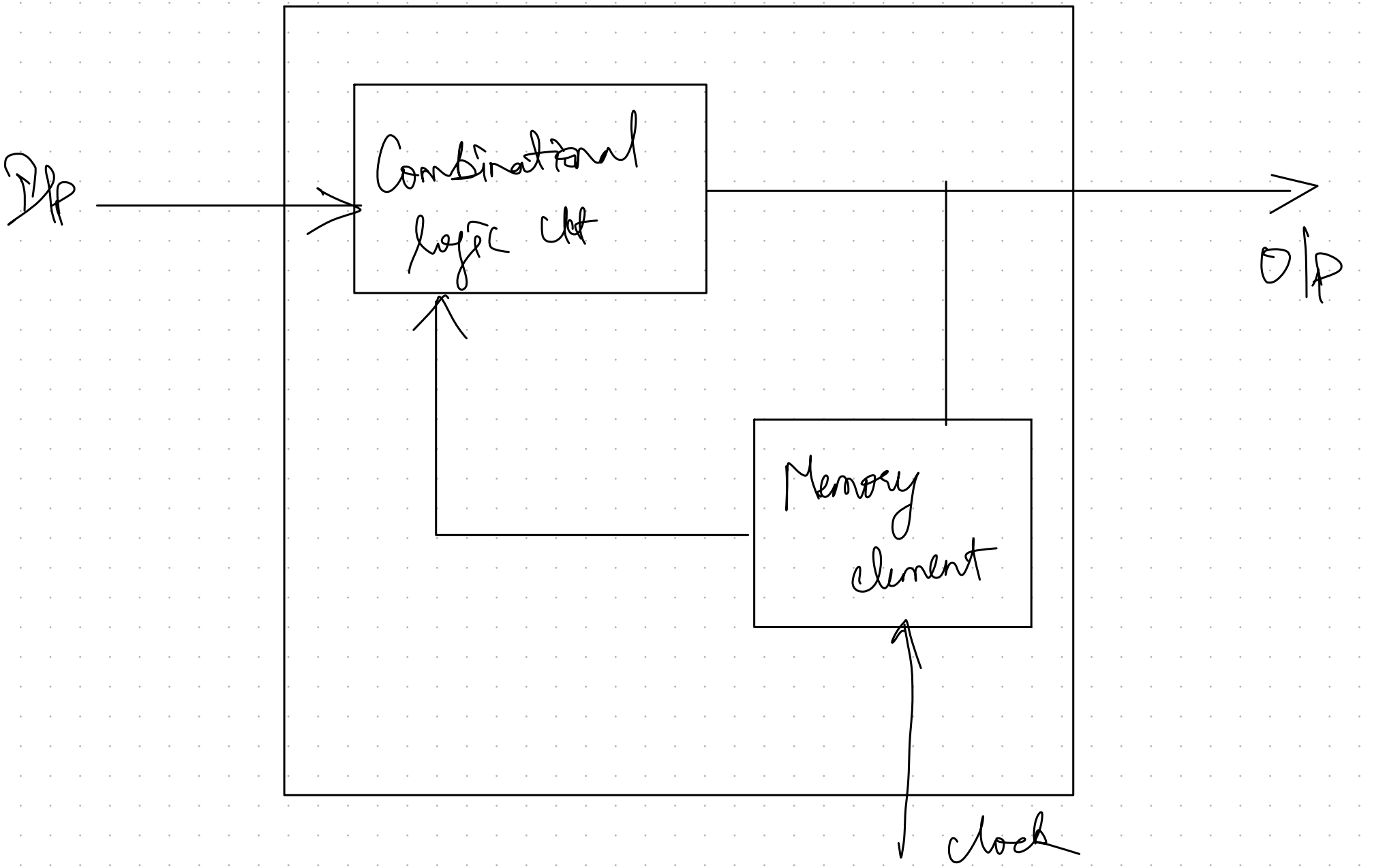


Sequential Circuit

Block diagram of SC



→ SR flip flop

→ JK flip flop

→ D flip flop

→ T flip flop

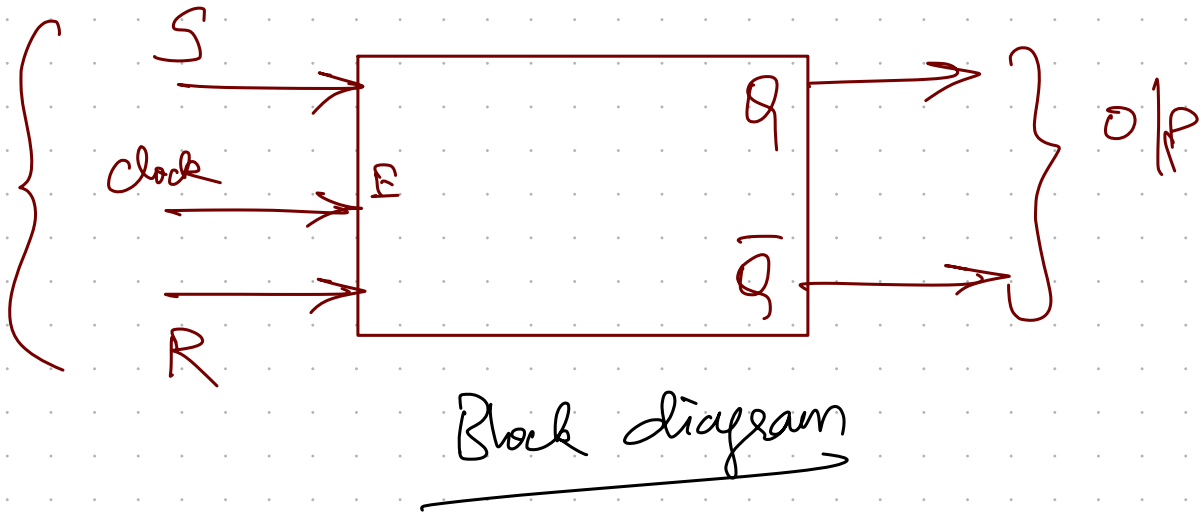
Sequential Ckts

↳ CC with memory.

SR flip flop

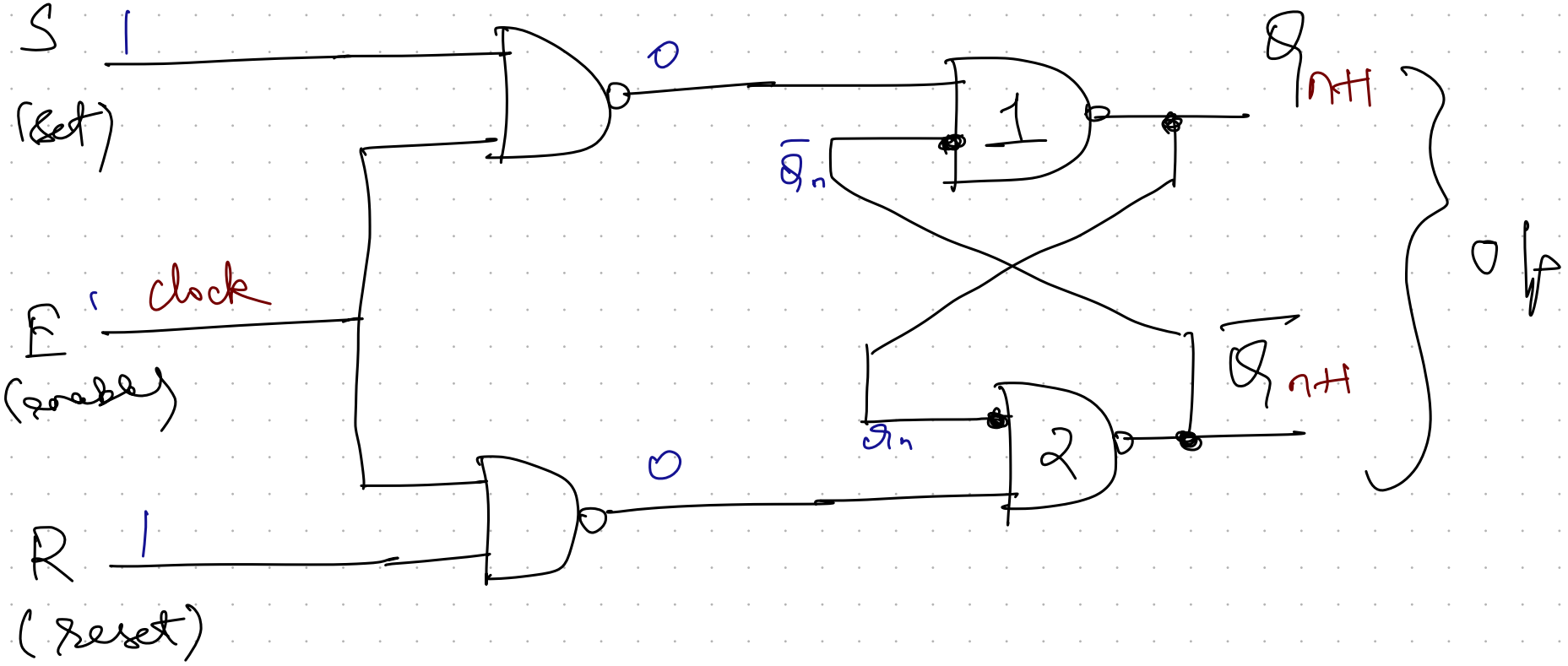
↓

NAND gates



Block diagram

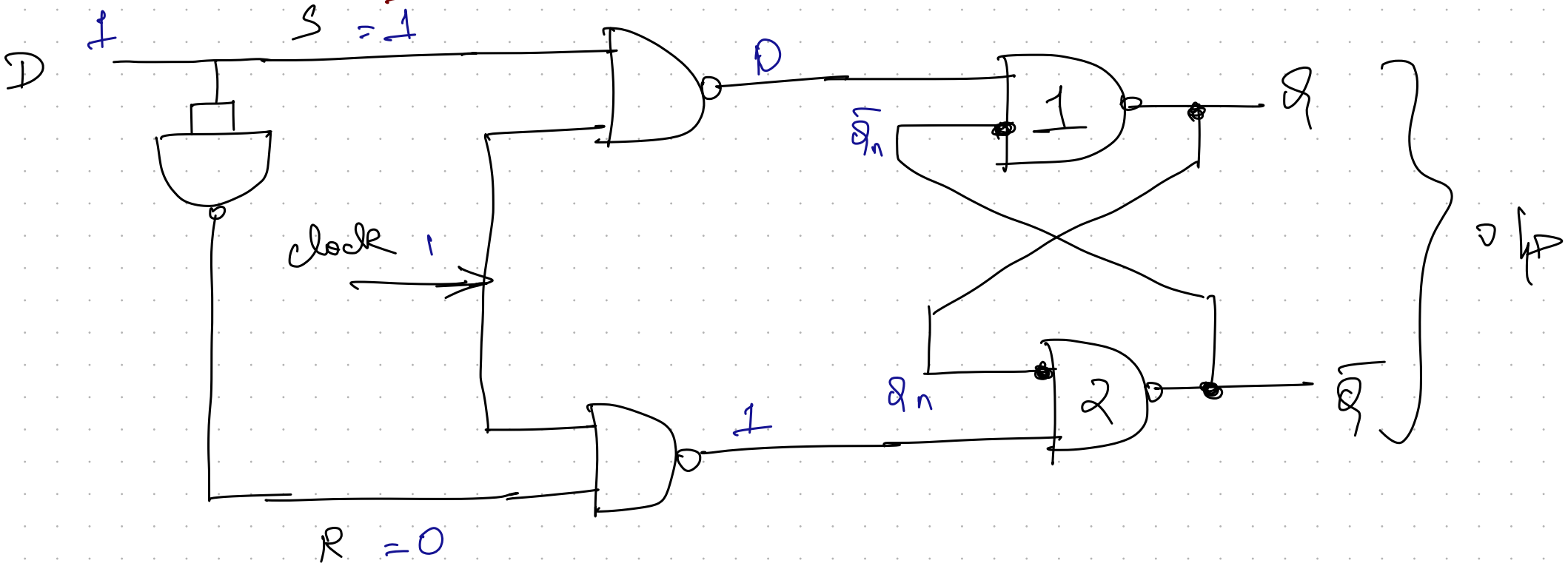
Circuit diagram



Clock	Inputs		Outputs		
E	S	R	Q_{n+1}	$\overline{Q_{n+1}}$	
1	0	0	Q_n	$\overline{Q_n}$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	1	1	Indeterminate

D - flip flop

Circuit diagram



if $D = 0 \rightarrow$

$Q_{n+1} = \overline{1 \cdot \bar{Q}_n} = Q_n = 0$

$\overline{Q_{n+1}} = \overline{0 \cdot Q_n} = 1$

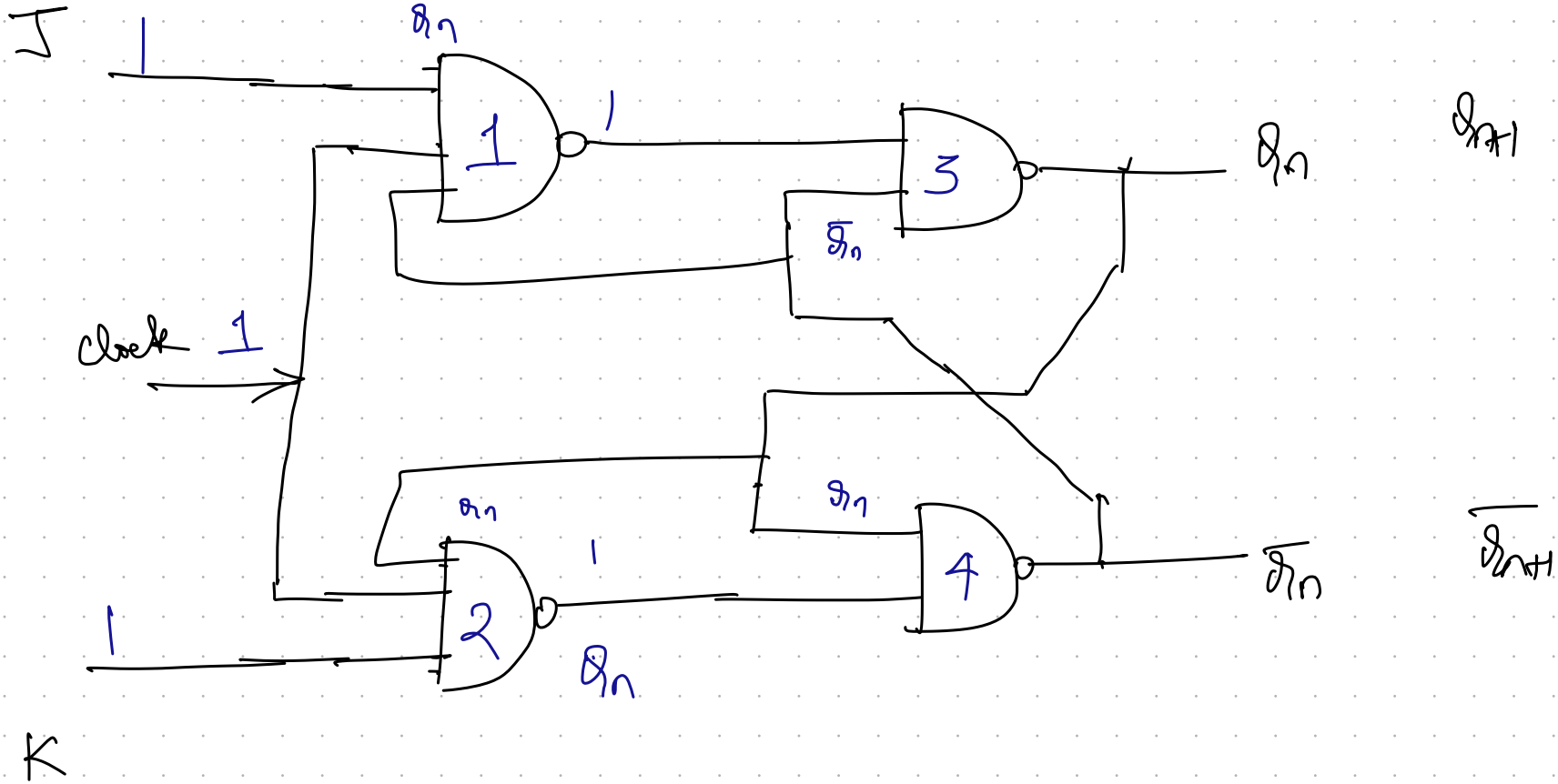
clock	D	Q_n	Q_{n+1}	
↑	0	X	0	→ Reset
↑	1	X	1	→ Set

if $D = 1 \rightarrow$

$Q_{n+1} = \overline{0 \cdot \bar{Q}_n} = 1$

$\overline{Q_{n+1}} = \overline{1 \, Q_n} = 0$

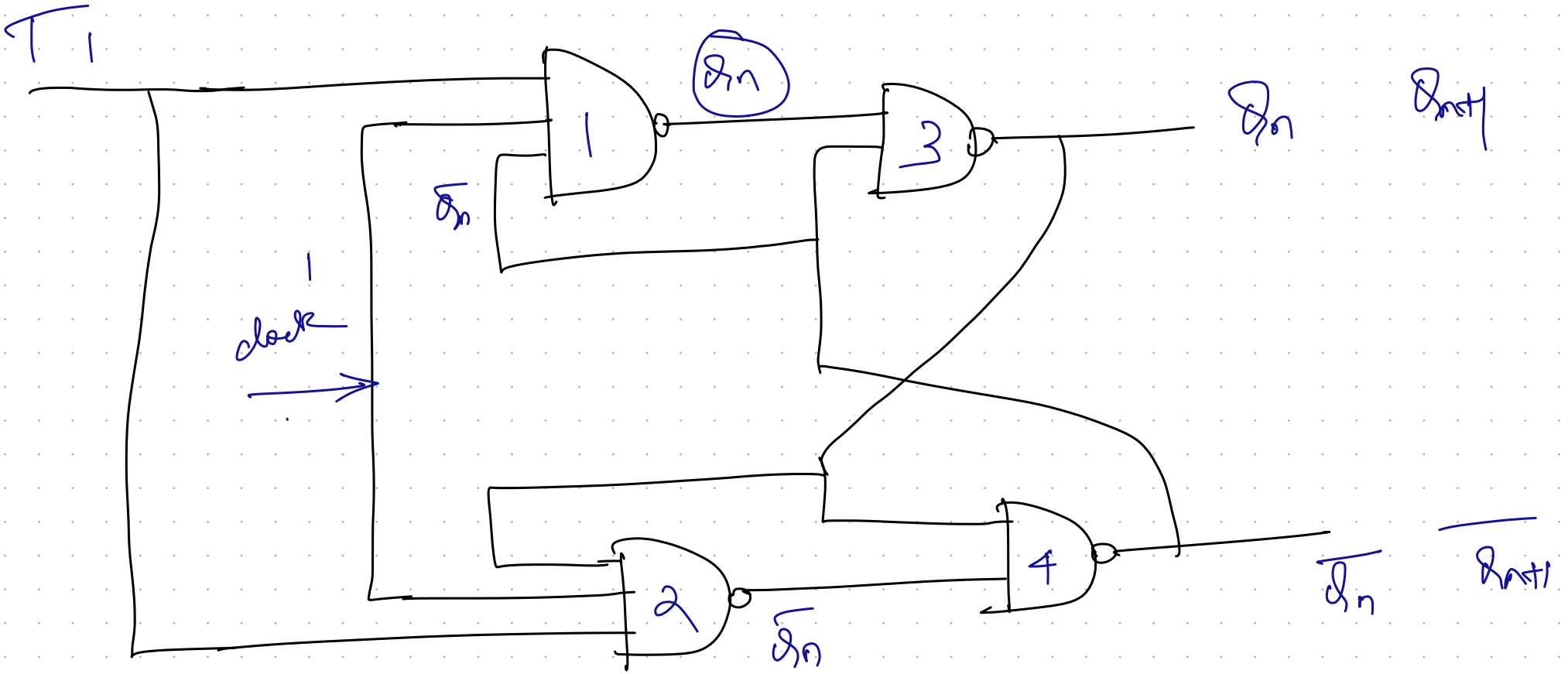
J - K flip flop



Clock = 1

J	K	Present state Q_n	Next state Q_{n+1}	$\overline{Q_{n+1}}$	
0	0	x	Q_n	$\overline{Q_n}$	
0	1	x	0	1	→ Reset
1	0	x	1	0	→ Set
1	1	x	$\overline{Q_n}$	Q_n	→ Toggle state

T- flip flop or toggle flip flop



E	T	For S Q_n	Next state Q_{n+1}
1	0	X	Q_n → No change
1	1	X	1 → toggle

if T = 0

$Q_{n+1} = 1 \cdot \overline{Q_n} = \overline{Q_n}$

$\overline{Q_{n+1}} = \overline{1 \cdot \overline{Q_n}} = Q_n$

if T = 1

$Q_{n+1} = 1$

$\overline{Q_{n+1}} = 0$