Basic Electronics

1. **Semiconductor:**
   A semiconductor is a substance whose resistivity lies between the conductors and insulators.
2. **Resistance:**
   It is the measure of opposition to current flow in an electrical circuit.
   $$R = \frac{\mathbf{\rho l}}{A}$$
3. **Capacitance:**
   The ability of a system to store a electric charge.
   $$\mathbf{C} = \frac{\varepsilon \mathbf{A}}{\mathbf{d}}$$
   There are three types of capacitances:
   Area capacitance- The capacitance formed between the substrate and any metal layer above is called self or area capacitance.
   Fringe capacitance- Fringe capacitance is formed between non-overlapping sidewall of one conductor and surface/sidewall of a second conductor on the same or different layer from the first one.
   Coupling capacitance- The capacitance between two parallel plates of the conductors.
4. **Lumped Delay:**

5. **Elmore Delay:**
   The Elmore delay analysis model estimates the delay from a source (root) to one of the leaf nodes as the sum of the resistance in the path to the i_{th} node multiplied by the capacitance present at the end of the branch.
6. **Sheet Resistance:**
   Sheet resistance, is **a measure of resistance of thin films that are uniform in thickness**. It is commonly used to characterize materials made by semiconductor doping, metal deposition, resistive paste printing, and glass coating.
   Rs = resistivity/thickness
7. **Power Density:**
   The amount of energy flow per unit area per unit time.
8. **Current Density:**
   The amount of Current flow per unit area per unit time.
9. **Duty Cycle:**
   The ratio of on time period to the total time period of a cycle.
   DC% = (on time/on time+off time)*100

10.Buffering:

In VLSI interconnect buffers are used to restore the signal level affected by the parasitics.

11.Noise Margin:

The amount of noise which is allowable in a cmos circuit without effecting the functionality.

$$NM_L = |V_{IL\ max} – V_{OL\ max}|$$

$$NM_H = |V_{OH\ max} – V_{IH\ max}|$$

12.Static Discipline:

Static discipline is a guarantee on CMOS Circuits that "if inputs meet valid input thresholds, then the system guarantees outputs will meet valid output thresholds".

$$V_{OL} < V_{IL} < V_{IH} < V_{OH}$$

13.Scalability:

Device scaling or just “scaling” is the reduction of all dimensions of the chip by a factor of “*s*.” If liner dimension decreases by “*s*,” then area decreases by *s*×*s*. With “s” being about 0.7 for the semiconductor industry, a reduction in the area of 50% results for every generation resulting in doubling of the transistor density. However, the performance doubles since the gate delays decrease with the reduction in the dimensions.

14.Mosfet Switch:

These devices act as voltage-controlled current sources, and are mainly used as switches or for the amplification of electrical signals. The MOSFET is controlled by applying certain voltage conditions to the gate. When the MOSFET is turned on, current flows from the drain to the source of the MOSFET, through a channel created in the bulk (also called the body).

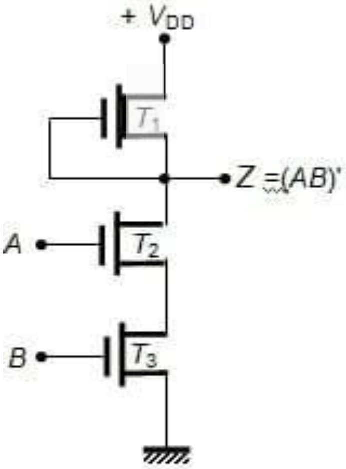
15.Threshold Voltage:

The minimum amount of voltage required to invert the channel between source and drain is called threshold voltage.

16.Gain :

The measure of ability of the circuit to increase the power or amplitude of a signal from the input to the output port.

17. 2 input NAND and NOR using NMOS:



(a) NMOS NAND

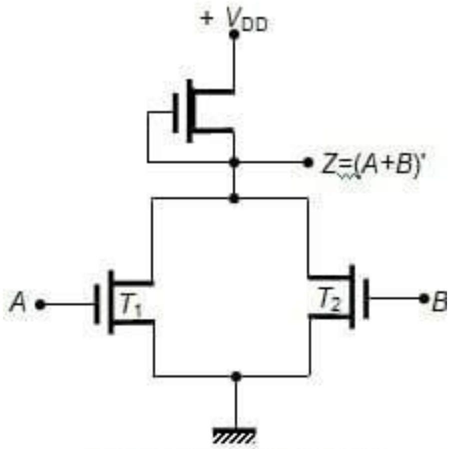


Fig. 3.24(a) NMOS NOR

18.Static Power:

The amount of power dissipated when the inputs of the circuit are stable. This is due to Internal disturbances in the MOSFET's. These disturbances are due to

- Sub-Threshold Voltage
- Gate Oxide Leakage

19. Dynamic Power:

The amount of power dissipated when the inputs of the circuit are Changing. Dynamic Power dissipation is of two types:

- Short-Circuit Power.
- Switching Power.

20.Short-Circuit Power:

This is caused due to the larger transition time. If the transition time is more then both the nmos and pmos will get ON simultaneously either in linear or saturation. More the transition time, more the short circuit power.

21.Switching Power:

This is caused due to switching of inputs. Higher the switching, higher the switching power.

22.PULL UP and PULL DOWN:

Pullup - a network that provides a low resistance path to Vdd when output is logic '1' and provides a high resistance to Vdd otherwise.

Pulldown - a network that provides a low resistance path to Gnd when output is logic '0' and provides a high resistance to Gnd otherwise.

23.Strong 1 and Strong 0:

Imagine you have a Nmos where Terminal 1 (the Top one) is connected to VDD.... Terminal 2 is Gate and Terminal 3 (the Bottom one) connected to an Output through a Capacitor.

Since in an Nmos, the Drain gets the Higher voltage; in our case, Drain is connected to VDD and Source becomes the output node.

Apply a VDD i.e Logic 1 to the Gate. The Nmos turns ON and the ouput node charges towards VDD. But you need a Vgs >= Vth to keep the Nmos in ON state. Currently Vg is at VDD and Vs charging towards VDD.

Now, when Vs approaches VDD - Vth , you have Vgs = VDD - (VDD - Vth) = Vth. Any extra voltage at Vs would turn the Nmos off and thus, you would never get a Strong 1 (i.e VDD) at the output. Thus Nmos passes a Weak 1 (VDD - Vth).

You could apply the similar analysis to the Pmos and prove it passes a weak Zero. (i.e Vth)

Try using the same analysis to the actual Inverter and you can prove that Pmos passes a Strong 1 (i.e VDD) and Nmos passes a Strong 0 (i.e VSS)

24.Advantages of CMOS:

- low power consumption
- Better Noise Margin
- strong temperature stability
- Negligible static power

25.Timing arc:

- Timing Arc is internal to the cell
- Combinational Cells has Timing Arcs from each Input to each Output of the cell
- Flip-flops have Timing Arcs from the Clock Input pin to Data Output Q pin (Propagation delay/ Delay Arc) and from Clock Input pin to Data Input D pin (setup, hold checks/ Constraint Arc)
- Latches have 2 timing arcs

    - Clock pin to Output Q pin, when D is stable.
    - Data D pin to Output Q pin when D changes (Latch is transparent).

26.Propagation Delay:

The propagation delay of a logic gate is the difference in time (calculated at 50% of input-output transition), when output switches, after application of input.

27. Drive Strength:

Drive strength simply means how much strength it needs to drive output cap/load. More is the drive strength, lesser will be the internal resistance, more is the current can be drawn from vdd and quickly, lesser is time it will take to charge the output cap, and finally lesser will be the delay.

28. Glitch:

A glitch is a small spike that happens at the output of a gate. A glitch happens generally, if the delays to the combinational gate output are not balanced.

Due to this functionality or timing may be effected. The power consumption is high due to unnecessary power dissipation due to this glitch.

Digital Electronics

1. **Combinational Circuits:**

   A combinational circuit is a circuit in which the output depends on the present combination of inputs. Combinational circuits are made up of logic gates. The output of each logic gate is determined by its logic function.

2. **Active low & Active High Signal:**

   For sake of example, assume a circuit operates on 5 volts.

   If the circuit uses "active high" logic, 5 volts represents a digital "1" and 0 volts represents a digital "0".

   If the circuit uses "active low" logic, 5 volts represents a digital "0" and 0 volts represents a digital "1".

3. **Multiplexer:**

   A device which is used to select a signal from multiple inputs and transmit to the output.

4. **Probability of 2 input NAND, NOR, XOR:**

5. **Multidriven net:**

   When multiple outputs of different cells drive the same net, then it is called multidriven net.

6. **Floating input:**

   If any input of a cell is unused and is not connected to any cell or net, it is called Floating input.

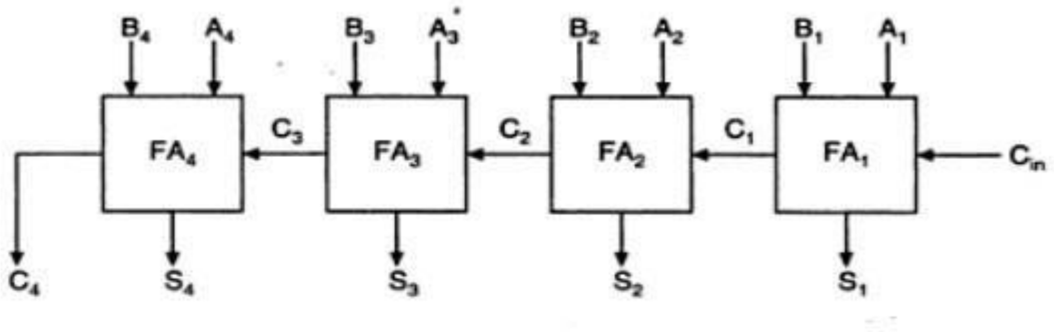
7. **Half & Full Adder:**

   The half adder circuit has two inputs A and B, which add two input digits and generates a carry and a sum.

   The full adder circuit has three inputs A, B and C, which add three input digits and generates a carry and a sum.

8. **Ripple Carry Adder:**

A structure of multiple full adders is cascaded in a manner to gives the results of the addition of an n bit binary sequence.



9. **Carry Look Ahead Adder:**

A carry look-ahead adder reduces the propagation delay by introducing more complex hardware. In this design, the ripple carry design is suitably transformed such that the carry logic over fixed groups of bits of the adder is reduced to two-level logic. Consider the full adder circuit shown above with corresponding truth table. We define two variables as **'carry generate'** G_i and **'carry propagate'** P_i then,

$P_i = A_i$ (xor) B_i

$G_i = A_i B_i$

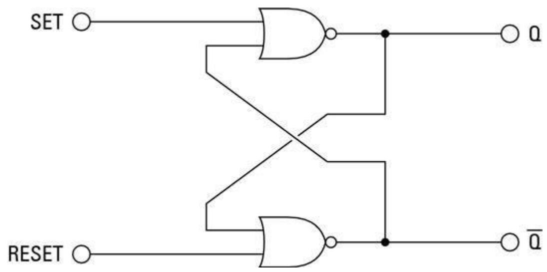
A	B	C	C +1	Condition
0	0	0	0	No Carry Generate
0	0	1	0	
0	1	0	0	
0	1	1	1	No Carry Propogate
1	0	0	0	
1	0	1	1	
1	1	0	1	Carry Generate
1	1	1	1	

10.Sequential Circuits:

In Sequential circuits, the output depends not only on the latest inputs, but also on the condition of earlier inputs. Sequential circuits contain memory elements.

11.Latch:

A latch is an electronic device that changes its output immediately on the basis of the applied input. One can use it to store either 0 or 1 at a specified time. A latch contains two inputs- SET and RESET, and it also has two outputs. They complement each other. One can use a latch for storing one bit of data.



12.Active Low & Active High Latch:

If the latch allows data to pass through when the enable signal has a value of 1, we say it is an active high latch.

If the latch allows data to pass through when the enable signal has a value of , we say it is an active low latch.

13.Transparent mode:

A transparent latch is one where the inputs are passed straight through to the outputs when the enable signal is active. When the select signal goes inactive, the final input state is latched on the outputs.

14.Setup &Hold requirement of latch:

Setup time is the minimum time required for the data to get settled before the latching edge of the clock, in this case it is the Rising edge.

Hold time is the minimum time required for the data to get settled after the latching edge of the clock, in this case it is the Rising edge.

15.Flip Flop:

A flip-flop in digital electronics is a circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs.

16.Positive and Negative FF:

A positive edge is the low-to-high transition. Positive edge flip-flops will allow its outputs to change only at the rising edge of the clock.

A negative edge is a high-to-low transition. Negative edge flip-flops will allow its outputs to change only at the falling edge of the clock.

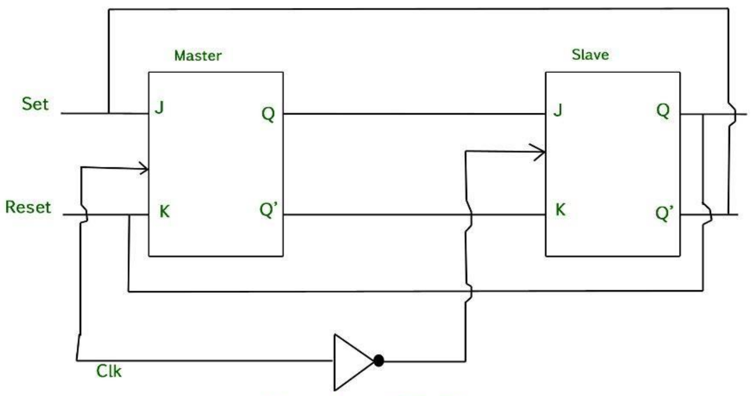
17.Race Around Condition:

In JK Flip-flop, if J=K=1, and if clk=1 for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip-flop unstable or uncertain. This problem is called race around condition in J-K flip-flop.

18.Master Slave Flip-Flop:

The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration. Out of these, one acts as the **"master"** and the other as a **"slave"**. The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip flop.

In addition to these two flip-flops, the circuit also includes an **inverter**. The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop. In other words if CP=0 for a master flip-flop, then CP=1 for a slave flip-flop and if CP=1 for master flip flop then it becomes 0 for slave flip flop.



Master-slave JK Flip-Flop

19.FlipFlop Conversions:

https://www.tutorialspoint.com/digital_circuits/digital_circuits_conversion_of_flip_flops.htm#

20.Counters:

https://www.geeksforgeeks.org/counters-in-digital-logic/amp/

21.Registers:

https://www.tutorialspoint.com/computer_logical_organization/digital_registers.htm

Static Timing Analysis (STA)

1. **What is Static Timing Analysis (STA):**

   STA is a method of validating timing performance of a design by checking all possible paths for timing violations.

2. **What is Dynamic Timing Analysis (DTA):**

   DTA determines the full behavior i.e., timing and functionality of the circuit for a given set of input test vectors.

3. **Difference between DTA and STA:**

DTA	STA
Checks for both timing and functionality.	Checks for only timing.
Dependent on input data (test vectors).	Independent of data.
Slower because it also checks the functionality.	Faster and takes less time.

4. **Setup time & Hold time:**

   The minimum amount of time required to stabilize the inputs before the clock edge is called "**Setup Time**".

   The minimum amount of time required to stabilize the inputs after the clock edge is called "**Hold Time**".

5. **Setup Slack & Hold Slack:**

   Setup Slack verifies that the data delay is small enough so that the data launched by launch flop should reach the capture flop within one clock cycle, and the data should arrive at least one unit time before the data gets captured by the capture clock.

SS = RT-AT

Arrival Time ≤ Required Time

$$t_{launch} + t_{ck\text{-}q} + t_{comb} + t_{wire} \leq t_{clk} - t_{su} - t_{un} + t_{capture}$$

Hold Slack verifies that the data already existing at the input of capture flop remains stable long enough after the clock edge that captures the data for the previous cycle.

HS = AT-RT

Arrival Time ≥ Required Time

$$t_{launch} + t_{ck\text{-}q} + t_{comb} + t_{wire} \geq t_{h} + t_{un} + t_{capture}$$

6. **Hold Check 1 & Hold Check 2:**

   The data launched by next launching edge must not capture by current capturing edge is HS1.

   The data launched by current launching edge must not capture by previous capturing edge is HS2.

7. **Single Cycle Behavior:**

   The data launched should be captured in a single cycle without violating setup and hold requirements.

8. **Skew:**

   The difference between capture flop latency and launch flop latency is called skew.

   Different types of skew are:

   - Local Skew
   - Global Skew
   - Useful Skew

9. **Local Skew:**

   The difference between capture flop latency and launch flop latency of two communicating flops is called local skew.

   Types:

   - Positive Skew - Effects hold requirement.
   - Negative Skew - Effects setup requirement.

10. **Global Skew & Useful Skew:**

    - Difference between max clock latency and min clock latency in a design is called **Global Skew**.
    - If we intentionally introduce skew in a timing path to meet setup or hold requirement, then it is called **Useful Skew**.

      To meet setup - we add delay in capture path

      To meet hold - we add delay in launch path

11. **Clock Jitter:**

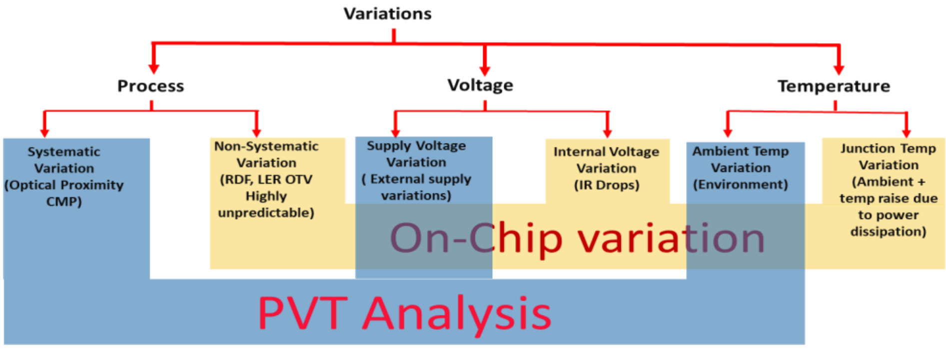
    The deviation of the clock edge from its actual position is called **Clock Jitter**.

12.Base Period:

Base period is the least common multiple (LCM) of all clock periods.

13.On Chip Variation (OCV):

In OCV a fixed timing derate factor is applied to the delay of all the cells present in the design so that in case of process variation affects the delay of any cells during the fabrication, it will not affect the timing requirements and the chip will not fail after fabrication. And this OCV is used above 90nm technology.



Fabrication process variations could either increase or decrease the delay of a cell. So we need to set early and late values while setting the derate factor.

CMD: set_timing_derate -cell_delay-rise -data -early 0.92

14.Derating Factor:

Timing derate numbers are ratios used to derate(increase/decrease) the delay numbers you get in your timing reports.

15.Common Path Pessimism Removal (CPPR):

It means the cells sitting in the common clock branch for both launching and capturing paths.

16.Advanced OCV (AOCV):

In AOCV derate is applied on each cell based on path depth and distance of the cell in the timing path and it also varies with cell type and drive strength of the cell. Distance is defined by a bounding box for the net and cells.

- Used above 40nm technology.

- Distance is the max net length of clock path.
- Path Depth defines the no. of cells in the clock path.

17.Parametric On chip Variation (POCV):

- In POCV instead of applying the specific derate factor to a cell, cell delay is calculated based on delay variation (σ) of the cell. In POCV it is assumed that the normal delay value of a cell follows the normal distribution curve.
- POCV uses a nominal delay value (μ) instead of using the min or max value of delay to model the random variations.
- Timing analysis is done using the nominal delay value (μ) and delay variation (σ).
- Used above 40nm technology.

18.Clock:

The signal which is used to trigger all the sequential elements in the design.

Types,

- Synchronous
- Asynchronous
- Exclusive

19.Synchronous & Asynchronous Clocks:

- Two clocks are **synchronous** with respect to each other if they share a common source and have a fixed phase relationship and a common base period(should have a common multiple).

  Ex: time period of two clocks : 2 and 6, here the common base period is 2.
- Two clocks are said to be **asynchronous** if they do not have a fixed phase relationship with each other in the design and don't have a common base period.

  Ex: time period of two clocks : 6 and 7, here there is no common base period.

20.Exclusive Clocks:

- Two clocks are exclusive if they do not interact with each other.
- For example, a circuit might multiplex two different clock signals onto a clock line, one a fast clock for normal operation and the other a slow clock for low-power operation.

- Only one of the two clocks is enabled at any given time, so there is no interaction between the two clocks.
- You may define "false path" between these mutually exclusive clocks.

21.Virtual Clock:

- A virtual clock has no actual source in the current design, but you can use it for setting input or output delays.
- You can use virtual clock cmd to define virtual clocks for signals that interface to external clocked devices (other block).

CMD: create_clock –period 8 –name vclk –waveform {0 4}

22.Create Clocks:

- The crete_clock cmd is used to create a clock at the specified source. A source can be defined at an input port of the design or an internal pin.
- To create a clock on ports C1 and CK2 with a period of 10, a rising edge at 2, and falling edge at 4, enter the cmd

CMD: create_clock –period 10 –waveform {2 4} [get_ports {C1 CK2}]

- With this an ideal clock is created that ignores the delay effects of the clock network.

23.Gated Clock:

A gated clock is a clock signal under the control of gating logic.Tool performs both setup and hold checks on the gating clock.

24.Generated Clocks:

- A generated Clock is a clock signal generated from another clock signal by a circuit within the design itself, such as a clock divider.
- The create_generated_clock cmd is used to create generated clocks in which you can create frequency divided (-divide_by) or frequency multiplied (-multiply_by) clock.

CMD: create_generated_clock –name dclk\
–source [get_ports CLK] –divide_by 2 [get_ports FF1/Q]

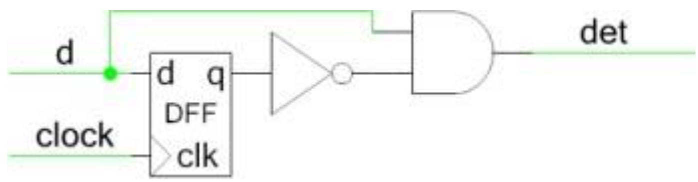
25.Edge detecting Circuits:

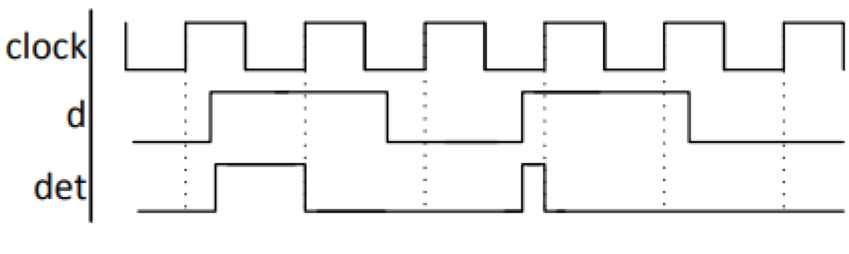
The Edge Detector component samples the connected signal and produces a pulse when the selected edge occurs.

We must select anyone of the edge for detection, Rising Edge, Falling Edge, or Either Edge.

Rising Edge Detector:

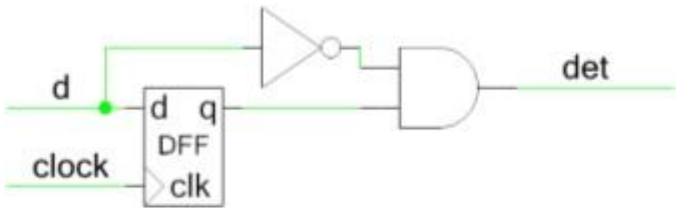
The Edge Detector stores the state of the signal at the last rising clock edge, and compares it to the current value of the signal. If the state change matches the edge type selected in the customizer, the det terminal will go high until the next rising clock edge. This means that the resulting pulse from an edge may be shorter than one clock cycle, but it will never be longer.

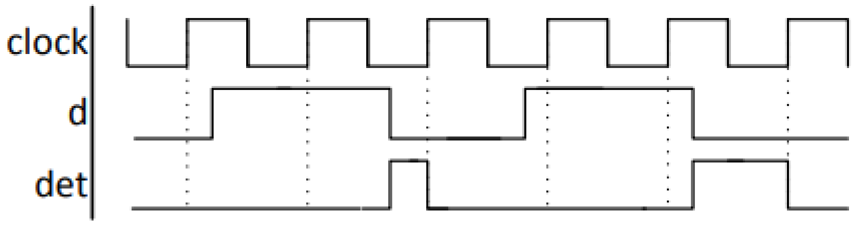




As seen in Figure 2, the det output will go high as soon as a rising edge is detected on the d input. The det output is cleared on the next rising clock edge.

Falling Edge Detector:





As seen in Figure 4, the det output will go high as soon as a falling edge is detected on the d input. The det output is cleared on the next rising clock edge.

26.Timing Path:

Timing path is defined as the path between start point and end point.

- Start Point - CK pin of flop or Input port of the block.
- End Point - D pin of the flop or output port of the block.

27.Types of Paths:

- Reg to Reg
- In to Reg
- Reg to Out
- In to Out

28.Input Delays:

- In order to do the timing analysis in the paths like I2R and I2O, tool needs information about the arrival times of the signals at the input ports.
- The set_input_delay cmd is used to specify the min and max amount of delay from a clock edge to the arrival of a signal at a specified input port.

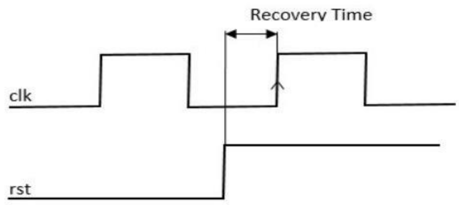
29.Output Delays:

- In order to do the timing analysis in the paths like R2O and I2O, tool needs information about the timing requirements at the output ports.

- The set_output_delay cmd is used to specify the min and max amount of delay between the output port and the external sequential device that captures the data from that output port is specified at that output port.

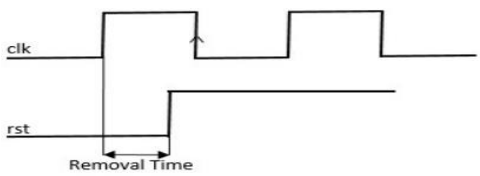
30.Recovery and Removal times:

Recovery time is the minimum time that as asynchronous control signal must be stable before the clock active-edge transition. In other words, this check ensures that after the asynchronous signal become inactive, there is adequate time to recover so that the next active clock edge can be effective.



Recovery Time

Removal time is the minimum length of time that an asynchronous control must be stable after the clock active edge transition. This check ensures that the active clock edge has no effect because the asynchronous control signal remains active until removal time after the active clock edge.



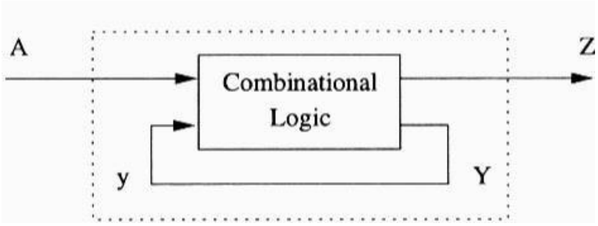
Removal Time

31.Hand Shaking Communication:

A handshake is a means of synchronization among communicating mechanisms. In its simplest form it involves two mechanisms connected by a pair of so-called links, one for sending signals and one for receiving signals.

32.When the circuit gets asynchronous:

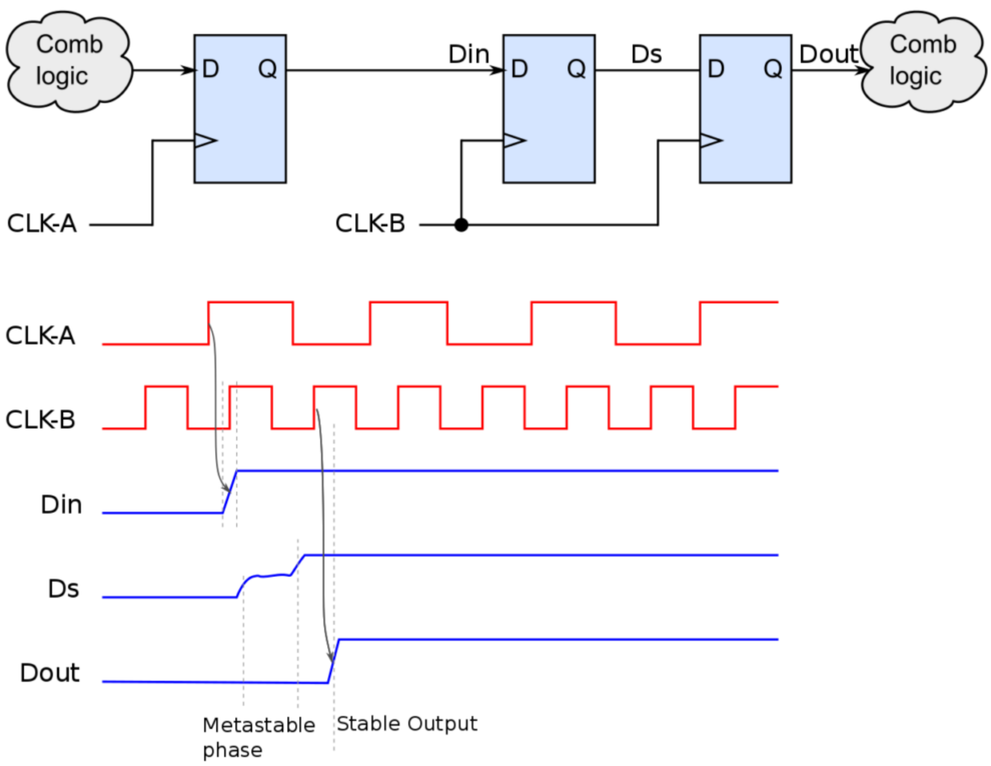
The asynchronous circuits do not need a global clock, and the state of the circuit changes as soon as the inputs change.



Since asynchronous circuits do not have to wait for a clock pulse to begin processing inputs, they can operate faster. Their speed is theoretically limited only by the propagation delays of the logic gates and other elements.

33.Two Stage Synchronizer:

When an asynchronous signal, or a signal from a block clocked by a different clock is received by a synchronous circuit, it is imperative that it is reliably sampled by the receiver. Since the signal is asynchronous to the receiver in these cases, a special circuitry named synchronizer is used to ensure proper sampling and synchornization with respect to the receiving clock. If the data changes in an unacceptable range of the clock, metastability occurs as explained previously. This can be avoided by giving enough time for the meta stable output to settle down. The most common method used is the two stage synchronizer using flops.



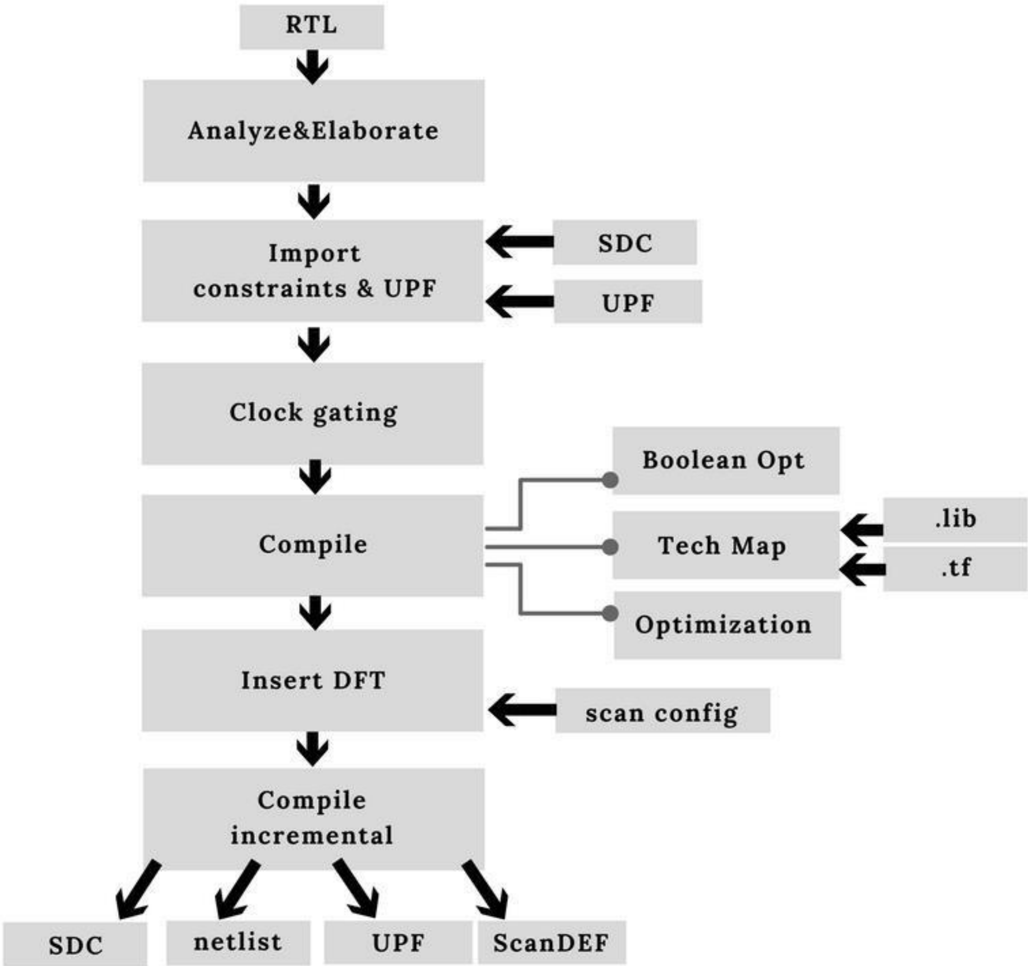
The two flops should be placed as close to each other as possible so there is no combinational delay between the flops. This ensures that entire clock cycle is available for the metastability to resolve. There is a possibility that the input will be settled into a wrong value, and this wrong input will be propagated to the subsequent stages. It is important that the input from one domain stays stable for at least one clock cycle so that the wrong stable data(after a metastability event) is not propagated. The disadvantage in using these synchronizers are the overhead it adds in propagation delay, area and power. Special synchronization flops are available in your libraries which have higher value of MTBF, and is specially designed for reducing the failure rate.

34.Mean Time Between Failure (MTBF):

Metastability failures are probablisitic in nature. You cannot avoid metstability, but MTBF or the Mean Time Between Failures gives you a measure to determine the reliability of the device with respect to metastability failures. It gives the average time between two failures for the device.

Logic Synthesis

1. **Logic Synthesis:**
   The process of converting high level abstraction(RTL) to implementable logic gates (Gate level Netlist) to a targeted technology by meeting design constraints(Timing, Area, Power).
2. **Synthesis Flow:**



3. **Sanity Checks:**

check_design - Netlist

- Unresolved References
- Empty Modules
- Unloaded Ports
- Unloaded Sequential Pins
- Undriven Leaf pins
- Undriven Ports
- Combinational Loops
- Multidriven Port

check_timing - SDC

- Sequential clock pin without clock waveform
- Sequential clock pin with multi clock waveform
- Generated clocks without clock waveform
- Generated clocks with multi master clocks
- Timing exceptions with no effect
- Inputs/Outputs without clocked external delay
  Exceptions with invalid timing start or end points

4. **Elaborate:**
Elaboration is the process that occurs between parsing and simulation. It binds modules to module instances, builds the model hierarchy, computes parameter values, resolves hierarchical names, establishes net connectivity, and prepares all of this for simulation.
5. **Inputs of Synthesis:**
   - .lib
   - .lef
   - SDC
   - RTL
   - Tech lef
6. **Types of libraries:**
Slow, Typical and Fast libraries.

Corner	Process	Voltage	Temperature
Slow	SS	0.9	125
Typical	TT	1	25
Fast	FF	1.1	M40

7. **Design Rule Violations(DRV):**
DRV constraints exist in .lib.
DRV constraints can't be relaxed. They can be chosen from .lib. These constraints are imposed upon the design by requirements specified in the target technology library. These precedence over optimization constraints to realize a functional design.
   - Max Cap
   - Max Tran
   - Max Fan Out
8. **Max transition:**
If any path having larger transition which are greater than defined max_transition value, then it reports max transition violation.
9. **Max capacitance:**
The maximum capacitance(C_L) of a cell is the sum of output pin capacitance of the driver, net capacitance and input pin capacitance of the driven cell.
If any path having larger capacitance which are greater than defined max_capacitance value, then it reports max capacitance violation.
10. **Max fanout:**
   - The number of loads a pin or port can drive.
   - Limits the number of components that can be driven by the input port.

- It is useful for signals that drive many blocks (e.g. global buses,reset).
- Fanout can be reduced by Cloning (or) Buffering.

11..LEF File(std & macro):

- Metal Layer Info
- Pin Name
- Pin Location
- Pin Layer
- Pin Direction
- Site Row
- Height of the cell
- Width of the cell
- Pin Width
- Pin Height

12. Tech LEF File:

- No of Metal Layers
- Via Definition
- Resistance Value of Metals
- Capacitance Value of Metals
- Pitch
- Minimum Spacing
- Layer name
- Metal direction

13..LIB File:

- PVT
- Units
- Cell Delay
- Input Transition
- Output Load
- Rise &Fall Times
- Wire Load Models
- Setup and Hold requirements of flops
- Power Info
- Functionality of all gates
- Area of STD Cells
- Unatnes

14. Intrapolation:

Interpolation is a method of estimating the value that lies between known data points and this is done using the known data points.

15. Extrapolation:

16. Clock Uncertainty:

It is the margin which we reserve in clock period for the clock effecting pessimistic parameters like

- Skew
- Jitter
- OCV
- Crosstalk

17. Wire load Model:

Wire load models (WLM) can be used to calculate interconnect wiring delays (capacitance (C), resistance (R)) due to interconnect.

The wire load model is also used to estimate the length of a net-based upon the number of its fanouts.

Types:

- Zero WLM - 0% Uncertainty
- Custom WLM -15% Uncertainty(user defined)
- Auto WLM -Tool calculates based on fanouts.

18. Gate Count:

Gate count refers to the number of logic gates built with transistors and other electronic devices, that are needed to implement a design.

19. Instance Count:

The instance count is the actual number of standard cells in your design.

20. Synthesis Strategies:

- Top-Down Approach/Flat Design
- Bottom-Up Approach/Hierarchical design

21. Hierarchical Synthesis:

- The entire is divided into different blocks and synthesized separately
- We may or may not have control over logic (less optimization)
- So less run time
- Less memory requirement
- Low end servers (Economical)
- Multiple persons can work on the design
- So design may get ready on time.

22. Flat Design synthesis:

- The whole design is considered as a single identity
- We have control over entire logic (well optimization)
- So Huge run time
- Huge Memory requirement
- High end servers (Expensive)
- Multiple persons won't work on the design, So design may get delayed.

25. Time Budgeting:

Timing budgeting is an important step in achieving timing closure in a physically hierarchical design. The timing budgeting determines the corresponding timing boundary constraints for each block in a design. If the timing boundary constraints for each block are met when they are implemented, the top-level timing constraints are satisfied.

In the chip designing, while you divide the design into small blocks, you have to take care about timing between block's I/O to other block's I/O, block's I/O to chip I/O. If a data is required by a block A for doing some processing and this data is generated by block B, so Block A should know when it will receive the data from the Block B. Since at the top level these blocks are Black Box, so during timing budgeting we have to define the constraint at input of Block A that it will receive the data after X time (this X we have to estimate correctly on the basic of experience and knowledge of the block, usually we constraint with X+x amount where x is the margin we are keeping in case of wrong estimation).

26. set_dont_use:

This cmd is used to specify the std cells, so that the tool don't use these cells in the design at the time of optimization.

27. False Path:

A false path is a timing path which is not required to meet its timing constraints for the design to function properly.

28. Multi Cycle Path:

A Multi-Cycle Path (MCP) is a flop-to-flop path, where the combinational logic delay in between the flops is permissible to take more than one clock cycle.

35. Min Delay & Max Delay:

A path must match a delay constraint that matches a specific value. It is not an integer like multicycle path.

36. Design for Testability (DFT):

The process in which we check for failures in the functionality due to manufacturing faults by inserting test patters in the design.

30. Scan:

Scan diagnosis helps identify the location and classification of a defect based on the design description, test patterns used to detect the failure, and data from failing pins/cycles.

31. Scan Stiching:

The process of serially connecting a group of scan flipflops together to form a scan chain is referred to as 'scan stitching'.

The scan chain stitching is made power aware by placing flip-flops with higher test combination requirements at the beginning of scan chains, while flip-flops with lower test combination requirements are put toward the end of scan chains.

32. Scan Chain:

- Scan chains are the elements in scan-based designs that are used to shift-in and shift-out test data.
- A scan chain is formed by a number of flops connected back to back in a chain with the output of one flop connected to another.
- The input of first flop is connected to the input pin of the chip (called scan-in) from where scan data is fed.
- The output of the last flop is connected to the output pin of the chip (called scan-out) which is used to take the shifted data out.

33. Memory Built In Self Test (MBIST):

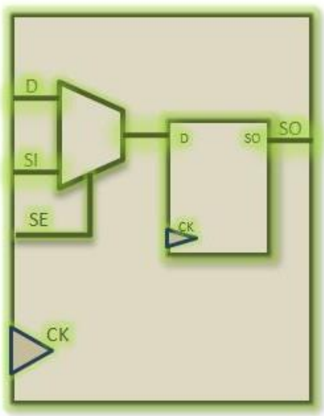
MBIST is a self-testing and repair mechanism which tests the memories through an effective set of algorithms to detect possibly all the faults that could be present inside a typical memory cell whether it is stuck-at (SAF).

34. Joint Test Action Group (JTAG):

JTAG is a powerful test technology that can be used to test the io pads for all the possible Manufacturing Defects or Faults.

35. Test Enable:

Input to the scan-flop that controls whether scan_in data or functional data will propagate to output.



36. Scan Chain Reordering:

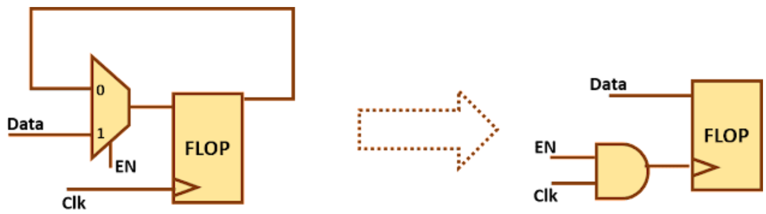
- It is the process of reconnecting the scan chains in a design to optimize for routing by reordering the scan connection which improve timing and congestion.
- It is done either at pre CTS or post CTS.
- And then the CTS def is sent to DFT team for changing the test vectors for the reordered scan chain.

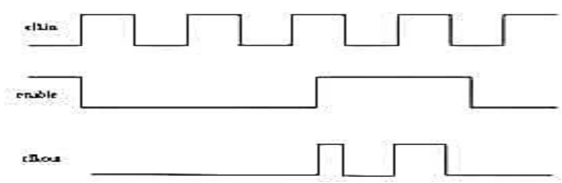
37. Power Opt Techniques:

- Clock Gating
- Operand Isolation
- Mixed Vt optimization
- ICG
- Multi VDD

38. Integrated Clock Gating(ICG):

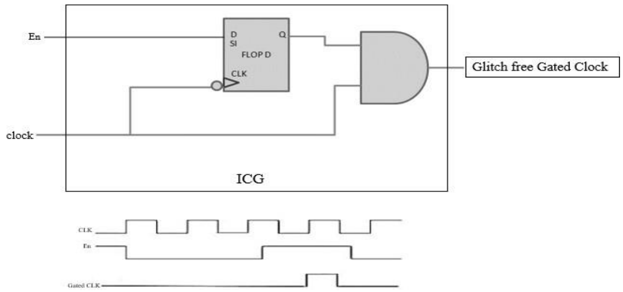
- Clock gating limits the clock from being given to every register or flops in the processor. It disables the clock of an unused device.
- It is used for reducing DYNAMIC POWER by controlling switching activities on the clock path.
- Generally gate or latch or flip flop based block gating cells are used for implementing clock gating.
- We can find these Clock Gating cells in .lib file.
- In load enabled flops, the output of the flops switches only when the enable is on. But clock switches continuously, increasing the dynamic power consumption.





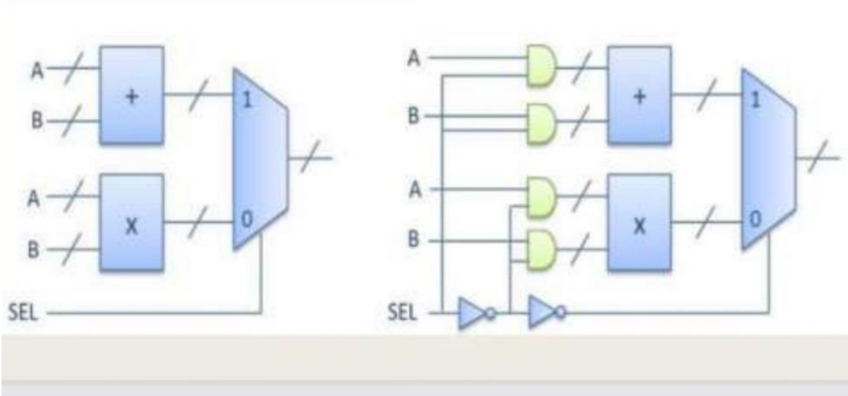
- By converting load enable circuits to clock gating circuit dynamic power can be reduced. Normal clock gating circuit consists of an AND gate in the clock path with one input as enable. But when enable becomes one in between positive level of the clock a glitch is obtained.

- To remove the glitches due to AND gate, integrated clock gate is used. It has a negative triggered flop and an AND gate.



39. Operand Isoation:

Operand isolation is a technique for minimizing the power consumption associated with combinational circuit operations by selectively blocking the propagation of switching activity through the circuit.



40. Mixed Vt optimization:

- Generally VT Swapping is used for optimizing both power and timing.
- By using this technique for optimization, the area remains unchanged.

For Timing :

- If the design is timing constrained, then we use HVT cells for the design.
- For the timing critical paths we swap,

HVT with SVT

(or)

SVT with LVT

For Power :

- If it is a low power design, then we use LVT cells for the design.
- For high switching cells we swap,

LVT with SVT

(or)

SVT with HVT

41. Why LVT cells are more leaky?

Below the Vt voltage also there will be some amount of current which is known as sub-threshold current. So for LVT very small amount of voltage will be enough for the sub threshold current. This sub-threshold current is the major factor for leakage in LVT cells.

42. Physical Layout estimation(PLE):

- PLE, Only requires Cap Table as an additional input, which will be used to estimate the net RC from Cap table instead of LEF.
- RC Eliminates WLM's with "Physical Layout Estimation (PLE)" Technique.
- Good timing results at 90nm node and below.
- Area grows about 5-10% more.

43. Spatial Synthesis:

It assumes PLE inputs + DEF (Floorplan). It does some Placement of the block and thus minimize the net lengths.

Synthesize_to_mapped -spatial

44. Physical Synthesis:

Physical Synthesis begins with a mapped netlist generated by logic synthesis and it have the capability of PnR. The target of PS is to achieve the minimum area usage at the required speed for a design.

45. Netlist Unification:

Every module/cell in the design should have an unique name.

CMD: checkUnique

If the netlist is unique, then it results 1, otherwise 0.

46. Incremental Synthesis:

Synthesizing the design without touching the already timing met paths is called Incremental Synthesis.

47. Logic Equivalence Check(LEC):

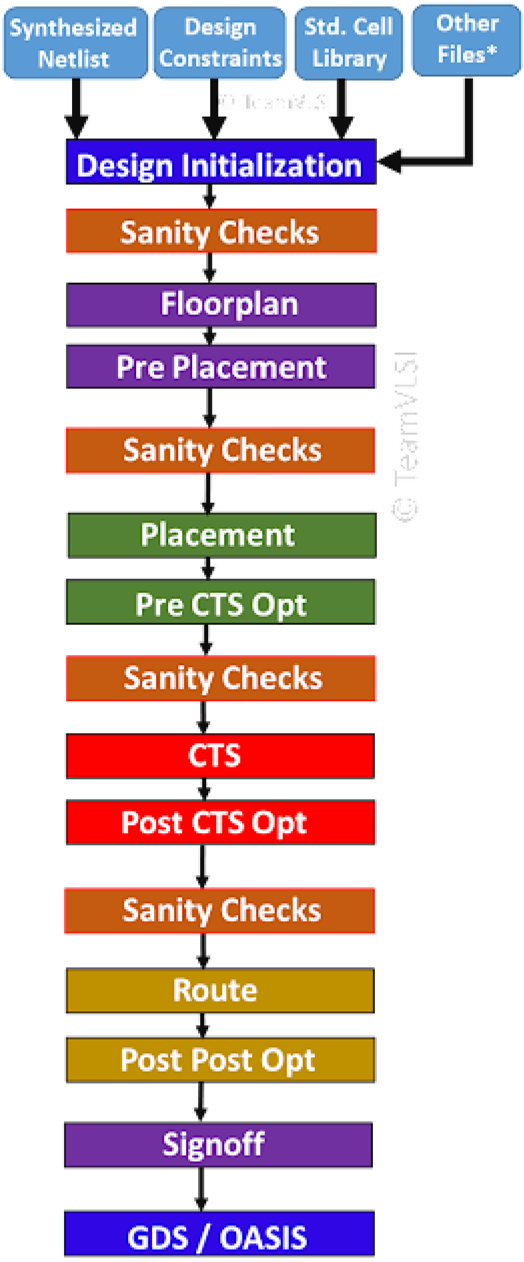
It looks at the combinatorial structure of the design to determine if the structure of two alternative implementations will exhibit the same behavior. It compares the RTL and Gate Level Netlist and checks for differences in structure of the design.

48. Activity Factor:

The activity factor is the probability that the circuit node transitions from 0 to 1 because that is only the time the circuits consume power. A clock has an activity factor $\alpha = 1$ because it rises and falls every cycle. The activity factor is powerful and easy to use lever for reducing power.

Place and Route

1. PnR Flow:



2. Inputs of PnR:

- Netlist(.V)
- Updated SDC(Standard Design Constraints)
- .lib (Liberty or Library file)
- .lef(Library Exchange Format)
- TLU+ (Table Look Up)
- Captable File
- UPF(Unified Power Format).

3. **DEF (Design Exchange Format):**

   DEF File is a text file which consist of :

   - Placement info
   - Pin Locations
   - Metal Blockages
   - Orientation
   - Macro Placement Info

4. **UPF (Unified Power Format):**

   UPF contains :
   - supply set definition,
   - power domain definition,
   - power switch definition
   - retention cell definition
   - level shifter cell definition and other low power related definition.

5. **TLU(Table Look Up):**
   It is a table containing wire capacitance at different net length and spacing. contain RC coefficients for specific technology.
6. **Manufacturing Deviations:**
   Minimum spacing rules to be followed to consider manufacturing deviations, otherwise adjacent nets gets shorted if the deviation on the adjacent nets is opposite.
7. **Pitch:**
   The distance between the centre to centre of the metal is called as pitch.
8. **Offset:**
   Offset is the distance between the core and first metal layer.
9. **Core:**
   A 'core' is the section of the chip where the fundamental logic of the design is placed.
10. **Die:**

    Die is the combination of core area and I/O pad area.

11. **Package:**

    The package is a case that surrounds the circuit material to protect it from corrosion or physical damage and allow mounting of the electrical contacts connecting it to the printed circuit board (PCB).
12. **I/O Pads:**
    - Input/ Output circuits (I/O Pads) are intermediate structures connecting internal signals from the core of the integrated circuit to the external pins of the chip package.
    - Typically I/O pads are organized into a rectangular Pad Frame.
    - The input/output pads are spaced with a Pad Pitch.

13. I/O Voltage:

The Voltage which powers the I/O Pads.

14. Core Voltage:

Core voltage *is the voltage which powers the Logic Blocks ,logic cells in the core area.*

15. OBUF:

Output Buffer is used to drive the signal from the design to the external output pads.

16. IBUF:

Input Buffer is used to drive the signal from the external pads to the design.

17. Level Shifters:

Level Shifters (LS) are special standard cells used in Multi Voltage designs to covert one voltage level to another.

18. STD.Cell Utilization:

The ratio of the total std. cell area to the core area is known as std. cell utilization.

19. Core Utilization:

The Ratio of the std.cell area, macro area and blockage are to the total core area.

$$Core\ Utilization = \frac{Std.cell\ area + Macro\ area + Blockage}{Total\ Core\ Area}$$

25. Aspect Ratio:

It is the Ratio of the Height of the core and the Width of the core.

$$Aspect\ Ratio = \frac{Height\ of\ the\ core}{Width\ of\ the\ core}$$

26. Abutting:

In Abutting type design there will be no space between the two blocks. So that these blocks touch each other.

27. PG Mesh:

Each of these stripes run both vertically and horizontally at regular interval then this is called power mesh.

30. Site:

The smallest unit of placement where the smallest cell can be placed is called as SITE.

31. IA:

A via is an electrical connection that establishes the connectivity between two layers.

32. Follow Pin:

A follow pin connects VDD and VSS pins of all std. Cells to the power mesh.

33. SSO Analysis:

34. Timing Driving Placement:

Tool tries to place the standard cells along timing critical path close together to reduce net RC and meet setup timing.

35. Congestion driven placement:

Tool tries to spread the cells where the density of cells are more for the reduction of congestion.

36. Core Limited Design:

Core logic dictates the die dimension is called core limited design.

37. Pad Limited Design:

I/O pads dictates the die dimension is called pad limited design.

38. Design Partitioning:

Partitioning is a process of dividing the chip into small blocks. This is done mainly to separate different functional blocks and also to make placement and routing easier.

39. Manufacturing Grid :

The minimum metal length that can be manufactured is called manufacturing grid.

40. Routing Tracks:

Routing Tracks are imaginary lines that tools would divide the whole routing area. Tool use these tracks as a reference for routing the nets. While routing tool will route such that routing tracks falls exactly to center of the route.

41. Macro:

Macros are the memory cells. There are two types of macro:

- Hard Macro (Placement is Fixed)
- Soft Macro (Can be moved while optimizing the design).

42. Fly-line Analysis:

Fly line analysis is the virtual lines which shows the connections between the blocks, While doing manual floor planning.

43. Floorplan Guidelines:

- All the macros should be placed at periphery of the core boundaries but not at the center of the core.
- Macros are to be placed such that pins must face towards the core area.
- Macros should not contain criss crossing.
- There must be a space between two macros.
- The space between a macro and core boundary is = (Total no. of pins/No. of vertical layers) x pitch
- Halo should be specified around the macros.
- Notches should be avoided.

44. Types of Blockages:

Blockages are used to avoid the congestion in our design. There are 2 types of blockages

- Placement Blockage.

  (a) Soft Blockage:

  This Blockage allows only optimization cells to be place in it.

  (b) Partial Blockage:

  It allows only specified percentage of cells to be placed.

  (c) Hard Blockage:

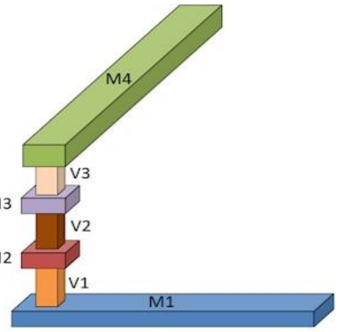
  It does not allow any cells to be placed.

- Routing Blockage.

  It allows only some specified metal layers inside the blockage.

45. Stack Via and Via Array

- A stacked via consists of multiple vias layered directly on top of each other.
- Array vias are used for connecting wide wires where the required cut size would exceed the maximum cut size of the simple via.



STACK VIA

ARRAY VIA

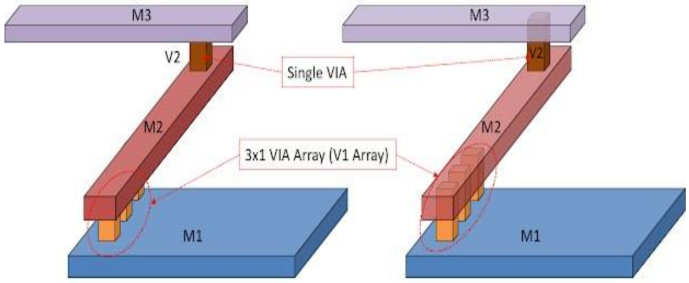


Fig: 3D_c

Fig: 3D_d

46. Halo:

Halo is special hard blockage around the macro which blocks the placement of std. cells near the macro.

47. Physical Cells:

These cells are not present in the design netlist. if the name of a cell is not present in the current design, it will consider as physical only cells. they do not appear on timing paths reports they are typically invented for finishing the chip.

48. Tap Cells:

- Used to avoid the latch.
- It creates low impedance path between the VDD and VSS.
- Well tap connects N-Well to VDD and P-Sub to VSS.
- It is place in pre-placement stage.

CMD : addWellTap -cell FILL1 -cellInterval 60 -fixedGap -InrowOffset 30 -StartRowNUM 2 -SkipRow 1 -Prefix WELLTAP

49. Tie Cells:

- Used to connect constant High and Constant Low.
- Its Creates high impedance path between power rail & gate of cell.
- It is placed in placement stage

CMD : addTieHiLo -cell “NAME” -Prefix “NAME”

50. END CAP cells:

- Used to avoid cell damage which are placed at core boundary & to main row continuity.
- These are placed at pre-placement stage.

CMD: addEndCap -preCap FILL1 -PostCap FILL1 -Prefix ENDCAP.

51. De Cap cells:

- Used to fix IR issue in power grid.
- These cells are placed between VDD and VSS.
- These are placed at power planning stage.

CMD: addDecapCellCandidates DECAP10 10

addDeCap -totCap 1000 -cells DECAP 10 DECAP 9

52. Spare Cells:

- Used to fix bugs in functionality at the time of tape out.
- These cells are connected to VDD and VSS through the Tie Cells.
- Generally, we use 2-3% of spare cells in design.
- These are placed at placement stage.

CMD: SpecifySpareGate -Cell “NAME”

53. Filler Cells:

- Used to maintain N-well continuity.
- These are placed after the routing stage.

CMD: addFiller -Cell “FILL1” -Prefix “FILLER”

54. Double Cut Via:

If two vias are provided for each connection point, such via is called a "double-cut via".

55. Redundant Via:

The occurrence of via defects Increases due to the shrinking size in integrated circuit manufacturing Redundant via insertion is an effective and recommended method to reduce the yield loss caused by via failures In this paper we introduce the redundant via allocation problem for layer partition based redundant via insertion methods

56. Cell Padding:

- Cell padding is used to avoid the congestion caused by high pin density cells. For these cells we reserve some site by using cell padding technique.
- Cell padding is done for specified cell name in the design.

57. Instance Padding:

- This is done for particular instance in the design.

58. Scaling factor:

To co-relate the delays between PnR tool and signoff tool we are using scaling factors. By using scaling. factors co-relation differences are included in advance in PnR tool. So that in sign-off tools the timing and RC values almost match with final sign-off quality tools. Hence the iterations are reduced.

59. Trail Route:

Trial Route will give idea on routing congestion at early stage so that one can avoid iterations and save timing.

60. Gcell:

The chip is divided into small blocks. These small blocks are called routing bin. The size of the routing bin depends on the algorithm the tool uses. Each routing bin is also called a GCELL.The size of this gcell depends on the tool.Each gcell has a finite number of horizontal and vertical tracks.

61. Over-Commiting:

If tool uses already used routing tracks, then it is called Over-Comitting.

62. Congestion:

When the number of routing tracks available for routing in a given location is less than the number necessary, the area is considered congested and hence, is termed as congestion.

63. Area Reclamation:

It is optimizing area without affecting timing.

Ex: Replacing high drive strength with low drive strength cells where ever possible.

64. CTS:

The process of distributing the clock to all sequential elements and balancing the minimum skew is called CTS.

65. Goals Of CTS:

- Minimum Skew
- Minimum latency
- DRV's

66. Leaf Pin:

The flop pin where the cts stops balancing the skew is known as leaf pin.

67. Root Pin:

The start point of the clock is called root pin.

68. Clock Insertion Delay:

The delay between the source of the clock signal and the flip-flop clock pin is known as Clock Insertion Delay.

69. Through Pin:

All clock pins of a generated clock flop.

70. Macro Model:

We specify the Insertion delay inside the macro as macro model for proper balancing the skew.

71. **Rise Skew:**

It is the max difference of all the arrival times of the clock signal at the leaf pin inputs as measured from rising edge at the clock root.

72. **Fall Skew:**

It is the max difference of all the arrival times of the clock signal at the leaf pin inputs as measured from falling edge at the clock root.

73. **Trigger Edge:**

It is based on all the arrival times of the clock signal at the leaf pin input.

74. **Bogus I/O Slack:**

After CTS In to Reg paths slacks would get improved by the amount of clock insertion delay and reg to out timing get deteriorated by the amount equal to clock insertion delay.

75. **Exclude Pin:**

Exclude pin are clock tree endpoints that are excluded from clock tree timing calculation and optimization. The tool considers exclude pins only in calculation and optimizations for design rule constraints. During CTS, the tool isolates exclude pins from the clock tree by inserting a guide buffer before the pin or these pins are need not to be considered during the clock tree propagation.

Example - Non clock input pin of sequential cell.

76. **Float pin:**

Float pins are clock pins that have special insertion delay requirements and balancing is done according to the delay [Macro modelling]. This is same as sync pin but internal clock latency of the pin is taken into consideration while building the clock tree. To adjust the clock arrival for specific endpoints with respect to all other endpoints.

Example - Clock entry pin of hard macros.

77. **Stop pin:**

Stop pins are the endpoints of clock tree that are used for delay balancing. In CTS, the tool uses stop pins in calculation & optimization for both DRC and clock tree timing.

Example - Clock sink are implicit stop pins.

The clock signal should not propagate after reaching the stop/sync. This pin needs to be considered for building the clock tree.

78. Detail Route:

- Detailed routing follows up with the track routed net segments and performs the complete DRC aware and timing driven routing.
- It is the final routing for the design built after the CTS and the timing is freeze
- Filler Cells are adding before Detailed Routing
- Detail Routing is done after analyze the cause for congestion in the design, add density screen or change floorplan etc.

79. Max_dept :

This parameter indicates no. of logic levels that tool can trace through before CTS is done.

80. RC Corners:

RC Corners are the wire delay corners which we use for timing analysis

- RC_Worst
- RC_Best
- C_Worst
- C_Best

81. SPEF(Standard Parasitic Extraction Format):

- SPEF mainly contains extracted RC values of every single net in the design.
- It is the input to the STA where we can get accurate RC delays of the net.

82. Design Modes:

- MBIST MODE
- JTAG MODE
- SCAN SHIFT MODE
- SCAN CAPTURE MODE

- FUNCTIONAL MODE.

83. Rise and Fall Glitch:

Whenever one net switches from low to high and other neighbouring net is supposed to remain constantly low, will get affected by the switching net due to the mutual capacitance in that case we have a **rising glitch** on it.

Whenever one net switches from high to low and other neighbouring net is supposed to remain constantly high, will get affected by the switching net due to the mutual capacitance in that case we have a **falling glitch** on it.

84. Increase in Cell Delay (Factors):

- Input Skew
- Library Setup Time
- Operating Conditions
- Wire Load Models
- Input Transition
- Output load Capacitance.

85. Glitch Analysis:

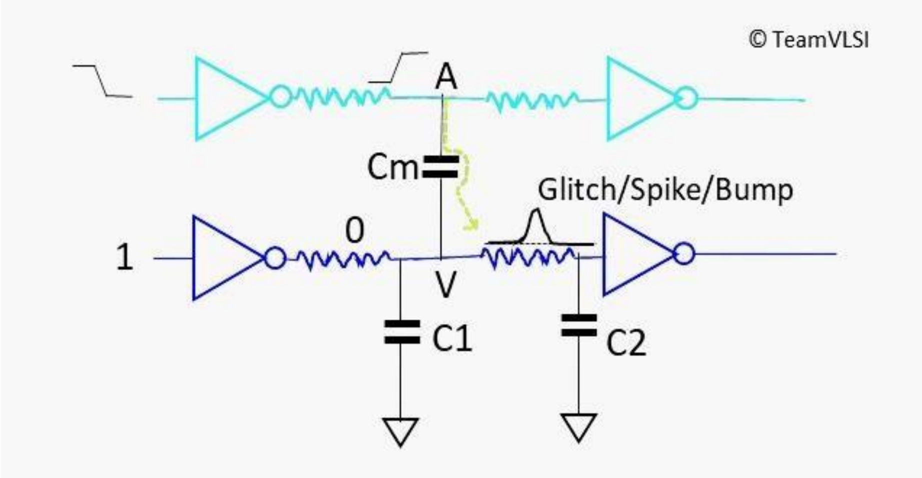
- Glitch analysis depends upon the height because of this height it could be safe or unsafe.
- If the glitch height is in between V_{ol} and V_{il} then it is safe.
- If the glitch height is in between V_{ih} and V_{oh} then it is unsafe.
- If the glitch is in between undefined region then it is unpredictable.
- The glitch height depends upon the factors
    - Coupling Capacitance

      h a $\frac{Cm}{C1+C2}$

      Cm a $\frac{1}{D}$

    - In lower node technologies the distance(D) $\downarrow$ Cm $\uparrow$ So the height(h) is more. So the glitch will be in unsafe.

- Aggressor drive strength is more, the slew rate is faster, higher the crosstalk.
- Victim drive strength is more, lower the crosstalk.



86. Delay Analysis:

The sole distinction between crosstalk delay and crosstalk noise is that the nets are not at steady state values and some switching activities are occurring on both the victim and aggressor nets. The propagation orientation of the aggressor and victim nets influences crosstalk delay. This causes either a slower or quicker transition of victim nets.

87. Dishing:

This refers to an increase in the surface topography of a composite structure, primarily due to the difference in CMP removal rate between the two (or more) materials of the composite. The dishing occurs in the material component with a higher removal rate.

88. Erosion:

The SiO2 Erosion is defined as the difference in the SiO2 thickness before and after the polish step.
http://www.vlsi-expert.com/2015/08/dishing-and-erosion-cmp.html

89. Clock Tree Jitter:

It can be defined as “deviation of a clock edge from its ideal location.”

90. Load Splitting:

- Load Splitting is the technique which adds the buffer in high fanout nets and divides the load.
- For max_tran violation we use this technique to reduce it.

91. DRC(Design Rule Check):

Design Rule Checking (DRC) verifies as to whether a specific design meets the constraints imposed by the process technology to be used for its manufacturing.

92. Module Constraints Types: Guide, Fence, Region

Sometimes we need to place a particular group of standard cells or modules in a particular area (box).

93. Fence:

- The fence is assigned with certain cells in the design.
- A fence does not allow the assigned cell to sit outside the box defined.
- A fence does not allow the other cells to sit inside the box also. So the area is exclusively reserved for the assigned cells.
- It is a hard constraint

94. Region:

- The region is assigned with certain cells in the design.
- A region does not allow the assigned cell to sit outside the box defined.
- It may cause congestion in the area assigned if not chosen the area wisely.
- The only difference between the region and the fence is that it allows the other cells to sit inside the box.
- It is a hard constraint

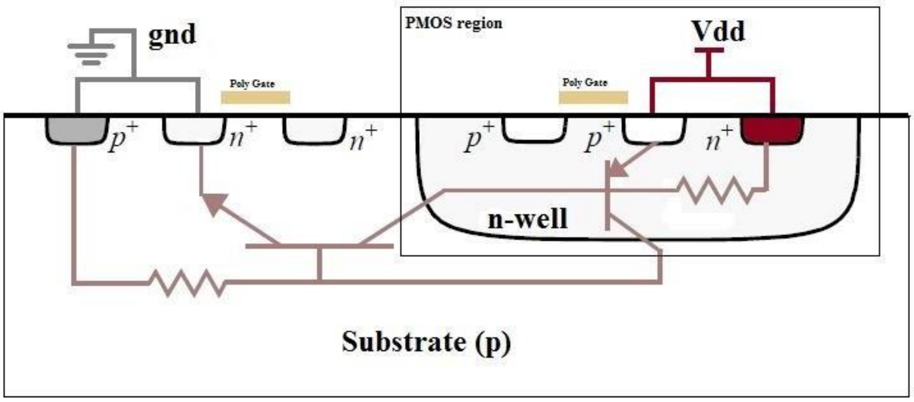
95. Guide:

- The guide is assigned to certain cells in the design
- The guide allows to assigned cell sit outside the box
- It also allows the other cells to sit inside the box.
- It is a soft constraint.

Sign-off:

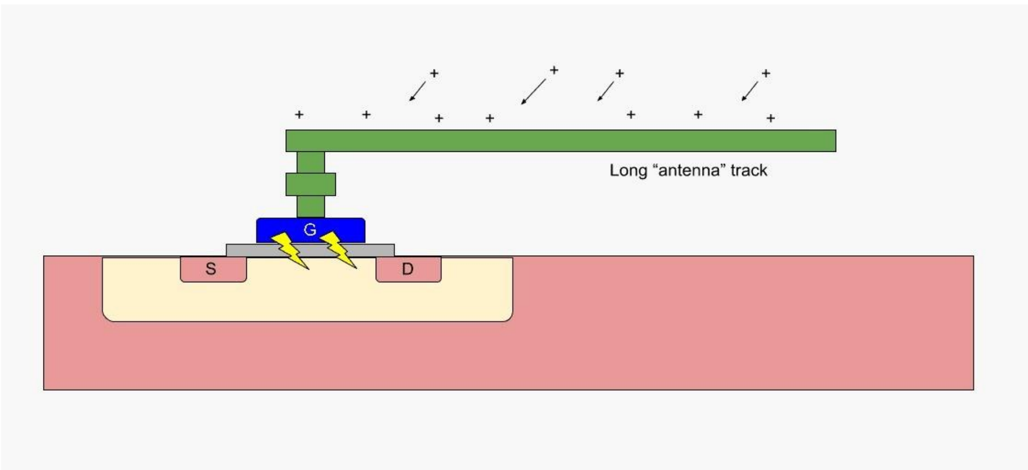
1. Latch Up:

Latchup refers to short circuit/low impedance path formed between power and ground rails in an IC leading to high current and damage to the IC. It occurs due to interaction between parasitic pnp and npn transistors. The structure formed by these resembles a Silicon Controlled rectifier (SCR).



2. Antenna Effect:

The oxide layer is often only a few molecules thick, and if enough charge builds up, the thin oxide layer breaks down, damaging or even completely destroying the MOSFET. This accumulation of charge is usually, and misleadingly, called the antenna effect.

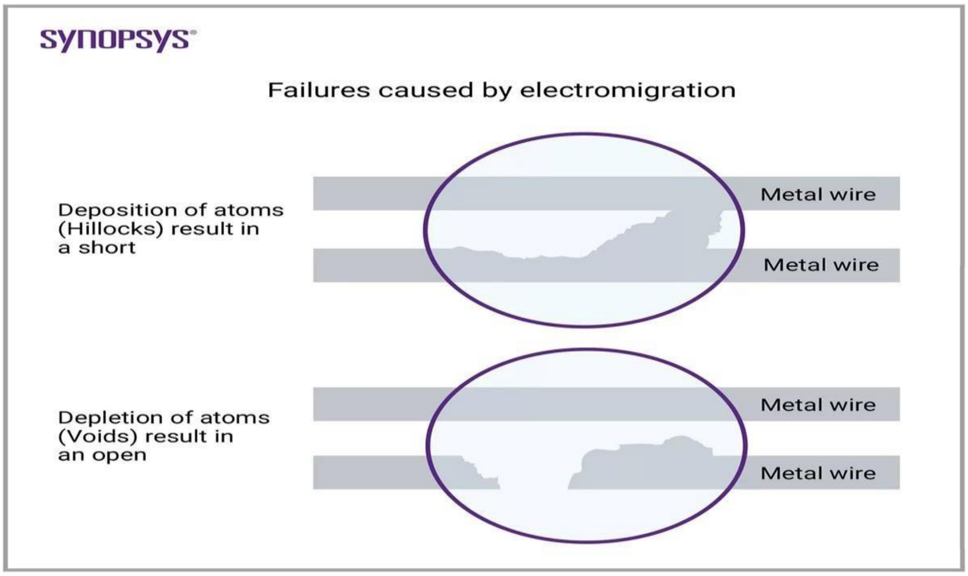


$$Antenna\ Ratio = \frac{Metal\ Area}{Gate\ Area}$$

3. **Electro Migration:**

Electromigration is the movement of atoms based on the flow of current through a material. If the current density is high enough, the heat dissipated within the material will repeatedly break atoms from the structure and move them. This will create both 'vacancies' and 'deposits'. The vacancies can grow and eventually break circuit connections resulting in open-circuits, while the deposits can grow and eventually close circuit connections resulting in short-circuit.

- Here the vacancies are called **voids**.
- The deposits are called **hillocks**.



4. **IR Drop:**

IR drop is the voltage drop in the metal wires constituting the power grid before it reaches the power pins of the standard cells. It becomes very important to limit the IR drop as it affects the speed of the cells and overall performance of the chip. There are two types of IR drops:

- Static - Vstatic_drop = Iavg x Rwire [Iavg are all factors of leakage currents]
- Dynamic - Vdynamic_drop = L (di/dt) [current L is due to switching current]

5. **Cross Talk:**

Crosstalk is a phenomenon that occurs when a signal carried on one net of a transmission system causes an undesirable effect in another net, due to coupling capacitance formed between them. The net which is effected is called victim net, the net which effects is called Aggressor.

6. **Overshoot and Undershoot:**

If a signal voltage level goes above the VDD value is called **Overshoot**.

If a signal voltage level goes below the VSS value is called **Undershoot**.

7. **ECO Flow:**

Engineering change order (ECO) refers to a practice in the VLSI design flow to accommodate specification changes, to rectify functional errors, or to fix non-functional design requirements, such as timing and power, with minimal disturbance to the existing implementation, to save as much as possible the already-spent optimization efforts.

8. **Metal Density Check:**

Density check is performed to check the even density through out the chip which required for manufacturing process to ensure the mechanical sturdiness of the chip to achieve planarity during CMP (Chemical Mechanical Polishing). Different density checks verify the overall density of each metal and densities per unit area.

9. **Why the Metal Fill is required?**

If there is lot of gap between the routed metal layers (empty tracks), during the process of Etching the etching material used will fall more in this gap due to which Over Etching of existing metal occurs which may create opens. So in order to have uniform Metal Density across the chip, Dummy Metal is added in these empty tracks.