Design & Comparative Analysis of Novel 8T and 6T SRAM Cell Using 16nm Technology.

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***Abstract*- Memory blocks are considered to be one among many important components in modern computing systems. Volatile memories namely DRAM, SRAM, and modern FLASH memory need constant voltage supply to store the information. This constant supply of voltage to store the information can be one of the reasons for power dissipation. DRAM memory has a disadvantage such as memory refreshing the memory block periodically, where the pre-existing data is removed and rewritten to maintain the integrity of the stored data. Some of the essential parameters such as SNM (Static Noise Margin), power dissipation, area consumption and delay are considered while designing any memory block. These memory blocks are selected based on the requirements of the application. This paper depicts extensive design and analysis of two different SRAM cell with various number of transistors. SRAMs are generally preferred due to faster access time in the range of ns, lower power consumption due to absence of refreshing, high reliability, and minimal power consumption during hold state. Various SRAM cells such as 6T, and novel 8T are designed and compared based on parameters – W/L ratios, average power dissipation, robustness against noise i.e., Static Noise Margin(SNM) and leakage current. The leakage current was at a maximum value of 169.9522pA in 8T and the least value was found to be in 6T cell at 66.1483pA. The Static Noise Margin of 6T was 0.3044 V whereas newly proposed Novel 8T had 0.1677 V. Similarly, 6T cell dissipated maximum power of 665.59nW whereas the average power dissipated is minimum by the proposed 8T at 74.685nW. The simulation such as DC analysis and transient analysis was carried out using LTSpice. The layout of the Novel 8T SRAM cell was drawn and various verification process such as DRC and LVS was performed using Cadence Virtuoso Tool Suite.**

Keywords— LTSpice, Cadence virtuoso, layout, SNM, leakage current, row decoder, column decoder, RBL, RWL.

I. Introduction

Memory blocks are integral part of an IC or a computing system which is utilised to store information that could be related to the CPU instructions or other form of data. Static RAM is one of the many types of volatile memory that resides on an IC. This type of memory is prominently used as cache memory which bridges gap between high-speed CPU registers and the Main Memory. These high-speed read-write operations demand SRAMs to be incredibly fast and energy efficient. With constant improvement in technology in terms of reduction in feature size and introduction of new architectures, extensive research is constantly conducted to minimize power dissipation, delay reduction and to improve robustness of the circuit by reducing susceptibility toward noise. With plethora of architectures available, a designer has to select the best one depending on the constraints and requirements of the application and these requirements could be minimal area consumption or reduced power dissipation. Considering these constraints this paper details the comparative study on 2 different SRAM memory architecture namely 6T and Novel 8T. Based on the comparison the architecture with relatively better result is chosen and its layout is drawn using cadence virtuoso, gpdk45 technology library.

II. Background Review

Research [1] suggests an efficient architecture by eliminating the traditional transistor used to access and adding a transistor to perform read operation and another transistor to drive memory, lead to increase in overall stability of the cell during read operation. As opposed to conventional 6T SRAM cell, in the modified design, in order to perform read and write operation only the bit line is charged. This led to significantly lowering of power consumption during read and write operation. The removal of NMOS transistor, ensures the memory node to be always pulled up to logic high V_{DD} resulting least write 1 delay. In contrast, due to the same reason writing 0 consumes more time. In research [7] Near-threshold computing – one among the voltage computing technique deployed to reduce consumption of power and cost by simultaneously increasing reliability. The undertaken research is aimed at utilising one read line, replacing the usage of 2 read lines, found in a traditional 6T SRAM cell. 8T cell has been proven as a reliable architecture. While performing read operation, traditional 6T SRAM cell works without any error during NTC voltage. There is reduction in current leak, approximately about 45 percent and area consumed of the cell is minimised by about 30%. In Research [13], it has been proposed a 10T cell consuming low power when in comparison to traditional 6T SRAM cell. The mask layout drawn using 45nm technology library shows reduced area consumption by 15% in comparison to Schmitt-trigger based 10T SRAM architecture. Similar to any other digital circuit this design must also be chosen based on the trade-off, which leads to delayed read access time and not so significant improvement in SNM. In [14] researcher has designed 9T cell having different data and bit line while performing read operation. We could observe notable improvement of SNM,

increased by about 2 times in comparison to traditional 6T. To minimize power consumption during IDLE state, the cell is driven to "super sleep cut-off mode" reducing amount of power consumed by about 23% in comparison to 6T cell of 65nm technology node. Further validating the enhancements of the read stability.

III. Methodology

The implementation flow of the research was started by implementing the schematic of the row/column address decoder and verifying it against the truth table of the decoder. Similarly, 6T and new 8T SRAM cell is implemented using schematic and their parameters such as power consumption, leakage current, and SNM are calculated and compared to obtain the best among them. The layout of the 8T cell was also executed on Cadence virtuoso using technology node gpdk45. The layout of the 8T cell was achieved by using 3 metal layers in order to provide flexibility to the SoC engineers to use higher order metal layer to route other sections.

IV. Working

A. Row/Column Address Decoder

Row and Column decoders play a vital role in a memory block. They are responsible for selection of a particular row and column while performing operations such as read and write.

Row decoders are responsible for controlling the access transistors via wordline whereas the Column decoders control the data that needs to be written into the cross-coupled inverter via bit and bit_bar lines.

The designing depends on the Boolean expressions for each output because of which truth table is necessary. Their working can be explained using their schematic designs which were designed using the Boolean expressions.

A	B	C	D	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Fig. 1. Truth table of 4 : 16 decoder

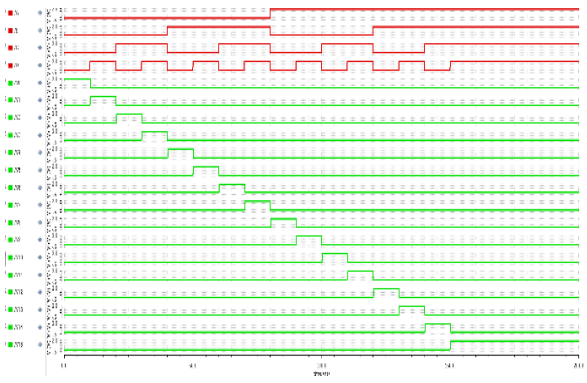

Fig. 2. Timing diagram of 4:16 decoder

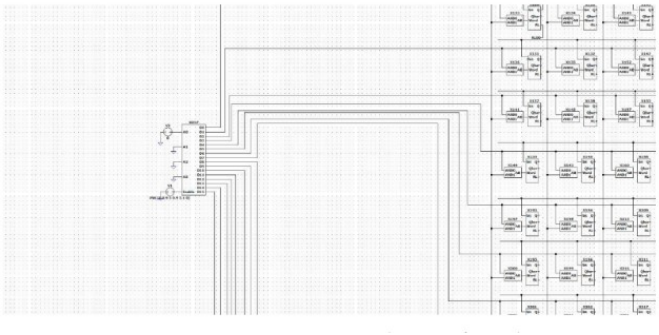

Fig. 3. Schematic of decoder

B. 6T SRAM Cell

Write Operation

In order to write value to the RAM cell, bit line is charged and the complement value is intrinsically pushed into bit_bar line due to the cross-coupled inverter. During this process the accessing transistors are enabled by driving the Word line high.

Read Operation

In order to read value of a cell, both bit_bar and bit lines are pre-charged to logic high V_{DD} and simultaneously word line that control access transistor is driven high. Assume Q has a value 1 and Q_bar is 0, while reading, the pre-charged bit line retains the value 1, in contrast the bit_bar discharges to ground due to potential difference and have value 0.

Hold Operation

To hold a value in a cross-coupled inverter the word lines are driven low, disabling the access transistors. As the access transistors are disabled the charge and discharge paths are blocked leading to previous value preservation.

TABLE I. Aspect Ratio (W/L Ratio) of 6T

Transistors	*W/L ratio (nm)*
M4, M6	20/16
M3, M5	12/16
M1, M2	12/16

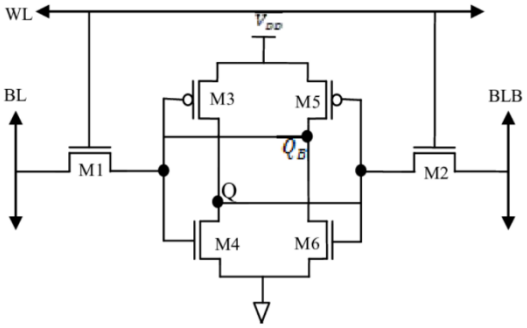

Fig. 4. Schematic of Traditional 6T SRAM

C. NOVEL 8T Architecture

Write Operation

To write a value into the cell, the write line will be pulled up to V_{DD} to enable access transistors and values of bit and the

complement bit_bar line will be written to cross-coupled inverter similar to 6T cell write operation.

Read Operation

While in read operation, write net is driven to GND and simultaneously read line will be pulled high. Either nMOS or the pMOS is turned on based on its pre-existing bit value present on the Q_bar and the Q value is extracted via read(RL).

Hold Operation

While during hold operation, lines read and write is driven to GND, disabling the access transistor, consequently, bit values in the cross-coupled inverters are retained.

TABLE II. ASPECT RATIO(W/L RATIO) VALUES OF 8T CELL

Transistors	*W/L ratio (nm)*
M6, M7	16/16
M3, M8	28/16
M4, M5	16/16
M1, M2	32/16

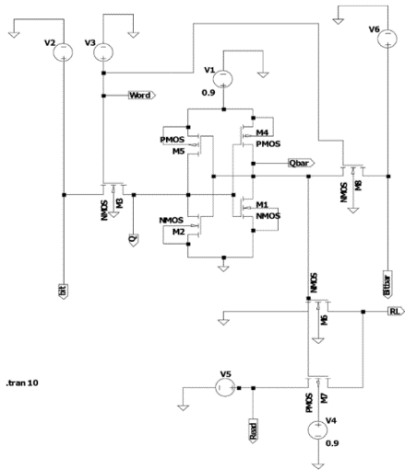

Fig. 5. Schematic of Novel 8T SRAM Cell

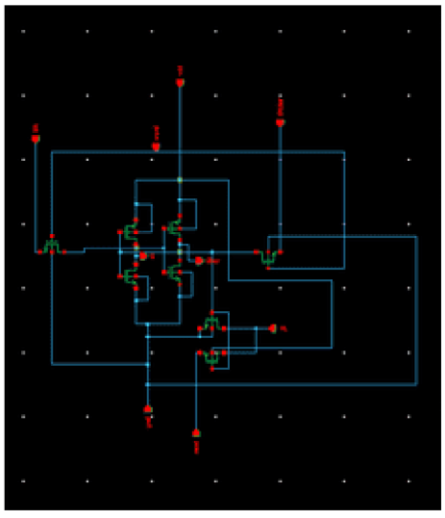

Fig. 6. Schematic of Novel 8T SRAM architecture using Cadence Virtuoso

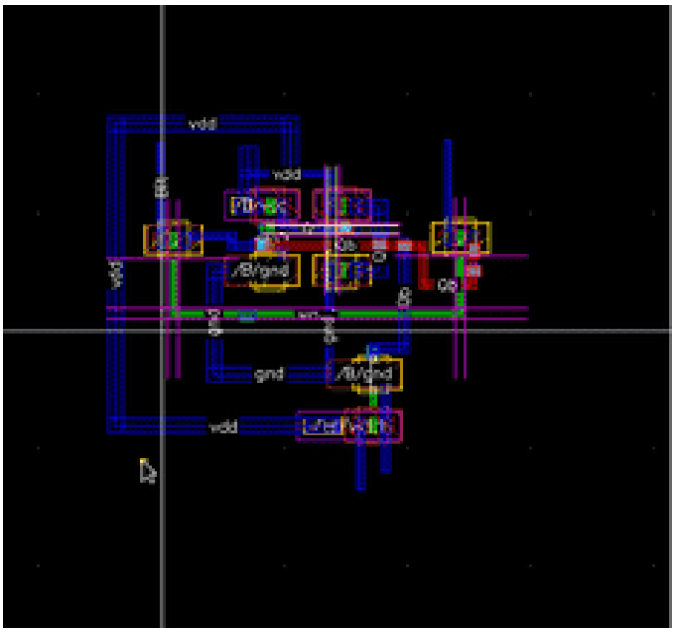

Fig. 7. Layout diagram of Novel 8T SRAM architecture

The layout diagram of the 8T architecture was also executed on Cadence virtuoso using technology node gpdk45. The layout of the 8T cell was achieved by using 3 metal layers in order to provide flexibility to the SoC engineers to use higher order metal layer to route other sections.

V. SIMULATION RESULTS AND OBSERVATION

Simulation of both SRAM cells were performed using open-source LTSpice. The parameters explained below were compared during the course of this study.

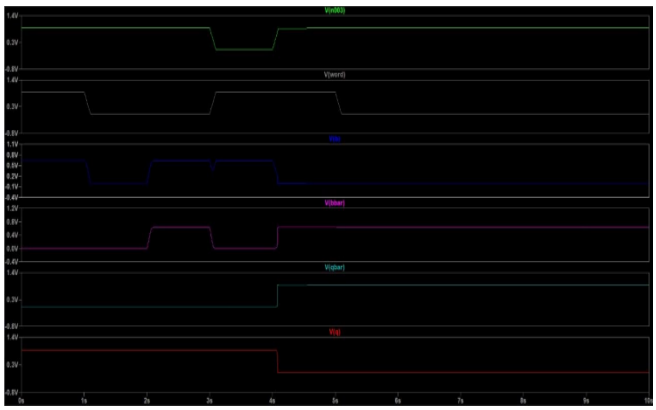

Fig. 8. Transient Analysis of 6T SRAM Cell

Figure[8] depicts the simulation result of traditional 6T SRAM. When the word line is high, simultaneously bit line is charged to logic high 0.9V and the bit_bar line is dropped to 0, therefore write operation takes place and a logic 1 is written into the memory, seen at Q. At time 2s bit line and bit_bar line is pulled up to 0.9V and at t=3s the pre-charge circuit is made to go low and the word line is made high, hence read operation is performed. Therefore, during the read operation the values present in Q that is logic 1 is written into bit line. From t=4s the word line is kept high and the bit line is pulled down to 0 and immediately bit bar line pre-charge's to logic 1 hence a logic 0 is written and stored into the memory as seen by the value present in Q and the negated value is present at Q_bar.

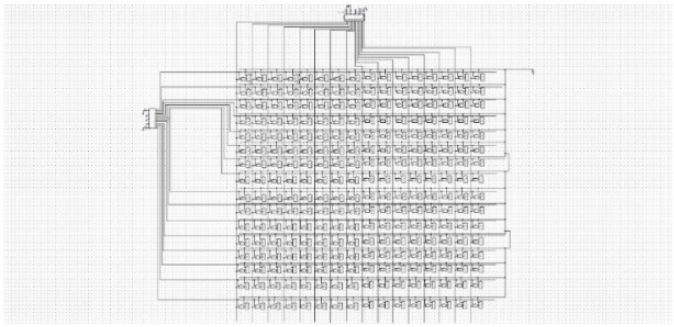

Fig. 9. Schematic of 16 x 16 SRAM memory array

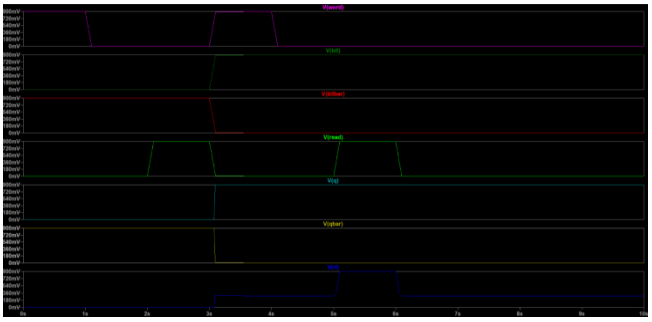

Fig. 10. Transient Analysis of Novel 8T SRAM Cell

Figure [10] displays the simulation result of Novel 8T SRAM. At t=0s, word line is charged to 0.9V and bit and bit_bar are further charged to 0V and 0.9V respectively hence a value of logic low 0 value is written into the cell as seen by the value present at Q. While performing the operation of reading, the read line is pulled high to V_{DD} and the word line is pulled to GND. Therefore, at t=2s the value present in Q that is logic 0 is read at the rl line. Similarly at t=3s word line is pulled up again and bit line is charged with logic 1, therefore as seen at Q a logic 1 is written into the cell successfully. At t=5s word line goes low and the value of read line is driven high for read operation and the value logic 1(value present at Q) is successfully read at the rl line.

Static Noise Margin – SNM is a measure of how much noise can a cross-coupled inverter sustain before reaching don't care state. The butterfly method of SNM calculation is used in this study.

$$NM_H = |V_{OHmin} - V_{IHmin}|$$

Where, NM_H is logical high noise margin. V_{OHmin} is the minimum output voltage level recognized as logic high and V_{IHmin} is the minimum input voltage level which is recognized as logic high.

$$NM_L = |V_{ILmax} - V_{OLmax}|$$

Where, NM_L is logical low noise margin. V_{OLmax} is the maximum output voltage level recognized as logic low and V_{ILmax} is the maximum voltage level which recognized as logic low (0).

TABLE III. SNM VALUES OF 6T AND NOVEL 8T SRAM ARCHITECTURE

Cell Architecture	*Static Noise Margin (V)*
6T	0.3044
Novel 8T	0.1677

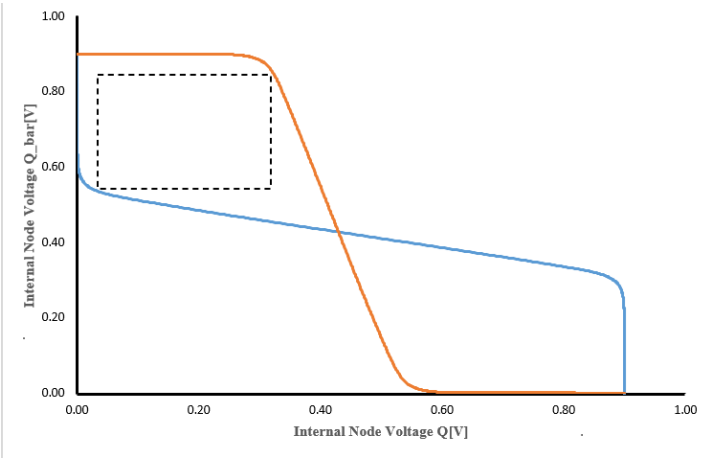

Fig. 11. SNM curve of 6T cell.

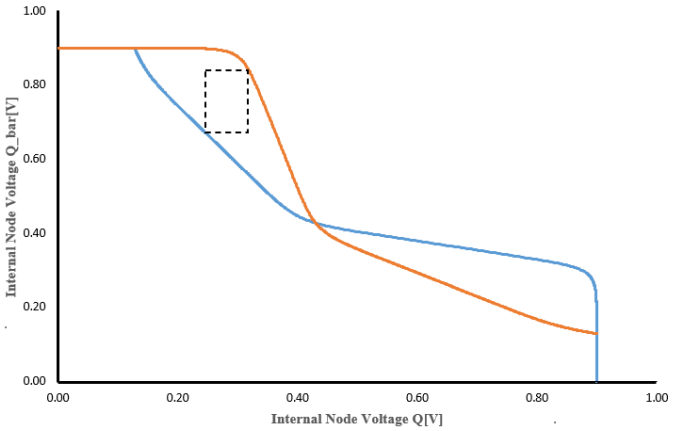

Fig. 12. SNM curves of Novel 8T cell.

Leakage Current- It is the flow of current caused due to the reverse-biased diodes formed at the junction of sources and drains in a transistor, which account to the power dissipation and can reduce robustness of the cell. Similarly, subthreshold current is occurring due to flow of current from the drain to source in a transistor during off state. The subthreshold current if given from [6] as

$$I_{sub} = A_{sub} \exp\left(\frac{q}{n'kT}(V_{GS} - V_{t0} - \gamma' V_{SB} + \eta V_{DS})\right) \times \left(1 - \exp\left(-\frac{q}{kT}V_{DS}\right)\right)$$

Where $A_{sub} = \mu C_{ox} W/L_{eff}(kT/q)^2 e^{1.8}$) is zero-biased mobility. C_{ox} is given as gate oxide capacitance of the transistor per unit area W, L_{eff} depicts effective length and width, k is Boltzmann constant, absolute temperature T, and electric charge of e^- 1. is zero bias threshold voltage V_{t0}, linearized body-effect coefficient γ', (DIBL) coefficient η, subthreshold swing coefficient of the transistor η'.

TABLE IV. LEAKAGE CURRENT OF 6T AND NOVEL 8T SRAM CELL

Cell Architecture	*Leakage Current (pA)*
Novel 8T	169.9522
6T	66.1483

Power Dissipated – It is the sum of power due to static nature i.e.. leakage currents and dynamic power due to switching capacitive loads between voltage states and are tabulated below.

$$Power = V_{dd} * I_{dd}$$

TABLE V. POWER DISSIPATION OF 6T AND NOVEL 8T SRAM CELL

Cell Architecture	***Average Power Dissipated (nW)***
6T	665.59
Novel 8T	74.685

The above Table V clearly depicts proposed 8T dissipating substantially less power in comparison with the traditional 6T cell, this is because while in read cycle, the word line is pulled to GND, due to which access transistor is turned off and do not dissipate power like 6T SRAM cell.

VI. CONCLUSION

This paper compares 2 types of SRAM architecture 6T and proposed Novel 8T based on various essential parameters. A novel 8T cell has outperformed the traditional SRAM cell with respect to amount of power dissipated. The focus our research was to compare and analyze their robustness by calculating SNM, power dissipated and amount of leakage currents. A particular architecture cannot be concluded best as each has its own merits and demerits depending on the trade-off parameters such as power dissipated, robustness and area consumed and these are selected based on the design requirement i.e., application. The above-mentioned results depict, 8T SRAM cell could be instinctively selected for low power design application because it draws about 47% less power compared to 6T with similar leakage currents. Making it well suitable for high speed and demanding applications. As mentioned earlier selection of a single architecture finally depends on the designer and the trade-off to choose one cell that best fits the application.

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