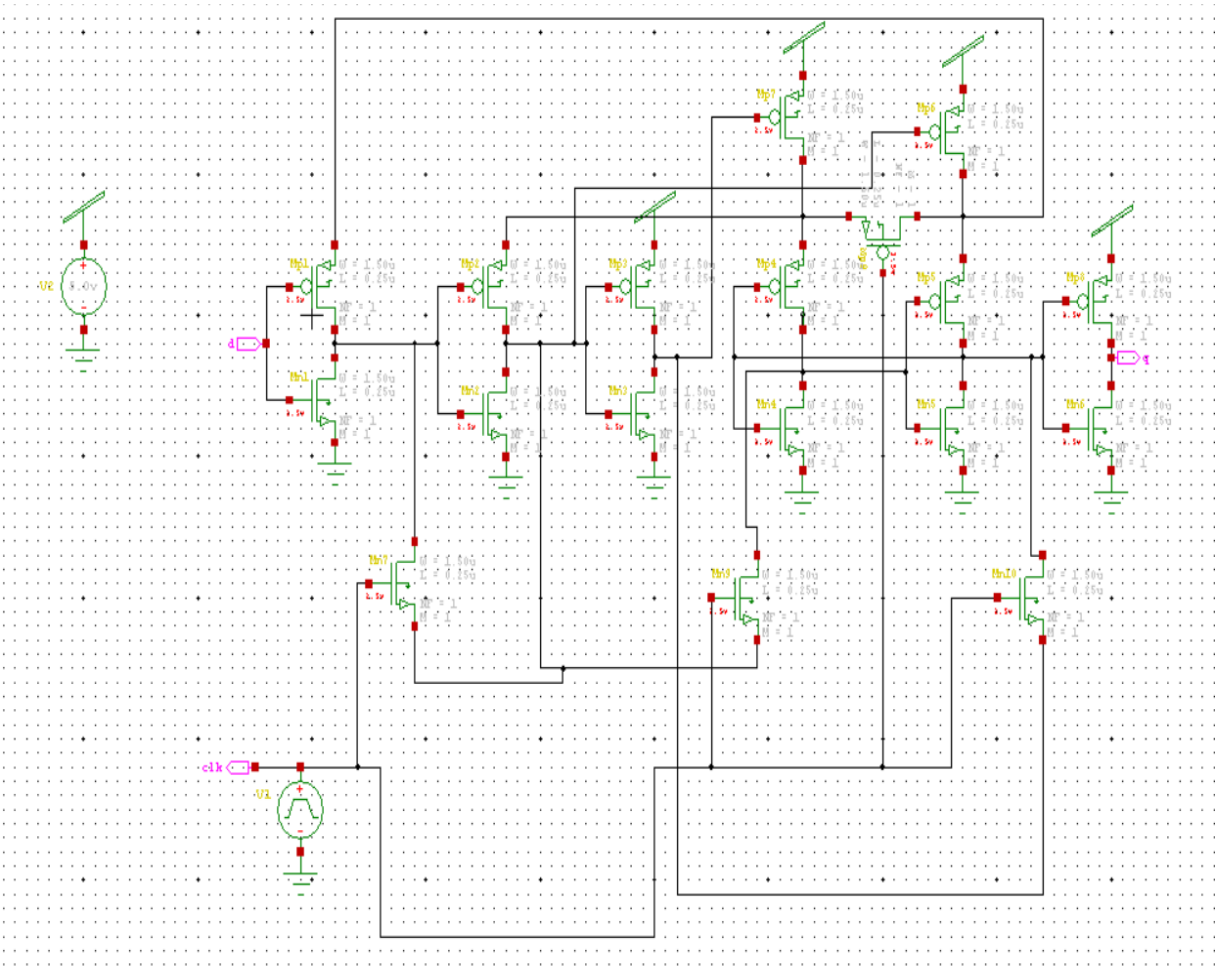
CHART PREPARATION

Aim: To design and simulate A Static High Frequency 18T Hybrid Flip-Flop Design for Low Power Application using TANNER EDA.

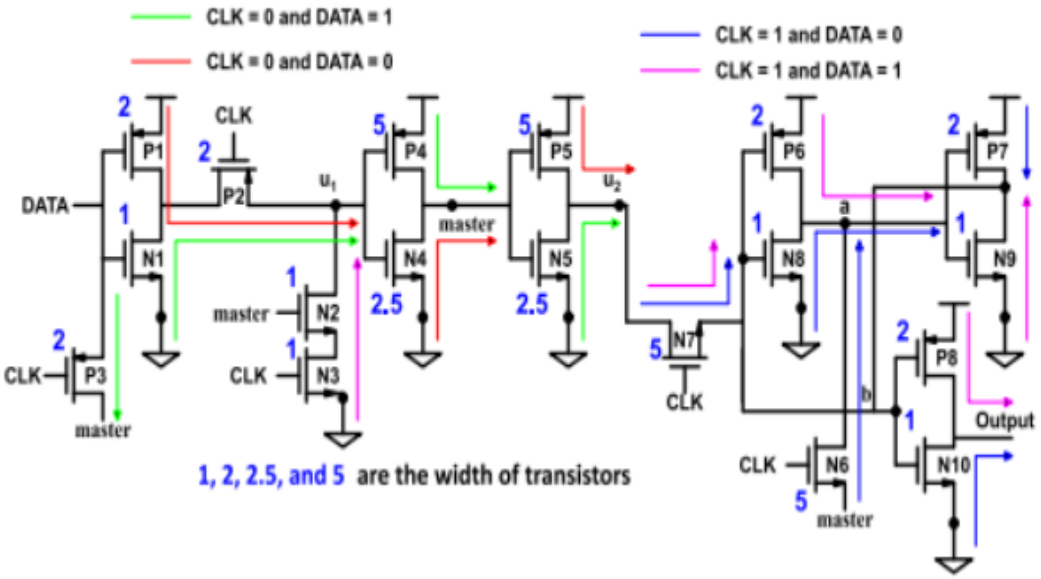
Software Tools Required:

1. Tanner Tools v16.0
2. Schematic-Edit
3. Layout –Edit (L-Edit)
4. Wave- Edit (W-Edit)

Circuit Diagram: 18T



BLOCK DIAGRAM



Procedure Of the Project:

1. Open S-Edit window.
2. Go to File New, New design
3. Go to Cell New View
4. Add libraries file to the New Cell.
5. Instance the devices by using appropriate library files.
6. Save the design and verify the design, check the errors. If errors are there modify the design.
7. Setup the simulation.
8. Run design and observe waveforms.
9. Observe inputs and outputs by giving appropriate inputs.
10. Calculate the power by writing (. power) into T-spice window

Advantages:

- high speed
- low power consumption and low voltage
- reduce circuit area
- reduce long discharging path problem
- low delay
- low complexity
- reduction in transistor count

Application:

- used in low power applications
- used in memories
- used in sequential circuit
- used in chip designs

Conclusion:

A new flip-flop is designed by using 18 transistors. For the proposed work, we have considered following parameters, which are C to Q delay, reduction in PMOS transistor count, no clock overloading, and lowering circuit complexity. The proposed circuit outperformed by 52.52%, 62.89%, and 49.73% in terms of power consumption as compared to ACFF, TCFF and LRFF respectively. In terms of leakage power our circuit excelled by 4.20%, 19.27% and 39.75% when compared with ACFF, TCFF, and LRFF respectively. It also excels in performance at different supply voltages, frequency range and does not have clock overloading. All the parameter taken for this work have been successfully addressed. The proposed design is also compared with the 18T TSPC FF. In which we are getting comparable results and, in some comparison, proposed circuit excels over 18T TSPC and hence proves the efficiency.