CHAPTER-1

INTRODUCTION

1.1 Introduction

The low-power redundant-transition-free TSPC dual-edge-triggering flip-flop using single-transistor-clocked buffer was proposed by Zisong Wang, Peiyi Zhao, and the rest of their research team at the Fowler School of Engineering, Chapman University, Orange, CA 92866, USA.

In coming days, Power consumption is major concern in digital electronics. Based on digital electronics microprocessors and micro-controller chips are major role. If we can reduce power consumption in these chips then overall device power consumption is decreases. In modern high-performance processors, flip-flops are one of the major sources of power consumption. This is because FFs are constantly switching to capture data at the rising and falling edges of the clock signal. To reduce the power consumption of FFs, a number of low-power FF designs have been proposed.

The Low-Power Redundant-Transition-Free TSPC Dual-Edge-Triggering Flip-Flop, employing a Single-Transistor-Clocked Buffer, represents a sophisticated circuit design aimed at minimizing power consumption and enhancing reliability in digital systems. This innovative flip-flop leverages dual-edge triggering for efficient signal processing while strategically integrating a single-transistor clocked buffer to optimize power efficiency. The redundancy elimination ensures a smooth transition between states, contributing to the overall reliability of the flip-flop.

This introduction sets the stage for a comprehensive exploration of the features and advantages inherent in this cutting-edge circuit design, especially when facing the drive from modern graphics processing unit (GPU)/artificial intelligence (AI) neural network processors. The computing power used in AI training has doubled every 3.4 months.

Conventional single-phase-clock FFs only use one clock edge in a time period to process input data, resulting in an unnecessary power overhead as the other clock edge stays

undeveloped for data processing. Dual Edge-Triggering (DET) FFs take advantage of both clock edges to process data, thus can lower clock frequency to half for reducing power consumption while still maintaining the same throughput.

In DET FFs, one of the power consumption issues is that the clocked transistors often cause unnecessary redundant power consumption overhead which occurs when input data remain unchanged but some transistors in the circuit still switch actively due to the circuit topology, to reduce the aforementioned redundant clock transition power in dual-phase-clock DET, a few single-phase-clock DET FFs have been proposed to avoid the cascaded clocked inverters. One of the approaches is the FS TSPC DET.

There is no explicit clocked inverter in FS TSPC, as only one clock phase is used. However, when input does not change, there is an implicit internal RT. If D stays at 1, D P will stay at 0, then the NOR structure in the middle of figure becomes an inverter that has one clocked PMOS and one clocked NMOS. The implicit-redundant transition has thus occurred because of the continual switching of the two clocked transistors. Similarly, if DN stays at 1, the NAND structure will become an inverter which will also have the constant switching problem, causing the implicit-redundant transition. Another static true-single-phase clock DET, TSPC DET, also suffers from the implicit-redundant transition in a similar mechanism.

We use Redundant Transition in Two-Phase-Clock DET, where two cascaded inverters are used to generate the two clock phases. However, when input data do not change, the cascaded inverters remain switching constantly, resulting in clock RT power 13. As an example, this redundant-transition behavior existing in FN_C-DET. Furthermore, there is a contention, which is a type of short circuit, between outer-C-elements (N1, N4, P1, P4) and inner-C-elements (N2, N3, N4, P2, P3, P4) at node B during transition time in FN_C-DET.

1.2 Motivation

With quick improvement of versatile advanced application, the interest for expanding speed, conservative usage and low power scattering triggers various endeavors. The desire to enhance the execution of rationale circuits, once in view of conventional CMOS technology, results in

creating of numerous rationale outline procedures amid most recent two decades. One type of rationale that is prominent in low control circuits is pass transistor rationale.

1.3 Objective

The fundamental target of the project is to decrease the transistors count and check, Area and power utilization.

1.4 Organization Of Project

Section 1: This part manages presentation of flipflops.

Section 2: This part manages writing study and existing strategy

Section 3: This part manages outline of flip flop to lessen zone and power utilization.

Section 4: Software Requirements.

Section 5: This part manages Results, Applications.

Section 6: This part manages conclusions, future degree

CHAPTER 2

LITERATURE SURVEY

Title: An energy-efficient high-performance ×86 core
Author: T. Singh et al.

Abstract: AMD's next-generation, high-performance, energy-efficient ×86 core, Zen, targets server, desktop, and mobile client applications with a 52% instructions per clock cycle (IPC) uplift over the previous generation. The increase in IPC complements a 15% process neutral reduction in CAC (switching capacitance). Performance and energy efficiency are further improved with various circuit techniques including write word line boost, contention-free dynamic logic, supply droop detection with mitigation, a per-core frequency synthesizer, and a per-core integrated linear voltage regulator. Utilizing a 14 nm Fin FET process, the Zen core complex unit consists of a shared 8 MB L3 cache and four cores.

Title: New low glitch and low power DET flip-flops using multiple C-elements," **Author**: S. Lapshev and S. M. R. Hasan

Abstract: The designs of static dual-edge-triggered (DET) flip-flops that exhibit unique circuit behavior owing to the use of C-elements. Five novel DET flip-flops are presented including two high-performance designs and designs that improve upon common Latch-MUX DET flip-flops so that none of their internal circuit nodes follow changes in the input signal. A common characteristic of the presented flip-flops is their low energy dissipation due to glitches at the input. Novel DET flip-flops are compared to existing DET flip-flops using simulation in a high performance 28 nm CMOS technology and are shown to have superior characteristics such as power and power-delay product (PDP) for a range of switching activities. Extensive Monte Carlo and voltage scaling simulations are performed to show that the presented designs are robust under PVT variations.

Title: comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors
Author: J.Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev

Abstract: A low conditional discharge(C-element) Flip-Flops that are basic elements in all digital design. The existing circuits are power hunger due to the dynamic and static power dissipation increases. For reducing power consumption C element technique is used to reduce glitches at the data out. Results obtained through 130nm technology shows reduction in energy dissipation and delay. Average dynamic power dissipation of the proposed flip-flop is compared with two existing techniques. Average power of proposed flip-flop is reduced by 28.41% and 36.18% when compared with Latch-Mux flip-flop and Latch-Mux using C-element.

Title: High-performance and low-power conditional discharge flip-flop
Author: P. Zhao, T. K. Darwish, and M. A. Bayoumi

Abstract: High-performance flip-flops are analyzed and classified into two categories: the conditional precharge and the conditional capture technologies. This classification is based on how to prevent or reduce the redundant internal switching activities. A new flip-flop is introduced: the conditional discharge flip-flop (CDFF). It is based on a new technology, known as the conditional discharge technology. This CDFF not only reduces the internal switching activities, but also generates less glitches at the output, while maintaining the negative setup time and small D-to-Q delay characteristics. With a data-switching activity of 37.5%, the proposed flip-flop can save up to 39% of the energy with the same speed as that for the fastest pulsed flip-flops.

Title: A fully static topologically-compressed 21-transistor flip-flop with 75% power saving
Author: N. Kawai et al.

Abstract: An extremely low-power flip-flop named topologically-compressed flip-flop (TCFF) is proposed. As compared with conventional flip-flops, the novel FF reduces power dissipation by 75% at 0% data activity. This power reduction ratio is the highest among FFs that have been reported so far. The reduction is achieved by applying topological compression method, merger of logically equivalent transistors to an unconventional latch structure. The very small number of transistors, only three, connected to clock signal reduces the power drastically, and the smaller total transistor count assures the same cell size as conventional FFs. In addition, fully static full-swing operation makes the cell tolerant of supply voltage and input slew

variation. An experimental chip design with 40-nm CMOS shows that almost all conventional FFs are replaceable with proposed FF while preserving the same system performance and layout size.

Title: Ultra-low power 18-transistor fully static contention free single-phase clocked flip-flop in 65-nm CMOS

Author: y. Cai, A. Savanth, P. Prabhat, J. Myers, A. S. Weddell, and T. J. Kazmiersk

Abstract: Flip-flops (FFs) are essential building blocks of sequential digital circuits but typically occupy a substantial proportion of chip area and consume significant amounts of power. This paper proposes 18-transistor single-phase clocked (18TSPC), a new topology of fully static contention-free single-phase clocked (SPC) FF with only 18 transistors, the lowest number reported for this type. Implemented in 65-nm CMOS, it achieves 20% cell area reduction compared to the conventional transmission gate FF (TGFF). Simulation results show the proposed 18TSPC is two times more efficient than TGFF in the energy-delay space. To demonstrate EDA compatibility and circuit/system-level benefits, a shift register and an AES-128 encryption engine have been implemented. Chip experimental measurements at 0.6 V, 25 °C show that, compared to TGFF, the proposed 18TSPC achieves reductions of 68% and 73% in overall and clock dynamic power, respectively, and 27% lower leakage.

Title: A novel design for ultra-low power pulse-triggered D-flip-flop with optimized leakage power

Author: A. Karimi, A. Rezai, and M. M. Hajhashemkhani,

Abstract: The power efficiency and reducing the layout area are two main concerns in D-Flip-Flops (D-FF) design. In this paper, a novel architecture is presented for the pulse-triggered D-FF in the CMOS 90-nm technology. This novel architecture utilizes a transmission gate to control the input data and the leakage power. The Pulse Generator (PG) is also modified to reduce the number of required transistors and the clock pulse delay. In addition, the pull-up P-MOS transistor is controlled by input data to reduce the power dissipation. The proposed D-FF is simulated using Hspice. The simulation results show that the proposed architecture has improvement in terms of power consumption, D-to-Q delay, and Power Delay Performance (PDP) in comparison with other D-Flip-Flop architectures.

Title: Ultra-low power pulse-triggered CNTFET-based flip-flop

Author: A. Karimi, A. Rezai, and M. M.Hajhashemkhani

Abstract: Reducing the power consumption and scaling the devices are the important concerns of today's electronics. Flip-Flop (FF) is one of the basic elements in electronic devices. Thus, the performance of the electronic devices is improved by improving these qualities in the FFs. In this paper, a novel pulse-triggered CNTFET-based D-Flip-Flop structure is proposed. This structure utilizes signal feed through technique to reduce the “0” to “1” transition, which requires only one CNTFET. Moreover, the discharging path is optimized to reduce the delay time for “1” to “0” transition by using only two CNTFETs. The novel structure is simulated in Hspice using Stanford model. The output results prove that the performance of the proposed structure is improved greatly in terms of power consumption, D-to-Q delay, the power-delay product, and the number of required transistors in comparison with other pulse-triggered Flip-Flop structures.

CHAPTER-3

EXISTING METHOD

3.1 Introduction

The conventional design of an edge triggered flip-flop contains a redundant which can be eliminated by replacing the three-input NAND gate with a two-input NAND gate. The design then consists of 6 two input NAND gates, arranged in a similar way to the conventional design as shown in Fig.3.1 N1 and N2 forms the R latch, N3 and N4 forms the S latch and N5 and N6 forms the main latch. The operation of the proposed flip-flop design is similar in to the conventional flip-flop but with the direct input 'D' to N2 removed. It now has to wait for the 'D' input from x3, which leads to glitches at the node x2. These glitches will increase the power consumption. This problem can be removed by using a method known as Pass Transistor Logic, which is implemented at the transistor level of the design. This design also uses a method known as transistor sharing, which decreases the number of transistors required by sharing a NMOS transistor requiring the same input.

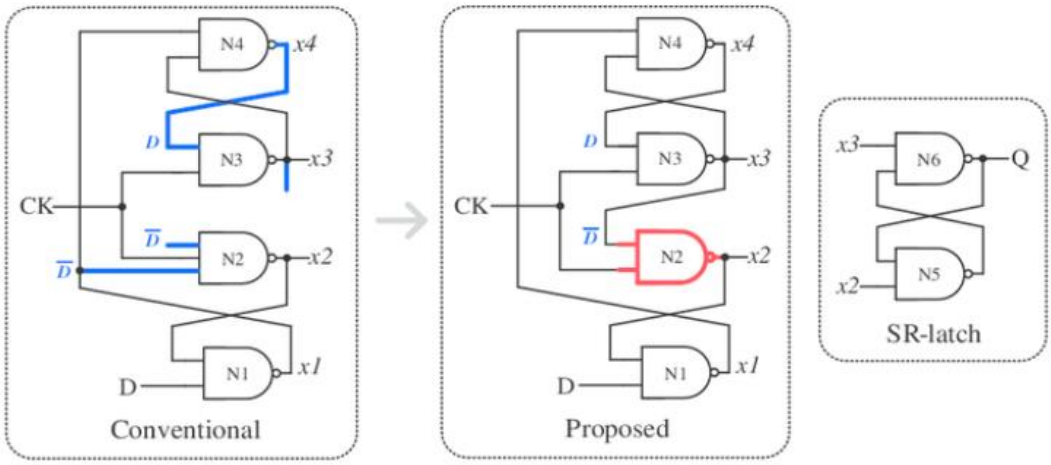

Fig 3.1: SR-latch

Initially the flip-flop is made of 21 transistors using the conventional design. The figures represent the conventional design, proposed design and SR-latch. Later it was reduced to 18 using transmission gate and clock gating network.

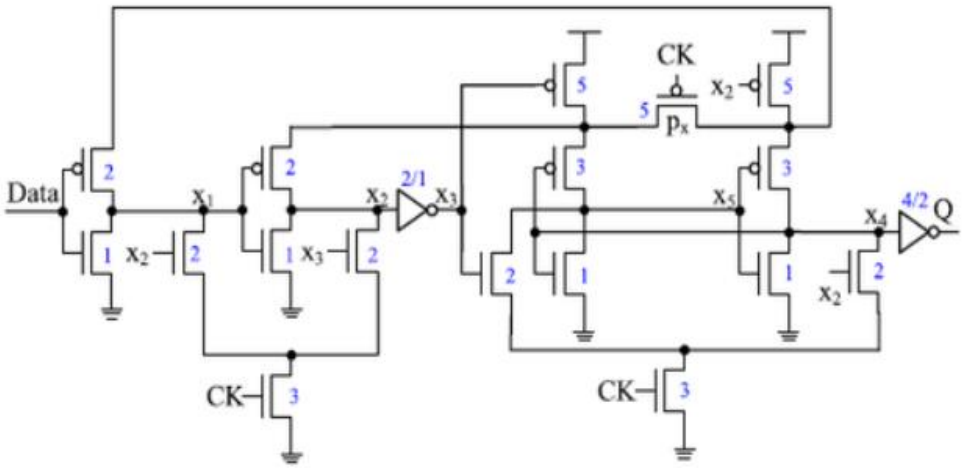

Fig 3.2: Flip-Flop using 21 transistors.

3.2 Transmission Gate Logic

As transmission doors, is like a transfer that can direct in the two headings or square by a control motion with any voltage potential. n guideline, a transmission entryway made up of two field impact transistors, in which rather than customary discrete field impact transistors - the substrate terminal (Bulk) is associated inside to the source terminal. The two transistors, a n-channel MOSFET and a p-direct MOSFET are associated in parallel with this, be that as it may, just the deplete and source terminals of the two transistors are associated together. Their door terminals are associated with each other by means of a NOT entryway (inverter), to frame the control terminal.

Similarly, as with discrete transistors, the substrate terminal is associated with the source association, so there is a transistor to the parallel diode (body diode), whereby the transistor passes in reverse. In any case, since a transmission door must square stream in either bearing, the substrate terminals are associated with the separate supply voltage potential so as to guarantee that the substrate diode is constantly worked in the switch heading. The substrate terminal of the n-channel MOSFET is in this way associated with the positive supply voltage potential and the substrate terminal of the p-channel MOSFET associated with the negative supply voltage potential.

At the point when the control input is a rationale zero (negative power supply potential), the door of the n-channel MOSFET is additionally at a negative supply voltage potential. The door terminal of the p-channel MOSFET is caused by the inverter, to the positive supply voltage potential. Despite on which exchanging terminal of the transmission entryway (An or B) a voltage is connected (inside the allowable range), the door source voltage of the n-channel MOSFETs is constantly negative, and the p-channel MOSFETs is constantly positive. In like manner, neither of the two transistors will lead and the transmission entryway turns off.

When the control input is a rationale one, so the door terminal of the n-channel MOSFETs is situated at a positive supply voltage potential. By the inverter, the door terminal of the p-channel MOSFETs is presently at a negative supply voltage potential. As the substrate terminal of the transistors isn't associated with the source terminal, the deplete and source terminals are relatively equivalent and the transistors begin at a voltage distinction between the door terminal and one of these behaviors.

One of the exchanging terminals of the transmission door is raised to a voltage close to the negative supply voltage, a positive entryway source voltage (door to-deplete voltage) will happen at the N-channel MOSFET, and the transistor starts to direct, and the transmission entryway conducts. The voltage at one of the exchanging terminals of the transmission door is currently raised persistently up to the positive supply voltage potential, so the entryway source voltage is lessened (entryway deplete voltage) on the n-channel MOSFET, and this starts to kill. In the meantime, the p-channel MOSFET has a negative door source voltage (entryway to-deplete voltage) develops, whereby this transistor begins to lead and the transmission door switches.

Subsequently it is accomplished that the transmission entryway disregards the whole voltage go. The change protection of the transmission door fluctuates relying on the voltage to be switched, and relates to a superposition of the protection bends of the two transistors.

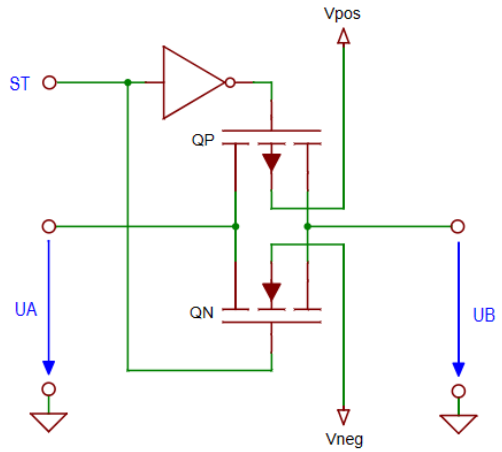

Fig 3.3: Principal diagram of a transmission gate

The control input ST must be able to take to control depending on the supply voltage and switching voltage different logic levels. To provide a basis for comparison, some existing FF designs are reviewed first. A classic master–slave-type TGFF design.

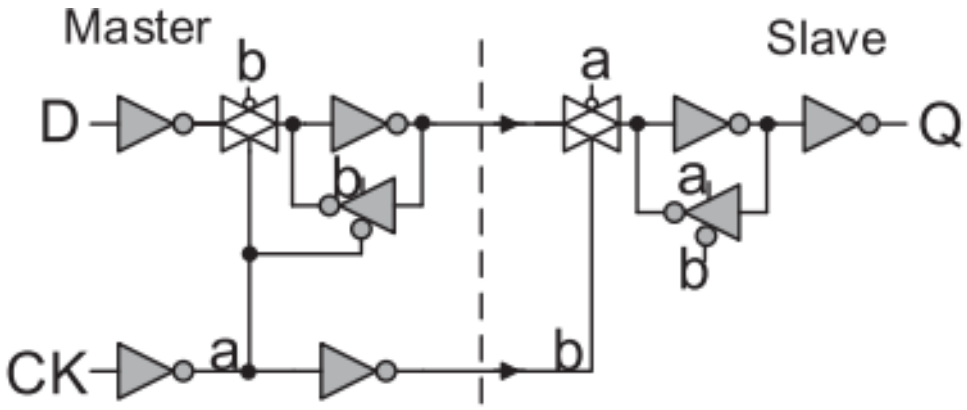

Fig 3.4: Master Slave type TGFF

Indicating that it comprises two TG-based latch designs. Inverters I1 and I2 are used to generate complementary clock signals. This design suffers from a high capacitive clock loading problem (a total of 12 transistors driven by the clock), which indicates a sustained power consumption even when the input remains static. This problem also occurs in conventional SRFF designs, as shown in Fig.3.5

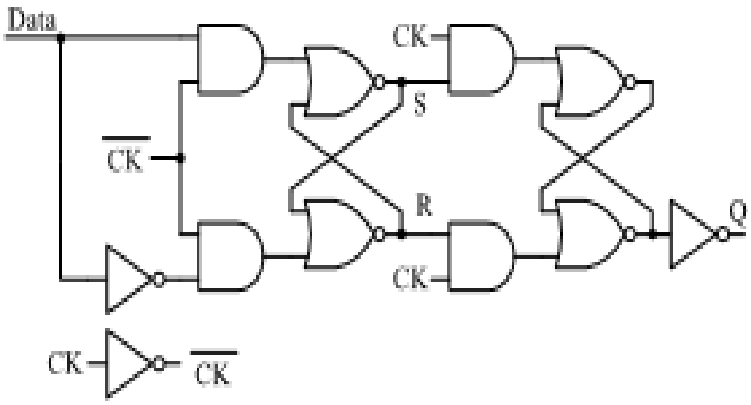

Fig 3.5: Conventional SRFF designs

To overcome the power consumption problem, two FF designs employing an adaptive coupling (ac) technique and a topologically compressed scheme have been proposed. Fig. 3.4 shows the AC FF design.

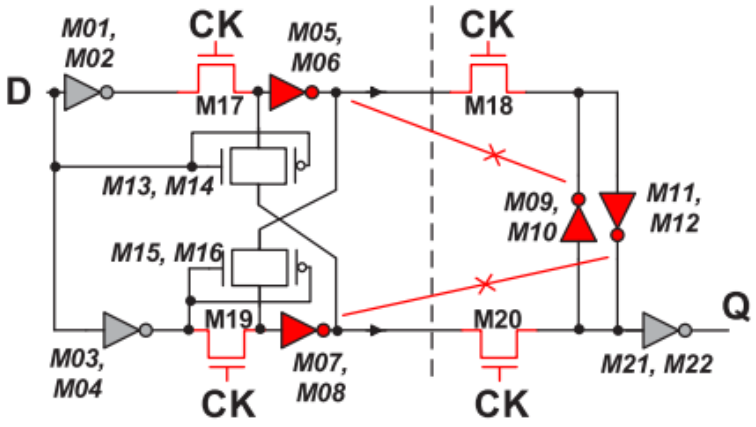

Fig 3.6: AC Flipflop design

Unlike conventional TGFF designs, this design uses a differential latch structure with pass-transistor logic to achieve TSPC operation. The TGs are replaced with either n- or p-type pass transistors. To overcome the impact of process variations on the master latch, a pair of level restoring circuits is inserted into the cross coupled paths of the master latch. In this design, only four MOS transistors (two pMOS and two nMOS) are driven by the clock signal, and the transistor count is lowered to 22.A lighter clock loading in addition to the circuit simplification

of the FF design can lower the power consumption significantly. In this design, the data contention problem in the slave latch deteriorates as the data switching activity increases, and the advantages of power saving are thus diminished. The level restoring circuit pair of the master latch results in a longer setup time. Moreover, this design suffers from a power leaking problem when certain input and internal node combinations occur.

3.3 Procedure

Fig.3.3 shows another SR-latch-based TSPC FF design named topologically compressed FF (TCFF), obtained through a topologically compressed scheme. The logic schematic of this design and the original MOS circuit. The master latch adopts the configuration of a MUX with feedback and can be implemented with two AND-OR-Invert (AOI) gates and an inverter. The latch is transparent when the clock signal CK is 0. The inputs pass through the AOI gates and the output of the inverter; that is, node x3 is always complementary to the input data. When CK turns 1, the contribution from the input data is blocked and x3 remains unchanged because of a closed path formed by the upper AOI and the inverter.

The slave latch also comprises two AOI gates and an inverter. the complementary inputs from the master latch are fed to AND terms, which are also controlled by the clock signal, of the two AOI gates. Only one phase of the clock signal is used in this design.

The MOS circuit can be further optimized by factoring out the shared terms. For N (pull-down) logic, one CK-controlled nMOS transistor can be shared by the two discharging paths. For P (pull-up) logic, four pairs of pMOS transistors are connected to *V*DD, and two of these pairs share identical inputs. Therefore, two pMOS pairs of the master latch can be eliminated.

Notably, nodes *x*2 and *x*3 are always complementary to each other, implying that either the *x*2- or *x*3-controlled pMOS transistors will turn ON. The drain node of the turned ON pMOS transistor corresponds to a virtual *V*DD. Through the addition of an extra clock controlled pMOS transistor across the two AOI gates, the two clock-driven pMOS transistors can be removed without affecting the function. The resultant circuit design is shown in Fig. 3.5. The transistor count is reduced from 28 to 21 and

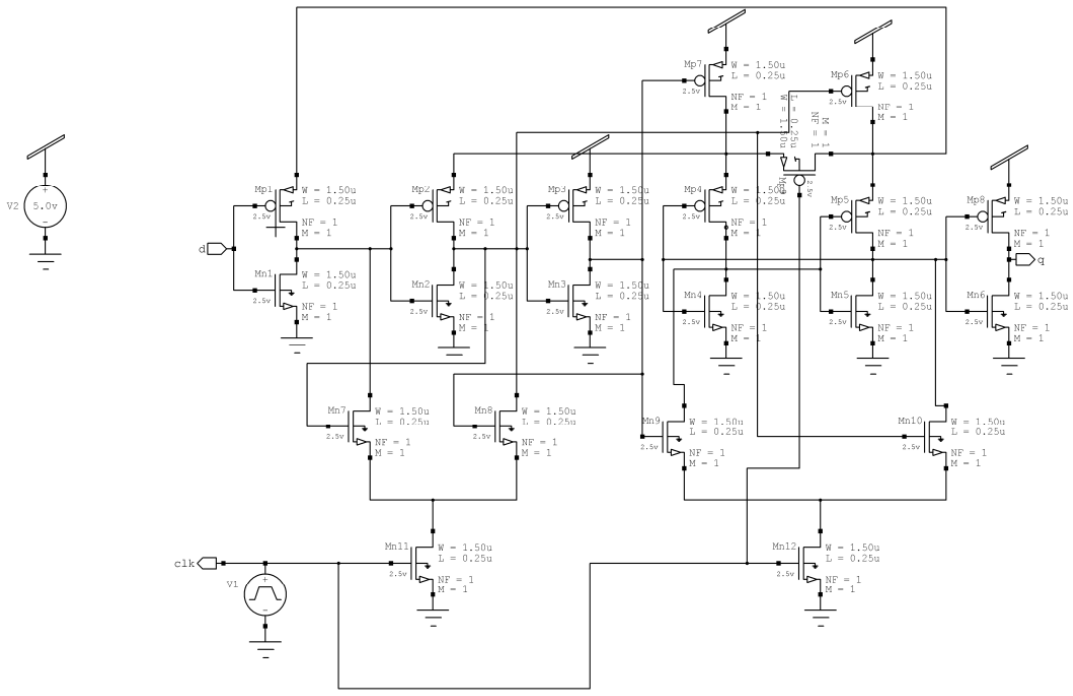

Fig 3.7: Circuit diagram of 21- transistor using reduction schemes

only three transistors are driven directly by the clock signal. All these factors contribute to a significant power saving of the design. This design is fully static, even though both pull-up and pull-down logic networks are largely simplified. In conclusion, the TCFF design is based on three optimization principles:

1) use only a single phased clock;
2) reduce the number of transistors driven by the clock; and
3) reduce the total transistor count.

Despite the significant improvement in the power consumption, the timing performance of the TCFF design is compromised. In particular, the design suffers from a longer setup time because of a weakened pull-up network in which only two pMOS transistors are connected to VDD directly.

The critical path consists of three pMOS transistors connected in series. Although this problem can be alleviated by enlarging the pMOS transistors, the power consumption is negatively impacted.

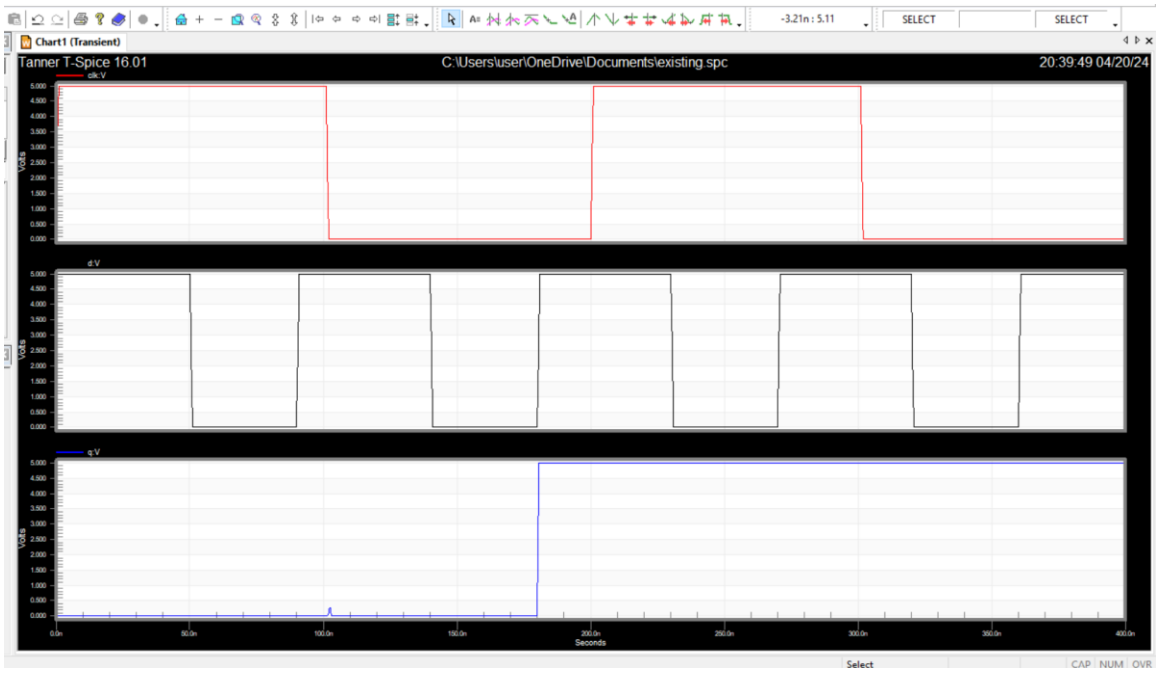

Fig 3.8: Simulation Wave forms for 21-Transistors

```
Input file:   existing.spc
Progress:     Simulation completed

Total nodes:    14    Active devices:    21    Independent sources:   0
Total devices:  24    Passive devices:   0     Controlled sources:    0

T-Spice - Tanner SPICE
Version 16.01
Network license
Product Release ID: T-Spice Win64 16.01.20130407.21:15:40
Copyright © 1988-2013 Tanner EDA

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Start of existing.spc
Loaded BSIM3v33 model library, Berkeley BSIM3 v3.3.0
Loaded BSIM3v31 model library, Berkeley BSIM3 VERSION 3.1 with extensions
Loaded BJT model library, Gummel-Poon Bipolar with extensions

   Opening simulation database "C:\Users\user\OneDrive\Documents\existing.tsim"

General options:
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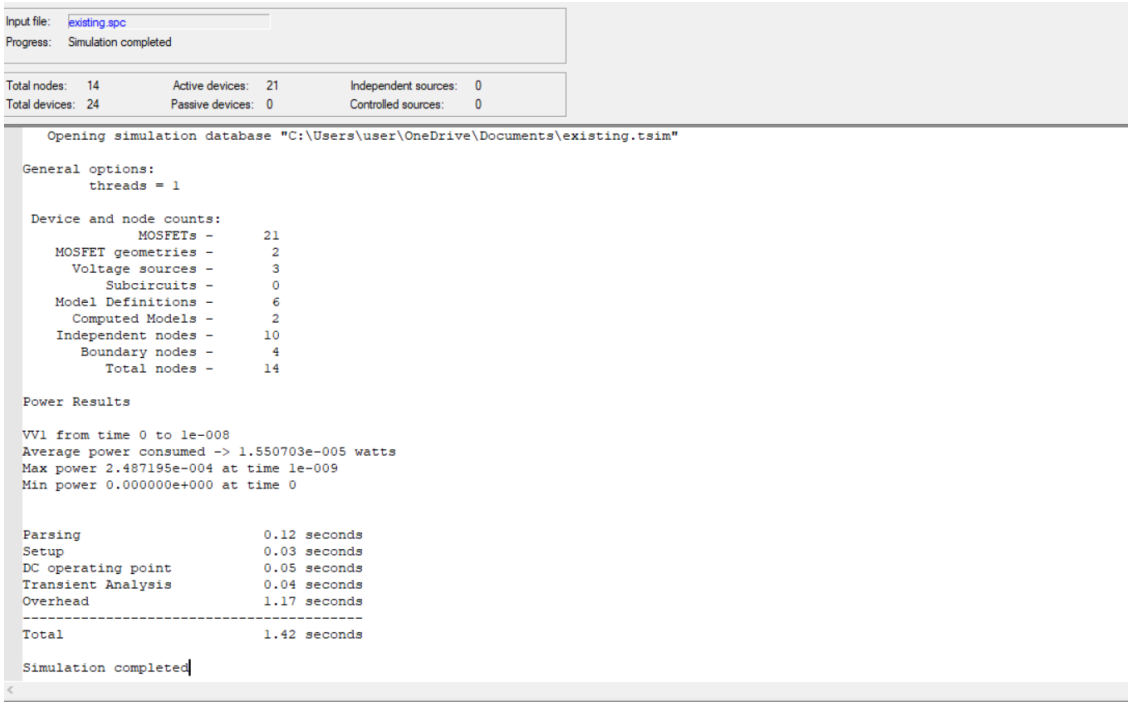


Fig.3.9: Power Consumption for 21 transistors

3.4 Advantages

- Less Delay
- Less Time for Execution
- Low Power Consumption
- Short Setup Time
- Less Power Leakage in The Node
- It Does Not Occurs the Node Floating
- Less Number of Transistors Required

CHAPTER-4

PROPOSED METHOD

4.1 Introduction

In the proposed system design the transistor count is further reduced from 19 to 18. This reduction simplifies the circuit and the power consumption also reduced. Figure 4.1 shows the structure of 18 transistor FF design. In this design the transistor in the master latch is combined with the clock signal and thus the transistor count is reduced by one.

The operation involves that when data=0 and clock is low the master latch becomes transparent and stores the data input. When data=1 and clock is high the master is in hold state and the slave latch changes its value that is the data stored in the master is transferred to slave and it is outputted to Q.

The clock controlled NMOS transistor is also connected with the x2 discharging node. Hence, the power gets reduced and the delay also compromised. The set-up time, hold time are in seconds.

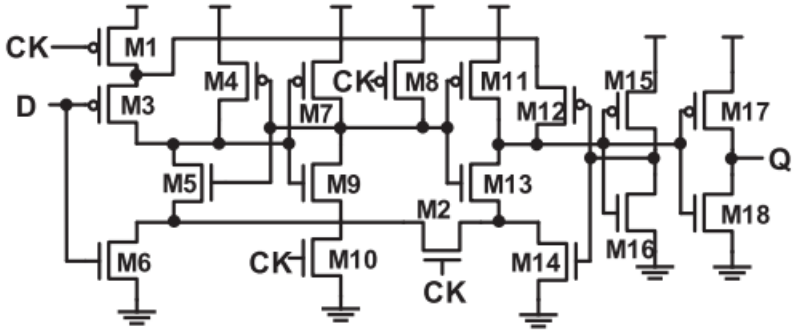


Fig 4.1: Proposed Flip-Flop design

- **Power-Delay-Product Evaluation**

Both PDPCQ and PDPDQ were employed as a composite performance index in our evaluation. When the switching activity was 12.5%, both PDP indices of the proposed design were the lowest, followed by those of the TCFF and ACFF. However, the indices of the remaining four non-TSPC designs trailed by a large margin.

The proposed LRFF design, in particular, can simultaneously balance the power and speed performance for the best results. Illustrates a bar chart summarizing the PDP comparison results under different switching activities. shows the PDP performance under process variations with a 25% data switching probability. For each process corner (SS 0.8 V/ 125 °C, TT 1 V/25 °C, FF 1.2 V/−40 °C, SF 1 V/25 °C, and FS 1 V/25 °C), the setup time and hold time were scanned to obtain the best PDP number. All FF designs were determined to function properly under process variations.

4.1.1 Flip Flop

The flip-flops are become the power consuming block in the Graphical Processer, Artificial intelligence (AI) era and other Electronic Devices. In this project we are going to reduce the power consumption of flip-flop. In this process we reduce the number of transistors used in flip-flops. By reducing the number of flip-flops, the switching activity will decrease, then the power consumption will also decrease to eliminate the aforementioned redundant transitions between two clocked transistors (one PMOS, one NMOS) in dual-edge FFs, a low power TSPC DET FF is proposed with innovative redundant-free STCB topology.

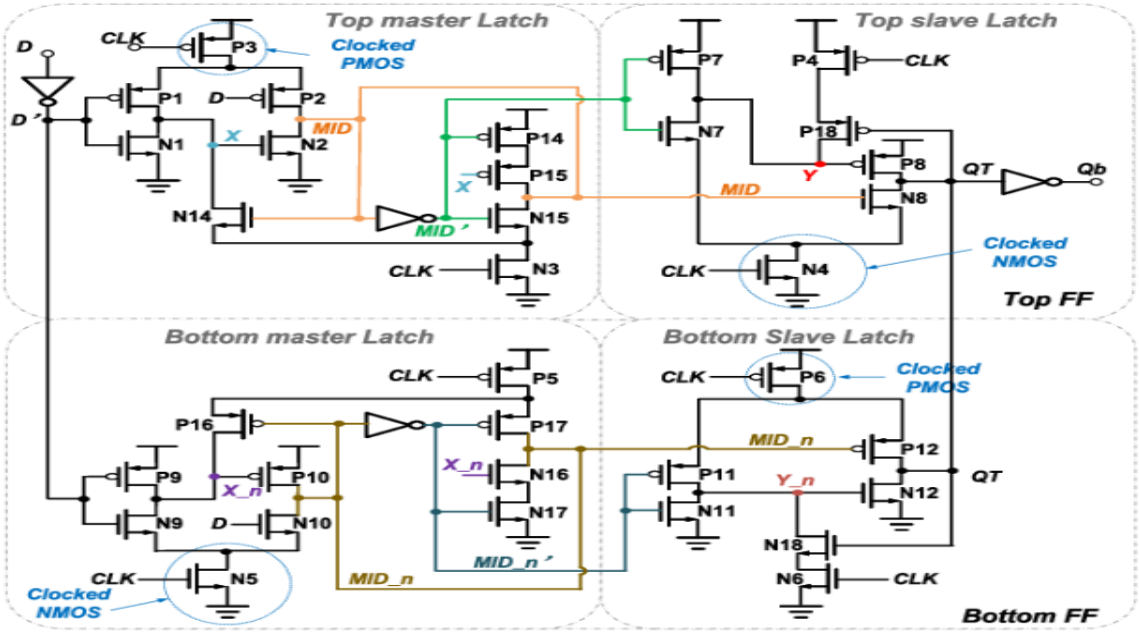


Fig 4.2: proposed TSPC single transistor clocked DET,STC-DET

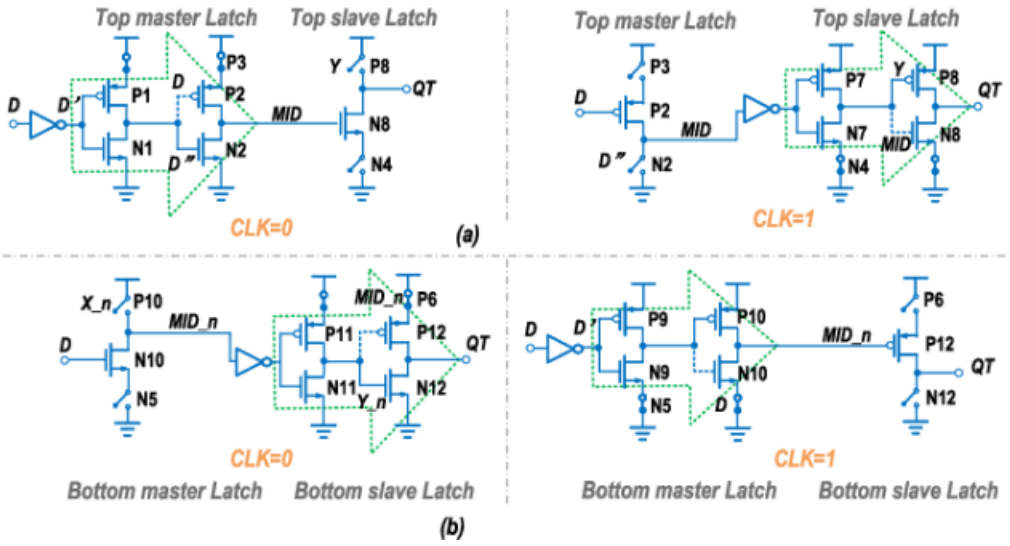


Fig 4.2(a): Top FF

Fig 4.2(b): bottom FF using equivalent simplified logic circuit diagram.

A. Operation of the Top FF in STC-DET

When *CLK* = 0, in the data sampling path of the top FF, the clocked PMOS P3 in the top master latch turns on, node *X* becomes *D*″ (see the top left of Fig. 4.2); since *D*″ is essentially *D*, then transistors (P2, N2) will become equivalent to a virtual inverter [A simplified logic diagram is illustrated in Fig. 4.2 (a)]. Then the input passes to *MI D* in the top master latch (see arrow in the top left of the above figure); On the other hand, in the top slave latch in Fig. 4.2, clocked NMOS N4 is off since *CLK* = 0, so node *Y* will not be 0, hence PMOS P8 is off. *QT* is not connecting with VDD or GND, meaning that *QT* in the top FF is floating (see the top left of Fig. 4.2 (a)).

In Fig. 4.2, transistors (N1, N2, P1, P2, P3) build *a negative triggered STCB*, where only one clocked transistor P3 is used in signal sampling path. The RT which occurs between one clocked PMOS and one NMOS in FN_C DET and FS-TSPC, Fig. 4.1, does not exist in STCDET. Neither is there any contention. Besides the clocked transistor P3, there is one more clocked NMOS transistor N3, in the top master latch (see the top left of Fig. 4.2), but it is used in keeper, rather than the data sampling path. All the four clocked transistors that are on the data sampling path have been marked out with an arrow in Fig. 4.2 (P3, N4, N5, and P6).

Transistors (N4, N7, N8, P7, P8) build another positive triggered STCB in the top FF.

When *CLK* = 1, in the top master latch in Fig. 4.2, clocked PMOS P3 is off since *CLK* = 1, so the paths associated with P1 and subsequently N2, are off. As a result, the logic state of *MI D* is kept by keeper (N3, N15, P14, P15). When *X*'s logic state is 0, it will be kept by pull down keeper (N14, N3). On the other hand, in the top slave latch, the clocked NMOS, N4, turns on, so *Y* is *MI D*″ which is essentially *MI D*. Therefore, transistors (N8, P8) act as a virtual inverter, the signal of *MI D* which is right before clock rising edge passes to *QT* (see the arrow in the top right of the Fig. 4.2(a)[1]). Hence, the top FF is activated at the clock positive edge.

B. Operation of the Bottom FF in STC-DET

When CLK = 0, in the bottom FF (see bottom left of Fig. 4.2), the clocked NMOS, N5, in the bottom master latch turns off. Consequently, the paths associated with N9 and P10 are off, and the logic state of MI D_n is kept by keeper (N16, N17, P5, P17); if logic state of X_n is 1, that state will be kept by pull up keeper (P16, P5). On the other hand, in the bottom slave latch (bottom right of Fig. 4.2), clocked PMOS P6 in top of the figure turns on when CLK = 0, Y_n becomes MI D_n″ which is essentially MI D_n, thus P12 and N12 act as a virtual inverter, and the signal of MI D_n which is right before clock falling edge passes to QT (see arrow in the left half of Fig. 4.2 (b)[1]). As a result, the bottom FF is activated on clock negative edge. There would be no redundant transition if *D* keeps the same value since it causes no switching. Transistors (N5, N9, N10, P9, P10) and (P6, N11, N12, P11, P12) build other two STCBs in the bottom FF.

When CLK = 1, the clocked NMOS N5 in the bottom master latch turns on (see the bottom left of Fig. 4.2), X_n will be *D*″ which is essentially *D*, thus P10 and N10 act as a virtual inverter, and input *D* passes to MI D_n in the bottom master latch [see arrow in right half of Fig. 4.2(b)]; On the other hand, the clocked PMOS P6 in the bottom slave latch turns off, so the paths associated with P11 and subsequently N12 will also be off. And it is worth mentioning that as QT node has another connection in the top FF which is active when CLK = 1 as discussed before, QT is a no floating node. There is still no redundant transition if D keeps the same value since it does not affect QT.

Since the top and bottom slave latches are activated by positive clock edge and negative clock edge, respectively, STC-DET can sample input at both edges of clock. Moreover, because the two slave latches are activated by different clock edges, so there is always one latch that is transparent and the other one is opaque for all periods, thus the slave latches' outputs can be connected together at QT without contention. Furthermore, this transparent connection to supply or ground for QT makes it an all-time non floating node. And if necessary, by adding an enable signal and scan input to the master latches on the left side, one can easily modify STC-DET to be scannable for supporting the design for test (DFT).

4.1.2 Advantages

- Reduced power consumption: The STC-DET FF uses a single clocked transistor in the data sampling path, which eliminates redundant transitions and reduces power consumption.
- Reduced redundant transitions: The STC-DET FF eliminates redundant transitions, which further reduces power consumption.
- Lowest power-delay-product (PDP): The STC-DET FF achieves the lowest PDP among DET FFs. PDP is a measure of the power and performance of a circuit, and a lower PDP indicates better performance and power efficiency.
- High performance: The STC-DET FF has high performance, similar to other DET FF designs.

4.2 CMOS LOGIC

4.2.1 Introduction

Complementary metal–oxide–semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. Frank Wanlass patented CMOS in 1963 (US patent 3,356,858). CMOS is also sometimes referred to as complementary-symmetry metal–oxide–semiconductor (or COS-MOS).[1] The words "complementary-symmetry" refer to the fact that the typical design

style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.[2]

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. Aluminum was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-k dielectric materials in the CMOS process.

CMOS" refers to both a particular style of digital circuitry design and the family of processes used to implement that circuitry on integrated circuits (chips). CMOS circuitry dissipates less power than logic families with resistive loads. Since this advantage has increased and grown more important, CMOS processes and variants have come to dominate, thus the vast majority of modern integrated circuit manufacturing is on CMOS processes.[4] As of 2010, CPUs with the best performance per watt each year have been CMOS static logic since 1976.

CMOS circuits use a combination of p-type and n-type metal–oxide–semiconductor field-effect transistors (MOSFETs) to implement logic gates and other digital circuits. Although CMOS logic can be implemented with discrete devices for demonstrations, commercial CMOS products are integrated circuits composed of up to billions of transistors of both types, on a rectangular piece of silicon of between 10 and 400 mm^2.

CMOS accomplishes current reduction by complementing every nMOSFET with a pMOSFET and connecting both gates and both drains together. A high voltage on the gates will

cause the nMOSFET to conduct and the pMOSFET to not conduct while a low voltage on the gates causes the reverse. This arrangement greatly reduces power consumption and heat generation. However, during the switching time both MOSFETs conduct briefly as the gate voltage goes from one state to another. This induces a brief spike in power consumption and becomes a serious issue at high frequencies.

The image on the right shows what happens when an input is connected to both a PMOS transistor (top of diagram) and an NMOS transistor (bottom of diagram). When the voltage of input A is low, the NMOS transistor's channel is in a high resistance state. This limits the current that can flow from Q to ground. The PMOS transistor's channel is in a low resistance state and much more current can flow from the supply to the output. Because the resistance between the supply voltage and Q is low, the voltage drops between the supply voltage and Q due to a current drawn from Q is small. The output therefore registers a high voltage.

The power supplies for CMOS are called V_{DD} and V_{SS}, or V_{CC} and Ground (GND) depending on the manufacturer. V_{DD} and V_{SS} are carryovers from conventional MOS circuits and stand for the drain and source supplies.[5] These do not apply directly to CMOS since both supplies are really source supplies. V_{CC} and Ground are carryovers from TTL logic and that nomenclature has been retained with the introduction of the 54C/74C line of CMOS.

Shown on the right is a circuit diagram of a NAND gate in CMOS logic. If both of the A and B inputs are high, then both the NMOS transistors (bottom half of the diagram) will conduct, neither of the PMOS transistors (top half) will conduct, and a conductive path will be established between the output and V_{ss} (ground), bringing the output low. If both of the A and B inputs are low, then neither of the NMOS transistors will conduct, while both of the PMOS transistors will conduct, establishing a conductive path between the output and V_{dd} (voltage source), bringing the output high. If either of the A or B inputs is low, one of the NMOS transistors will not conduct, one of the PMOS transistors will, and a conductive path will be established between the output and V_{dd} (voltage source), bringing the output high. As the only configuration of the two inputs that results in a low output is when both are high, this circuit implements a NAND (NOT AND) logic gate.

4.2.2 Pass Transistor Logic

Pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input If several devices are chained in series in a logic path, a conventionally constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Since there is less isolation between input signals and outputs, designers must take care to assess the effects of unintentional paths within the circuit. For proper operation, design rules restrict the arrangement of circuits, so that sneak paths, charge sharing, and slow switching can be avoided.[3] Simulation of circuits may be required to ensure adequate performance.

The pass transistor is driven by a periodic clock signal and acts as an access switch to either charge up or charge down the parasitic capacitance C_x, depending on the input signal V_{in}. Thus, the two possible operations when the clock signal is active (CK = 1) are the logic "1" transfer (charging up the capacitance C_x to a logic-high level) and the logic "0" transfer (charging down the capacitance C_x to a logic-low level). In either case, the output of the depletion load nMOS inverter obviously assumes a logic-low or a logic-high level, depending upon the voltage V_x. Complementary pass-transistor logic or "Differential pass transistor logic" refers to a logic family which is designed for certain advantages. It is common to use this logic family for multiplexers and latches.

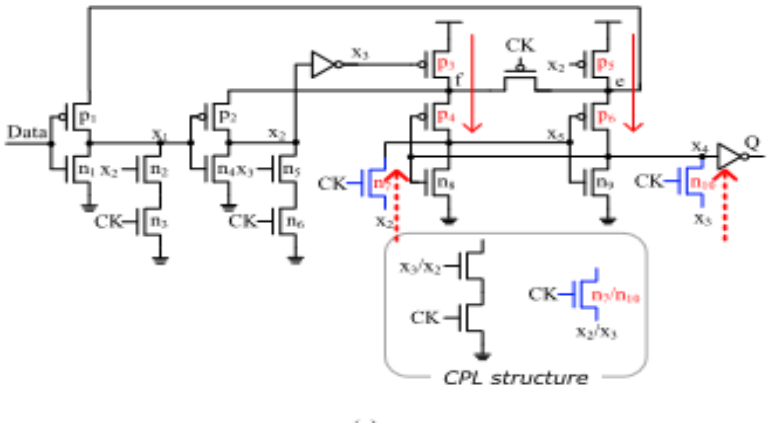


Fig 4.3: CPL Structure

CPL uses series transistors to select between possible inverted output values of the logic, the output of which drives an inverter The CMOS transmission gates consist of nMOS and pMOS transistor connected in parallel.

Double-pass transistor logic eliminates some of the inverter stages required for complementary pass transistor logic by using both N and P channel transistors, with dual logic paths for every function. While it has high speed due to low input capacitance, it has only limited capacity to drive a load. Static and dynamic types of pass transistor logic exist, with differing properties with respect to speed, power and low-voltage operation.[6] As integrated circuit supply voltages decrease, the disadvantages of pass transistor logic become more significant; the threshold voltage of transistors becomes large compared to the supply voltage, severely limiting the number of sequential stages

Interconnecting any two logic families often required special techniques such as additional pull-up resistors or purpose-built interface circuits, since the logic families may use different voltage levels to represent 1 and 0 states, and may have other interface requirements only met within the logic family. For example, TTL levels are different from those of CMOS. Generally, a TTL output does not rise high enough to be reliably recognized as a logic 1 by a CMOS input, especially if it is only connected to a high-input-impedance CMOS input that does not source significant current. This problem was solved by the invention of the 74HCT family of

devices that uses CMOS technology but TTL input logic levels. These devices only work with a 5V power supply.

The use of either the higher or the lower voltage level to represent either logic state is arbitrary and may even be changed at different levels within a system. Active-high and active-low states can be mixed at will: for example, a read only memory integrated circuit may have a chip-select signal that is active-low, but the data and address bits are conventionally active-high. Occasionally a logic design is simplified by inverting the choice of active level (see De Morgan's theorem). An active-high signal represents a binary digit of 1, or asserted state of a logical condition, by the *higher* of two voltages: The higher voltage represents a binary 1 or "mark", and the lower voltage represents a binary 0 or "space". An active-low signal represents a binary digit of 1, or asserted state of a logical condition, by the *lower* of two voltages: The higher voltage represents a binary 0 or "space", and the lower voltage represents a binary 1 or "mark".

Nearly all digital circuits use a consistent logic level for all internal signals — however, that level varies widely from one system to another. A level shifter connects one digital circuit that uses one logic level to another digital circuit that uses another logic level. Often two-level shifters are used, one at each system: A "line driver" converts from internal logic levels to standard interface line levels; a "line receiver" converts from interface levels to internal voltage levels. The most common agreed-upon voltage levels are the TTL logic levels; almost as common is the RS-232 voltage levels.

4.2.3 Power Consumption

An advantage of CMOS over NMOS is that both low-to-high and high-to-low output transitions are fast since the pull-up transistors have low resistance when switched on, unlike the load resistors in NMOS logic. In addition, the output signal swings the full voltage between the low and high rails. This strong, more nearly symmetric response also makes CMOS more resistant to noise.

MOS logic dissipates less power than NMOS logic circuits because CMOS dissipates power only when switching ("dynamic power"). On a typical ASIC in a modern 90 nanometer

process, switching the output might take 120 picoseconds, and happens once every ten nanoseconds. NMOS logic dissipates power whenever the transistor is on, because there is a current path from V_{dd} to V_{ss} through the load resistor and the n-type network. Static CMOS gates are very power efficient because they dissipate nearly zero power when idle. Earlier, the power consumption of CMOS devices was not the major concern while designing chips. Factors like speed and area dominated the design parameters. As the CMOS technology moved below sub-micron levels the power consumption per unit area of the chip has risen tremendously.

4.2.4 Broadly classifying, power dissipation in CMOS circuits occurs because of two components:

1. Static dissipation

- Sub threshold conduction when the transistors are off

  Both NMOS and PMOS transistors have a gate–source threshold voltage, below which the current (called sub threshold current) through the device drops exponentially. Historically, CMOS designs operated at supply voltages much larger than their threshold voltages (V_{dd} might have been 5 V, and V_{th} for both NMOS and PMOS might have been 700 mV). A special type of the CMOS transistor with near zero threshold voltage is the native transistor.

- Tunneling current through gate oxide

  SiO_2 is a very good insulator, but at very small thickness levels electrons can tunnel across the very thin insulation; the probability drops off exponentially with oxide thickness. Tunnelling current becomes very important for transistors below 130 nm technology with gate oxides of 20 Å or thinner.

- Leakage current through reverse-biased diodes

  Small reverse leakage currents are formed due to formation of reverse bias between diffusion regions and wells (for e.g., p-type diffusion vs. n-well), wells and substrate (for e.g., n-well vs. p-substrate). In modern process diode leakage is very small compared to sub threshold and tunneling currents, so these may be neglected during power calculations.

2. Dynamic dissipation

- Charging and discharging of load capacitances

CMOS circuits dissipate power by charging the various load capacitances (mostly gate and wire capacitance, but also drain and some source capacitances) whenever they are switched. In one complete cycle of CMOS logic, current flows from V_{DD} to the load capacitance to charge it and then flows from the charged load capacitance (C_L) to ground during discharge. Therefore, in one complete charge/discharge cycle, a total of $Q=C_LV_{DD}$ is thus transferred from V_{DD} to ground. Multiply by the switching frequency on the load capacitances to get the current used, and multiply by the average voltage again to get the characteristic switching power dissipated by a CMOS device: $P=0.5CV^2f$.

Since most gates do not operate/switch at every clock cycle, they are often accompanied by a factorα, called the activity factor. Now, the dynamic power dissipation may be re-written as: $P=\alpha CV^2f$.

A clock in a system has an activity factor $\alpha=1$, since it rises and falls every cycle. Most data have an activity factor of 0.1.[6] If correct load capacitance is estimated on a node together with its activity factor, the dynamic power dissipation at that node can be calculated effectively.

The focus of most contemporary clock distribution network designs is the power dissipation associated with the clock signal. Increasing die sizes and operating frequencies have resulted in a significant, and sometimes inordinate, percentage of a chip power dedicated to the clock distribution. This cause and effect can be simply represented by the dynamic power equation:

$$P = CV^2f \tag{2.1}$$

Where C is the capacitive load, f is the switching frequency and V is the voltage swing of the signal.

A third method of reducing the power dissipation in the clock network is to shut on the clock signal to unused portions of the chip. This method is used to significant gain on the DEC Strong ARM microprocessor. It is estimated that conditional clocking reduced the power dissipation of the Strong ARM's clock network almost four-fold.

In logic design, dynamic power increases whenever logic toggles from 1 to 0 or 0 to 1. To avoid this, large clusters of logic are often gated if the particular function isn't used. An example of this is in the case of a microprocessor ALU with many sub pipes of dedicated functions. If an ADD operation is being performed, the logic paths for logical (AND, OR, etc.), multiplies, shifting, etc. are not being used. If the ADD sub pipe shares its inputs with the others, it may reduce dynamic power consumption to gate off the inputs to those sub pipes if an ADD is occurring. Static power is mostly a function of both area as well as circuit design. This parallel setup increases the static power of the circuit, as the effective resistance of the two parallel transistors in their "off" state is 1/(1/R1 + 1/R2) of one transistor's resistance.

Static CMOS gates in older technologies were very power-efficient. In newer technologies, power is a primary design constraint. Power dissipation has skyrocketed due to transistor scaling, chip transistor counts and clock frequencies.

4.2.5 Instantaneous Power

The instantaneous power P(t) drawn from the power supply is proportional to the supply current iDD(t) and the supply voltage VDD.

$$P(t) = iDD(t)VDD$$

- **Energy**

The energy consumed over the time interval T is the integral of P(t)

$$E = \int_0^T i_{DD}(t)V_{DD}\,dt \tag{2.2}$$

- **Average Power**

The average power over this interval is

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}\,dt \tag{2.3}$$

- **CMOS Power Dissipation**

Power dissipation in CMOS circuits comes from two components:

Static dissipation due to

- sub threshold conduction through OFF transistors
- tunneling current through gate oxide
- Leakage through reverse-biased diodes
- Contention current in ratioed circuits

Dynamic dissipation due to

- charging and discharging of load capacitances
- Short circuit current while both PMOS and NMOS networks are partially ON

P total = P static + P dynamic

We have discussed most of the static dissipation factors before. Below 130nm static power is rapidly becoming a primary design issue eventually, static power dissipation may become comparable to dynamic power Rationed circuits have more static dissipation

- **Dynamic Power Dissipation**

Primary source of dynamic dissipation is charging of the load capacitance. Suppose load **C** is switched between VDD and GND at average frequency **fsw**. Over time **T**, load is charged and discharged **Tfsw** times. In one complete charge/discharge cycle, a total charge of **Q=CVDD** is transferred between VDD and GND

The average dynamic power dissipation is

$$P_{dynamic} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}\,dt = \frac{V_{DD}}{T}\int_0^T i_{DD}(t)dt \tag{2.4}$$

Taking the integral of the current over interval T as the total charge delivered during time T

$$P_{dynamic} = \frac{V_{DD}}{T}[Tf_{sw}CV_{DD}] = CV_{DD}f_{sw}^2 \tag{2.5}$$

As not all gates switch every clock cycle the above quantity is multiplied by α. α=1 for clock, for data maximum is α=0.5, empirically static CMOS has α=0.1 Also due to non-zero input rise and fall times (slew), both NMOS and PMOS will be ON Causes short circuit current that depends on input slew and output capacitance.

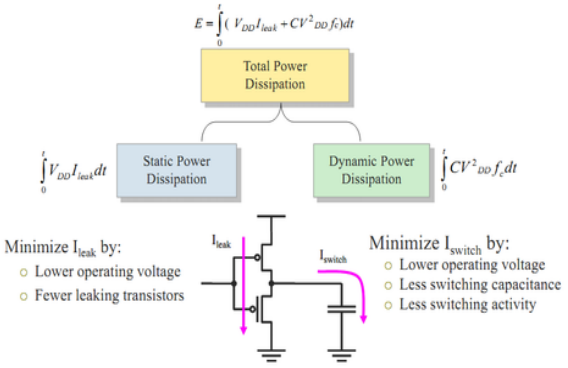


Fig 4.4: Power Dissipation

4.3 TANNER TOOL

The tool used for simulation purpose for the research work is tanner tool version 8.3. The features and functionality of this tool has been described below:

4.3.1 Simulation Tool

The design cycle for the development of electronic circuits includes an important pre-fabrication verification phase. Because of the expense and time pressures associated with the fabrication step, accurate verification is crucial to efficient design. The role of EDA tool is to help design and verify a circuit's operation by numerically solving the differential equations describing the circuit.

Tanner EDA tool is complete circuit design and analysis system that includes:

- **Schematic Editor(S-Edit)**

Schematic editor is powerful design capture and analysis package that can generate netlist directly usable T-Spice simulations.

- **T-Spice circuit simulator**

T-Spice performs fast and accurate simulation of analog and mixed analog/digital circuits. The simulator includes the latest and best device modals via tables or C functions. T-Spice uses an extended version of the SPICE input language that is compatible with all industry standard SPICE simulation programs.

All of SPICE'S device models are in comported, as well as resistors, capacitors, inductors, mutual inductors, single and coupled transmission lines, current sources, voltage sources, controlled sources, and a full complement of the latest advanced semiconductor device models from Berkeley and pho lops Labs.

- **Waveform Editor(W-Edit)**

W-Edit displays T-Spice simulation output waveforms as they are being generated during simulation. Visualizing the complex numerical data resulting from VLSI circuit simulation is critical to testing understanding, and improving those circuits. W-Edit is a waveform viewer that provides ease of use, power, and speed in a flexible environment designed for graphical data presentation.

- **Layout Editor(L-Edit)**

Tanner EDA tool includes L-Edit for layout editing, interactive DRC for real-time design rule checking during, Standard DRC for hierarchical DRC, Schematic, Node highlighting for highlighting all geometry associated with a node and SPR for standard cell place & route.

T-Spice

To transform your ideas into design, you must be able to simulate large circuits quickly and with a high degree of accuracy. That means you need a simulation tool that offers fast run times, integrates with your other design tools, and is compatible with industry standards. Tanner T-Spice circuit simulator puts you in control of simulation jobs with an easy-to-use graphical interface and a faster, more intuitive design environment.

With key features such as multi-threading support, device state plotting, real-time waveform viewing and analysis, and a command wizard for simple SPICE syntax creation, T-

Spice enables more accurate simulations by supporting the latest transistor models including BSIM4 and the pen n state Ph fillips (PSP) model.

T-Spice incorporates numerous innovation and improvements not found in other SPICE AND SPICE-compatible simulation:

- **Speed:** T-Spice provides highly optimized code for evaluating device models, formulating the systems of linear equations, and solving device models. In addition to then standard direct model evaluation, T-Spice also provide the option of table base transistor model evaluation, in which the results of device model evaluations are stored in tables and reused. Because evaluation of devices models can be computationally expansive, this technique can yield dramatic simulation speed increases.

- **Convergence:** T-Spice uses advantages mathematical methods to achieve superior numerical stability. Large circuits and feedback circuits, impossible to analyze with other SPICE products, can be simulated in T-Spice.

- **Accuracy:** T-Spice uses very accurate numerical methods and charge conservation to achieve superior simulation accuracy.

- **Macro modeling:** T-Spice simulates circuits containing “black box” macro devices. A macro device can directly use experimental data as its device model. Macro devices can also represent complex devices, such as logic gates, for which only the overall transfer characteristics, are of interest.

- **Input language extensions:** The T-Spice input language is an enriched version of the standard SPICE language. It contains many enhancements, including parameters, algebraic expressions, and a powerful bit and bus input wave specification syntax.

- **External modal interface:** You can develop custom device models using C or C++.

- **Runtime waveform viewing:** The W-Edit waveform viewer displays graphical results during simulation. T-Spice analysis results for voltages, currents, charges, and power can be written to single or multiple files.

T-Spice also supports foundry extensions, including HSPICE foundry extension to models:

- Supports the PSP, BSIM3.3, BSIM4.6, BSIM4.6, BSIM SOI 4.0, MOS 9, 11,20,30,31,40, PSP, RPI a-Si & Poly-Si TFT, VBIC, Modella, and MEXTRAM models.
- Includes two stress effect models, from the Berkeley BSIM4 model and from TSMC processes, in the BSIM3 model to provide more accuracy in smaller geometry processes.
- Supports gate and body resistance networks on RF modelling.
- Performs non-quasi- static (NQS)modelling.
- Supports comprehensive geometry-based parasitic models for multi-finger devices.
- Models partially depleted, fully depleted, and unified FD-PD SOI devices. Models self-heating and RF resistor networks.
- Performs table-based modelling for using measured device data to model a device.
- Includes enhanced diode and temperature equations to improve compatibility with many foundry model libraries.

4.3.2 Tools And Hardware Requirements

Tanner tool

- For s -edit, go to Start > Electrical> Tanner EDA > Tanner Tools v7.2 > S-Edit v7.2 64-bit. For inverter schematic and symbol. Start with creating a new design by going to File > New > New Design.
- Specify the folder you want to create your design in and the name of your design. If its name is as “ENGN1600_tutorial”. It will show up in the library’s navigator on the left.
- On public machines, the libraries might not immediately be loaded. To add library to your design, download the Tanner Libraries folder.

- Now, click the button on the "Add…" button on the libraries window-in S-EDIT, or go to File > Open > Add Library and browse the download folder to point to Libraries\All\All tanner file.

- After loading the library, several sub-libraries will show up in the libraries window, those are IO pads and devises.

- Once the library is loaded you will see the following libraries loaded in the libraries window:

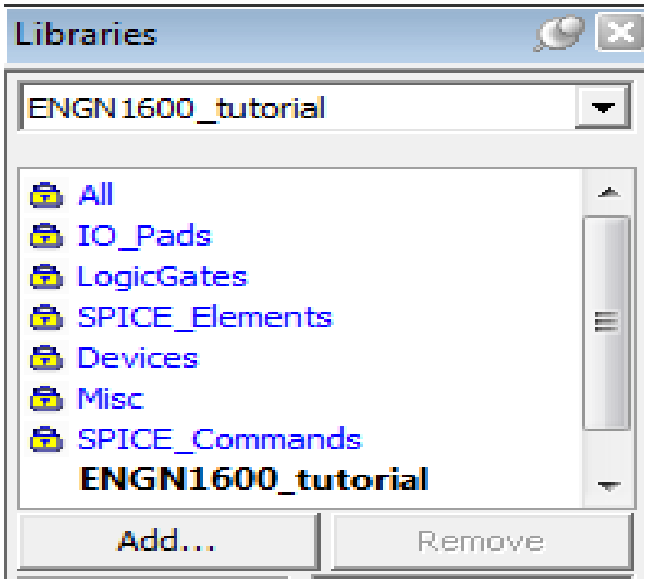


Fig 4.5: Libraries Window

- Schematic creationTo load a schematic cell, go to Cell > New View… You will see the following screen:

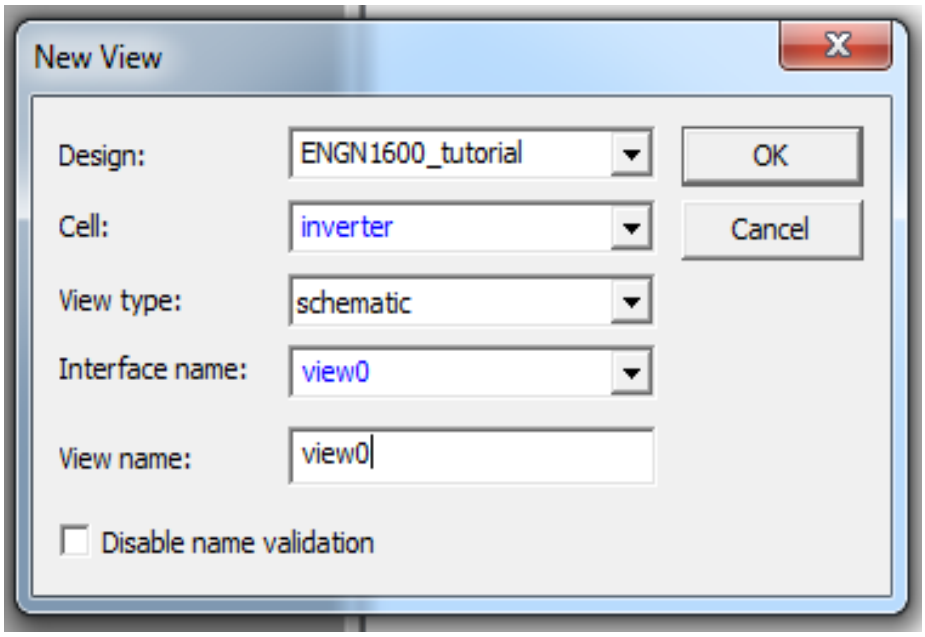


Fig 4.6: Schematic Cell To New Cell

- Give the name of the cell you want to create the schematic of and then click OK. A view of new cell will open up.
- A CMOS inverter needs an NMOS, a PMOS, V_{dd}, Gnd and In/Out ports. On the left in the libraries window, click on the library tools, its symbol objects will be shown in the window below.
- Find the NMOS from the list. Choose your device, and click on Instance, or simply drag and drop it to the design area. Make as same for PMOS, V_{dd} and Gnd symbols. Before you drop the instance, a window may show up like the one on the left below

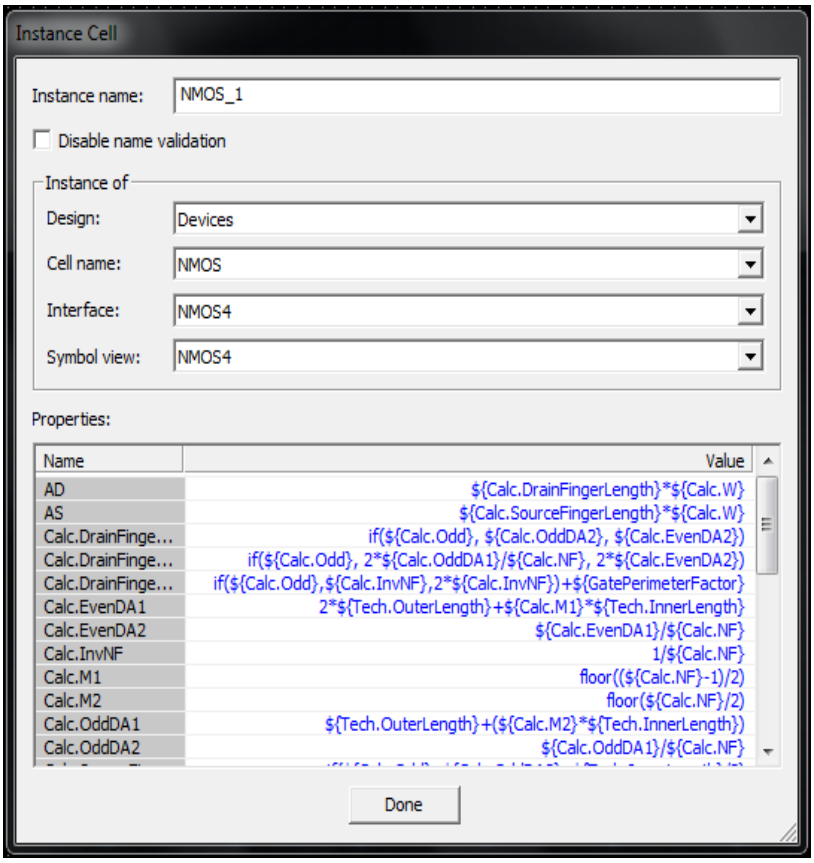


Fig 4.7: Instance cell

- After drop the time of instant, a second window (like the one on the right) will show up on the right side of the screen.
- Here we want to initiate the properties, such as its Length and Width. Or after placing the instance, just we give always single-click on it and edit its properties in the Properties navigator on the right.
- Let's say we set the length and width of NMOS devices to be 50n and 150n, and the length and width of PMOS devices to be 50n and 300n, respectively.
- NOTE: in order to run SPICE simulations with our libraries, the model has to be changed from NMOS to NMOS_VTG.

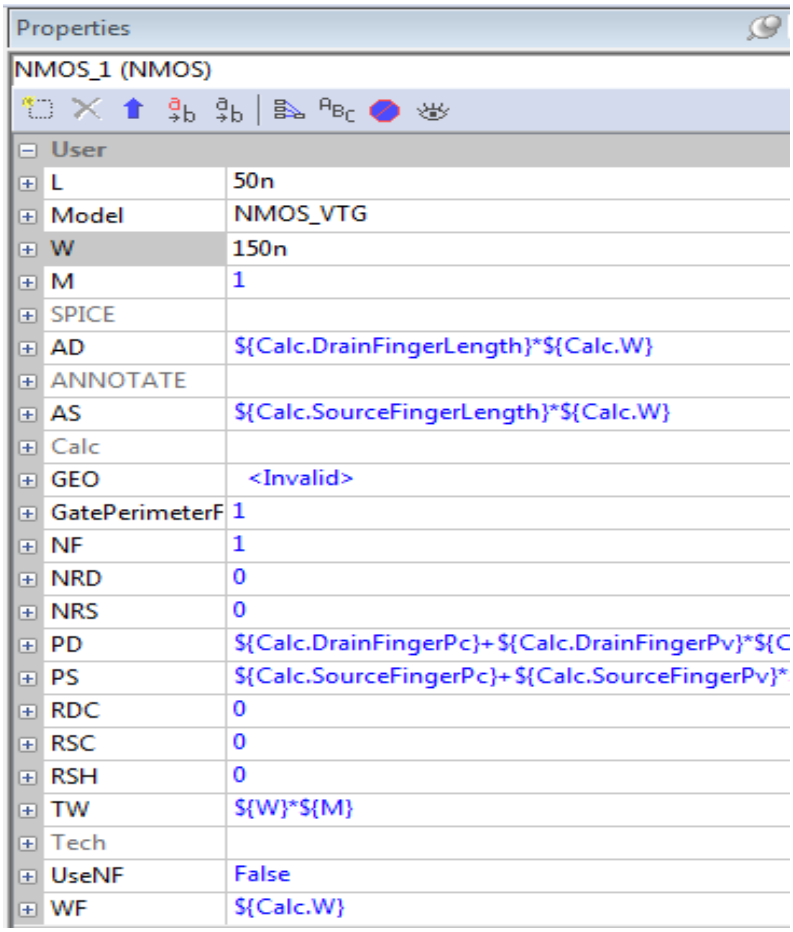


Fig 4.8: Properties NMOS

- You might have to move your parts around to make the schematic look the way you want it. When you click on a particular part on the schematic, the function of the THREE-BUTTON MOUSE is shown somewhere on the toolbar like this:

- At that point we need move to the schematic part select the part any of an either LEFT or RIGHT mouse catch and utilize the MIDDLE catch to move. Alternatively, just we should tap on the part, hold down ALT key and drag the part to elsewhere on the screen. To make the Zoom in and out, by utilize the View menu or the mouse Scroll wheel or utilize the + sign to zoom in and – sign to zoom out.

- On the off chance that we have the fundamental parts set up, then the time has come to include I/O ports and wire the parts together. On the schematic simply select the information port and yield port and give the names of the ports an extraordinarily.

- Now are going to using the wiring tool and make appropriate connections with terminals. If we clicking on the wiring tool, a SINGLE MOUSE CLICK starts the wiring. If you want to end wiring at a particular location, just give the DOUBLE CLICK. Your completed inverter schematic should look like this is at the input port and is at the output port.

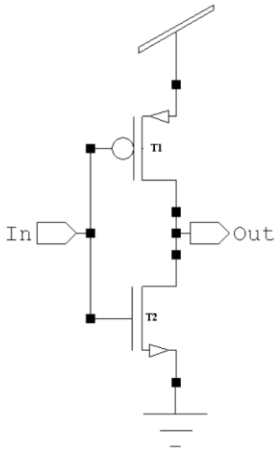


Fig.4.9: Circuit for Cmos inverter

- So we have made the connections. Now as per the specification we want to go to change the length and width of MOS transistors

4.3.3 Symbol for inverter

- The symbol is created as, first create a View — create a new cell with a new symbol view, or create a new symbol view of an existing cell using Cell > New View. Give the symbol a by the name, and select the interface it is to be associated with. Then, using the w the output ports. Make sure to give the ports the same name that you used in the

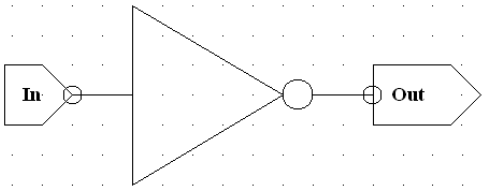


Fig 4.10: Inverter

The creation of the symbol might be helpful when you do hierarchical design.

Spice Netlist Will Be Created from The Schematic

Go to File > Export> Export Spice.

- Output filename should be specified. Check Exclude. ending Options (Without the. end, the generated SPICE file can be included in other SPICE files.) Say Export.
- The SPICE file is saved in the same directory as the schematic. The file contains information like given below:
- MNMOS_1 Out in $G_{nd}G_{nd}$ NMOS_VTG W=150n L=50n AS=135f PS=2.1u AD=135f PD=2.1u and MPMOS_1 Out in V_{dd}Vdd PMOS_VTG W=300n L=50n AS=270f PS=2.4u AD=270f PD=2.4u
- As usually spice model in complete. It is just an encapsulation of the circuit schematic that is just drawn by us.to simulating the circuit, we should add some modules, MOS by giving the stimulus input the simulation will be processed.
- The content of the description to the spice whatever we add which given below.
- Simulate the circuit with smart spice.
- After completion of the simulation, download it and copy to your folder the 45nm model that you will be using for the MOS models.
- The SPICE Net list generated from S-Edit contains the following information and is saved as inverter.

```
* SPICE export by:  S-Edit 15.22
* Export time:      Wed Jan 30 16:39:09 2013
* Design:           ENGN1600_tutorial
* Cell:             inverter
* Interface:        view0 * View:            view0
* View type:        connectivity
* Export as:        top-level cell
* Export mode:      flat
* Exclude empty cells: no
* Exclude. model:   yes
* Exclude. end:     yes
* Exclude simulator commands:     yes
* Expand paths:     yes
* Wrap lines:       no
* Root path:        C:\Users\Marco\Desktop\EN1600_test\ENGN1600_tutorial
* Exclude global pins:
* Exclude instance locations: yes
* Control property name: SPICE
MNMOS_1 Out in GndGnd NMOS_VTG W=150n L=50n AS=135f PS=2.1u
AD=135f PD=2.1u
MPMOS_1 Out in VddVdd PMOS_VTG W=300n L=50n AS=270f PS=2.4u
AD=270f PD=2.4u
```

Fig 4.11: SPICE Net list

- This produced SPICE file which has the basic description of the circuit body. By using model library now, we will add the section that specifies, the power supply, other simulation specific parameters, the type of analysis and the stimulus input

- See at the spice deck .this file contains all thing that we want to study the inverter

```
*Main inverter file
. param Supply=1.1
. include '../models/hspice_nom.include'
. options post
* Define power supply
. global VddGnd
VddVddGnd 'Supply'
*Set Transient Analysis
.tran 100ps 500ns
*** CIRCUIT NETLIST ***
*. include <name_of_extracted_spice_file>
. include 'inverter.sp'
*** INPUT STIMULS ***
* Add any input vector here
vin1 In Gnd pulse (0 Supply 10n 1n 1n 50n 100n)
* If you want to see the VTC for the inverter add a DC analysis
. DC vin1 0 Supply 0.1
. END
```

Fig 4.12: Main inverter file

- If we move from the one design to other design the blue line has not edit. The changing is necessary of the transient analysis. We want change the time. for different analysis because setting the design circuit.
- The inverts p will be shown by the second red line' will change file of spice based on Tanner tool. This example describes the inverters evaluated.
- The labels are written in the third line .and the green lines are used to write the dc analysis to create voltage transfer characteristics of invert T the green line shows how to use a DC analysis to generate a VTC for the inverter. Give the Comment for the Green line if we are not running any DC analysis.

- Then we will get started with SPICE. A more detailed description of a SPICE DECK is given beginning on page 9 of this archive.
- Imperative: Remember to have the models index in a similar catalog where your outline is spared, and duplicate the spice_ deck. sp record in the plan registry. The diverse organizers are must be incorporate into proclamation that could be indicates the all ways.
- The total spile will be made by utilizing brilliant record. That shrewd file spice.
- The information documents are beginning with sourcing device... drag the deck the internet window Click on the source catch, in the wake of altering the records spare those documents by press catch and give required data sources. Smart Spice will demonstrate the contributions of document. You shouldn't perceive any blunders.
- For investigation tap on the examination choice and run alternative tan data box will show up it will run it likewise keep running by the utilizing the easy route Ctrl-R.
- See the info look like plot which are b well needs. Tap the vectors catch. Diverse plots are open and vectors are shown itself then we go to other reason. Tap on the tran1 plot.
- Go to further procedure to achieve the required yields and data sources. At that point bolding the lines for demonstrated the great show up and surely know with utilizing control key chosen by us.
- After fruition of the running recreation reload it and it will demonstrate diverse If any change Spice input document after the run a reenactment, then reload and run it once more, we it indicates sorts of vectors accessible. named as tran1, tran2, tran3, and so on... Make sure to unselect your old plots before tapping the plot catch, other insightful old plots are show up.
- Case: it will demonstrate the all information and the outputs for reaction.
- On the off chance that mimicking the two-input door, you need to ensure that the entryway works for each of the four conceivable information blends (00, 01, 10 and 11). Suppose that your two information sources are named An and B.
- Utilizing:

vin1 A Gnd pulse (0 Supply 10n 1n 50n 100n)

vin2 B Gnd pulse (0 Supply 10n 1n 100n 200n)

- as the two-info heartbeat ought to reproduce every one of the four blends in one single run.

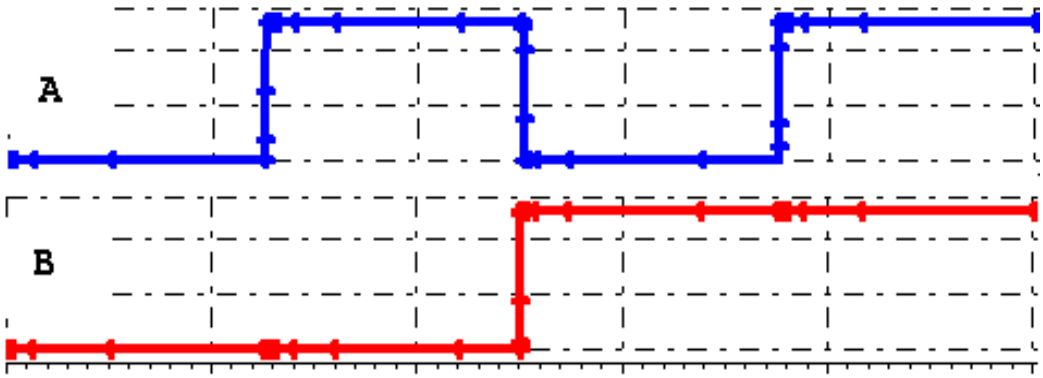


Fig 4.13: Timing Diagram

- See the tutorial below if you want to find out what exactly the pulse statement does

4.3.4 How to add a little SPICE to design circuit

- For this class we will utilize SILVACO's Smart Spice, an industry standard circuit test system. This instructional exercise will give you a fundamental thought on the most proficient method to compose flavor documents starting with no outside help or how to alter zest net records produced by Tanner.

- Before we begin ensure you download 45nm Technology record from here (same secret key). Case of the flavor deck circuit.

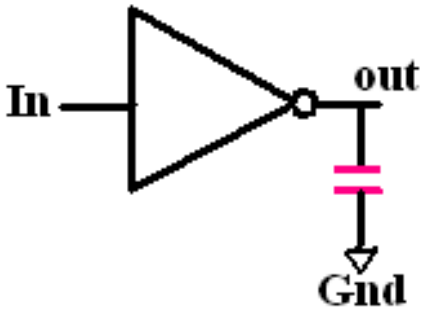


Fig 4.14: flavor deck

```
* Spice Net list of an Inverter
* This spice deck creates a simple inverter with an output load
* Cap, runs a transient analysis and measures the propagation delay
**********************************************************************
* Set supply and library
**********************************************************************
. temp 27 * Set operating temp
. param Supply=1.1
. include '../models/hspice_nom.include' * the 45nm MOS model library
. options post * this will allow you to view the result
**********************************************************************
* Define power supply
**********************************************************************
. global VddGnd
VddVddGnd 'Supply'
**********************************************************************
* Define Sub circuits
**********************************************************************
.subcktinv In Out
M1 Out In GndGnd NMOS_VTG W=150n L=50n AS=135f PS=2.1u AD=135f PD=2.1u
M2 Out In VddVdd PMOS_VTG W=300n L=50n AS=270f PS=2.4u AD=270f PD=2.4u
```

```
.ends
********************************************************************************
* Top level simulation net list
********************************************************************************
x1 In Out inv
c1 Out Gnd 10f
********************************************************************************
* Stimulus
********************************************************************************
Vin In Gnd pulse (0 'Supply' 5n 100p 100p 25n 50n)
* Run a transient analysis
.tran .01ns 100ns
********************************************************************************
* Measurements
********************************************************************************
* Measure delay of the inverter
. measure prop_delay
+ TRIG v(In) VAL='Supply/2' RISE=1
+ TARG v(Out) VAL='Supply/2' FALL=1
********************************************************************************
* End of Deck
********************************************************************************
.end
```

Fig 4.15: Simulation Net List

Looks scary? Try not to freeze...

Here are some regular things you find in the above zest deck

- The FIRST LINE of the deck is constantly translated as the 'Title'. Brisk reference is help full to title for any circuit.

- Any line that starts with a * is a COMMENT and will be overlooked by the SPICE device.

- In SMARTSPICE on the off chance that you need to square remark utilizes #COM and #ENDCOM.

- Eg.

  #COM

  this is a remark line1

  this is a remark line2

  #ENDCOM

  . temp explanation gives the temperature in Celsius else it will default the room temperature.

  the constants are incudes in the announcements which are composed in the programmed and know how "Supply" is utilized as a part of the above SPICE deck.

- . all articulation is incorporated into the announcement by the incorporate key ward. NMOS and PMOS display definitions for the 45nm strategy for the manufactures.

  Let's see the estimations of the "Vdd" and "Gnd" in circuits.

  The things are specifically duplicated by the press the catch duplicate all documents are show up in the record extend. Every one of the things that I have examined so far can be straightforwardly duplicated to any SPICE deck. temp must be change it required.

- This is the straightforward plan so that not require the sub circuits in the event that we took the much complex outline. the genuine net rundown will plan by the basic definitions and the general arrangement is as subcircuit and name input 1,2 and it will end with sub definition.

- Go to the fundamental part. The main level of the net rundown of the simulation.in this really clarify the associations of fringe gadgets are going to determined after these alterations are done. the resister and capacitances are indicated well. The format of the release of the considerable number of segments are given resister after capacitances and transistors alongside the greater part of the info and the output the width of the length and proportion is all around characterized.

- The anther part is only clarifying the reenactment area which for patter of data sources. For computerized reproductions, you will either utilize the beat or the pwl (piecewise linear). I suggest beat explanation over pwl. The arrangement of the beat explanation is:

  voltage node1 node2 Pulse

  (Start_voltend_voltinitial_delayrise_timefall_timepulse_width period

  So, the beat explanation in the deck above: Vin In Gnd pulse (0 "Supply" 5n 100p 25n 50n)

  indicates a heartbeat at hub In, beginning ascent time is the characterized as time taken for the flag going the 90%of its unique esteem and fall time will be the ideal opportunity for flag setting off to the 10% of its unique esteem.

- Up to now we have done the setup of the all voltages and the net rundown of the gadgets then other segment is only tell the which sort of recreation is to be utilized. These only dc investigation or transient examination for dc configuration is indicated below. start1 star2… …same as to transient examination.

- We ought to include an end proclamation. Now and then you might need to make a few estimations without going through a repetitive technique for deriving certain qualities from a plot. In the above illustration, the inverter gives the engendering delay between the information sources and yields and figure the components that are voltage current power time here + image demonstrates that not expansion but rather it gives that as one line which for some lines are required so inputs the zest of explanation with consider to

the past lines. Similarly for instance this is the way you would gauge the normal energy of the inverter:

. the energy of the normal. FROM=10n TO 50n

At that point effortlessly it demonstrates the net rundown components again take after the run part. Appreciate next part.

Like this we take after the circuit plan of the flavor demonstrate.

4.3.5 Creating Curve for Pmos Of V-I Characteristics

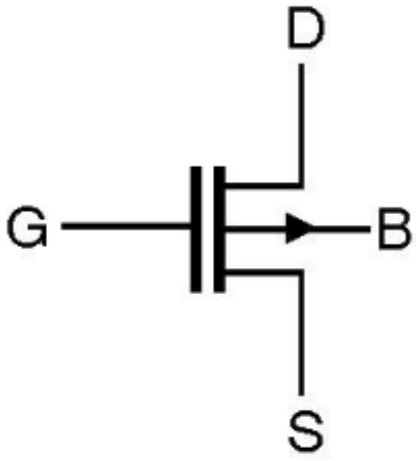


Fig 4.16: PMOS

Copy the following SPICE deck to your folder. Make sure you have downloaded the 45nm library file into the same folder.

```
*I-V curve PMOS
.param Supply=1.1
.include '../models/hspice_nom.include'
.options post
* Define power supply
.global VddGnd
VddVddGnd 'Supply'
*** CIRCUIT NETLIST ***
*** mpmos1 drain gate source bulk L= length W= width
M1 dsgsVddVdd PMOS_VTG W=500n L=160n
*** DEFINE VOLTAGE CONNECTIONS ***
**********************************
* you need to change some connections around for NMOS
* Voltage Name Node+ Node- Voltage Value
VdsVdd ds 'Supply'
VgsVddgs 'Supply'
****************************************
*** INPUT STIMULS ***
*increase Vds from 0 to 1.1v with step of 0.01 increase Vgs from 0 to 1.1v with
step of 0.2
.DC Vds 0 1.1 0.01 SWEEP vgs0 1.1 0.2


.END
```

Fig 4.17: I-V curve PMOS

Open Smart Spice and load the spice deck. Run the spice deck.

Plot i(V_{ds}vs.V_{ds})by clicking  and choosing i(V_{ds}) from the list.

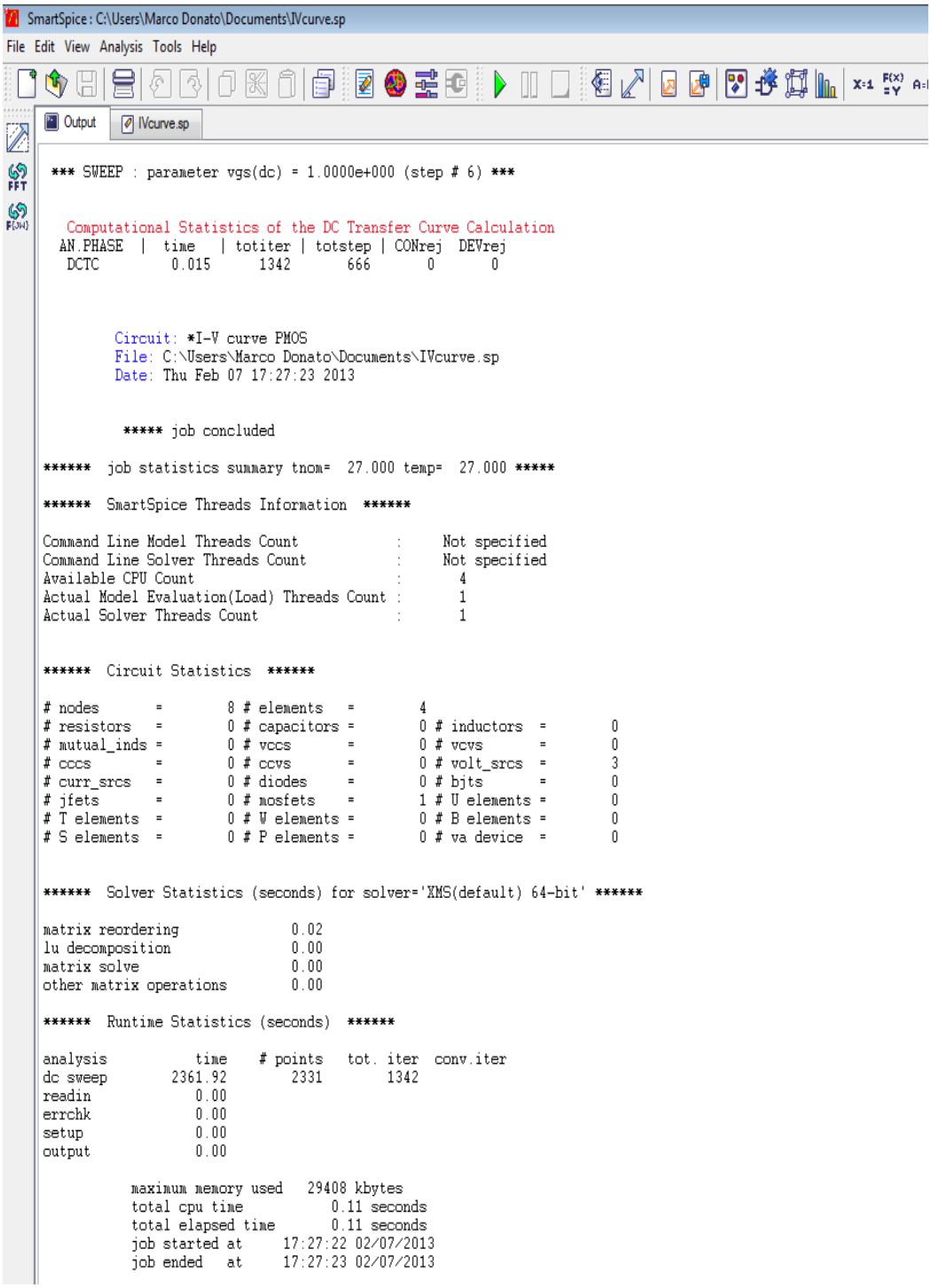


Fig 4.18: Smart spice output

This will invoke SmartView and produce the following plot for the PMOS:

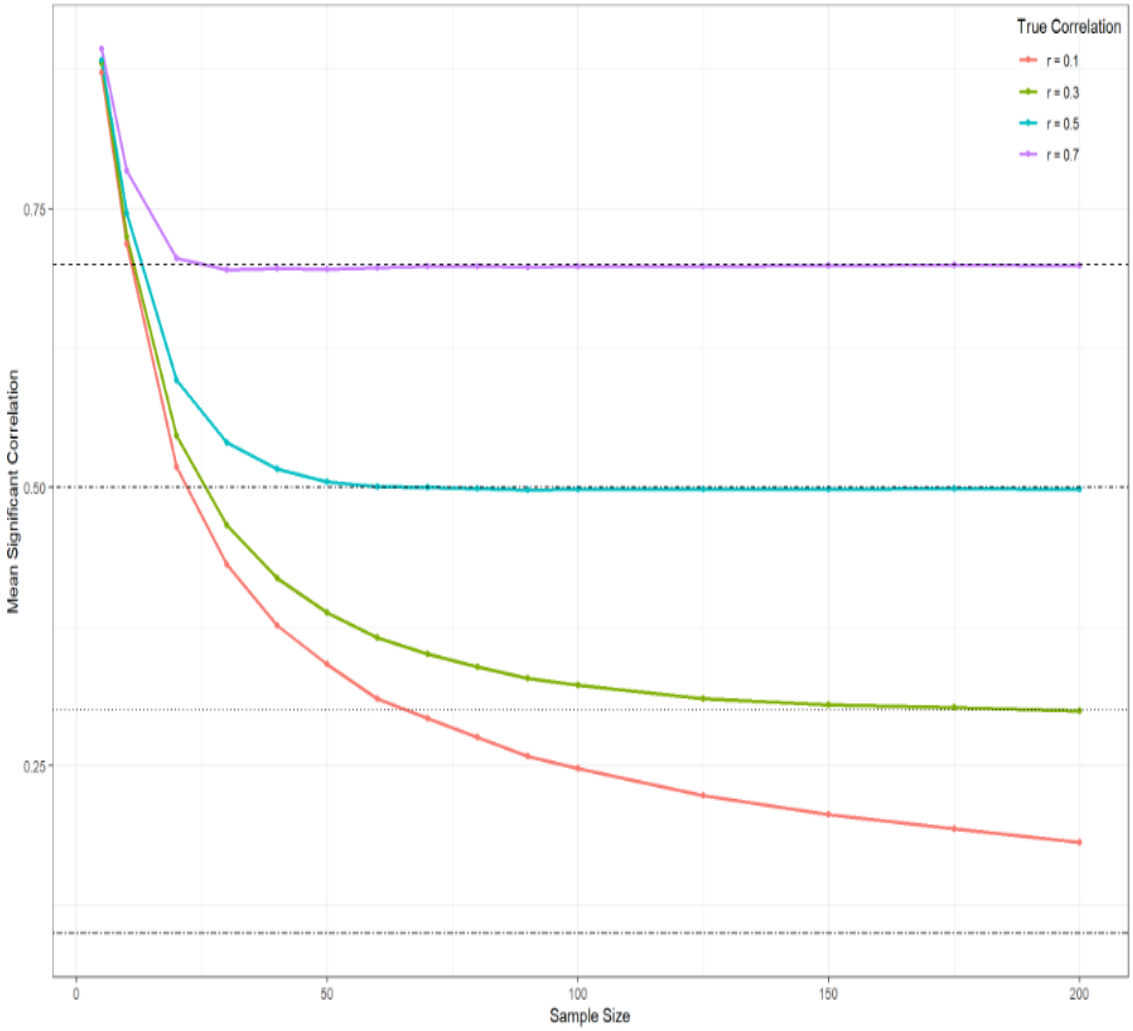


Fig 4.19: DC Analysis

This should give you an idea of what to do for an NMOS.

4.3.6 Smart Spice Plots

After the complete analysis, click on  from the toolbar to launch the vectors window.

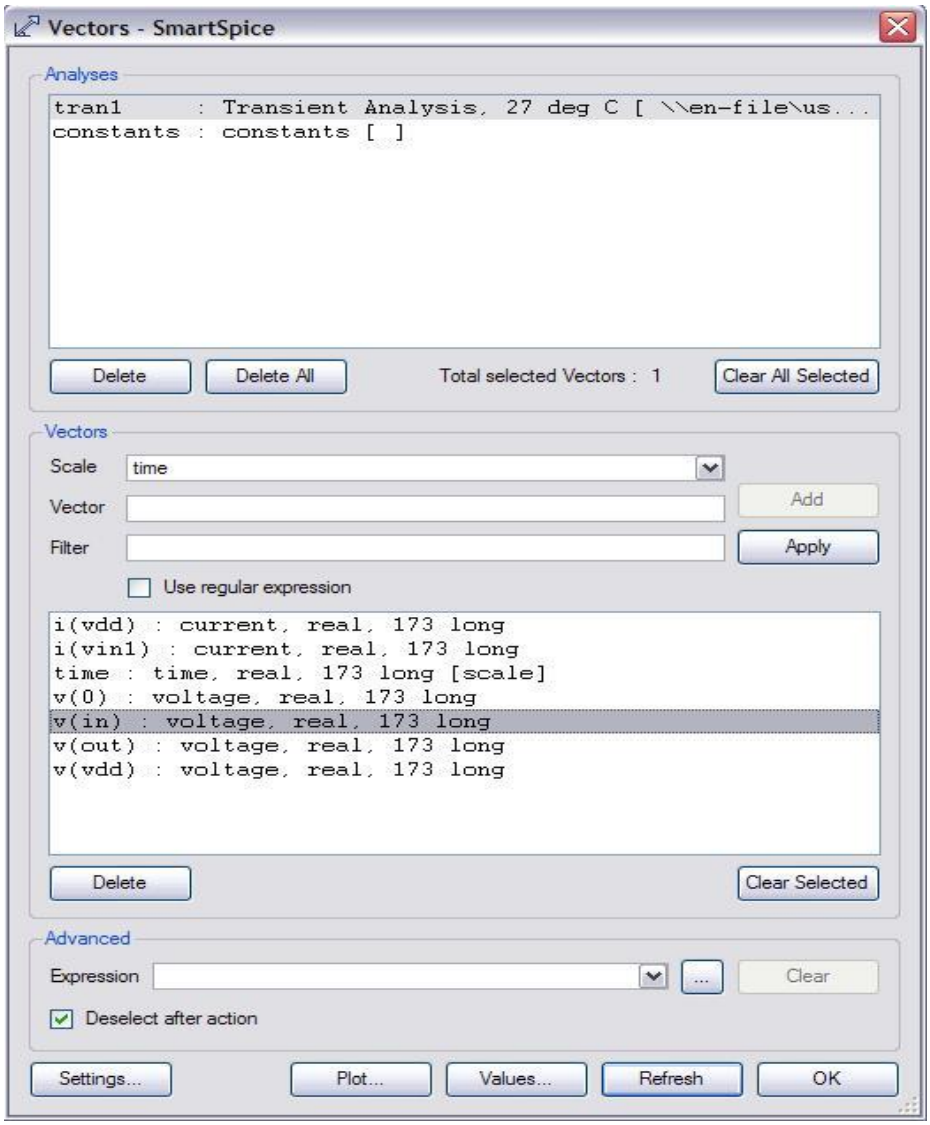


Fig 4.20:Vectors-Smartspice

Tap on the voltage name that you need to print. Click Plot.

At the point when it's plotted in SmartView, tap on the left, which will begin another plot space.

In Smart Spice once more, tap on the second voltage name. Click Plot.

Rehash this procedure until we get the information and yield plotted

This will bring about every one of the sources of info and yield voltages on an indistinguishable plot from subplots.

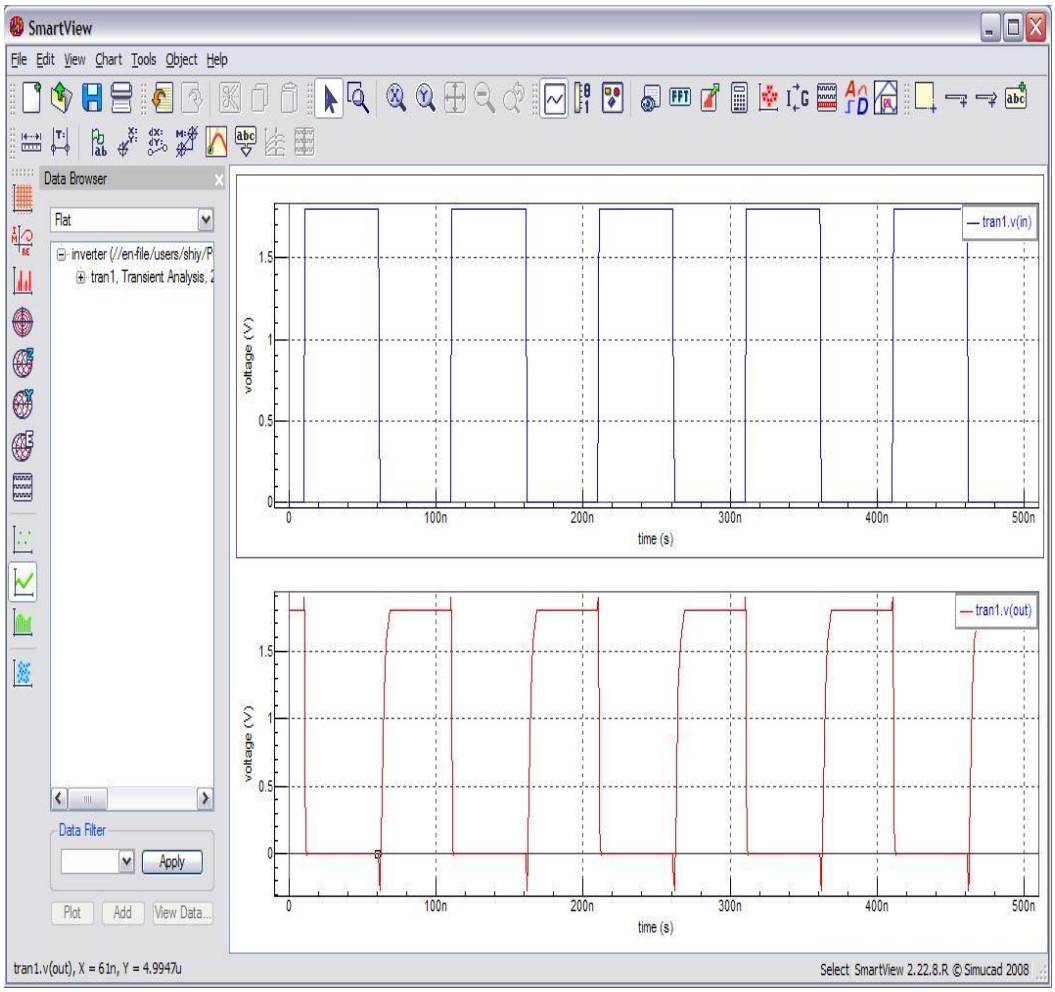


Fig 4.21: Simulation output

Easy for you to visualize and simulate.

If you have plotted two signals in one plot and want to split them up, right click on the plot and select Split All/Selected. Then it will show a stacked view.

Because of default foundation will be dark. We can change this to a white foundation by going to Edit > Preferences > Colors and choosing a white foundation with dark tomahawks.

CHAPTER-5

RESULTS

5.1 RESULT

5.1.1 Existing Method Using 21 Transistors

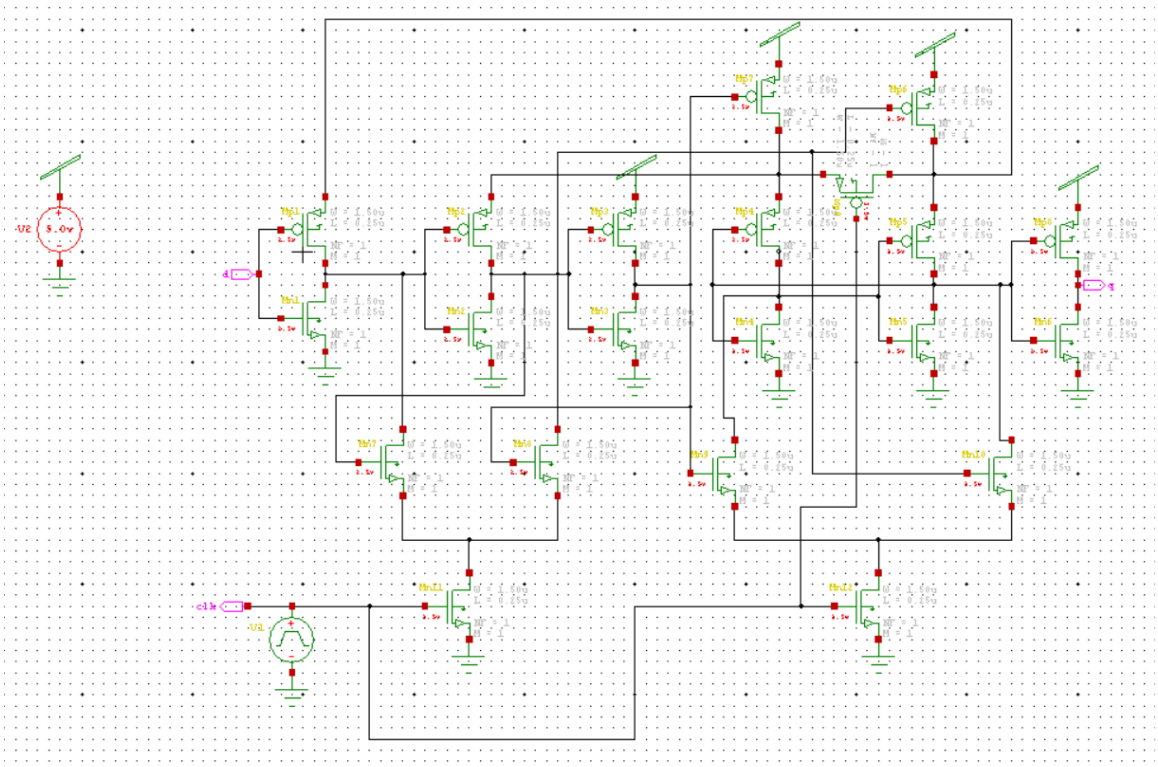


Fig 5.1: Circuit connection of Master- slave SR-flip-flop using TCFF technique

The figure 5.1 represents the circuit of master- slave SR-flip-flop using modified Pass transistor input technique. The circuit is designed in the tanner tool. The input to the circuits is SR and the clock.

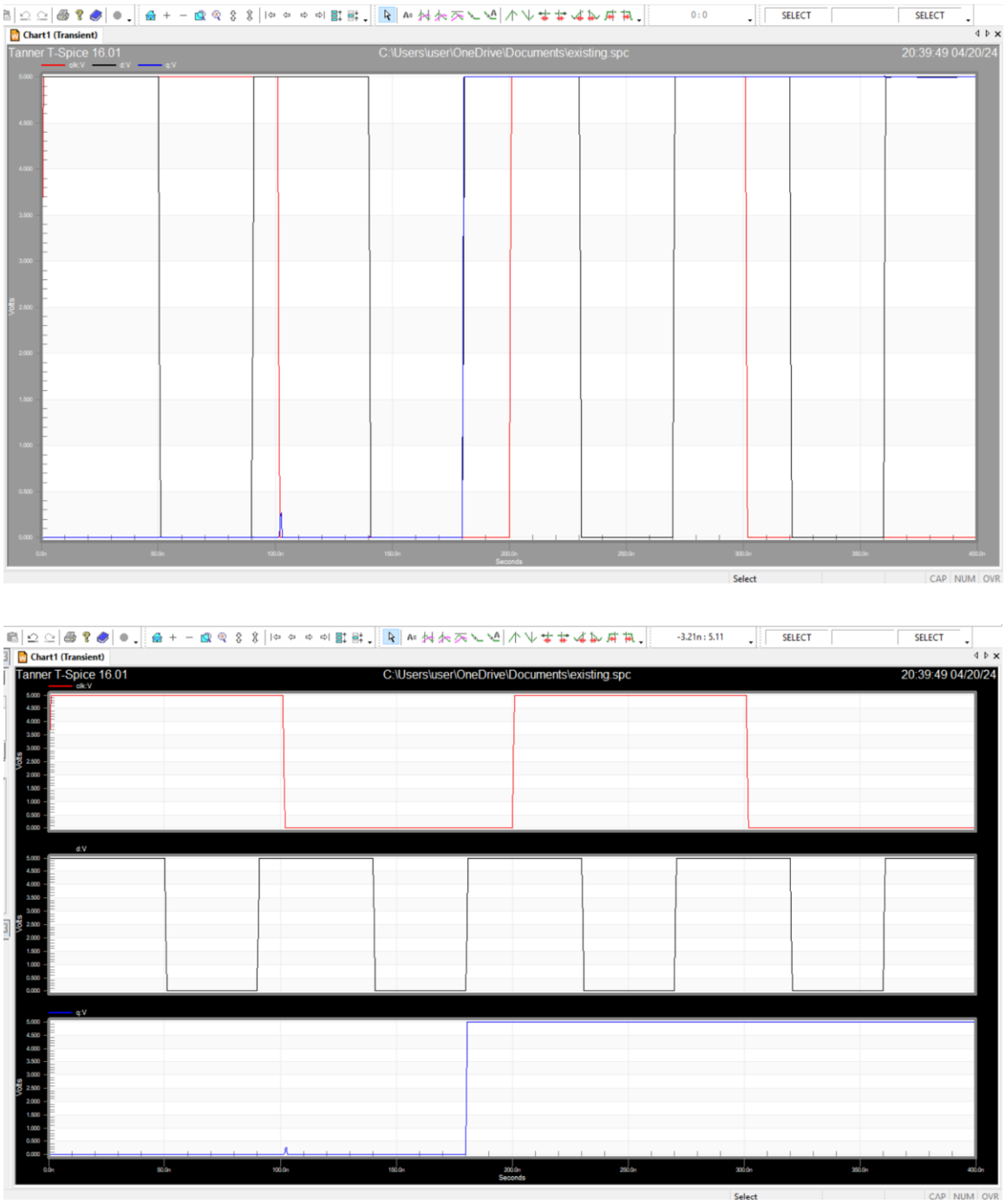


Fig 5.2: Simulation wave forms low power 21- transistor true single phase clocking using Pass transistor schemes

The represents the outputs wave forms of the low power 21- transistor true single phase clocking using Pass transistor schemes, v(clk) is the clock input of the circuit, v(d) is the data input of the circuit, v(q), is the output of circuit.

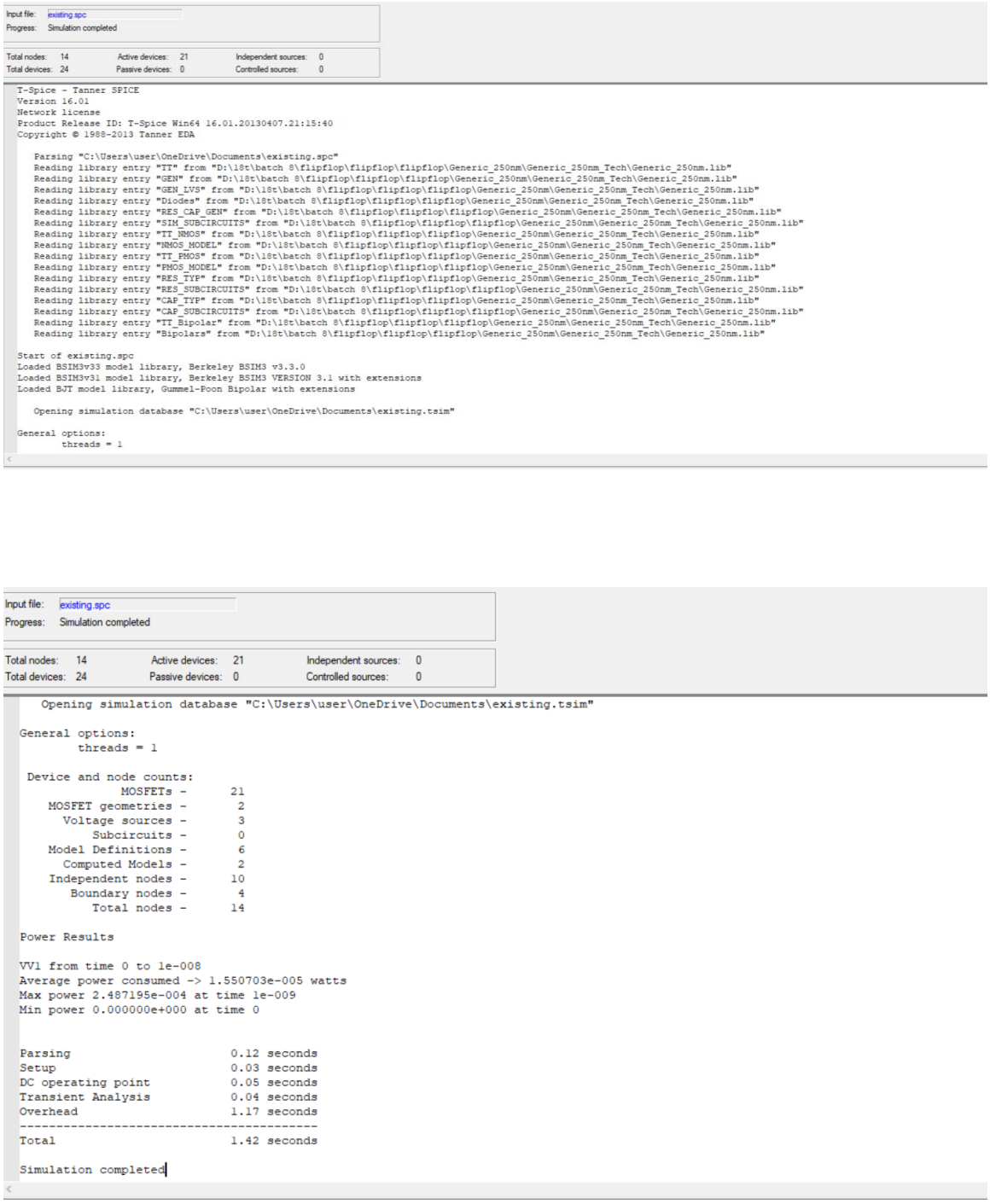


Fig 5.3: Power Consumption 21T

5.1.2 Proposed Method Using 18 Transistor

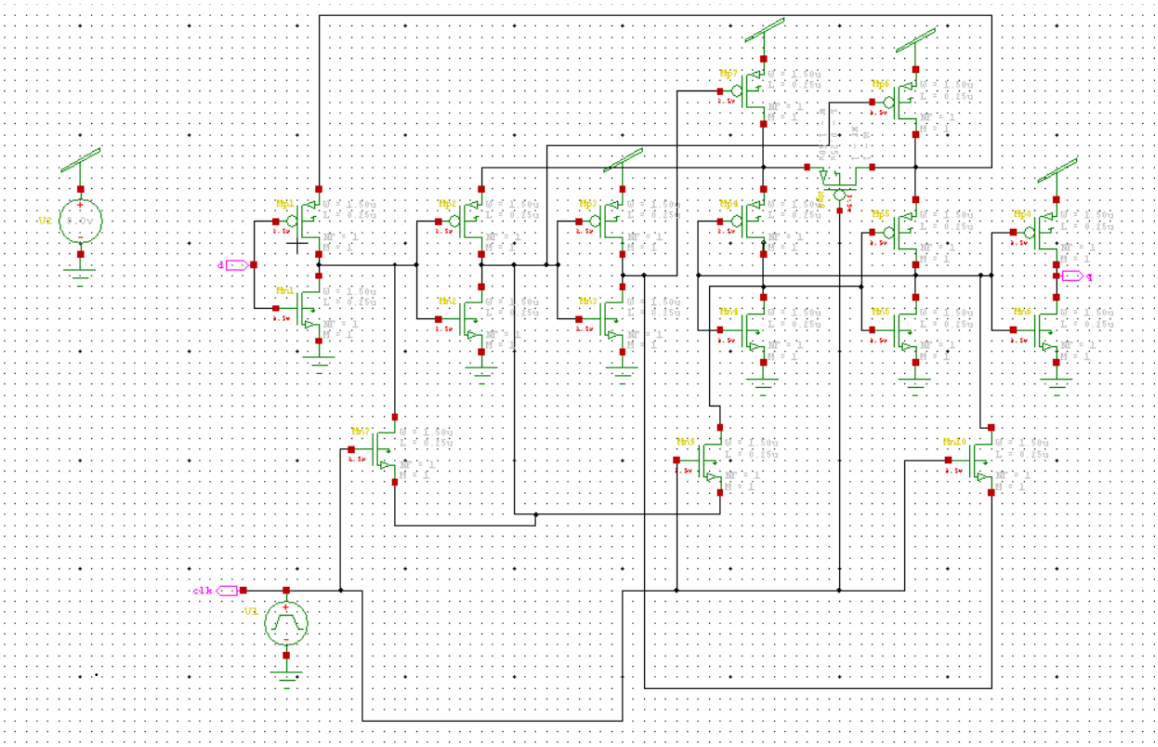


Fig 5.4: Circuit connection of Master- slave D-flip-flop using TCFF technique

The figure 5.4 represents the circuit of master- slave D-flip-flop using modified logic reduction input technique. The circuit is designed in the tanner tool. The input to the circuits is D and the clock.

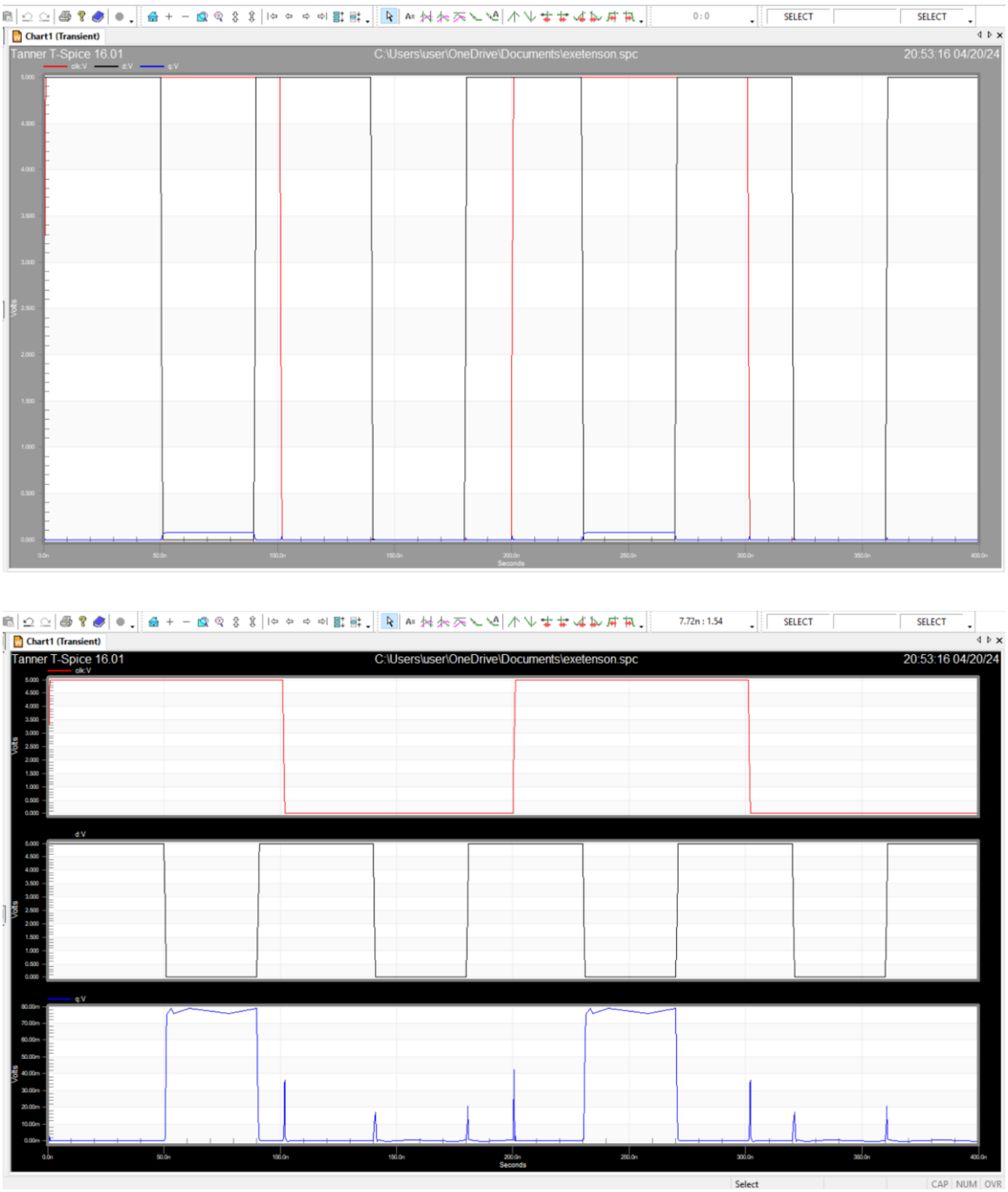
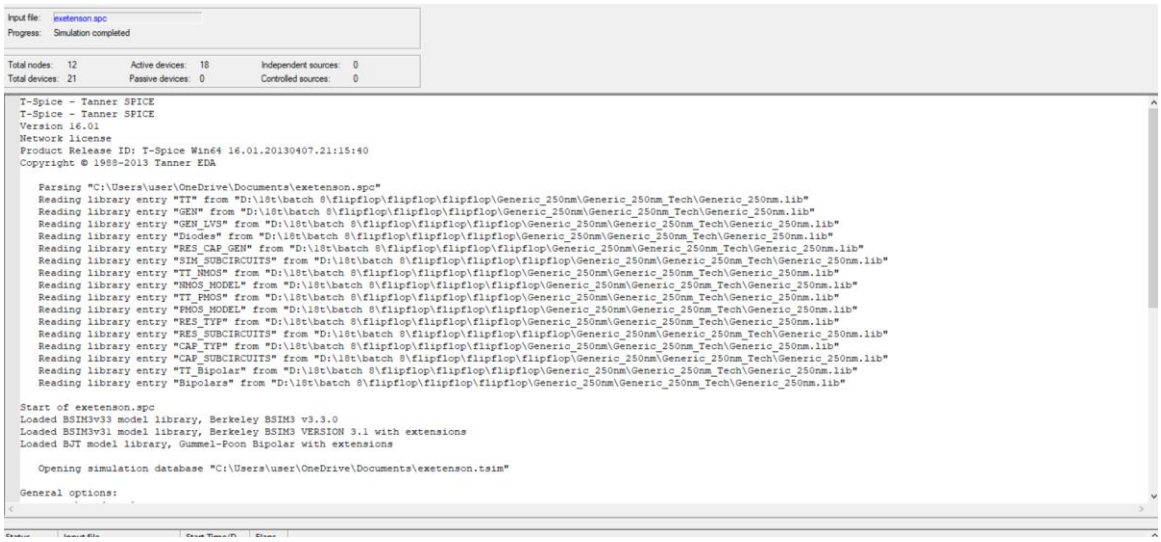


Fig 5.5: Simulation wave forms low power 18- transistor true single phase clocking using logic reduction schemes

The represents the outputs wave forms of the low power 18- transistor true single phase clocking using logic reduction schemes, v(clk) is the clock input of the circuit, v(d) is the data input of the circuit, v(q), is the output of circuit.



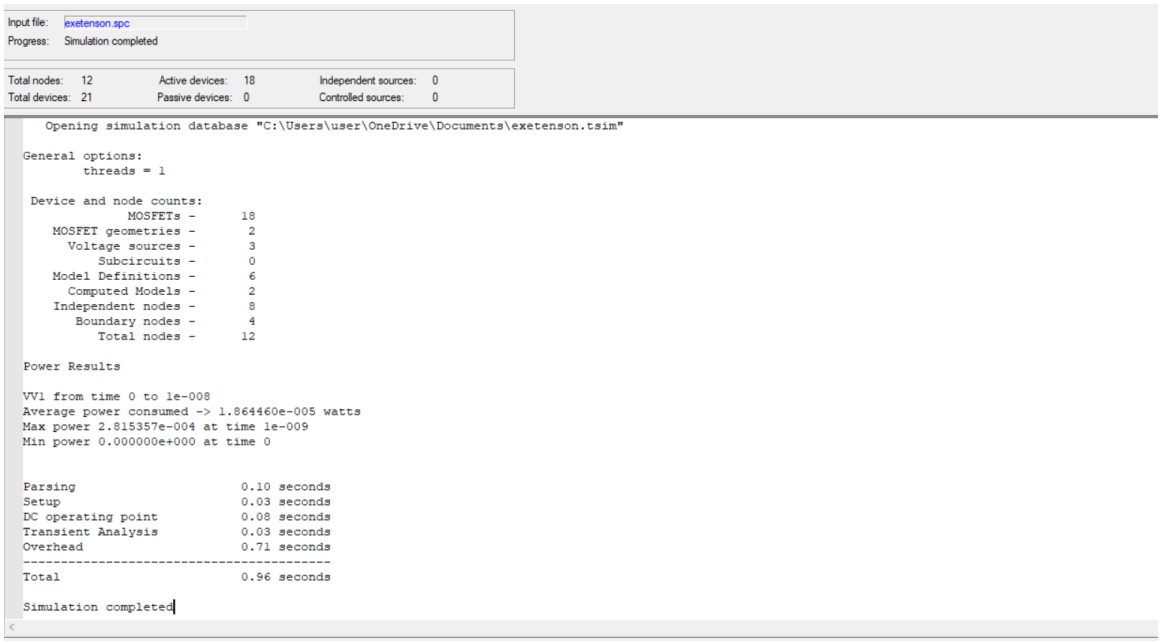


Fig 5.3: Power Consumption 18T

5.2 Netlist Details of The Circuit

Transistor count

Transistor - 21

Power Results

VV1 from time 0 to 1e-008

Average power consumed -> 1.550703e-005 watts

Max power 2.487195e-004 at time 1e-009

Min power 0.000000e+000 at time 0

Propagation Time

Parsing	0.12 seconds
Setup	0.04 seconds
DC operating point	0.09 seconds
Transient Analysis	0.05 seconds
Overhead	0.78 seconds

Total	1.07 seconds

Transistor count

Transistor - 18

Power Results

VV1 from time 0 to 1e-008

Average power consumed -> 1.864460e-005 watts

Max power 2.815357e-004 at time 1e-009

Min power 0.000000e+000 at time 0

Propagation Time

Parsing	0.11 seconds
Setup	0.03 seconds
DC operating point	0.08 seconds
Transient Analysis	0.03 seconds
Overhead	0.39 seconds
---	---
Total	0.64 seconds

5.3 Advantages

High speed

Low power consumption and low voltage

Reduce circuit Area

Reduce long discharging path problem

5.4 Applications

Used in low power applications

Used in Memories

Used in Sequential circuit

Used in Chip designs

CHAPTER-6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

A new flip-flop is designed by using 18 transistors. For the proposed work, we have considered following parameters, which are C to Q delay, reduction in PMOS transistor count, no clock overloading, and lowering circuit complexity. The proposed circuit outperformed by 52.52%, 62.89%, and 49.73% in terms of power consumption as compared to ACFF, TCFF and LRFF respectively. In terms of leakage power our circuit excelled by 4.20%, 19.27% and 39.75% when compared with ACFF, TCFF, and LRFF respectively. It also excels in performance at different supply voltages, frequency range and does not have clock overloading. All the parameter taken for this work have been successfully addressed. The proposed design is also compared with the 18T TSPC FF. In which we are getting comparable results and, in some comparison, proposed circuit excels over 18T TSPC and hence proves the efficiency.

6.2 FUTURE SCOPE

- We hope that presented results will encourage further research activities in TCFF technique.
- The issue of sequential logic design with TCFF is currently being explored, as well as technology compatibility.
- More work was recently done in automation of logic design methodology based on TCFF technology.

REFERENCES

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