

- In this assignment, I am tasked with designing a 32-bit ripple carry adder circuit. Below is the flow chart illustrating the structure of the 32-bit ripple carry adder, which comprises a collection of 32 full adders.

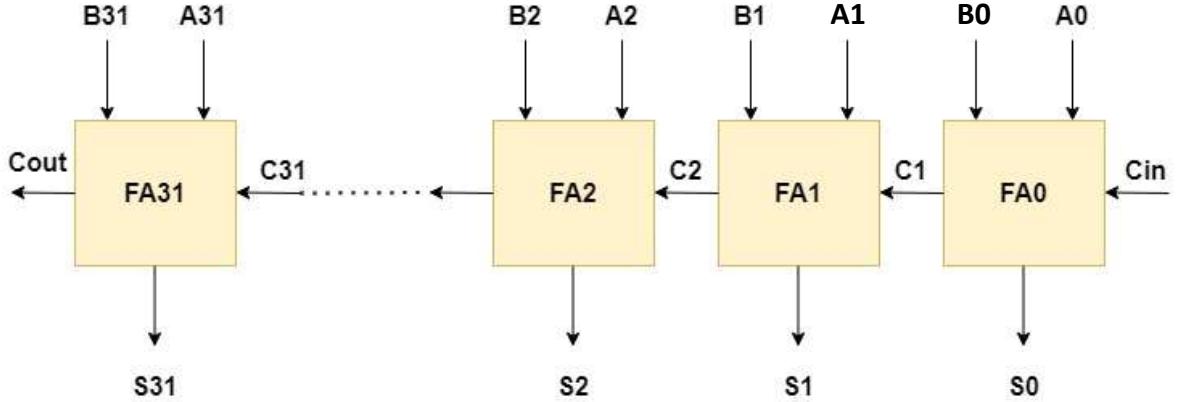


FIGURE 01: DIAGRAM OF 32-BIT RIPPLE CARRIER ADDER

- So far, I have initiated the design process by creating the design for a full adder. The information below presents the Boolean expression and the corresponding logic circuit for the full adder.

$$S_o = A_0 B_0 C_{in} + \overline{A_0} \overline{B_0} C_{in} + A_0 \overline{B_0} \overline{C_{in}} + \overline{A_0} B_0 \overline{C_{in}} = A_0 \oplus B_0 \oplus C_{in}$$

$$C_0 = A_0 B_0 + B_0 C_{in} + A_0 C_{in} = A_0 B_0 + C_{in}(A_0 + B_0)$$

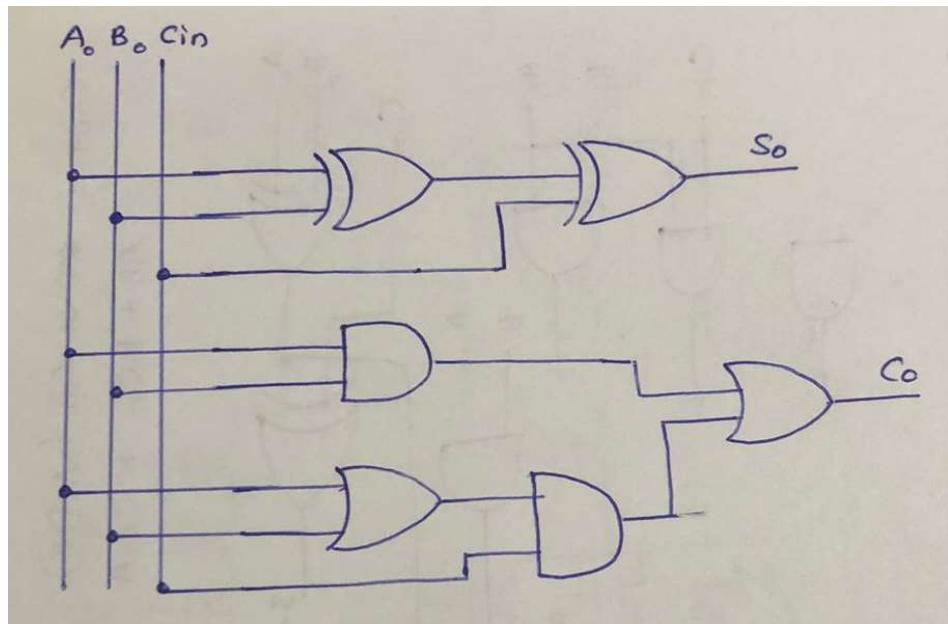


FIGURE 02: LOGIC CIRCUIT OF THE FULL ADDER

- By replacing all the gates with CMOS components, the resulting circuit for a full adder is as follows.

CMOS equivalent circuit for C_0

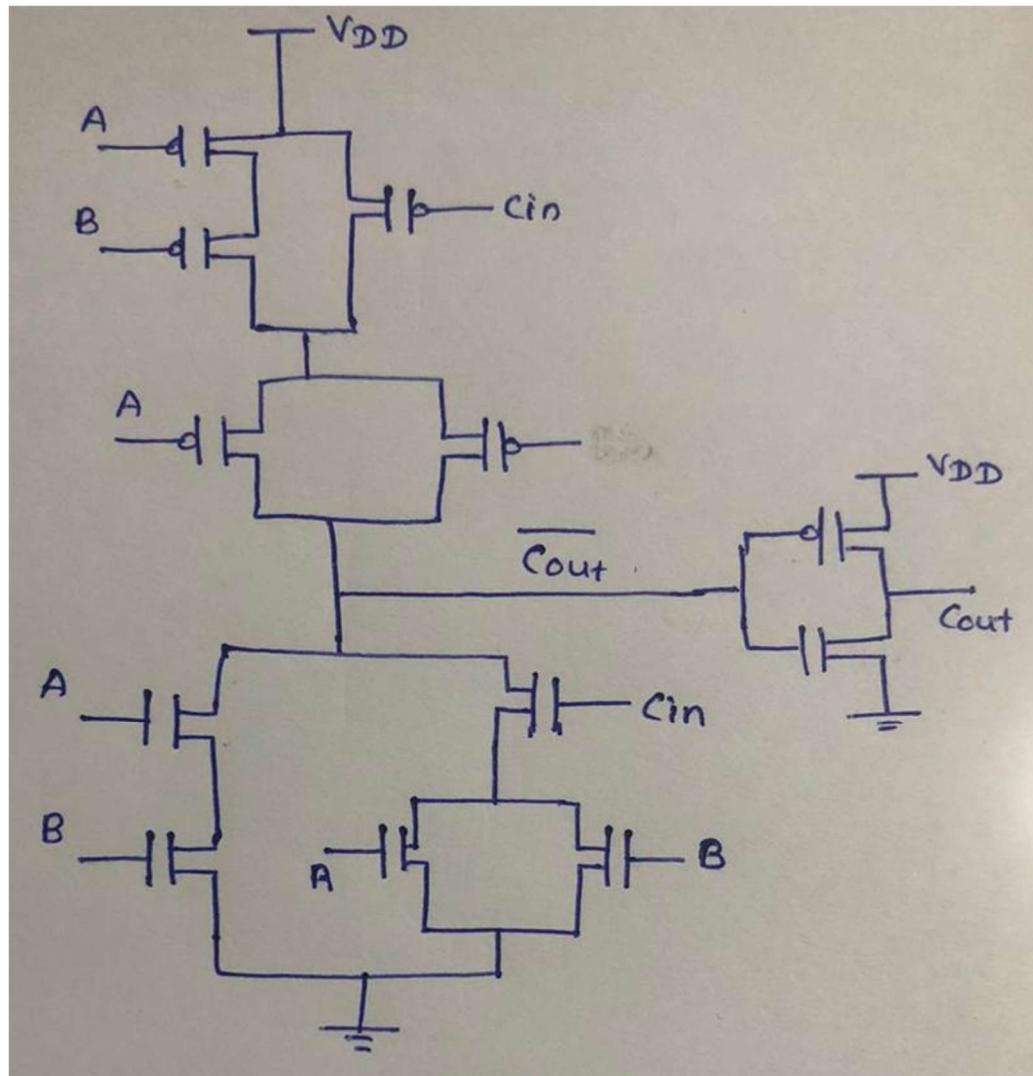


FIGURE 03: CMOS EQUIVALENT CIRCUIT FOR C_{out}

CMOS equivalent circuit for S_0

- To optimize the implementation and reduce the number of transistors required, let's rearrange the equation using \bar{C}_0 . This rearrangement aims to simplify the circuitry and enhance efficiency while maintaining the functionality of the full adder.

A_0	B_0	C_{in}	S_0	C_0	\bar{C}_0
0	0	0	0	0	1
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	0

$$S_0 = C_{in}\bar{C}_0 + B_0\bar{C}_0 + A_0\bar{C}_0 + A_0B_0C_{in}$$

$$S_0 = \bar{C}_0(C_{in} + B_0 + A_0) + A_0B_0C_{in}$$

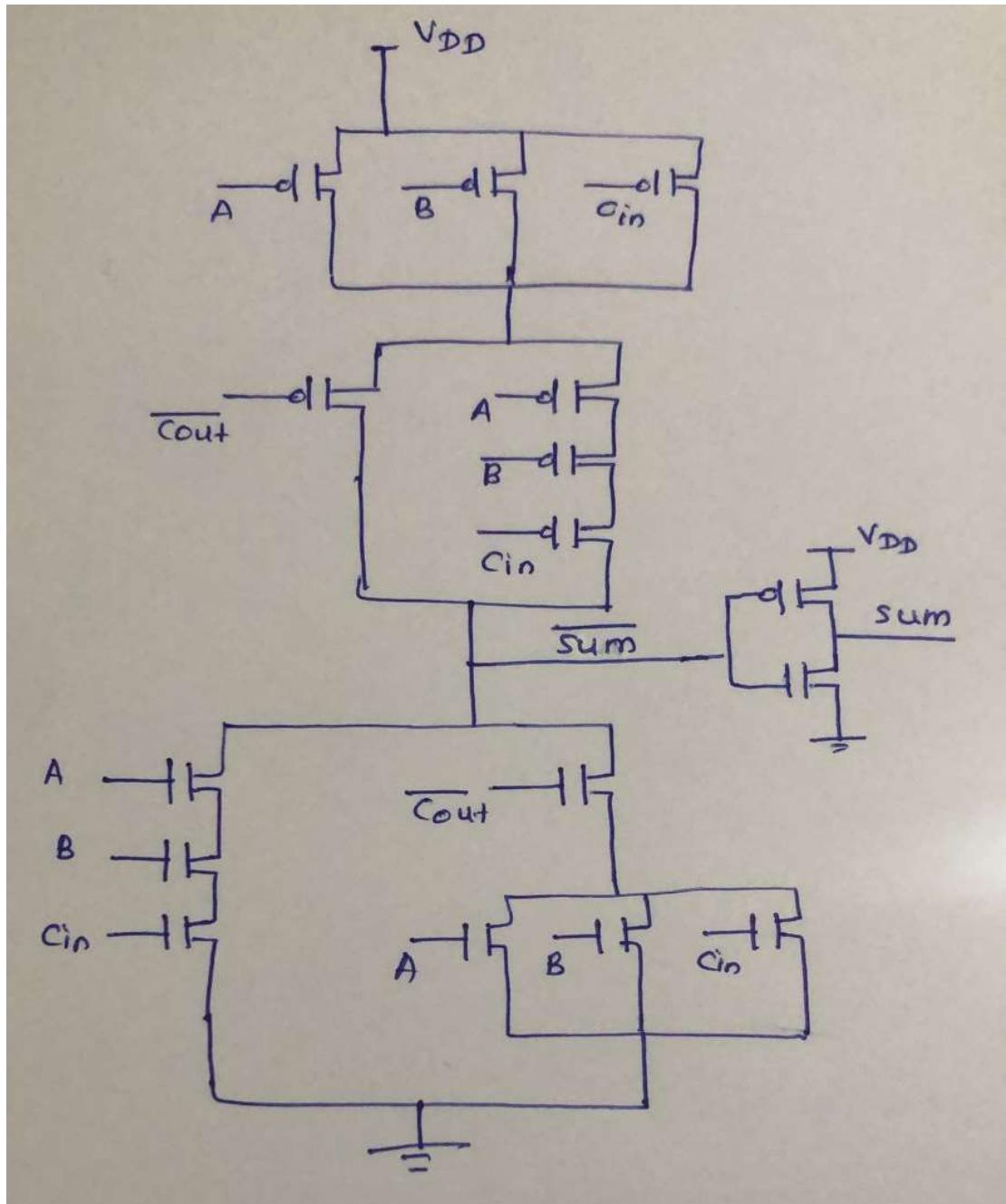


FIGURE 04: CMOS EQUIVALEN CIRCUIT FOR SUM

Full Adder (1-bit Adder)

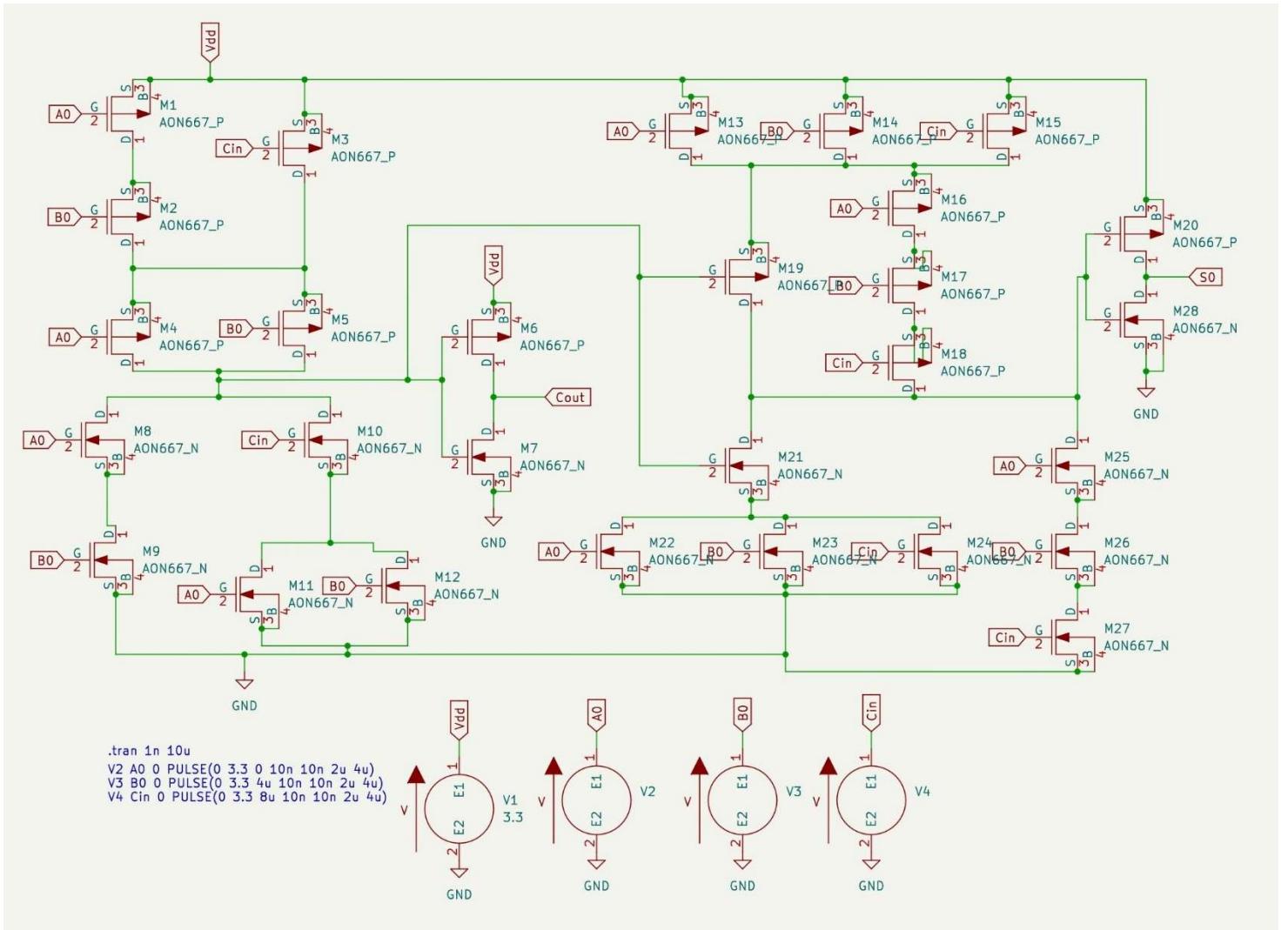


FIGURE 05: SCHEMATIC DIAGRAM FOR THE FULL ADDER USING CMOS TECHNOLOGY

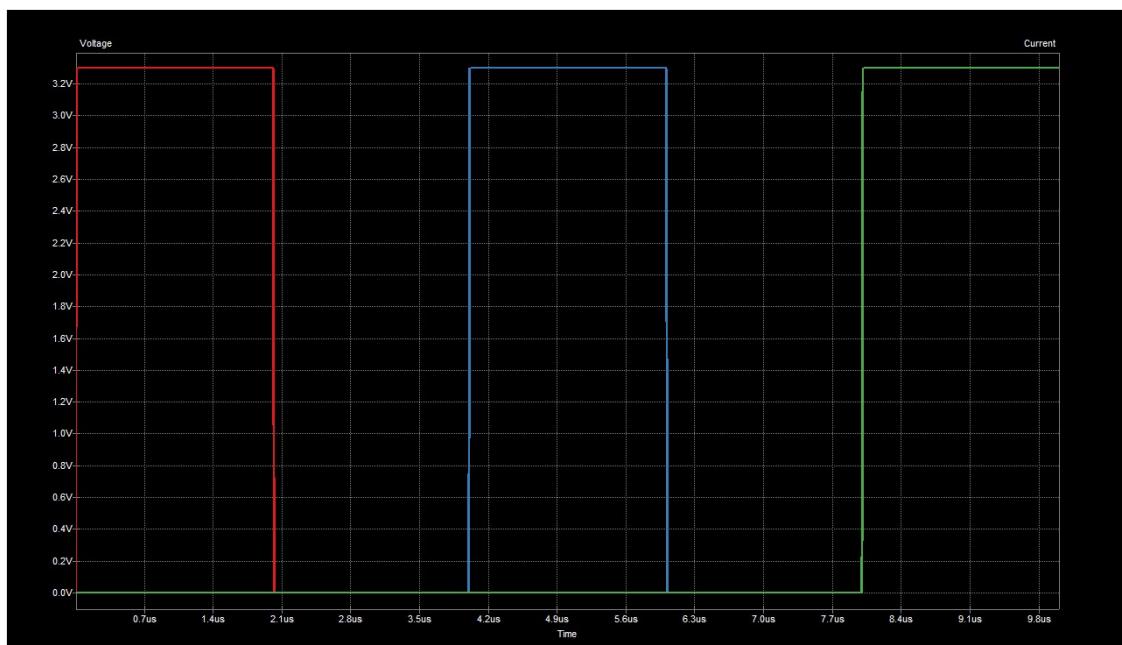


FIGURE 06: INPUT SIGNALS TO THE FULL ADDER

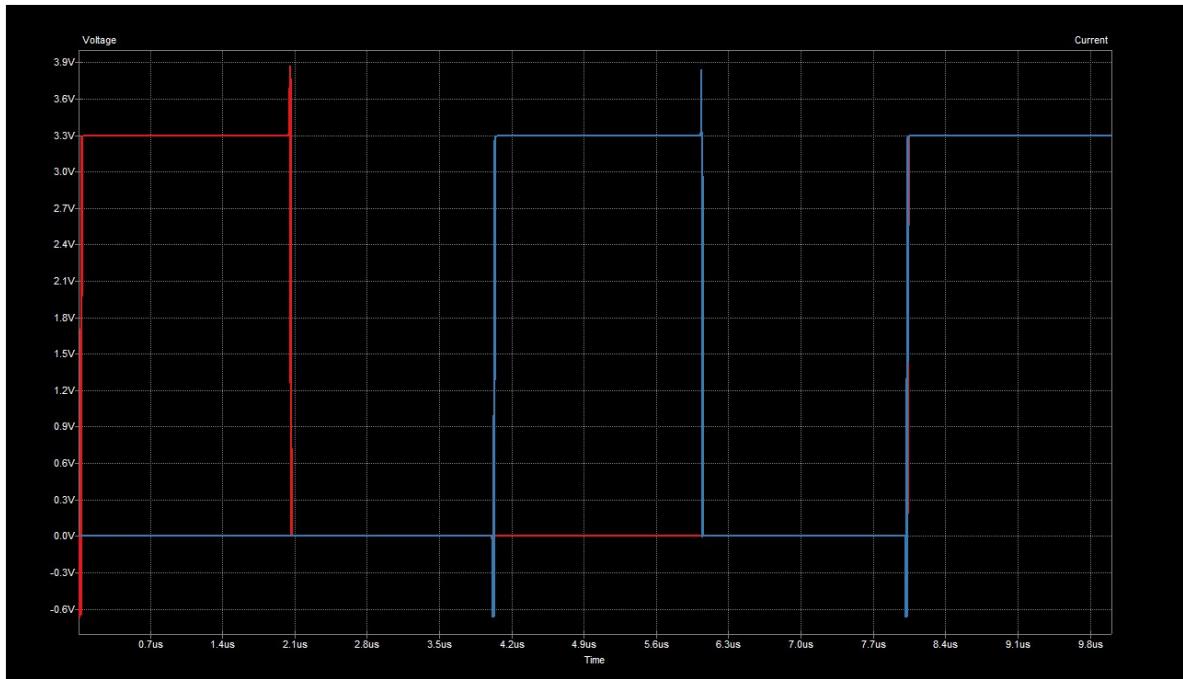
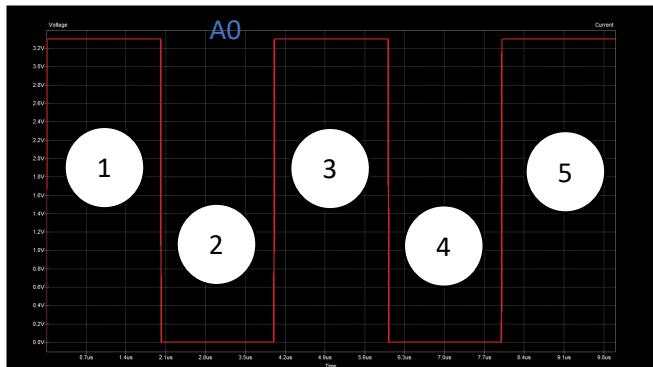


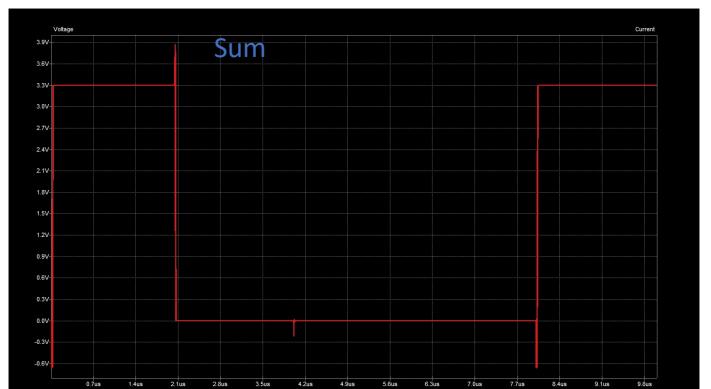
FIGURE 07: OUTPUT SIGNALS OF THE FULL ADDER

Verifying the output

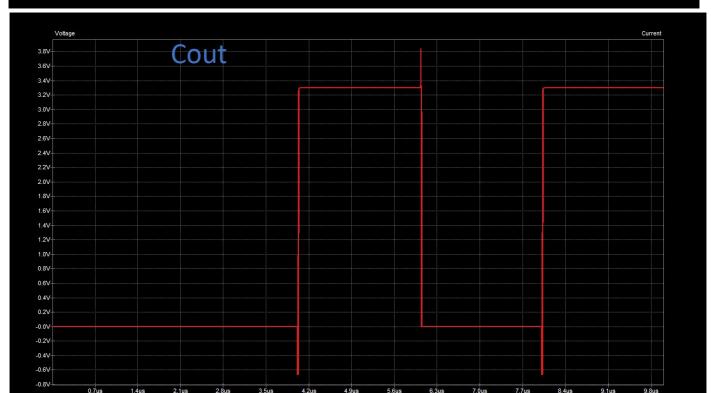
Input Signals



Output Signals



Cout



Results of the simulation for full adder

A ₀	B ₀	C _{in}	Expected Output		Results	
			Sum	C _{out}	Sum	C _{out}
1	0	0	1	0	1	0
0	0	0	0	0	0	0
1	1	0	0	1	0	1
0	0	0	0	0	0	0
1	1	1	1	1	1	1

- According to the input and output waveforms observed in the table, the simulation output aligns precisely with the expected results. Consequently, it can be concluded that the designed 2-bit adder circuit functions correctly.
- Now, the next step is to expand this circuit for a 2-bit adder.

2-bit Adder

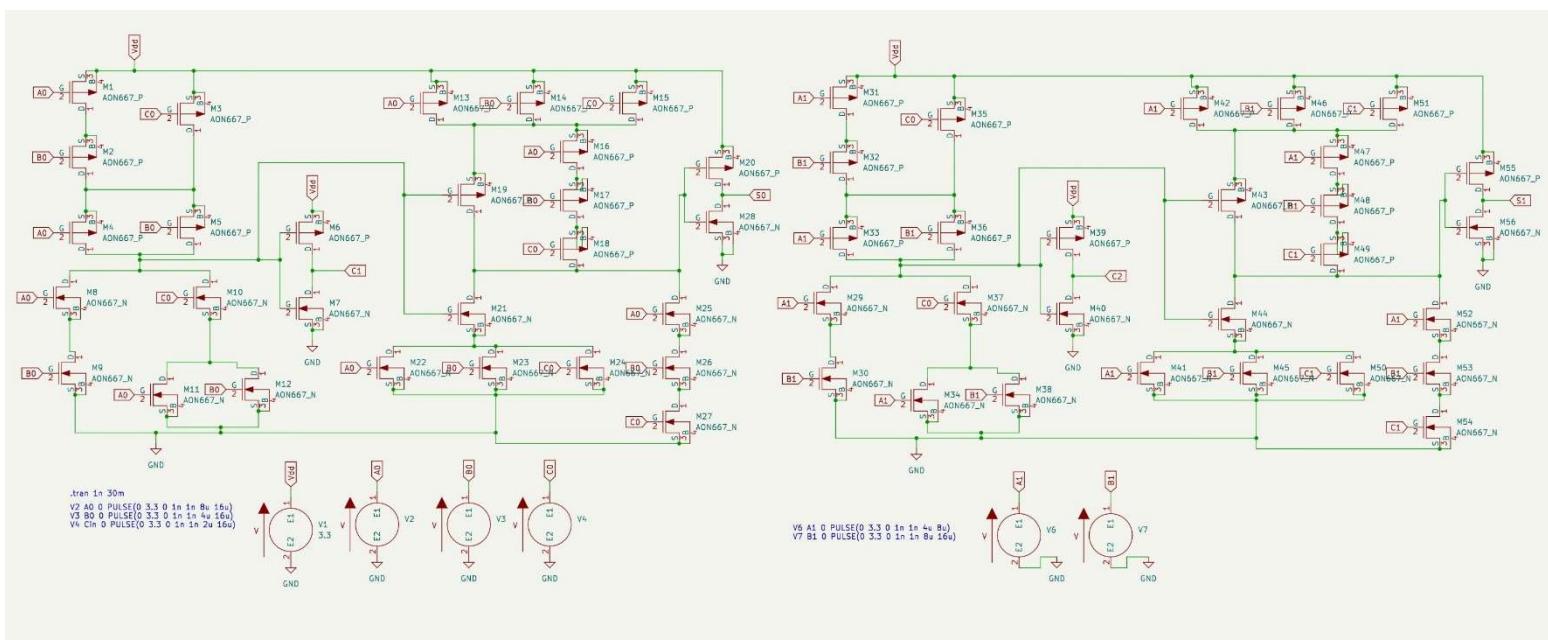


FIGURE 07: SCHEMATIC DIAGRAM OF THE 2 BIT ADDER CIRCUIT

Verifying the output

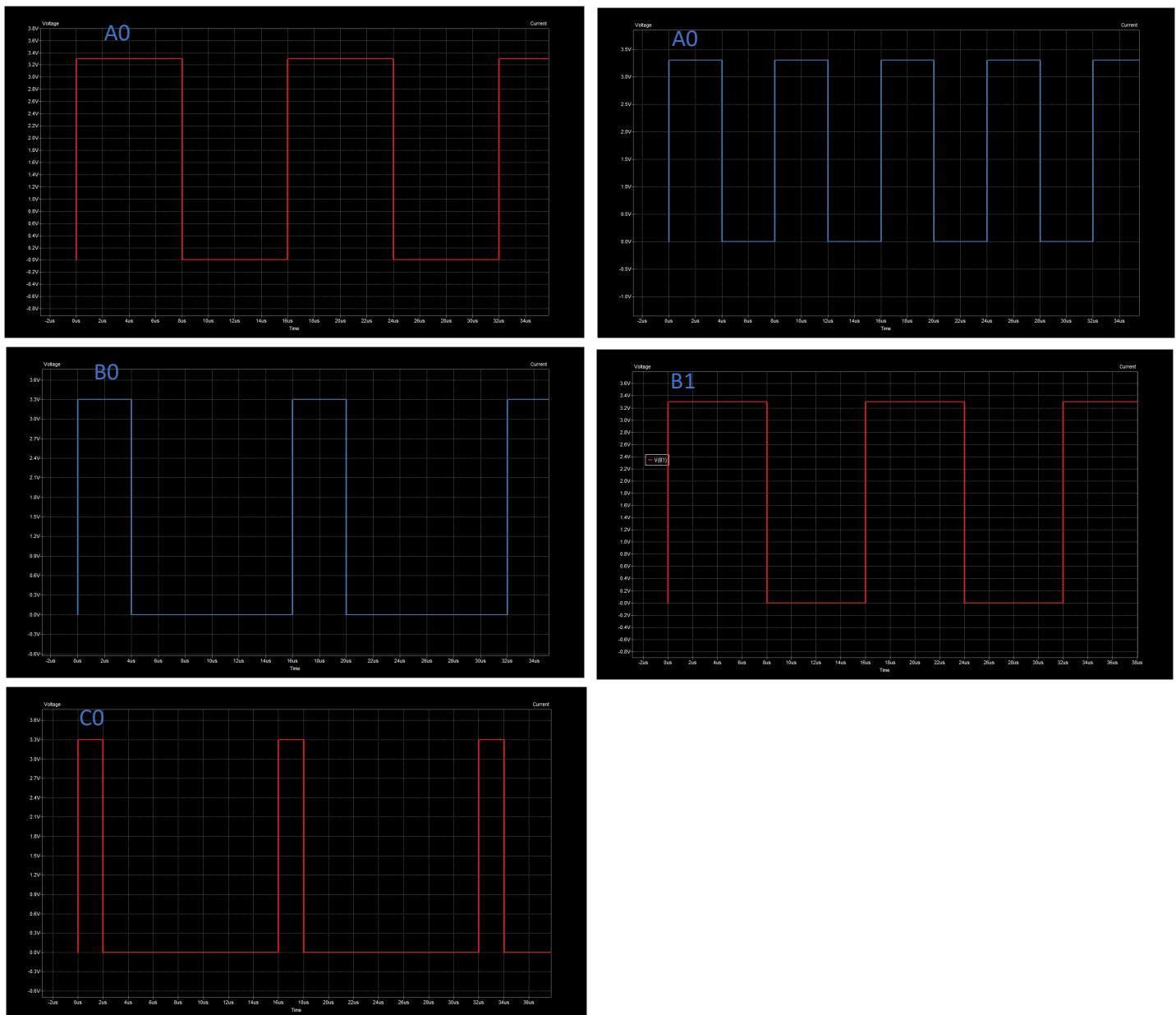
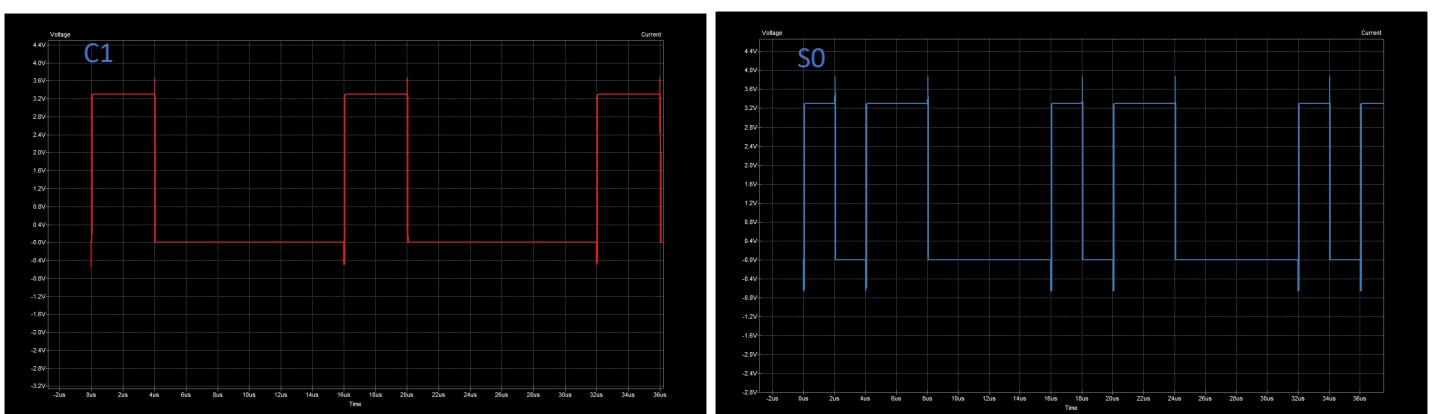


FIGURE 08: INPUT WAVEFORMS TO THE 2 BIT ADDER CIRCUIT



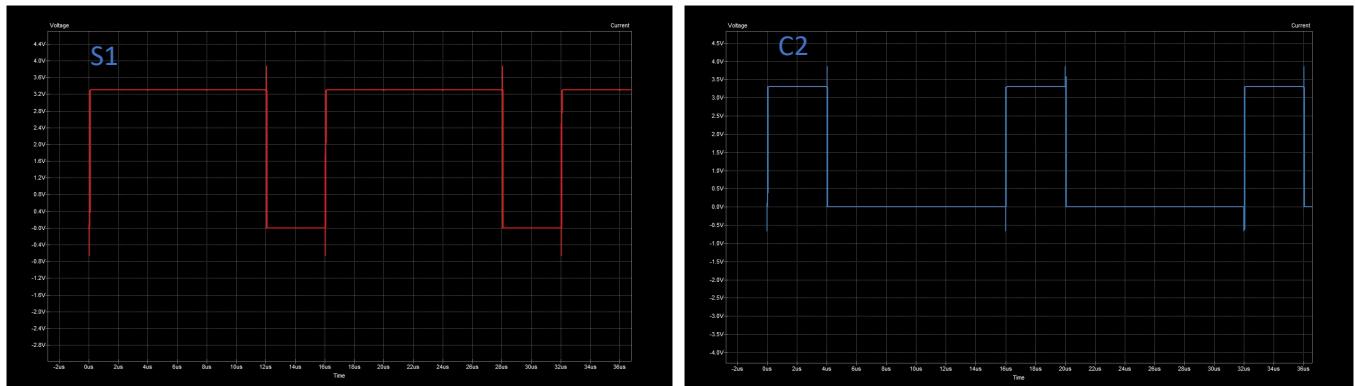


FIGURE 09: OUTPUT WAVEFORMS OF THE 2 BIT ADDER CIRCUIT

Results of the simulation for 2-bit adder

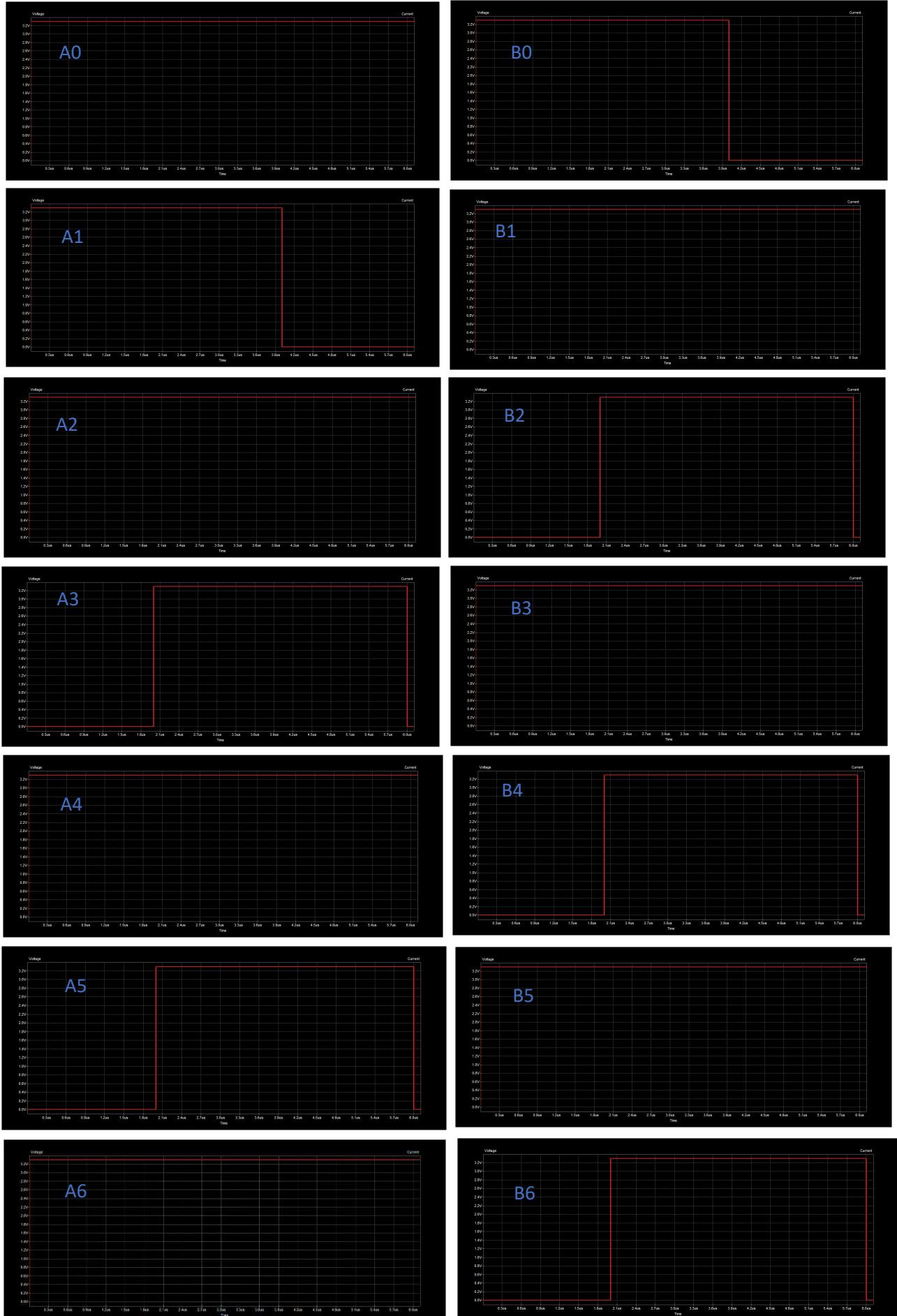
Time (us)	A ₀	B ₀	C ₀	Expected Output		Results	
				S ₀	C ₁	S ₀	C ₁
0-2	1	1	1	1	1	1	1
2-4	1	1	0	0	1	0	1
4-6	1	0	0	1	0	1	0
6-8	1	0	0	1	0	1	0
8-10	0	0	0	0	0	0	0

Time (us)	A ₁	B ₁	C ₁	Expected Output		Results	
				S ₁	C ₂	S ₁	C ₂
0-2	1	1	1	1	1	1	1
2-4	1	1	1	1	1	1	1
4-6	0	1	0	1	0	1	0
6-8	0	1	0	1	0	1	0
8-10	1	0	0	1	0	1	0

- Based on the provided table, it is evident that the expected values and the simulation results align perfectly for the above case. Therefore, it is reasonable to proceed with expanding this circuit to an 8-bit configuration.

8-bit Adder

- Since the schematic diagram for the 8-bit adder is extensive, it is attached as a PDF within the zip file. Let's proceed to verify the output of the 8-bit ripple carry adder.



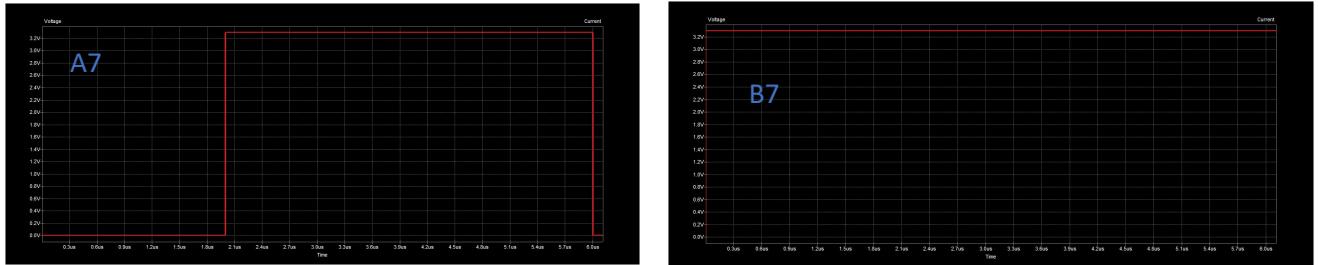
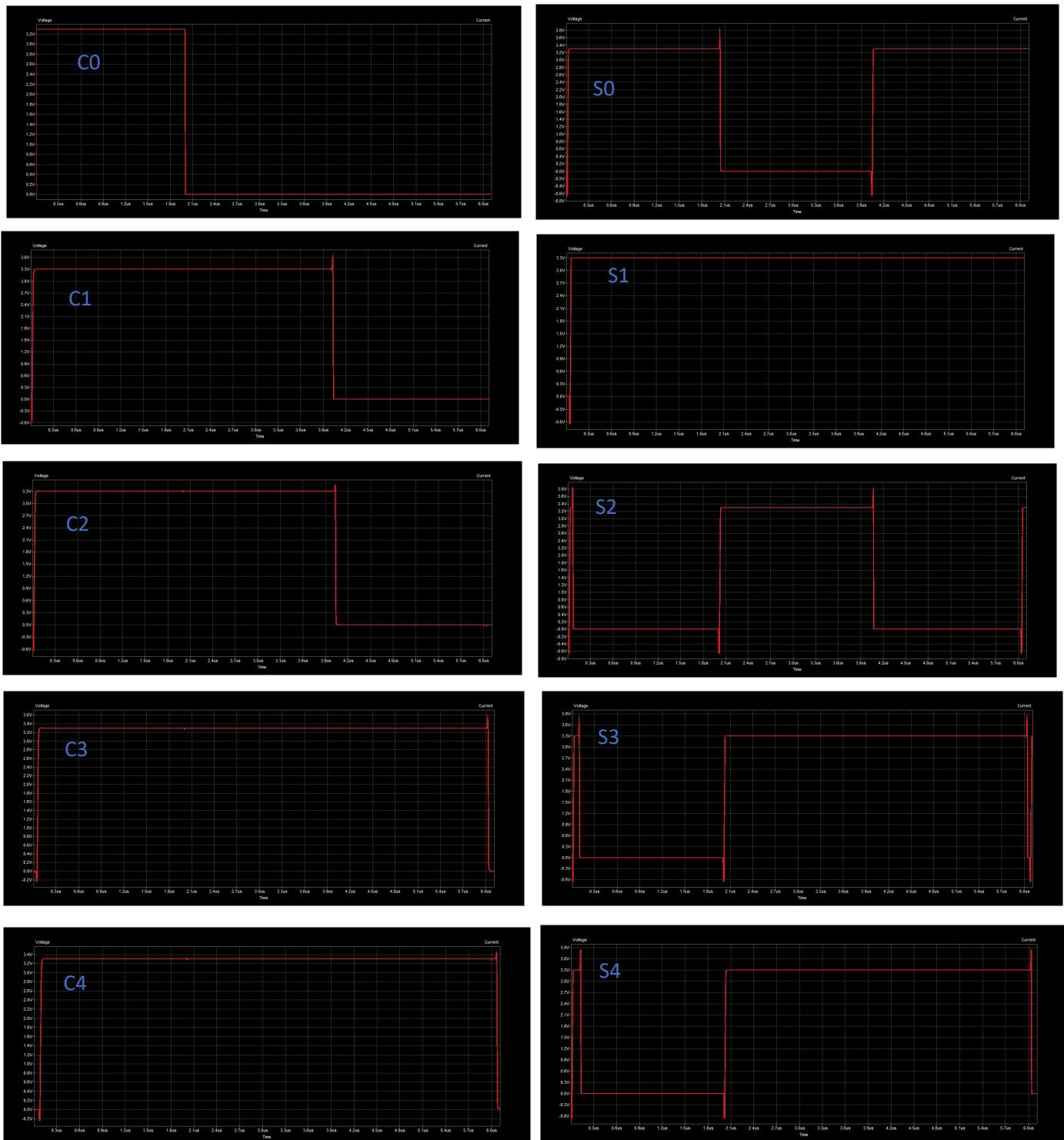


FIGURE 10: INPUT WAVEFORMS TO THE 8 BIT ADDER CIRCUIT



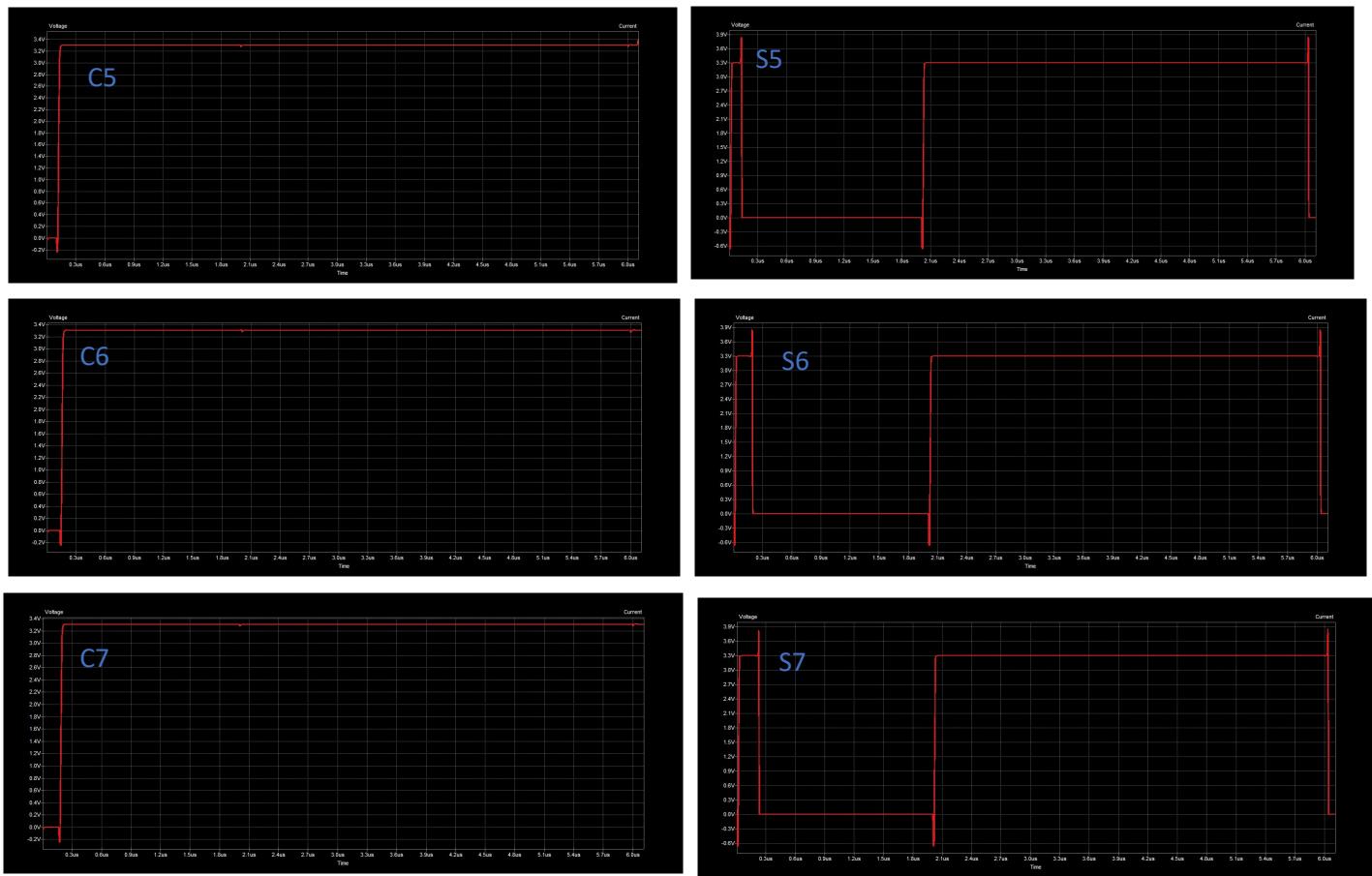


FIGURE 10: INPUT WAVEFORMS OF THE 8 BIT ADDER CIRCUIT

Results of the simulation for 8-bit adder

Time (us)	A ₀	B ₀	C ₀	Expected Output		Results	
				S ₀	C ₁	S ₀	C ₁
0-2	1	1	1	1	1	1	1
2-4	1	1	0	0	1	0	1
4-6	1	0	0	0	0	1	0

Time (us)	A ₁	B ₁	C ₁	Expected Output		Results	
				S ₁	C ₂	S ₁	C ₂
0-2	1	1	1	1	1	1	1
2-4	1	1	1	1	1	1	1
4-6	0	1	0	1	0	1	0

Time (us)	A ₂	B ₂	C ₂	Expected Output		Results	
				S ₂	C ₃	S ₂	C ₃
0-2	1	0	1	0	1	0	1
2-4	1	1	1	1	1	1	1
4-6	1	1	0	0	1	0	1

Time (us)	A ₃	B ₃	C ₃	Expected Output		Results	
				S ₃	C ₄	S ₃	C ₄
0-2	0	1	1	0	1	0	1
2-4	1	1	1	1	1	1	1
4-6	1	1	1	1	1	1	1

Time (us)	A ₄	B ₄	C ₄	Expected Output		Results	
				S ₄	C ₅	S ₄	C ₅
0-2	1	0	1	0	1	0	1
2-4	1	1	1	1	1	1	1
4-6	1	1	1	1	1	1	1

Time (us)	A ₅	B ₅	C ₅	Expected Output		Results	
				S ₅	C ₆	S ₅	C ₆
0-2	0	1	1	0	1	0	1
2-4	1	1	1	1	1	1	1
4-6	1	1	1	1	1	1	1

Time (us)	A ₆	B ₆	C ₆	Expected Output		Results	
				S ₆	C ₇	S ₆	C ₇
0-2	1	0	1	0	1	0	1
2-4	1	1	1	1	1	1	1
4-6	1	1	1	1	1	1	1

Time (us)	A ₇	B ₇	C ₇	Expected Output		Results	
				S ₇	C ₈	S ₇	C ₈
0-2	0	1	1	0	1	0	1
2-4	1	1	1	1	1	1	1
4-6	1	1	1	1	1	1	1

- According to the tables and the output waveforms, it is evident that the expected values align precisely with the resulting values for every considered condition. Consequently, we can conclude that the 8-bit ripple carry adder is functioning properly.
- Similarly, we can connect 32 full adders to create the 32-bit ripple carry adder.