University of North Texas
Department of Computer Science and Engineering

Exam I (60 minutes)

CSCE5610 Computer System Architecture (Fall 2024)

Version II

Name: _____ Student ID: _____

Instructions: No cell phones are permitted for any reason! The examination consists of 8 pages, and the total of all questions is 100 points. Read all the questions and their values before you start answering. Please answer as many questions as you can in the time allowed.

Q1 Multi-Choice Questions (15pts)		
Q2 Concept (15pts)		
Q3 Calculation Question (80pts)	1(30pts)	
	2(20pts)	
	3(20pts)	
Total (100pts)		

Question 1 [15 points]. Multi-Choice, Multi-Answer Questions

Put your answers in the following table. You don't need to justify your choice.

Question	1	2	3	4	5
Answer:	AB	D	D	A	T

[3pts/each]

1) Which of the following operations require three register operands in MIPS? [select all that apply]
   A. add
   B. sub
   C. lw
   D. sw

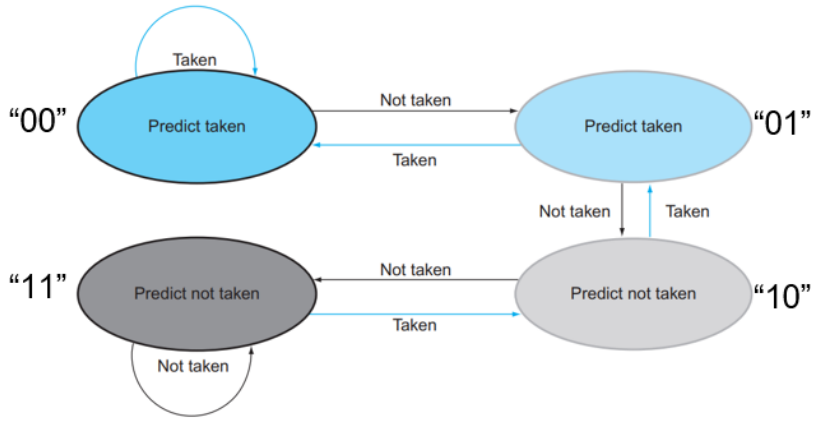
2) If the processor has 32 registers, what is the bit width of the register address?
   A. 2
   B. 4
   C. 3
   D. 5

3) Sometimes, we can replace multiplication and division instructions with more efficient shift operations. Given the division instruction below,

   divi $t0, $t0, 4

   which of the following shift operations performs the same function as the given division operation?
   A. sll $t0, $t0, 4
   B. sll $t0, $t0, 2
   C. srl $t0, $t0, 4
   D. srl $t0, $t0, 2

4) Below is a 2-bit Dynamic Branch Prediction Scheme:



Given: Consider a loop that **branches nine times** in a row and then **is not taken once**.

What is the prediction accuracy for **ten consecutive predictions** using the 2-bit prediction

scheme with an initial state of '**10**'?

A. 80%
B. 87.5%
C. 62.5%
D. 70%

5) (True/False) Given the program below:

lw $t2, 0($a0)
add $t1, $t0, $t2
addi $t3, $t4, 2

To avoid the pipeline stall, we can reorder the execution of the instructions to:

lw $t2, 0($a0)
addi $t3, $t4, 2
add $t1, $t0, $t2

Question 2 [15 points]. Concept Questions

1. List the **R-type MIPS instruction** formats with an instruction example. Clearly show the fields and the number of bits in format. [Hint: 32 bits machine code divides into different fields]

Answer:

R-type instruction: add $4, $5, $6 (1 point)

opcode (6 bits)	rs(5 bits)	rt(5 bits)	rd(5bits)	shamt(5 bits)	func(6 bits)

(4 point)

2. Briefly define the following term:

spatial locality

Answer: The principle of spatial locality says that if a program accesses one memory address, there is a good chance that it will also access other nearby addresses. (5pts)

3. Provide two instructions that illustrate a **Write-After-Read (WAR)** data hazard.

Answer (5pts): [answer not unique, as long as the 1st instruction read from a register that the 2nd instruction write to, it is correct.]

add $t2, $t1, $t3

sub $t1, $t4, $a0

Question 3 [70 points]. Calculation question

1. Consider a system with the following processor components and policies:

- A direct-mapped L1 data cache of size 64 bytes and block size of 4 bytes, indexed and tagged using physical addresses
- A 4-way associative data Translation lookaside buffer (TLB) with 16 page table entries
- Physical addresses of 32 bits, and virtual addresses of 40 bits
- Byte addressable memory
- Page size of 1MB (1024*1024 bytes)

1). Perform the physical memory address field encoding, given the 32-bit physical memory address, how many bits are used for the tag?

Answer: 26 bits (10pts)

2). Given the 40-bit virtual address, how many bits are used for the page offset?

Answer: 1MB=2^20bytes, so 20 bits are used for page offset. (10pts)

3). In the Translation lookaside buffer (TLB), calculate the total numbers of bits used for tag field?

Answer: 18 bit/entry*16 entries= 288 bits (10pts)

2. [30pts] The below table shows three processors P1, P2, and P3 running programs with instructions and clock rates as shown below. Answer the following.

Processor	Clock rate	Clock Cycles	Instructions
P1 running Program 1	2GHz	2000	1000
P2 running Program 2	3.0GHz	7000	3500
P3 running Program 3	10GHz	5500	3000

a. [10 points] Calculate the CPU time of each program. Which program has the lowest CPU time?
b. [10 points] What is the average CPI for each of the program running on processors P1, P2, and P3?

Answer:

a. $CPU\ time_{P1,program1} = \frac{Clock\ Cycles}{Clock\ Rate} = \frac{2000}{2} = 1000ns$ (3 points)

$CPU\ time_{P2,program2} = \frac{Clock\ Cycles}{Clock\ Rate} = \frac{7000}{3} = 2333.3ns$ (3 points)

$CPU\ time_{P3,program3} = \frac{Clock\ Cycles}{Clock\ Rate} = \frac{5500}{10} = 550ns$ (3 points)

Program 3 has the lowest CPU time. (1pts)

b. $CPI_{Program1} = \frac{Clock\ Cycles}{Instruction\ Count} = \frac{2000}{1000} = 2$ (4 points)

$CPI_{Program2} = \frac{Clock\ Cycles}{Instruction\ Count} = \frac{7000}{3500} = 2$ (3 points)

$CPI_{Program3} = \frac{Clock\ Cycles}{Instruction\ Count} = \frac{5500}{3000} = 1.8$ (3 points)

3. [20 points]. Given the code below:

```
          li   $4,  1000
Ostrich:  subi $4,  $4, 1
          bne  $4,  $0, Ostrich
```

1). [8 points] How many static instructions in the program? How many dynamic instructions in the program?

2). [12 points] Assume that we have Processor 1 with 500MHz clock rate and CPI 1.2 to run this program. Processor 2 with a clock rate 1GHz and CPI 2 to run the same program. Calculate the CPU time for processor 1 and processor 2 respectively.

Answer:

1). Static instructions: 3 (4 point)

Dynamic instructions: 2001(4 point)

2). $CPU\ time_{P1} = \frac{clock\ cycles}{clock\ rate} = \frac{Instruction\ count * CPI}{clock\ rate} = \frac{2001*1.2}{500*10^6} = 4.8 * 10^{-6}s$ (6 points)

$CPU\ time_{P2} = \frac{clock\ cycles}{clock\ rate} = \frac{Instruction\ count * CPI}{clock\ rate} = \frac{2001*2}{1*10^9} = 4.002 * 10^{-6}s$(6 points)