University of North Texas
Department of Computer Science and Engineering

Exam I (60 minutes)

CSCE5610 Computer System Architecture (Fall 2024)

Version III

Name: _____ Student ID: _____

Instructions: No cell phones are permitted for any reason! The examination consists of 8 pages, and the total of all questions is 100 points. Read all the questions and their values before you start answering. Please answer as many questions as you can in the time allowed.

Q1 Multi-Choice Questions (15pts)		
Q2 Concept (15pts)		
Q3 Calculation Question (80pts)	1(30pts)	
	2(20pts)	
	3(20pts)	
Total (100pts)		

Question 1 [10 points]. Multi-Choice, Multi-Answer Questions

Put your answers in the following table. You don't need to justify your choice.

Question	1	2	3	4	5
Answer:	F	C	A	B	T

[3pts/each]

1) (True/False) Shift operations (sll, srl) are I-type instructions.

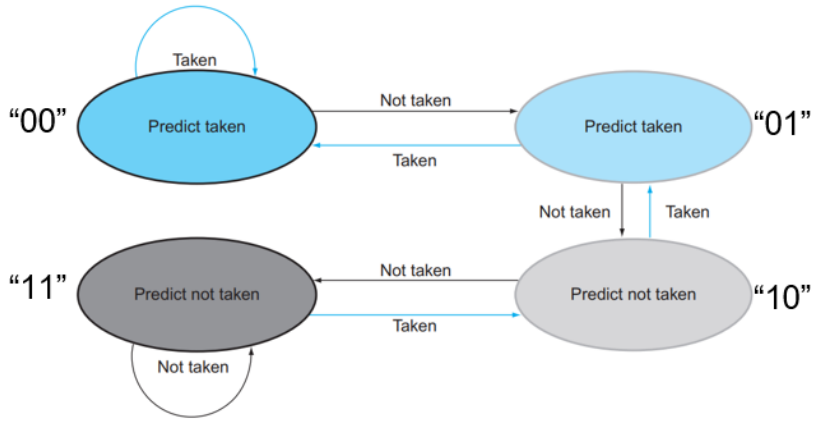
2) If the processor has 8 registers, what is the bit width of the register address?
   A. 2
   B. 4
   C. 3
   D. 5

3) Sometimes, we can replace multiplication and division instructions with more efficient shift operations. Given the multiplication instruction below,

   muli $t0, $t0, 8

   which of the following shift operations performs the same function as the given multiplication operation?
   A. sll $t0, $t0, 3
   B. sll $t0, $t0, 8
   C. srl $t0, $t0, 3
   D. srl $t0, $t0, 8

4) Below is a 2-bit Dynamic Branch Prediction Scheme:



Given: Consider a loop that **branches nine times** in a row and then **is not taken once**.

What is the prediction accuracy for **ten consecutive predictions** using the 2-bit prediction scheme with an initial state of '**01**'?
   A. 80%
   B. 90%
   C. 62.5%
   D. 70%

5) (True/False) Given the program below:

```
lw $t2, 0($a0)
add $t1, $t0, $t2
addi $t3, $t4, 2
```

To avoid the pipeline stall, we can reorder the execution of the instructions to:

```
lw $t2, 0($a0)
addi $t3, $t4, 2
add $t1, $t0, $t2
```

Question 2 [15 points]. Concept Questions

1. List the **J-type MIPS instruction** formats with an instruction example. Clearly show the fields and the number of bits in format. [Hint: 32 bits machine code divides into different fields]

Answer:

J-type: j L(0.5 points)

opcode (6bits)	addr. (26bits)

(4 points)

2. Briefly define the following term:

Cache hit

Answer: A **cache hit** occurs if the cache contains the data that we're looking for. (5 pts)

3. Provide two instructions that illustrate a **Read-After-Read (RAW)** data hazard.

Answer (5pts): [answer not unique, as long as the 2nd instruction read from a register that the 1st instruction write to, it is correct.]

add $t2, $t1, $t3

sub $t4, $t2, $a0

Question 3 [70 points]. Calculation question

1. [30pts] Consider a system with the following processor components and policies:

- A direct-mapped L1 data cache of size 64 bytes and block size of 1 word and word size of 4 bytes, indexed and tagged using physical addresses
- A 4-way associative data Translation lookaside buffer (TLB) with 16 page table entries
- Physical addresses of 32 bits, and virtual addresses of 40 bits
- Byte addressable memory
- Page size of 1MB (1024*1024 bytes)

1). In the direct-mapped L1 cache, calculate the total number of bits for tag field.

Answer: 26 bits/block*16 blocks=416 bits (10pts)

2). How many bits are used for the PPN (physical page number)?

Answer: 12 bits are used for PPN. (10pts)

3). Calculate the number of sets in the Translation lookaside buffer (TLB)?

Answer: 4 sets (10pts)

2. [20pts] The below table shows three processors P1, P2, and P3 running programs with instructions and clock rates as shown below. Answer the following.

Processor	Clock rate	Clock Cycles	Instructions
P1 running Program 1	1.0GHz	2000	1050
P2 running Program 2	3.0GHz	7000	2000
P3 running Program 3	2.5GHz	5500	3000

a. [10 points] Calculate the CPU time of each program. Which program has the lowest CPU time?
b. [10 points] What is the average CPI for each of the program running on processors P1, P2, and P3?

Answer:

a. $CPU\ time_{P1,program1} = \frac{Clock\ Cycles}{Clock\ Rate} = \frac{2000}{1} = 2000ns$ (3 points)

$CPU\ time_{P2,program2} = \frac{Clock\ Cycles}{Clock\ Rate} = \frac{7000}{3} = 2333.3ns$ (3 points)

$CPU\ time_{P3,program3} = \frac{Clock\ Cycles}{Clock\ Rate} = \frac{5500}{2.5} = 2200ns$ (3 points)

Program 1 has the lowest CPU time. (1pts)

b. $CPI_{Program1} = \frac{Clock\ Cycles}{Instruction\ Count} = \frac{2000}{1050} = 1.9$ (4 points)

$CPI_{Program2} = \frac{Clock\ Cycles}{Instruction\ Count} = \frac{7000}{2000} = 3.5$ (3 points)

$CPI_{Program3} = \frac{Clock\ Cycles}{Instruction\ Count} = \frac{5500}{3000} = 1.8$ (3 points)

3. [20 points]. Given the code below:

```
          li   $4,  1000
Ostrich:  subi $4,  $4, 1
          bne  $4,  $0, Ostrich
```

1). [8 points] How many static instructions in the program? How many dynamic instructions in the program?

2). [12 points] Assume that we have Processor 1 with 800MHz clock rate and CPI 1.2 to run this program. Processor 2 with a clock rate 1GHz and CPI 1.5 to run the same program. Calculate the CPU time for processor 1 and processor 2 respectively.

Answer:

1). Static instructions: 3 (4 point)

Dynamic instructions: 2001(4 point)

2). $CPU\ time_{P1} = \frac{clock\ cycles}{clock\ rate} = \frac{Instruction\ count * CPI}{clock\ rate} = \frac{2001*1.2}{800*10^6} = 3.0015 * 10^{-6}s$ (6 points)

$CPU\ time_{P2} = \frac{clock\ cycles}{clock\ rate} = \frac{Instruction\ count * CPI}{clock\ rate} = \frac{2001*1.5}{1*10^9} = 3.0015 * 10^{-6}s$ (6 points)