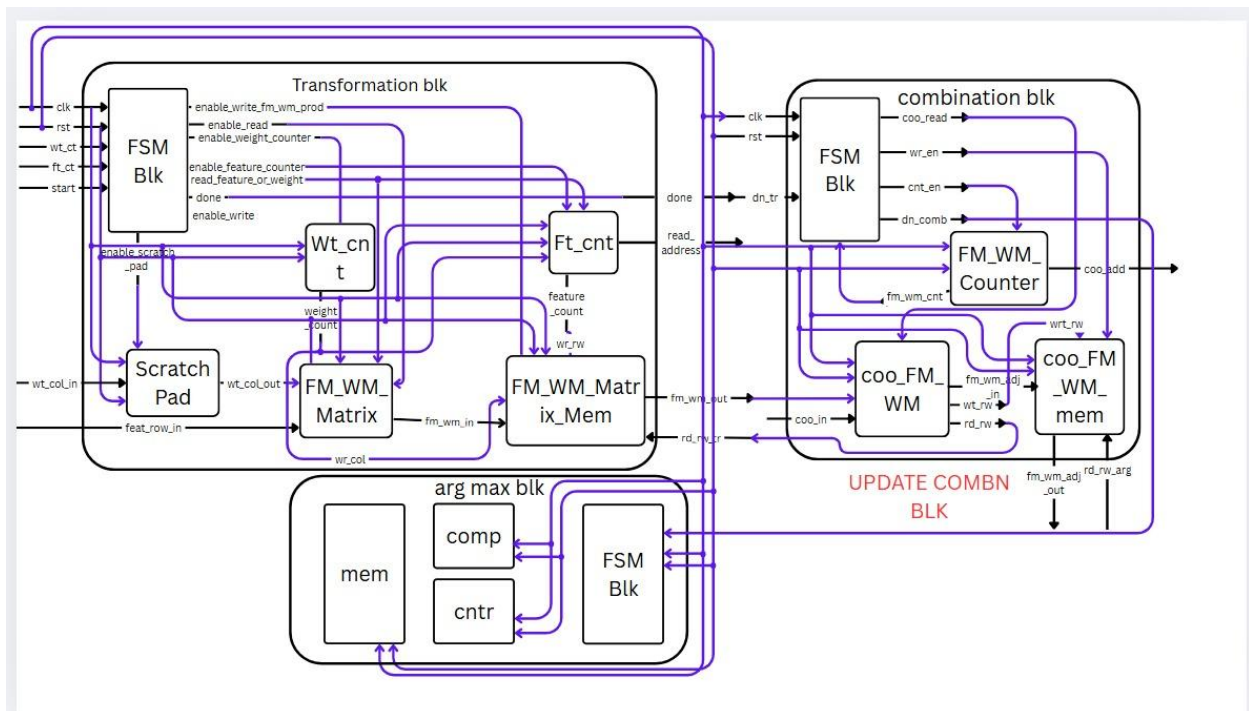
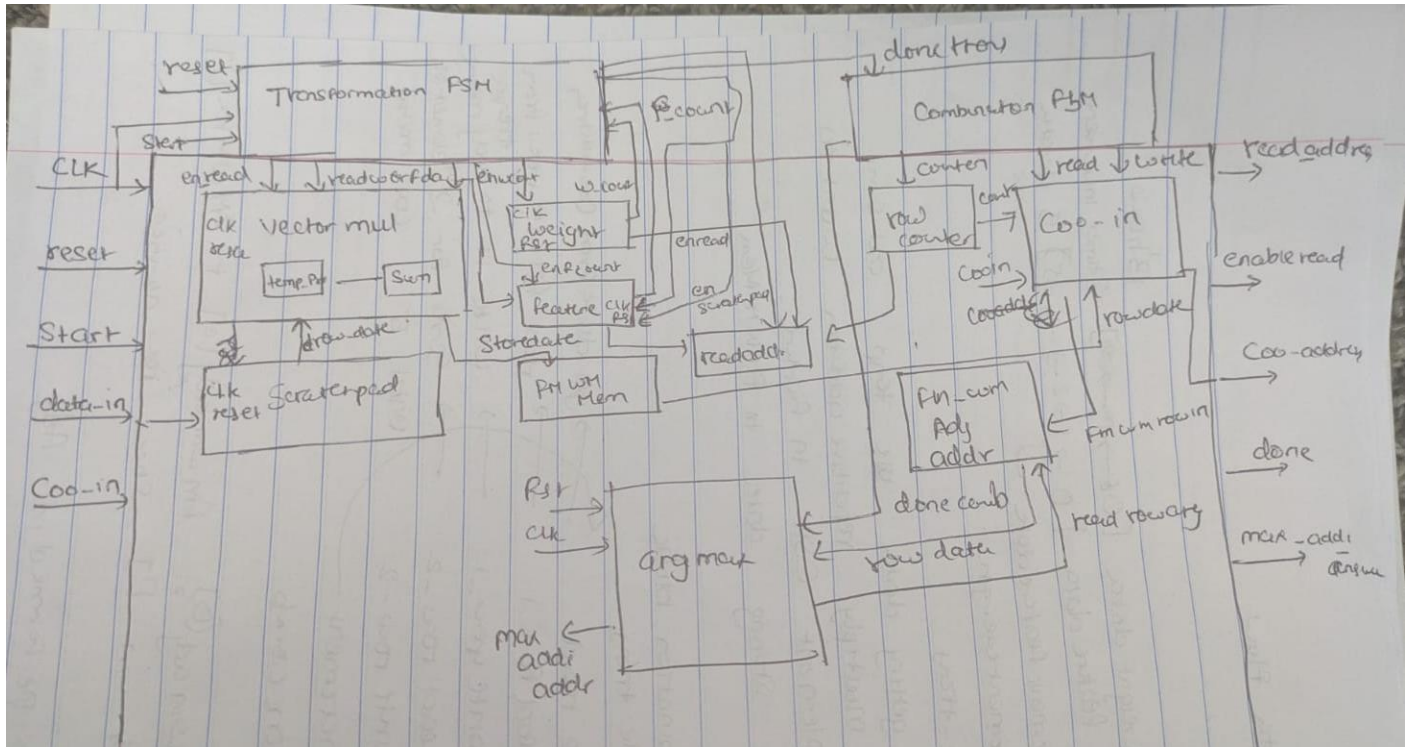


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Data Flow

Start

13'h0000

Read weight data [06 → 10 → 14] 3 times increment

Read Feature data [0 → 1 → 2 → 3 → 4 → 5] 5 iterations

Increment Feature data

Increment weight

Done - tray

While getting data use temp and sum
to multiply repetitive addition want to
implement CSA in future

Keep storing data to F1 W1 Mem

Combination block

done tray

Coo read

Read Row - 1

write row - 1

Read row - 2

write row - 2

Increment

Done comb

get data from Coo-address
read F1 W1 row from
tray
write it to adj mem
same for 2nd element
until 5 Coo - matrix

logic

$$F1W1adj[0] = F1W1adj[0] + F1W1row[i]$$

Boxes in [i] show row number

Addition performed in Adj

1. Transformation Block

The Transformation_Block performs matrix-vector multiplication between features and weights. It includes submodules: Vector_Multiplier, Weight_Counter, Feature_Counter, Scratch_Pad, Matrix_FM_WM_Memory, and Transformation_FSM.

- Feature and weight vectors are stored in local scratchpads.
- Counters select feature rows and weight columns.
- The Vector_Multiplier performs parallel dot-products (WEIGHT_COLS = 3 parallel multipliers).
- Results are stored in Matrix_FM_WM_Memory.
- Transformation_FSM controls read, multiply, and write sequences.

2. Combination Block

The Combination_Block aggregates transformed features based on sparse graph connections (COO format).

It includes coo_in, ROW_Counter, Matrix_FM_WM_ADJ_Memory, and Combination_FSM.

- coo_in provides source-target node pairs.
- ROW_Counter iterates over edges.
- Features are accumulated selectively according to graph edges.
- Sparse aggregation is handled efficiently to reduce unnecessary operations.
- Combination_FSM manages control flow and signals completion.

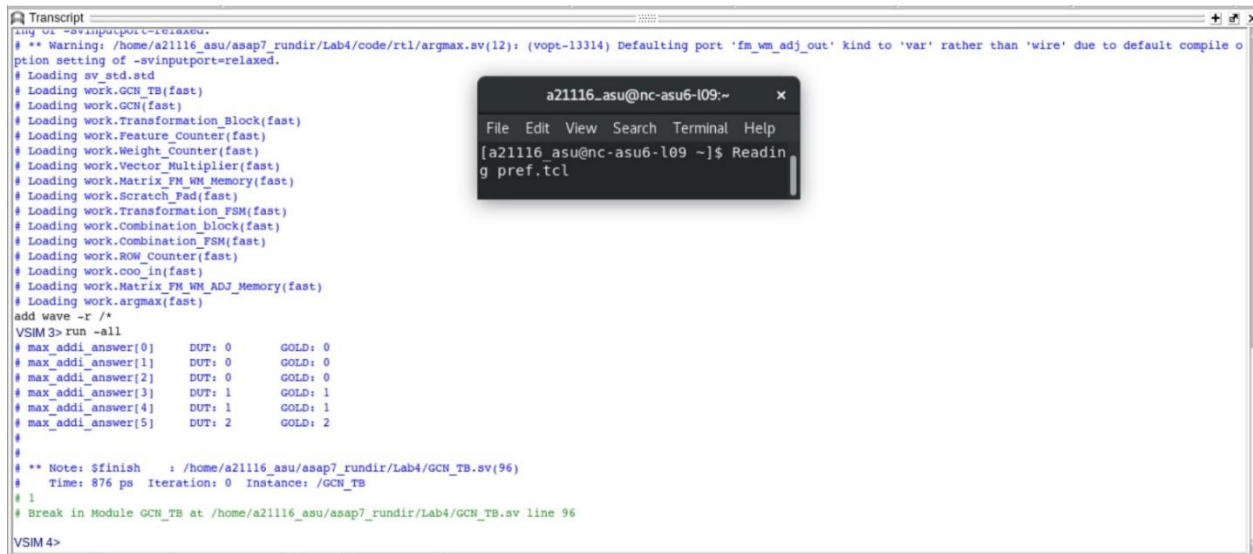
3. Argmax Block

The argmax module selects the maximum feature per node after aggregation.

- Accepts aggregated feature vectors.
- Uses compare-and-select logic to find the maximum value per node.
- Stores maximum indices in max_addi_answer.
- Internal FSM controls idle, compare, and output states.
- Triggered after done_comb from Combination Block.

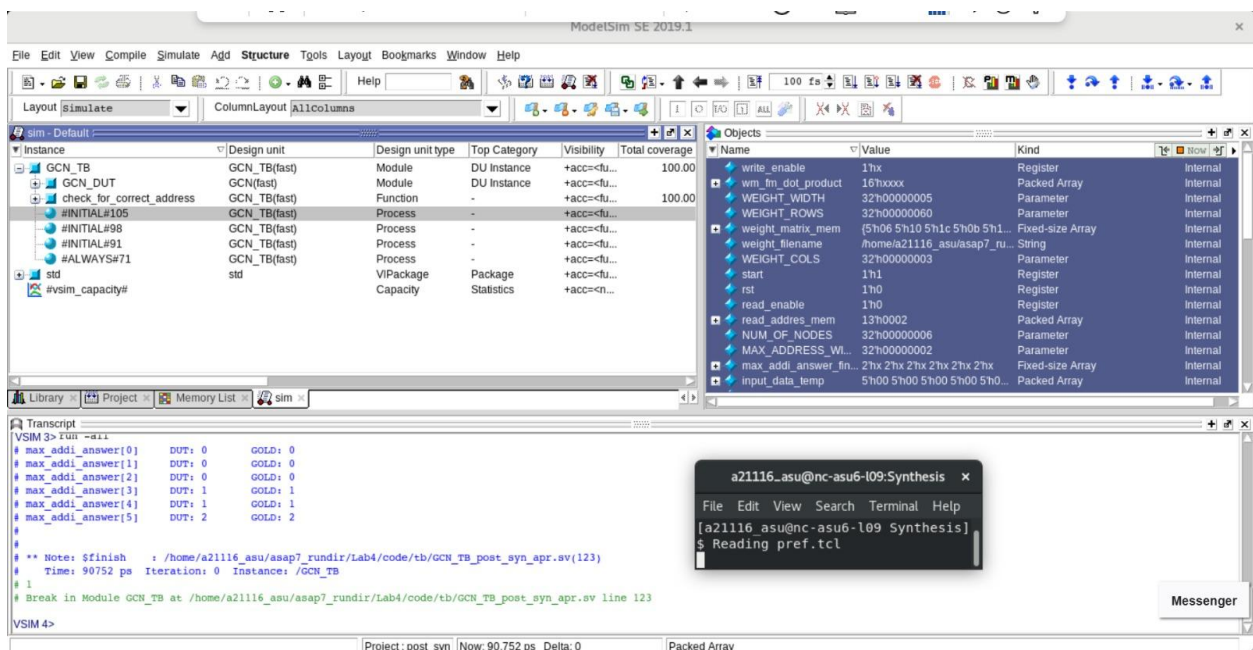
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Behavioral Verilog Netlist output



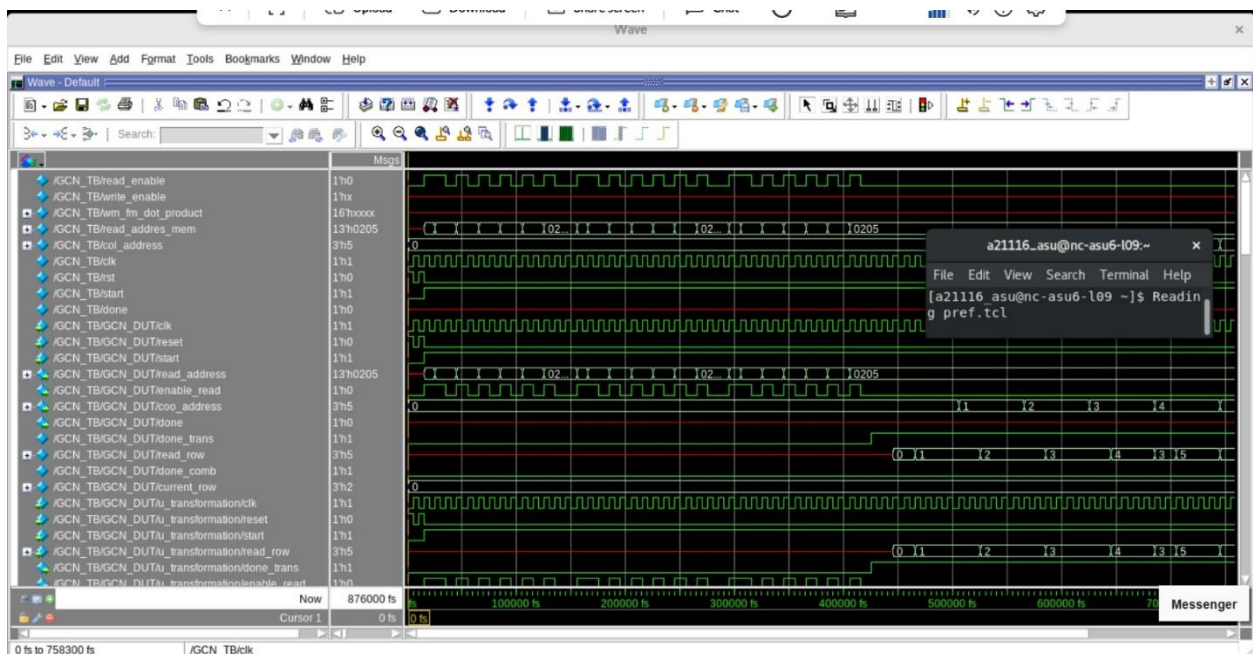
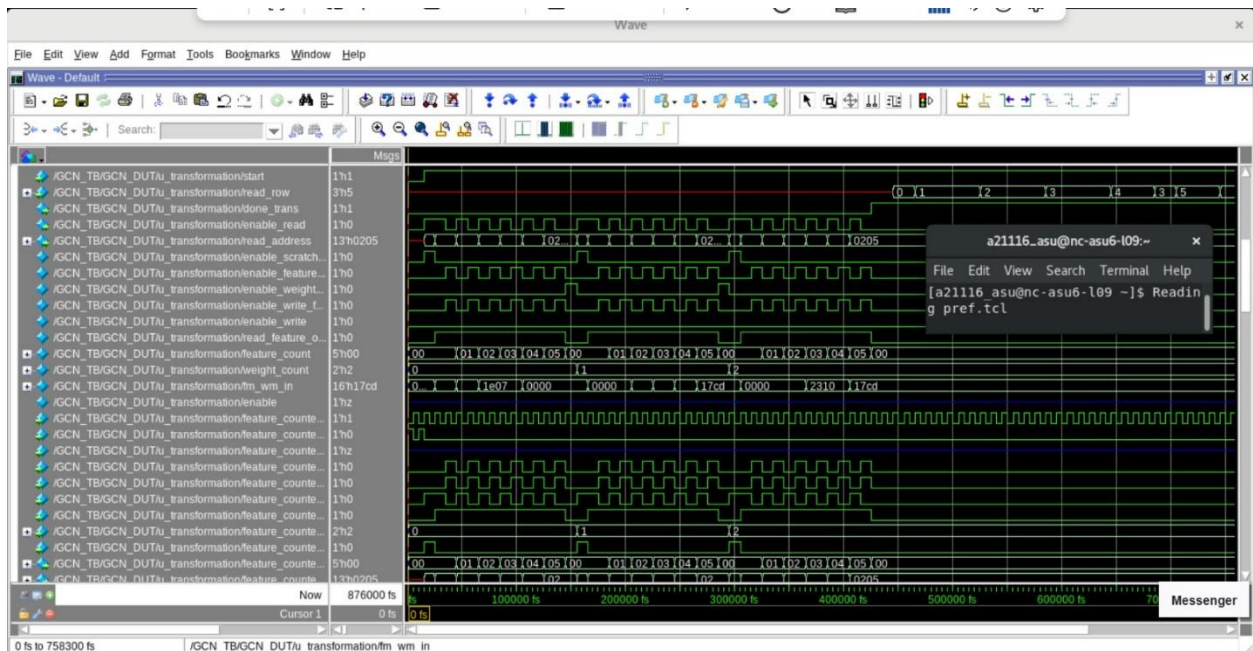
```
Transcript
a21116_asu@nc-asu6-109:~$ vlog -sv -inputport=relaxed.
# ** Warning: /home/a21116_asu/asap7_rundir/Lab4/code/rtl/argmax.sv(12): (vopt-13314) Defaulting port 'fm_adj_out' kind to 'var' rather than 'wire' due to default compile option setting of -svinputport=relaxed.
# Loading sv_std.std
# Loading work.GCN_TB(fast)
# Loading work.GCN(fast)
# Loading work.Transformation_Block(fast)
# Loading work.Feature_Counter(fast)
# Loading work.Weight_Counter(fast)
# Loading work.Vector_Multiplier(fast)
# Loading work.Matrix_FM_WM_Memory(fast)
# Loading work.Scratch_Pad(fast)
# Loading work.Transformation_FSM(fast)
# Loading work.Combination_Block(fast)
# Loading work.Combination_FSM(fast)
# Loading work.ROW_Counter(fast)
# Loading work.coo_in(fast)
# Loading work.Matrix_FM_WM_ADJ_Memory(fast)
# Loading work.argmax(fast)
add wave -r /*
VSIM3> run -all
# max_addi_answer[0] DUT: 0 GOLD: 0
# max_addi_answer[1] DUT: 0 GOLD: 0
# max_addi_answer[2] DUT: 0 GOLD: 0
# max_addi_answer[3] DUT: 1 GOLD: 1
# max_addi_answer[4] DUT: 1 GOLD: 1
# max_addi_answer[5] DUT: 2 GOLD: 2
#
# ** Note: $finish : /home/a21116_asu/asap7_rundir/Lab4/GCN_TB.sv(96)
# Time: 876 ps Iteration: 0 Instance: /GCN_TB
# 1
# Break in Module GCN_TB at /home/a21116_asu/asap7_rundir/Lab4/GCN_TB.sv line 96
VSIM4>
```

Synthesized Verilog Netlist output

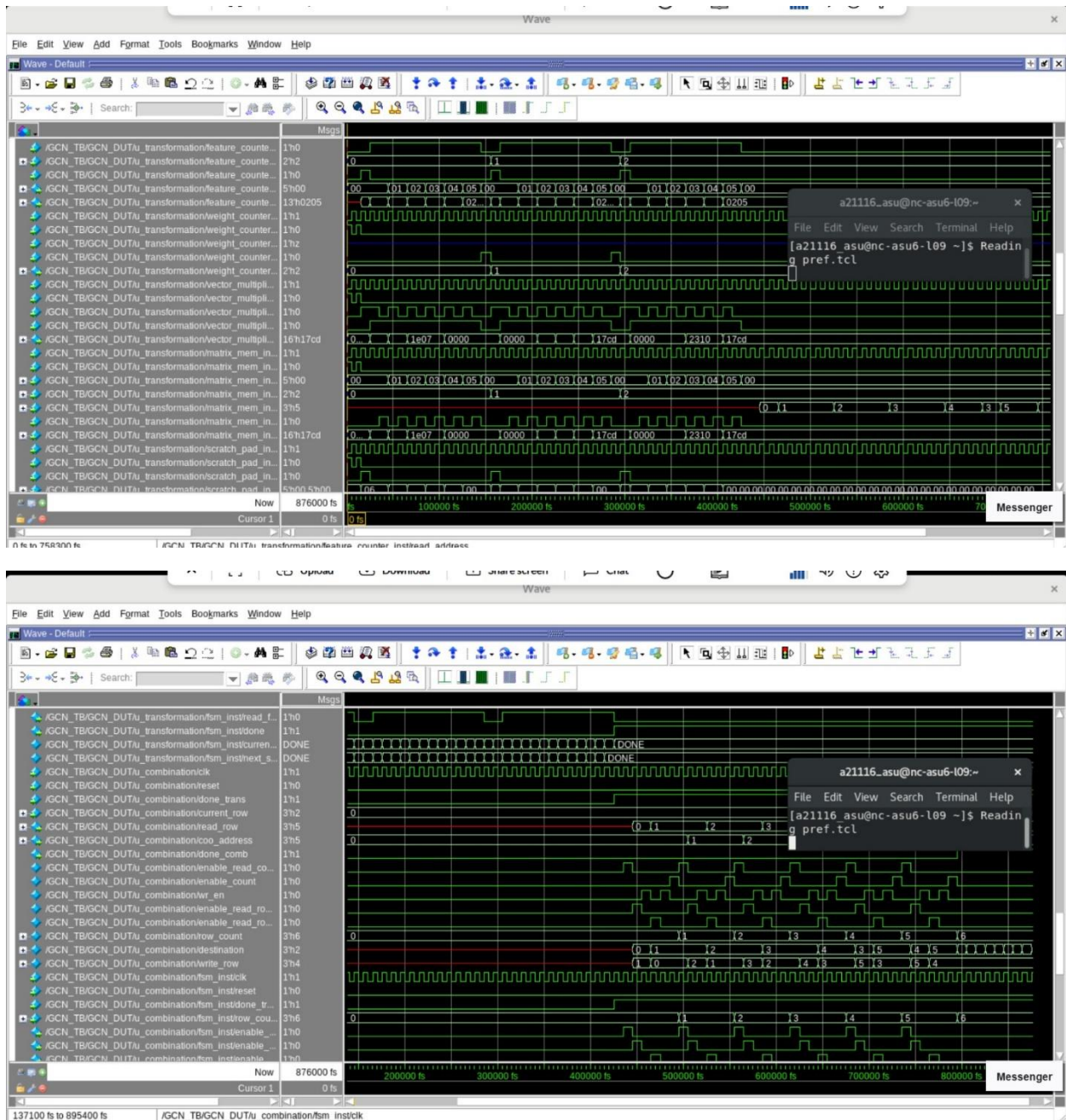


```
ModelSim SE 2019.1
File Edit View Compile Simulate Add Structure Tools Layout Bookmarks Window Help
Layout Simulate ColumnLayout AllColumns
sim - Default
Instance Design unit Design unit type Top Category Visibility Total coverage
GCN_TB GCN_TB(fast) Module DU Instance +acc=clu... 100.00
GCN_DUT GCN(fast) Module DU Instance +acc=clu... 100.00
check_for_correct_address GCN_TB(fast) Function - +acc=clu... 100.00
INITIAL#105 GCN_TB(fast) Process - +acc=clu... 100.00
INITIAL#98 GCN_TB(fast) Process - +acc=clu... 100.00
INITIAL#91 GCN_TB(fast) Process - +acc=clu... 100.00
ALWAYS#71 GCN_TB(fast) Process - +acc=clu... 100.00
std std VPackage Package +acc=clu... 100.00
sim_capacity# Capacity Statistics +acc=clu... 100.00
Objects
Name Value Kind
write_enable 1'hx Register Internal
wm_fm_dot_product 16'hxxxx Packed Array Internal
WEIGHT_WIDTH 32'h00000005 Parameter Internal
WEIGHT_ROWS 32'h00000060 Parameter Internal
weight_matrix_mem {5'h06 5'h10 5'h1c 5'h0b 5'h1... Fixed-size Array Internal
weight_filename /home/a21116_asu/asap7_nu... String Internal
WEIGHT_COLS 32'h00000003 Parameter Internal
start 1'h1 Register Internal
rst 1'h0 Register Internal
read_enable 1'h0 Register Internal
read_address_mem 13'h0002 Packed Array Internal
NUM_OF_NODES 32'h00000006 Parameter Internal
MAX_ADDRESS_WL... 32'h00000002 Parameter Internal
max_addi_answer_fin... 2'hx 2'hx 2'hx 2'hx 2'hx Fixed-size Array Internal
input_data_temp 5'h00 5'h00 5'h00 5'h00 5'h0... Packed Array Internal
Transcript
VSIM3> run -all
# max_addi_answer[0] DUT: 0 GOLD: 0
# max_addi_answer[1] DUT: 0 GOLD: 0
# max_addi_answer[2] DUT: 0 GOLD: 0
# max_addi_answer[3] DUT: 1 GOLD: 1
# max_addi_answer[4] DUT: 1 GOLD: 1
# max_addi_answer[5] DUT: 2 GOLD: 2
#
# ** Note: $finish : /home/a21116_asu/asap7_rundir/Lab4/code/tb/GCN_TB_post_syn_apr.sv(123)
# Time: 90752 ps Iteration: 0 Instance: /GCN_TB
# 1
# Break in Module GCN_TB at /home/a21116_asu/asap7_rundir/Lab4/code/tb/GCN_TB_post_syn_apr.sv line 123
VSIM4>
```


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