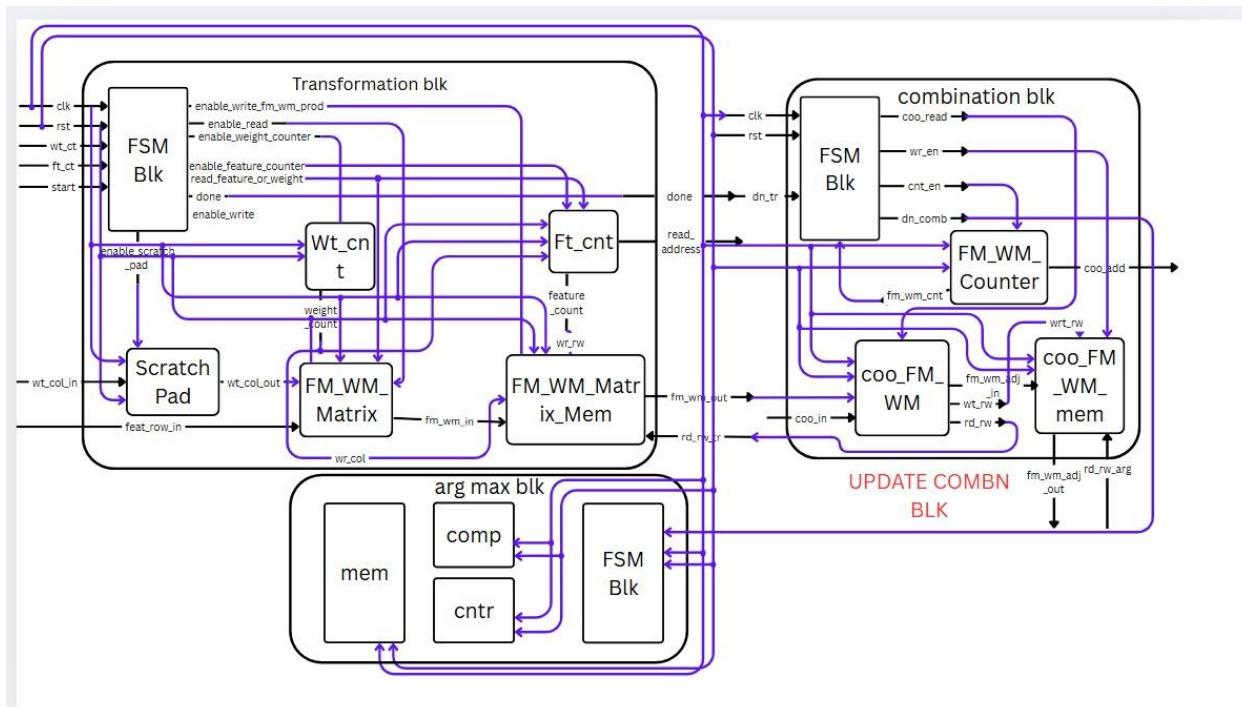
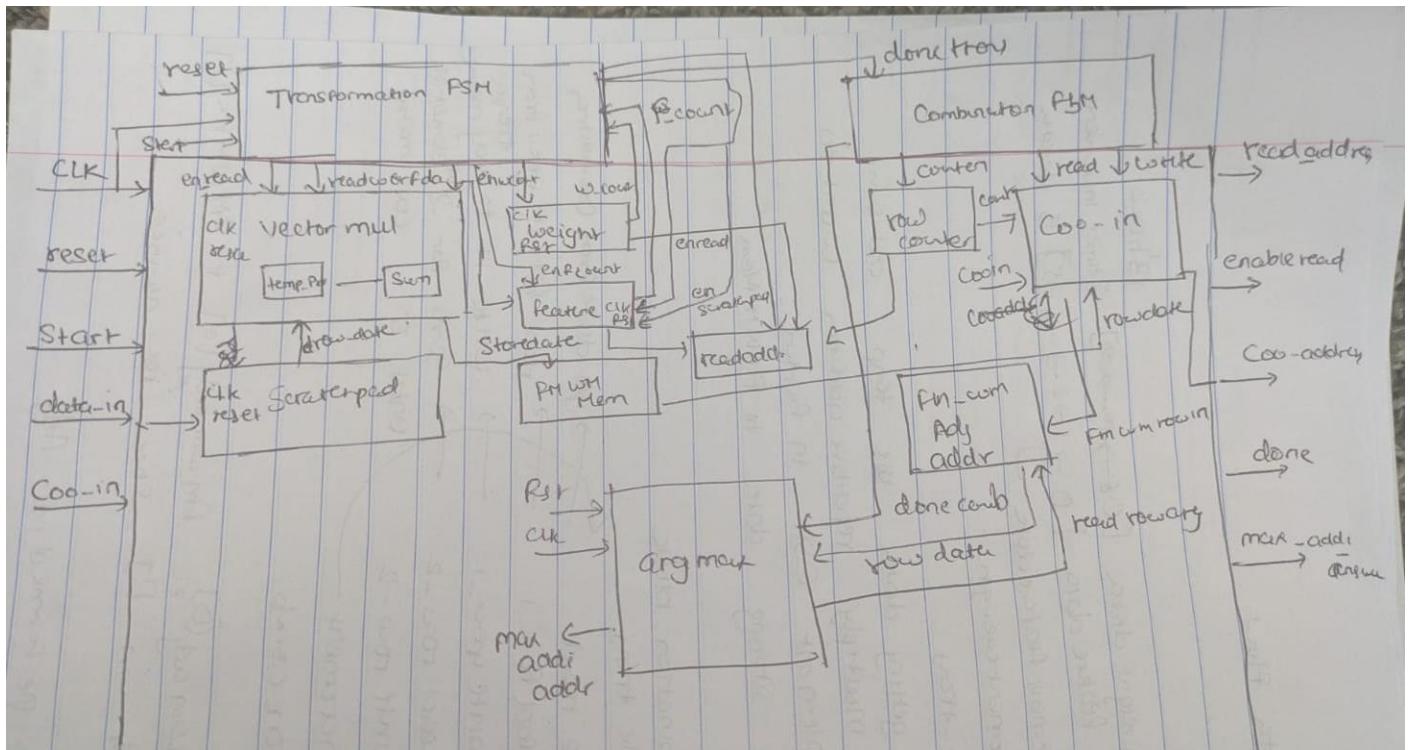


VLSI LAB 4 Milestone 1



## Data Flow

Start

13 hours

Read weight data  $[0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5]$  3 times incrementRead feature data  $[0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5]$  5 iterate

Increment Feature data

Increment weight

Done-tray

while getting data use temp and sum

to multiply repetitive addition want to

Implement CSA in future

Keep storing data to FFMW Mem

## Combination block

done tray

Coo read

get data from Coo-address

Read Row-1

read FFMW row from tree

Write Row-1

write it to adj mem

Read Row-2

serve for 2<sup>nd</sup> element or

Write Row-2

until 5 Coo-matrix

Increment

Done comb

loop

$$\text{fmwmadj}[0] = \text{fmwmadj}[0] + \text{fmwmrow}[i]$$

Boxer in [ ] show row number

Addition performed in Adj

### 1. Transformation Block

The Transformation\_Block performs matrix-vector multiplication between features and weights. It includes submodules: Vector\_Multiplier, Weight\_Counter, Feature\_Counter, Scratch\_Pad, Matrix\_FM\_WM\_Memory, and Transformation\_FSM.

- Feature and weight vectors are stored in local scratchpads.
- Counters select feature rows and weight columns.
- The Vector\_Multiplier performs parallel dot-products (WEIGHT\_COLS = 3 parallel multipliers).
- Results are stored in Matrix\_FM\_WM\_Memory.
- Transformation\_FSM controls read, multiply, and write sequences.

### 2. Combination Block

The Combination\_Block aggregates transformed features based on sparse graph connections (COO format).

It includes coo\_in, ROW\_Counter, Matrix\_FM\_WM\_ADJ\_Memory, and Combination\_FSM.

- coo\_in provides source-target node pairs.
- ROW\_Counter iterates over edges.
- Features are accumulated selectively according to graph edges.
- Sparse aggregation is handled efficiently to reduce unnecessary operations.
- Combination\_FSM manages control flow and signals completion.

### 3. Argmax Block

The argmax module selects the maximum feature per node after aggregation.

- Accepts aggregated feature vectors.
- Uses compare-and-select logic to find the maximum value per node.
- Stores maximum indices in max\_addi\_answer.
- Internal FSM controls idle, compare, and output states.
- Triggered after done\_comb from Combination Block.

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## Behavioral Verilog Netlist output

```

#> vcs -svinputport=relaxed
# ** Warning: /home/a21116_asu/asap7_rundir/Lab4/code/rtl/argmax.sv(12): (vopt-13314) Defaulting port 'fm_wm_adj_out' kind to 'var' rather than 'wire' due to default compile option setting of -svinputport=relaxed.
# Loading sv_std.std
# Loading work.GCN_TB(fast)
# Loading work.GCN(fast)
# Loading work.Transformation_Block(fast)
# Loading work.Feature_Counter(fast)
# Loading work.Weight_Counter(fast)
# Loading work.Vector_Multiplier(fast)
# Loading work.Matrix_FM_WM_Memory(fast)
# Loading work.Scratch_Fad(fast)
# Loading work.Transformation_FSM(fast)
# Loading work.combination_block(fast)
# Loading work.combination_FSM(fast)
# Loading work.ROW_counter(fast)
# Loading work.cooc_in(fast)
# Loading work.Matrix_FM_WM_ANJ_Memory(fast)
# Loading work.argmax(fast)
add wave -r /*
VSM> run -all
# max_addi_answer[0] DUT: 0 GOLD: 0
# max_addi_answer[1] DUT: 0 GOLD: 0
# max_addi_answer[2] DUT: 0 GOLD: 0
# max_addi_answer[3] DUT: 1 GOLD: 1
# max_addi_answer[4] DUT: 1 GOLD: 1
# max_addi_answer[5] DUT: 2 GOLD: 2
#
# ** Note: $finish : /home/a21116_asu/asap7_rundir/Lab4/GCN_TB.sv(96)
# Time: 876 ps Iteration: 0 Instance: /GCN_TB
# 1
# Break in Module GCN_TB at /home/a21116_asu/asap7_rundir/Lab4/GCN_TB.sv line 96
VSIM>

```

## Synthesized Verilog Netlist output

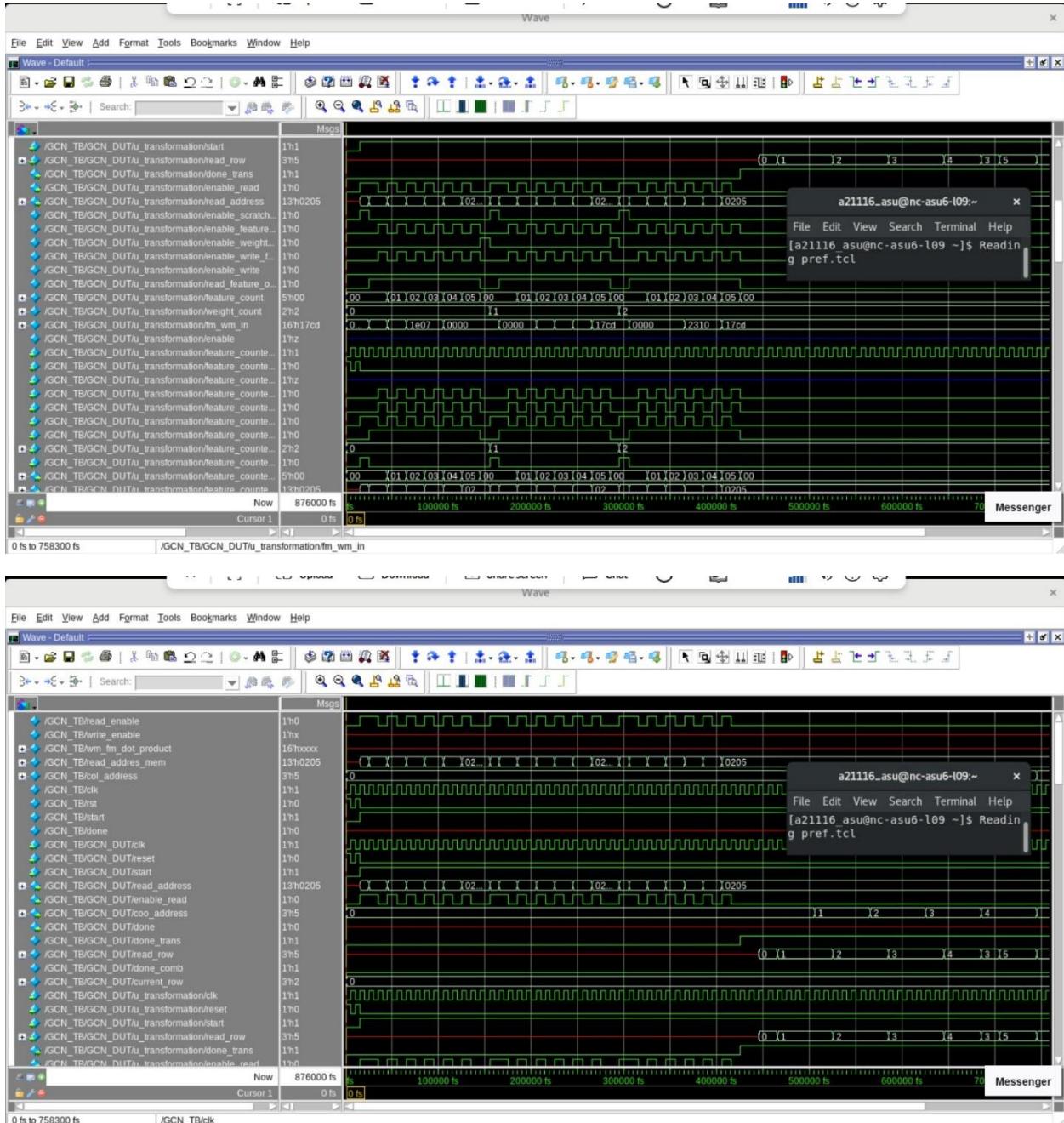
Name	Type	Value	Kind
write_enable	Register	1hx	Internal
wm_fn_dot_product	Packed Array	16hxxxx	Internal
WEIGHT_WIDTH	Parameter	32h00000005	Internal
WEIGHT_ROWS	Parameter	32h00000000	Internal
weight_matrix_mem	Fixed-size Array	(5h06 5h10 5h1c 5h0b 5h1...	Internal
weight_filename	String	/home/a21116_asu/asap7_ru...	Internal
WEIGHT_COLS	Parameter	32h00000003	Internal
start	Register	1h1	Internal
rst	Register	1h0	Internal
read_enable	Register	1h0	Internal
read_address_mem	Packed Array	13h0002	Internal
NUM_OF_NODES	Parameter	32h00000006	Internal
MAX_ADDRESS_WL...	Parameter	32h00000002	Internal
max_addi_answer_fn...	Fixed-size Array	2hx 2hx 2hx 2hx 2hx 2hx	Internal
input_data_temp	Packed Array	5h00 5h00 5h00 5h00 5h0...	Internal

```

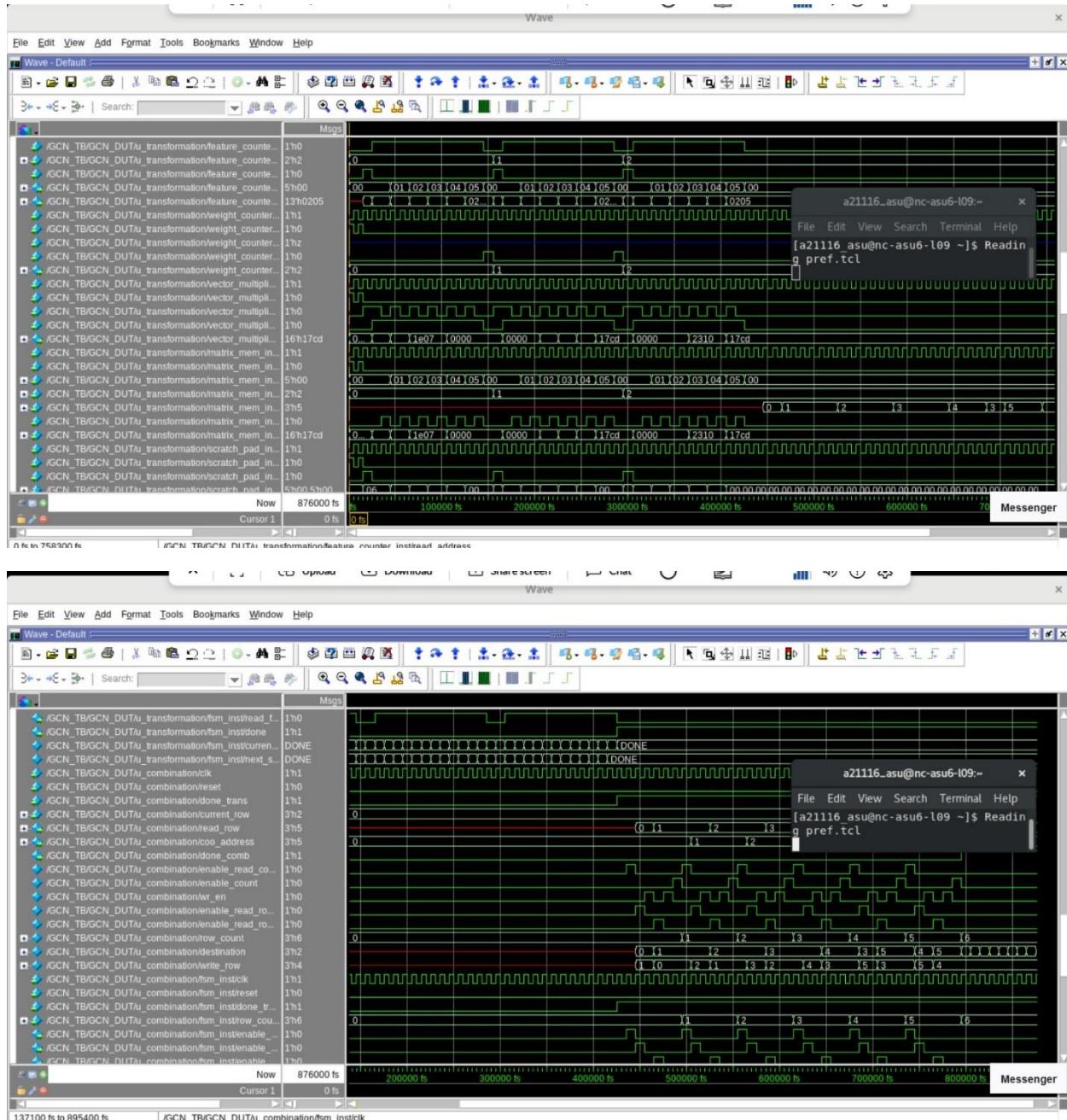
#> sim -Default
#> run -all
# max_addi_answer[0] DUT: 0 GOLD: 0
# max_addi_answer[1] DUT: 0 GOLD: 0
# max_addi_answer[2] DUT: 0 GOLD: 0
# max_addi_answer[3] DUT: 1 GOLD: 1
# max_addi_answer[4] DUT: 1 GOLD: 1
# max_addi_answer[5] DUT: 2 GOLD: 2
#
# ** Note: $finish : /home/a21116_asu/asap7_rundir/Lab4/code/tb/GCN_TB_post_syn_apr.sv(123)
# Time: 90752 ps Iteration: 0 Instance: /GCN_TB
# 1
# Break in Module GCN_TB at /home/a21116_asu/asap7_rundir/Lab4/code/tb/GCN_TB_post_syn_apr.sv line 123
VSIM>

```

# VLSI LAB 4 Milestone 1



# VLSI LAB 4 Milestone 1



# VLSI LAB 4 Milestone 1

