Simulation Report: 4-bit ALU in Verilog

1. Design Description

A 4-bit Arithmetic Logic Unit (ALU) is designed in Verilog. The ALU supports the following operations: 000 – Addition (A + B) 001 – Subtraction (A - B) 010 – AND (A & B) 011 – OR (A | B) 100 – NOT (~A) The ALU provides two outputs: a 4-bit result and a carry_out flag to indicate overflow/borrow conditions.

2. Testbench Description

The testbench applies various test cases to the ALU. Inputs A, B, and opcode are varied to check all operations. Simulation results are observed using $monitor for console output and $dumpfile/$dumpvars for waveform generation.

3. Simulation Console Output

Time (ns)	A	B	Opcode	Result	Carry_out	Operation
0	0101	0011	000	1000	0	5 + 3 = 8
10	1111	0001	000	0000	1	15 + 1 = 16 (carry=1)
20	1000	0011	001	0101	0	8 - 3 = 5
30	0010	0100	001	1110	1	2 - 4 = borrow, result=1110
40	1100	1010	010	1000	0	1100 & 1010 = 1000
50	1100	1010	011	1110	0	1100 | 1010 = 1110
60	1010	0000	100	0101	0	~1010 = 0101

4. Waveform Analysis

The generated VCD file (alu_tb.vcd) was viewed in GTKWave. The waveforms confirmed the following: Addition overflow is correctly captured by carry_out. Subtraction borrow is reflected in carry_out. Logical operations (AND, OR, NOT) execute correctly with carry_out = 0.

5. Conclusion

The 4-bit ALU was successfully designed and simulated in Verilog. The simulation results matched expected values for all operations. Carry/borrow functionality was correctly handled, and logical operations were verified. This ALU design can serve as a basic processing unit for further processor or digital system projects.