

K.V.G. COLLEGE OF ENGINEERING

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Department of Electronics and Communication Engineering

Name of the Faculty	Dr. SAVITHA. M
Designation	Professor
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• Educational Qualification

Degree	Specialization	Year of Passing	College & University
B.E	Electrical and Electronics	1995	KVG college of engineering Sullia- Mangalore
M. Tech	Industrial Electronics	2003	NITK Surathkal, NITK
Ph.D.	Mixed Mode VLSI	2020	REVA University Bangalore

• Work Experience

Teaching	Research	Industry
22+Experience	4+Experience	2 year

• Date of Joining to the College

10th May 1999

• In-House Experience				
Designation	Duration		Department	
Designation	From	То	Department	
Lecturer	10-05-1999	31-03-2005	E & C	
Asst. Professor	01-04-2005 26-02-2012		E & C	
Associate Professor	27-02-2012 to 2021		E & C	
Professor	2021 to Till the Date		E & C	

• Outside Experience

		Duration	
Designation	Place		To
Engineer –Trainee	Power Gear Limited, Bangalore	01-08-1996	30-01-1998

• Area of Interest

Analog and Mixed Mode VLSI	Verilog and VHDL Languages	Digital Signal Processing	Power Electronics	CMOS VLSI	Microprocessor
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Subject Taught

For UG:

- 1. Analog Electronics Circuit
- 2. Signal And System
- 3. VLSI Design
- 4. CMOS VLSI Design
- 5. Low Power VLSI
- 6. Digital Signal Processing
- 7. Analog and mixed Mode VLSI

- 8. Basic VLSI
- 9. Power electronics
- 10. Fundamental of HDL
- 11. Microelectronics
- 12. Digital Design using VHDL
- 13. Embedded system
- 14. Computer Organization
- 15. Basic Electronics
- 16. Verilog HDL

For PG:

- 1. CMOS VLSI design
- 2. Research Methodology and IPR
- 3. Cryptography and network security
- 4. Advances VLSI Design
- 5. VLSI design verification
- 6. Design of CMOS RF circuit
- 7. Advanced Analog and mixed Mode VLSI
- 8. Research Methodology

Membership in Professional Bodies/University Bodies/Organizations

- **Member of Indian Society for Technical Education (MISTE):** LM-37012 (2001)

Publications

National / International Journals	National / International Conferences
03	05

• Publications: International Journals

- 1. Savitha .M, R.Venkat Siva Reddy, "Dual Split-Three Segment Capacitor Array Design Based Successive Approximation ADC for Io-T Ecosystem" Integration", The VLSI Journal https://doi.org/10.1016/j.vlsi.2019.05.004
- 2. Savitha .M, Venkat Siva Reddy, "A 14-bit Dual-Split Capacitor Array DAC Design Based Successive Approximation ADC" International Journal of Recent Technology and Engineering (IJRTE)' at Volume-8 Issue-1, May 2019.
- 3. Raghavendra, Savitha .M, "Multi-serial to Ethernet gateway by using FPGA" International Journal of Recent Technology and Engineering (IJRTE)' at issue no. 2250-3536, 2012.

• Publications: National / International Conferences

- "14 -bit Low Power Successive Approximation ADC using Two Step Split Capacitive array DAC with multiplexer switching". *IEEE, second ICAECC-2018*
- "FPGA implementation of Fingerprint Verification Based on Fusion of minutiae and Ridges" was presented in "International Conference on Current Trends in Engineering and Management ICCTE-M2012" held on12, 13 &14th July 2012 at Vidyavardhaka College of Engineering, Mysore.
- "Multi-serial to Ethernet gateway by Using FPGA" was presented in "National conference on Emerging Trends in Technology –NCET-Tech 2O12" held on 26th 27th April 2012 at Nagarjuna college of Engineering and Technology, Bangalore.
- "FPGA implementation of realization of efficient BCD adder using reversible logic" was presented in *National Conference on "Advances in Computer Applications-NCACA-2012* which was held at Sri Siddhartha Institute of Technology, Tumkur, Karnataka on 10th and 11th May 2012.
- "Design and analysis of an efficient double tail comparator using 0.18µm technology" was presented in *National Conference on "Recent trends in Electronics and communication engineering -NCRTEC-14* which was held at SJB institute of technology Bangalore on 10^{th th} May 2014.

Professional Activities: NPTEL Course

NPTEL	Subject	Year of Certification	Result
(National Program on	1. Teaching and Learning in	March-2019	72%
Technology Enhanced	Engineering (TALE)	(4weeks. FDP)	(Silver Medal)
Learning)	(Prof. N J Rao, IISc, Bangalore)		

• Faculty Development Programmes (FDP) Participated					
SL. No.	Program Title	Venue	Date & Year		
1.	DSP and its application	SJCE Mysore	25th to 28th March 2008		
2.	Faculty training program on internal audit	Power Gear ltd	11 th to 12 th July 2003		
3.	Faculty training program on VLSI design	RNSIT Bangalore	4th to 6th August 2005		
4.	Eighth state level convention on ISTE	KVGCE Sullia	18 th 19 th November		
5.	Applications of Artificial intelligence and machine learning	Reva Universisty Bangaluru	10 th to 14 th of May 2021		
6	An Overview of Teaching Techniques in Innovation & Design Thinking	VTU Human Resource Development Centre	6th to 10th December 2021		
7	"An Overview of Teaching Techniques in Scientific Foundations of Health	VTU Human Resource Development Centre	20th & 24th December 2021		

SL. No.	Workshop Title	Place	Date & Year
1.	Research Methodology and Latex Documentation	REVA university - Bangalore	9th and 10th Jan 2017
2.	Machine dynamics and instrumentation" [MDI _ 2012]	KVGCE SULLIA	26 th - 30 th March 2012
3.	Mission 10X'	KVGCE SULLIA	20 th to 24 th December 2010
4.	Faculty training program in power Electronics (theory and lab)	NMAMIT,Nitte	23 rd to 28 th February 2004
5.	Application on Signal Processing - AICTE sponsored)	SJCE Mysore	2004
6	ASIC Design flow using Mentor graphics tools	CoreEL Technolog Blore	06th September 2021

No. of Project Guided		
UG	PG	
15	13	

Responsibilities Taken in College Level					
Event	Positions	Duration			
Lvent	1 ositions	From	То		
PG studies	Director of PG studies	06-06-2022	Till the date		
Alumni Association Sullia chapter	Treasurer	2010	Till the date		
Language Lab Coordinator	Coordinator	2021	Till the date		

Responsibilities Taken in Department Level **Duration Event** Role То From 1. Research and MOU Coordinator Till the Date 2021 1. ENCEA Treasurer 2008 Till the Date In- charge 2. VLSI Lab 2010 Till the date 3 NBA/NAAC Coordinator Till the date 2012

• Participation details in the college level event.

SL .No.	Event	Position / Role	
1.	College sports meet	Member	
2.	Aluminee meet	M ember and Treasurer	
3.	College Day function	Member	
4.	Thanthrajna -2017	Member	

• Participation details in the Department level activities

SL .No.	Event	Role / Responsibilities
1.	e-congregation-2004	Chairman -Technical presentation

	2.	ENCEA activities	Judge for mini project and cultural activities	
	3.	LAB setup	In -charge for HDL lab, VLSI Lab	
4. Counselling		Counselling	Counselor for EC Students & Other dept. activities	

• No. of Lab Manual / Program Guidelines Prepared

SL. No. Lab manual / Guide lines Title		Lab manual / Guide lines Title Semester and branch	
1.	VLSI Lab manual	7 th sem E & C	2008 to 2019
2.	VHDL/Verilog Lab manual	4 th sem E & C	2008,2017,2021
3	Analog Circuits Lab Manual	4 th sem	2021

• No. of Labs handled for UG and PG

SL. No.	Lab Title	Year	Semester & Branch
1.	Power Electronics Lab	2004	VII E&C
2.	VLSI Lab	2008 to 2021	VII E&C
3.	AEC Lab	2010,to 2021	III E&C
4.	HDL Lab	2004to 2021	IV E&C
5.	Microprocessor Lab	2016, 2017	1V E&C
6.	Embedded Lab	2019	VI E&C

• Interaction with Outside World / Invited Lectures

Sl.No.	Program	Venue and Organizer	Date
1.	Sristi Project Exhibition	Sahyadri College of Engineering	12 th to 16 th May -2012

• Awards / Recognition / Achievements/ Others

- **Valuator** of VTU Digital Valuation Centre, KVGCE, Sullia for the digital Valuation work of UG/PG answer scripts VTU Examination.
- Served/Serving as Question Paper setter and Moderator for UG and PG program for VTU and other reputed autonomous institutes and Universities like NMAMIT @ Nitte, MIT@ Manipal.