

K.V.G. COLLEGE OF ENGINEERING

Kurunjibhag, Sullia, D.K.-574 327, Karnataka, INDIA E-mail: office@kvgengg.com website: www.kvgengg.com

Department of Electronics and Communication Engineering

FACULTY PROFILE

Name of the Faculty	JAGADEESH M
Designation	Assistant Professor
Contact Numbers	Office: 08257- 231141 Mobile: +91 - 9901730364
E-mail ID	jagadeesh.sullia@gmail.com



• Educational Qualification

Degree	Specialization	Year of Passing	College & University
B.E	Electronics and Communication	2008	KVGCE, Sullia, VTU
M. Tech	VLSI Design and Embedded Systems	2014	KVGCE, Sullia, VTU

• Work Experience

Teaching	Research	Industry
10+Experience		6 Months

• Date of Joining to the College

12th February 2009

• In-House Experience			
Desirentian	Dura	Department	
Designation	From	То	Department
Lecturer	12-02-2009	31-07-2014	E & C
Asst. Professor	01-08-2014	Till the Date	E & C

• Outside Experience

		Duration		
Designation	Place	From	То	
QC Engineer	Smile Electronics, Bangalore	01-08-2008	10-02-2009	

• Area of Interest

Embedded System	Assembly and Embedded C Programming	Signal Processing	Electrical Network Analysis	Electromagnetic Field Theory	Communication Systems
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Subject Taught

1. Antennas and Wave Propagation	8. 8051 Microcontroller
2. Analog communication	9. Electromagnetic Field Theory
3. Signals And Systems	10. Digital Switching System
4. Field Theory	11. Analog and Mixed Mode VLSI Design
5. Satellite Communication	12. Error Control Coding
6. Network Analysis	13. Control System
7. Optical Fiber Communication	14. ARM microcontroller and embedded systems

Publications

National / International Journals	National / International Conferences
	01

• Publications: National / International Conferences

 Design And Analysis of An Area Efficient Boostable Repeater for Variation Resilience in VLSI Interconnect, "6th National Conference on Recent Trends in Electronics and Communication Engineering" at SJBIT, Bangalore, 10th May 2014.

Professional Activities: NPTEL Course				
NPTEL	Subject	Year of Certification	Result	
(National Program on	-			
Taska alaan Enkanaad	1. Teaching and Learning in	March-2019	Pass	
Technology Enhanced	Engineering (TALE)	(4weeks. FDP)	(55%)	
Learning)	(Prof. N J Rao, IISc, Bangalore)	(TWEEKS, I'DI)	(33%)	

• Faculty Development Programmes (FDP) Participated SL. No. Program Title Venue

1. Faculty Enrichment Program VTU Regional Office, Mysore 23-07-2018 to 27-07--2018 (Five days)

Date & Year

• No. of Project Guided

UG	PG
10	

Responsibilities Taken in College Level

Event	Positions	Duration	
	1 obtains	From	From
SC/ST Grievance Cell	Program coordinator	2012	Till date
NBA	Coordinator for Criteria – 4	2018	Till date
NBA	Coordinator for Criteria – 8	2018	Till date

• Responsibilities Taken in Department Level

Event	Role	Duration		
	Koic	From	То	
1. Time Table	Co-ordinator	2011	Till date	
2. 8051 Microcontroller Lab	In- charge	2014	2015	
3. DIMENSION	Co-ordinator	2017	Till date	
4. Internal Test	Co-ordinator	2018	Till date	
5.Examination	Coordinator	2020	Till date	

6.Embedded System Lab	In-charge	2020	Till date

Participation details in the college level event.			
SL .No.	Event	Position / Role	
1.	College sports meet	Volunteers committee	
2.	Aluminee meet	Program committee	
3.	College Day function	Member	
4.	College Day function	Member - Food committee	
5.	Science Talent Hunt Program	Member for Quiz Committee	
6.	Shilpi Magazine-XXV	Member	

Participation details in the Department level activities

SL .No.	Event	Role / Responsibilities
1.	e-congregation-2012	Co-ordinator
2.	e-congregation -2013 to till date	Member
3.	Counselling	Counselor for EC Students

• No. of Lab Manual / Program Guidelines Prepared

SL. No.	Lab manual / Guide lines Title	Semester and branch	Year
1.	Microcontroller Lab Manual	IV E&C	2014
2.	Embedded System Lab Manual	VI E&C	2021

• No. of Labs handled for UG and PG

SL. No.	Lab Title	Year	Semester & Branch
1.	Microcontroller lab	2009 to	IV E&C & V E&E
1.	Microcontroller lab	2019	IV EQU Q V EQE
2.	HDL Lab	2009	IV E&C
3.	Analog Electronics Lab	2010	III E&C
4.	Logic Design Lab	2010	III E&C
5.	DSP LAB	2010 to	V E&C
J.	DOI LAD	2015	V LCC

6.	Power Electronics Lab	2012	VII EC
7.	VLSI Lab	2011	VII EC
8.	Embedded Controller lab	2018	VI EC

• Interaction with Outside World / Invited Lectures

Sl.No.	Program	Venue and Organizer	Date	
		Srinivasa college of Engineering		
1.	Judge for Project Exhibition	and Technology, Srinivasa	22.05.2019	
		University, Mukka, Mangaluru.		
2.	Technical Talk, Resource person.	KVGP, Sullia	10.04.2018	
2.	(Advanced Microprocessor)	iii di , bama	10.01.2010	

• Awards / Recognition / Achievements / Others

- Served as Question Paper setter for UG Program (Signals and Systems) for NMAMIT @ Nitte
- Participated in State Level Sullia half marathon on 19-01-2019

PROF. JAGADEESH M, E &C DEPT., KVGCE, SULLIA, D.K - 574 327

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