

IIIT BANGALORE

VLS 502

Analog CMOS VLSI Design

Project Report

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Externally compensated LDO

1. Specifications

In this project, we have designed low dropout voltage regulator for both internally and externally compensated cases. We have designed these circuits in 45nm and 130nm technology nodes.

Below are the specifications for the externally compensated LDO:

Table 1: Specifications Summary

Parameter	Value
Vin	1.4V
Vout	1V
PSRR	60dB
Iload (min)	2mA
Iload (max)	10mA
Cload	1uF
Iquiescent	50uA
Transient duration	1u

The design includes calculation and simulation for both heavy load and light load current of 10mA and 2mA respectively.

2. Purpose of an LDO

Low Drop-Out (LDO) is a linear regulator used to get stable output voltage despite noise at the supply voltage. Consistent voltage levels is essential in various VLSI applications including digital, analog, and mixed-signal components in an IC.

Key Purposes of an LDO

- **Voltage Regulation:** Maintains a stable output voltage despite variations in input voltage or load current, ensuring consistent operation of sensitive electronic components.
- **Low Noise Power Supply:** Provides clean, low-ripple power, which is essential for noise-sensitive applications such as RF circuits, audio devices, and ADCs/DACs.
- **Load Current Stability:** Supports a range of load currents while maintaining stability, which is vital in circuits with dynamic power requirements.
- **Protection for Downstream Components:** Safeguards sensitive downstream components from voltage fluctuations and over voltage conditions.
- **Power Efficiency at Low Dropout:** Operates efficiently when the difference between input and output voltage is minimal, reducing energy loss compared to traditional linear regulators.

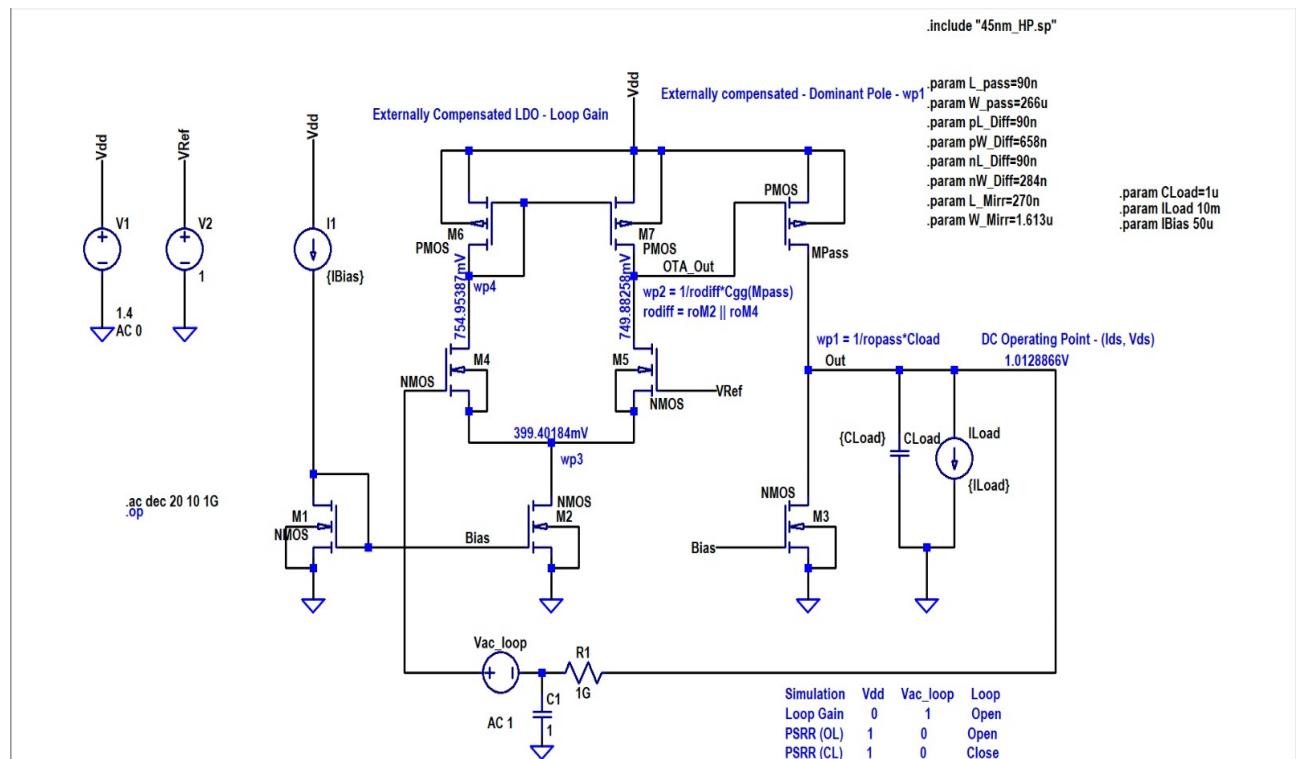


Figure 1: LDO schematic

3. Relevance of Techplots

Techplots are used as alternative for the square law, as the square law breaks at lower technology nodes due to short channel effects. Cadence Virtuoso is used to generate techplots for both NMOS and PMOS using gpdks of 45nm and 130nm.

Below are the generated techplots and five takeaways obtained from them.

- **Github Link:** <https://github.com/Bhavana-s-iiitb/Analog-CMOS-VLSI-Design/blob/main/README.md>
Technology node used - 45nm, 130nm and 180nm.
- f_T improves with shorter channel lengths, making circuits faster with scaling.
- Compared to 180nm the FOMs
- We chose the Vds to be 0.4 mV, and we expect that to result in some error because the Vds across every MOSFET might not be the same after sizing the circuit under a particular load. It is very possible that the Vds across the MOSFETs can change under different values of load current. The above phenomenon can be understood from the output log files mentioned below.

Techplots for 45nm

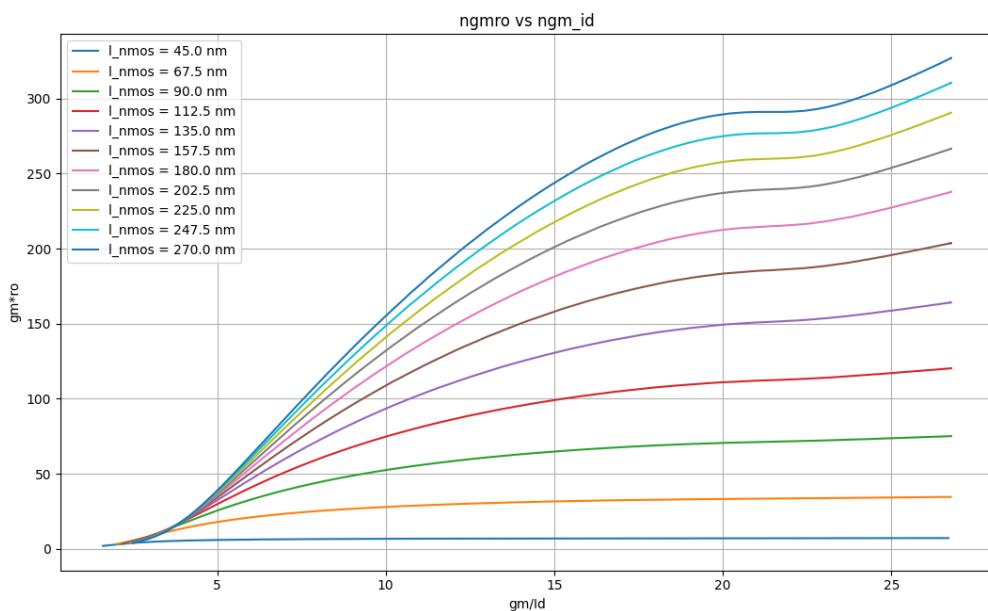
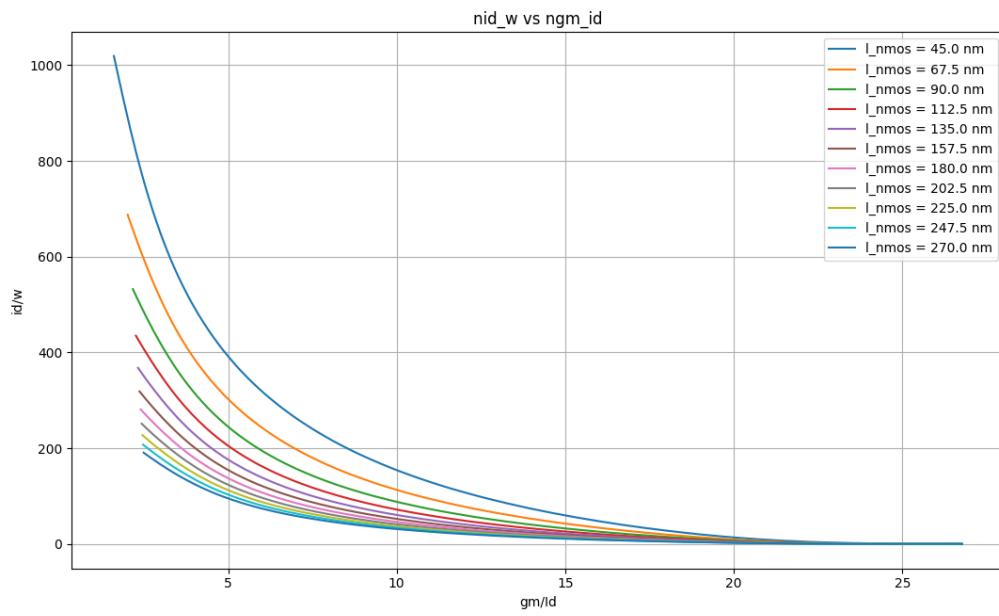
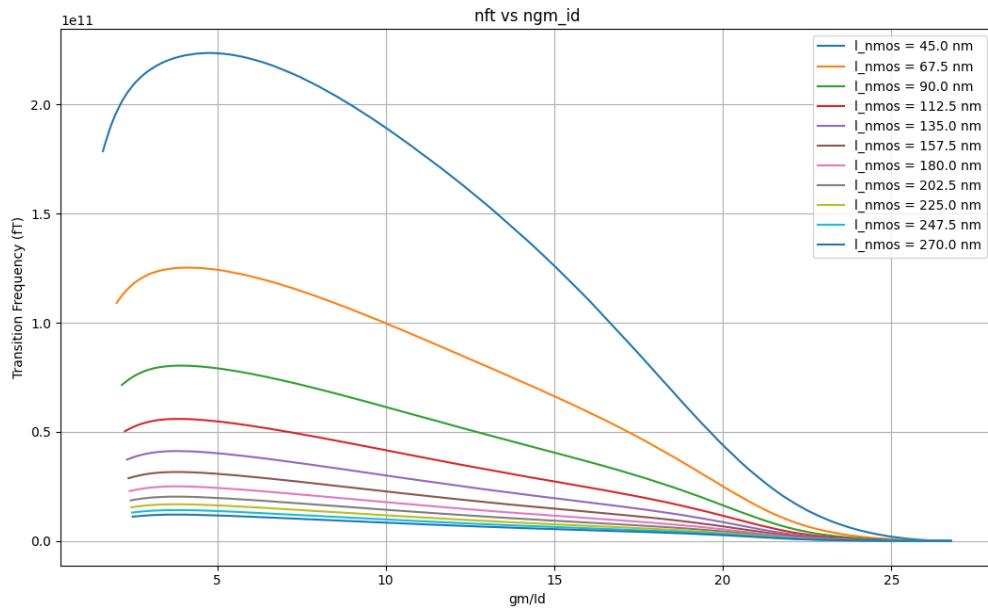
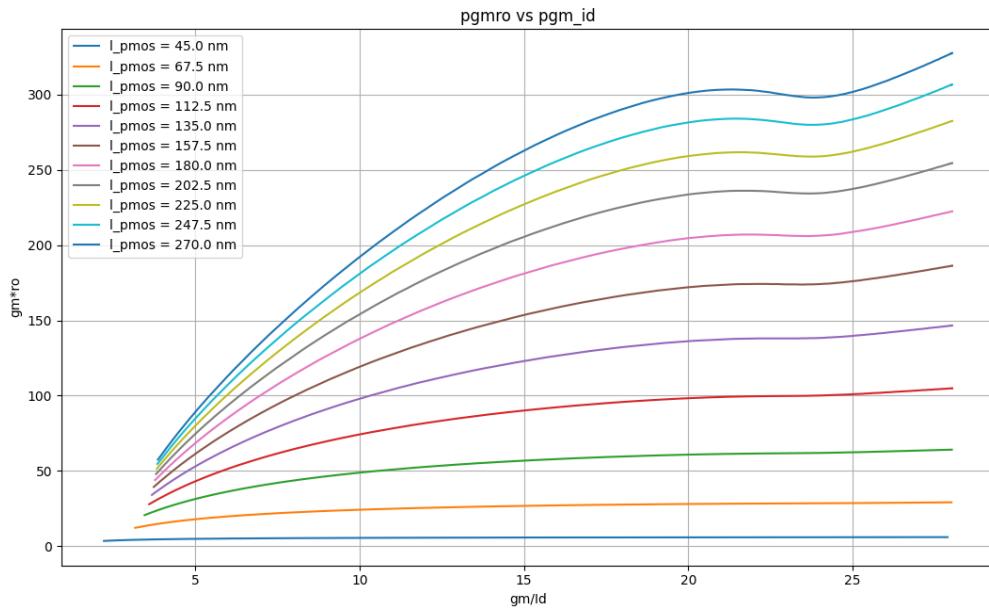
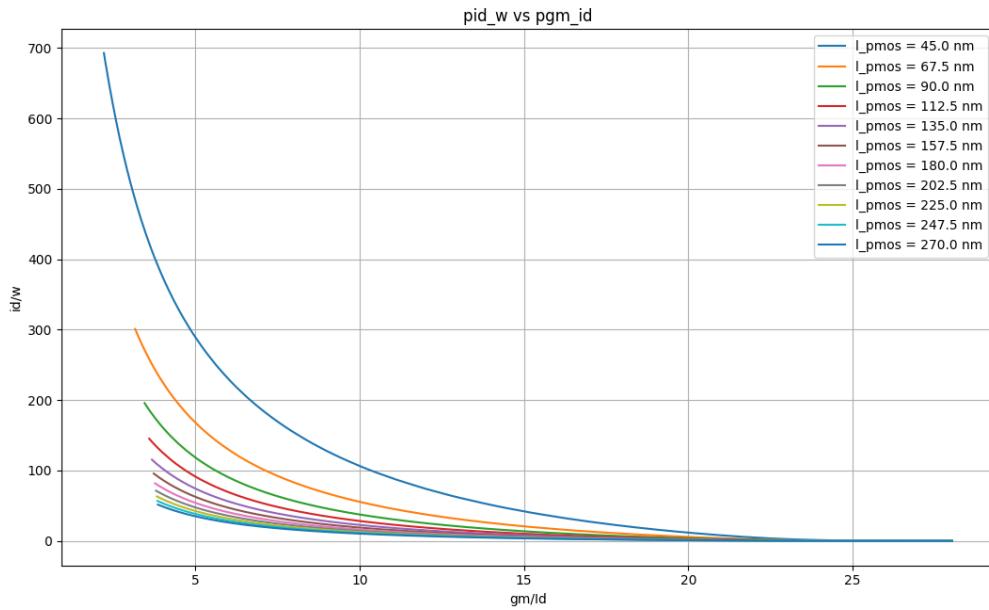
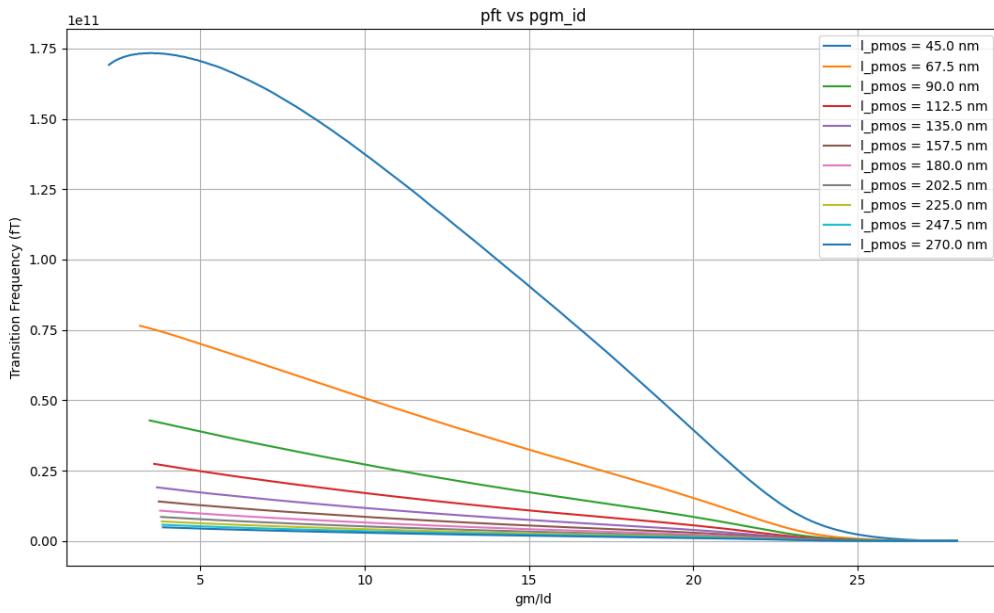


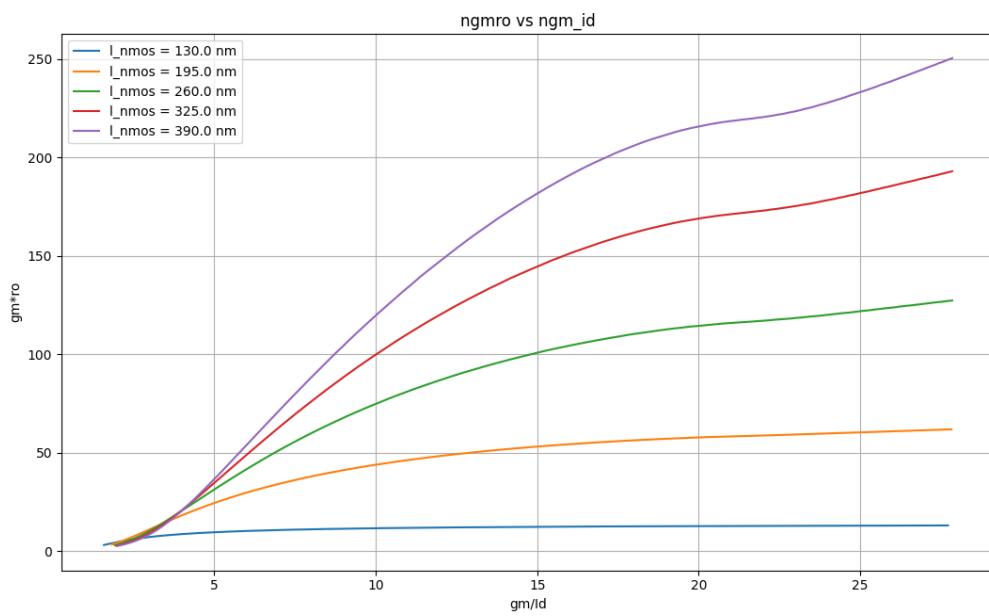
Figure 2: $gmro$ – NMOS – 45nm

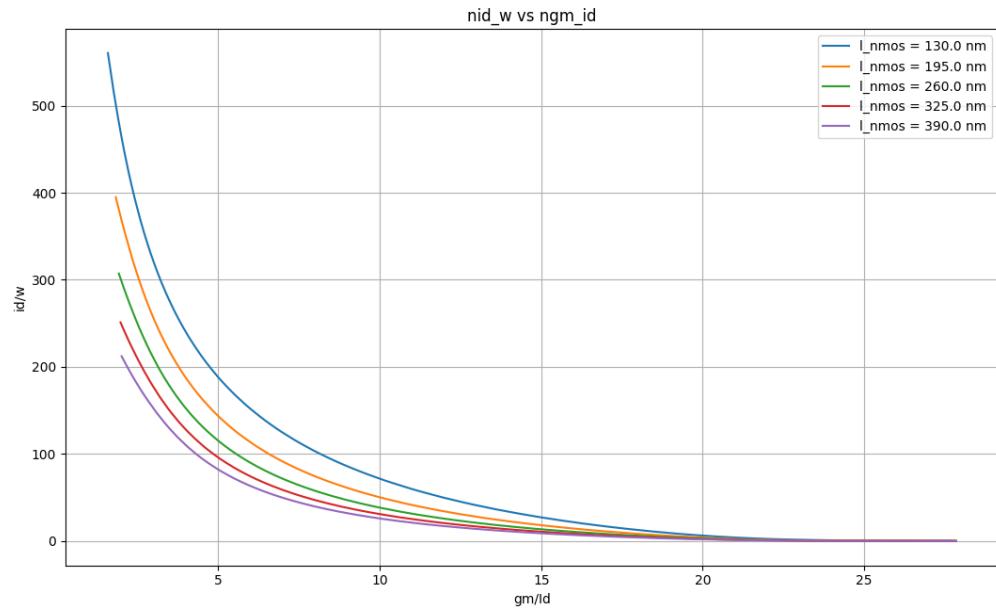
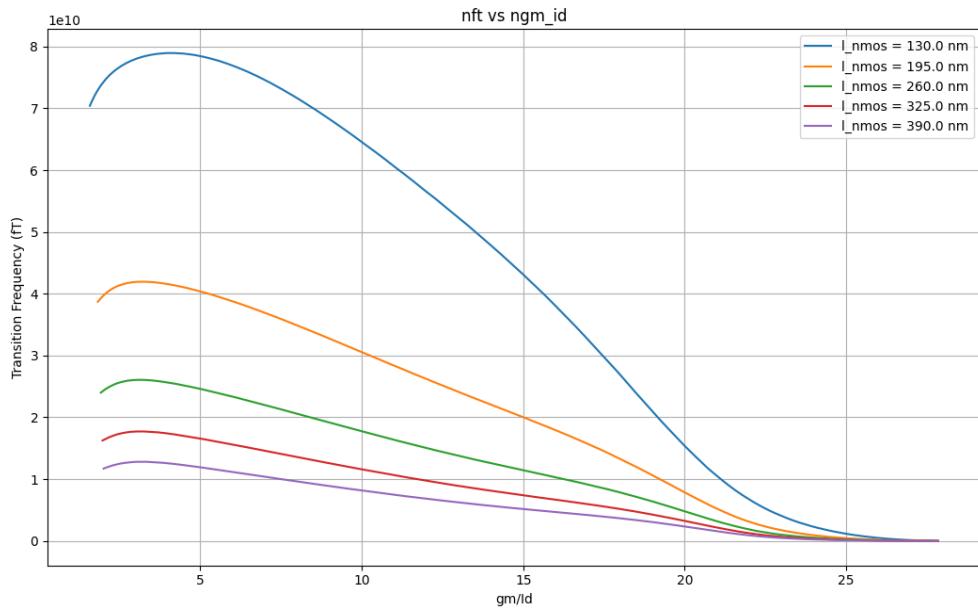
Figure 3: $idw - NMOS - 45nm$ Figure 4: $ft - NMOS - 45nm$

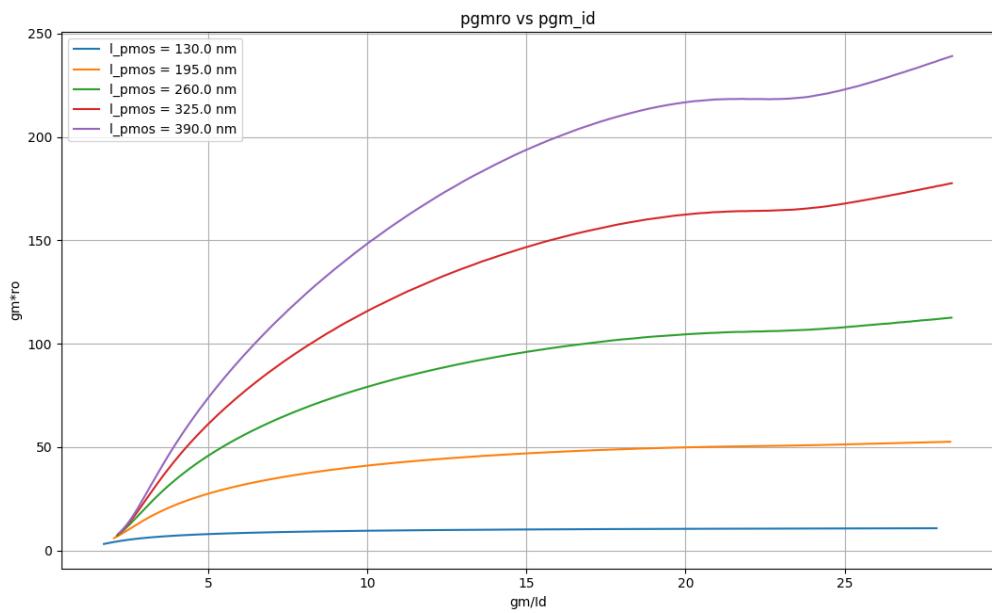
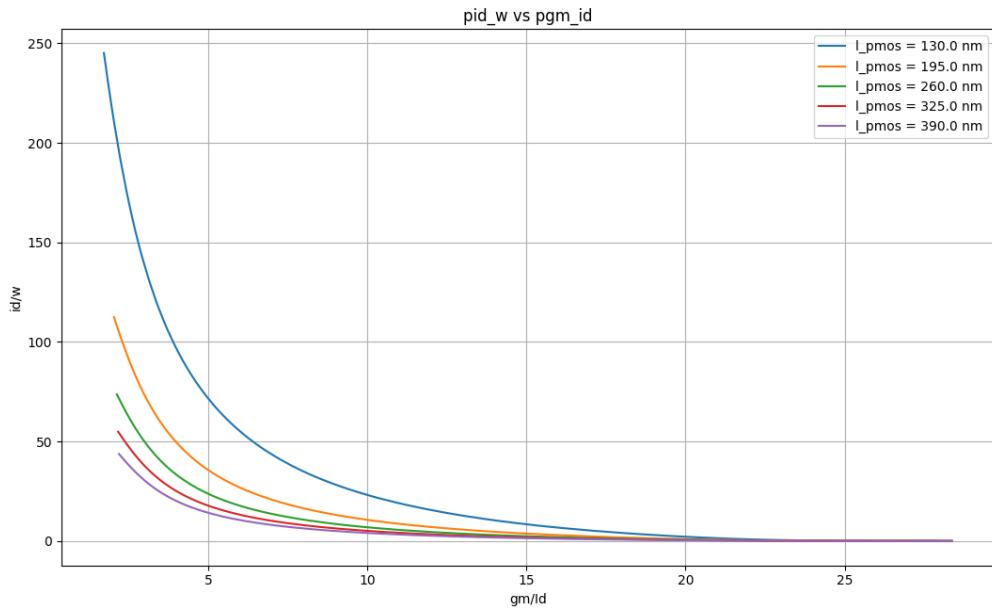
Figure 5: $gmro - PMOS - 45nm$ Figure 6: $idw - PMOS - 45nm$

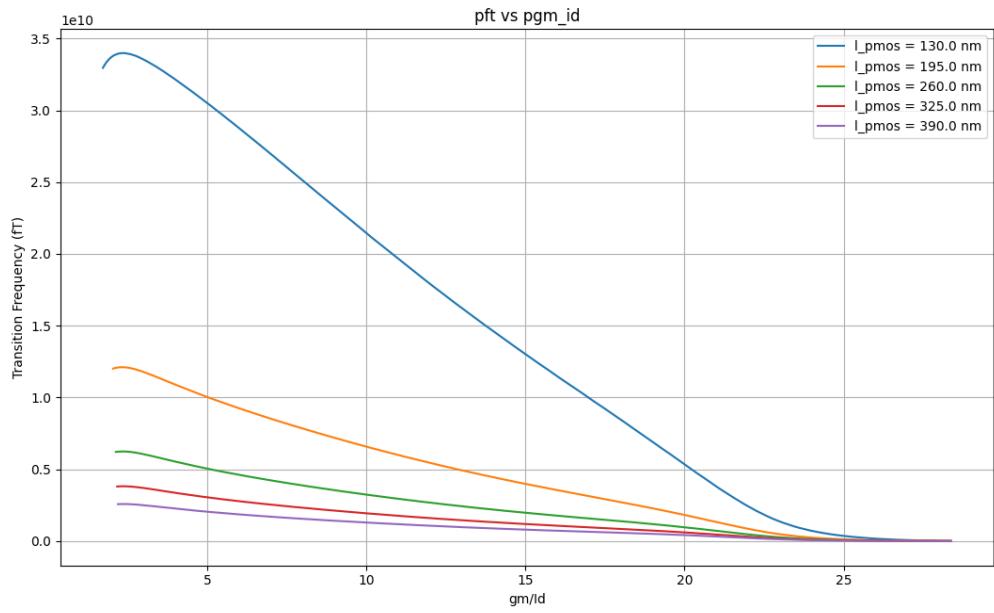
Figure 7: $ft - PMOS - 45nm$

Techplots for 130nm

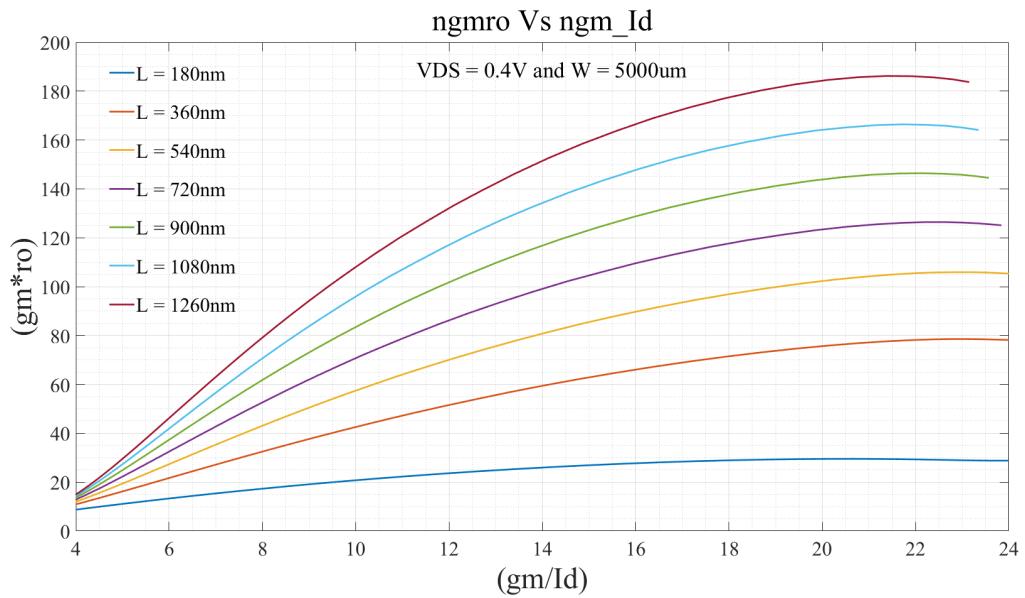
Figure 8: $gmro - NMOS - 130nm$

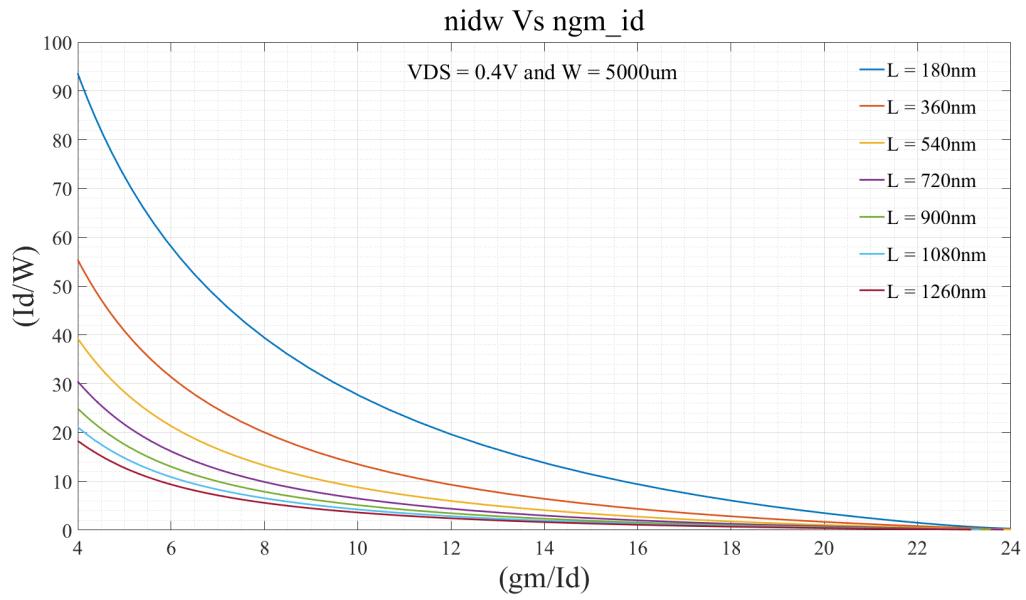
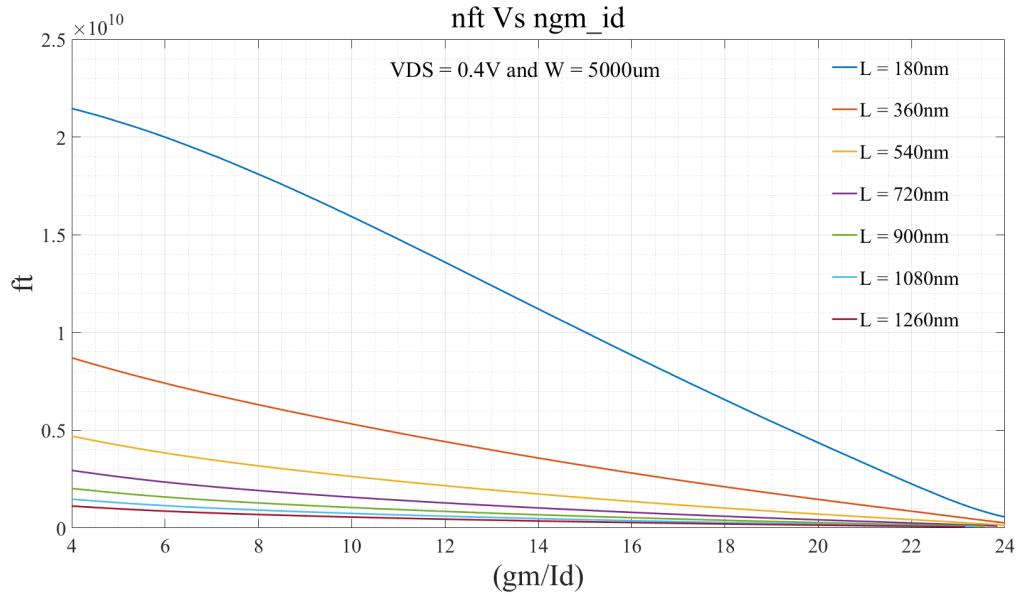
Figure 9: $idw - NMOS - 130nm$ Figure 10: $ft - NMOS - 130nm$

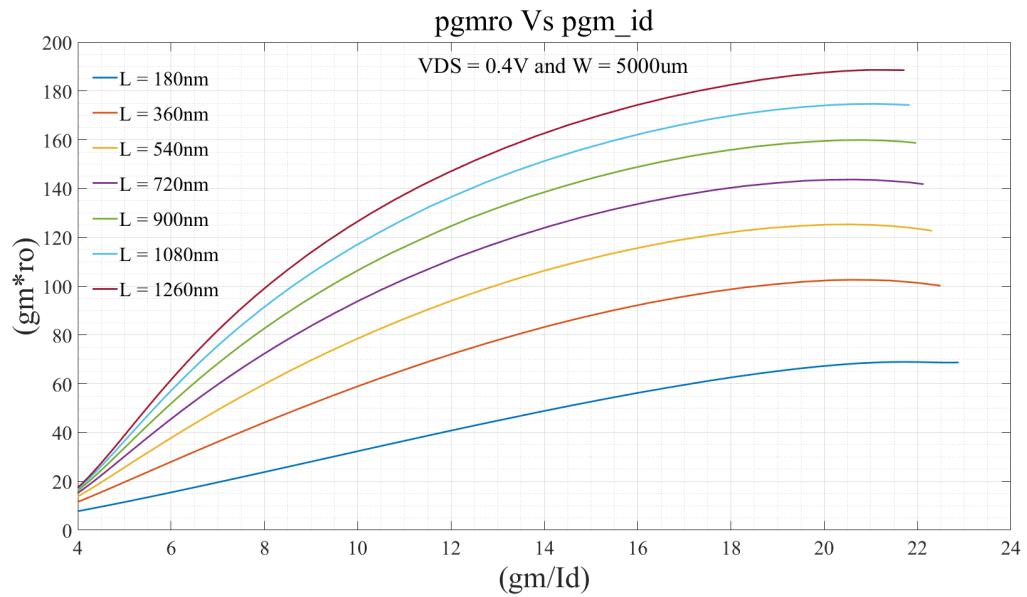
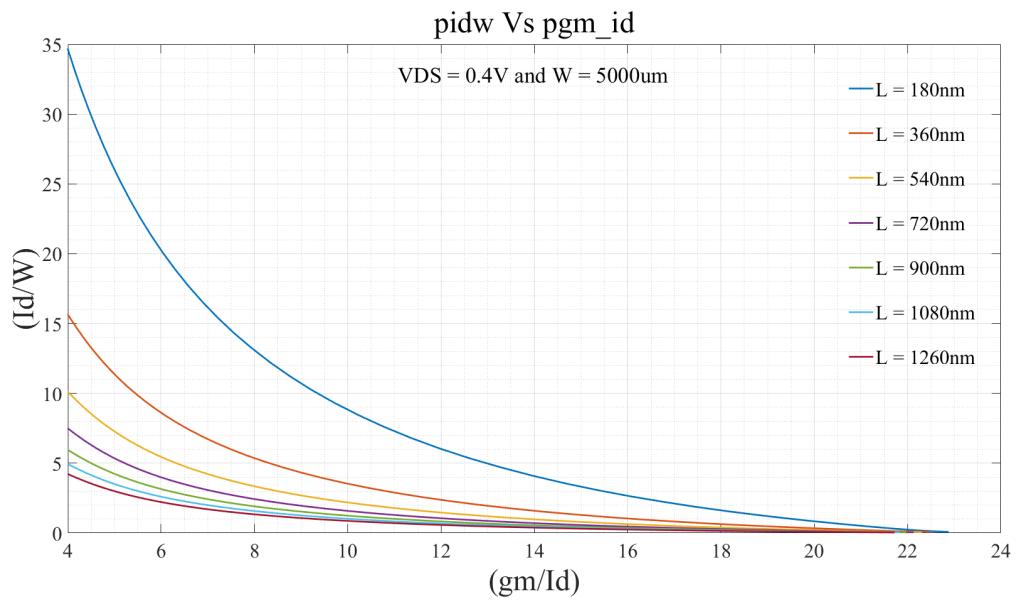
Figure 11: gm^{ro} – PMOS – 130nmFigure 12: idw – PMOS – 130nm

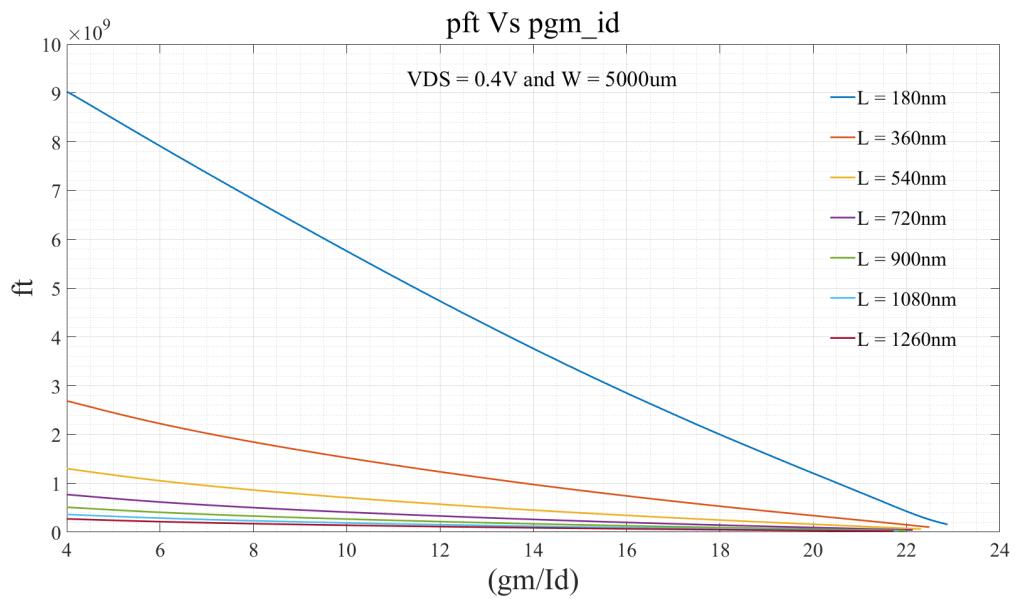
Figure 13: $f_T - PMOS - 130nm$

Techplots for 180nm

Figure 14: $gmro - NMOS - 180nm$

Figure 15: idw – NMOS – 180nmFigure 16: ft – NMOS – 180nm

Figure 17: $gmro - PMOS - 180nm$ Figure 18: $idw - PMOS - 180nm$

Figure 19: $ft - PMOS - 180nm$

4. FET Sizes

The sizes of the passFET, differential amplifier MOSFETs, and mirror transistors are designed based on the specifications given. Here we also include small-signal parameters and figures of merit (FOMs).

Sizing for 45nm

Table 2: FET Sizes and Parameters

Transistor	Size (W/L)	g_m/I_d	$g_m r_o$	I_d/W	f_t
PassFET PMOS (Mpass)	266u/90n	10	50	37.5	27.2 GHz
OTA NMOS (M4, M5)	284n/90n	10	40	88	61.4 GHz
OTA PMOS (M6, M7)	658n/90n	10	40	38	27.2 GHz
Current Mirror NMOS (M1, M2, M3)	1613n/270n	10	155	31	8.36 GHz

Sizing for 130nm

Table 3: FET Sizes and Parameters

Transistor	Size (W/L)	g_m/I_d	$g_m r_o$	I_d/W	f_t
PassFET PMOS (Mpass)	943.4u/195n	10	41	10.6	6.57 GHz
OTA NMOS (M4, M5)	500n/195n	10	48.78	50	30.55 GHz
OTA PMOS (M6, M7)	2.3585u/195n	10	48.78	10.59	6.57 GHz
Current Mirror NMOS (M1, M2, M3)	1941.7n/390n	10	120	25.75	8.16 GHz

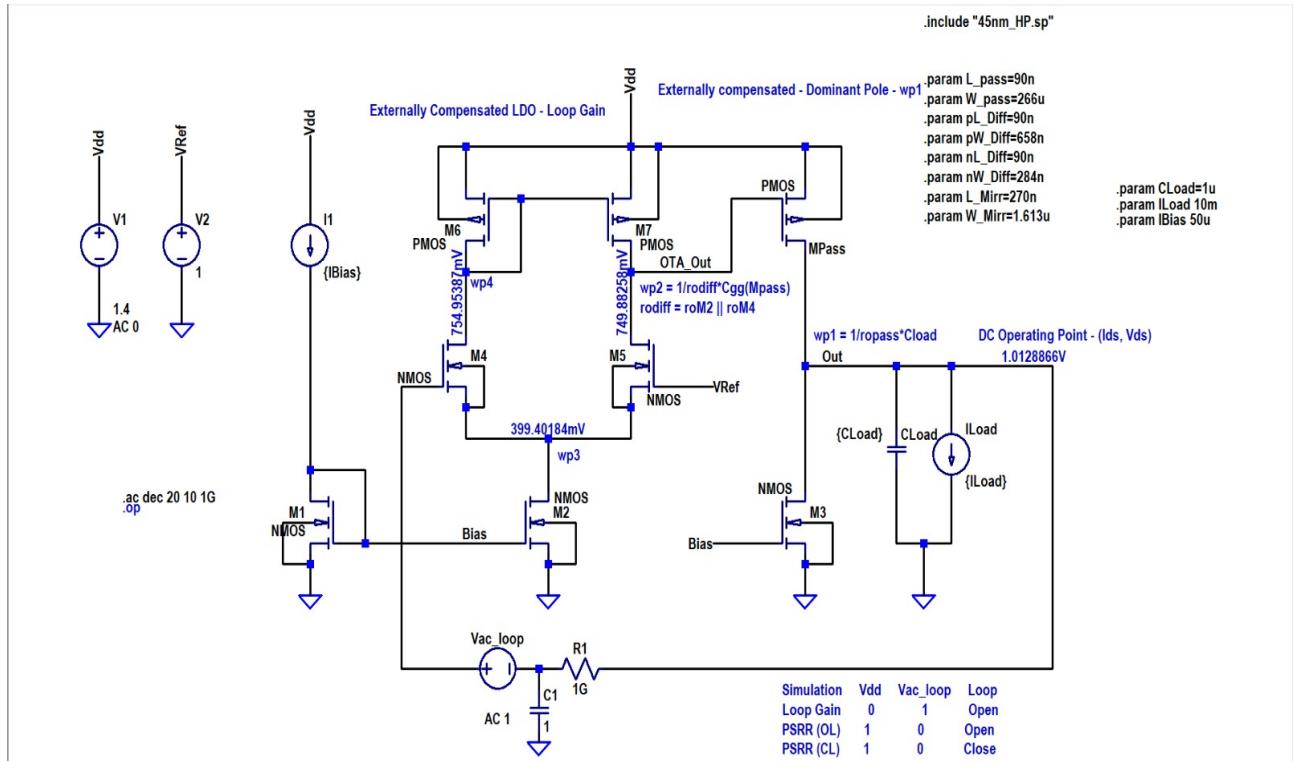


Figure 20: FET sizes and characteristics.

5. Stability Analysis

Externally Compensated LDO

Heavy Load (10mA) - 45nm:

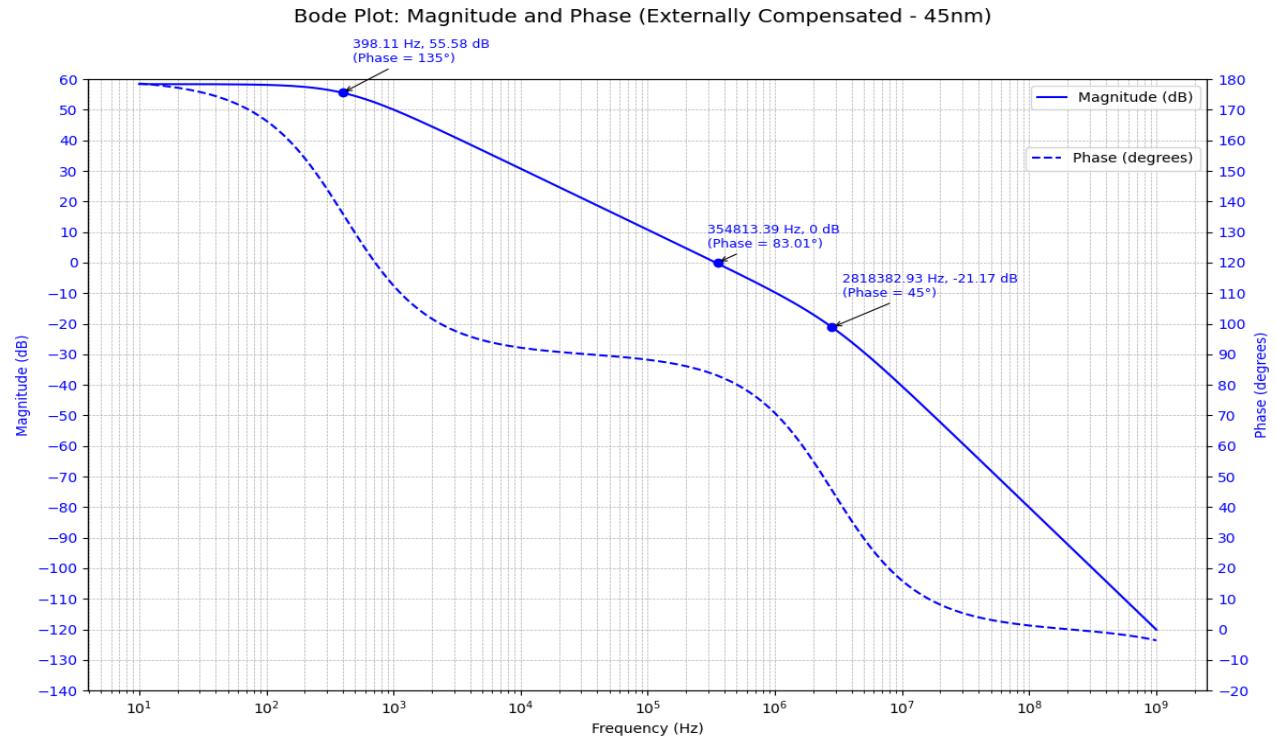


Figure 21: Magnitude and Phase Plot for Heavy Load - 45nm

Heavy Load (10mA) - 130nm:

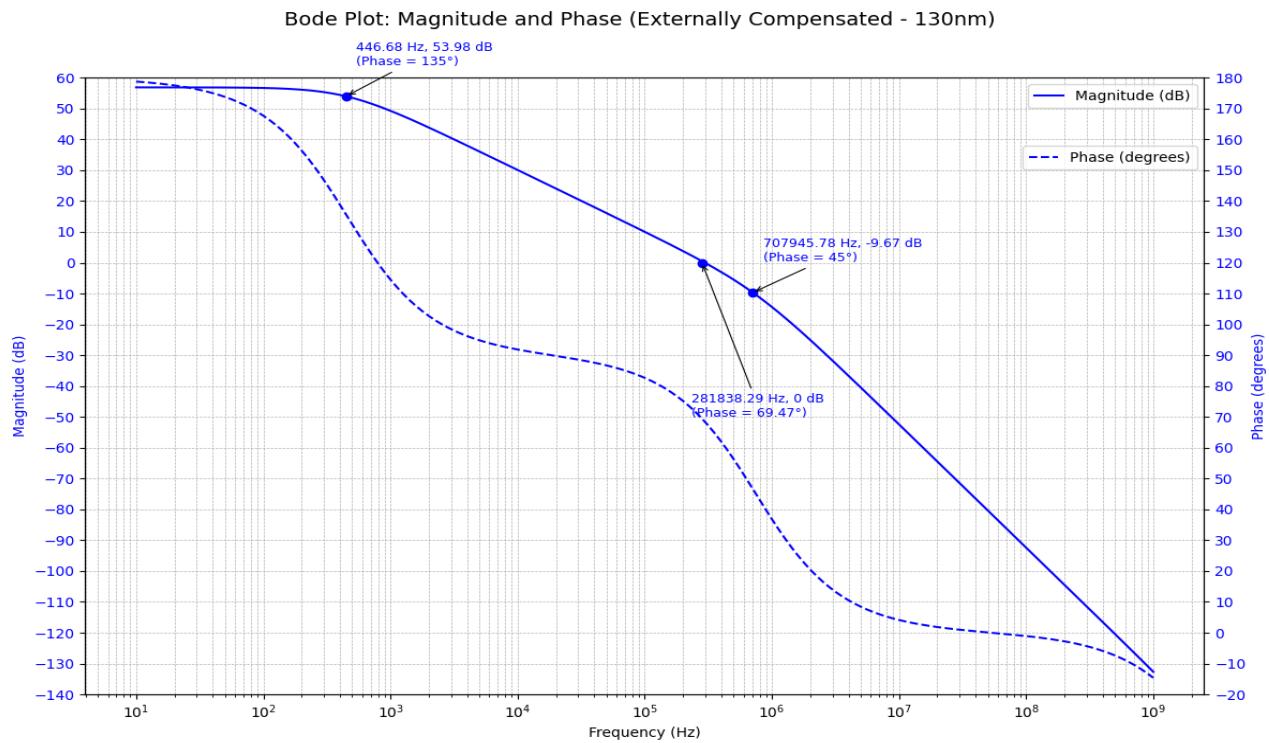


Figure 22: Magnitude and Phase Plot for Heavy Load - 130nm

Heavy Load (10mA) - 180nm:

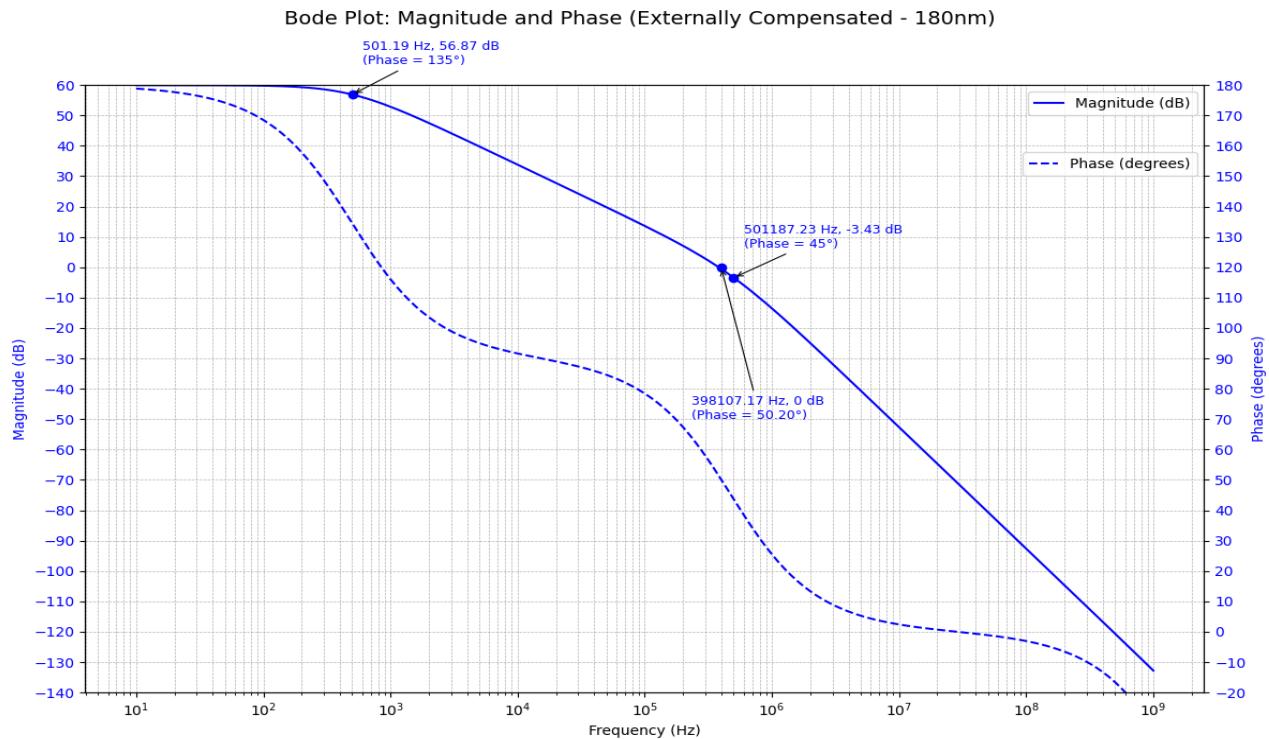


Figure 23: Magnitude and Phase Plot for Heavy Load - 180nm

Light Load (2mA) - 45nm:

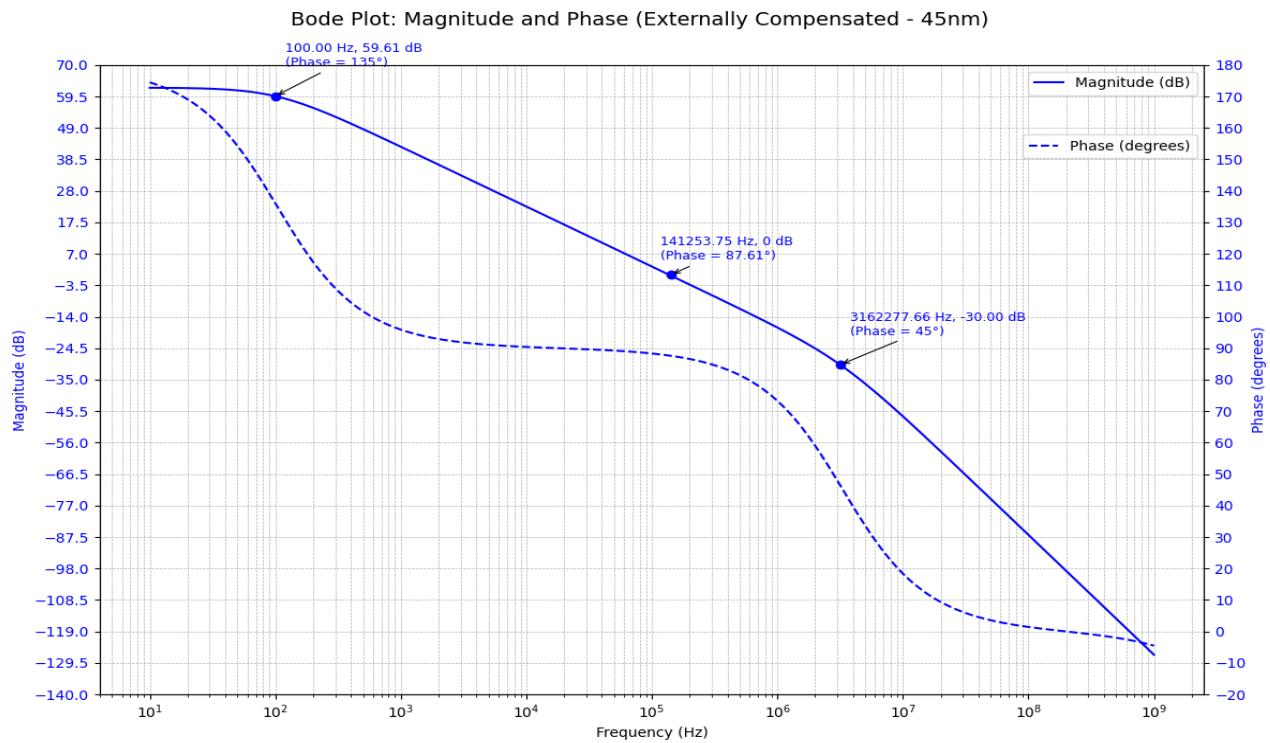


Figure 24: Magnitude and Phase Plot for Light Load - 45nm

Light Load (2mA) - 130nm:

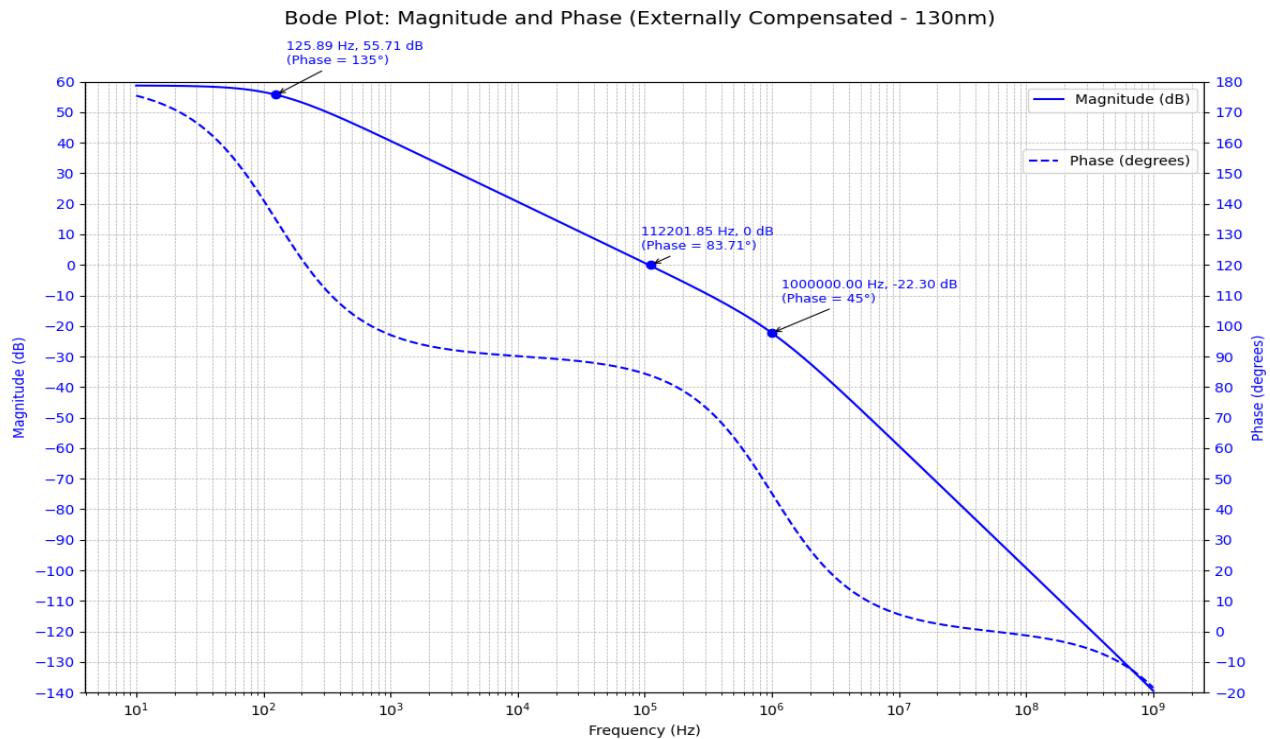


Figure 25: Magnitude and Phase Plot for Light Load - 130nm

Light Load (2mA) - 180nm:

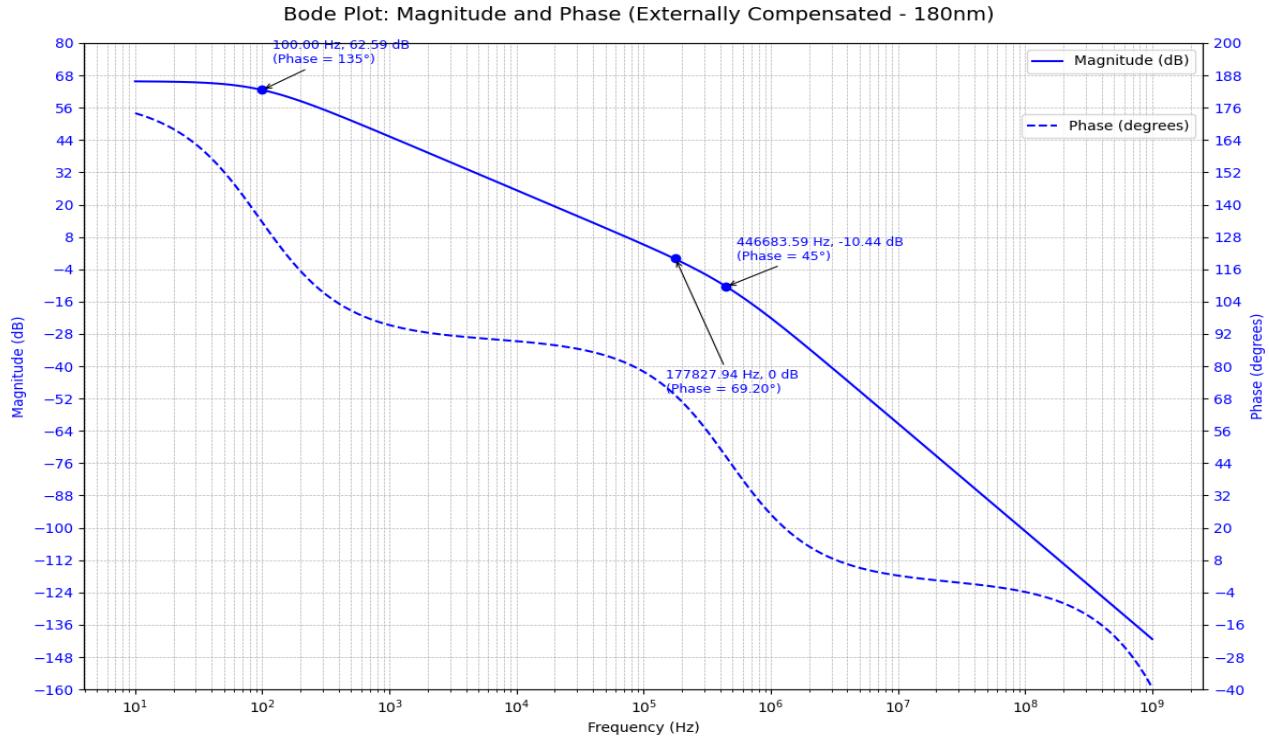


Figure 26: Magnitude and Phase Plot for Light Load - 180nm

Internally Compensated LDO

Heavy Load (10mA) - 45nm:

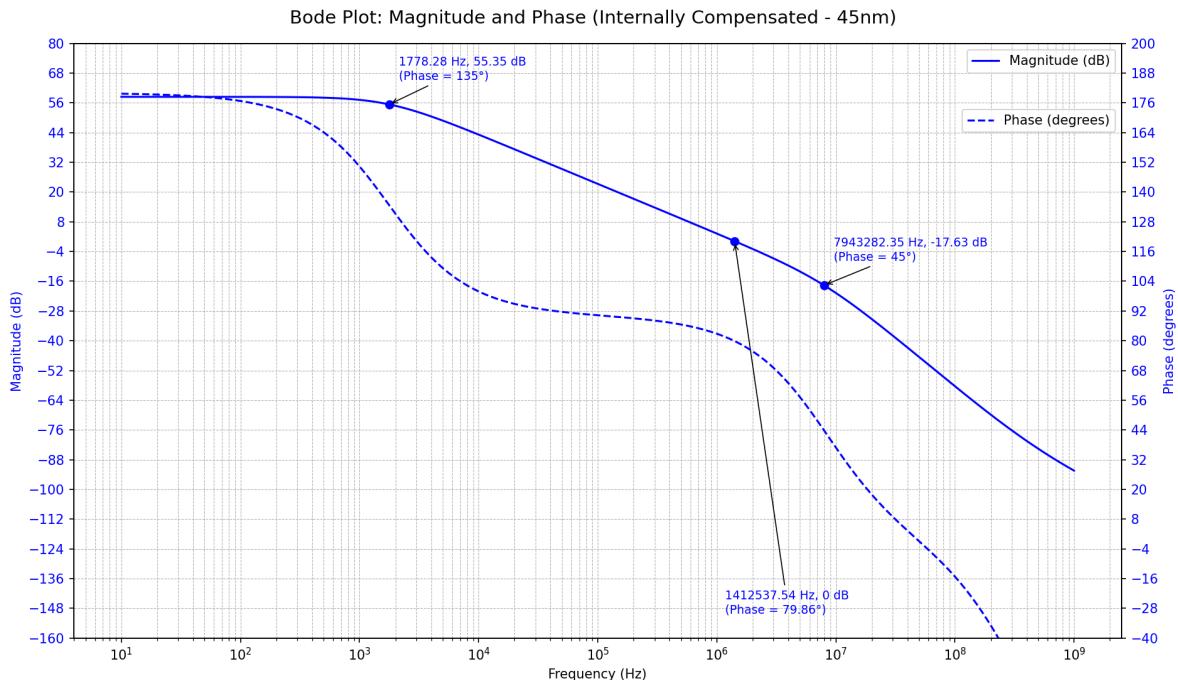


Figure 27: Magnitude and Phase Plot for Heavy Load - 45nm

Heavy Load (10mA) - 130nm:

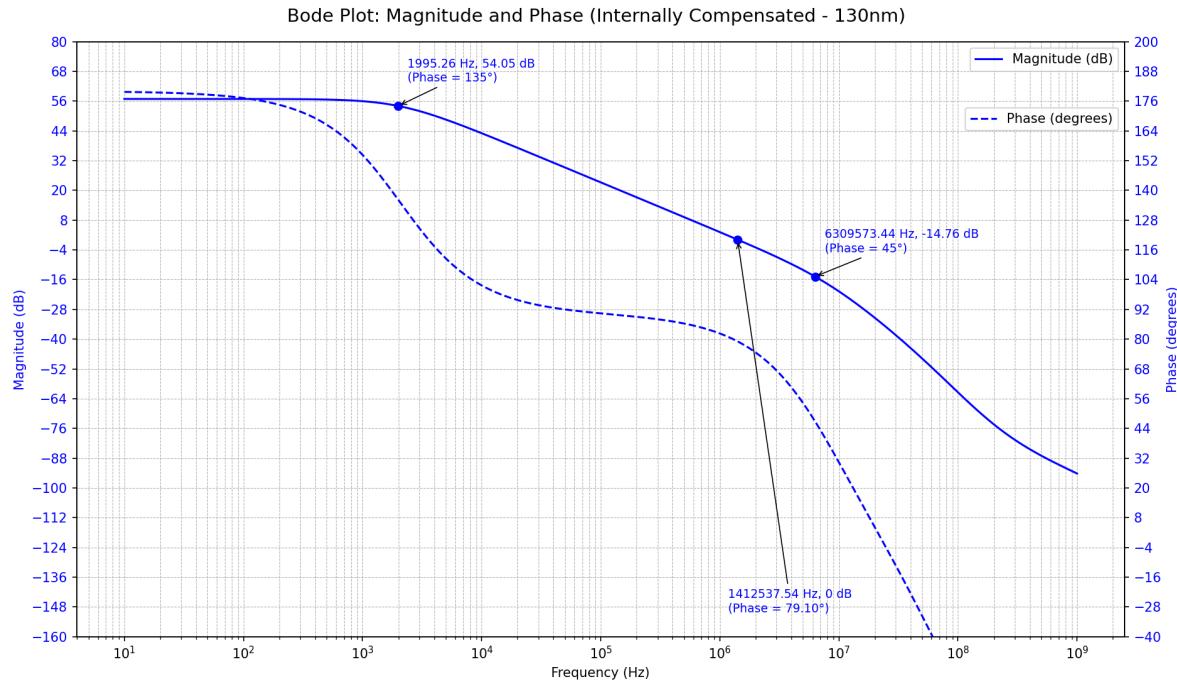


Figure 28: Magnitude and Phase Plot for Heavy Load - 130nm

Light Load (2mA) - 45nm:

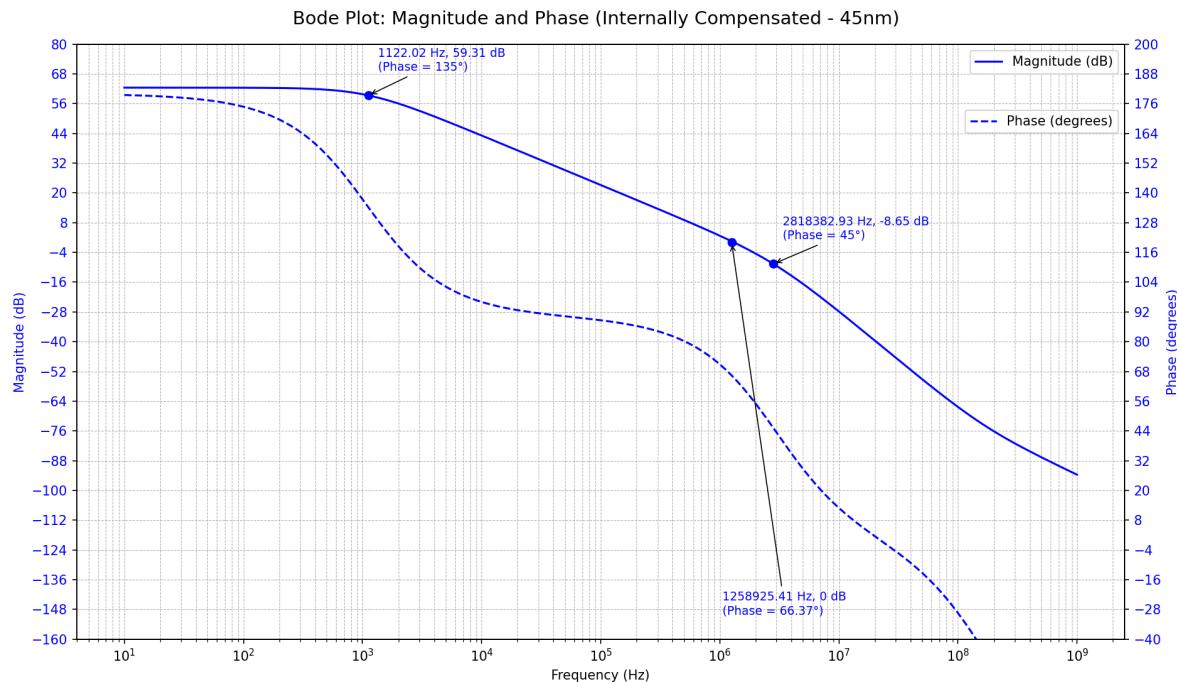


Figure 29: Magnitude and Phase Plot for Light Load - 45nm

Light Load (2mA) - 130nm:

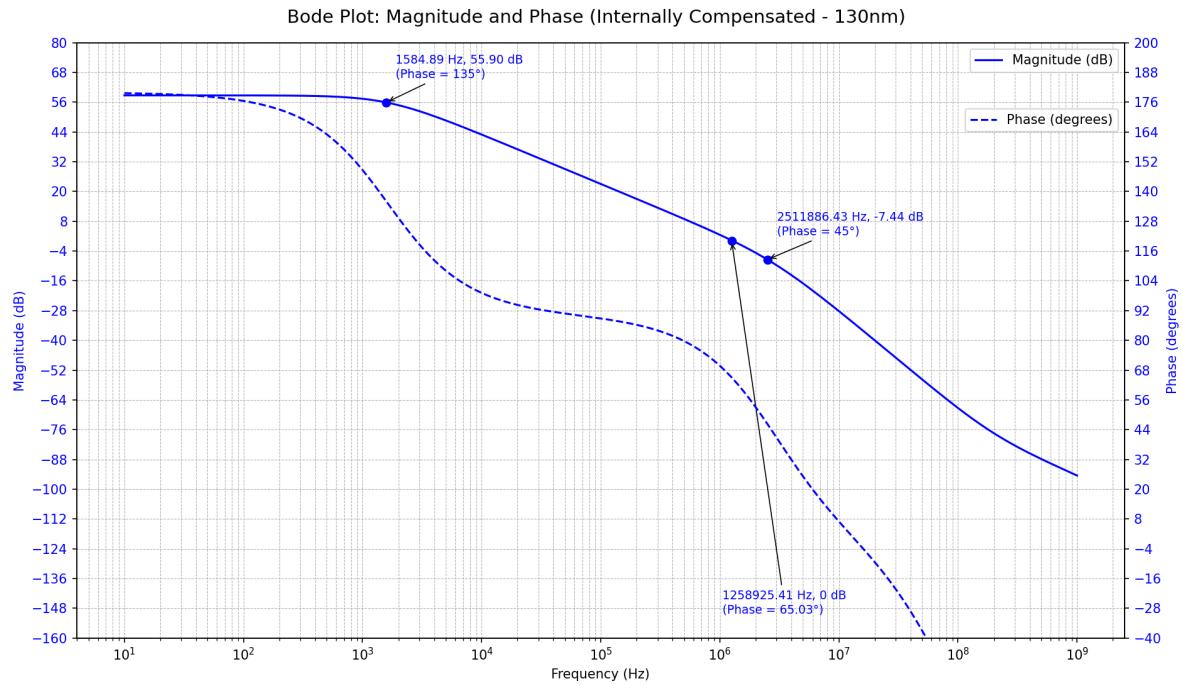


Figure 30: Magnitude and Phase Plot for Light Load - 130nm

From the above analysis we can see that the unity gain bandwidth is closer to the second pole for the heavy load case than the light load case. The parameters such as DC loop gain, pole location and phase margin for different configuration and technology nodes are listed in the table below.

Externally Compensated LDO

For 45nm

Table 4: Key Metrics under Heavy and Light Load Conditions

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	58.42	62.42
Unity Gain Bandwidth (kHz)	354.81	141.25
Phase Margin (degrees)	83.01	87.61
Pole 1 (Hz)	398.11	100
Pole 2 (MHz)	2.818	3.16

For 130nm

Table 5: Key Metrics under Heavy and Light Load Conditions

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	58.72	62.41
Unity Gain Bandwidth (kHz)	281.84	112.2
Phase Margin (degrees)	69.47	83.71
Pole 1 (Hz)	446.68	125.89
Pole 2 (MHz)	0.707	1

Internally Compensated LDO

For 45nm

Table 6: Key Metrics under Heavy and Light Load Conditions

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	58.42	62.45
Unity Gain Bandwidth (MHz)	1.41	1.26
Phase Margin (degrees)	79.86	66.37
Pole 1 (kHz)	1.77	1.122
Pole 2 (MHz)	7.943	2.818

For 130nm

Table 7: Key Metrics under Heavy and Light Load Conditions

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	56.88	58.75
Unity Gain Bandwidth (MHz)	1.41	1.26
Phase Margin (degrees)	79.10	65.03
Pole 1 (kHz)	1.99	1.584
Pole 2 (MHz)	6.3	2.51

6. PSRR Explanation

LDOs are essential components in the power supply of most ICs. They provide a ripple-free, stable fixed output voltage; isolating it from the input noise. An LDO has several important performance specifications and the power supply rejection ratio (PSRR) is one of them. PSRR is a quantitative measure of the attenuation of input ripples by the LDO at its output. These ripples can originate from various parts of the circuit, like DC/DC converters or shared power supplies of other circuit blocks. PSRR is expressed as $\text{PSRR} = 20\log(v_{\text{out}}/v_{\text{in}})$, where v_{out} and v_{in} refer to magnitudes of input and output ripples. In the below PSRR curve, the PSRR of LDO is divided into two distinct regions (region 1 and region 2). Region 1 covers the low and mid frequency range till the regulator bandwidth frequency (ω_{REG}), where PSRR primarily depends on the loop gain (LG) of the regulator. Region 2 starts after ω_{REG} , where PSRR is independent of LG and is dominated by output parasitics, PCB impedance, etc.

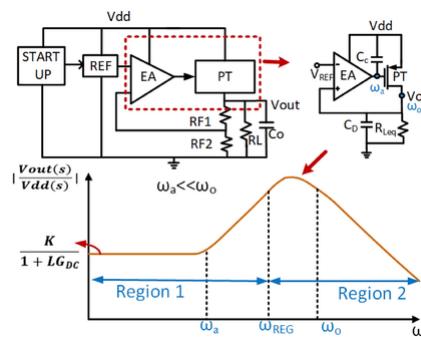


Figure 31: : LDO Block Diagram and PSRR Curve

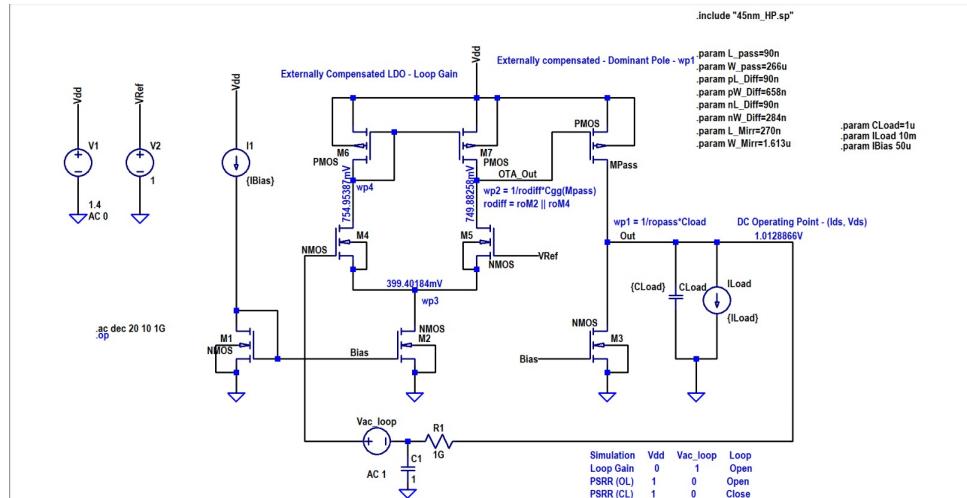


Figure 32: PSRR block diagram.

7. PSRR Simulation Results

Three schematics are created in LTSpice to calculate the three conditions as mentioned below:

Case 1 : Loop Gain Analysis

Case 2 : Open Loop PSRR Calculation

Case 3 : Closed Loop PSRR Calculation

For 45nm

Heavy Load (10mA)

Schematic

Case 1:- Loop gain analysis:-

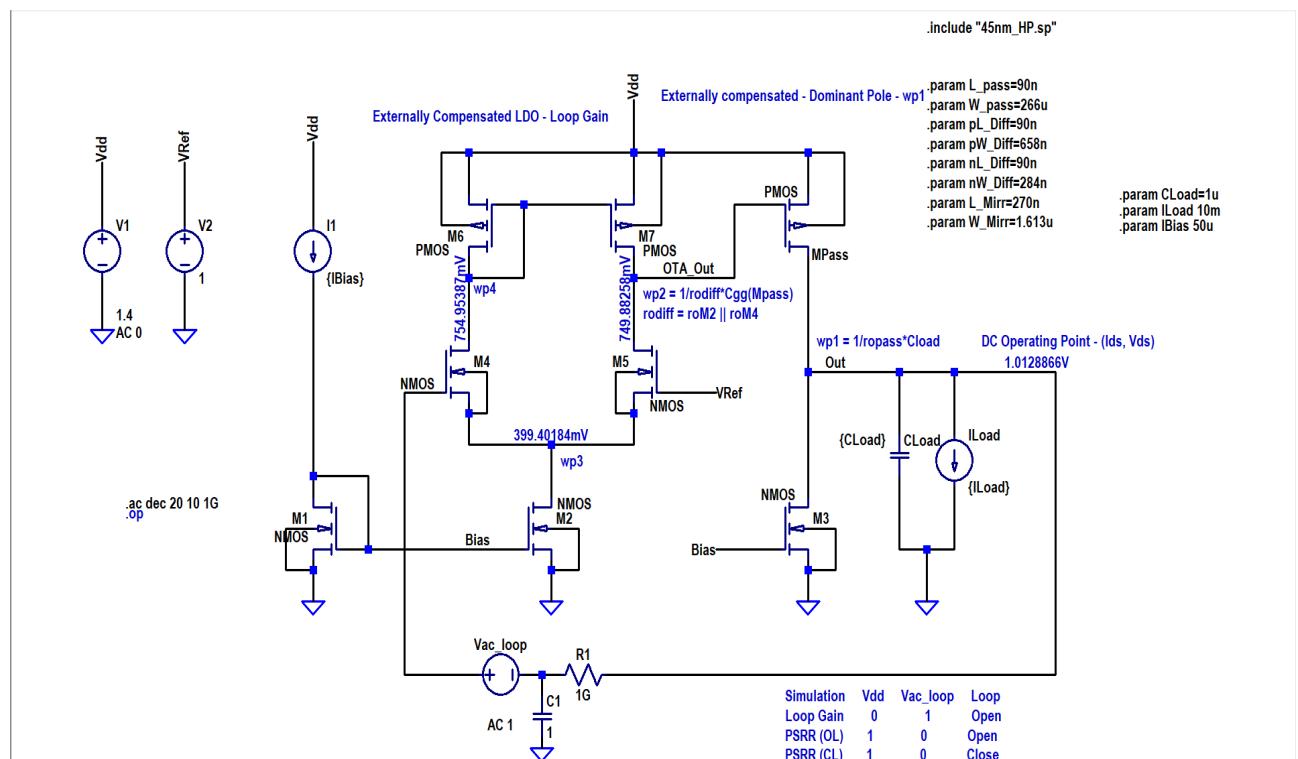


Figure 33: Schematic

Explanation of the artifact used:-

In order to calculate the loop gain we have given a RC circuit in the feedback loop alongwith a AC source with amplitude 1 (as we want to maintain an AC voltage of 1V) at the output. At the same time we also need to bias the circuit and provide a dc voltage to the gate of the nmos in the differential amplifier and for this we are giving the RC circuit which will prevent the flow of dc current to ground but will send any AC signal at the output to ground at high frequency. Also the drop across the resistor will be very less as we have given a very high resistance with very negligible current (since current

going into the gate of the mosfet is zero). Thus we will bias the circuit and also calculate the loop gain.

Output Log File:

```

LTspice 24.0.12 for Windows
Circuit: * C:\Users\karthik\OneDrive - iiit-b\ACMOS Project Files\Heavy Load\Externally_Compensated_45nm\External_45nm_LG.asc
Start Time: Sun Dec 8 19:59:50 2024
solver = Normal
Maximum thread count: 16
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
    --- BSIM4 MOSFETS ---
Name:      m4      m5      m2      m1      m3
Model:     nmos    nmos    nmos    nmos    nmos
Id:       2.47e-05  2.48e-05  4.94e-05  5.00e-05  5.08e-05
Vgs:       6.00e-01  6.01e-01  6.17e-01  6.17e-01  6.17e-01
Vds:       3.56e-01  3.50e-01  3.99e-01  6.17e-01  1.01e+00
Vbs:        0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00
Vth:       4.66e-01  4.66e-01  4.69e-01  4.69e-01  4.69e-01
Vdsat:     1.42e-01  1.43e-01  1.61e-01  1.61e-01  1.61e-01
Gm:        2.44e-04  2.44e-04  4.96e-04  5.02e-04  5.09e-04
Gds:       5.08e-06  5.16e-06  3.19e-06  2.30e-06  2.12e-06
Gmb:       5.62e-05  5.63e-05  1.16e-04  1.18e-04  1.20e-04
Cbd:       1.28e-16  1.29e-16  7.22e-16  6.88e-16  6.40e-16
Cbs:       2.27e-16  2.27e-16  1.29e-15  1.29e-15  1.29e-15

Name:      m6      m7      mpass
Model:     pmos    pmos    pmos
Id:      -2.47e-05 -2.47e-05 -1.01e-02
Vgs:      -6.45e-01 -6.45e-01 -6.50e-01
Vds:      -6.45e-01 -6.50e-01 -3.87e-01
Vbs:        0.00e+00  0.00e+00  0.00e+00
Vth:      -4.84e-01 -4.84e-01 -4.87e-01
Vdsat:     -1.76e-01 -1.76e-01 -1.78e-01
Gm:        2.45e-04  2.46e-04  9.88e-02
Gds:       4.95e-06  4.94e-06  2.52e-03
Gmb:       5.20e-05  5.20e-05  2.09e-02
Cbd:       2.79e-16  2.79e-16  1.19e-13
Cbs:       5.26e-16  5.26e-16  2.13e-13

Total elapsed time: 0.071 seconds.

```

Figure 34: Output Log

From the above file, it can be verified that all the devices are in saturation as follows:

Transistor Operating Regions Table

The table below summarizes the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	[h!]	Operating Region
m1	nmos	6.17E-01	6.17E-01	4.69E-01	1.48E-01		Saturation
m2	nmos	3.99E-01	6.17E-01	4.69E-01	1.48E-01		Saturation
m3	nmos	1.01E+00	6.17E-01	4.69E-01	1.48E-01		Saturation
m4	nmos	3.56E-01	6.00E-01	4.66E-01	1.34E-01		Saturation
m5	nmos	3.50E-01	6.01E-01	4.66E-01	1.35E-01		Saturation
m6	pmos	6.45E-01	6.45E-01	4.84E-01	1.61E-01		Saturation
m7	pmos	6.50E-01	6.45E-01	4.84E-01	1.61E-01		Saturation
mpass	pmos	3.87E-01	6.50E-01	4.87E-01	1.63E-01		Saturation

Table 8: Transistor Parameters and Operating Regions

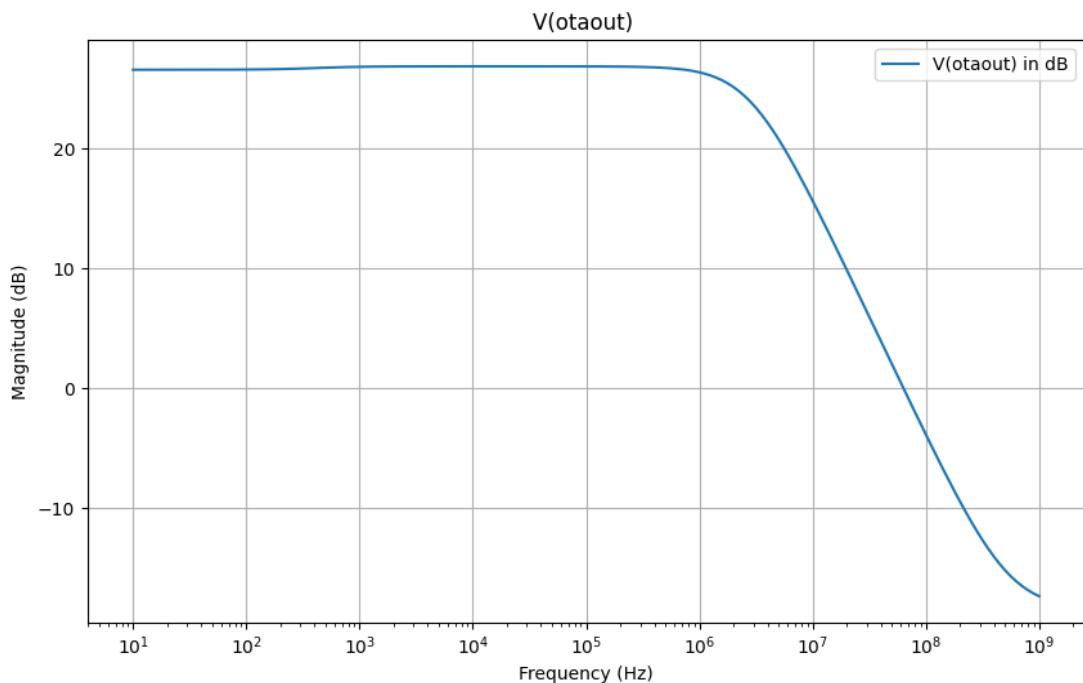
Output waveforms plot using Python:

Figure 35: OTA Output loop gain

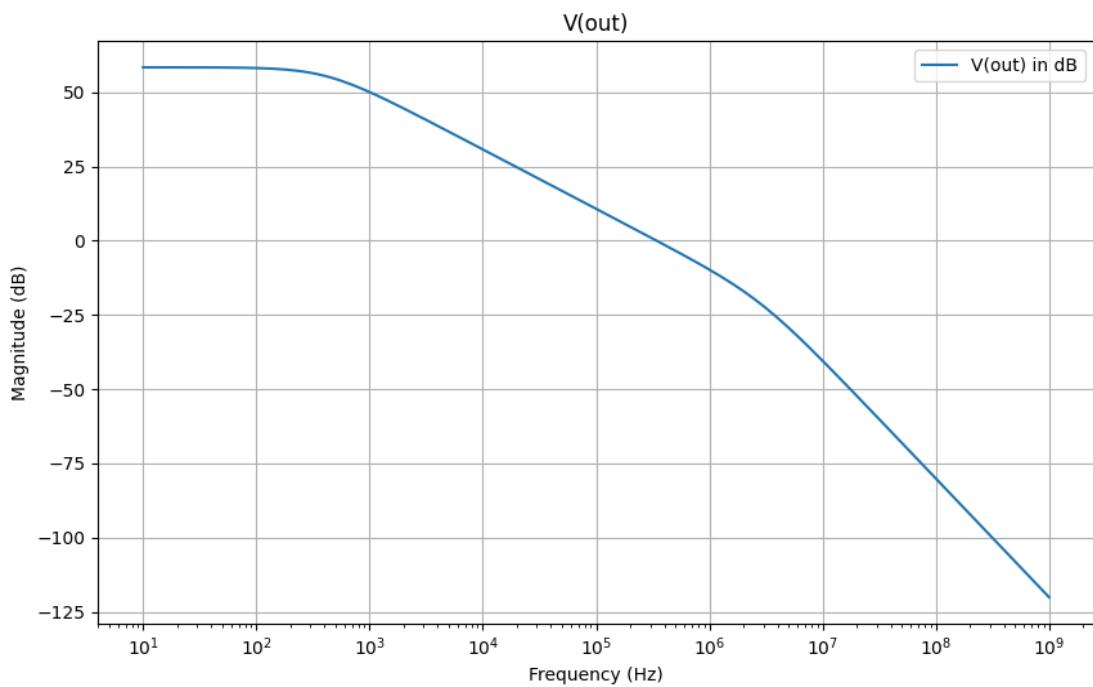


Figure 36: Output loop gain

Phase margin

The phase margin is 83.01

The output voltage (Loop gain) comes out to be 58.42 dB . The formula for loop gain is product of Adiff and Apass where Adiff is differential amplifier gain and Apass is the passfet gain.

Case 2:- Open Loop PSRR calculation

Schematic

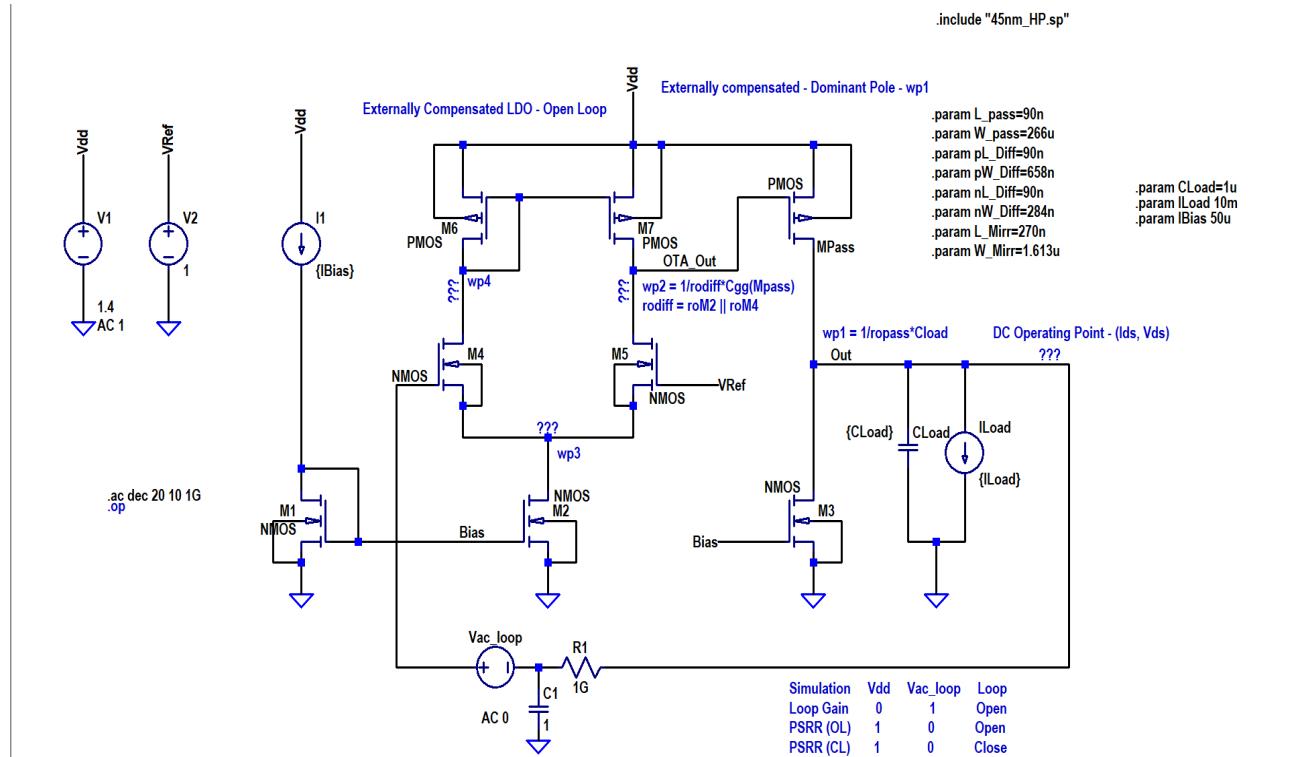


Figure 37: Schematic

Explanation of the artifact used:-

In order to calculate the open loop PSRR we need to send an AC signal from the source which in our case is V_{DD} . Here we are giving an AC 1 signal in the source. This signal is given to the source of the passfet and the source of pmos in the diffamp. We will ideally want very bad PSRR in the diffamp as we want the OTA output to have all the AC noise such that V_{sg} of pmos = 0 (small signal analysis). Thus all the noise will get rejected and we will get a noise free dc voltage at the output of the LDO. Here in order to calculate the open loop PSRR we have a RC circuit to bias the differential amplifier. You can see AC 0 in the circuit indicating that there is an open loop in the circuit . From here we have calculated the open loop PSRR in the circuit. Since there is no feedback in the circuit we can thus say that there will be noise at the output and thus the rejection will be very poor.

Output waveforms plot using Python:

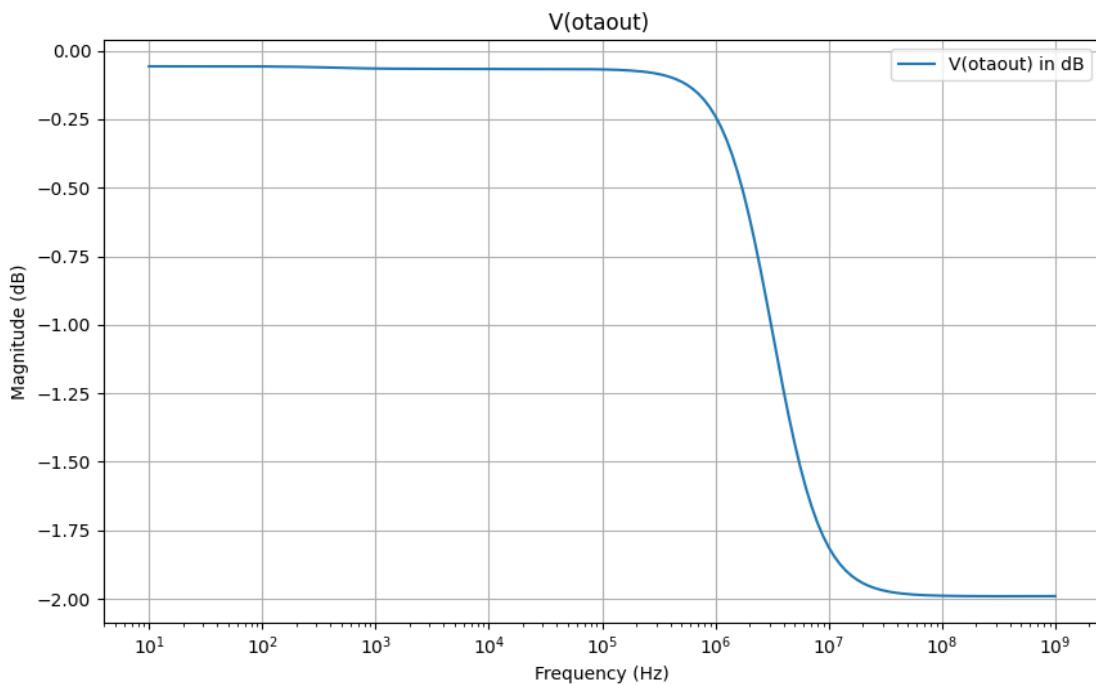


Figure 38: Vota for open loop psrr

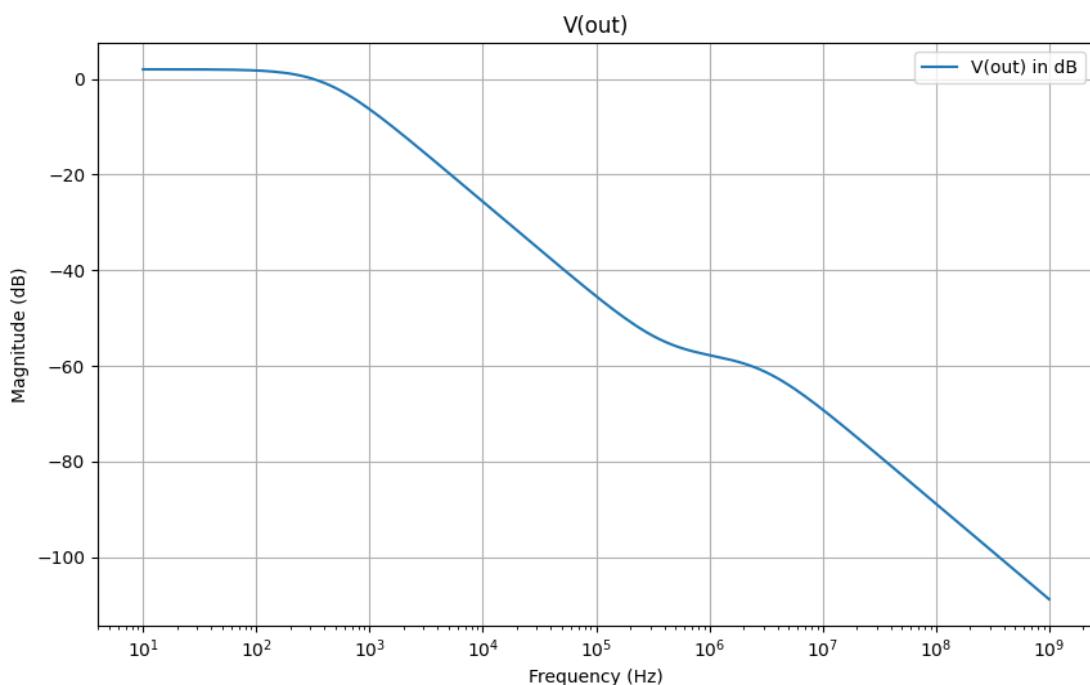


Figure 39: Vout for open loop psrr

Note:- Always observe the Vota output should be closer to 1v, the better it is for PSRR at the output as the Vsg value will be close to 0.

Case 3:- Closed Loop PSRR Calculation

Schematic

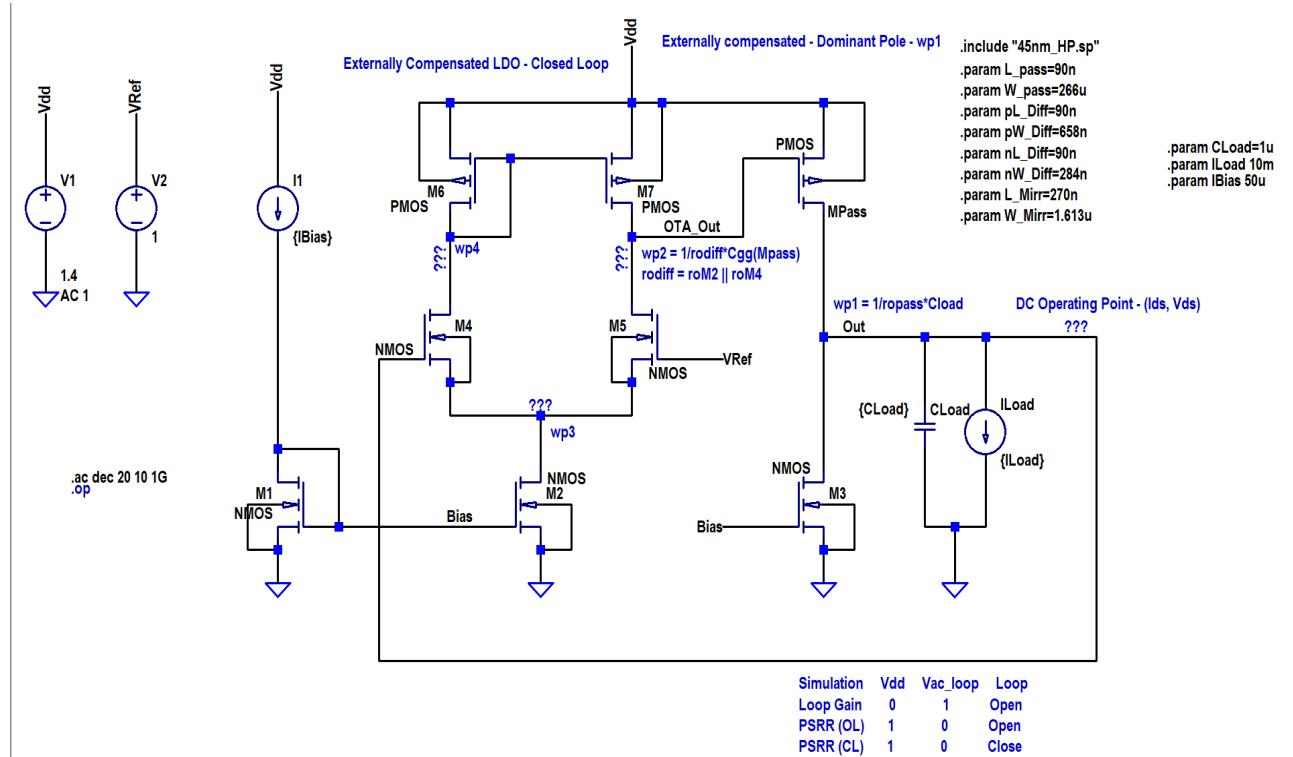


Figure 40: open loop psrr

Explanation of the artifact used:-

In this case we can see that we have given a AC source in the voltage source VDD . We want to see the negative feedback in the circuit due to which we will get the output voltage cancelled out (small signal analysis). Here we should observe a high PSRR according to our specifications (60db) which tells us that our sizing is perfect. For this circuit we have given a feedback from the output terminal to the input of the diffamp which indicates the feedback path.

Output waveforms plot using Python:

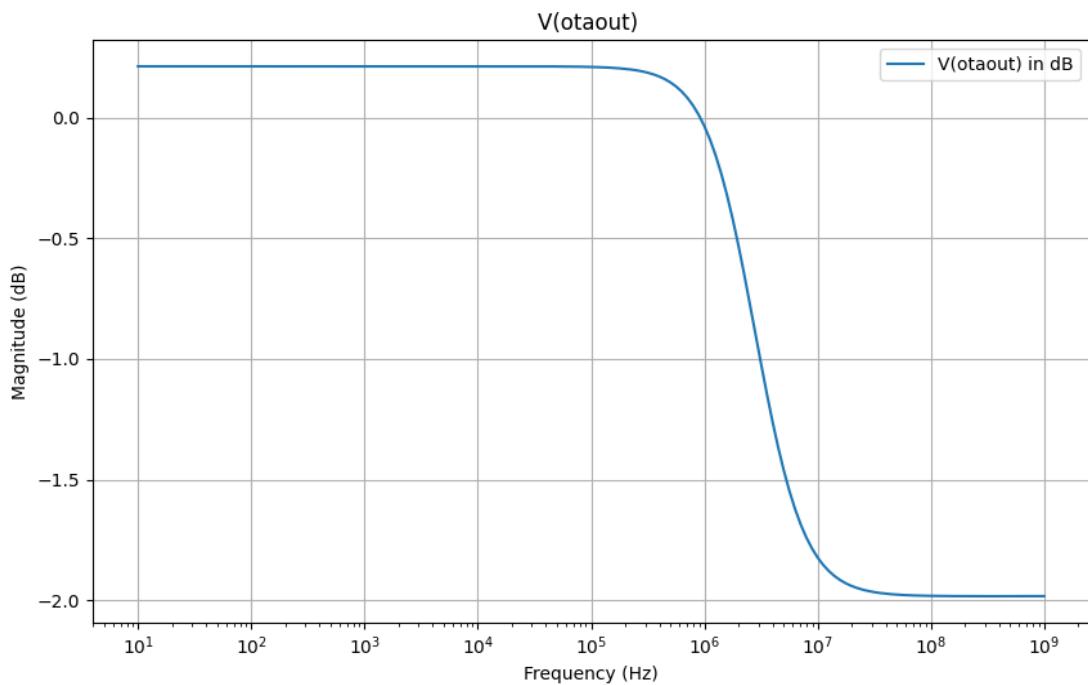


Figure 41: Vota for close loop psrr

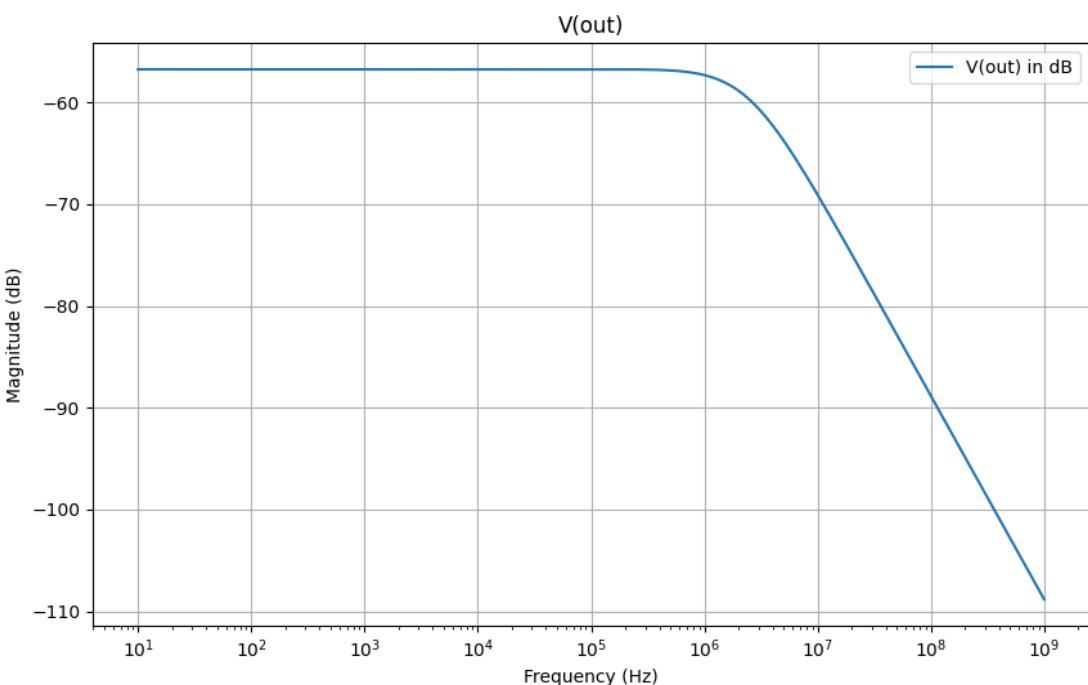


Figure 42: Vout for close loop psrr

Light Load (2ma)

Case 1:- Loop gain analysis

Schematic

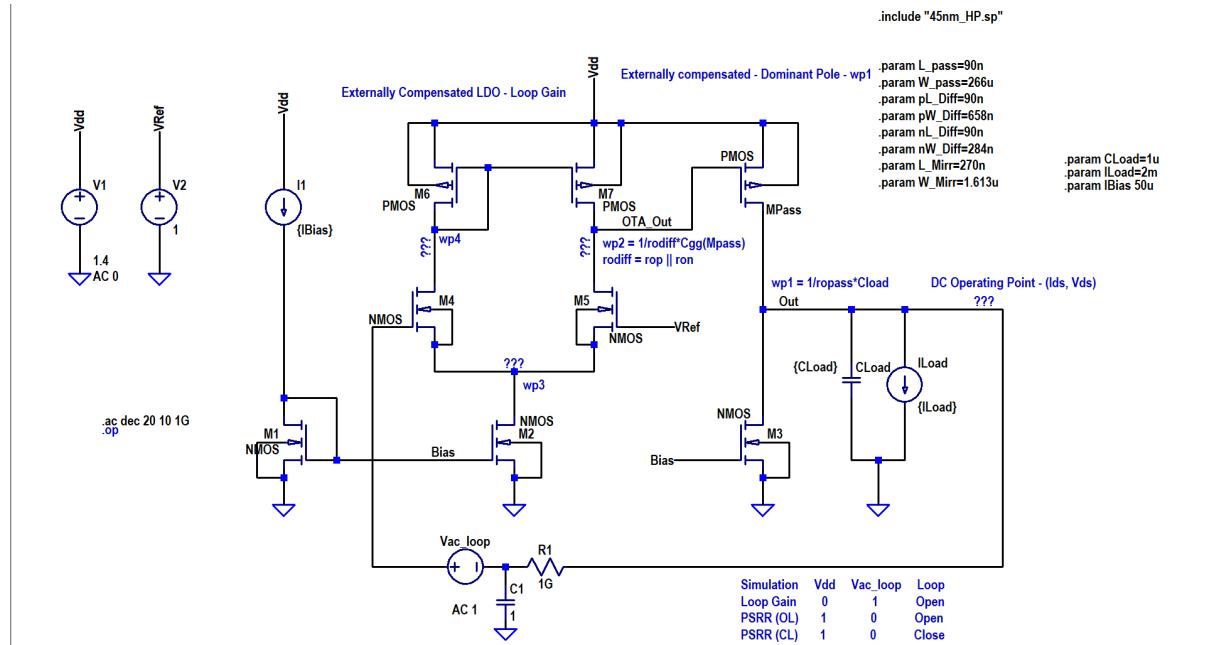


Figure 43: Schematic

Output Log File

Transistor Operating Regions Table

The table below summarizes the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
m1	nmos	6.17E-01	6.17E-01	4.69E-01	1.48E-01	Saturation
m2	nmos	4.03E-01	6.17E-01	4.69E-01	1.48E-01	Saturation
m3	nmos	1.02E+00	6.17E-01	4.69E-01	1.48E-01	Saturation
m4	nmos	3.51E-01	6.02E-01	4.66E-01	1.36E-01	Saturation
m5	nmos	4.65E-01	5.97E-01	4.65E-01	1.32E-01	Saturation
m6	pmos	6.46E-01	6.46E-01	4.84E-01	1.62E-01	Saturation
m7	pmos	5.32E-01	6.46E-01	4.85E-01	1.61E-01	Saturation
mpass	pmos	3.82E-01	5.32E-01	4.87E-01	4.50E-02	Saturation

Table 9: Transistor Parameters and Operating Regions

```

LTspice 24.0.12 for Windows
Circuit: * C:\Users\karthik\OneDrive - iiit-b\ACMOS Project Files\Light Load\Externally_Compensated_45nm\External_45nm_LG.asc
Start Time: Sun Dec 8 22:12:39 2024
solver = Normal
Maximum thread count: 16
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
    --- BSIM4 MOSFETS ---
Name:      m4      m5      m2      m1      m3
Model:     nmos    nmos    nmos    nmos    nmos
Id: 2.50e-05 2.44e-05 4.94e-05 5.00e-05 5.09e-05
Vgs: 6.02e-01 5.97e-01 6.17e-01 6.17e-01 6.17e-01
Vds: 3.51e-01 4.65e-01 4.03e-01 6.17e-01 1.02e+00
Vbs: 0.00e+00 0.00e+00 0.00e+00 0.00e+00 0.00e+00
Vth: 4.66e-01 4.65e-01 4.69e-01 4.69e-01 4.69e-01
Vdsat: 1.43e-01 1.41e-01 1.61e-01 1.61e-01 1.61e-01
Gm: 2.45e-04 2.44e-04 4.96e-04 5.02e-04 5.10e-04
Gds: 5.21e-06 4.33e-06 3.15e-06 2.30e-06 2.13e-06
Gmb: 5.65e-05 5.63e-05 1.16e-04 1.18e-04 1.20e-04
Cbd: 1.29e-16 1.25e-16 7.21e-16 6.88e-16 6.40e-16
Cbs: 2.27e-16 2.27e-16 1.29e-15 1.29e-15 1.29e-15

Name:      m6      m7      mpss
Model:     pmos    pmos    pmos
Id: -2.50e-05 -2.44e-05 -2.05e-03
Vgs: -6.46e-01 -6.46e-01 -5.32e-01
Vds: -6.46e-01 -5.32e-01 -3.82e-01
Vbs: 0.00e+00 0.00e+00 0.00e+00
Vth: -4.84e-01 -4.85e-01 -4.87e-01
Vdsat: -1.77e-01 -1.76e-01 -9.51e-02
Gm: 2.47e-04 2.43e-04 3.58e-02
Gds: 4.99e-06 5.19e-06 6.59e-04
Gmb: 5.24e-05 5.14e-05 7.38e-03
Cbd: 2.79e-16 2.86e-16 1.20e-13
Cbs: 5.26e-16 5.26e-16 2.13e-13

Total elapsed time: 0.065 seconds.

```

Figure 44: Output Log

Output waveforms plot using Python:

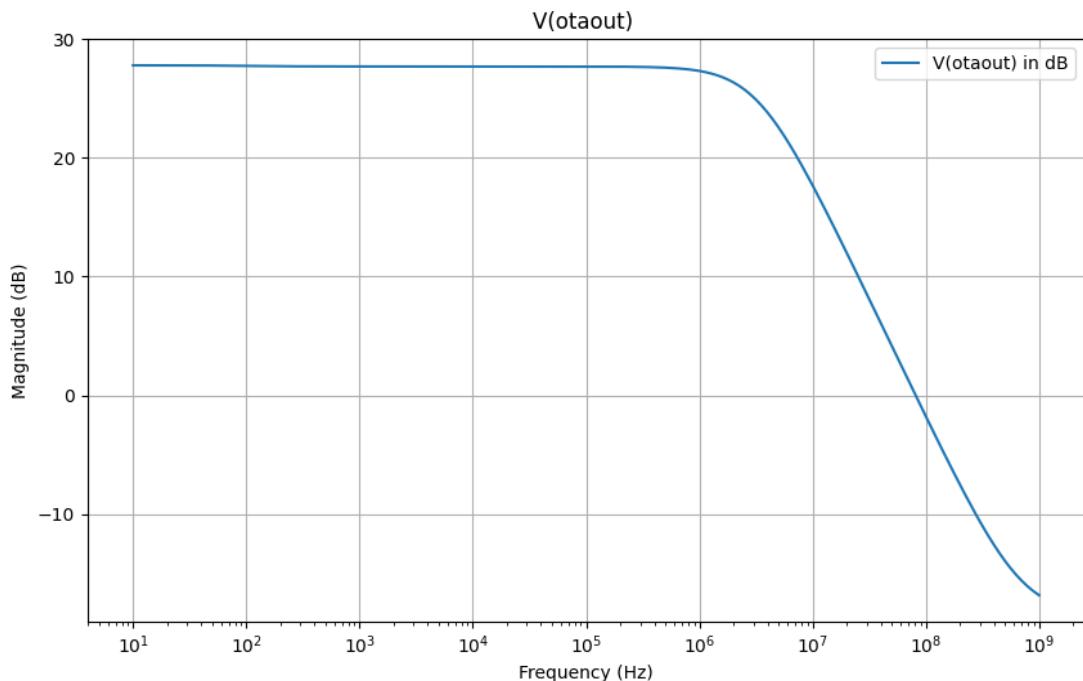


Figure 45: Vota for loop gain

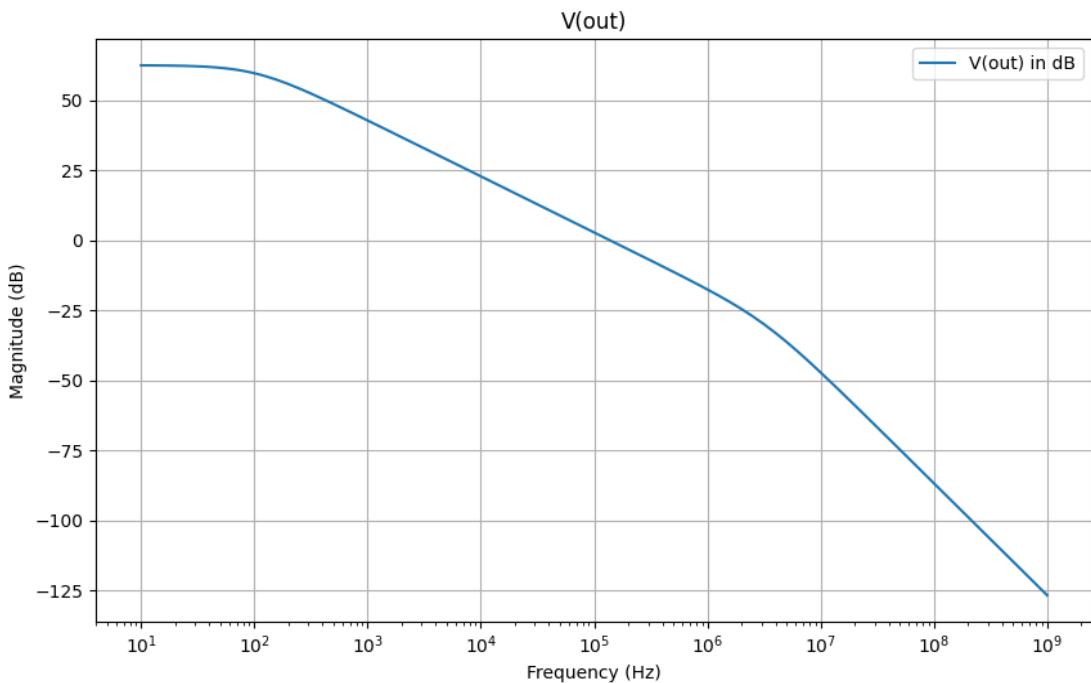


Figure 46: Vout for loop gain

The phase margin obtained is 87.61 degrees. The loop gain is around 62.42dB. The phase margin is more than that of the value obtained for heavy load. Thus proving the point that for light load we get a better phase margin as the 1st pole and the 2nd pole are far apart.

Case 2:- Open Loop PSRR calculation

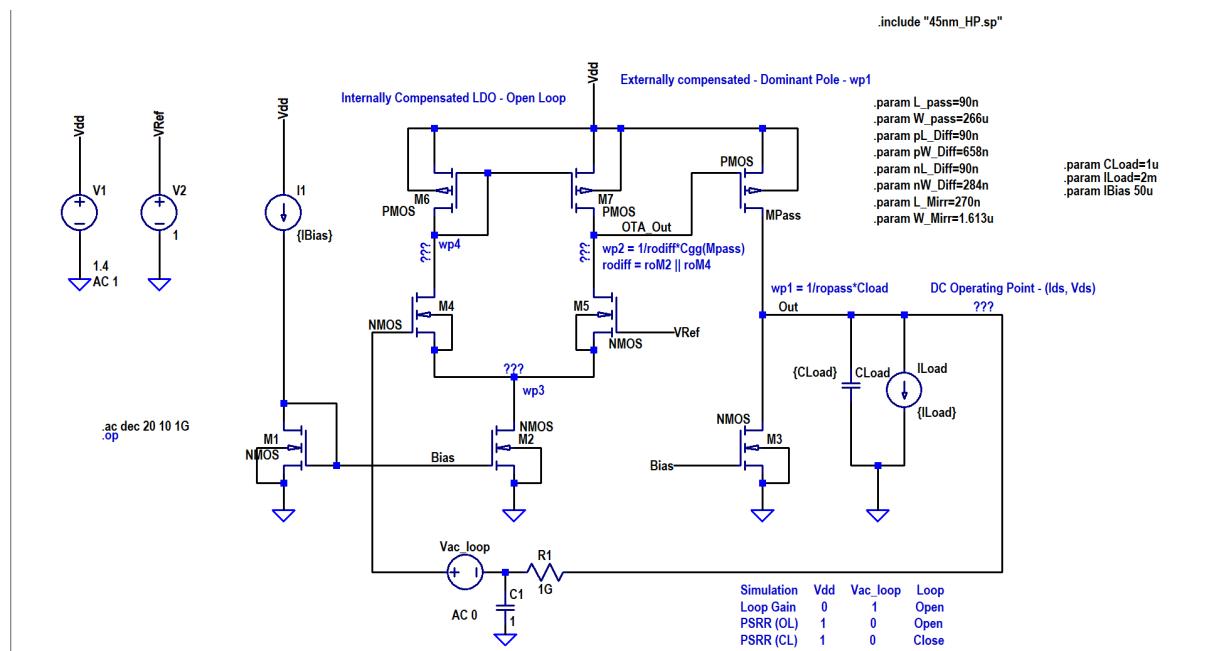


Figure 47: Schematic

Output waveforms plot using Python:

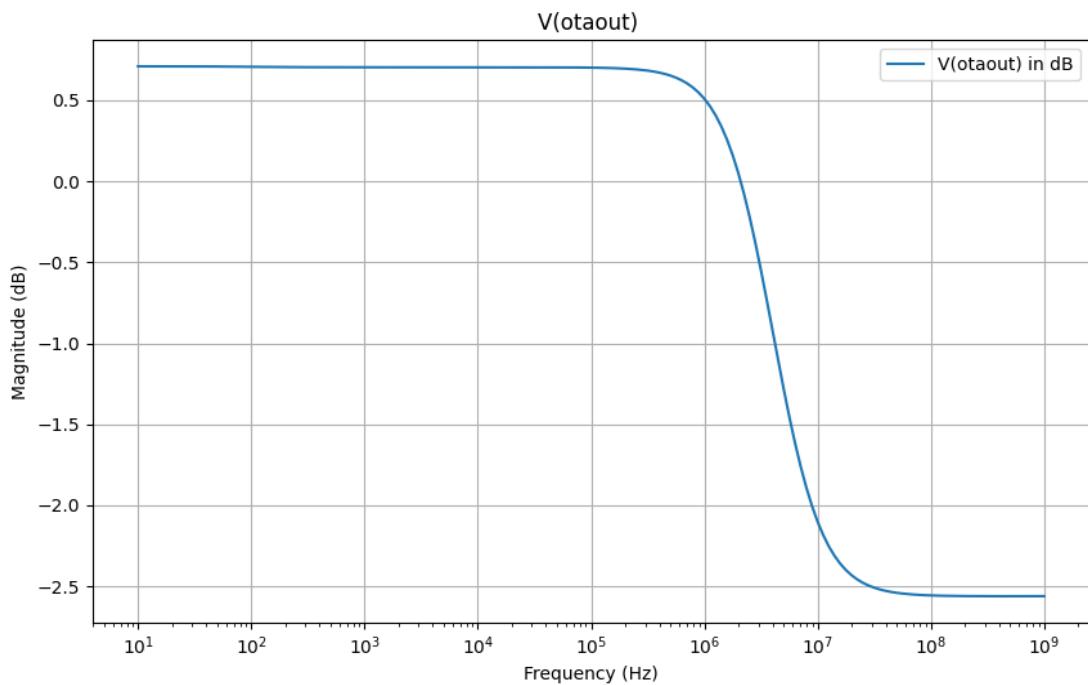


Figure 48: Vota for Open loop psrr

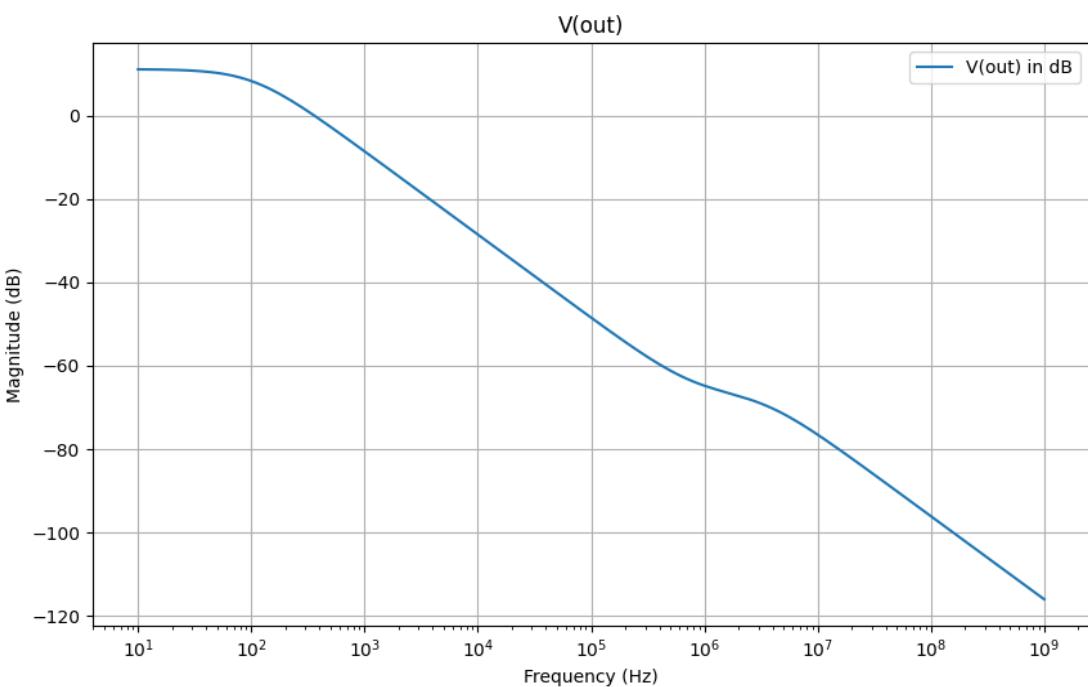


Figure 49: Vout for Open loop psrr

Case 3:- Closed loop PSRR calculation

Schematic

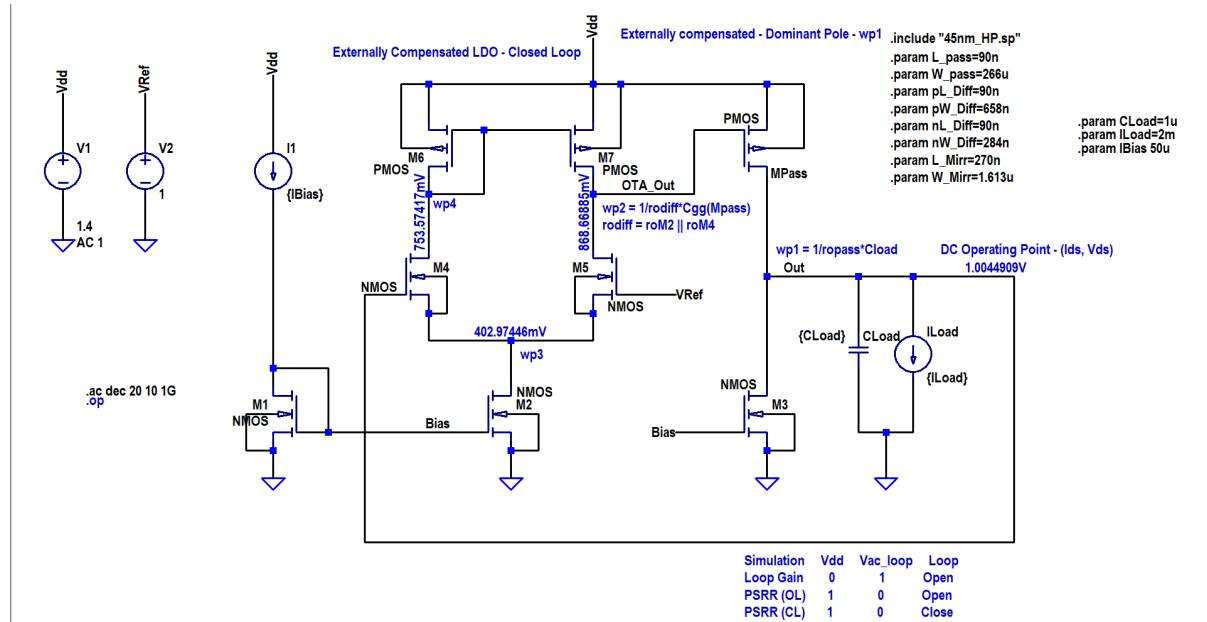


Figure 50: Schematic

Output waveforms plot using Python:

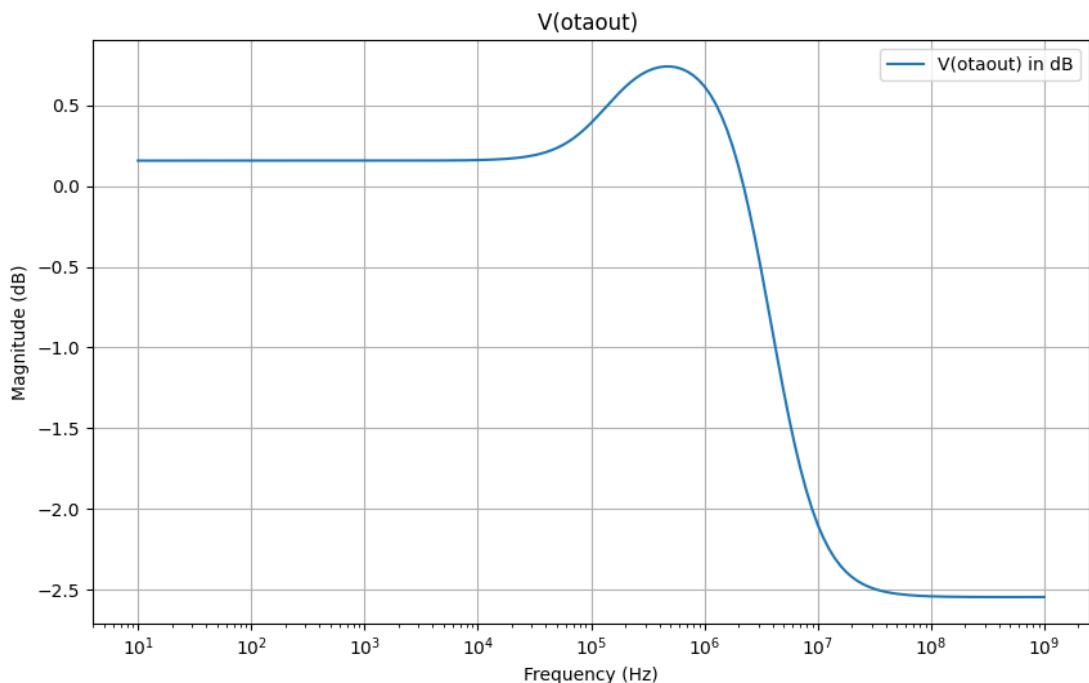


Figure 51: Vota for close loop gain

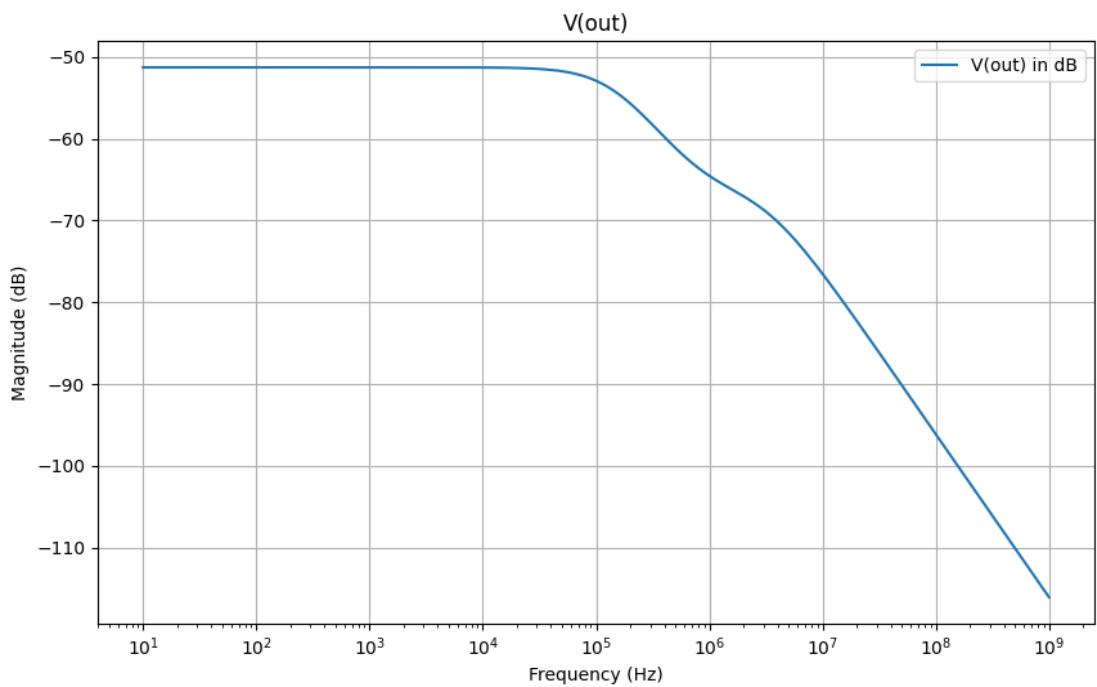


Figure 52: V_{out} for close loop gain

8. Transient Simulation Results

We have given a pulse at the load with a rise time and fall time of 1u. Also the period of the pulse is 10m with a 50% duty cycle. From the below figure we can understand that the output is able to settle within the specified range of time. We are not able to observe any overshoot or undershoot in the output.

Schematic:-

Output waveform plots using Python:

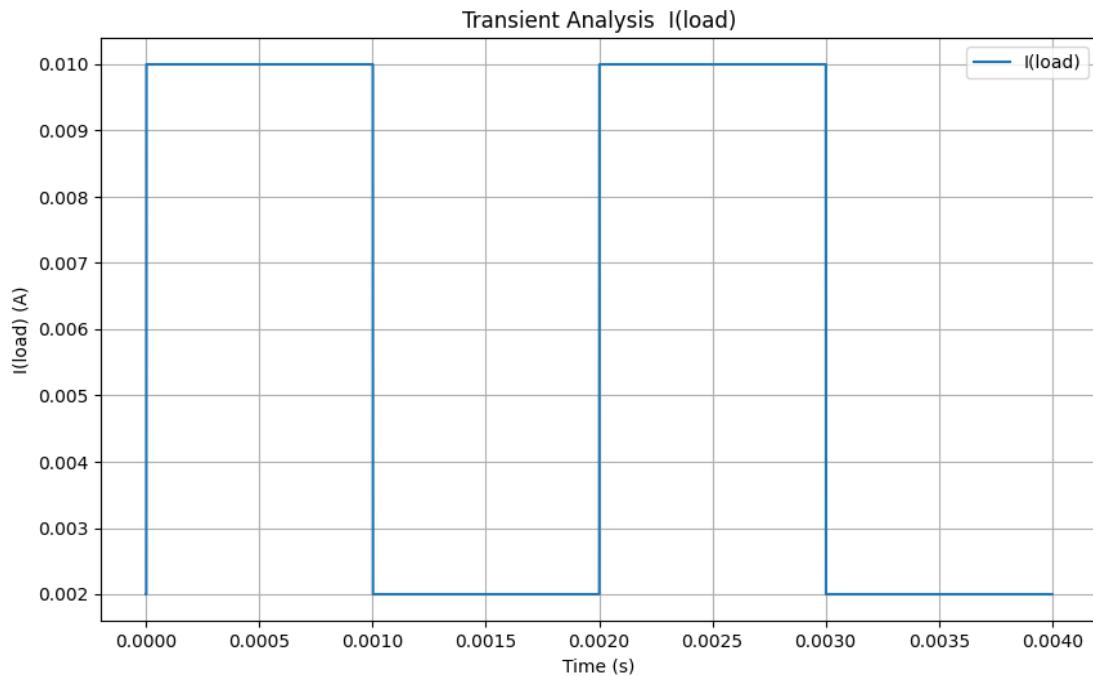
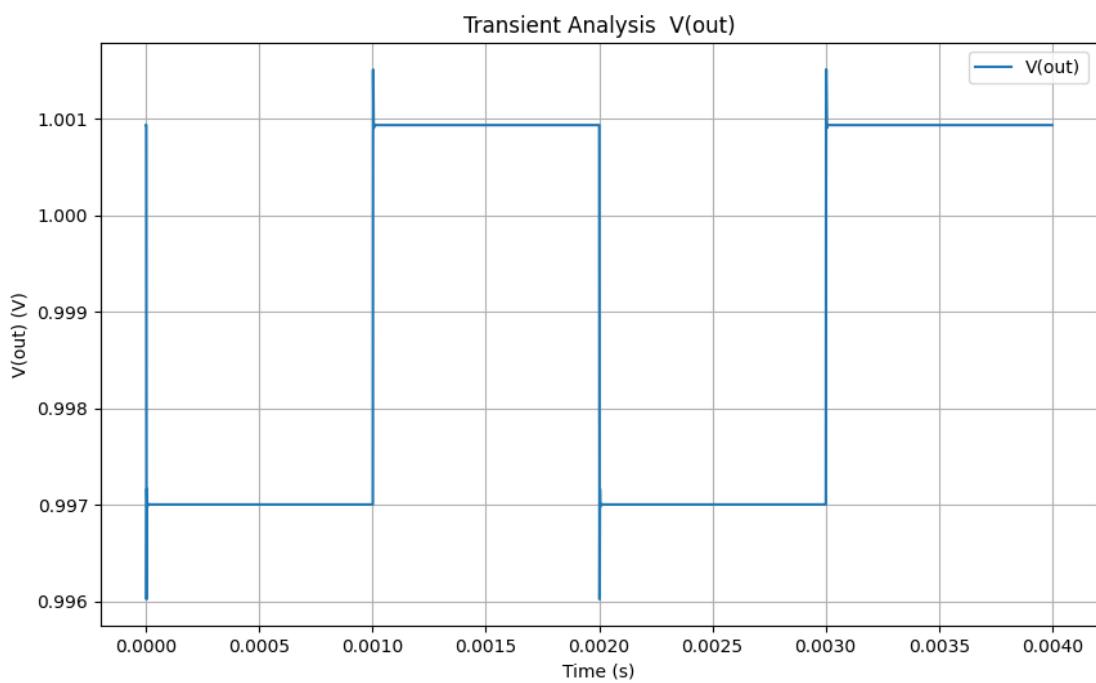


Figure 53: I(load)

Figure 54: $V(\text{out})$

9. Simulation vs. Hand Calculations

For Passfet HEAVY LOAD

Hand Calculation

- $r_o = 500 \Omega$
- $g_m = 0.1 \text{ A/V}$
- $W_{p1} = 2\text{k}$
- $f_{p1} = 318.3\text{Hz}$
- $g_m r_o = 50$
- $C_L = 1\text{u}$
- $C_{gg} = 0.585p$

Pole location comparison for hand calculation vs simulation result:

Table 10: Hand Calculation vs Simulation Results

Parameter	Hand Calculation	Simulation Result	% Error Percentage
f_{p1}	318.3Hz	398.11Hz	20.04%
f_{p2}	3.34MHz	2.82MHz	18.44%
f_{ugb}	318.3kHz	354.8kHz	10.29%

Name	m1	m2	m3	m4	m5	m6	m7	mpass
Model	nmos	nmos	nmos	nmos	nmos	pmos	pmos	pmos
Id	5.00E-05	4.94E-05	5.08E-05	2.47E-05	2.48E-05	-2.47E-05	-2.47E-05	-1.01E-02
Vgs	6.17E-01	6.17E-01	6.17E-01	6.00E-01	6.01E-01	-6.45E-01	-6.45E-01	-6.50E-01
Vds	6.17E-01	3.99E-01	1.01E+00	3.56E-01	3.50E-01	-6.45E-01	-6.50E-01	-3.87E-01
Vbs	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth	4.69E-01	4.69E-01	4.69E-01	4.66E-01	4.66E-01	-4.84E-01	-4.84E-01	-4.87E-01
Vdsat	1.61E-01	1.61E-01	1.61E-01	1.42E-01	1.43E-01	-1.76E-01	-1.76E-01	-1.78E-01
Gm	5.02E-04	4.96E-04	5.09E-04	2.44E-04	2.44E-04	2.45E-04	2.46E-04	9.88E-02
Gds	2.30E-06	3.19E-06	2.12E-06	5.08E-06	5.16E-06	4.95E-06	4.94E-06	2.52E-03
Gmb	1.18E-04	1.16E-04	1.20E-04	5.62E-05	5.63E-05	5.20E-05	5.20E-05	2.09E-02
Cbd	6.88E-16	7.22E-16	6.40E-16	1.28E-16	1.29E-16	2.79E-16	2.79E-16	1.19E-13
Cbs	1.29E-15	1.29E-15	1.29E-15	2.27E-16	2.27E-16	5.26E-16	5.26E-16	2.13E-13
ro	4.35E+05	3.13E+05	4.72E+05	1.97E+05	1.94E+05	2.02E+05	2.02E+05	3.97E+02
gmro	2.18E+02	1.55E+02	2.40E+02	4.80E+01	4.73E+01	4.95E+01	4.98E+01	3.92E+01

Table 11: Transistor Parameters Table

For Passfet LIGHT LOAD

Hand Calculation

- $r_o = 2500 \Omega$

- $g_m = 0.02 \text{ A/V}$
- $W_{p1} = 400$
- f_{p1} (first pole location) = 83.661Hz
- $g_m r_o = 50$
- $C_L = 1u$
- $C_{gg} = 0.1136p$

Table 12: Hand Calculation vs Simulation Results

Parameter	Hand Calculation	Simulation Result	% Error Percentage
f_{p1}	83.661Hz	100Hz	16.34%
f_{p2}	4.2MHz	3.16MHz	24.76%
f_{ugb}	83.661kHz	141.25kHz	40.77%

Name	m1	m2	m3	m4	m5	m6	m7	mpass
Model	nmos	nmos	nmos	nmos	nmos	pmos	pmos	pmos
Id	5.00E-05	4.94E-05	5.09E-05	2.50E-05	2.44E-05	-2.50E-05	-2.44E-05	-2.05E-03
Vgs	6.17E-01	6.17E-01	6.17E-01	6.02E-01	5.97E-01	-6.46E-01	-6.46E-01	-5.32E-01
Vds	6.17E-01	4.03E-01	1.02E+00	3.51E-01	4.65E-01	-6.46E-01	-5.32E-01	-3.82E-01
Vbs	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth	4.69E-01	4.69E-01	4.69E-01	4.66E-01	4.65E-01	-4.84E-01	-4.85E-01	-4.87E-01
Vdsat	1.61E-01	1.61E-01	1.61E-01	1.43E-01	1.41E-01	-1.77E-01	-1.76E-01	-9.51E-02
Gm	5.02E-04	4.96E-04	5.10E-04	2.45E-04	2.44E-04	2.47E-04	2.43E-04	3.58E-02
Gds	2.30E-06	3.15E-06	2.13E-06	5.21E-06	4.33E-06	4.99E-06	5.19E-06	6.59E-04
Gmb	1.18E-04	1.16E-04	1.20E-04	5.65E-05	5.63E-05	5.24E-05	5.14E-05	7.38E-03
Cbd	6.88E-16	7.21E-16	6.40E-16	1.29E-16	1.25E-16	2.79E-16	2.86E-16	1.20E-13
Cbs	1.29E-15	1.29E-15	1.29E-15	2.27E-16	2.27E-16	5.26E-16	5.26E-16	2.13E-13
ro	4.35E+05	3.17E+05	4.69E+05	1.92E+05	2.31E+05	2.00E+05	1.93E+05	1.52E+03
gmro	2.18E+02	1.57E+02	2.39E+02	4.70E+01	5.64E+01	4.95E+01	4.68E+01	5.43E+01

Table 13: Transistor Parameters Table

Internally Compensated LDO

1. Specifications

Table 14: Specifications Summary

Parameter	Value
Vin	1.4V
Vout	1V
PSRR	60dB
Iload (min)	2mA
Iload (max)	10mA
Cload	2nF
Iquiescent	50uA
Transient duration	1u

We have made three schematics in LTSpice to calculate the three conditions as shown below:

Case 1 : Loop Gain Analysis

Case 2 : Open Loop PSRR Calculation

Case 3 : Closed Loop PSRR Calculation

For 45nm

Light Load (2mA)

Schematic

Case 1:- Loop gain analysis:

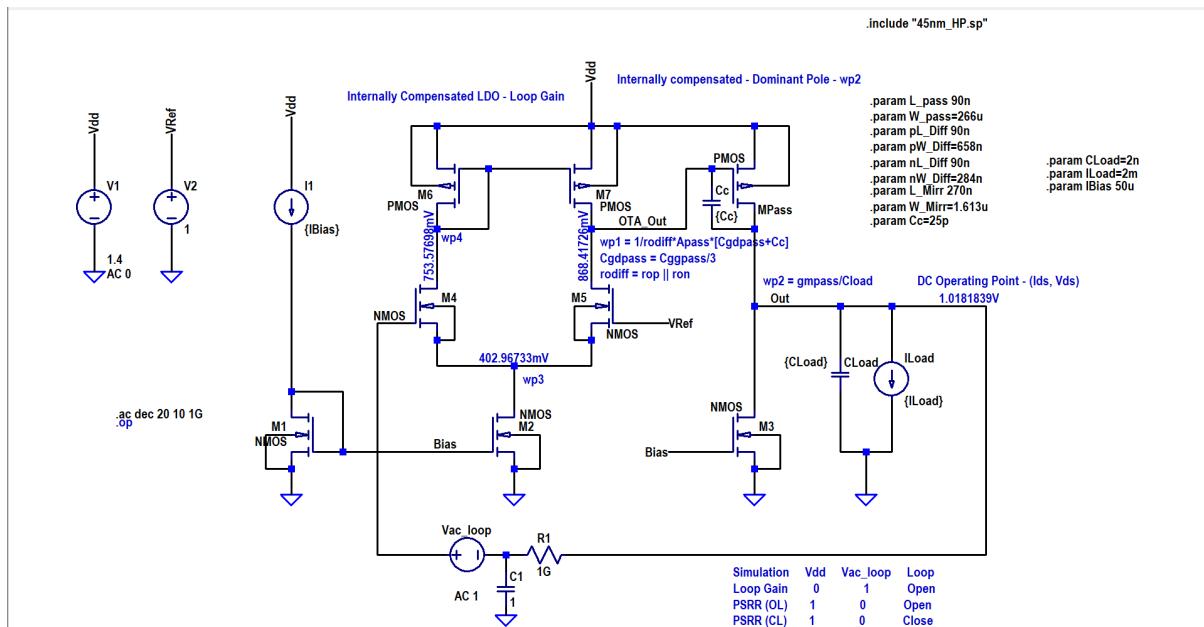


Figure 55: Schematic

Output Log File:

```

LTspice 24.0.12 for Windows
Circuit: * C:\Users\karthik\OneDrive - iit-b\ACMOS Project Files\Light Load\Internally_Compensated_45nm\Internal_45nm_LG.asc
Start Time: Sun Dec 8 23:43:46 2024
solver = Normal
Maximum thread count: 16
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
    --- BSIM4 MOSFETS ---
Name:      m4      m5      m2      m1      m3
Model:     nmos    nmos    nmos    nmos    nmos
Id:        2.50e-05  2.44e-05  4.94e-05  5.00e-05  5.09e-05
Vgs:       6.02e-01  5.97e-01  6.17e-01  6.17e-01  6.17e-01
Vds:       3.51e-01  4.65e-01  4.03e-01  6.17e-01  1.02e+00
Vbs:       0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00
Vth:       4.66e-01  4.65e-01  4.69e-01  4.69e-01  4.69e-01
Vdsat:    1.43e-01  1.41e-01  1.61e-01  1.61e-01  1.61e-01
Gm:        2.45e-04  2.44e-04  4.96e-04  5.02e-04  5.10e-04
Gds:       5.21e-06  4.33e-06  3.15e-06  2.30e-06  2.13e-06
Gmb:       5.65e-05  5.63e-05  1.16e-04  1.18e-04  1.20e-04
Cbd:       1.29e-16  1.25e-16  7.21e-16  6.88e-16  6.40e-16
Cbs:       2.27e-16  2.27e-16  1.29e-15  1.29e-15  1.29e-15

Name:      m6      m7      mpass
Model:     pmos    pmos    pmos
Id:        -2.50e-05  -2.44e-05  -2.05e-03
Vgs:      -6.46e-01  -6.46e-01  -5.32e-01
Vds:      -6.46e-01  -5.32e-01  -3.82e-01
Vbs:       0.00e+00  0.00e+00  0.00e+00
Vth:      -4.84e-01  -4.85e-01  -4.87e-01
Vdsat:   -1.77e-01  -1.76e-01  -9.51e-02
Gm:        2.47e-04  2.43e-04  3.58e-02
Gds:       4.99e-06  5.19e-06  6.59e-04
Gmb:       5.24e-05  5.14e-05  7.38e-03
Cbd:       2.79e-16  2.86e-16  1.20e-13
Cbs:       5.26e-16  5.26e-16  2.13e-13

Total elapsed time: 0.185 seconds.

```

Figure 56: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

Transistor	Type	Vds (V)	Vgs/Vsg (V)	Vt (V)	Vgs/Vsg-Vth (V)	Operating Region
m1	nmos	6.17E-01	6.17E-01	4.69E-01	1.48E-01	Saturation
m2	nmos	4.03E-01	6.17E-01	4.69E-01	1.48E-01	Saturation
m3	nmos	1.02E+00	6.17E-01	4.69E-01	1.48E-01	Saturation
m4	nmos	3.51E-01	6.02E-01	4.66E-01	1.36E-01	Saturation
m5	nmos	4.65E-01	5.97E-01	4.65E-01	1.32E-01	Saturation
m6	pmos	6.46E-01	6.46E-01	4.84E-01	1.62E-01	Saturation
m7	pmos	5.32E-01	6.46E-01	4.85E-01	1.61E-01	Saturation
mpass	pmos	3.82E-01	5.32E-01	4.87E-01	4.50E-02	Saturation

Table 15: Transistor Data

Output waveforms plot using Python:

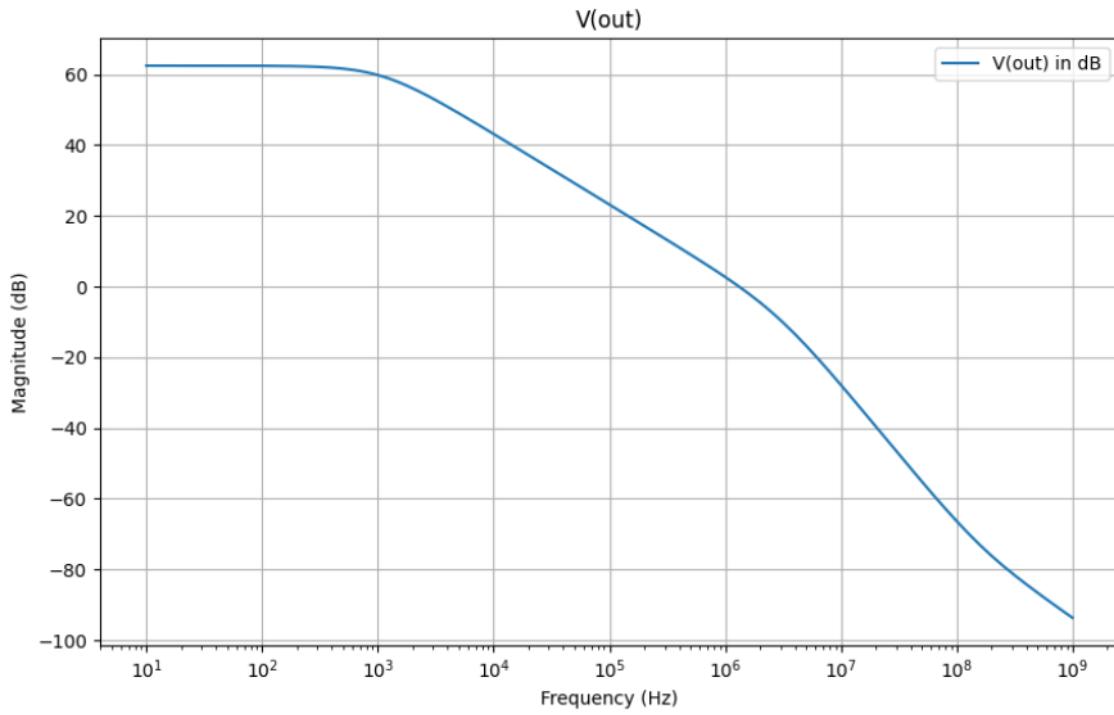


Figure 57: V_{out} for Loop Gain

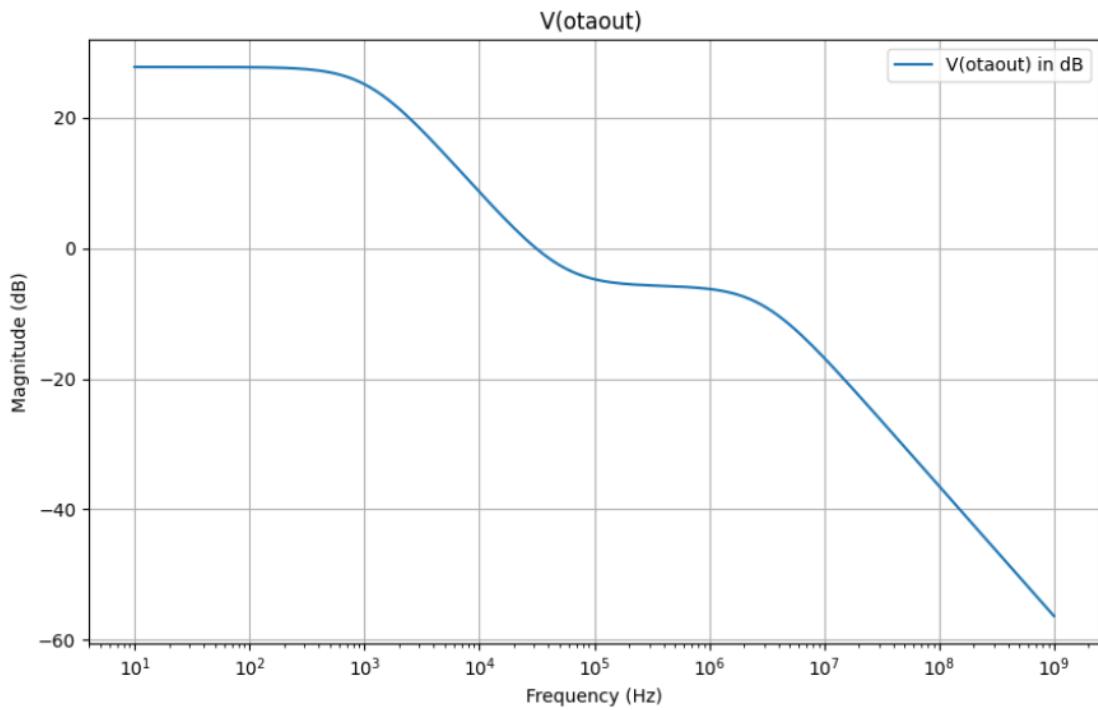


Figure 58: V_{otaout} for Loop Gain

Case 2:- Open Loop PSRR calculation

Schematic

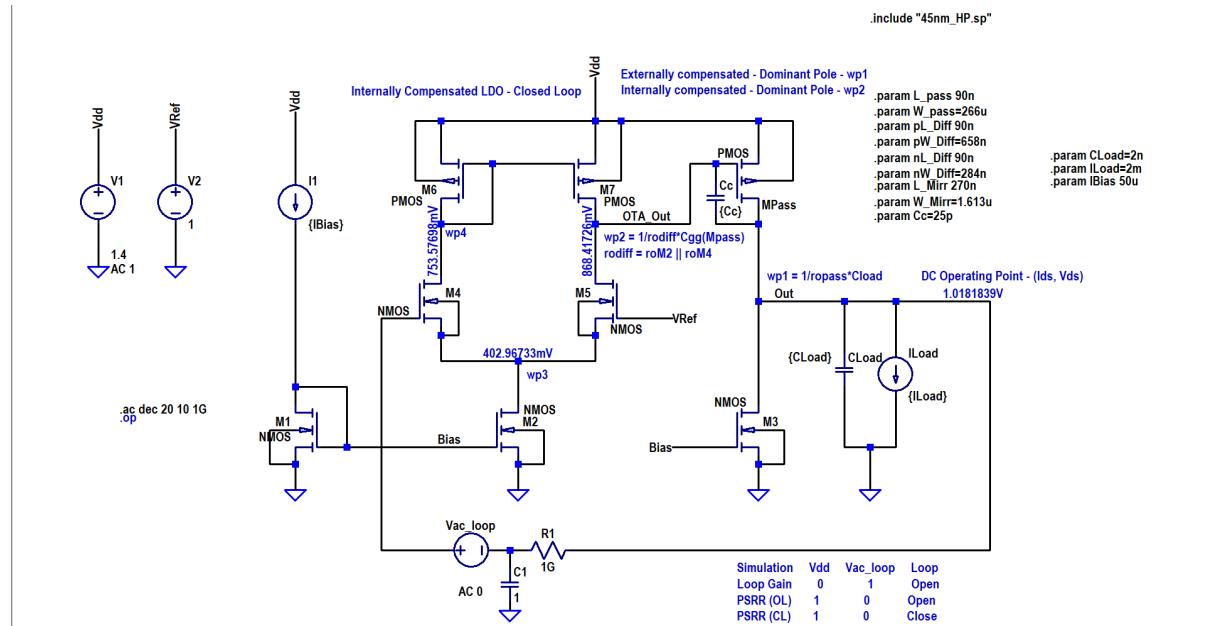


Figure 59: Schematic

Output waveforms plot using Python:

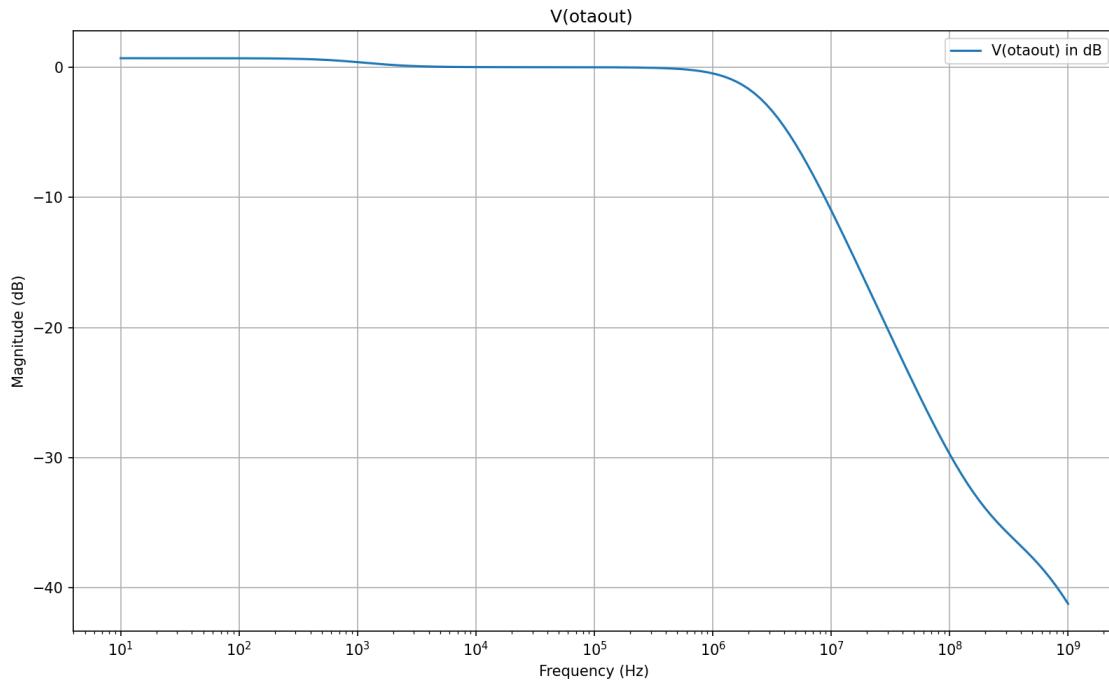


Figure 60: Vota for Open Loop PSRR

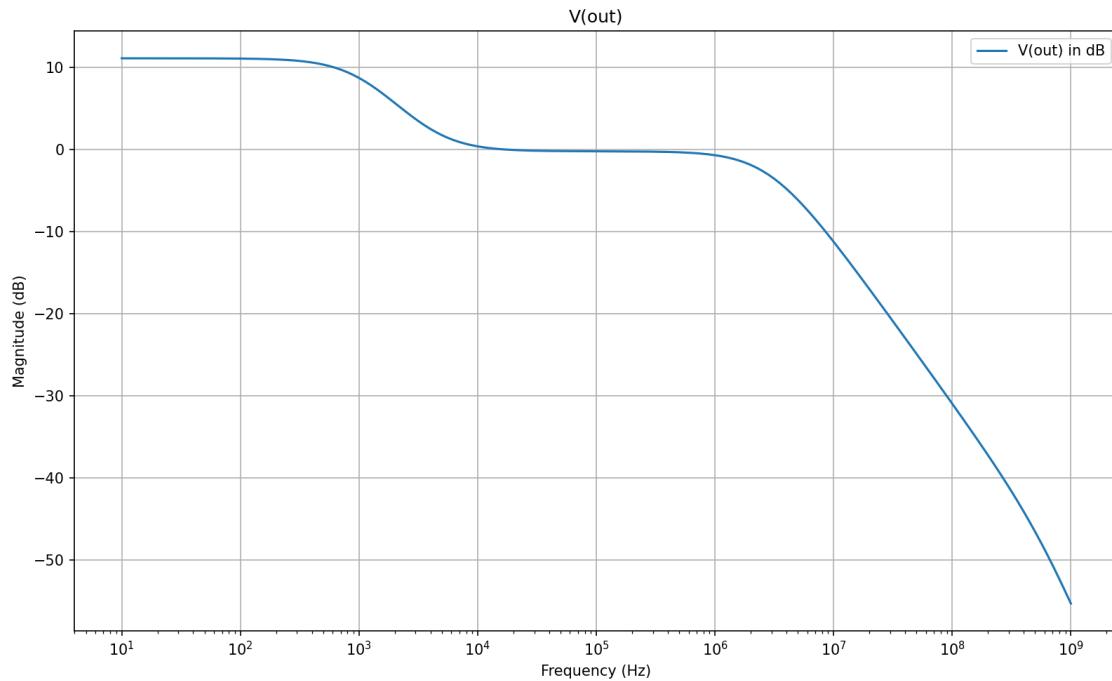


Figure 61: Vout for Open Loop PSRR

Case 3:- Closed loop PSRR calculation

Schematic

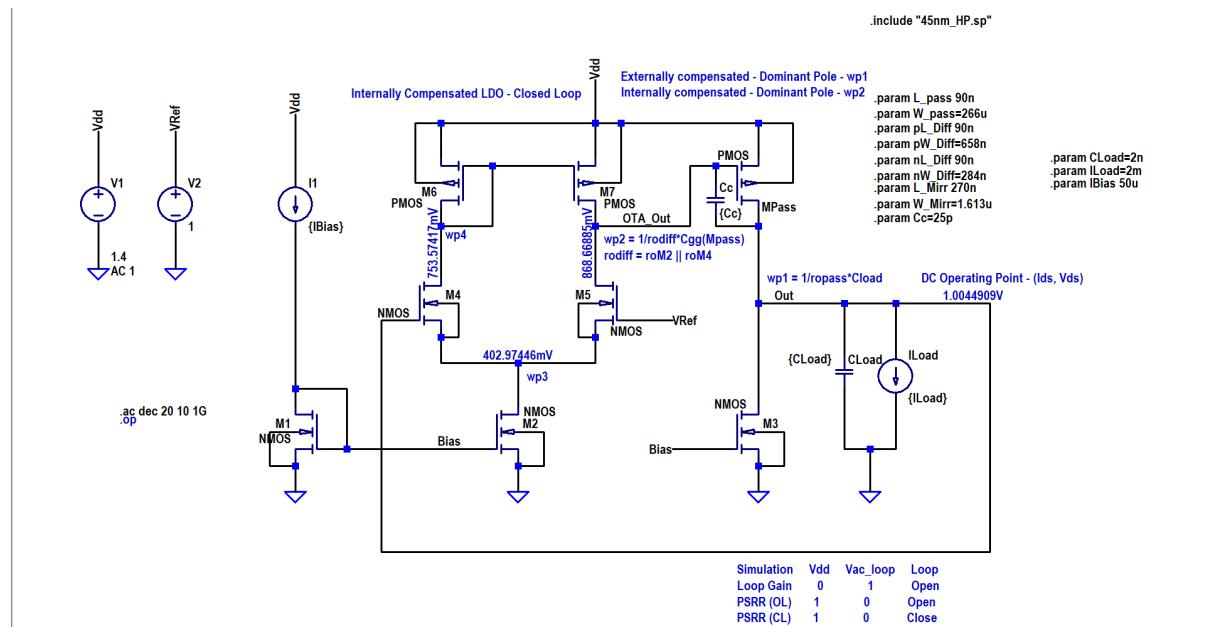


Figure 62: Schematic

Output waveforms plot using Python:

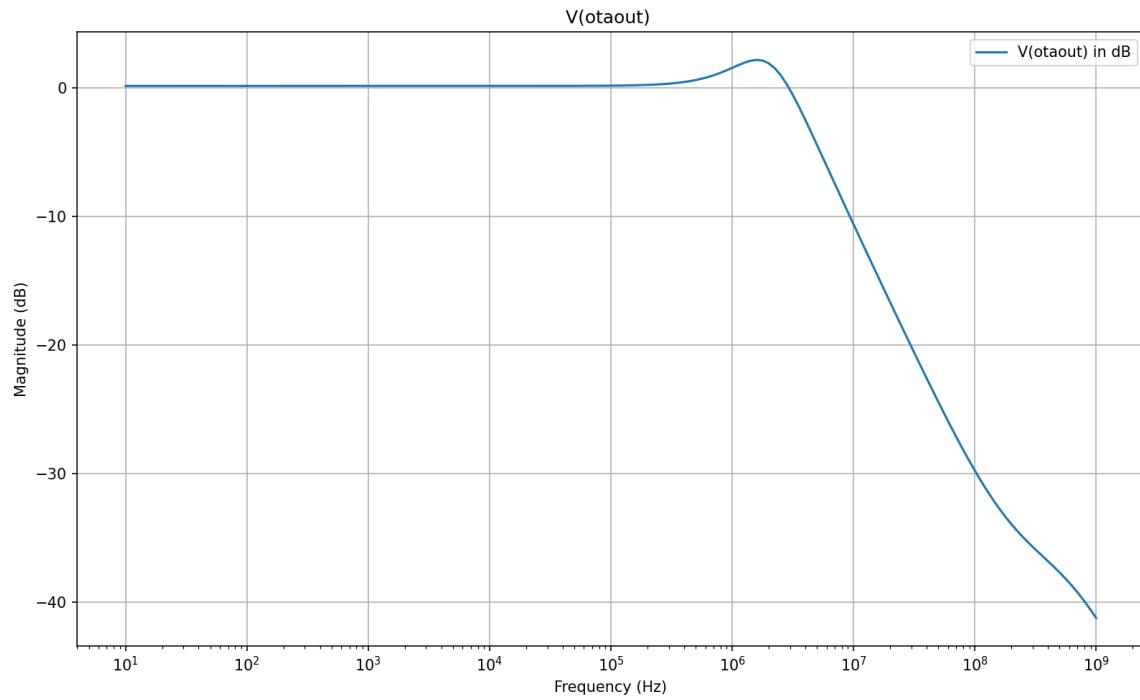


Figure 63: Vota for closed loop PSRR

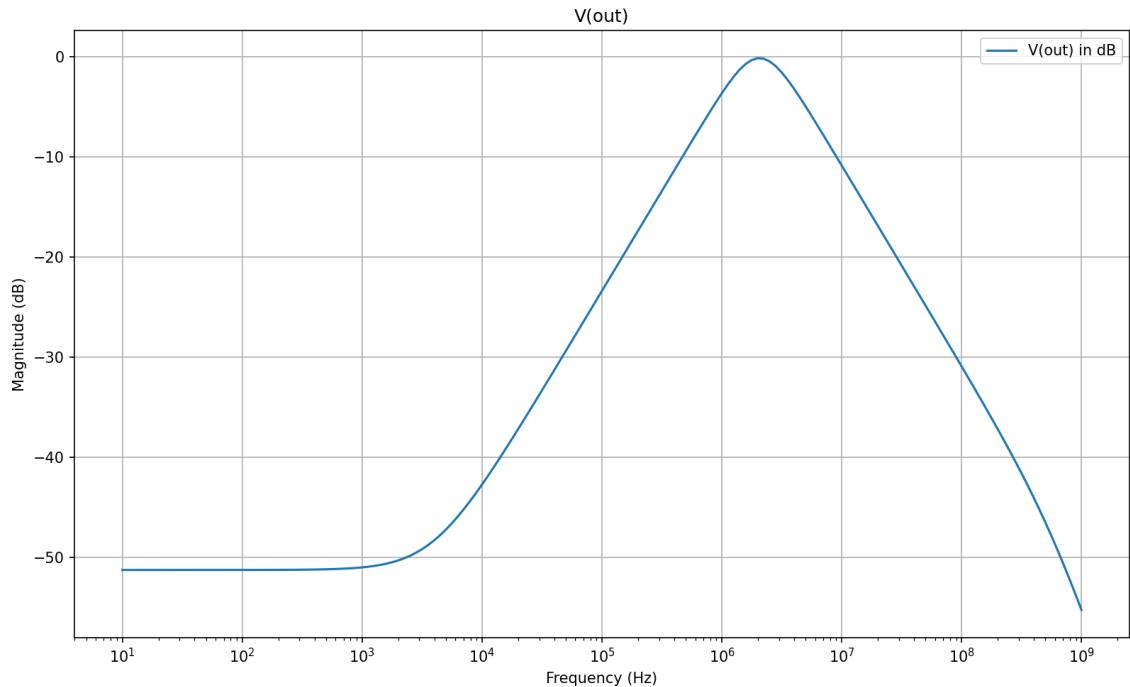


Figure 64: Vout for closed loop PSRR

Heavy Load (10mA)

Schematic

Case 1:- Loop gain analysis:

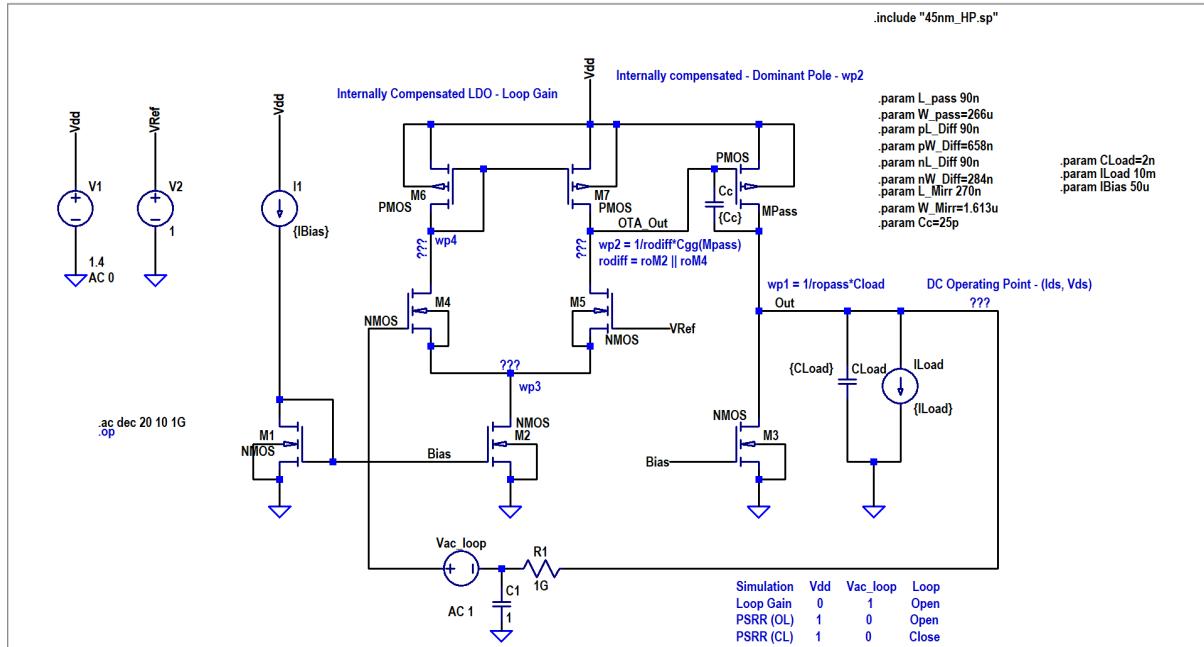


Figure 65: Schematic

Output Log File:

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg}-V_{th}$ (V)	Operating Region
m1	nmos	6.17E-01	6.17E-01	4.69E-01	1.48E-01	Saturation
m2	nmos	3.99E-01	6.17E-01	4.69E-01	1.48E-01	Saturation
m3	nmos	1.01E+00	6.17E-01	4.69E-01	1.48E-01	Saturation
m4	nmos	3.56E-01	6.00E-01	4.66E-01	1.34E-01	Saturation
m5	nmos	3.50E-01	6.01E-01	4.66E-01	1.35E-01	Saturation
m6	pmos	-6.45E-01	-6.45E-01	-4.84E-01	-1.61E-01	Saturation
m7	pmos	-6.50E-01	-6.45E-01	-4.84E-01	-1.61E-01	Saturation
mpass	pmos	-3.87E-01	-6.50E-01	-4.87E-01	-1.63E-01	Saturation

Table 16: Transistor Data

```

LTspice 24.0.12 for Windows
Circuit: * C:\Users\karthik\OneDrive - iiit-b\ACMOS Project Files\Heavy Load\Internally_Compensated_45nm\Internal_45nm_LG.asc
Start Time: Mon Dec 9 00:19:25 2024
solver = Normal
Maximum thread count: 16
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
    --- BSIM4 MOSFETS ---
Name:      m4        m5        m2        m1        m3
Model:     nmos      nmos      nmos      nmos      nmos
Id:       2.47e-05  2.48e-05  4.94e-05  5.00e-05  5.08e-05
Vgs:      6.00e-01  6.01e-01  6.17e-01  6.17e-01  6.17e-01
Vds:      3.56e-01  3.50e-01  3.99e-01  6.17e-01  1.01e+00
Vbs:      0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.00e+00
Vth:      4.66e-01  4.66e-01  4.69e-01  4.69e-01  4.69e-01
Vdsat:   1.42e-01  1.43e-01  1.61e-01  1.61e-01  1.61e-01
Gm:       2.44e-04  2.44e-04  4.96e-04  5.02e-04  5.09e-04
Gds:      5.08e-06  5.16e-06  3.19e-06  2.30e-06  2.12e-06
Gmb:      5.62e-05  5.63e-05  1.16e-04  1.18e-04  1.20e-04
Cbd:     1.28e-16  1.29e-16  7.22e-16  6.88e-16  6.40e-16
Cbs:     2.27e-16  2.27e-16  1.29e-15  1.29e-15  1.29e-15

Name:      m6        m7        mpass
Model:     pmos      pmos      pmos
Id:       -2.47e-05 -2.47e-05 -1.01e-02
Vgs:     -6.45e-01 -6.45e-01 -6.50e-01
Vds:     -6.45e-01 -6.50e-01 -3.87e-01
Vbs:     0.00e+00  0.00e+00  0.00e+00
Vth:     -4.84e-01 -4.84e-01 -4.87e-01
Vdsat:  -1.76e-01 -1.76e-01 -1.78e-01
Gm:      2.45e-04  2.46e-04  9.88e-02
Gds:     4.95e-06  4.94e-06  2.52e-03
Gmb:     5.20e-05  5.20e-05  2.09e-02
Cbd:    2.79e-16  2.79e-16  1.19e-13
Cbs:    5.26e-16  5.26e-16  2.13e-13

Total elapsed time: 0.157 seconds.

```

Figure 66: Output Log File

Output waveforms plot using Python:

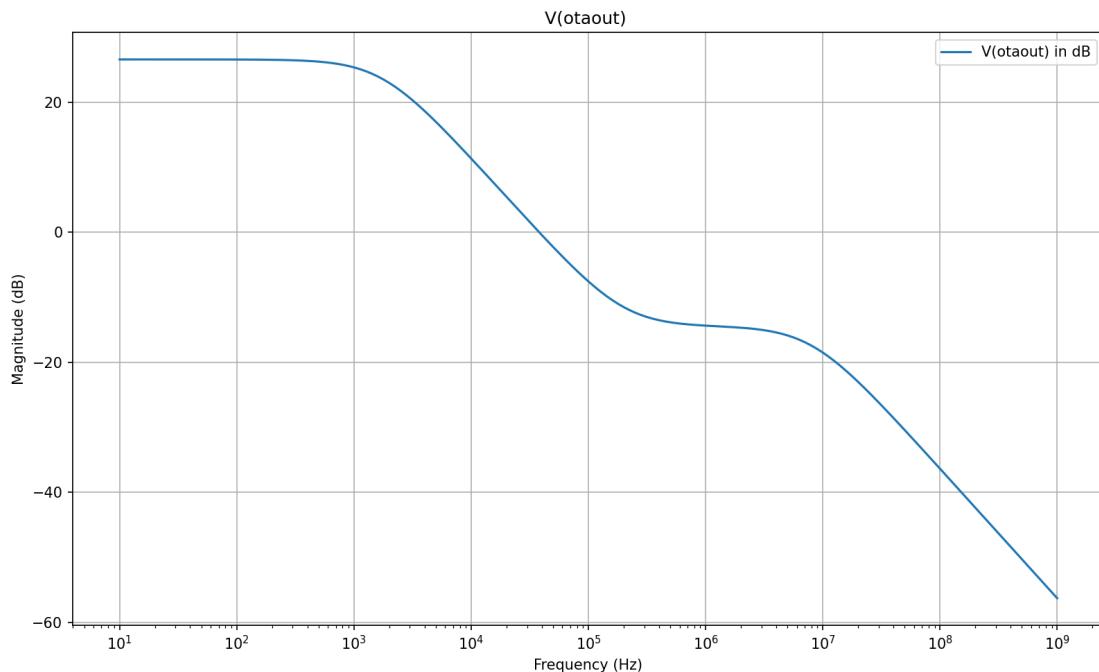


Figure 67: Vota for loop gain

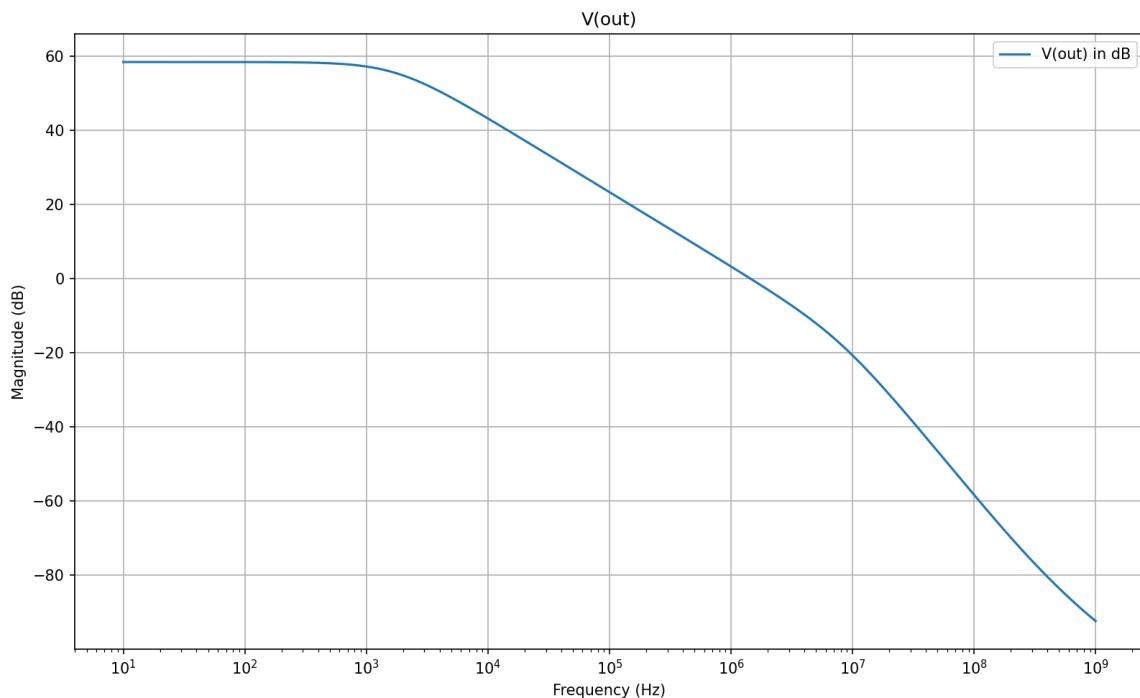


Figure 68: Vout for loop gain

Case 2:- Open Loop PSRR calculation

Schematic

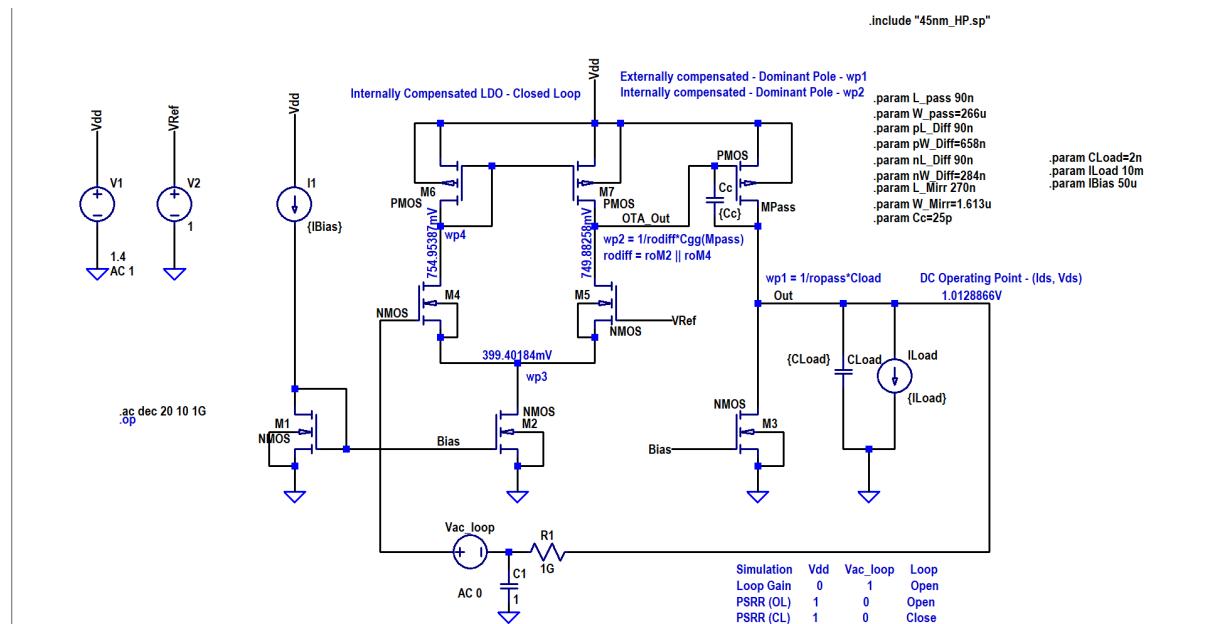


Figure 69: Schematic

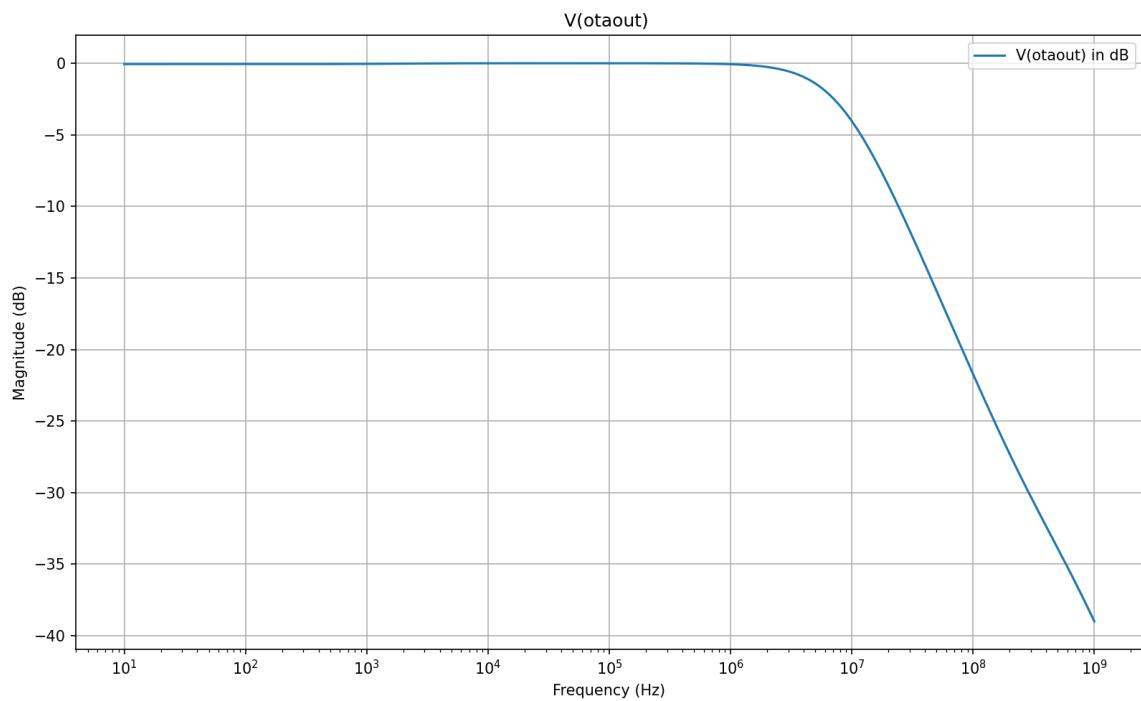
Output waveforms plot using Python:

Figure 70: Vota for open loop PSRR

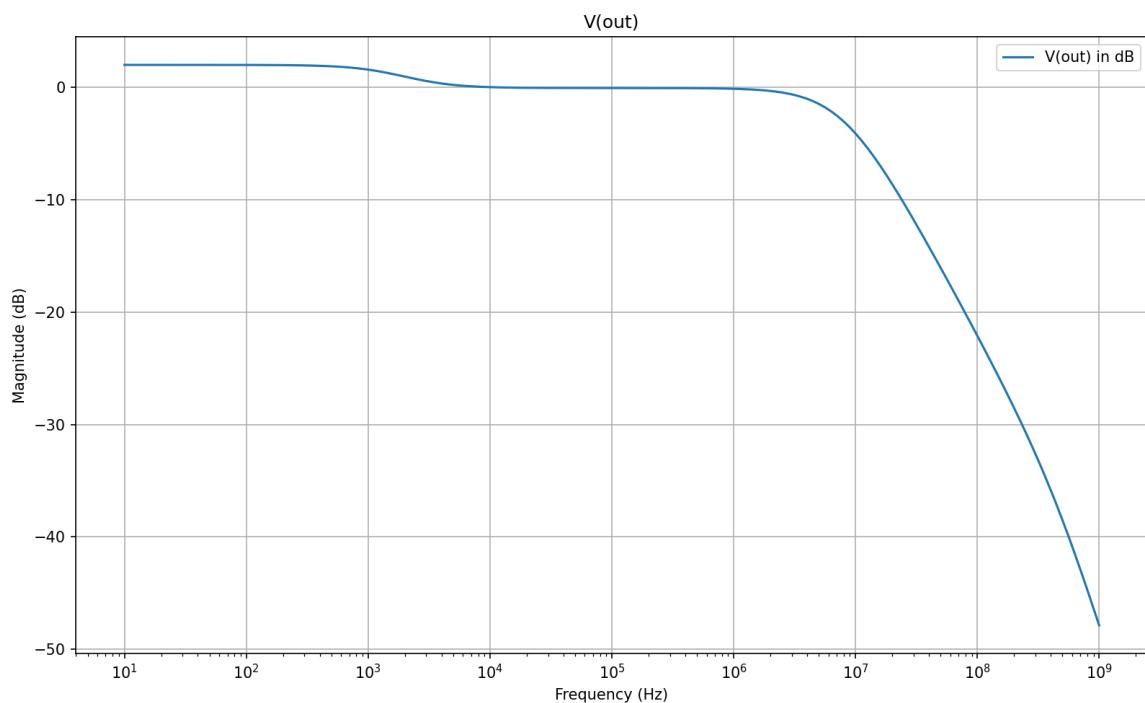


Figure 71: Vout for open loop PSRR

Case 3:- Closed loop PSRR calculation

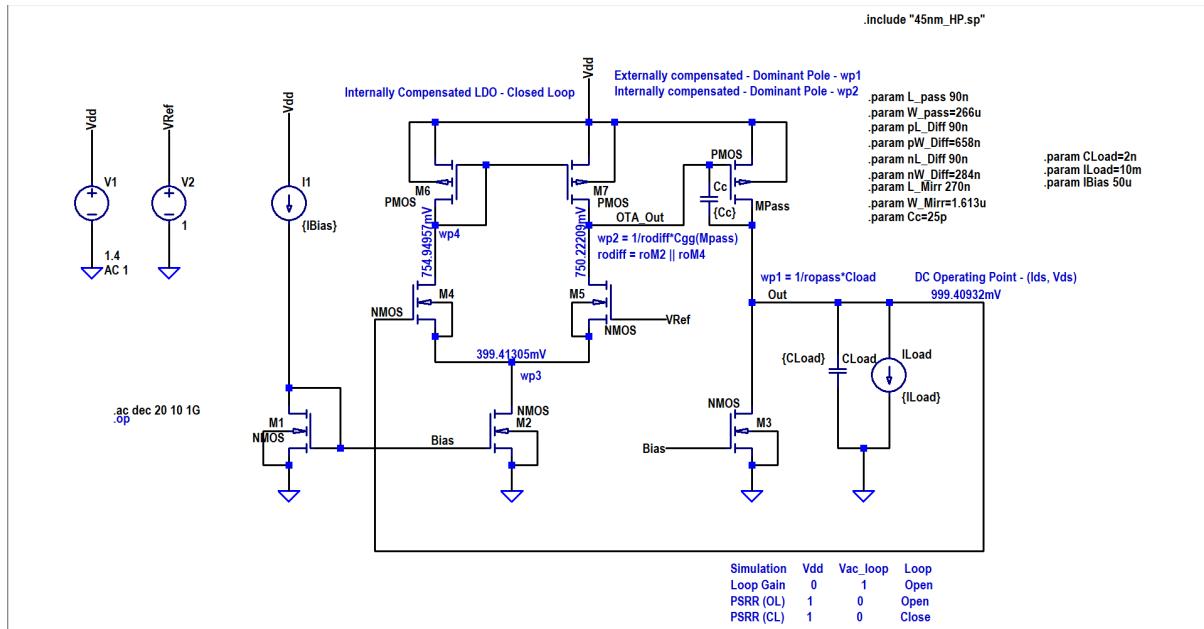


Figure 72: Schematic

Output waveforms plot using Python:

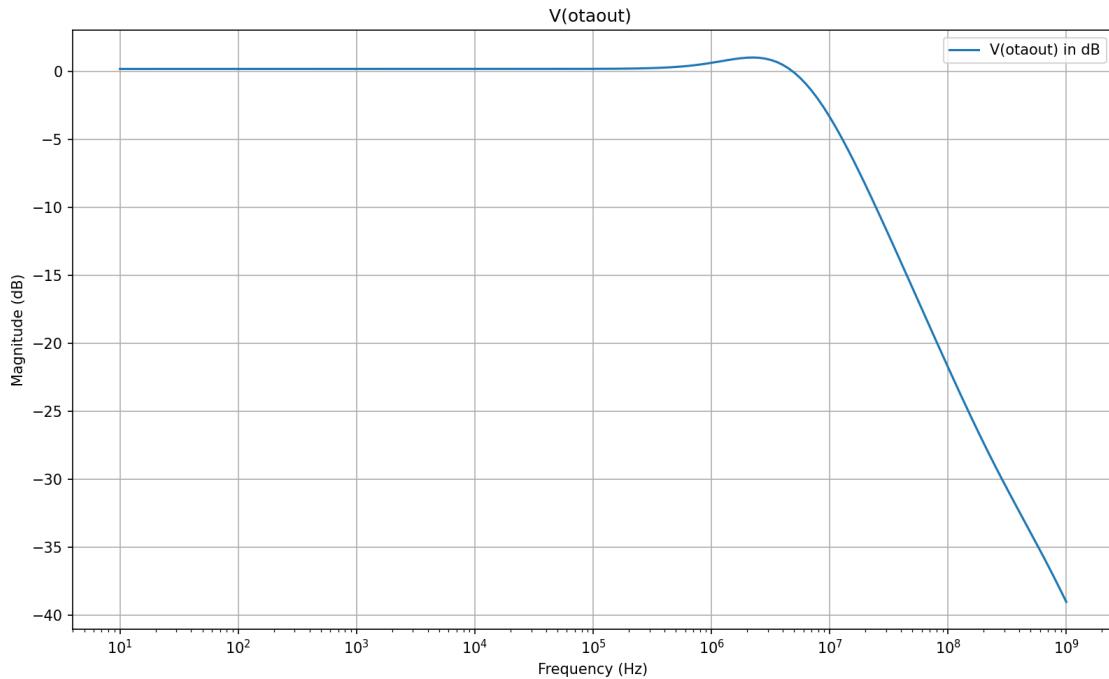


Figure 73: Vota for closed loop PSRR

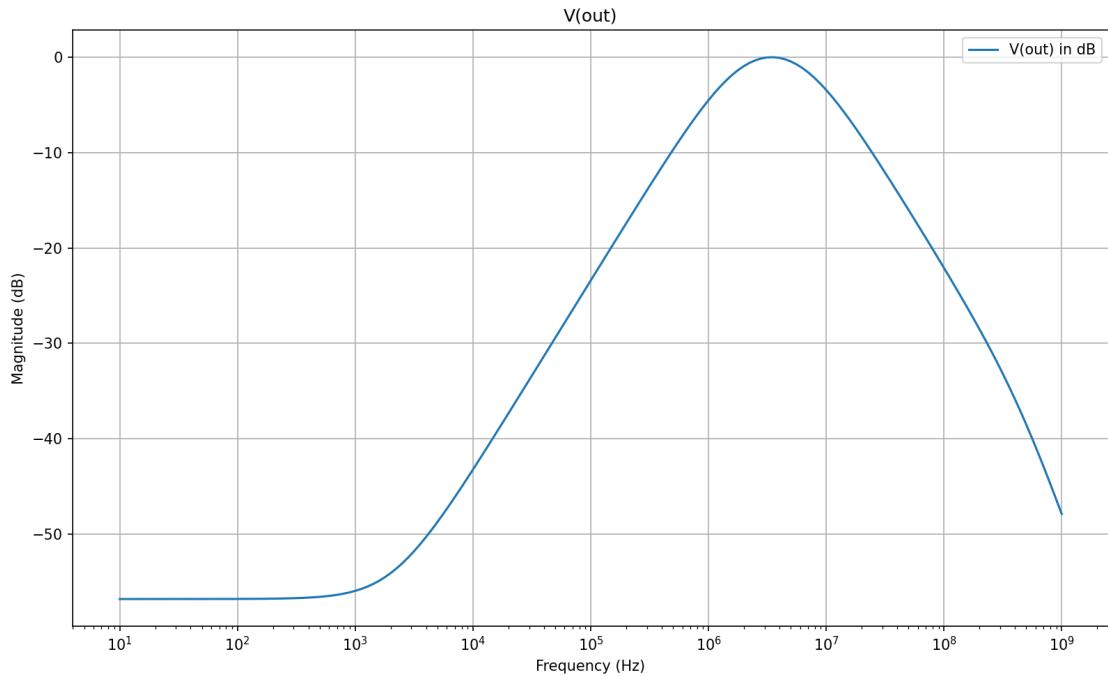


Figure 74: V_{out} for closed loop PSRR

Transient Analysis

Iload Vs Time

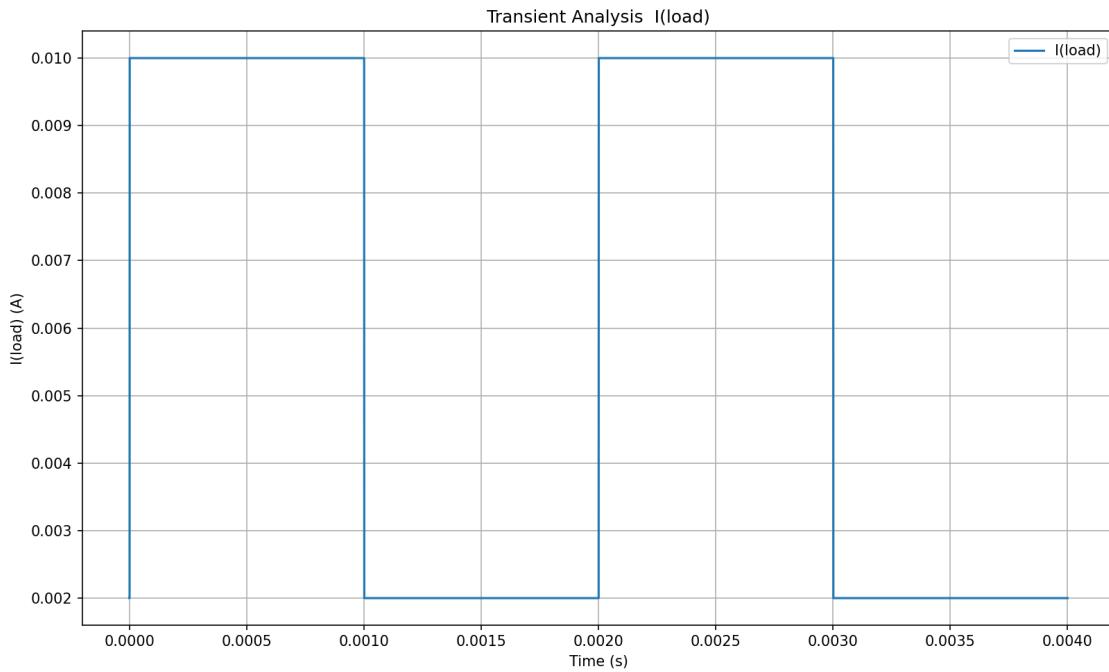


Figure 75: I(load)

Vout Vs Time

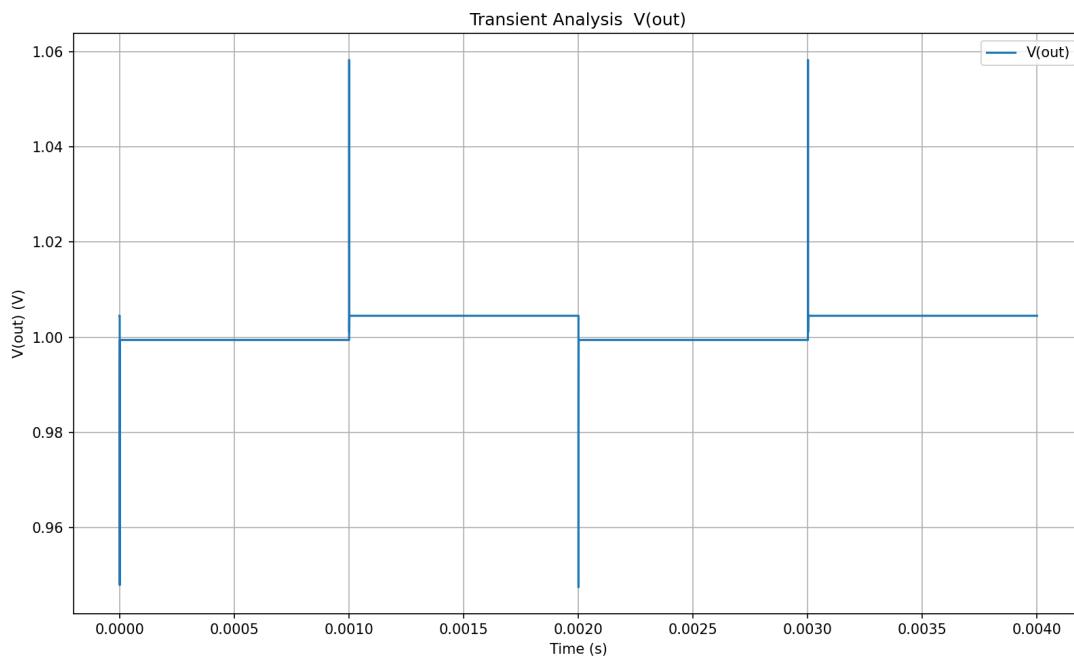


Figure 76: V(out)

Simulation vs. Hand Calculations

For Passfet HEAVY LOAD

Hand Calculation

- $r_o = 500 \Omega$
- $g_m = 0.1 \text{ A/V}$
- $f_{p1} \text{ (first pole location)} = 1.579 \text{ MHz}$
- $g_m r_o = 50$
- $C_{gg} = 0.585p$
- $C_{load} = 2n$
- $C_c = 25p$

Table 17: Hand Calculation vs Simulation Results

Parameter	Hand Calculation	Simulation Result	% Error Percentage
f_{p1}	1.59kHz	1.78kHz	10.674%
f_{p2}	7.957MHz	7.943MHz	0.176%
f_{ugb}	1.59MHz	1.41MHz	12.765%

Name	m1	m2	m3	m4	m5	m6	m7	mpass
Model	nmos	nmos	nmos	nmos	nmos	pmos	pmos	pmos
Id	5.00E-05	4.94E-05	5.08E-05	2.47E-05	2.48E-05	-2.47E-05	-2.47E-05	-1.01E-02
Vgs	6.17E-01	6.17E-01	6.17E-01	6.00E-01	6.01E-01	-6.45E-01	-6.45E-01	-6.50E-01
Vds	6.17E-01	3.99E-01	1.01E+00	3.56E-01	3.50E-01	-6.45E-01	-6.50E-01	-3.87E-01
Vbs	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth	4.69E-01	4.69E-01	4.69E-01	4.66E-01	4.66E-01	-4.84E-01	-4.84E-01	-4.87E-01
Vdsat	1.61E-01	1.61E-01	1.61E-01	1.42E-01	1.43E-01	-1.76E-01	-1.76E-01	-1.78E-01
Gm	5.02E-04	4.96E-04	5.09E-04	2.44E-04	2.44E-04	2.45E-04	2.46E-04	9.88E-02
Gds	2.30E-06	3.19E-06	2.12E-06	5.08E-06	5.16E-06	4.95E-06	4.94E-06	2.52E-03
Gmb	1.18E-04	1.16E-04	1.20E-04	5.62E-05	5.63E-05	5.20E-05	5.20E-05	2.09E-02
Cbd	6.88E-16	7.22E-16	6.40E-16	1.28E-16	1.29E-16	2.79E-16	2.79E-16	1.19E-13
Cbs	1.29E-15	1.29E-15	1.29E-15	2.27E-16	2.27E-16	5.26E-16	5.26E-16	2.13E-13
ro	4.35E+05	3.13E+05	4.72E+05	1.97E+05	1.94E+05	2.02E+05	2.02E+05	3.97E+02
gmro	2.18E+02	1.55E+02	2.40E+02	4.80E+01	4.73E+01	4.95E+01	4.98E+01	3.92E+01

Table 18: Transistor Parameters Table

For Passfet LIGHT LOAD

Hand Calculation

- $r_o = 2.5k\Omega$
- $g_m = 20m \text{ A/V}$
- $f_{p1} \text{ (first pole location)} = 1.348\text{kHz}$
- $g_m r_o = 50$
- $C_{gg} = 0.585p$
- $C_{load} = 2n$
- $C_c = 25p$

Table 19: Hand Calculation vs Simulation Results

Parameter	Hand Calculation	Simulation Result	% Error Percentage
f_{p1}	1.348kHz	1.12kHz	20.35%
f_{p2}	2.801MHz	2.818MHz	0.6%
f_{ugb}	1.348MHz	1.259MHz	7.07%

Name	m1	m2	m3	m4	m5	m6	m7	mpass
Model	nmos	nmos	nmos	nmos	nmos	pmos	pmos	pmos
Id	5.00E-05	4.94E-05	5.09E-05	2.50E-05	2.44E-05	-2.50E-05	-2.44E-05	-2.05E-03
Vgs	6.17E-01	6.17E-01	6.17E-01	6.02E-01	5.97E-01	-6.46E-01	-6.46E-01	-5.32E-01
Vds	6.17E-01	4.03E-01	1.02E+00	3.51E-01	4.65E-01	-6.46E-01	-5.32E-01	-3.82E-01
Vbs	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth	4.69E-01	4.69E-01	4.69E-01	4.66E-01	4.65E-01	-4.84E-01	-4.85E-01	-4.87E-01
Vdsat	1.61E-01	1.61E-01	1.61E-01	1.43E-01	1.41E-01	-1.77E-01	-1.76E-01	-9.51E-02
Gm	5.02E-04	4.96E-04	5.10E-04	2.45E-04	2.44E-04	2.47E-04	2.43E-04	3.58E-02
Gds	2.30E-06	3.15E-06	2.13E-06	5.21E-06	4.33E-06	4.99E-06	5.19E-06	6.59E-04
Gmb	1.18E-04	1.16E-04	1.20E-04	5.65E-05	5.63E-05	5.24E-05	5.14E-05	7.38E-03
Cbd	6.88E-16	7.21E-16	6.40E-16	1.29E-16	1.25E-16	2.79E-16	2.86E-16	1.20E-13
Cbs	1.29E-15	1.29E-15	1.29E-15	2.27E-16	2.27E-16	5.26E-16	5.26E-16	2.13E-13
ro	4.35E+05	3.17E+05	4.69E+05	1.92E+05	2.31E+05	2.00E+05	1.93E+05	1.52E+03
gmro	2.18E+02	1.57E+02	2.39E+02	4.70E+01	5.64E+01	4.95E+01	4.68E+01	5.43E+01

Table 20: Transistor Parameters Table