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School

of

Electronics and Communication Engineering

ADLD COURSE PROJECT

**IE-TEAM -1**

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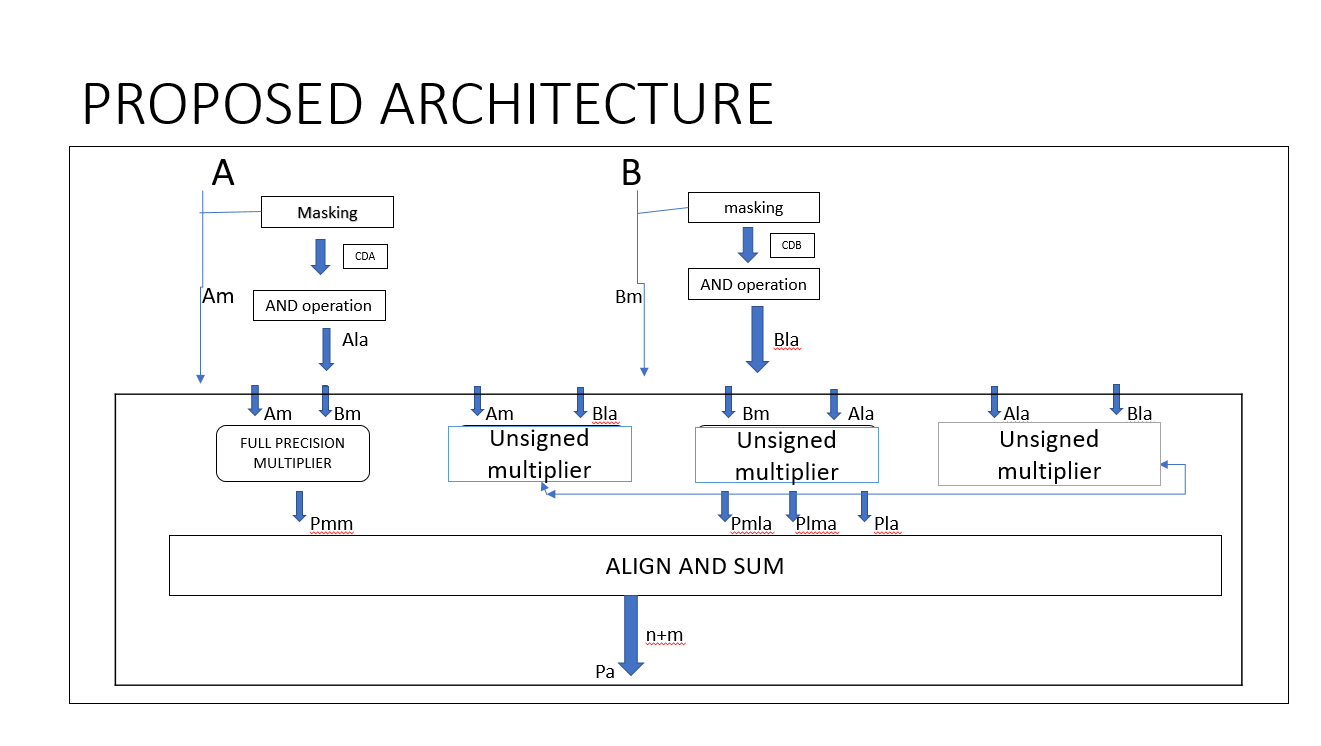
1. Problem Statement :

Design application specific approximate multipliers on fpga.

2) Architecture :

For our architecture , we have considered 2 8-bit numbers as a input.

By Splitting the numbers into 2 equal parts , we get Am/Bm and Ala /Bla.MSB bits namely Am and Bm are multiplied by using full precision multiplier whereas other bits are encoded first by using mask and 'and' operation then multiplication is performed by unsigned multiplier.Then by using suitable align and or operation final product is obtained*.*



3) Theory:

Approximate multipliers are designed to trade accuracy for reduced power consumption, area, or latency. These multipliers aim to provide an approximate result that is close enough to the exact result for certain applications where high precision is not necessary.

One common approach used in approximate multipliers is to reduce the number of partial products computed during the multiplication process. In a conventional multiplier, all possible pair-wise combinations of bits are multiplied and then added together to obtain the final product. However, in an approximate multiplier, fewer partial products are generated, leading to reduced computational complexity.

A full precision multiplier refers to a multiplication operation that computes the exact or precise result without any loss of precision. It multiplies two numbers with the maximum number of bits available for the operands and produces a result with a bit width that can accommodate the full range of possible values.

An unsigned multiplier is a type of multiplier that performs multiplication operations on unsigned numbers, also known as non-negative numbers. It disregards the sign bit of the operands and focuses solely on the magnitude of the numbers.

Compared to signed multiplication, unsigned multiplication can be simpler and more straightforward since it does not require consideration of sign extension or two's complement representation. This simplicity often leads to faster and more efficient implementations of unsigned multipliers.

4) Algorithm :

Step 1 : split equal no of bits in A and B as Am ,Bm and AL and BL representing MSB and LSB respectively.

Step 2: Perform the Masking of Lower bits and also perform AND operation. Pass the Higher bits without changing

Step 3: For AM and BM perform Full precision Multiplication.

Step 4: For remaining partial products perform unsigned booth multiplication.

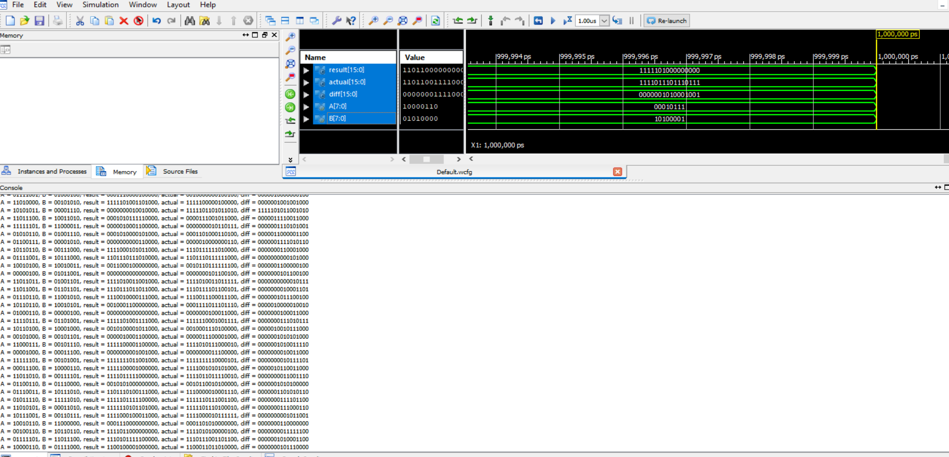
Step 5: Perform Align and Sum operation of all partial products.

Step 6: Display the approximate multiplication result.

4) Results:

Simulation

The waveform shown consists of A and B 8-bit inputs whose approximate multiplication is performed . The inputs are also multipled by using conventional multipler . The approximate results and the accurate results are compared and displayed using diff[15:0]



6) Conclusion:

The approximate multiplier is verified for 256 combinations of binary numbers using the proposed architecture.