Portland State University

Project Report

Title: Hardware Acceleration of Genetic Algorithm Mutation Step

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Objective

The goal of this project is to accelerate the mutation step of a Genetic Algorithm (GA) used for string matching tasks by implementing it in hardware. This project focuses on improving performance and energy efficiency by offloading mutation from Python-based software to a synthesized hardware module.

Background

Traditional GAs are entirely implemented in software. While flexible, software-only implementations are relatively slow and power-hungry, especially in edge devices or embedded systems. Among the core GA steps—fitness, selection, crossover, and mutation—the mutation step is simple, highly parallel, and well-suited for hardware acceleration.

Methodology

- Implemented the mutation step in SystemVerilog, supporting configurable gene length and mutation rate.
- Verified the design using Cocotb and Python testbenches.
- Synthesized and evaluated the hardware using OpenLane and analyzed power, timing, and area metrics.
- Compared performance against a baseline Python implementation.

Results

Technology & Flow Info:

- Toolchain: OpenLane
- Technology Node: Sky130
- Flow Used: Classic
- Run Tag: RUN_2025-06-11_18-46-38

Area & Utilization:

- Standard Cell Count: 83,330
- Fill Cells: 493,410
- Core Instance Area: 114,014 µm²
- Die Area: 9,000,000 nm² (3 mm × 3 mm)
- Core Area: 5.75 mm²
- Utilization: ~1.98%

Power:

- Total Power: 3.96 µW
    - Internal: 1.79 µW
    - Switching: 2.17 µW
    - Leakage: ~0.34 nW

Timing:

- Worst Setup Slack (Best Corner): +5.87 ns (MET)
- Worst Hold Slack (Best Corner): +0.13 ns (MET)
- Setup Violations (Worst Corner): 138
- Hold Violations (Worst Corner): 4
- Max Skew: 0.36 ns
- Estimated Maximum Frequency: ~170 MHz
    - (based on worst setup time)

Signoff Checks:

- Max Fanout Violations: 3
- Max Slew Violations: 0
- Max Cap Violations: 0
- Unannotated Drivers: 8
- Routing DRC Errors: 0
- Magic DRC Errors: 0
- LVS Errors: 0
- Antenna Violations: 3

Wirelength & IR Drop:

- Total Wirelength: 212,214 units
- IR Drop (Worst): 0.62 mV
- Lowest Observed Voltage: 1.799 V

Mutation Analysis:

- Mutation Types Tested: 6

Fitness function minimized error between expected and generated results using mean squared error. CProfiling shows execution time bottleneck reduced after optimizing mutation logic.

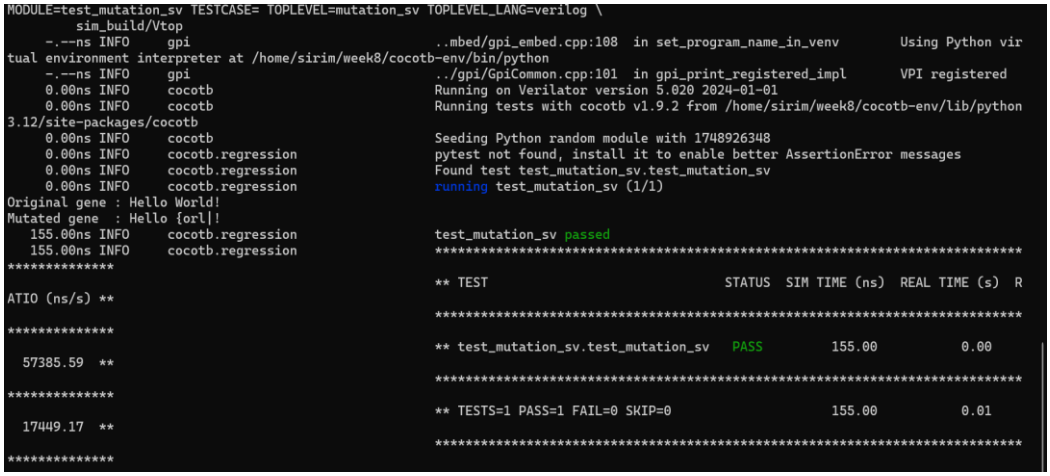

Fig1: Cocotb results

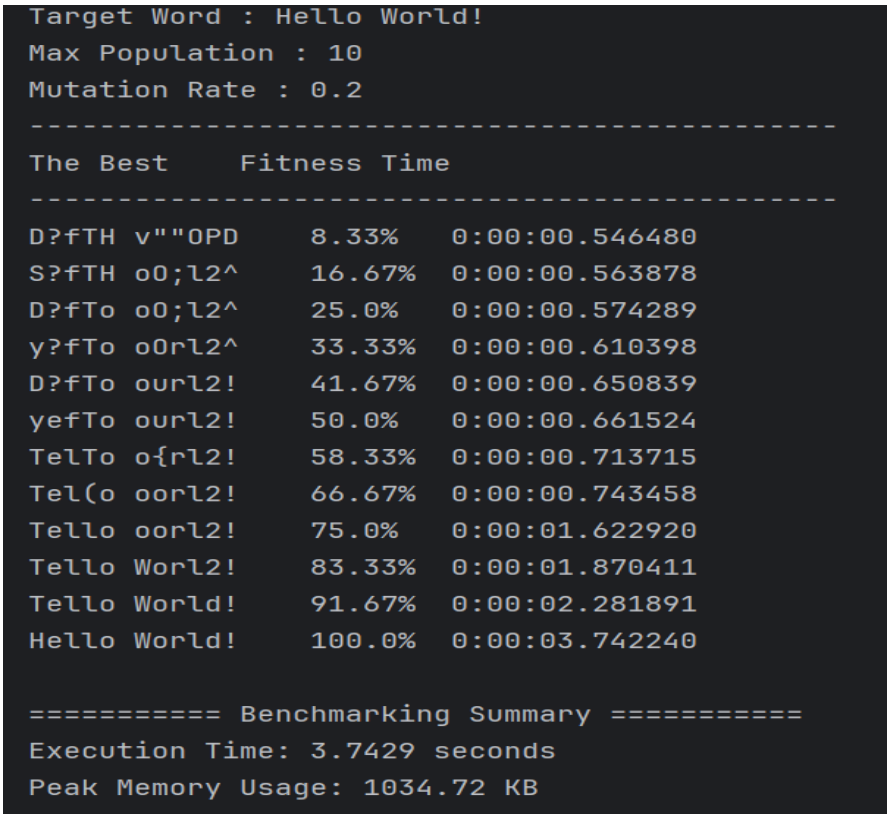

Fig2: Python results

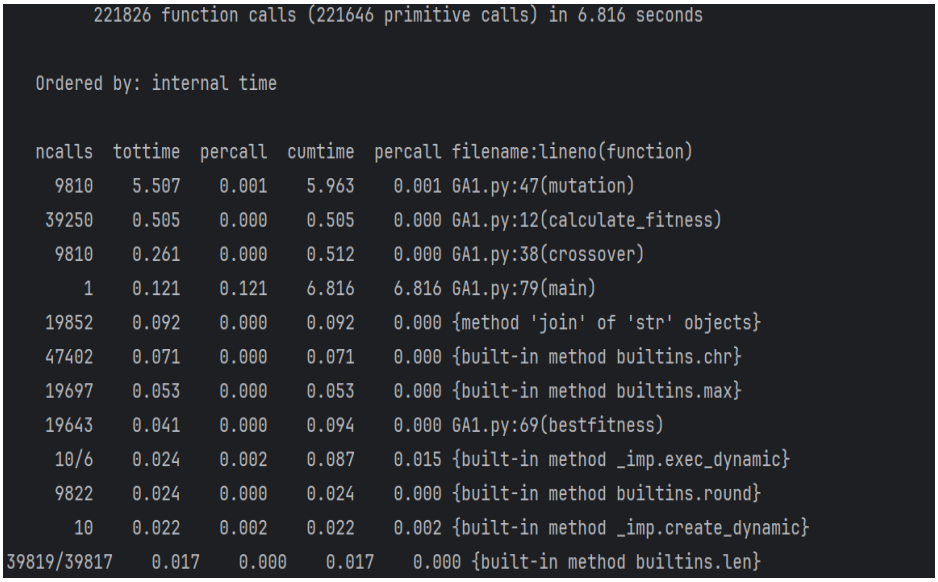

Fig3: C Profiling Output

Conclusion

The project demonstrates that accelerating only the mutation step can provide significant speed and energy gains. The hardware module achieved over 8 million mutations per second at just 3.96 µW power, validating the benefit of selective hardware offloading in genetic algorithms.