Question 1: Logical to Physical Address Translation

Objective: To understand the process of address translation in a paging system.

Problem: Consider a system with a logical address space of NP (128) pages, where each page is PSize (1 KB) in size. The physical memory consists of MSize (64) frames. The following is a partial page table for a running process (you should try other examples also):

Page #	Frame #
3	4
10	61
25	18
50	7
111	42

For each of the logical addresses below, determine the corresponding physical address. If the address results in a page fault, state "Page Fault". Show all your calculation steps. (Try other examples also)

1. Logical Address: 10542
2. Logical Address: 25610
3. Logical Address: 3686

Of course, here are two more questions focusing on virtual memory and segmentation.

Question 2: Two-Level Paging and Address Translation

Objective: To understand address translation in a system with a two-level page table structure.

Problem:

Consider a system with a 32-bit logical address space and a page size of 4 KB. The system uses a two-level paging scheme, where the logical address is divided as follows:

- A 10-bit page directory index.
- A 10-bit page table index.
- A 12-bit offset.

Inputs are the following:

- The base address of the Page Directory is memory location 0x00401000.
- A partial dump of the Page Directory and relevant Page Tables is provided below. Each entry is 4 bytes.

Page Directory (at 0x00401000):

| Index (Hex) | Content (Frame #) (Hex) |

| 0x001 | 0x00105 |

| 0x002 | 0x00106 |

| ... | ... |

| 0x1A3 | 0x0020A |

Page Table (at frame 0x00105):

| Index (Hex) | Content (Frame #) (Hex) |

| ... | ... |

| 0x20F | 0x0035B |

| ... | ... |

Page Table (at frame 0x0020A):

| Index (Hex) | Content (Frame #) (Hex) |

| ... | ... |

| 0x03C | 0x0041F |

| ... | ... |

For the following logical addresses, translate them into their corresponding physical addresses. Show every step of your calculation, including how you break down the logical address.

1. Logical Address: 0x00420FABC
2. Logical Address: 0x068C03C12

Question 6: Segmentation and Address Translation

Objective: To understand logical to physical address translation in a segmented memory system.

Problem: A process is running on a system that uses segmentation. The segment table for this process is as follows:

Segment #	Base Address	Limit (Length)
0	219	600
1	2300	14
2	90	100
3	1327	580
4	1952	96

For each of the logical addresses below (given as segment number, offset), calculate the corresponding physical address. If the address is invalid (i.e., the offset is outside the segment's bounds), state "Segmentation Fault".

1. Logical Address: 0, 430
2. Logical Address: 1, 10
3. Logical Address: 2, 101
4. Logical Address: 3, 500
5. Logical Address: 4, 100