**Project One**

EE 490/590 Computer Architecture, Spring 2016

Assigned at Feb. 19 2016.

Due at 23:59:59, March. 11 2016.

1. **Grading**
2. (***50 points***) **Report (Do not print)**
3. Please use the template we provided. Follow all the steps.
4. (***50 points***) **Coding** (**No demo)**
5. Please submit your project through UBlearn, not TA-email.
6. Please modify the 00000000 folder as UBID (Only the number) at first.
7. Then Zip the folder as UBID.zip.
8. Submit zip file ONLY please.
9. Only 2 Things inside the zip file please:
10. .pdf file. Report (pdf file only, named as project1.pdf)
11. project1 folder

Inside project1 folder, .v file (maybe .v files), no matter one file or multi files, please name TOP LEVEL DESIGN as project1.v. We have provided the sample project1.v. Please use it without changing any existing variable names. You can add more variables. For example, reset signal.

.v file (test file), please name test file as test\_project1.v. Please don’t change it. We are going to use it to grade your project.

1. **Kindly Remind**
2. Start it earlier. Not easy.
3. Practice recitation examples and do homework at first.
4. Please read recitation\_Bonus.pdf at first, understand the definition of state. STATE FLOW is the soul of Verilog.
5. **DESCRIPTION**

We are using FPGA board below to clarify the project1. (But, you are not required to implement project1 design into FPGA board.)

You must finish your design by using Verilog not VHDL.

1. Import 4 numbers into the board.
2. Sort them from small -> large. (You can choose bubble sort, but others are also accepted.)
3. Display the sorted numbers by decimal on 7-segment display.

Here are the details below:



Part A (Function: among 4 numbers, which one you want to import): We need to import 4 numbers into the board. By using different combination of Part A, we could import different one.

4’b0001 is to import the 1st one;

4’b0010 to import 2nd;

4’b0100 to import 3rd;

4’b1000 to import 4th.

Part B (Function: What value do you want to import): The range of value is controlled by using Part B. We have 4 bits here, so the range should start from 4’b0000 to 4’b1111 (In decimal, it is 0 to 15).

Part C: After you select where to import (Part A) and what value to import (Part B), click Button C.

For example,

4’b0001 (Part A) + 4’b0101 (Part B) + Button C (click): 5 should be stored into 1st

4’b1000 (Part A) + 4’b1111 (Part B) + Button C (click): 15 should be stored into 4th

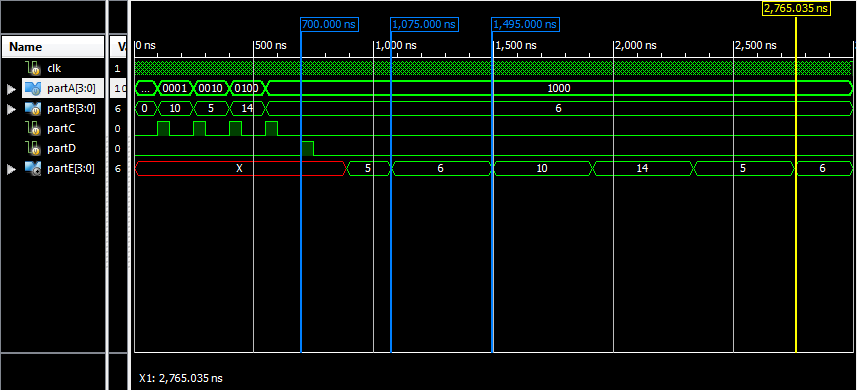
4’b1101 (Part A) + 4’b0101 (Part B) + Button C (click): Nothing happen, because Part A is not available

4’b1000 (Part A) + 4’b1111 (Part B): Nothing happen, because you did not click Button C

Part D: Sort them. Display sorted number one by one.

Part E: Display. The value range should start from 0 to 15. (Last year, we asked students to display all the results into 7 segment display. This semester, it is not necessary. Go through the simulation result from TA. You will understand clearly.)

1. **Simulation Results from TA**



At shown in the simulation result,

Starting from 0ns, input values into memory by clicking partC.

partA = 2’b0001, partB = 10 decimal value

partA = 2’b0010, partB = 5

partA = 2’b0100, partB = 14

partA = 2’b1000, partB = 6

At 700ns, click partD to sort.

After sorting finished, display results at partE.

Simulation Run time = 3000ns.