Q1. 2 BIT COMPARATOR USING TERNARY OPERATOR.

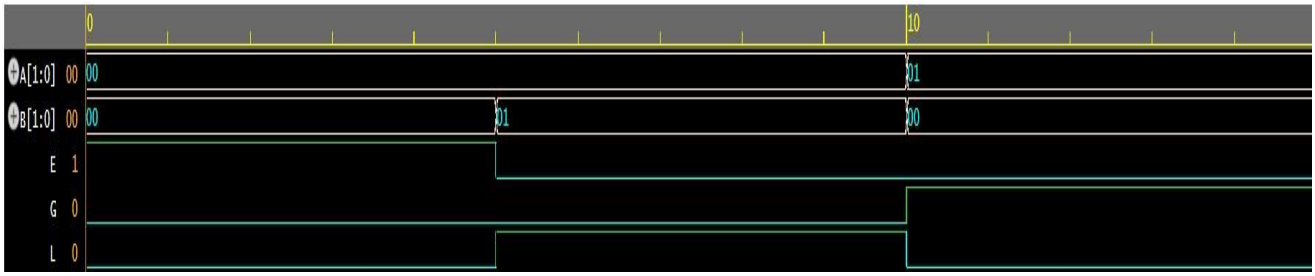
VERILOG CODE:

```
module comparator2bit(A,B,E,G,L);
  input [1:0]A,B;                    // Declare 2-bit input ports A and B
  output E,G,L;                      // Declare output ports:  E for Equal, G for Greater, L for Less
  assign E=(A==B)?1'b1:1'b0;    // If A is equal to B, set E to 1 (true), else 0 (false)
  assign G=(A>B)?1'b1:1'b0;     // If A is greater than B, set G to 1 (true), else 0 (false)
  assign L=(A<B)?1'b1:1'b0;     // If A is less than B, set L to 1 (true), else 0 (false)
endmodule
```

TEST BECH CODE:

```
module comparator2bit_test;
  reg [1:0]A,B;
  wire E,G,L;
  comparator2bit dut(A,B,E,G,L);
  initial begin
     A=2'b00; B=2'b00;
   #5 A=2'b00; B=2'b01;
   #5 A=2'b01; B=2'b00;
   #5 A=2'b01; B=2'b01;
  end
  initial begin
    $monitor("Sim time=%0t,A=%b,B=%b,E=%b,G=%b,L=%b",$time,A,B,E,G,L);
  end
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(0,A,B,E,G,L);
  end
endmodule
```

OUTPUT WAVEFORM:



SIMULATION OUTPUT:

Sim time=0,A=00,B=00,E=1,G=0,L=0
Sim time=5,A=00,B=01,E=0,G=0,L=1
Sim time=10,A=01,B=00,E=0,G=1,L=0
Sim time=15,A=01,B=01,E=1,G=0,L=0