1. SoC and Package:

- An SoC (System on a Chip) is often called a "chip" but is technically a "package."
- The QFN-48 (Quad Flat No-Leads) package is commonly used in Arduino boards.
- The package connects to various pins or I/Os based on the PCB design.

2. Core Components of a Chip:

- Pads: Connectors inside the chip for electrical signals.
- Core: Contains digital logic (AND, OR, XOR gates, MUXes).
- Die: Part of a semiconductor wafer that houses cores and logic.

3. Foundry IPs and Macros:

- Foundry IPs: Pre-designed, tested components (e.g., PLLs, ADCs, SRAM).
- Macros: Pre-made digital logic for common uses (e.g., GPIO bank, SPI).

4. RISC-V:

- RISC-V ISA: An open-source instruction set architecture (ISA).
- Software gets compiled into assembly (RISC-V), then into machine code, and implemented through HDL (e.g., picorv32).

5. Software Applications to Hardware:

- **Operating Systems**: Handle I/O operations, memory allocation, and low-level system functions.
- Compilers: Convert high-level language (C/C++) to machine language.
- Assemblers: Convert compiled instructions into binary for execution.

6. SoC Design and OpenLANE:

- **ASIC Design:** Uses RTL IPs (pre-designed blocks), EDA tools (for design and simulation), and PDK data (from foundries).
- **OpenLANE**: Open-source digital ASIC design flow, automating the RTL to GDSII process using tools like Yosys, OpenSTA, and Magic.

7. Simplified RTL to GDS Flow:

- Synthesis: Converts RTL to gate-level representation.
- Floor Planning: Optimizes chip performance, power, and connectivity.
- **Placement & Routing**: Places components on the chip and establishes interconnections.
- Clock Tree Synthesis: Routes the clock signal to all sequential elements.
- **Sign-off**: Includes DRC, LVS, and STA to verify design rules, layout consistency, and timing.

<u>LABS</u>





