

SAB 8086 16-Bit Microprocessor

SAB 8086-2 8 MHz
SAB 8086-1 10 MHz

SAB 8086 5 MHz

- Direct addressing capability to 1 Mbyte of memory
- Assembly language compatible with SAB 8080 / SAB 8085
- 14-word by 16-bit register set with symmetrical operations
- 8 and 16-bit signed and unsigned arithmetic in binary or decimal including multiply and divide

- Bit, byte, word and block operations
- 24 operand addressing modes
- Clock rates up to 10 MHz (SAB 8086-1)
- Compatible with industry standard 8086
- 40-pin plastic dual-in-line package (P-DIP-40)

Figure 1 Pin Diagram

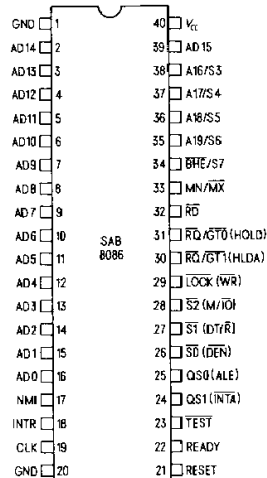


Figure 2 Pin Names

AD0-15	Address/Data	A16-19	Address
S0-2	Status	S3-7	Status
INTR	Interrupt Request	BHE	Bus High Enable
CLK	Clock	HOLD	Hold
QS0-1	Queue Status	HLDA	Hold Acknowledge
TEST	Test for Busy	WR	Write
READY	Ready	DT/R	Bus Driver Transmit/Receive
RESET	Chip Reset	DEN	Bus Driver Enable
MN/MX	Minimum/Maximum Mode	ALE	Address Latch Enable
RD	Read	INTA	Interrupt Acknowledge
RQ/GT0-1	Request/Grant	NMI	Non-Maskable Interrupt
LOCK	Bus Lock	GND	Ground
M/I/O	Memory/IO	V _{CC}	+5V

SAB 8086 is a new-generation, high-performance 16-bit microprocessor implemented in +5 V depletion load, N channel, silicon gate Siemens MYMOS technology, packaged in a 40-pin plastic dual-in-line package (P-DIP-40). It is 100 percent

compatible with the industry standard 8086. With features like string handling, 16-bit arithmetic with multiply and divide it significantly increases system performance. It is highly suited for multiprocessor applications in various configurations.

Pin Definitions and Functions

The following pin definitions are for SAB 8086 systems in **either minimum or maximum mode**. The "Local Bus" in these descriptions is the

direct multiplexed bus interface connection to the SAB 8086 (without regard to additional bus buffers).

Symbol	Pin	Input (I) Output (O)	Function															
AD0–AD15	2–16 39	I/O	ADDRESS DATA BUS These lines constitute the time multiplexed memory I/O address (T1) and data (T2, T3, T4) bus. A0 is analogous to BHE for the lower byte of the data bus, pins D7 to D0. It is low during T1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A0 to condition chip select functions. These lines are active high and float to tristate OFF during interrupt acknowledge and local bus “hold acknowledge”.															
A16/S3 A17/S4 A18/S5 A19/S6	35–38	O	ADDRESS/STATUS During T1 these are the four most significant address lines for memory operations. During I/O operations these lines are low. During memory and I/O operations, status information is available on these lines during T2, T3, TW and T4. The status of the interrupt enable flag bit (S5) is updated at the beginning of each CLK cycle. A17/S4 and A16/S3 are encoded as follows: <table><tr><th>A17/S4</th><th>A16/S3</th><th>Characteristics</th></tr><tr><td>0 (low)</td><td>0</td><td>Alternate Data</td></tr><tr><td>0</td><td>1</td><td>Stack</td></tr><tr><td>1 (high)</td><td>0</td><td>Code or None</td></tr><tr><td>1</td><td>1</td><td>Data</td></tr></table> S6 is 0 (low) This information indicates which relocation register is presently being used for data accessing. These lines float to tristate OFF during local bus “hold acknowledge”.	A17/S4	A16/S3	Characteristics	0 (low)	0	Alternate Data	0	1	Stack	1 (high)	0	Code or None	1	1	Data
A17/S4	A16/S3	Characteristics																
0 (low)	0	Alternate Data																
0	1	Stack																
1 (high)	0	Code or None																
1	1	Data																
BHE/S7	34	O	BUS HIGH ENABLE/STATUS During T1 the bus high enable signal (BHE) should be used to enable data onto the most significant half of the data bus, pins D15 to D8. Eight-bit oriented devices tied to the upper half of the bus would normally use BHE to condition chip select functions. BHE is low during T1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S7 status information is available during T2, T3, and T4. The signal is active low, and floats to tristate OFF in “hold”. It is low during T1 for the first interrupt acknowledge cycle.															
RD	32	O	READ strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the S2 pin. This signal is used to read devices which reside on the SAB 8086 local bus. RD is active low during T2, T3 and TW of any read cycle, and is guaranteed to remain high in T2 until the SAB 8086 local bus has floated. This signal floats to tristate OFF in “hold acknowledge”.															

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
READY	22	I	READY is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory I/O is synchronized by the SAB 8284B clock generator to form READY. This signal is active high. The SAB 8086 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.
INTR	18	I	INTERRUPT REQUEST is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active high.
$\overline{\text{TEST}}$	23	I	The TEST input is examined by the "wait" instruction. If this input is low execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NON-MASKABLE INTERRUPT is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a low to high initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET causes the processor to immediately terminate its present activity. The signal must be active high for at least four clock cycles. It restarts execution, as described in the Instruction Set Description, when RESET returns low. RESET is internally synchronized.
CLK	19	I	The CLOCK provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
MN/ $\overline{\text{MX}}$	33	I	MINIMUM/MAXIMUM indicates which mode the processor is to operate in. The two modes are discussed in the following sections.
V _{CC}	40		POWER SUPPLY (+5V)
GND	1, 20		GROUND (0V)

Pin Definitions and Functions (cont'd)

The following pin definitions are for the SAB 8086/8288 system in **maximum mode** (i. e. MN/M \overline{X} = GND). Only the pin functions which are

unique to maximum mode are described; all other pin functions are as already described.

Symbol	Pin	Input (I) Output (O)	Function																																				
$\overline{S2}, \overline{S1}, \overline{S0}$	26–28	O	<p>These STATUS lines are encoded as follows:</p> <table> <tr> <th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Characteristics</th></tr> <tr> <td>0 (low)</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>Read I/O Port</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>Write I/O Port</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>Halt</td></tr> <tr> <td>1 (high)</td><td>0</td><td>0</td><td>Code Access</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>Passive</td></tr> </table> <p>Status is active during T4, T1, and T2 and is returned to the passive state (1,1,1) during T3 or during TW when READY is high. This status is used by the SAB 8288A bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or TW is used to indicate the end of a bus cycle. These signals float to tristate OFF in "hold acknowledge".</p>	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics	0 (low)	0	0	Interrupt Acknowledge	0	0	1	Read I/O Port	0	1	0	Write I/O Port	0	1	1	Halt	1 (high)	0	0	Code Access	1	0	1	Read Memory	1	1	0	Write Memory	1	1	1	Passive
$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics																																				
0 (low)	0	0	Interrupt Acknowledge																																				
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0	1	1	Halt																																				
1 (high)	0	0	Code Access																																				
1	0	1	Read Memory																																				
1	1	0	Write Memory																																				
1	1	1	Passive																																				
$\overline{RQ}/\overline{GT0}, \overline{RQ}/\overline{GT1}$	30–31	I/O	<p>The REQUEST/GRANT pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT0}$ having higher priority than $\overline{RQ}/\overline{GT1}$. $\overline{RQ}/\overline{GT}$ has an internal pullup resistor so may be left unconnected. The request/grant sequence is as follows (see figure 14):</p> <ol style="list-style-type: none"> 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the SAB 8086 (pulse1). 2. During the CPU's next T4 or T1 a pulse 1 CLK wide from the SAB 8086 to the requesting master (pulse 2) indicates that the SAB 8086 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge". 3. A pulse 1 CLK wide from the requesting master indicates to the SAB 8086 (pulse 3) that the "hold" request is about to end and that the SAB 8086 can reclaim the local bus at the next CLK. <p>Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active low.</p> <p>If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met:</p> <ol style="list-style-type: none"> 1. Request occurs on or before T2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. 																																				

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function															
$\overline{\text{LOCK}}$	29	O	The LOCK output indicates that other system bus masters are not to gain control of the system bus while LOCK is active low. The LOCK signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active low, and floats to tristate OFF in "hold acknowledge".															
QS1, QS0	24–25	O	<p>The QUEUE STATUS is valid during the CLK cycle after which the queue operation is performed. QS1 and QS0 provide status to allow external tracking of the internal SAB 8086 instruction queue.</p> <table><tr><th>QS1</th><th>QS0</th><th>Characteristics</th></tr><tr><td>0 (low)</td><td>0</td><td>No Operation</td></tr><tr><td>0</td><td>1</td><td>First Byte of Op Code from Queue</td></tr><tr><td>1 (high)</td><td>0</td><td>Empty the Queue</td></tr><tr><td>1</td><td>1</td><td>Subsequent Byte from Queue</td></tr></table>	QS1	QS0	Characteristics	0 (low)	0	No Operation	0	1	First Byte of Op Code from Queue	1 (high)	0	Empty the Queue	1	1	Subsequent Byte from Queue
QS1	QS0	Characteristics																
0 (low)	0	No Operation																
0	1	First Byte of Op Code from Queue																
1 (high)	0	Empty the Queue																
1	1	Subsequent Byte from Queue																

Pin Definitions and Functions (cont'd)

The following pin definitions are for the SAB 8086 **minimum mode** (i. e. $MN/\overline{MX} = V_{CC}$). Only the pin functions which are unique to minimum

mode are described; all other pin functions are as described before.

Symbol	Pin	Input (I) Output (O)	Function
M/\overline{IO}	28	O	This STATUS LINE is logically equivalent to S2 in the maximum mode. It is used to distinguish a memory access from an I/O access. M/\overline{IO} becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (M = high, \overline{IO} = low). M/\overline{IO} floats to tristate OFF in local bus "hold acknowledge".
\overline{WR}	29	O	WRITE strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/\overline{IO} signal. \overline{WR} is active for T2, T3 and TW of any write cycle. It is active low, and floats to tristate OFF in local bus "hold acknowledge".
\overline{INTA}	24	O	INTA is used as a read strobe for interrupt acknowledge cycles. It is active low during T2, T3 and TW of each interrupt acknowledge cycle.
ALE	25	O	ADDRESS LATCH ENABLE is provided by the processor to latch the address into the SAB 8282A/SAB 8283A address latch. It is a high pulse active during T1 of any bus cycle. Note that ALE is never floated.
DT/\overline{R}	27	O	DATA TRANSMIT/RECEIVE is needed in minimum system that desires to use a SAB 8286A/SAB 8287A data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/\overline{R} is equivalent to S1 in the maximum mode, and its timing is the same as for M/\overline{IO} . (T =high, \overline{R} =low). This signal floats to tristate OFF in local bus "hold acknowledge".
\overline{DEN}	26	O	DATA ENABLE is provided as an output enable for the SAB 8286A/SAB 8287A in a minimum system which uses the transceiver. \overline{DEN} is active low during each memory and I/O access and for \overline{INTA} cycles. For a read or \overline{INTA} cycle it is active from the middle of T2 until the middle of T4, while for a write cycle it is active from the beginning of T2 until the middle of T4. \overline{DEN} floats to tristate OFF in local bus "hold acknowledge".
HOLD HLDA	30–31	I O	HOLD indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active high. The processor receiving the "hold" request will issue HLDA (high) as an acknowledgement in the middle of T4 or T1. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being low, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time. The same rules as for RQ/\overline{GT} apply regarding when the local bus will be released.

Figure 3 Functional Block Diagram

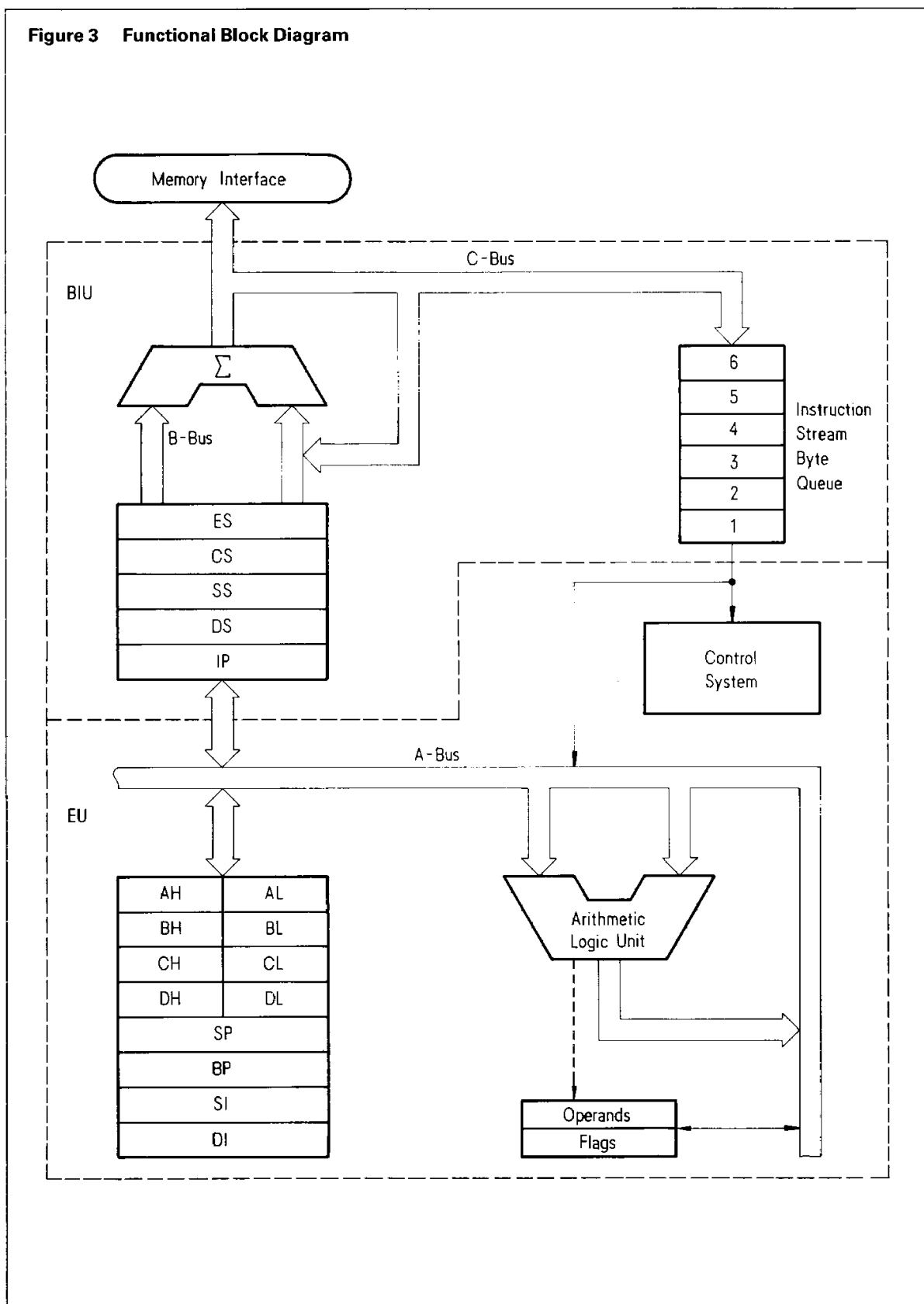
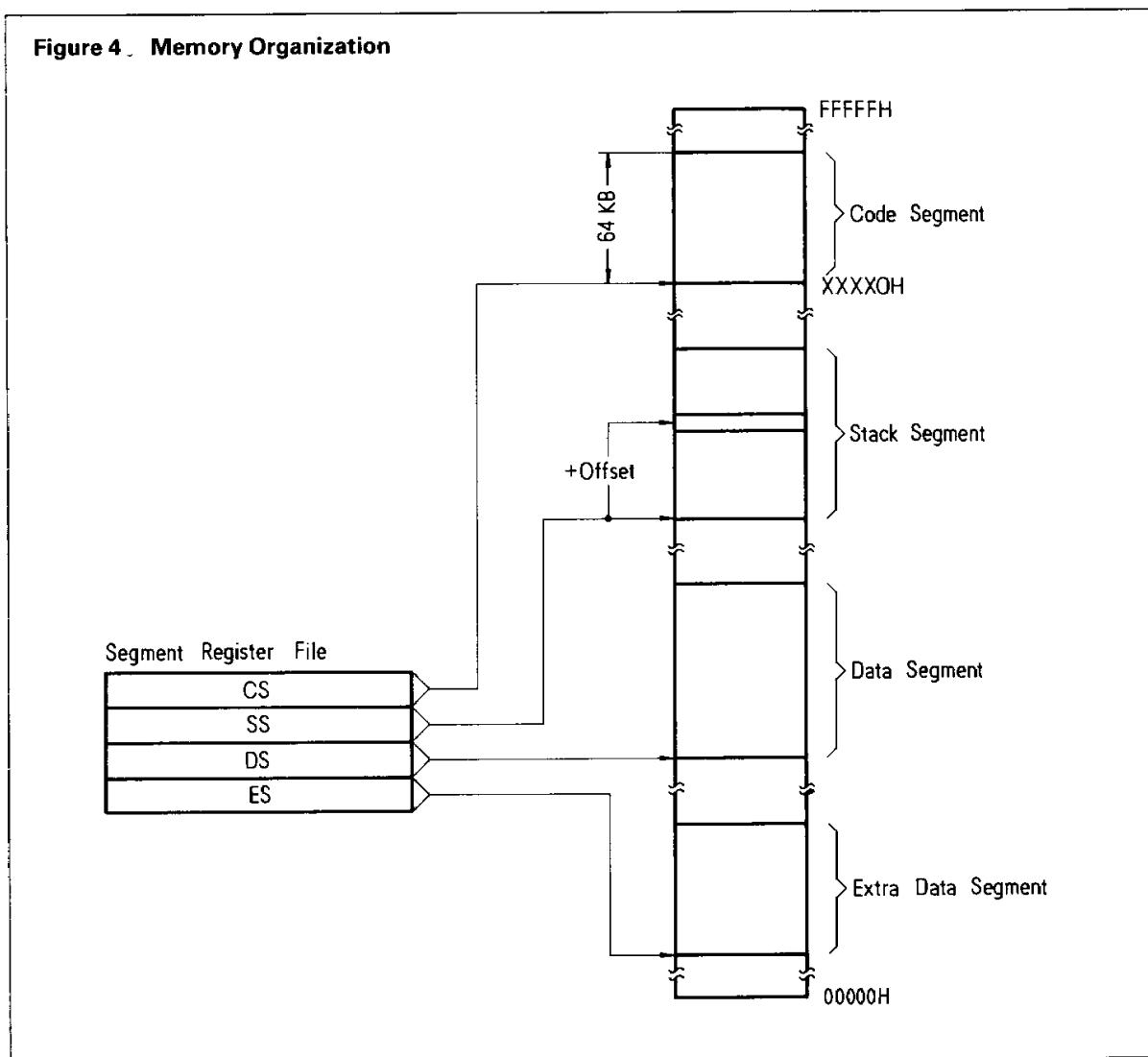


Figure 4 . Memory Organization



Functional Description

The internal functions of the SAB 8086 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the block diagram of figure 3.

The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the

queue, the BIU will attempt a word fetch memory cycle. This greatly reduces „dead time“ on the memory bus.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is logically organized as a linear array of 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory can further be logically divided into code, data, alternate data, and stack segments of up to 64 Kbytes each, with each segment falling on 16-byte boundaries (see figure 4).

Minimum and Maximum Modes

The requirements for supporting minimum and maximum mode in SAB 8086 systems are sufficiently different that they cannot be met efficiently with 40 uniquely defined pins. Consequently, the SAB 8086 is equipped with a strap pin ($\overline{MN}/\overline{MX}$) which defines the system configuration.

The definition of a certain subset of the pins changes dependent on the condition of the strap pin.

When $\overline{MN}/\overline{MX}$ pin is strapped to GND, the SAB 8086 treats pins 24 through 31 in maximum mode. An SAB 8288A bus controller interprets status information coded into $\overline{S0}$, $\overline{S1}$, $\overline{S2}$ to generate bus timing and control signals.

When the $\overline{MN}/\overline{MX}$ pin is strapped to V_{CC} , the SAB 8086 generates bus control signals itself on pins 24 through 31, as shown in parentheses in figure 1.

Bus Operation

The SAB 8086 has a combined address and data bus commonly referred to as a time multiplexed bus.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3 and T4 (see figure 5). The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "wait" states (TW) are inserted between T3 and T4. Each inserted wait state is of the same duration as a CLK cycle. Periods can occur between SAB 8086 bus cycles. These are referred to as "idle" states (Ti) or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T1 of any bus cycle the ALE (Address Latch Enable) signal is emitted (by either the processor or the SAB 8288A bus controller, depending on the $\overline{MN}/\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ are used, in maximum mode, by the bus controller to identify the type of bus transaction according to the following table:

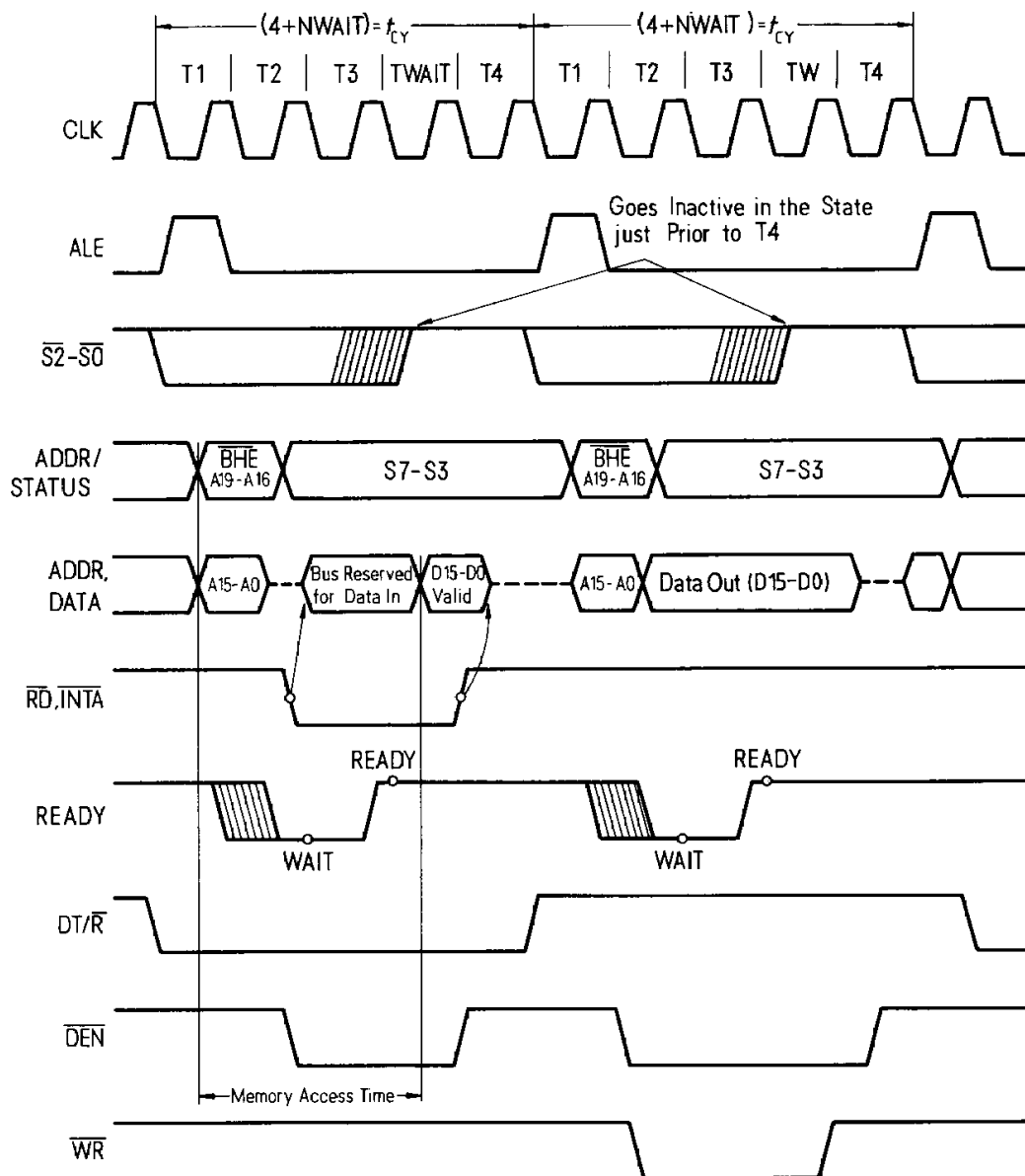
$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0 (Low)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (High)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S3 through S7 are multiplexed with high-order address bits and the \overline{BHE} signal, and are therefore valid during T2 through T4. S3 and S4 indicate which segment register (see Instruction Set Summary) was used for this bus cycle in forming the address, according to the following table:

S4	S3	Characteristics
0 (Low)	0	Alternate Data (extra segment)
0	1	Stack
1 (High)	0	Code or None
1	1	Data

S5 is a reflection of the PSW interrupt enable bit. S6 = 0 and S7 is a spare status bit.

Figure 5 Basic System Timing



I/O Addressing

In the SAB 8086, I/O operations can address up to a maximum of 64 K I/O byte registers or 32 K I/O word registers.

The I/O address appears in the same format as the memory address on bus lines A15 to A0. The address lines A19 to A16 are zero in I/O operations.

The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

System Components

SAB 8282A	Octal Latch
SAB 8283A	Octal Latch (inverting)
SAB 8284B	Clock Generator and Driver
SAB 8286A	Octal Bus Transceiver
SAB 8287A	Octal Bus Transceiver (inverting)
SAB 8288A	Bus Controller
SAB 8289	Bus Arbiter
SAB 8259A	Programmable Interrupt Controller

Typical Applications

SAB 8086 is a general-purpose 16-bit microprocessor which can be used for applications ranging from process control to data processing. Figures 6 and 7 show typical system configurations for SAB 8086 family components.

Figure 6 Minimum Mode SAB 8086 Typical System Configuration

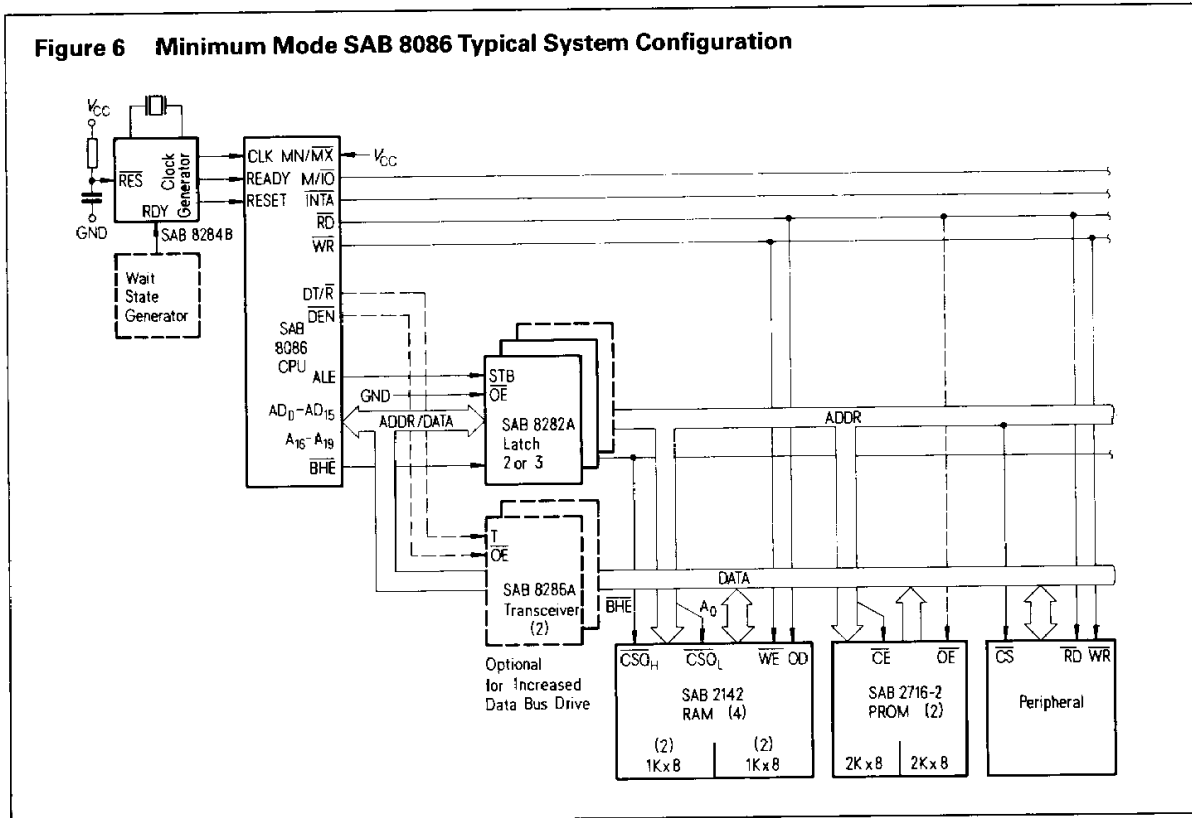
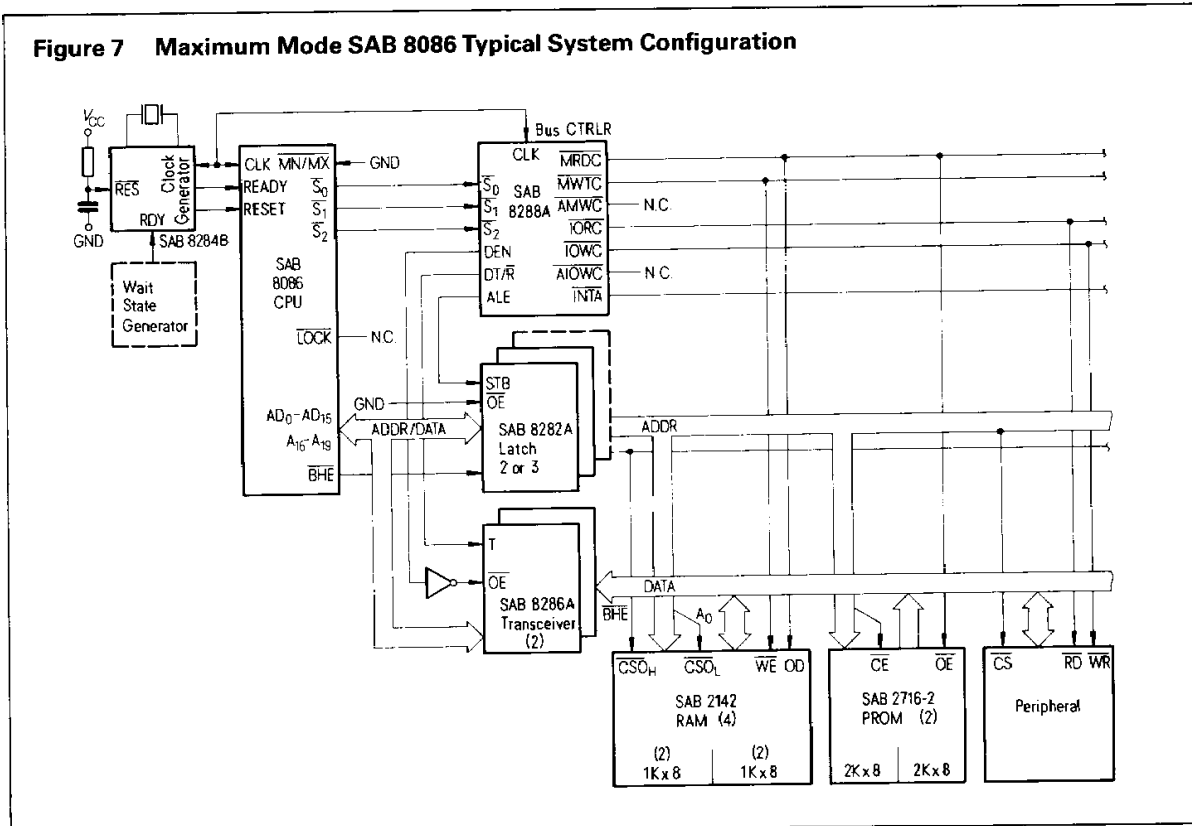


Figure 7 Maximum Mode SAB 8086 Typical System Configuration



Instruction Set Summary

Data Transfer

MOV = Move:

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register / memory to / from register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w=1
Immediate to register	1 0 1 1 w reg	data	data if w=1	
Memory to accumulator	1 0 1 0 0 0 w	addr-low	addr-high	
Accumulator to memory	1 0 1 0 0 1 w	addr-low	addr-high	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		

PUSH = Push:

Register/memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m
Register	0 1 0 1 0 reg	
Segment register	0 0 0 reg 1 1 0	

POP = Pop:

Register/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m
Register	0 1 0 1 1 reg	
Segment register	0 0 0 reg 1 1 1	

XCHG = Exchange:

Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m
Register with accumulator	1 0 0 1 0 reg	

IN = Input from:

Fixed port	1 1 1 0 0 1 0 w	port
Variable port	1 1 1 0 1 1 0 w	

OUT = Output to:

Fixed port

7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0

1 1 1 0 0 1 1 w	port
-----------------	------

Variable port

1 1 1 0 1 1 1 w

XLAT = Translate byte to AL

1 1 0 1 0 1 1 1

LEA = Load EA to register

1 0 0 0 1 1 0 1	mod reg r/m
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LDS = Load pointer to DS

1 1 0 0 0 1 0 1	mod reg r/m
-----------------	-------------

LES = Load pointer to ES

1 1 0 0 0 1 0 0	mod reg r/m
-----------------	-------------

LAHF = Load AH with flags

1 0 0 1 1 1 1 1

SAHF = Store AH into flags

1 0 0 1 1 1 1 0

PUSHF = Push flags

1 0 0 1 1 1 0 0

POPF = Pop flags

1 0 0 1 1 1 0 1

Arithmetic

ADD = Add:

Reg./memory with register to either

0 0 0 0 0 0 d w	mod reg r/m
-----------------	-------------

Immediate to register/memory

1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s:w=01
-----------------	---------------	------	----------------

Immediate to accumulator

0 0 0 0 0 1 0 w	data	data if w=1
-----------------	------	-------------

ADC = Add with carry:

Reg./memory with register to either

0 0 0 1 0 0 d w	mod reg r/m
-----------------	-------------

Immediate to register/memory

1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s:w=01
-----------------	---------------	------	----------------

Immediate to accumulator

0 0 0 1 0 1 0 w	data	data if w=1
-----------------	------	-------------

INC = Increment:

Register/memory

1 1 1 1 1 1 1 w	mod 0 0 0 r/m
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Register

0 1 0 0 0 reg

AAA = ASCII adjust for add

0 0 1 1 0 1 1 1

DAA = Decimal adjust for add

0 0 1 0 0 1 1 1

SUB = Subtract:

Reg./memory and register to either

Immediate from register/memory

Immediate from accumulator

7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0

0 0 1 0 1 0 d w	mod reg r/m		
1 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s:w=01
0 0 1 0 1 1 0 w	data	data if w=1	

SBB = Subtract with borrow:

Reg./memory and register to either

Immediate from register/memory

Immediate from accumulator

0 0 0 1 1 0 d w	mod reg r/m		
1 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s:w=01
0 0 0 1 1 1 0 w	data	data if w=1	

DEC = Decrement:

Register/memory

Register

NEG = Change sign

7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0

1 1 1 1 1 1 1 w	mod 0 0 1 r/m
0 1 0 0 1 reg	
1 1 1 1 0 1 1 w	mod 0 1 1 r/m

CMP = Compare:

Register/memory and register

Immediate with register/memory

Immediate with accumulator

AAS = ASCII adjust for subtract

DAS = Decimal adjust for subtract

MUL = Multiply (unsigned)

IMUL = Integer multiply (signed)

AAM = ASCII adjust for multiply

DIV = Divide (unsigned)

IDIV = Integer divide (signed)

AAD = ASCII adjust for divide

CBW = Convert byte to word

CWD = Convert word to double word

0 0 1 1 1 0 d w	mod reg r/m		
1 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s:w=01
0 0 1 1 1 1 0 w	data	data if w=1	
0 0 1 1 1 1 1			
0 0 1 0 1 1 1			
1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
1 0 0 1 1 0 0 0			
1 0 0 1 1 0 0 1			

Logic

NOT = Invert

7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0

1 1 1 1 0 1 1 w	mod 0 1 0 r/m
-----------------	---------------

SHL/SAL = Shift logical/arithmetic left

1 1 0 1 0 0 v w	mod 1 0 0 r/m
-----------------	---------------

SHR = Shift logical right

1 1 0 1 0 0 v w	mod 1 0 1 r/m
-----------------	---------------

SAR = Shift arithmetic right

1 1 0 1 0 0 v w	mod 1 1 1 r/m
-----------------	---------------

ROL = Rotate left

1 1 0 1 0 0 v w	mod 0 0 0 r/m
-----------------	---------------

ROR = Rotate right

1 1 0 1 0 0 v w	mod 0 0 1 r/m
-----------------	---------------

RCL = Rotate through carry flag left

1 1 0 1 0 0 v w	mod 0 1 0 r/m
-----------------	---------------

RCR = Rotate through carry flag right

1 1 0 1 0 0 v w	mod 0 1 1 r/m
-----------------	---------------

AND = And:

Reg./memory and register to either

0 0 1 0 0 0 d w	mod reg r/m
-----------------	-------------

Immediate to register/memory

1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w=1
-----------------	---------------	------	-------------

Immediate to accumulator

0 0 1 0 0 1 0 w	data	data if w=1
-----------------	------	-------------

TEST = And function to flags, no result:

Register/memory and register

1 0 0 0 0 1 0 w	mod reg r/m
-----------------	-------------

Immediate data and register/memory

1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w=1
-----------------	---------------	------	-------------

Immediate data and accumulator

1 0 1 0 1 0 0 w	data	data if w=1
-----------------	------	-------------

OR = Or:

Reg./memory and register to either

0 0 0 0 1 0 d w	mod reg r/m
-----------------	-------------

Immediate to register/memory

1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w=1
-----------------	---------------	------	-------------

Immediate to accumulator

0 0 0 0 1 1 0 w	data	data if w=1
-----------------	------	-------------

XOR = Exclusive Or:

Reg./memory and register to either

0 0 1 1 0 0 d w	mod reg r/m
-----------------	-------------

Immediate to register/memory

1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w=1
-----------------	---------------	------	-------------

Immediate to accumulator

0 0 1 1 0 1 0 w	data	data if w=1
-----------------	------	-------------

String Manipulation

7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0

REP = Repeat

1 1 1 1 0 0 1 z

MOVS = Move byte/word

1 0 1 0 0 1 0 w

CMPS = Compare byte/word

1 0 1 0 0 1 1 w

SCAS = Scan byte/word

1 0 1 0 1 1 1 w

LODS = Load byte/word to AL/AX

1 0 1 0 1 1 0 w

STOS = Store byte/word from AL/A

1 0 1 0 1 0 1 w

Control Transfer**CALL** = Call:

Direct within segment

1 1 1 0 1 0 0 0	disp-low	disp-high
-----------------	----------	-----------

Indirect within segment

1 1 1 1 1 1 1 1	mod 0 1 0 r/m
-----------------	---------------

Direct intersegment

1 0 0 1 1 0 1 0	offset-low	offset-high
	seg-low	seg-high

Indirect intersegment

1 1 1 1 1 1 1 1	mod 0 1 1 r/m
-----------------	---------------

JMP = Unconditional jump:

Direct within segment

1 1 1 0 1 0 0 1	disp-low	disp-high
-----------------	----------	-----------

Direct within segment short

1 1 1 0 1 0 1 1	disp
-----------------	------

Indirect within segment

1 1 1 1 1 1 1 1	mod 1 0 0 r/m
-----------------	---------------

Direct intersegment

1 1 1 0 1 0 1 0	offset-low	offset-high
	seg-low	seg-high

Indirect intersegment

1 1 1 1 1 1 1 1	mod 1 0 1 r/m
-----------------	---------------

RET = Return from CALL:

7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0

Within segment

1 1 0 0 0 0 1 1

Within seg. adding immediate to SP

1 1 0 0 0 0 1 0	data-low	data-high
-----------------	----------	-----------

Intersegment

1 1 0 0 1 0 1 1

Intersegment adding immediate to SP

1 1 0 0 1 0 1 0	data-low	data-high
-----------------	----------	-----------

JE/JZ = Jump on equal/zero

0 1 1 1 0 1 0 0	disp
-----------------	------

JL/JNGE = Jump on less/not greater or equal

0 1 1 1 1 1 0 0	disp
-----------------	------

JLE/JNG = Jump on less or equal/not greater

0 1 1 1 1 1 1 0	disp
-----------------	------

JB/JNAE = Jump on below/not above or equal

0 1 1 1 0 0 1 0	disp
-----------------	------

JBE/JNA = Jump on below or equal/not above

0 1 1 1 0 1 1 0	disp
-----------------	------

JP/JPE = Jump on parity/parity even

0 1 1 1 1 0 1 0	disp
-----------------	------

JO = Jump on overflow

0 1 1 1 0 0 0 0	disp
-----------------	------

JS = Jump on sign

0 1 1 1 1 0 0 0	disp
-----------------	------

JNE/JNZ = Jump on not equal/not zero

0 1 1 1 0 1 0 1	disp
-----------------	------

JNL/JGE = Jump on not less/greater or equal

0 1 1 1 1 1 0 1	disp
-----------------	------

JNLE/JG = Jump on not less or equal/greater

0 1 1 1 1 1 1 1	disp
-----------------	------

JNB/JAE = Jump on not below/above or equal

0 1 1 1 0 0 1 1	disp
-----------------	------

JNBE/JA = Jump on not below or equal/above

0 1 1 1 0 1 1 1	disp
-----------------	------

JNP/JPO = Jump on not parity/parity odd

0 1 1 1 1 0 1 1	disp
-----------------	------

JNO = Jump on not overflow

0 1 1 1 0 0 0 1	disp
-----------------	------

JNS = Jump on not sign

0 1 1 1 1 0 0 1	disp
-----------------	------

LOOP = Loop CX times

1 1 1 0 0 0 1 0	disp
-----------------	------

LOOPZ/LOOPE = Loop while zero/equal

1 1 1 0 0 0 0 1	disp
-----------------	------

LOOPNZ/LOOPNE = Loop while not zero/equal

1 1 1 0 0 0 0 0	disp
-----------------	------

JCXZ = Jump on CX zero

1 1 1 0 0 0 1 1	disp
-----------------	------

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
INT = Interrupt		
Type specified	1 1 0 0 1 1 0 1	type
Type 3	1 1 0 0 1 1 0 0	
INTO = Interrupt on overflow	1 1 0 0 1 1 1 0	
IRET = Interrupt return	1 1 0 0 1 1 1 1	
Processor Control		
CLC = Clear carry	1 1 1 1 1 0 0 0	
CMC = Complement carry	1 1 1 1 0 1 0 1	
STC = Set carry	1 1 1 1 1 0 0 1	
CLD = Clear direction	1 1 1 1 1 1 0 0	
STD = Set direction	1 1 1 1 1 1 0 1	
CLI = Clear interrupt	1 1 1 1 1 0 1 0	
STI = Set interrupt	1 1 1 1 1 0 1 1	
HLT = Halt	1 1 1 1 0 1 0 0	
WAIT = Wait	1 0 0 1 1 0 1 1	
ESC = Escape (to external device)	1 1 0 1 1 x x x	mod x x x r/m
LOCK = Bus lock prefix	1 1 1 1 0 0 0 0	

Notes:

AL = 8-bit accumulator
 AX = 16-bit accumulator
 CX = Count register
 DS = Data segment
 ES = Extra segment
 Above/below refers to unsigned value.
 Greater = more positive;
 Less = less positive (more negative) signed values
 if d = 1 then "to" reg; if d = 0 then "from" reg
 if w = 1 then word instruction; if w = 0 then byte instruction
 if s:w = 01 then 16-bits of immediate data from the operand
 if s:w = 11 then an immediate data byte is sign-extended to form the 16-bit operand
 if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
 x = don't care
 z is used for string primitives for comparison with ZF FLAG

if mod = 11 then r/m is treated as a REG field
 if mod = 00 then DISP = 0*, disp-low and disp-high are absent
 if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp high is absent
 if mod = 10 then DISP = disp-high: disp low
 if r/m = 000 then EA = (BX) + (SI) + DISP
 if r/m = 001 then EA = (BX) + (DI) + DISP
 if r/m = 010 then EA = (BP) + (SI) + DISP
 if r/m = 011 then EA = (BP) + (DI) + DISP
 if r/m = 100 then EA = (SI) + DISP
 if r/m = 101 then EA = (DI) + DISP
 if r/m = 110 then EA = (BP) + DISP*
 if r/m = 111 then EA = (BX) + DISP
 DISP follows 2nd byte of instruction (before data if required)

* except if mod = 00 and r/m = 110 then EA = disp-high:disp-low.

Segment Override Prefix

0 0 1 reg 1 1 0

REG is assigned according to the following table

16-bit (w=1)	8-bit (w=0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instruction which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):
 X:(AF):X:(PF):X:(CF)

Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−1.0 to +7V
Power dissipation	2.5 W

Note:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

SAB 8086: $T_A = 0$ to 70°C, $V_{CC} = 5V \pm 10\%$

SAB 8086-1/8086-2: $T_A = 0$ to 70°C, $V_{CC} = 5V \pm 5\%$

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input low voltage	V_{IL}	−0.5	+0.8	V	—
Input high voltage	V_{IH}	2.0	$V_{CC} + 0.5$	V	—
Output low voltage	V_{OL}	—	0.45	V	$I_{OL} = 2.5$ mA
Output high voltage	V_{OH}	2.4	—	V	$I_{OH} = -400$ μ A
Power supply current SAB 8086 SAB 8086-2 SAB 8086-1	I_{CC}	— — —	340 350 360	mA mA mA	All outputs open $T_A = 25^\circ\text{C}$
Input leakage current	I_{LI}	—	± 10	μ A	$0V \leq V_{IN} \leq V_{CC}$
Output leakage current	I_{LO}	—	± 10	μ A	$0.45V \leq V_{OUT} \leq V_{CC}$
Clock input low voltage	V_{CL}	−0.5	+0.6	V	—
Clock input high voltage	V_{CH}	3.9	$V_{CC} + 1.0$	V	—
Capacitance of input buffer (all inputs except AD0 to AD15, RQ/GT)	C_{IN}	—	15	pF	$f_c = 1$ MHz
Capacitance of I/O buffer (AD0 to AD15, RQ/GT)	C_{IO}	—	15	pF	$f_c = 1$ MHz

AC Characteristics for SAB 8086/8086-2

SAB 8086: $T_A = 0$ to 70°C , $V_{CC} = 5\text{V} \pm 10\%$

SAB 8086-2: $T_A = 0$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$

Minimum Complexity System (figures 8, 9, 12, 15)

Timing Requirements

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 8086		SAB 8086-2			
		min.	max.	min.	max.		
CLK cycle period SAB 8086	t_{CLCL}	200	500	125	500	ns	—
CLK low time	t_{CLCH}	118	—	68	—	ns	—
CLK high time	t_{CHCL}	69	—	44	—	ns	—
CLK rise time	t_{CH1CH2}	—	10	—	10	ns	from 1.0 to 3.5V
CLK fall time	t_{CL2CL1}	—	10	—	10	ns	from 3.5 to 1.0V
Data in setup time	t_{DVCL}	30	—	20	—	ns	—
Data in hold time	t_{CLDX}	10	—	10	—	ns	—
RDY setup time into SAB 8284A ¹⁾ ²⁾	t_{R1VCL}	35	—	35	—	ns	—
RDY hold time into SAB 8284A ¹⁾ ²⁾	t_{CLR1X}	0	—	0	—	ns	—
READY setup time into SAB 8086	t_{RYHCH}	118	—	68	—	ns	—
READY hold time into SAB 8086	t_{CHRYX}	30	—	20	—	ns	—
READY inactive to CLK ³⁾	t_{RYLCL}	—8	—	—8	—	ns	—
HOLD setup time	t_{HVCH}	35	—	20	—	ns	—
INTR, NMI, $\overline{\text{TEST}}$ setup time ²⁾	t_{INVCH}	30	—	15	—	ns	—
Input rise time (except CLK)	t_{ILIH}	—	20	—	20	ns	from 0.8 to 2.0V
Input fall time (except CLK)	t_{IHIL}	—	12	—	12	ns	from 2.0 to 0.8V

¹⁾ Signal at SAB 8284B shown for reference only.

²⁾ Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

³⁾ Applies only to T2 state {8 ns into T3}.

Timing Responses

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 8086		SAB 8086-2			
		min.	max.	min.	max.		
Address valid delay	t_{CLAV}	10	110	10	60	ns	$C_L = 20$ to 100 pF for all SAB 8086 outputs (in addition to SAB 8086 self-load)
Address hold time	t_{CLAX}	10	—	10	—	ns	
Address float delay	t_{CLAZ}	t_{CLAX}	80	t_{CLAX}	50	ns	
ALE width	t_{LHLL}	$t_{CLCH}-20$	—	$t_{CLCH}-10$	—	ns	
ALE active delay	t_{CLLH}	—	80	—	50	ns	
ALE inactive delay	t_{CHLL}	—	85	—	55	ns	
Address hold time to ALE inactive	t_{LLAX}	$t_{CHCL}-10$	—	$t_{CHCL}-10$	—	ns	
Data valid delay	t_{CLDV}	10	110	10	60	ns	
Data hold time	t_{CHDX}	10	—	10	—	ns	
Data hold time after WR	t_{WHDX}	$t_{CLCH}-30$	—	$t_{CLCH}-30$	—	ns	
Control active delay 1	t_{CVCTV}	10	110	10	70	ns	
Control active delay 2	t_{CHCTV}	10	110	10	60	ns	
Control inactive delay	t_{CVCTX}	10	110	10	70	ns	
Address float to READ active	t_{AZRL}	0	—	0	—	ns	
\overline{RD} active delay	t_{CLRL}	10	165	10	100	ns	
\overline{RD} inactive delay	t_{CLRH}	10	150	10	80	ns	
\overline{RD} inactive to next address active	t_{RHAV}	$t_{CLCL}-45$	—	$t_{CLCL}-40$	—	ns	
HLDA valid delay	t_{CLHAV}	10	160	10	100	ns	
\overline{RD} width	t_{RLRH}	$2 t_{CLCL}-75$	—	$2 t_{CLCL}-50$	—	ns	
\overline{WR} width	t_{WLWH}	$2 t_{CLCL}-60$	—	$2 t_{CLCL}-40$	—	ns	
Address valid to ALE low	t_{AVAL}	$t_{CLCH}-60$	—	$t_{CLCH}-40$	—	ns	
Output rise time	t_{OLOH}	—	20	—	20	ns	from 0.8 to 2.0V
Output fall time	t_{OHOL}	—	12	—	12	ns	from 2.0 to 0.8V

SAB 8086

Maximum Mode System (using SAB 8288A bus controller) (figures 10 to 14) Timing Requirements

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 8086		SAB 8086-2			
		min.	max.	min.	max.		
CLK cycle period SAB 8086	t_{CLCL}	200	500	125	500	ns	—
CLK low time	t_{CLCH}	118	—	68	—	ns	—
CLK high time	t_{CHCL}	69	—	44	—	ns	—
CLK rise time	t_{CH1CH2}	—	10	—	10	ns	from 1.0 to 3.5V
CLK fall time	t_{CL2CL1}	—	10	—	10	ns	from 3.5 to 1.0V
Data in setup time	t_{DVCL}	30	—	20	—	ns	—
Data in hold time	t_{CLDX}	10	—	10	—	ns	—
RDY setup time into SAB 8284A ^{1) 2)}	t_{R1VCL}	35	—	35	—	ns	—
RDY hold time into SAB 8284A ^{1) 2)}	t_{CLR1X}	0	—	0	—	ns	—
READY setup time into SAB 8086	t_{RYHCH}	118	—	68	—	ns	—
READY hold time into SAB 8086	t_{CHRYX}	30	—	20	—	ns	—
READY inactive to CLK ⁴⁾	t_{RYLCL}	—8	—	—8	—	ns	—
Setup time for recognition (INTR, NMI, TEST) ²⁾	t_{INVCH}	30	—	15	—	ns	—
$\overline{RQ}/\overline{GT}$ setup time	t_{GVCH}	30	—	15	—	ns	—
\overline{RQ} hold time into SAB 8086	t_{CHGX}	40	—	30	—	ns	—
Input rise time (except CLK)	t_{ILIH}	—	20	—	20	ns	from 0.8 to 2.0V
Input fall time (except CLK)	t_{IHIL}	—	12	—	12	ns	from 2.0 to 0.8V

¹⁾ Signal at SAB 8284B or SAB 8288A shown for reference only.

²⁾ Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

³⁾ Applies only to T3 and wait states.

⁴⁾ Applies only to T2 state (8 ns into T3).

Timing Responses

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 8086		SAB 8086-2			
		min.	max.	min.	max.		
Command active delay ¹⁾	t_{CLML}	10	35	10	35	ns	C _L = 20 to 100 pF for all SAB 8086 outputs (in addition to SAB 8086 self-load)
Command inactive delay ¹⁾	t_{CLMH}	10	35	10	35	ns	
READY active to status passive ³⁾	t_{RYHSH}	—	110	—	65	ns	
Status active delay	t_{CHSV}	10	110	10	60	ns	
Status inactive delay	t_{CLSH}	10	130	10	70	ns	
Address valid delay	t_{CLAV}	10	110	10	60	ns	
Address hold time	t_{CLAX}	10	—	10	—	ns	
Address float delay	t_{CLAZ}	t_{CLAX}	80	t_{CLAX}	50	ns	
Status valid to ALE high ¹⁾	t_{SVLH}	—	20	—	20	ns	
Status valid to MCE high ¹⁾	t_{SVMCH}	—	20	—	20	ns	
CLK low to ALE valid ¹⁾	t_{CLLH}	—	20	—	20	ns	
CLK low to MCE high ¹⁾	t_{CLMCH}	—	20	—	20	ns	
ALE inactive delay ¹⁾	t_{CHLL}	4	15	4	15	ns	
Data valid delay	t_{CLDV}	10	110	10	60	ns	
Data hold time	t_{CHDX}	10	—	10	—	ns	
Control active delay ¹⁾	t_{CVNV}	5	45	5	45	ns	
Control inactive delay ¹⁾	t_{CVNX}	10	45	10	45	ns	

¹⁾ Signal at SAB 8284B or SAB 8288A shown for reference only.

²⁾ Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

³⁾ Applies only to T3 and wait states.

⁴⁾ Applies only to T2 state (8 ns into T3).

Timing Responses (cont'd)

Parameter	Symbol	Limit values				Unit	Test conditions
		SAB 8086		SAB 8086-2			
		min.	max.	min.	max.		
Address float to READ active	t_{AZRL}	0	—	0	—	ns	
\overline{RD} active delay	t_{CLRL}	10	165	10	100	ns	$C_L = 20$ to 100 pF for all SAB 8086 outputs (in addition to SAB 8086 self-load)
\overline{RD} inactive delay	t_{CLRH}	10	150	10	80	ns	
\overline{RD} inactive to next address active	t_{RHAV}	$t_{CLCL}-45$	—	$t_{CLCL}-40$	—	ns	
Direction control active delay ¹⁾	t_{CHDTL}	—	50	—	50	ns	
Direction control inactive delay ¹⁾	t_{CHDTH}	—	30	—	30	ns	
\overline{GT} active delay	t_{CLGL}	0	85	0	50	ns	
\overline{GT} inactive delay	t_{CLGH}	0	85	0	50	ns	
\overline{RD} width	t_{RLRH}	$2t_{CLCL}-75$	—	$2t_{CLCL}-50$	—	ns	
Output rise time	t_{OLOH}	—	20	—	20	ns	from 0.8 to 2.0V
Output fall time	t_{OHOL}	—	12	—	12	ns	from 2.0 to 0.8V

¹⁾ Signal at SAB 8284B or SAB 8288A shown for reference only.

²⁾ Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

³⁾ Applies only to T3 and wait states.

⁴⁾ Applies only to T2 state (8 ns into T3).

AC Characteristics for SAB 8086-1

$T_A = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$

Minimum Complexity System (figures 8, 9, 12, 15)

Timing Requirements (preliminary)

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
CLK cycle period	t_{CLCL}	100	500	ns	—
CLK low time	t_{CLCH}	53	—	ns	—
CLK high time	t_{CHCL}	39	—	ns	—
CLK rise time	t_{CH1CH2}	—	10	ns	from 1.0 to 3.5V
CLK fall time	t_{CL1CL2}	—	10	ns	from 3.5 to 1.0V
Data in setup time	t_{DVCL}	5	—	ns	—
Data in hold time	t_{CLDX}	10	—	ns	—
RDY setup time into SAB 8284A ¹⁾²⁾	t_{R1VCL}	35	—	ns	—
RDY hold time into SAB 8284A ¹⁾²⁾	t_{CLR1X}	0	—	ns	—
READY setup time into SAB 8086	t_{RYHCH}	53	—	ns	—
READY hold time into SAB 8086	t_{CHRYX}	20	—	ns	—
READY inactive to CLK ³⁾	t_{RYLCL}	—10	—	ns	—
HOLD setup time	t_{HVCH}	20	—	ns	—
INTR, NMI, $\overline{\text{TEST}}$ setup time ²⁾	t_{INVCH}	15	—	ns	—
Input rise time (except CLK)	t_{ILIH}	—	20	ns	from 0.8 to 2.0V
Input fall time (except CLK)	t_{ILHIL}	—	12	ns	from 2.0 to 0.8V

¹⁾ Signal at SAB 8284B shown for reference only.

²⁾ Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

³⁾ Applies only to T2 state (8 ns into T3).

Timing Responses SAB 8086-1 (preliminary)

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Address valid delay	t_{CLAV}	10	50	ns	$C_L = 20$ to 100 pF for all SAB 8086 outputs (in addition to SAB 8086 self-load)
Address hold time	t_{CLAX}	10	–	ns	
Address float delay	t_{CLAZ}	10	40	ns	
ALE width	t_{LHLL}	$t_{CLCH}-10$	–	ns	
ALE active delay	t_{CLLH}	–	40	ns	
ALE inactive delay	t_{CHLL}	–	45	ns	
Address hold time to ALE inactive	t_{LLAX}	$t_{CHCL}-10$	–	ns	
Data valid delay	t_{CLDV}	10	50	ns	
Data hold time	t_{CHDX}	10	–	ns	
Data hold time after WR	t_{WHDX}	$t_{CLCH}-25$	–	ns	
Control active delay 1	t_{CVCTX}	10	50	ns	
Control active delay 2	t_{CHCTV}	10	45	ns	
Control inactive delay	t_{CVCTX}	10	50	ns	
Address float to READ active	t_{AZRL}	0	–	ns	
\overline{RD} active delay	t_{CLRL}	10	70	ns	
\overline{RD} inactive delay	t_{CLRH}	10	60	ns	
\overline{RD} inactive to next address active	t_{RHAV}	$t_{CLCL}-35$	–	ns	
HLDA valid delay	t_{CLHAV}	10	60	ns	
\overline{RD} width	t_{RLRH}	$2t_{CLCL}-40$	–	ns	
\overline{WR} width	t_{WLWH}	$2t_{CLCL}-35$	–	ns	
Address valid to ALE low	t_{AVAL}	$t_{CLCH}-35$	–	ns	
Output rise time	t_{OLOH}	–	20	ns	from 0.8 to 2.0V
Output fall time	t_{OHOL}	–	12	ns	from 2.0 to 0.8V

Maximum Mode System (using SAB 8288A bus controller) (figures 10-14)
Timing Requirements SAB 8086-1 (preliminary)

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
CLK cycle period	t_{CLCL}	100	500	ns	—
CLK low time	t_{CLCH}	53	—	ns	—
CLK high time	t_{CHCL}	39	—	ns	—
CLK rise time	t_{CH1CH2}	—	10	ns	from 1.0 to 3.5V
CLK fall time	t_{CL2CL1}	—	10	ns	from 3.5 to 1.0V
Data in setup time	t_{DVCL}	5	—	ns	—
Data in hold time	t_{CLDX}	10	—	ns	—
RDY setup time into SAB 8284A ¹⁾²⁾	t_{R1VCL}	35	—	ns	—
RDY hold time into SAB 8284A ¹⁾²⁾	t_{CLR1X}	0	—	ns	—
READY setup time into SAB 8086	t_{RYHCH}	53	—	ns	—
READY hold time into SAB 8086	t_{CHRYX}	20	—	ns	—
READY inactive to CLK ³⁾	t_{RYLCL}	–10	—	ns	—
Setup time for recognition (INTR, NMI, TEST) ²⁾	t_{INVCH}	15	—	ns	—
$\overline{RQ}/\overline{GT}$ setup time	t_{GVCH}	12	—	ns	—
\overline{RQ} hold time into SAB 8086	t_{CHGX}	20	—	ns	—
Input rise time (except CLK)	t_{ILIH}	—	20	ns	from 0.8 to 2.0V
Input fall time (except CLK)	t_{IHIL}	—	12	ns	from 2.0 to 0.8V

¹⁾ Signal at SAB 8284B or SAB 8288A shown for reference only.

²⁾ Setup requirement for asynchronous signal only to guarantee recognition at next CLK.

³⁾ Applies only to T2 state (8 ns into T3).

Timing Responses SAB 8086-1 (preliminary)

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Command active delay ¹⁾	t_{CLML}	10	35	ns	C _L = 20 to 100 pF for all SAB 8086 outputs (in addition to SAB 8086 self-load)
Command inactive delay ¹⁾	t_{CLMH}	10	35	ns	
READY active to status passive ²⁾	t_{RYHSH}	—	45	ns	
Status active delay	t_{CHSV}	10	45	ns	
Status inactive delay	t_{CLSH}	10	55	ns	
Address valid delay	t_{CLAV}	10	50	ns	
Address hold time	t_{CLAX}	10	—	ns	
Address float delay	t_{CLAZ}	10	40	ns	
Status valid to ALE high ¹⁾	t_{SVLH}	—	20	ns	
Status valid to MCE high ¹⁾	t_{SVMCH}	—	20	ns	
CLK low to ALE valid ¹⁾	t_{CLLH}	—	20	ns	
CLK low to MCE high ¹⁾	t_{CLMCH}	—	20	ns	
ALE inactive delay ¹⁾	t_{CHLL}	4	15	ns	
Data valid delay	t_{CLDV}	10	50	ns	
Data hold time	t_{CHDX}	10	—	ns	
Control active delay ¹⁾	t_{CVNV}	5	45	ns	
Control inactive delay ¹⁾	t_{CVNX}	10	45	ns	

¹⁾ Signal at SAB 8284B or SAB 8288A shown for reference only.

²⁾ Applies only to T3 and wait states.

Timing Responses SAB 8086-1 (cont'd)
(preliminary)

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Address float to READ active	t_{AZRL}	0	—	ns	$C_L = 20$ to 100 pF for all SAB 8086 outputs (in addition to SAB 8086 self-load)
\overline{RD} active delay	t_{CLRL}	10	70	ns	
\overline{RD} inactive delay	t_{CLRH}	10	60	ns	
\overline{RD} inactive to next address active	t_{RHAV}	$t_{CLCL}-35$	—		
Direction control active delay ¹⁾	t_{CHDTL}	—	50	ns	
Direction control inactive delay ¹⁾	t_{CHDTH}	—	30	ns	
\overline{GT} active delay	t_{CLGL}	0	45	ns	
\overline{GT} inactive delay	t_{CLGH}	0	45	ns	
\overline{RD} width	t_{RLRH}	$2 t_{CLCL}-40$	—	ns	
Output rise time	t_{OLOH}	—	20	ns	from 0.8 to 2.0V
Output fall time	t_{OHOL}	—	12	ns	from 2.0 to 0.8V

¹⁾ Signal at SAB 8284B or SAB 8288A shown for reference only.

²⁾ Applies only to T3 and wait states.

Figure 8 Bus Timing – Minimum Mode System

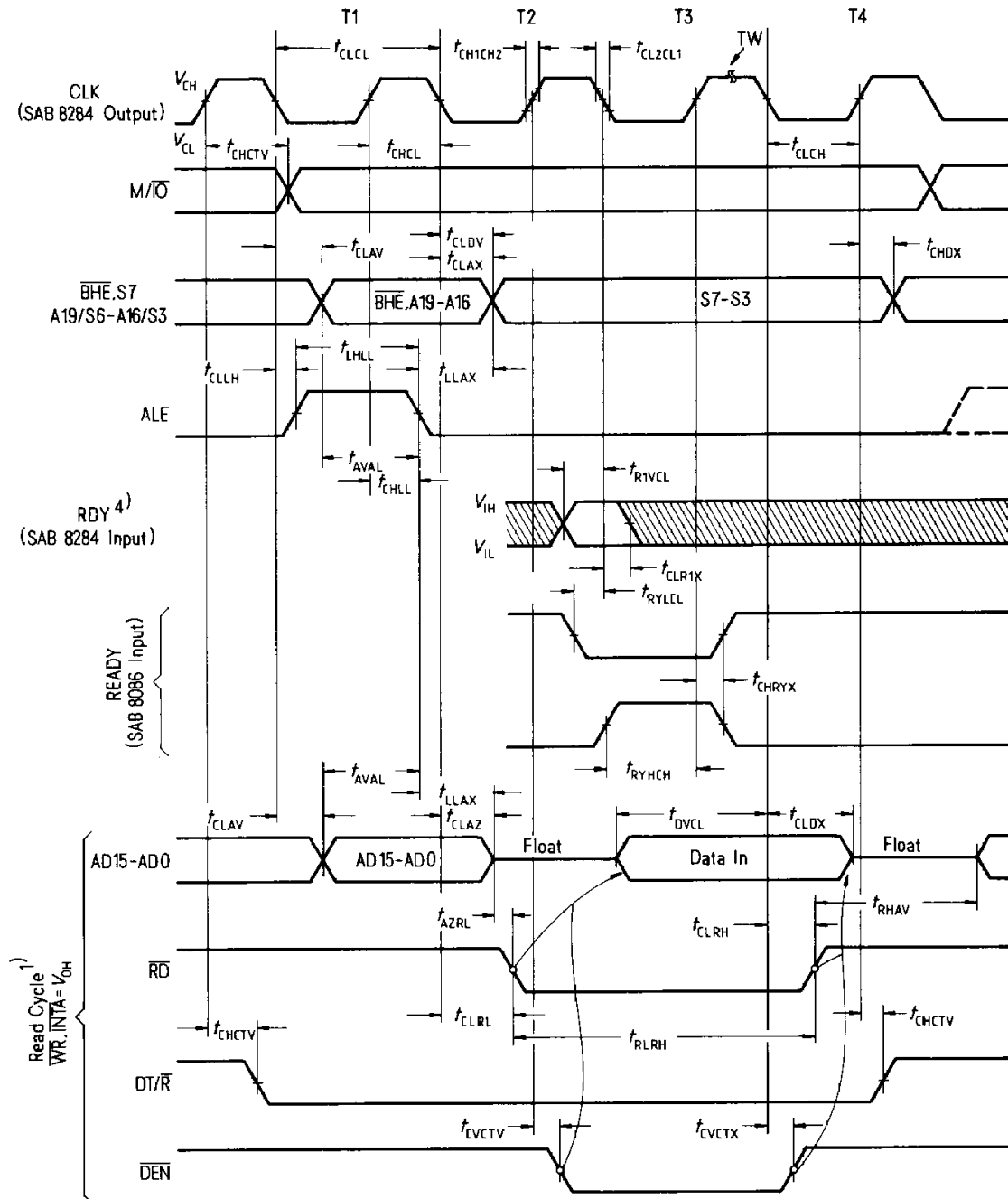
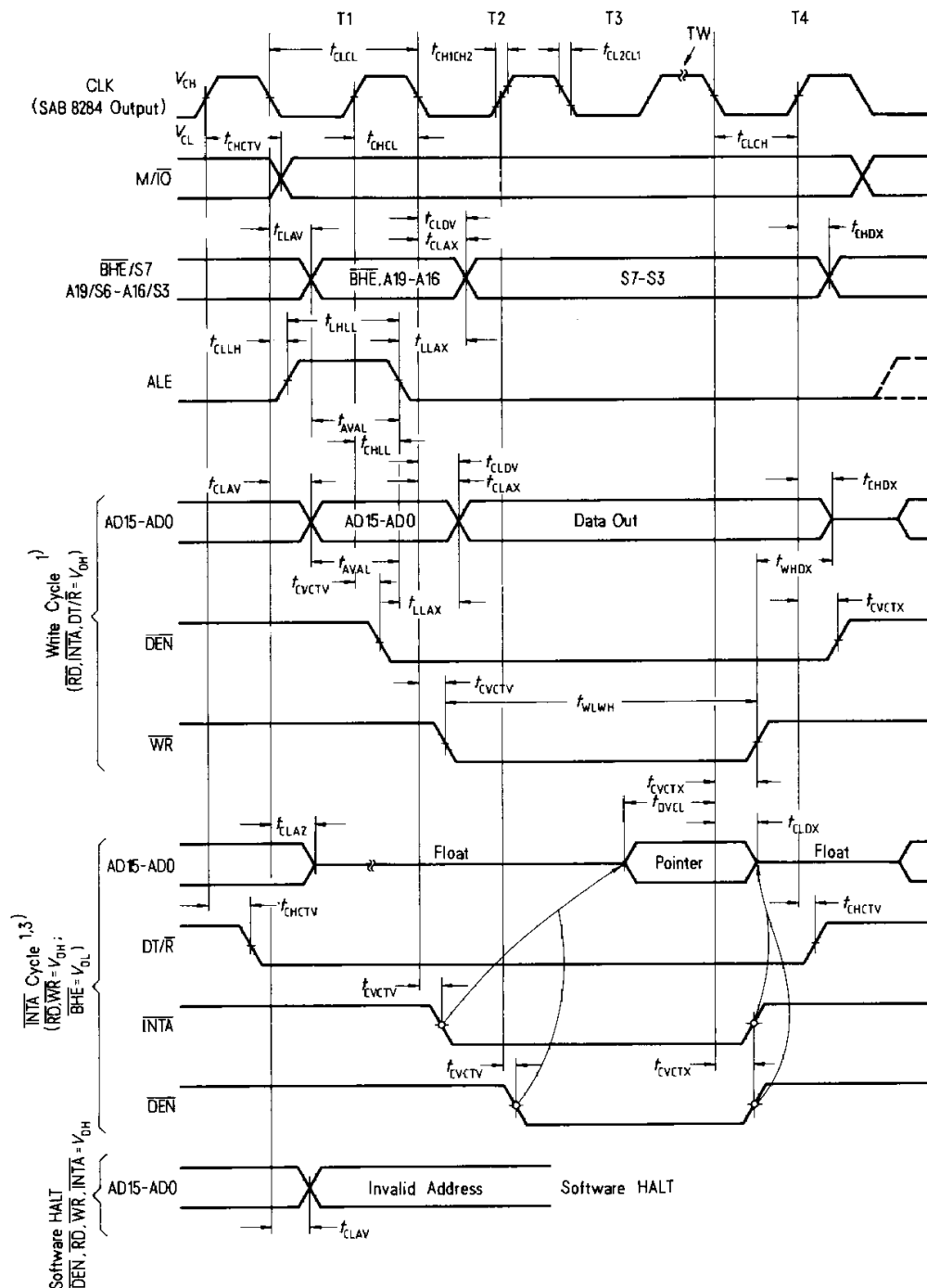


Figure 9 SAB 8086 Bus Timing – Minimum Mode System (cont'd)



¹⁾ All signals switch between V_{OH} and V_{OL} unless otherwise specified.

²⁾ RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.

³⁾ Two INTA cycles run back to back. The SAB 8086 local ADDR/DATA bus is floating during both INTA cycles. Control signals shown for second INTA cycle.

⁴⁾ Signals at SAB 8284B are shown for reference only.

⁵⁾ All timing measurements are made at 1.5 V unless otherwise noted.

Figure 10 SAB 8086 Bus Timing – Maximum Mode System (using SAB 8288A)

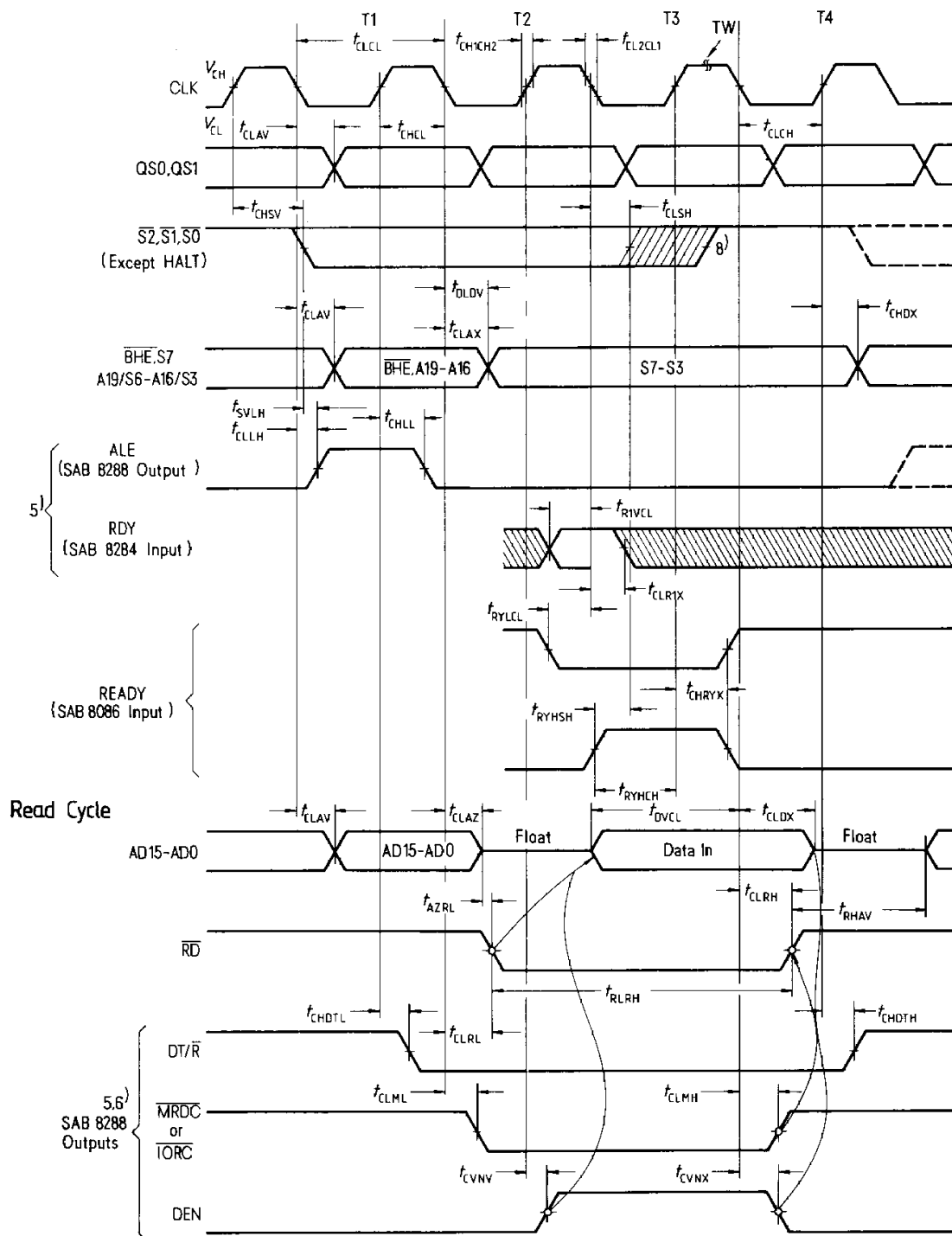
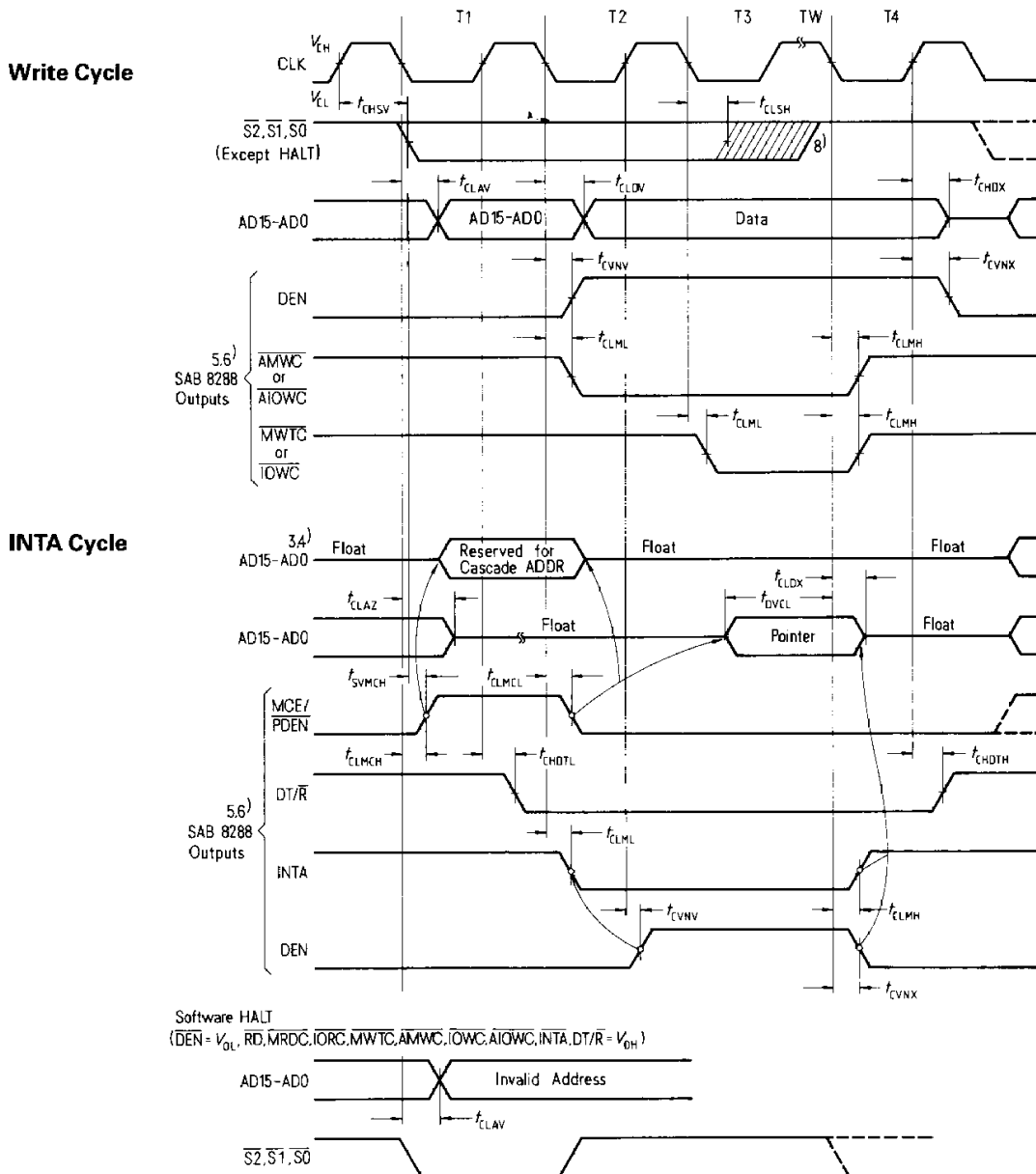


Figure 11 SAB 8086 Bus Timing – Maximum Mode System (using SAB 8288A) (cont'd)



¹⁾ All signals switch between V_{OH} and V_{OL} unless otherwise specified.

²⁾ RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.

³⁾ Cascade address is valid between first and second INTA cycle.

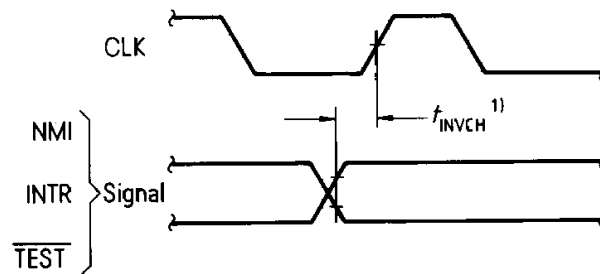
⁴⁾ Two INTA cycles run back-to-back. The SAB 8086 local ADDR/DATA bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.

⁵⁾ Signals at SAB 8284B or SAB 8288A are shown for reference only.

⁶⁾ The issuance of the SAB 8288A command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high SAB 8288A DEN.

⁷⁾ All timing measurements are made at 1.5 V unless otherwise noted.

⁸⁾ Status inactive in state just prior to T4.

Figure 12 Asynchronous Signal Recognition

¹⁾ Setup requirements for asynchronous signals only to guarantee recognition at next CLK

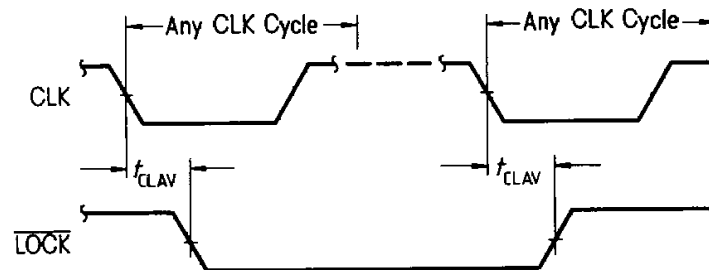
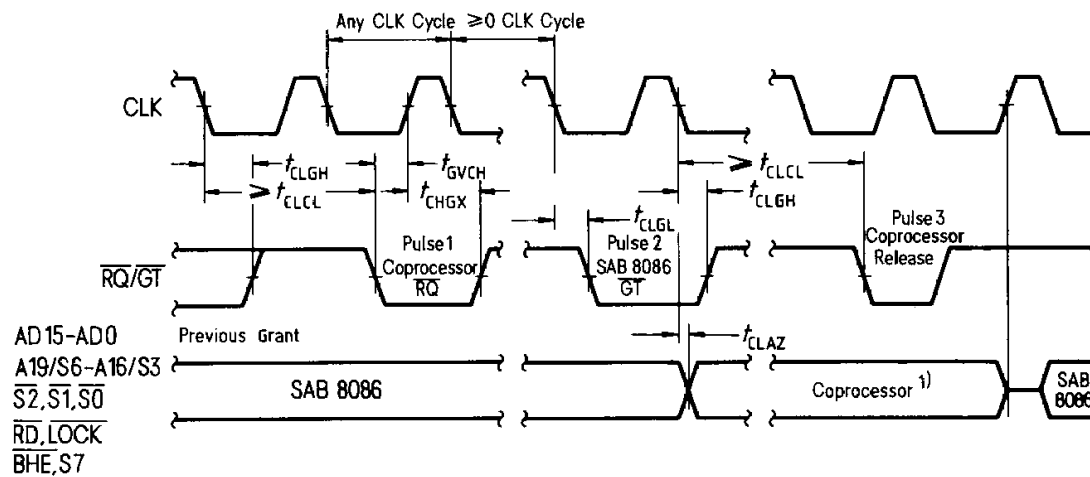
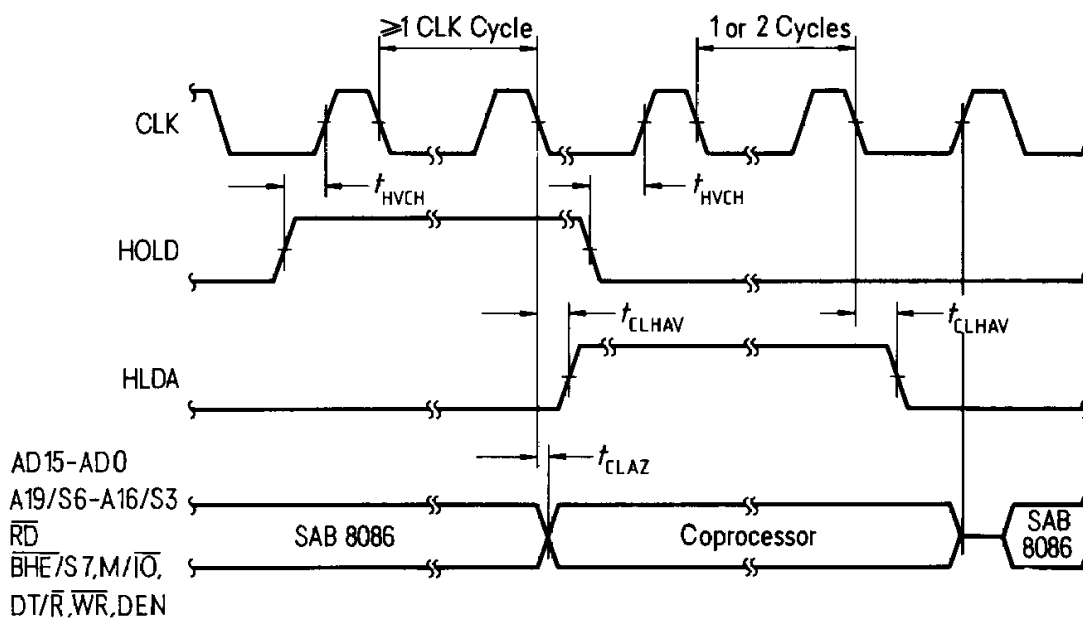
Figure 13 Bus Lock Signal Timing (Maximum Mode only)

Figure 14 Request/Grant Sequence Timing (Maximum Mode only)



1) The coprocessor may not drive the buses outside the region shown without risking contention

Figure 15 Hold/Hold Acknowledge Timing (Minimum Mode only)



SAB 8086

Ordering Information

Type	Ordering code	Description
SAB 8086-P	Q67120-C116	16-bit microprocessor – 5 MHz (plastic)
SAB 8086-2-P	Q67120-C142	16-bit microprocessor – 8 MHz (plastic)
SAB 8086-1-P	Q67120-C141	16-bit microprocessor – 10 MHz (plastic)

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