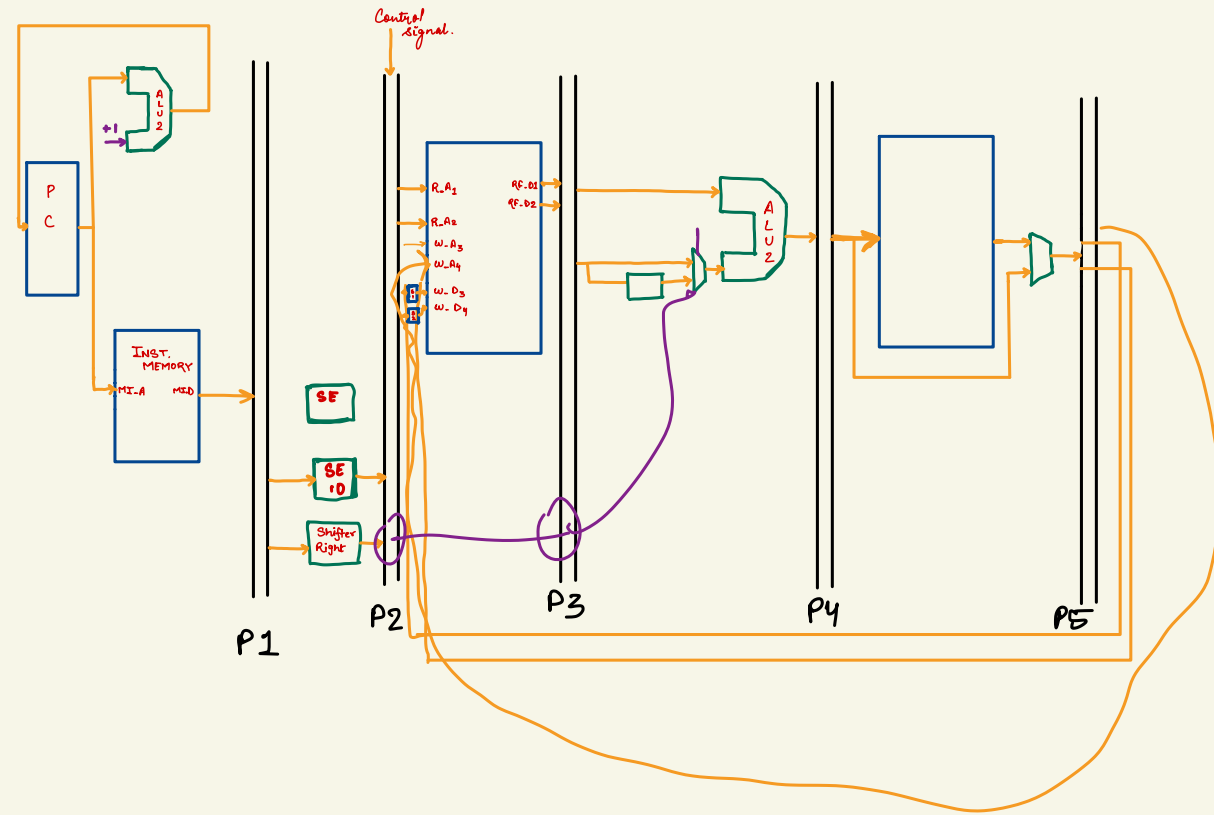
EE-309

PROJECT


Control signal.
ALU 2
+1
P C
INST. MEMORY
MI-A
MID
SE
SE rD
Shifter Right
R_A1
R_A2
W_A3
W_A4
W_D3
W_D4
RF.D1
RF.D2
ALU
P1
P2
P3
P4
P5

Load ✓

Branch ✓

ADA:

PC → MI_A
PC → W.D4
MI_D → P1_A
PC → ALU2_A
+1 → ALU2_B
ALU2_C → PC

M_RE
PC_R
PC_W
P1_W

} S1.

P1 → P2

C.S
P2_W

} S2

P2 → R_A1
P2 → R_A2
R_D1 → P3
R_D2 → P3

} S3

P3 → ALU1_A
P3 → ALU2_B
ALU1_C → P4

} S4

P4 → P5

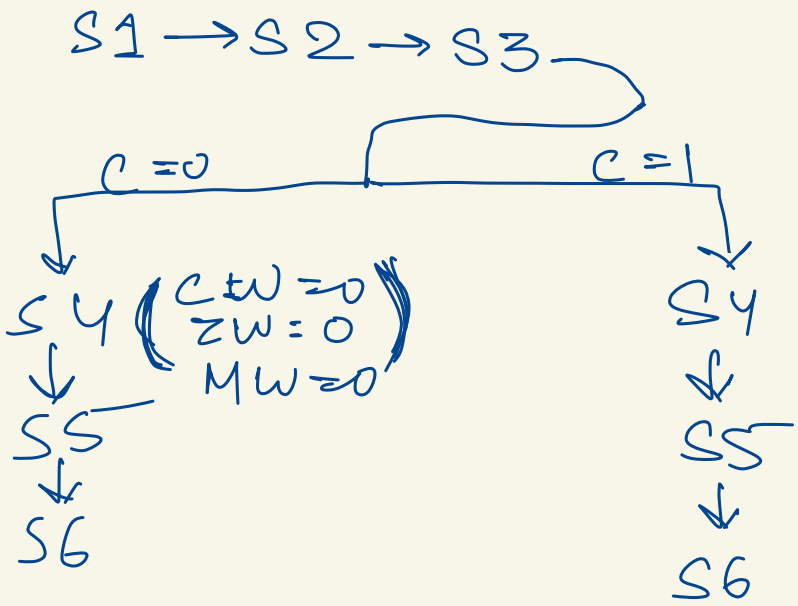
} S5

P5 → RFA3
P5 → RF_D3

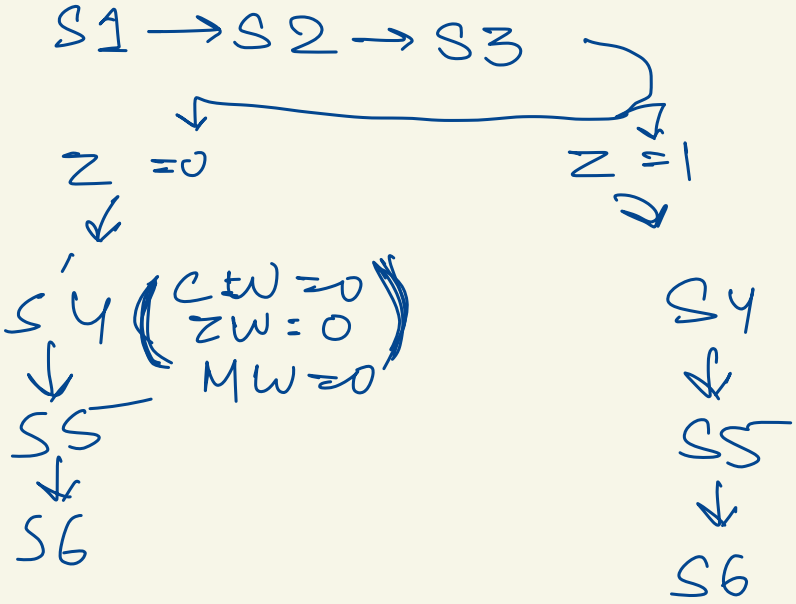
} S6 • RF_EA3

P1_A (16)
P2_A(8)
P2_B(8)
P3_A(16)
P3_B(16)
P4_A(16)
P5_A(16)

ADC:


S1 → S2 → S3
C = 0
C = 1
S4
CW = 0
ZW = 0
MW = 0
S5
S6
S4
S5
S6

ADZ:


S1 → S2 → S3
Z = 0
Z = 1
S4
CW = 0
ZW = 0
MW = 0
S5
S6
S4
S5
S6

PC_R
PC_W
IM_R
P1_W

[STAGE-1]
I.F

P2_W

[STAGE-2]
I.D

P3_W
SE_W
SE_W
RF_R
COMP_W

[STAGE-3]
R.R

ALU_op C_e
ALU_Out Z_e
P4_W T1_W
PE_W

[STAGE-4]
Ex

DM_W
DM_R
P5_W

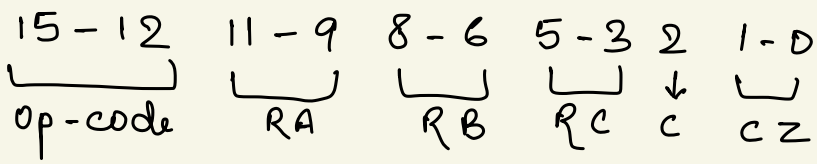
[STAGE-5]
MEM

RF_W1
RF_W2

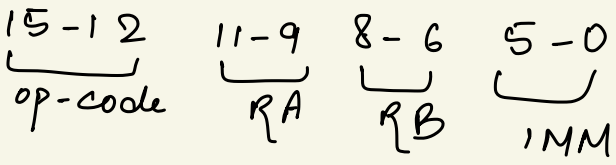
[STAGE-6]
W.B

INSTRUCTION ENCODING

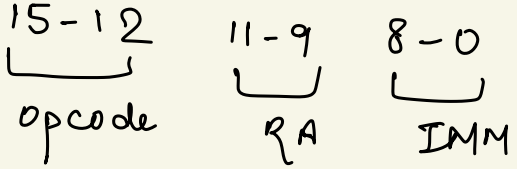
R-type:



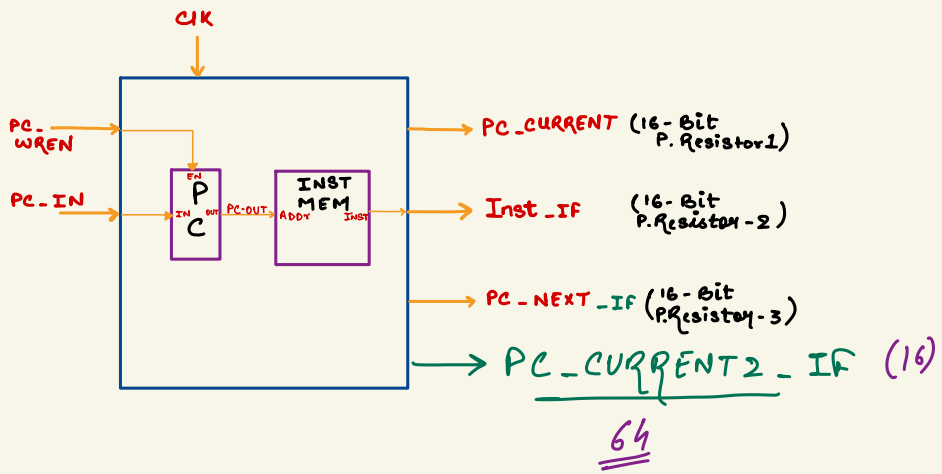
I-type:



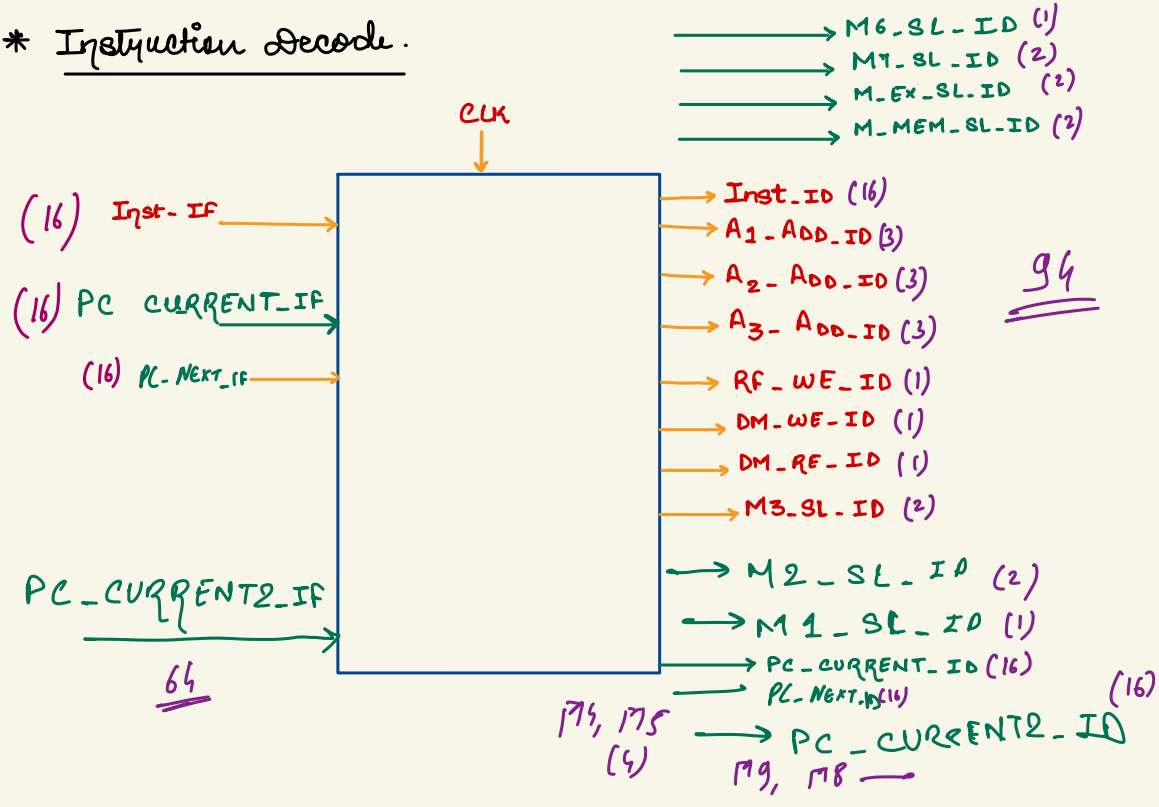
J-type:



* Instruction Fetch



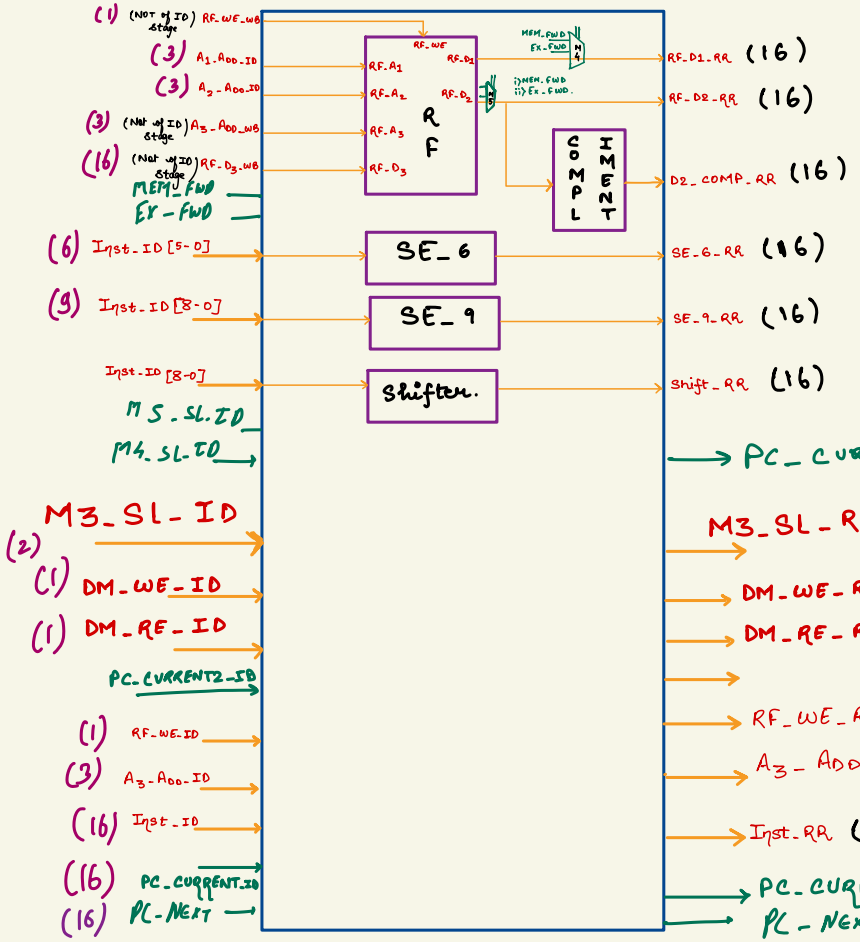
* Instruction Decode.



* Register Read.

* Here, A_3_ADD_WB is of WB stage.
* Here, RF_D_3_WB is of W.B stage.
* Here, RF_WE_WB is of W.B stage.

+16 +16 +16 +1 +3



178 +2

M1_SL_ID →
M2_SL_ID →
M6_SL_ID →
M7_SL_ID →
M_Ex_SL_ID →
M_MEM_SL_ID →
M9, M8 —

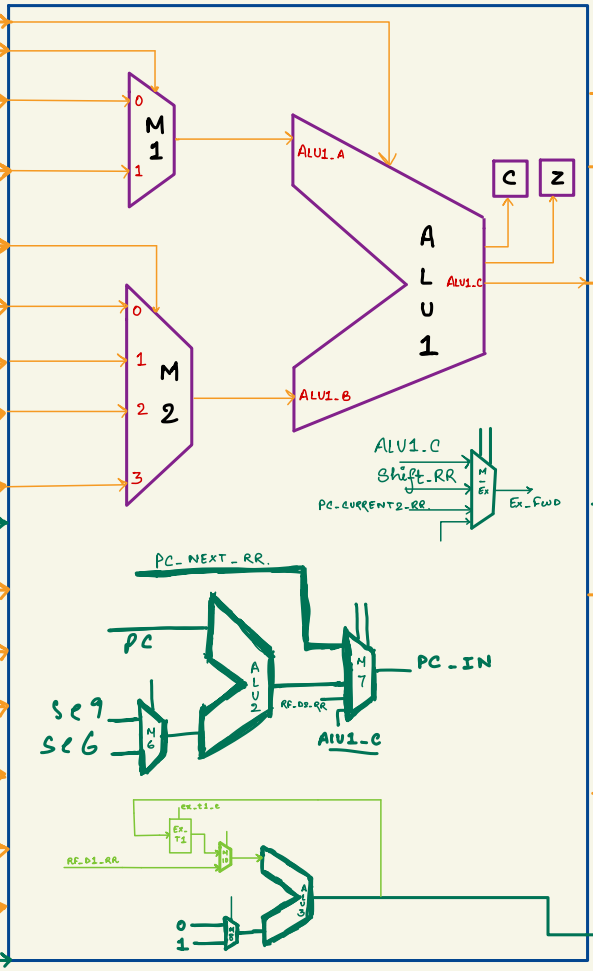
94 + 52
↓
150

→ M1_SL_RR (1)
→ M2_SL_RR (2)
→ M6_SL_RR (1)
→ M7_SL_RR (2)
→ M_Ex_SL_RR (2)
→ M_MEM_SL_RR (2)
M9, M8 → (2)

* Execution stage

* Always use D2 line to store something in DM.

180



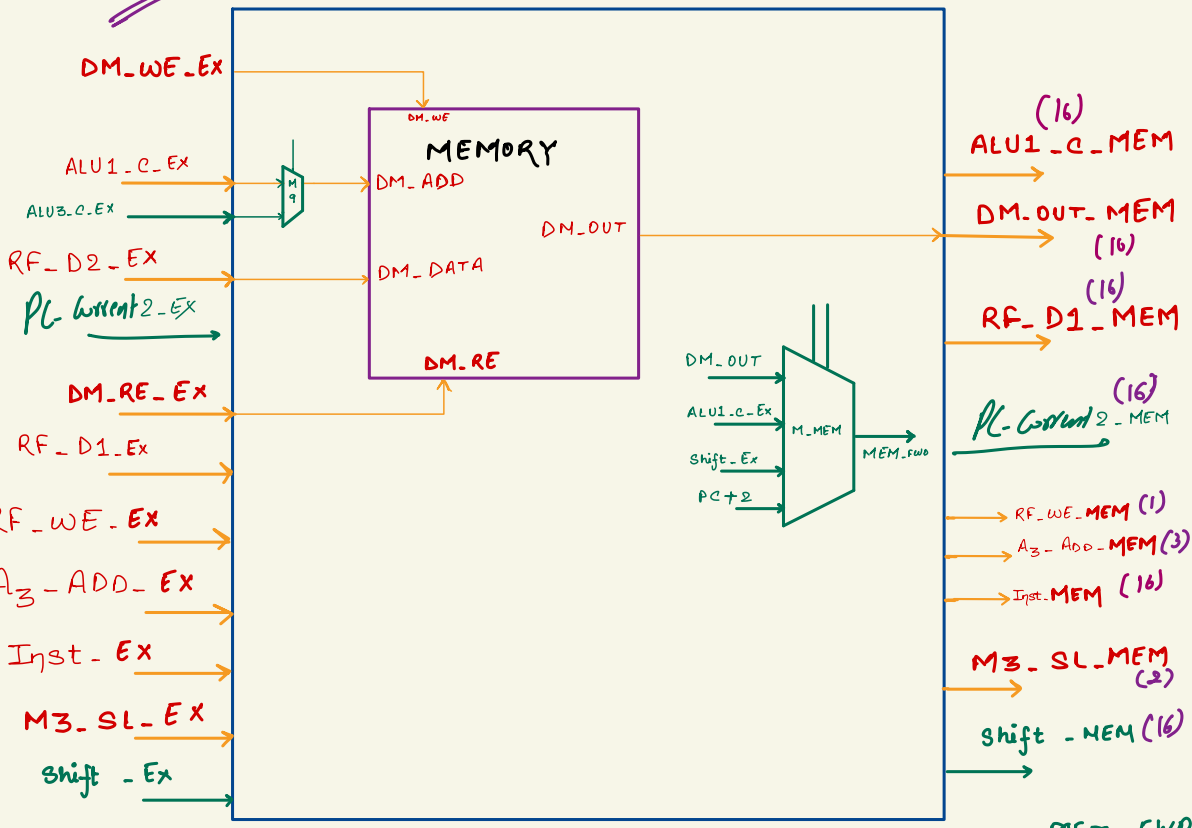
(4) ALU1_OP_RR
(1) M1_SL_RR
(16) RF_D1_RR
(16) RF_D2_RR
(2) M2_SL_RR
RF_D2_RR
(16) SE_6_RR
(16) SE_9_RR
(16) D2_COMP_RR
(16) PC_CURRENT_RR
(2) M3_SL_RR
(1) DM_WE_RR
(1) DM_RE_RR
(1) RF_WE_RR
(3) A3_ADD_RR
(16) Inst_RR
(16) Shift_RR
PC_NEXT
PC_CURRENT2_RR
M9_SL_RR
M6_SL_RR
M7_SL_RR
M_EX_SL_RR
M_MEM_SL_RR
M8_SL_RR

RF_D1_EX (16)
RF_D2_EX (16)
ALU1_C_EX (16)
PC_Current2_EX (16)
Shift_EX (16)
M3_SL_EX (2)
DM_WE_EX (1)
DM_RE_EX (1)
RF_WE_EX (1)
A3_ADD_EX (3)
Inst_EX (16)
ALU3_C_EX (16)
M_MEM_SL_RR (2)
M9_SL_EX (1)

155

* Memory R/W

155



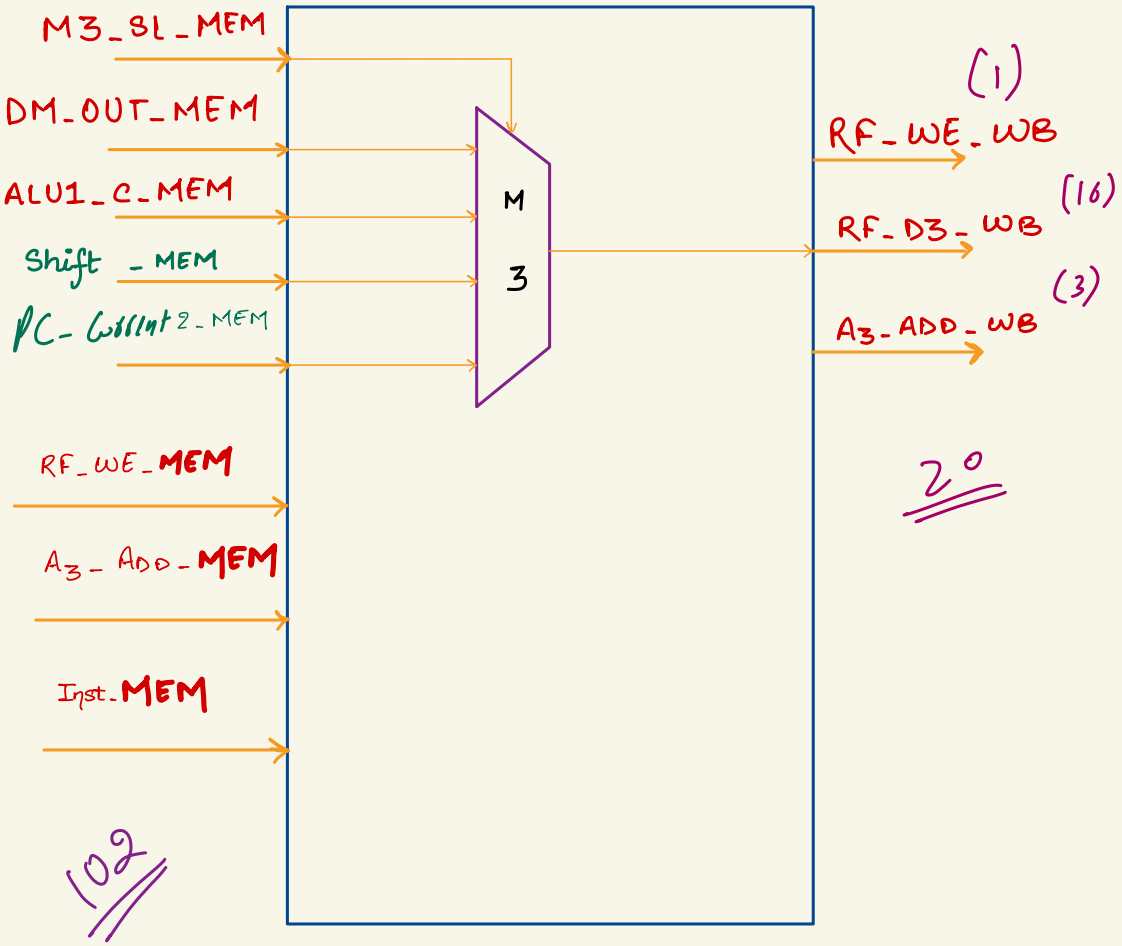
M_MEM_SL_Ex

M3_SL_Ex

* Always use D2 line to store something in DM.

118 + 16

* Write Back.


M3_SL_MEM
DM_OUT_MEM
ALU1_C_MEM
Shift _MEM
PC_Write2_MEM
RF_WE_MEM
A3_ADD_MEM
Inst_MEM
102
M
3
(1)
RF_WE_WB
(16)
RF_D3_WB
(3)
A3_ADD_WB
20

* Dependency of LW-SW Inst.
* LM-SM
* BEQ and Jump instructions.
* MAIN file development
* Instruction-fetch stage.