OPTIREG™ PMIC TLF35585QV

Functional Safety PMIC

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AEC Qualified | RoHS | ISO 26262 compliant

Features

- High efficient power management integrated circuit (PMIC)
- Serial step up and step down pre regulator for wide input voltage range from 3.0 V to 40 V with full performance and low overall power loss
- Low drop post regulator 5.0 V/200 mA for communication supply (QCO)
- Low drop post regulator 5.0 V/600 mA (TLF35585QVS01) or 3.3 V/600 mA (TLF35585QVS02) for µC supply (QUC)
- Voltage reference 5.0 V ±1% for ADC supply, 150 mA current capability (QVR)
- Two trackers for sensor supply following voltage reference 150 mA current capability each (QT1 and QT2)
- Standby regulator 5.0 V/10 mA (TLF35585QVS01) or 3.3 V/10 mA (TLF35585QVS02) (QST)
- Provides enable, sync out signal and voltage monitoring of an optional external post regulator for core supply
- Independent voltage monitoring block and error pin monitoring
- Configurable window watchdog and functional watchdog
- Safe State Control with two safe state signals with programmable delay
- 16-bit SPI, interrupt and reset function
- High junction temperature operation up to 175°C
- PRO-SIL™ Features:
  - ISO 26262 Safety Element out of Context for safety requirements up to ASIL D
  - Safety documentation (Safety Manual & Safety Analysis Summary Report)
- Green Product (RoHS compliant)

Potential applications

- Electric Power Steering
- Battery Management
- Inverter
- Engine Management
- Domain Control

Product validation

Qualified for automotive applications with higher temperature requirements. Product validation according to AEC-Q100.

Description

The OPTIREG™ PMIC TLF35585QV is a highly efficient Functional Safety PMIC (Power management integrated circuit) for safety-relevant applications.

The power supply includes a serial boosted buck pre-regulator supplying 5.0V or 3.3V post regulator rails for microcontroller supply, communication supply and a precise voltage reference. In addition, two 5 V trackers are available to supply off-board sensors.

The OPTIREG™ PMIC TLF35585QV comes with a configurable window (time based trigger) and functional (question & answer based trigger) watchdog, error pin monitoring and voltage monitoring functions as major supervision functions. For microcontroller interaction a 16-bit SPI, interrupt and reset function are provided.

The device has been developed according to ISO26262 targeting systems up to ASIL-D and supports an extended junction temperature range of up to 175°C.

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Type	Package	Marking (Line1 / Line2)
TLF35585QVS01	PG-VQFN-48	35585 / S01 B21
TLF35585QVS02	PG-VQFN-48	35585 / S02 B21

Table of contents

Features . . . 1
Potential applications . . . 1
Product validation . . . 2
Description . . . 2
Table of contents . . . 3
1 Block diagram . . . 8
2 Pin configuration . . . 9
2.1 Pin assignment PG-VQFN-48 . . . 9
2.2 Pin definitions and functions PG-VQFN-48 . . . 9
3 General product characteristics . . . 14
3.1 Absolute maximum ratings . . . 14
3.2 Functional range . . . 17
3.3 Thermal resistance . . . 18
3.4 Current consumption . . . 19
3.4.1 Typical performance characteristics current consumption . . . 21
4 Wake and Enable function . . . 22
4.1 Introduction Wake and Enable function . . . 22
4.2 Electrical characteristics Enable signal . . . 23
4.3 Electrical characteristics Wake signal . . . 24
4.4 Typical performance characteristics Wake and Enable signals . . . 25
5 Pre regulators . . . 26
5.1 Introduction pre regulators . . . 26
5.2 Step up pre regulator . . . 27
5.2.1 Functional description step up pre regulator . . . 27
5.2.2 Electrical characteristics step up pre regulator . . . 28
5.3 Step down pre regulator . . . 30
5.3.1 Functional description step down pre regulator . . . 30
5.3.2 Electrical characteristics step down pre regulator . . . 31
5.3.3 Typical performance characteristics step down pre regulator . . . 35
5.4 Frequency setting . . . 36
5.4.1 Introduction frequency setting . . . 36
5.4.2 Electrical characteristics frequency setting . . . 36
5.4.3 Typical performance characteristics frequency setting . . . 37
6 Post regulators . . . 38
6.1 Introduction post regulators . . . 38
6.2 Microcontroller main supply QUC . . . 40

6.2.1 Functional description microcontroller main supply . . . 40
6.2.2 Electrical characteristics microcontroller main supply . . . 41
6.2.3 Typical performance characteristics microcontroller main supply . . . 43
6.3 Communication supply QCO . . . 44
6.3.1 Functional description communication supply . . . 44
6.3.2 Electrical characteristics communication supply . . . 45
6.3.3 Typical performance characteristics communication supply . . . 46
6.4 Voltage reference supply QVR . . . 47
6.4.1 Functional description voltage reference supply . . . 47
6.4.2 Electrical characteristics voltage reference supply . . . 48
6.4.3 Typical performance characteristics voltage reference supply . . . 49
6.5 Tracker 1 QT1 and tracker 2 QT2 . . . 50
6.5.1 Functional description tracker 1 and tracker 2 . . . 50
6.5.2 Electrical characteristics tracker 1 and tracker 2 . . . 51
6.5.3 Typical performance characteristics tracker 1 and tracker 2 . . . 53
6.6 External post regulator for core supply (optional) . . . 54
6.7 Power sequencing . . . 57
6.7.1 Power sequencing from POWERDOWN to INIT-state . . . 58
6.7.2 Power sequencing STANDBY to INIT-state . . . 60
6.7.3 Power sequencing SLEEP to WAKE-state . . . 61

7 Monitoring function . . . 63
7.1 Introduction monitoring function . . . 63
7.2 Shutdown function . . . 64
7.3 Reset function . . . 64
7.4 Interrupt function . . . 68
7.5 Electrical characteristics voltage monitoring and reset function . . . 70

8 Standby supply and internal supplies . . . 75
8.1 Standby supply QST . . . 75
8.1.1 Functional description standby supply . . . 75
8.1.2 Electrical characteristics standby supply . . . 76
8.1.3 Typical performance characteristics standby supply . . . 78
8.2 Internal supplies . . . 79

9 Wake-up timer . . . 80
9.1 Description of wake-up timer . . . 80
9.2 Electrical characteristics wake-up timer . . . 81

10 State machine . . . 82
10.1 Introduction state machine . . . 82
10.2 Description of states . . . 84
10.2.1 POWERDOWN-state . . . 84
10.2.2 INIT-state . . . 85
10.2.3 NORMAL-state . . . 87

10.2.4 STANDBY-state . . . 88
10.2.5 SLEEP-state . . . 89
10.2.6 WAKE-state . . . 91
10.2.7 FAILSAFE-state . . . 93
10.3 Transition between states . . . 94
10.3.1 POWERDOWN → INIT-state . . . 94
10.3.2 INIT → NORMAL-state . . . 95
10.3.3 Movements between NORMAL and SLEEP-state . . . 97
10.3.3.1 NORMAL → SLEEP-state . . . 97
10.3.3.2 SLEEP → WAKE-state . . . 100
10.3.3.3 WAKE → SLEEP-state . . . 103
10.3.4 Movements between NORMAL and STANDBY-state . . . 106
10.3.4.1 NORMAL → STANDBY-state . . . 106
10.3.4.2 STANDBY → INIT-state . . . 109
10.3.4.3 INIT → NORMAL-state . . . 110
10.3.5 NORMAL → WAKE-state . . . 111
10.3.6 WAKE → NORMAL-state . . . 111
10.3.7 INIT/WAKE → STANDBY-state . . . 113
10.3.8 FAILSAFE → INIT-state . . . 116
10.4 Reaction on detected faults . . . 118
10.4.1 Stay in current state (Interrupt event) . . . 118
10.4.2 Transition to INIT-state . . . 120
10.4.2.1 INIT → INIT-state due to detected fault . . . 121
10.4.2.1.1 INIT → INIT-state due to INIT timer expired for the first time . . . 121
10.4.2.1.2 INIT → INIT-state due to INIT timer expired for the second time . . . 122
10.4.2.2 NORMAL → INIT-state due to detected fault . . . 123
10.4.2.3 STANDBY → INIT-state due to detected fault . . . 124
10.4.2.4 SLEEP → INIT-state due to detected fault . . . 125
10.4.2.5 WAKE → INIT-state due to detected fault . . . 126
10.4.3 Transition to FAILSAFE-state . . . 127
10.4.3.1 INIT → FAILSAFE-state due to detected fault . . . 128
10.4.3.2 XXXX → INIT → FAILSAFE-state due to detected fault . . . 129
10.4.3.3 NORMAL → FAILSAFE-state due to detected fault . . . 130
10.4.3.4 STANDBY → FAILSAFE-state due to detected fault . . . 131
10.4.3.5 SLEEP → FAILSAFE-state due to detected fault . . . 132
10.4.3.6 WAKE → FAILSAFE-state due to detected fault . . . 133
10.4.3.7 Transition to FAILSAFE-state due to thermal shutdown . . . 134
10.4.4 Transition to POWERDOWN . . . 135
10.5 Electrical characteristics state machine . . . 136
10.6 Built In Self Test (BIST) features . . . 137
10.6.1 Analog Built In Self Test (ABIST) . . . 137
10.6.1.1 How to run the ABIST . . . 138

10.6.1.2 Testing the comparator logic only . . . 140
10.6.1.3 Testing the comparator logic and the corresponding deglitching logic . . . 141
10.6.1.4 Testing the complete monitoring chain (comparators, deglitching and output) . . . 143
10.6.1.4.1 Testing the activation of the secondary safety shutdown path . . . 143
10.6.1.4.2 Testing the generation of an interrupt event . . . 144
10.6.1.5 Abort conditions for ABIST operation . . . 144
10.6.2 Logic supervision self test . . . 145
10.7 Microcontroller programming support . . . 146

11 Safe State Control function . . . 147
11.1 Introduction Safe State Control function . . . 147
11.2 Electrical characteristics Safe State Control . . . 150
11.3 Reaction on microcontroller Safety Management Unit (SMU - pin ERR): . . . 153
11.3.1 Immediate reaction on ERR monitoring failure . . . 153
11.3.2 Recovery delay reaction on ERR monitoring failure . . . 155
11.4 Reaction on error-triggered state transitions . . . 159
11.5 Reaction on Window Watchdog Output (WWO) . . . 160
11.6 Reaction on Functional Watchdog Output (FWO) . . . 161
11.7 Reaction on Thermal Shutdown (TSD) . . . 162

12 SPI (Serial Peripheral Interface) . . . 164
12.1 Introduction SPI . . . 164
12.2 SPI write access to protected registers . . . 168
12.3 SPI write initiated state transition request and regulator configuration . . . 169
12.4 Registers description . . . 170
12.4.1 Device registers . . . 172
12.5 Electrical characteristics SPI signals . . . 242

13 Interrupt generation . . . 244

14 Watchdog supervision . . . 247
14.1 Introduction window watchdog and functional watchdog . . . 247
14.2 Window watchdog . . . 248
14.2.1 Timing diagrams window watchdog . . . 251
14.2.1.1 Normal operation: correct triggering . . . 251
14.2.1.2 Fault operation: no trigger in open window after initialization . . . 252
14.2.1.3 Fault operation: no trigger in open window in steady state . . . 253
14.2.1.4 Fault operation: false trigger in closed window after initialization . . . 254
14.2.1.5 Fault operation: false trigger in closed window in steady state . . . 255
14.2.2 Electrical characteristics window watchdog . . . 256
14.3 Functional watchdog . . . 257
14.3.1 Timing diagrams functional watchdog . . . 260
14.3.1.1 Normal operation: correct triggering . . . 260
14.3.1.2 Fault operation: missing synchronization . . . 261
14.3.1.3 Fault operation: wrong answer . . . 262

14.3.1.4 Fault operation: missing response 263
15 Application information 264
16 Package information 266
Revision history 267
Disclaimer 269

1 Block diagram

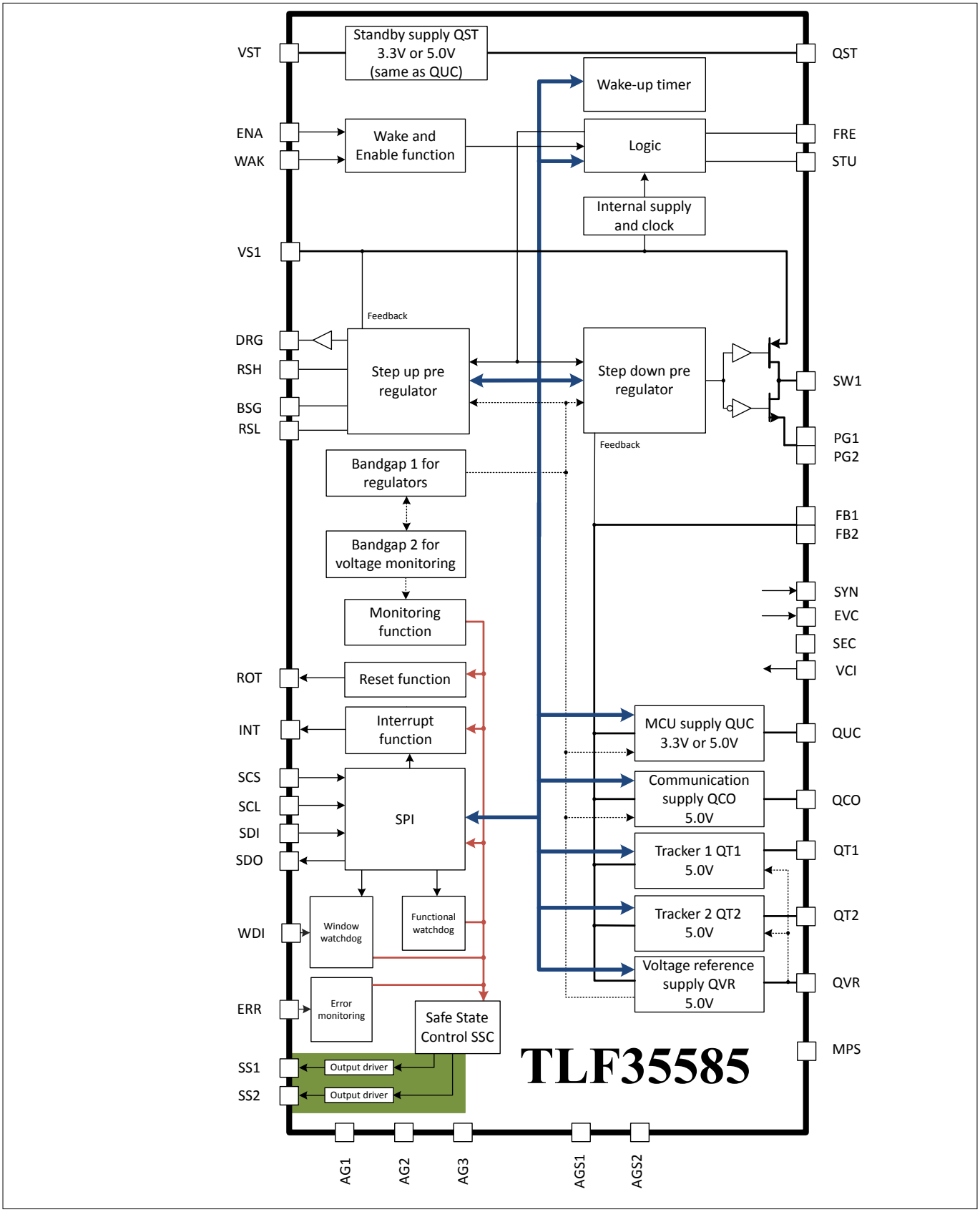


Figure 1 **Block diagram**

2 Pin configuration

2.1 Pin assignment PG-VQFN-48

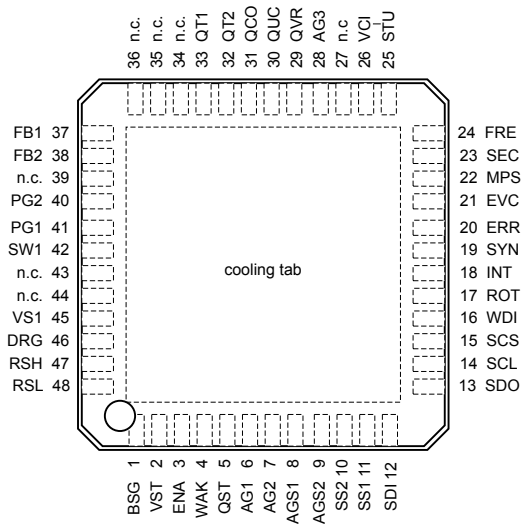


Figure 2 **Pin configuration PG-VQFN-48**

2.2 Pin definitions and functions PG-VQFN-48

Pin	Symbol	Function
1	BSG	Boost driver ground: Connect this pin to ground at the low side of an external current sense resistor to decouple the driver noise from the sensitive ground. If step up pre regulator option is not used, connect to ground.
2	VST	Standby supply input: Connect this input directly to pin VS1. It is recommended to place a local capacitor between pin and ground.
3	ENA	Enable input: A rising edge signal at this pin generates a wake-up event for the device. In case of not used connect to ground.
4	WAK	Wake input: A "high" signal at this pin generates a wake-up event for the device. In case of not used, connect to ground.
5	QST	Standby supply output: Connect a capacitor as close as possible to pin.
6	AG1	Analog ground, pin 1: Connect this pin directly (low ohmic and low inductive) to ground.
7	AG2	Analog ground, pin 2: Connect this pin directly (low ohmic and low inductive) to ground.

Pin	Symbol	Function
8	AGS1	Analog ground safety, pin 1: Connect this pin directly (low ohmic and low inductive) to ground. In case a safety switch is used, connect directly to the source of the NMOS used.
9	AGS2	Analog ground safety, pin 2: Connect this pin directly (low ohmic and low inductive) to ground. In case a safety switch is used, connect directly to the source of the NMOS used.
10	SS2	Safe state signal 2: Safe state output signal 2, sets the application into a safe state. Signal is delayed against SS1, delay can be adjusted via SPI command. In case of not used, leave open.
11	SS1	Safe state signal 1: Safe state output signal 1, sets the application into a safe state.
12	SDI	Serial peripheral interface, signal data input (MOSI): SPI signaling port, connect to SPI port "data output"(MOSI) of microcontroller to receive commands during SPI communication.
13	SDO	Serial peripheral interface, signal data output (MISO): SPI signaling port, connect to SPI port "data input" of microcontroller to send status information during SPI communication.
14	SCL	Serial peripheral interface, signal clock input (SCLK): SPI signaling port, connect to SPI port "clock" (SCLK) of microcontroller to clock the device for SPI communication.
15	SCS	Serial peripheral interface, signal chip select input: SPI signaling port, connect to SPI port "chip select" of microcontroller to address the device for SPI communication.
16	WDI	Watchdog pin-trigger input: Input for trigger signal, connect the "trigger signal output" of the microcontroller to this pin. In case of not used, leave open (internal pull-down).
17	ROT	Reset signal output: Open drain structure with internal pull-up current source. A low signal at this pin indicates a reset event.
18	INT	Interrupt signal output: Push-pull-stage. A "low" pulse at this pin indicates an interrupt, the microcontroller shall read out the SPI status registers. Connect to a non maskable interrupt port (NMI) of the microcontroller core supply voltage.
19	SYN	Synchronization signal output: Connect this output to the optional external switch mode post regulator synchronization input. The signal delivers the step down regulator switching frequency either in phase or shifted by 180° (selectable via SPI command). The switch mode post regulator shall synchronize to the rising edge. If not used, then leave open.

Pin	Symbol	Function
20	ERR	Error signal input: Input for error signal from microcontroller safety managing unit (SMU, internal failure detection of the microcontroller). Connect the "error signal output" (FSP) of the microcontroller to this pin. If the function is not used, then connect this pin to ground.
21	EVC	Enable signal output for external post regulator for core supply: Connect this pin to the enable input of the external post regulator. If not used, then leave open.
22	MPS	Microcontroller programming support input: Input to enable microcontroller programming support (MPS). For details please refer to Chapter 10.7. If the function is not used, then connect this pin to ground.
23	SEC	Hardware configuration pin for external post regulator for core supply: If the option external post regulator is used, then leave open. If the option external post regulator is not used, then connect this pin to ground.
24	FRE	Hardware configuration pin for step down pre regulator base frequency: Connect this pin to ground for low frequency range or leave open for high frequency range.
25	STU	Hardware configuration pin for step up converter: If the option step up pre regulator is not used, then connect this pin to ground. If the option step up pre regulator is used, then leave open.
26	VCI	Input for optional external post regulator output voltage monitoring (core supply): Connect an external resistor divider to adjust the overvoltage and undervoltage thresholds of the reset output signal ROT. If the option external post regulator is not used, then leave open.
27	N.C.	Internally not connected: This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
28	AG3	Analog ground, pin 3: Connect this pin directly (low ohmic and low inductive) to ground.
29	QVR	Voltage reference supply output: Connect a capacitor as close as possible to pin.
30	QUC	MCU supply output (microcontroller main supply): Connect a capacitor as close as possible to pin.
31	QCO	Communication supply output: Connect a capacitor as close as possible to pin.
32	QT2	Tracker 2 output: Connect a capacitor as close as possible to pin.

Pin	Symbol	Function
33	QT1	Tracker 1 output: Connect a capacitor as close as possible to pin.
34	N.C.	Internally not connected: This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
35	N.C.	Internally not connected: This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
36	N.C.	Internally not connected: This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
37	FB1	Step down pre regulator feedback input and input for linear post regulators and trackers, pin 1: Connect the capacitor of the step down pre regulator output filter with low ohmic and low inductive connection straight to this pin. Always connect in parallel with pin FB2.
38	FB2	Step down pre regulator feedback input and input for linear post regulators and trackers, pin 2: Connect the capacitor of the step down pre regulator output filter with low ohmic and low inductive connection straight to this pin. Always connect in parallel with pin FB1.
39	N.C.	Internally not connected: This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
40	PG2	Step down pre regulator power ground, pin 2: Connect this pin straight (low ohmic and low inductive) to ground and pre regulator output capacitor minus. Always connect in parallel with pin PG1.
41	PG1	Step down pre regulator power ground, pin 1: Connect this pin straight (low ohmic and low inductive) to ground and pre regulator output capacitor minus. Always connect in parallel with pin PG2.
42	SW1	Step down pre regulator power stage output: Connect this pin straight (low ohmic and low inductive) to the pre regulator output filter.
43	N.C.	Internally not connected: This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
44	N.C.	Internally not connected:

Pin	Symbol	Function
		This pin is electrically not connected internally and can be kept open/floating, connected to GND or any other signal. Consider neighboring signals for potential failures.
45	VS1	Supply voltage step down pre regulator input: Connect this input to the output of the step up pre regulator. If step up pre regulator option is not used, connect to supply (battery) voltage with reverse protection diode and capacitor between pin and ground. An EMC filter is recommended.
46	DRG	Driver output for external step up regulator power stage: Gate of low side switch of step up pre regulator: Connect to the gate of an external N-channel MOSFET, line to be straight and as short as possible. If step up pre regulator option is not used, then leave open.
47	RSH	Sense resistor input for external step up regulator power stage, high side: Connect this pin to the high side of an external current sense resistor to determine the maximum current threshold through the external N-channel MOSFET. If step up pre regulator option is not used, then connect to ground.
48	RSL	Sense resistor input for external step up regulator power stage, low side: Connect this pin to the low side of an external current sense resistor to determine the maximum current threshold through the external N-channel MOSFET. If step up pre regulator option is not used, then connect to ground.
Cooling tab	GND	Cooling tab. Connect externally to GND and heat sink area.

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings[4)]

T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Voltages							
Boost driver ground	V_{BSG}	-0.3	–	0.3	V	–	P_4.1.1
Input standby supply	V_{VST}	-0.3	–	40	V	5)6)	P_4.1.2
Input voltage pin 1 (pre regulator)	V_{VS1}	-0.3	–	40	V	5)6)	P_4.1.3
External step up power stage, gate	V_{DRG}	-0.3	–	40	V	5)	P_4.1.4
External power stage, sense resistor high	V_{RSH}	-0.3	–	40	V	5)	P_4.1.5
External power stage, sense resistor low	V_{RSL}	-0.3	–	2.5	V	–	P_4.1.6
Enable input	V_{ENA}	-0.3	–	40	V	5)	P_4.1.7
Enable input	I_{ENA}	-5	–	–	mA	7)	P_4.1.8
Wake input	V_{WAK}	-0.3	–	40	V	5)	P_4.1.9
Wake input	I_{WAK}	-5	–	–	mA	7)	P_4.1.10
Reset output	V_{ROT}	-0.3	–	40.0	V	–	P_4.1.11
SPI chip select input	V_{SCS}	-0.3	–	40.0	V	–	P_4.1.12
SPI clock input	V_{SCL}	-0.3	–	40.0	V	–	P_4.1.13
SPI data in (MOSI) input	V_{SDI}	-0.3	–	40.0	V	–	P_4.1.14
SPI data out (MISO output)	V_{SDO}	-0.3	–	40.0	V	–	P_4.1.15
Interrupt output	V_{INT}	-0.3	–	40.0	V	–	P_4.1.16
Window watchdog trigger input	V_{WDI}	-0.3	–	40.0	V	–	P_4.1.17
Error pin input	V_{ERR}	-0.3	–	40.0	V	–	P_4.1.18

(table continues...)

4 Not subject to production test, specified by design.
5 Maximum rating is 60 V, if rising slewrate of voltage at the pin is lower than 6 V/ms , for an overall time of 1 hour during the lifetime of the product
6 Maximum rating is 43.5 V, for an overall time of 10 s (in the range of 40 V to 43.5 V) during the lifetime of the product independent from the rise time.
7 Consider external series resistor for negative voltages < -0.3 V to ensure maximum rating of current

Table 1 (continued) Absolute maximum ratings[4)]

T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Safe state 1 output	V_{SS1}	-0.3	–	40.0	V	–	P_4.1.19
Safe state 2 output	V_{SS2}	-0.3	–	40.0	V	–	P_4.1.20
Output voltage reference supply	V_{QVR}	-0.3	–	6.0	V	–	P_4.1.21
Output tracker 2	V_{QT2}	-1.0	–	40	V	–	P_4.1.22
Output tracker 1	V_{QT1}	-1.0	–	40	V	–	P_4.1.23
Output communication supply	V_{QCO}	-0.3	–	6.0	V	–	P_4.1.24
Output microcontroller main supply	V_{QUC}	-0.3	–	6.0	V	–	P_4.1.25
External core voltage monitor input	V_{VCI}	-0.3	–	6.0	V	–	P_4.1.26
HW config: ext. core voltage monitor	V_{SEC}	-0.3	–	6.0	V	–	P_4.1.27
Synchronization output	V_{SYN}	-0.3	–	40.0	V	–	P_4.1.28
Enable output for ext. core supply	V_{EVC}	-0.3	–	40.0	V	–	P_4.1.29
Step down feedback input 2	V_{FB2}	-0.3	–	8.0	V	–	P_4.1.30
Step down feedback input 1	V_{FB1}	-0.3	–	8.0	V	–	P_4.1.31
Step down power ground 2	V_{PG2}	-0.3	–	0.3	V	–	P_4.1.32
Step down power ground 1	V_{PG1}	-0.3	–	0.3	V	–	P_4.1.33
Step down switching node	V_{SW1}	-0.3	–	40	V	[6)]	P_4.1.34
HW config: step up pre regulator	V_{STU}	-0.3	–	6.0	V	–	P_4.1.35
HW config: step down frequency	V_{FRE}	-0.3	–	6.0	V	–	P_4.1.36
Output standby supply	V_{QST}	-0.3	–	6.7	V	–	P_4.1.37
Input MPS	V_{MPS}	-0.3	–	20	V	–	P_4.1.38
Temperatures							
Junction temperature	T_j	-40	–	175	°C	–	P_4.1.39
Storage temperature	T_{stg}	-55	–	175	°C	–	P_4.1.40

(table continues...)

4 Not subject to production test, specified by design.

6 Maximum rating is 43.5 V, for an overall time of 10 s (in the range of 40 V to 43.5 V) during the lifetime of the product independent from the rise time.

Table 1 (continued) Absolute maximum ratings[4]

T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
ESD susceptibility							
ESD susceptibility to GND	V_{ESD}	-2	–	2	kV	HBM [8]	P_4.1.41
ESD susceptibility to GND	V_{ESD}	-500	–	500	V	CDM [9]	P_4.1.42
ESD susceptibility (corner pins) to GND	$V_{ESD,Corner}$	-750	–	750	V	CDM [9]	P_4.1.43

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information visit www.jedec.org.

4 Not subject to production test, specified by design.
8 ESD susceptibility, Human Body Model (HBM) according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).
9 ESD susceptibility, Charged Device Model (CDM) according to ESDA STM5.3.1 or ANSI/ESD S.5.3.1.

3.2 Functional range

Table 2 Functional range

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation at input of the step-up converter	V_{Bat}	3	–	40	V	with step up pre regulator active in front of step down pre regulator [10)]	P_4.2.1
Supply voltage range for normal operation at pin VSx	V_{VS}	6	–	40	V	without step up pre regulator active in front of step down pre regulator	P_4.2.2
Start-up voltage threshold for power sequencing	$V_{PS,start}$	4.9	5.0	5.1	V	V_{VS} increasing	P_4.2.3
Internal start-up time from POWERDOWN	$t_{tr,pwrd}$	–	1	2	ms	from first VS connection to start of power sequence	P_4.2.4
POWERDOWN shutdown threshold	$V_{PD,lo}$	2.7	3.0	3.5	V	V_{VS} decreasing; Except STANDBY-state	P_4.2.5
POWERDOWN shutdown threshold	$V_{PD,lo}$	2.7	3.0	4.5	V	V_{VS} decreasing; STANDBY-state	P_4.2.6
Junction temperature	T_j	-40	–	175	°C	–	P_4.2.7

Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

10 The initial start-up of the device requires a minimum input voltage of $V_{PS,start}$ at the pin VSx for the time $t_{tr,pwrd}$.

3.3 Thermal resistance

Table 3 Thermal resistance[11)]

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	–	12.2	K/W	–	P_4.3.1
Junction to soldering point (pin)	R_{thJSP}	20.1	–	22.1	K/W	JEDEC 2s2p, measured to pin: 1, 6, 7, 28	P_4.3.2
Junction to soldering point (pin)	R_{thJSP}	34.9	–	37.6	K/W	JEDEC 1s0p, measured to pin: 1, 6, 7, 28	P_4.3.3
Junction to soldering point (soldering pad)	R_{thJSP}	11.0	–	14.7	K/W	JEDEC 2s2p	P_4.3.4
Junction to soldering point (soldering pad)	R_{thJSP}	13.1	–	18.0	K/W	JEDEC 1s0p	P_4.3.5
Junction to ambient	R_{thJA}	–	37	–	K/W	[12)]	P_4.3.6

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information visit www.jedec.org.

11 Not subject to production test, specified by design.

12 Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable, a thermal via array next to the package contacted the first inner copper layer.

3.4 Current consumption

Table 4 Current consumption [13)]

V_{VS} = 10 V to 28 V, T_j = -40°C to 85°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
INIT-,NORMAL-,WAKE-state	$I_{q,HF}$	–	–	45	mA	$f_{PREREG,BUCK}$ = 2.2 MHz; [13)] $T_j \le 85°C$; 10 V ≤ V_{VS} ≤ 28 V	P_4.4.1
INIT-,NORMAL-,WAKE-state	$I_{q,LF}$	–	–	30	mA	$f_{PREREG,BUCK}$ = 440 kHz; [13)] $T_j \le 85°C$; 10 V ≤ V_{VS} ≤ 28 V	P_4.4.2
STANDBY-state	I_q	–	7.5	10	µA	QST is disabled; [13)] $T_j \le 40°C$; 10 V ≤ V_{VS} ≤ 14 V; wake-up timer disabled	P_4.4.3
STANDBY-state	I_q	–	7.5	15	µA	QST is disabled; [13)] $T_j \le 85°C$; 10 V ≤ V_{VS} ≤ 28 V; wake-up timer disabled	P_4.4.4
STANDBY-state	I_q	–	–	30	µA	QST is disabled; [13)] $T_j \le 85°C$; 10 V ≤ V_{VS} ≤ 28 V; wake-up timer enabled	P_4.4.5
STANDBY-state	I_q	–	40	56	µA	QST is enabled; [13)] $T_j \le 40°C$; 10 V ≤ V_{VS} ≤ 28 V	P_4.4.6
STANDBY-state	I_q	–	40	70	µA	QST is enabled; [13)] $T_j \le 85°C$; 10 V ≤ V_{VS} ≤ 28 V	P_4.4.7
SLEEP-state	I_q	–	180	250	µA	[13)] $T_j \le 40°C$; 12 V ≤ V_{VS} ≤ 28 V	P_4.4.8
SLEEP-state	I_q	–	180	280	µA	[13)] $T_j \le 85°C$; 12 V ≤ V_{VS} ≤ 28 V	P_4.4.9
SLEEP-state	I_q	–	180	300	µA	[13)] $T_j \le 85°C$; 10 V ≤ V_{VS} ≤ 28 V	P_4.4.10

(table continues...)

13 All quiescent current consumption parameters are measured with zero load and all selectable options (outputs, monitors, watchdog, timers, step-up converter) switched off unless otherwise specified.

Table 4 (continued) Current consumption [13)]

V_{VS} = 10 V to 28 V, T_j = -40°C to 85°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
FAILSAFE-state	I_q	–	90	150	µA	[13)] $T_j \leq 40°C$; 10 V ≤ V_{VS} ≤ 18 V; $t_{FAILSAFE} > t_{FAILSAFE,min}$	P_4.4.11
FAILSAFE-state	I_q	–	90	200	µA	[13)] $T_j \leq 85°C$; 10 V ≤ V_{VS} ≤ 28 V; $t_{FAILSAFE} > t_{FAILSAFE,min}$	P_4.4.12

13 All quiescent current consumption parameters are measured with zero load and all selectable options (outputs, monitors, watchdog, timers, step-up converter) switched off unless otherwise specified.

3.4.1 Typical performance characteristics current consumption

INIT, NORMAL and WAKE current consumption I_q versus supply voltage V_{VS} (FRE-Pin: open)

INIT, NORMAL and WAKE current consumption I_q versus supply voltage V_{VS} (various configuration)

STANDBY current consumption I_q versus supply voltage V_{VS} (QST disabled)

STANDBY current consumption I_q versus supply voltage V_{VS} (QST enabled)

4 Wake and Enable function

4.1 Introduction Wake and Enable function

The TLF35585QV is automatically turned on when connected to a battery (Power-On-Reset POR to move the device out of POWERDOWN) and moves into INIT-state, where the device is available for configuration. After successful configuration and initial service of supervision functions, the device allows for transition to NORMAL-state via SPI command. From NORMAL or WAKE-state, the device can be sent to a low power state (SLEEP or STANDBY) via SPI commands. The WAK and ENA signal are external triggers to leave the low power states (or the FAILSAFE-state).

Wake (pin WAK - level triggered) / Enable (pin ENA - edge triggered)

The WAK and ENA input pins are battery voltage level capable. A signal, with a voltage higher than $V_{WAK,hi}$ applied at pin WAK for $t_{WAK,min}$ represents a valid Wake-Signal. A positive going edge at pin ENA represents a valid Wake-Signal as well. A valid Wake-Signal triggers a wake-up event and transitions the device from STANDBY to INIT-state, from SLEEP to WAKE-state or from FAILSAFE to INIT-state.

A low signal $V_{WAK,lo}$ at pin WAK as well as a negative going edge at pin ENA does not have a direct influence to the state machine and does not initiate a transition between states.

In case a valid Wake-Signal is detected during the transition phase from NORMAL to SLEEP-state, the device initiates a transition to WAKE-state and generate an interrupt.

In case a valid Wake-Signal is detected during the transition phase from NORMAL to STANDBY-state, the device initiates a transition to INIT-state and a Reset (ROT) event is generated.

Before sending a SPI transition command, pin ENA does not have to be brought below $V_{ENA,thrlo}$. Even if pin ENA is high (above $V_{ENA,thrhi}$), the SPI transition command instructs the device to move into SLEEP or STANDBY-state.

The actual interpretation of the signal level at the pins ENA and WAK can be read via SPI from the register **WKSF**.ENAST (signal level at pin ENA) and **WKSF**.WAKST (signal level at pin WAK).

For further details please refer to Chapter 10 State machine.

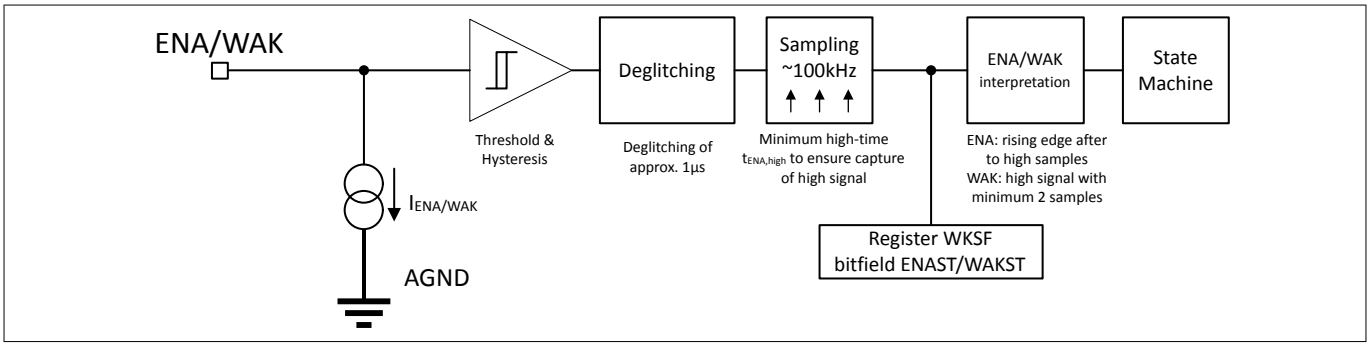


Figure 3 **Principle of the enable and wake function**

4.2 Electrical characteristics Enable signal

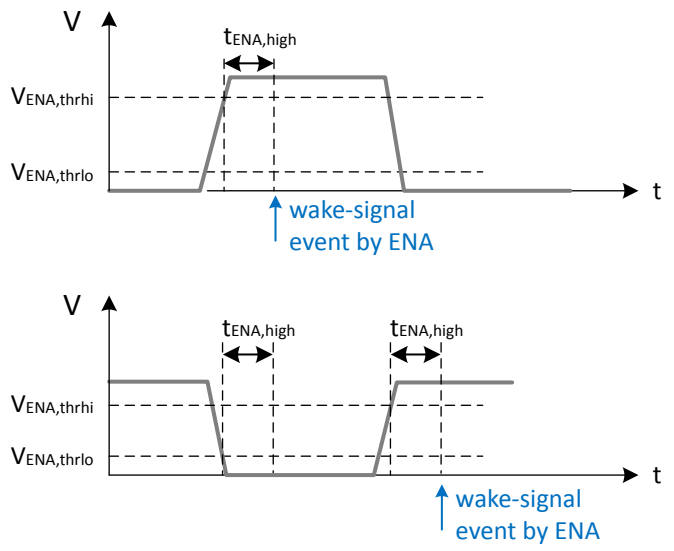


Figure 4 **Valid enable signal**

Table 5 **Electrical characteristics Enable signal**

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Enable EN							
Enable upper threshold	$V_{ENA,thrhi}$	–	–	1.95	V	V_{ENA} increasing	P_5.2.1
Enable lower threshold	$V_{ENA,thrlo}$	1.0	–	–	V	V_{ENA} decreasing	P_5.2.2
Enable threshold hysteresis	$V_{ENA,hyst}$	200	330	500	mV	–	P_5.2.3
Enable signal high time	$t_{ENA,high}$	20	–	–	µs	–	P_5.2.4
Enable high input current	$I_{ENA,hi}$	–	8	11	µA	V_{ENA} = 16 V	P_5.2.5
Enable low input current	$I_{ENA,lo}$	–	0.1	2	µA	V_{ENA} = 0.5 V	P_5.2.6

4.3 Electrical characteristics Wake signal

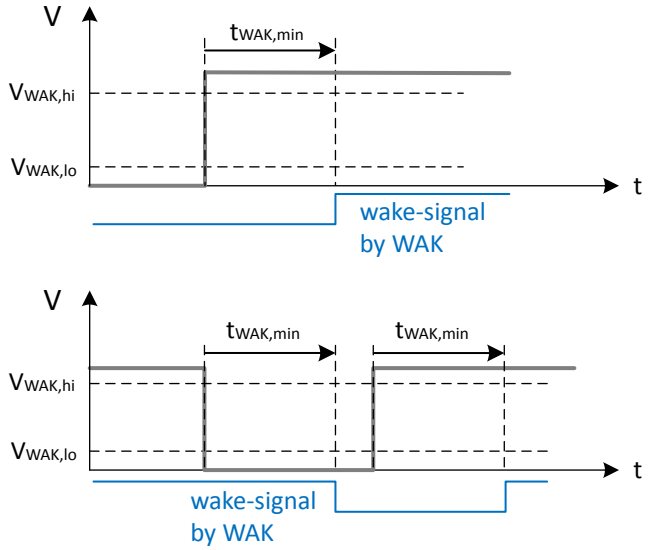


Figure 5 **Valid wake signal**

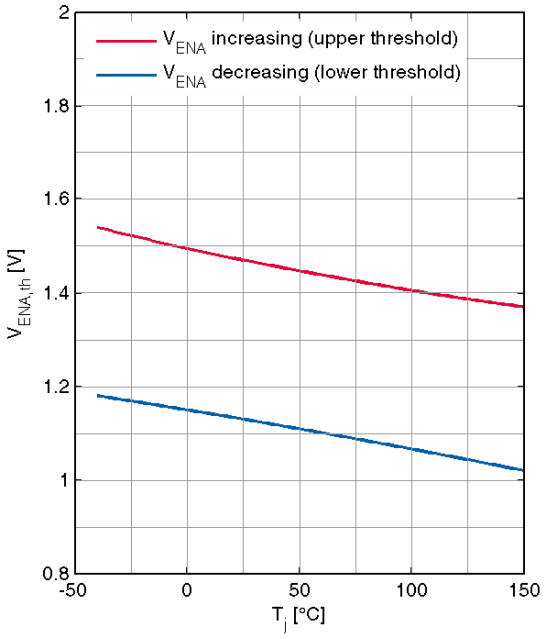
Table 6 **Electrical characteristics Wake signal**

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

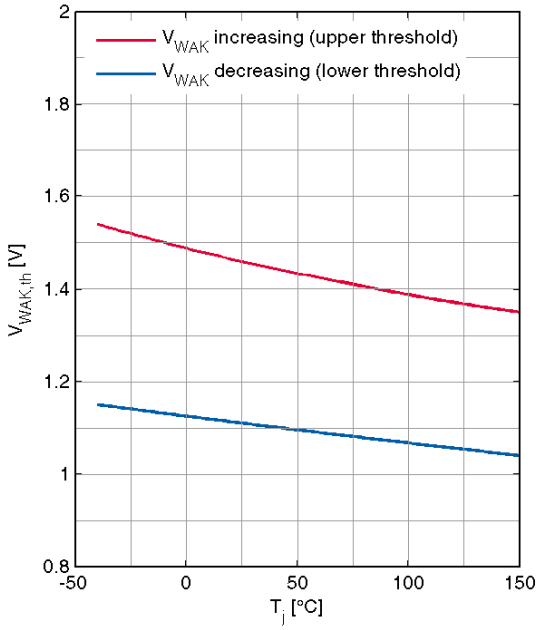
Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Wake/Inhibit							
Wake upper threshold	$V_{WAK,hi}$	–	–	1.95	V	V_{WAK} increasing	P_5.3.1
Wake lower threshold	$V_{WAK,lo}$	1.0	–	–	V	V_{WAK} decreasing	P_5.3.2
Wake signal hysteresis	$V_{WAK,hyst}$	200	330	500	mV	–	P_5.3.3
Wake signal minimum length	$t_{WAK,min}$	40	–	–	µs	–	P_5.3.4
Wake high input current	$I_{WAK,hi}$	–	8	11	µA	V_{WAK} = 5.0 V	P_5.3.5
Wake low input current	$I_{WAK,lo}$	–	0.1	2	µA	V_{WAK} = 0.5 V	P_5.3.6

4.4 Typical performance characteristics Wake and Enable signals

Enable input threshold voltage $V_{ENA,th}$ versus junction temperature T_j



Wake input threshold voltage $V_{WAK,th}$ versus junction temperature T_j



5 Pre regulators

5.1 Introduction pre regulators

The pre regulator is mandatory to maintain a stabilized and constant intermediate circuit voltage to supply the following post regulators. It consists of two independent regulators: A step up converter with an external power stage in front to maintain a minimum input voltage to the following step down converter.

The step up converter can be deactivated (if not needed) by connecting pin STU to ground. Leaving pin STU open activates the step up regulator.

The step down regulator frequency can be preset by leaving pin FRE open for the high switching frequency range or connecting to GND for the low switching frequency range.

The step down converter is constantly on, providing a stabilized intermediate circuit voltage V_{PREREG} to supply the following post regulators. The step up converter is connected directly to the input voltage V_{Bat}. It only operates during low input voltage condition (i.e. cranking) when the input voltage drops below the threshold $V_{PRE_REG,boost,UV}$, to maintain an input voltage high enough for the following step down regulator. Low input voltage condition means, that the input voltage at pin VSx is too low to provide an intermediate circuit voltage V_{PREREG} within the specified limits. An internal comparator connected to the input voltage path detects the threshold when to turn on the step up converter. In case the input voltage is above the step up converter output voltage (threshold for switching on the step up converter), this regulator is deactivated by the internal comparator. An internal logic switches the step up converter on (and off again) whenever it is needed.

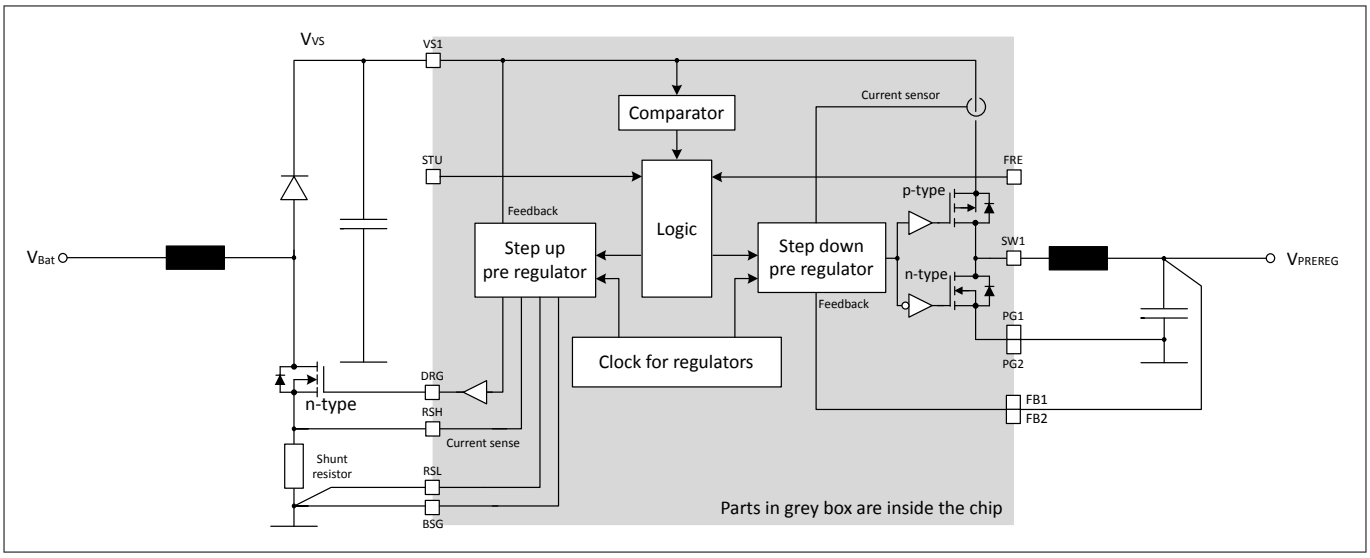


Figure 6 **Principle pre regulator stage**

5.2 Step up pre regulator

5.2.1 Functional description step up pre regulator

The asynchronous step up pre regulator provides a higher output voltage than the input voltage when operating. This is the case whenever the supply voltage should be too low to allow nominal values at the post regulator outputs. The boost pre regulator output voltage is well below the nominal supply (battery) voltage to make sure, that it only operates during low input voltage conditions.

Protection functions are installed to prevent the regulator and the application from damage:

- To protect the external components of the step up pre regulator from overstress a shunt resistor based peak current limitation (specified by $V_{RSH-RSL}$) limits the duty cycle of the DRG pin to avoid excessive current flows, thus the output voltage decreases. In case the step up pre regulator operates in peak current limitation for more than $t_{StG,boost}$, the device moves into FAILSAFE-state. This event is stored in the SPI status register bitfield **MONSF3**.STUSG.
- An over current pre warning is implemented to provide an interrupt based warning, if the current through the shunt resistor is generating a voltage of more than $0.8*V_{RSH-RSL}$ for more than 500 µs. The diagnosis of over current pre warning is indicated to **CEFUMON**.STUOC.

If the step up feature should not be necessary for the application, the external power elements (MOSFET, diode, shunt-resistor) could be skipped, the filter elements might be adjusted to the application requirements.

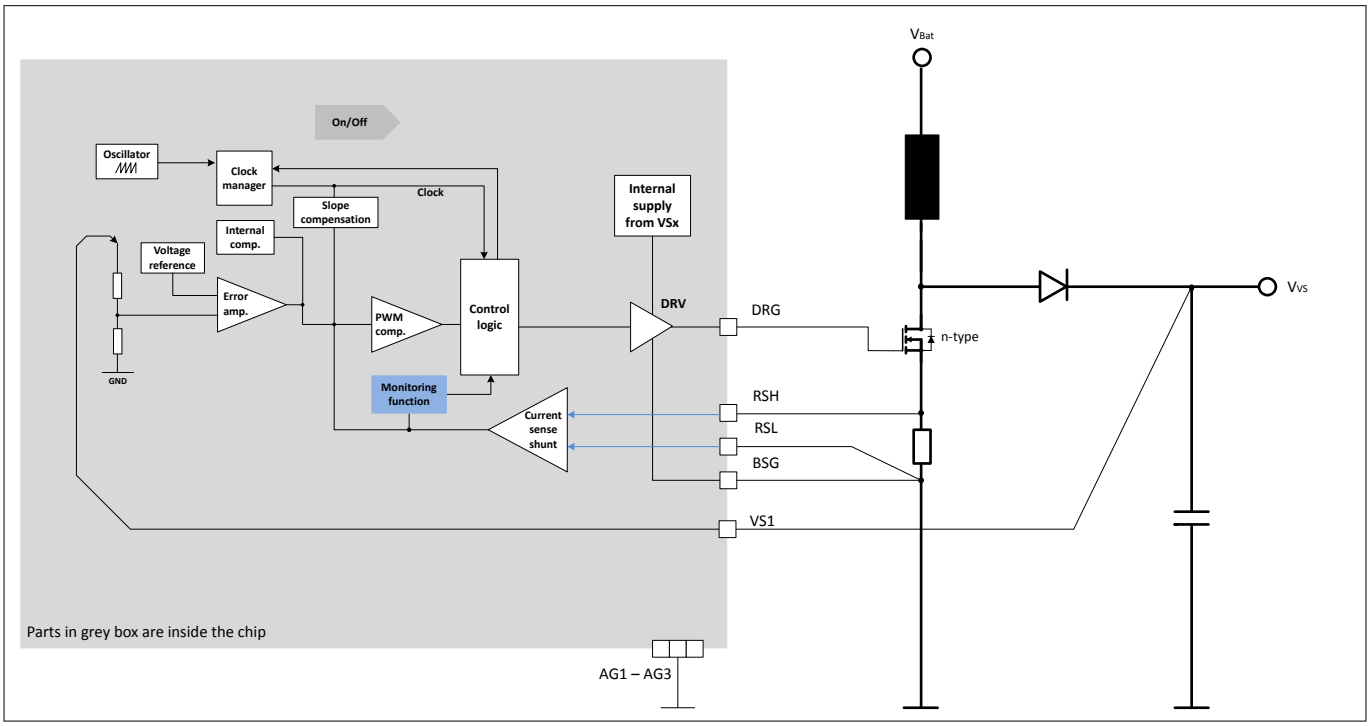


Figure 7 **Step up regulator**

5.2.2 Electrical characteristics step up pre regulator

Table 7 Electrical characteristics step up pre regulator

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Step up pre regulator							
Pre regulator boost output voltage	$V_{PREREG,boost}$	7.00	7.5	8.00	V	–	P_6.2.2.1
Threshold external sense resistor for OC	$V_{RSH-RSL}$	190	210	230	mV	–	P_6.2.2.2
Low side sense input current	I_{RSL}	-45	-30	-15	µA	V_{RSL} = 0 V	P_6.2.2.3
High side sense input current	I_{RSH}	-45	-30	-15	µA	tested at V_{RSH} = 0 V	P_6.2.2.4
Input undervoltage threshold	$V_{PREREG,boost,UV}$	8	8.3	8.6	V	–	P_6.2.2.5
Input undervoltage threshold hysteresis	$V_{PREREG,boost,UV,hyst}$	80	–	200	mV	–	P_6.2.2.6
Gate driver sourcing current	$I_{DRG,SRC}$	100	130	160	mA	measured at V_{DRG} = 2.5 V	P_6.2.2.7
Gate driver sinking current	$I_{DRG,SNK}$	100	130	160	mA	measured at V_{DRG} = 2.5 V	P_6.2.2.8
Gate driver sinking current (boost off)	$I_{DRG,SNK,off}$	TBD	TBD	TBD	mA	measured at V_{DRG} = 1.0 V	P_6.2.2.9
Gate driver output voltage	V_{DRG}	4.5	5	5.5	V	–	P_6.2.2.11
Maximum duty cycle	D_{MAX}	75	80	–	%	–	P_6.2.2.12
Blanking time	t_{Blank}		240		ns	–	P_6.2.2.13
Input inductor	L_{Boost}	15.4	22	28.6	µH	*14) 15)*	P_6.2.2.14
Output main capacitor	C_{Boost}	56	100	220	µF	*14) 15)*	P_6.2.2.15
Output main capacitor ESR	$ESR_{C,Boost}$	10	–	300	mΩ	*14)* Relevant ESR at capacitors self-resonance frequency.	P_6.2.2.16
Output support capacitor	C_{Boost2}	0.7	–	–	µF	*14) 15)* ceramic capacitor	P_6.2.2.17

(table continues...)

14 Specified by design, not subject to production test

15 The input filter natural frequency (1/√(L*C)) is to be maintained in the range of 24 kHz +/- 25 %. Accordingly the inductance and capacitance is to be selected in mutual correlation. E.g. a smaller inductance requires a bigger capacitance in order to grant stability.

Table 7 (continued) Electrical characteristics step up pre regulator

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Output support capacitor ESR	$ESR_{C,Boost2}$	–	15	30	mΩ	[14] Relevant ESR at capacitors self-resonance frequency.	P_6.2.2.18

[14] Specified by design, not subject to production test

5.3 Step down pre regulator

5.3.1 Functional description step down pre regulator

The synchronous step down pre regulator is continuously in operation providing a stable intermediate circuit voltage to supply the following post regulators. The internal power stage consists of synchronous P-channel (high side) and N-channel (low side) MOSFET's. For start-up a softstart function is implemented.

The regulation loop operates in current mode.

In the operative states the step down pre regulator operates in Continuous Conduction Mode(CCM) using Pulse Width Modulation (PWM). In SLEEP state under light load conditions the device operates in Discontinuous Conduction Mode(DCM) using Pulse Frequency Modulation (PFM) whenever applicable to minimize the internal current consumption (only in SLEEP-state, not in NORMAL, WAKE or INIT-state).

The output filter of the step down regulator has to be sized to ensure a maximum output voltage ripple of 100 mV in order to be in line with the PSRR specified for the post regulators.

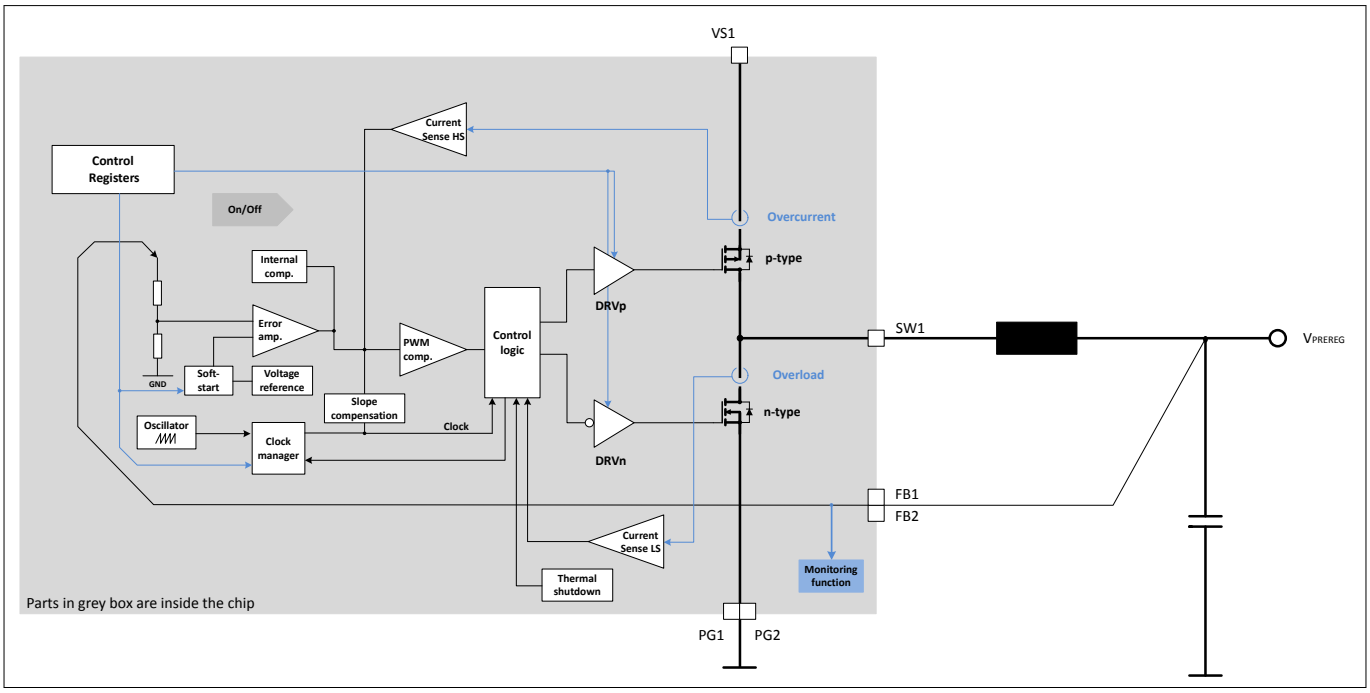


Figure 8 **Step down regulator**

5.3.2 Electrical characteristics step down pre regulator

Table 8 Electrical characteristics step down pre regulator

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Step down pre regulator							
Output voltage	$V_{PREREG,BUCK}$	5.65	5.8	5.95	V	PWM-mode; $V_{VS} \geq 5.75$ V + ($R_{ON,HS}$[Max] + DCR_{ext}) * $I_{PREREG,BUCK}$; $I_{PREREG,BUCK} \leq 1.5$ A; $T_j \leq 150$ °C	P_6.3.2.1
Output voltage	$V_{PREREG,BUCK,hot}$	5.65	5.8	6.10	V	PWM-mode; $V_{VS} \geq 5.75$ V + ($R_{ON,HS,hot}$[Max] + DCR_{ext}) * $I_{PREREG,BUCK}$; $I_{PREREG,BUCK} \leq 1.2$ A	P_6.3.2.2
Output voltage	$V_{PREREG,BUCK}$	5.6	5.8	6.00	V	PFM-mode; $V_{VS} \geq 5.7$ V + ($R_{ON,HS}$[Max] + DCR_{ext}) * $I_{PREREG,BUCK}$; $T_j \leq 150$ °C	P_6.3.2.3
Output voltage	$V_{PREREG,BUCK,hot}$	5.6	5.8	6.20	V	PFM-mode; $V_{VS} \geq 5.7$ V + ($R_{ON,HS,hot}$[Max] + DCR_{ext}) * $I_{PREREG,BUCK}$;	P_6.3.2.4
Power stage high side switch on resistance	$R_{ON, HS}$	150	350	580	mΩ	$V_{VS} \geq 6$ V; $T_j \leq 150$ °C	P_6.3.2.5
Power stage high side switch on resistance	$R_{ON, HS,hot}$	150	350	720	mΩ	$V_{VS} \geq 6$ V	P_6.3.2.6
Power stage low side switch on resistance	$R_{ON, LS}$	50	200	300	mΩ	$V_{VS} \geq 6$ V; $T_j \leq 150$ °C	P_6.3.2.7
Power stage low side switch on resistance	$R_{ON, LS,hot}$	50	200	345	mΩ	$V_{VS} \geq 6$ V	P_6.3.2.8
Buck peak overcurrent limit	$I_{PREREG, max}$	1.95	2.4	2.8	A	–	P_6.3.2.9

(table continues...)

Table 8 (continued) Electrical characteristics step down pre regulator

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
SW rise time	$t_{R, Buck}$	2	6	14	ns	[16] 6.5V ≤ V_{VS} ≤ 18 V; I_{PREREG} ≥ 0.5 A	P_6.3.2.10
SW fall time	$t_{F, Buck}$	2	9	18	ns	[16] 6.5V ≤ V_{VS} ≤ 18 V; I_{PREREG} ≥ 0.5 A	P_6.3.2.11
Maximum duty cycle	$D_{BUCK, max}$	-	-	100	%	–	P_6.3.2.12
Minimum switch on time	$t_{ON, min}$	20	70	85	ns	I_{PREREG} ≥ 0.5 A	P_6.3.2.13
Softstart ramp (HF)	$t_{SS, BUCK}$	400	640	705	µs	[16] $V_{PREREG,BUCK}$ rising from 5 % to 95 % of typ. $V_{PREREG,BUCK}$; 2.2 MHz switching frequency (pin FRE open), no load	P_6.3.2.14
Softstart ramp (LF)	$t_{SS, BUCK}$	3.2	5.12	5.65	ms	[16] $V_{PREREG,BUCK}$ rising from 5 % to 95 % of typ. $V_{PREREG,BUCK}$; 400 kHz switching frequency (pin FRE to GND), no load	P_6.3.2.15
Current threshold for transition from PWM to PFM	$I_{PWM/PFM}$	26	57	90	mA	–	P_6.3.2.16
Current threshold for transition from PFM to PWM	$I_{PFM/PWM}$	100	145	190	mA	–	P_6.3.2.17
Overtemperature warning threshold	$T_{j,OT, WRN}$	135	145	158	°C	T_j increasing [16]	P_6.3.2.18
Overtemperature shutdown threshold	$T_{j,OT, shutdown}$	176	190	200	°C	T_j increasing [16]	P_6.3.2.19
Overtemperature sensor hysteresis	$T_{j,OT, hyst}$	–	10	–	°C	[16]	P_6.3.2.20

(table continues...)

16 Specified by design, not subject to production test

Table 8 (continued) Electrical characteristics step down pre regulator

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Output inductor (HF)	$L_{BUCK,HF}$	2.65	4.7	8.2	µH	16) 17) 2.2 MHz nominal switching frequency (pin FRE open)	P_6.3.2.21
Output capacitor (HF)	$C_{BUCK,HF}$	8.0	22	56.5	µF	16) 17) 2.2 MHz nominal switching frequency (pin FRE open)	P_6.3.2.22
Output capacitor ESR (HF)	$ESR_{C,HF}$	1	–	150	mΩ	16) Relevant ESR at capacitors self-resonance frequency. 2.2 MHz nominal switching frequency (pin FRE open)	P_6.3.2.23
Output inductor (LF)	$L_{BUCK,LF}$	12.5	22	81.5	µH	16) 18) 440 kHz nominal switching frequency (pin FRE to GND)	P_6.3.2.24
Output capacitor (LF)	$C_{BUCK,LF}$	54	100	265	µF	16) 18) 440 kHz nominal switching frequency (pin FRE to GND)	P_6.3.2.25

(table continues...)

16 Specified by design, not subject to production test

17 The output filter natural frequency (1/√(L*C)) is to be maintained in the range of 100 kHz +/- 25 %. Accordingly the inductance and capacitance is to be selected in mutual correlation. E.g. a smaller inductance requires a bigger capacitance in order to grant stability.

18 The output filter natural frequency (1/√(L*C)) is to be maintained in the range of 24 kHz +/- 25 %. Accordingly the inductance and capacitance is to be selected in mutual correlation. E.g. a smaller inductance requires a bigger capacitance in order to grant stability.

Table 8 (continued) Electrical characteristics step down pre regulator

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Output capacitor ESR (LF)	$ESR_{C,LF}$	5	–	300	mΩ	[16] Relevant ESR at capacitors self-resonance frequency. 440 kHz nominal switching frequency (pin FRE to GND)	P_6.3.2.26
Active discharge pull-down	$R_{BUCK,pd}$	60	100	215	Ω	[16] $V_{PREREG,BUCK} \geq 2$ V	P_6.3.2.27

16 Specified by design, not subject to production test

5.3.3 Typical performance characteristics step down pre regulator

Pre regulator output voltage V_{PreReg} versus junction temperature T_j (FRE-Pin: open)

Pre regulator output voltage V_{PreReg} versus junction temperature T_j (FRE-Pin: GND)

Pre regulator output voltage V_{PreReg} versus load current I_{PreReg} (FRE-Pin: open)

Pre regulator output voltage V_{PreReg} versus load current I_{PreReg} (FRE-Pin: GND)

Pre regulator output voltage V_{PreReg} versus supply voltage V_{VS} (FRE-Pin: open)

Pre regulator output voltage V_{PreReg} versus supply voltage V_{VS} (FRE-Pin: GND)

High-side switch ON resistance $R_{ON, HS}$ versus supply voltage V_{VS}

Low-Side switch ON resistance $R_{ON, LS}$ versus supply voltage V_{VS}

PreReg dynamic load response (2 mA to 500 mA) (FRE-Pin: open; $V_{PreReg,nom}$ = 5.8 V)

PreReg dynamic load response (2 mA to 500 mA) (FRE-Pin: GND; $V_{PreReg,nom}$ = 5.8 V)

5.4 Frequency setting

5.4.1 Introduction frequency setting

The frequency source supplies the step up pre regulator and the step down pre regulator with a constant frequency. The synchronous power switches of the step down pre regulator are switching with the frequency f_{OSC}.

The frequency range of the step down pre regulator can be set to the high switching frequency range by leaving pin FRE open or to the low switching frequency range by connected the pin FRE to GND. The switching frequency is set to the default value of the chosen frequency range. Optionally it can be fine tuned by SPI command (**BCK_FREQ_CHANGE**) or the spread-spectrum option can be activated (**BCK_FRE_SPREAD**).

The switching frequency range of the step up pre regulator is synchronized to switching frequency range of the step down pre regulator. For the low frequency range of the step-down pre regulator the ratio of the synchronization is 1:1. For the high frequency range of the step-down pre regulator the ratio of the synchronization is 1:5. The synchronization aligns the step down pre regulator high-side switch activation (rising edge of buck switching node) with the step up pre regulators low side NMOS activation (falling edge of boost switching node) with an delay of approximately 10 ns.

The switching frequency of the step down pre regulator can be made available by SPI configuration at pin SYN for the optional external switch mode post regulator for the MCU core supply.

The synchronization functions are not available in the step down pre regulators PFM mode (SLEEP-state).

The TLF35585QV cannot be synchronized to an external frequency source.

5.4.2 Electrical characteristics frequency setting

Table 9 Electrical characteristics frequency setting

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Frequency setting FREQ							
Step-up frequency range	$f_{OSC,step-up}$	395	440	485	kHz	–	P_6.4.2.1
Step-down low frequency range	$f_{OSC,step-down}$	395	440	485	kHz	FRE pin connected to GND	P_6.4.2.2
Step-down high frequency range	$f_{OSC,step-down}$	2000	2200	2400	kHz	FRE pin open	P_6.4.2.3

5.4.3 Typical performance characteristics frequency setting

Step-up switching frequency $f_{OSC,step\text{-}up}$versus junction temperature T_j (FRE-Pin: open)

Step-down switching frequency $f_{OSC,step\text{-}down}$versus junction temperature T_j (FRE-Pin: GND)

Step-down switching frequency $f_{OSC,step\text{-}down}$versus junction temperature T_j (FRE-Pin: open)

6 Post regulators

6.1 Introduction post regulators

The TLF35585QV includes a number of linear low drop post regulators and trackers and offers the possibility to connect an external post regulator for the MCU core supply if needed.

The linear post regulators and trackers are supplied from pins FBx. The bandgap 1 for regulator block provides the reference values for the error amplifiers of microcontroller main supply (pin QUC), the communication supply (pin QCO) and the reference voltage supply (pin QVR). The trackers get their reference value from the reference voltage supply (pin QVR). The output voltage of trackers 1 and 2 (present at pins QT1 and QT2) is following the reference voltage supply QVR with a small drop.

An additional external post regulator can be added to deliver the core supply for the microcontroller. If this option is used the configuration pin SEC must be left open. If the option is not used, pin SEC must be connected to ground.

The post regulator is to be connected external and uses its own reference voltage, the input is fed from the pre regulator output voltage V_{PREREG} (which is similar to the values at pins FBx). The post regulator is enabled by a high signal at pin EVC and switched off with a low signal at pin EVC. A synchronization signal (in phase or shifted by 180 degree with the step down pre regulator signal) is offered at pin SYN for usage of a switch mode post regulator.

All output voltages of the post regulators are connected to the voltage monitoring function (please refer to chapter Monitoring function).

In case of a detected overvoltage or short to ground condition the related post regulator is switched off, the shutdown signal is generated by the voltage monitoring function.

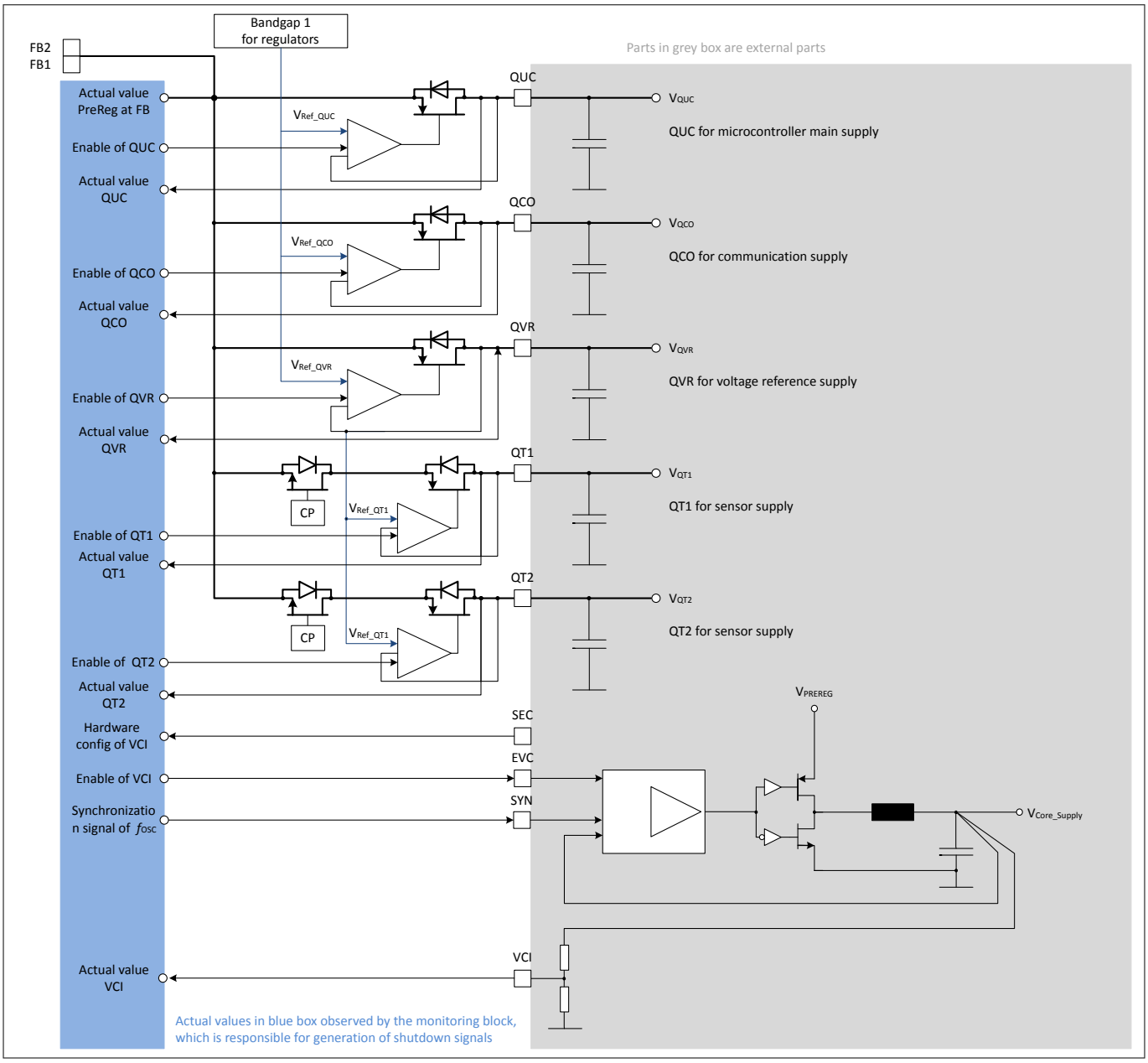


Figure 9 **Principle post regulators**

6.2 Microcontroller main supply QUC

6.2.1 Functional description microcontroller main supply

The linear low drop regulator QUC offers a precise 3.3 V or 5.0 V output voltage for microcontroller main supply.

The regulator is supplied from the intermediate circuit voltage V_{PREREG} which provides a stabilized voltage. The output voltage V_{QUC} (at pin QUC) is controlled by the error amplifier. The actual value is compared to a reference voltage derived from bandgap 1 for regulators. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor should be chosen according the specified requirements (capacitance value and electrical series resistance ESR) in Table 10. The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.

Protection circuitry is installed to prevent the regulator and the application from damage:

- To protect the pass element of the QUC from overstress the current limitation limits the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached, the current is limited, thus the output voltage decreases. The regulator is protected against short circuit to ground.
- The output voltage is monitored by the voltage monitoring. In case of overvoltage at pin QUC, the QUC is switched off and the device moves into FAILSAFE-state. The event is stored in the SPI status register (**MONSF1**). In case of undervoltage at pin QUC, the device moves into INIT-state, pin ROT is pulled low and the event is stored in an SPI status register (**MONSF2**). The regulator is not switched off in case of output undervoltage, which is shorter than the short to ground detection time t_{StG}. If the undervoltage should be present for more than t_{StG}, the device moves into FAILSAFE-state. This event is stored in an SPI status register as well (**MONSF0**).
- There is a dedicated temperature sensor for this regulator. In case the power stage temperature exceeds the pre warning threshold, an interrupt indicates this event and it is stored in an SPI status register (**OTWRNSF**). If the power stage temperature exceeds the temperature shutdown threshold, the device moves into FAILSAFE-state, the regulator is switched off and the event is stored in an SPI status register (**OTFAIL**). The off time due to temperature shut down is at least one second.

If the device enters FAILSAFE-state the ROT is pulled low and all supplies are switched off.

If the device enters STANDBY-state the QUC is switched off

For further details please refer to Chapter 10 State machine.

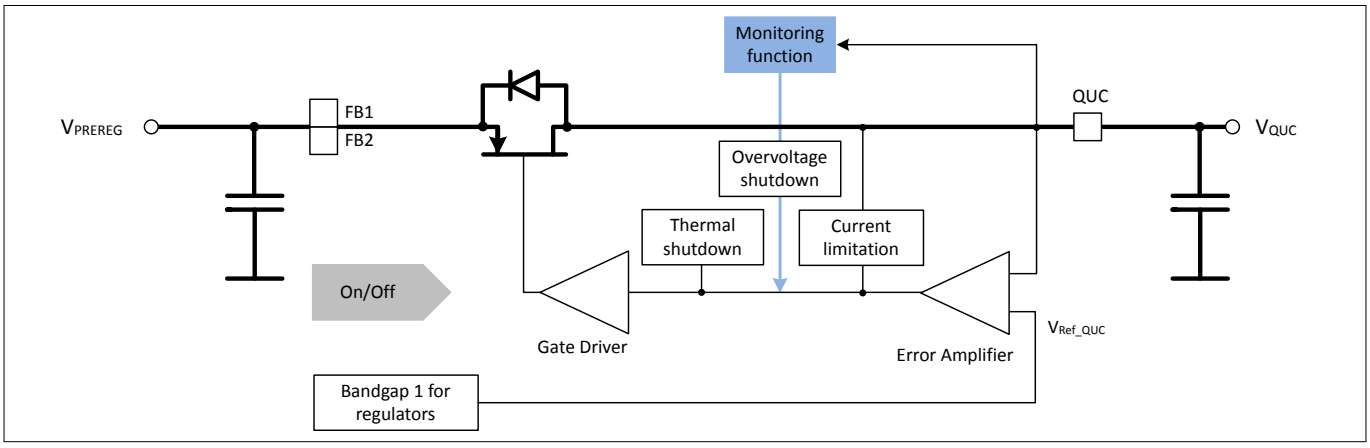


Figure 10 **Low drop linear regulator for microcontroller main supply QUC**

6.2.2 Electrical characteristics microcontroller main supply

Table 10 Electrical characteristics: microcontroller main supply

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Microcontroller main supply QUC							
Output voltage TLF35585QVS01	V_{QUC}	4.9	5.0	5.1	V	0 mA ≤ I_{QUC} ≤ 600 mA	P_7.2.2.1
Output voltage TLF35585QVS02	V_{QUC}	3.23	3.3	3.37	V	0 mA ≤ I_{QUC} ≤ 600 mA	P_7.2.2.2
Output current limitation	$I_{QUC,max}$	650	–	1100	mA	–	P_7.2.2.3
Drop voltage TLF35585QVS01	$V_{dr,QUC}$	–	–	400	mV	19)	P_7.2.2.4
Drop voltage TLF35585QVS02	$V_{dr,QUC}$	–	–	500	mV	19)	P_7.2.2.5
Load regulation TLF35585QVS01	ΔV_{QUC}	–	45	81	mV	I_{QUC} = 100µA to 600 mA	P_7.2.2.6
Load regulation TLF35585QVS02	ΔV_{QUC}	–	39	60	mV	I_{QUC} = 100µA to 600 mA	P_7.2.2.7
Power supply ripple rejection	$PSRR_{QUC}$	26	–	–	dB	20) V_{PREREG} = 5.8 V; $ESRC_{QUC}$ ≤ 100 mΩ	P_7.2.2.8
Output capacitor	C_{QUC}	2.2	–	47	µF	20)	P_7.2.2.9
Output capacitor, ESR	$ESR_{C,QUC}$	0	–	200	mΩ	20) Relevant ESR at capacitors self-resonance frequency.	P_7.2.2.10
Overtemperature warning threshold	$T_{j,OT,WRN}$	135	145	158	°C	T_j increasing 20)	P_7.2.2.11
Overtemperature shutdown threshold	$T_{j,OT,shutdown}$	176	190	200	°C	T_j increasing 20)	P_7.2.2.12
Overtemperature sensor hysteresis	$T_{j,OT,hyst}$	–	10	–	°C	20)	P_7.2.2.13

(table continues...)

19 Dropout voltage is defined as the difference between input and output voltage when the output voltage decreases 100 mV from output voltage measured at $V_I = V_{Q,nom} + V_{dr,max}$ + 100 mV.

20 Specified by design, not subject to production test

Table 10 (continued) Electrical characteristics: microcontroller main supply

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Softstart time	$t_{SS,QUC}$	130	200	270	µs	[20] C_{QUC} ≤ 15 µF; V_{QUC} rising from 5 % to 95 % of typ. V_{QUC}	P_7.2.2.14
Active discharge pull-down	$R_{QUC,pd}$	70	100	150	Ω	[20] V_{QUC} ≥ 1.8 V	P_7.2.2.15

[20] Specified by design, not subject to production test

6.2.3 Typical performance characteristics microcontroller main supply

QUC output voltage V_{QUC} versus junction temperature T_j (TLF35585QVS01)

QUC output voltage V_{QUC} versus junction temperature T_j (TLF35585QVS02)

QUC output voltage V_{QUC} versus load current I_{QUC} (TLF35585QVS01)

QUC output voltage V_{QUC} versus load current I_{QUC} (TLF35585QVS02)

QUC dropout voltage $V_{dr,QUC}$ versus load current I_{QUC} (TLF35585QVS01)

QUC dropout voltage $V_{dr,QUC}$ versus load current I_{QUC} (TLF35585QVS02)

QUC dynamic load response (1 mA to 400 mA) TLF35585QVS01 ($V_{QUC,nom}$ = 5.0 V)

QUC dynamic load response (1 mA to 400 mA) TLF35585QVS02 ($V_{QUC,nom}$ = 3.3 V)

QUC dynamic load response (1 mA to 600 mA) TLF35585QVS01 ($V_{QUC,nom}$ = 5.0 V)

QUC dynamic load response (1 mA to 600 mA) TLF35585QVS02 ($V_{QUC,nom}$ = 3.3 V)

6.3 Communication supply QCO

6.3.1 Functional description communication supply

The linear low drop regulator QCO offers a precise 5.0 V output voltage for communication supply.

The regulator is supplied from the intermediate circuit voltage V_{PREREG}, which provides a stabilized voltage. The output voltage V_{QCO} (at pin QCO) is controlled by the error amplifier. The actual value is compared to a reference voltage derived from bandgap 1 for regulators. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor should be chosen according the specified requirements (capacitance value and electrical series resistance ESR) in Table 11. The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.

Protection circuitry is installed to prevent the regulator and the application from damage:

- To protect the pass element of the QCO from overstress the current limitation limits the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached, the current is limited, thus the output voltage decreases. The regulator is protected against short circuit to ground.
- The output voltage is monitored by the voltage monitoring. In case of overvoltage at pin QCO, the QCO is switched off, the event is indicated by an interrupt and stored in an SPI status register (**MONSF1**). In case of undervoltage at pin QCO, the event is indicated by an interrupt and stored in an SPI status register (**MONSF2**). The regulator is not switched off in case of output undervoltage, which is shorter than the short to ground detection time t_{StG}. If the undervoltage should be present for more than t_{StG}, the regulator is switched off. This event is stored in the SPI status register (**MONSF0**) and an interrupt is generated.
- There is a dedicated temperature sensor for this regulator. In case the power stage temperature exceeds the pre warning threshold, an interrupt indicates this event and it is stored in an SPI status register (**OTWRNSF**). If the power stage temperature exceeds the temperature shutdown threshold, this event is stored in an SPI status register (**OTFAIL**), the regulator is switched off and an interrupt is generated. After a temperature shut down the QCO can be re enabled via SPI command.

The regulator QCO is switched off in STANDBY and FAILSAFE-state. In INIT, SLEEP, NORMAL and WAKE-state QCO is ON or OFF depending on the SPI configuration.

For further details please refer to Chapter 10 State machine.

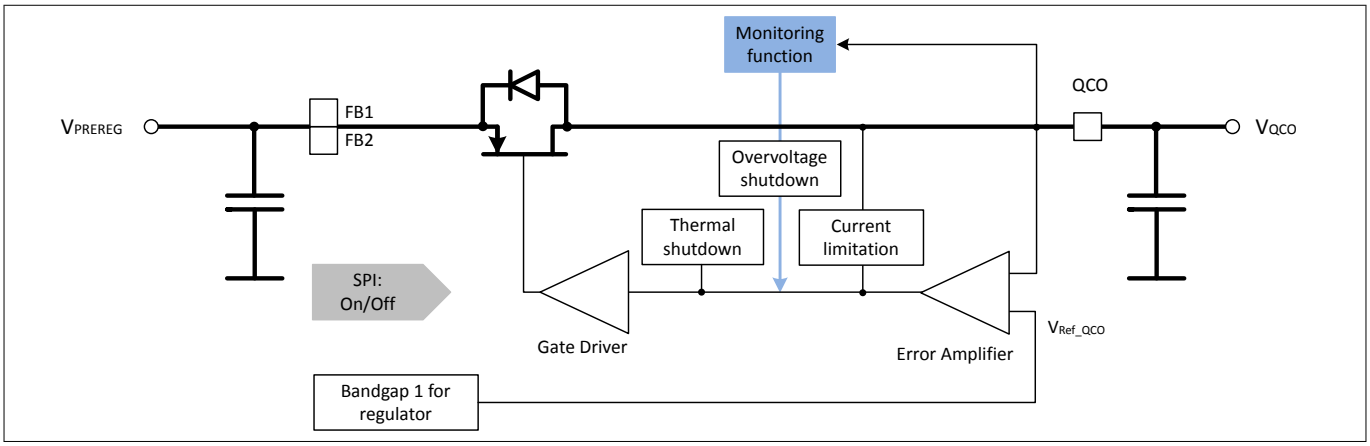


Figure 11 **Low drop linear regulator for communications supply QCO**

6.3.2 Electrical characteristics communication supply

Table 11 Electrical characteristics communication supply

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Communication supply QCO							
Output voltage	V_{QCO}	4.90	5.00	5.10	V	0 mA ≤ I_{QCO} ≤ 200 mA	P_7.3.2.1
Output current limitation	$I_{QCO, max}$	250	–	400	mA	–	P_7.3.2.2
Drop voltage	$V_{dr, QCO}$	–	–	400	mV	[21]	P_7.3.2.3
Load regulation	ΔV_{QCO}	–	40	70	mV	I_{QCO} = 100µ to 200 mA	P_7.3.2.4
Power supply ripple rejection	$PSRR_{QCO}$	26	–	–	dB	[22] V_{PREREG} = 5.8 V; $ESRC_{QCO}$ ≤ 100mΩ	P_7.3.2.5
Output capacitor	C_{QCO}	1	–	47	µF	[22]	P_7.3.2.6
Output capacitor, ESR	$ESR_{C,QCO}$	0	–	200	mΩ	[22] Relevant ESR at capacitors self-resonance frequency.	P_7.3.2.7
Overtemperature warning threshold	$T_{j,OT, WRN}$	135	145	158	°C	T_j increasing [22]	P_7.3.2.8
Overtemperature shutdown threshold	$T_{j,OT, shutdown}$	176	190	200	°C	T_j increasing [22]	P_7.3.2.9
Overtemperature sensor hysteresis	$T_{j,OT, hyst}$	–	10	–	°C	[22]	P_7.3.2.10
Softstart time	$t_{SS,QCO}$	130	200	500	µs	[22] C_{QCO} ≤ 15 µF; V_{QCO} rising from 5% to 95% of typ. V_{QCO}	P_7.3.2.11
Active discharge pull-down	$R_{QCO,pd}$	70	100	150	Ω	[22] V_{QCO} ≥ 1.8 V	P_7.3.2.12

21 Dropout voltage is defined as the difference between input and output voltage when the output voltage decreases 100 mV from output voltage measured at $V_I = V_{Q,nom} + V_{dr,max}$ + 100 mV.

22 Specified by design, not subject to production test

6.3.3 Typical performance characteristics communication supply

QCO output voltage V_{QCO} versus junction temperature T_j

QCO output voltage V_{QCO} versus load current I_{QCO}

QCO dropout voltage $V_{dr,QCO}$ versus load current I_{QCO}

QCO dynamic load response (1 mA to 100 mA) ($V_{QCO,nom}$ = 5.0 V)

6.4 Voltage reference supply QVR

6.4.1 Functional description voltage reference supply

The linear low drop regulator QVR offers a highly precise 5.0 V output voltage as a voltage reference.

The regulator is supplied from the intermediate circuit voltage V_{PREREG}, which provides a stabilized voltage. The output voltage V_{QVR} at pin QVR is controlled by the error amplifier. The actual value is compared to a reference voltage derived from bandgap 1 for regulators. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor should be chosen according the specified requirements (capacitance value and electrical series resistance ESR) in Table 12. The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.

Protection circuitry is installed to prevent the regulator and the application from damage:

- To protect the pass element of the QVR from overstress the current limitation limits the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached the current is limited, thus the output voltage decreases. The regulator is protected against short circuit to ground.
- The output voltage is monitored by the voltage monitoring.

  In case of overvoltage at pin QVR, the QVR is switched off and the device moves into FAILSAFE-state. The event is stored in an SPI status register (**MONSF1**).

  In case of undervoltage at pin QVR, the event is indicated by an interrupt and stored in an SPI status register (**MONSF2**). The regulator is not switched off in case of output undervoltage, which is shorter than the short to ground detection time t_{StG}. If the undervoltage should be present for more than t_{StG}, the regulator is switched off. This event is stored in an SPI status register (**MONSF0**) and an interrupt is generated.
- There is no dedicated temperature sensor for this regulator. The temperature is sensed on the chip by other temperature sensors located at QUC and step down pre regulator. In case of the chip temperature exceeds the pre warning threshold, an interrupt indicates this event and it is stored in a SPI status register (**OTWRNSF**). If the chip temperature exceeds the temperature shutdown threshold, the regulator is switched off. The temperature switch off time is at least one second.
- An overload at QVR (overcurrent detected for more than 1 ms) is indicated by an interrupt and it is stored in a SPI status register (**OTWRNSF**).

If the device enters FAILSAFE-state the ROT is pulled low and all supplies are switched off.

The regulator QVR is switched off in STANDBY and FAILSAFE-state. In INIT, SLEEP, NORMAL and WAKE-state QVR is ON or OFF depending on the SPI configuration.

For further details please refer to Chapter 10 State machine.

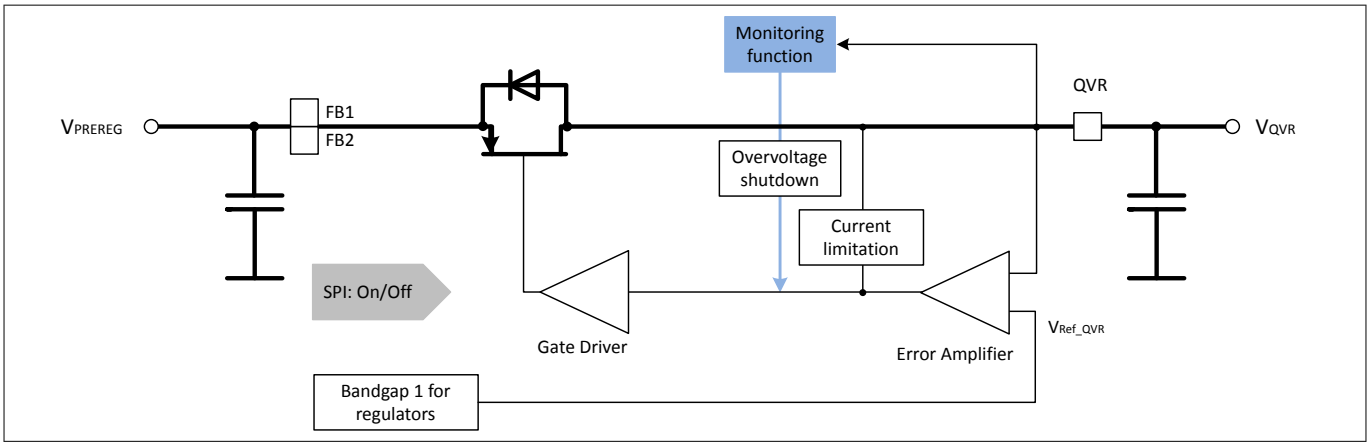


Figure 12 **Precise low drop linear regulator as a voltage reference supply QVR**

6.4.2 Electrical characteristics voltage reference supply

Table 12 Electrical characteristics voltage reference supply

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Voltage reference supply QVR							
Output voltage	V_{QVR}	4.95	5.00	5.05	V	0 mA ≤ I_{QVR} ≤ 150 mA	P_7.4.2.1
Output current limitation	$I_{QVR, max}$	170	–	345	mA	–	P_7.4.2.2
Drop voltage	$V_{dr, QVR}$	–	–	400	mV	[23]	P_7.4.2.3
Load regulation	ΔV_{QVR}	–	4.5	9	mV	I_{QVR} = 100µ to 150 mA	P_7.4.2.4
Power supply ripple rejection	$PSRR_{QVR}$	26	–	–	dB	[24] V_{PREREG} = 5.8 V; $ESRC_{QVR}$ ≤ 100 mΩ	P_7.4.2.5
Output capacitor	C_{QVR}	1	–	10	µF	[24]	P_7.4.2.6
Output capacitor, ESR	$ESR_{C,QVR}$	0	–	200	mΩ	[24] Relevant ESR at capacitors self-resonance frequency.	P_7.4.2.7
Softstart time	$t_{SS,QVR}$	130	200	350	µs	[24] C_{QVR} ≤ 10 µF; V_{QVR} rising from 5 % to 95 % of typ. V_{QVR}	P_7.4.2.8
Active discharge pull-down	$R_{QVR,pd}$	70	100	150	Ω	[24] V_{QVR} ≥ 1.8 V	P_7.4.2.9

23 Dropout voltage is defined as the difference between input and output voltage when the output voltage decreases 100 mV from output voltage measured at $V_I = V_{Q,nom} + V_{dr,max}$ + 100 mV.

24 Specified by design, not subject to production test

6.4.3 Typical performance characteristics voltage reference supply

QVR output voltage V_{QVR} versus junction temperature T_j

QVR output voltage V_{QVR} versus load current I_{QVR}

QVR dropout voltage $V_{dr,QVR}$ versus load current I_{QVR}

QVR dynamic load response (1 mA to 100 mA) ($V_{QVR,nom}$ = 5.0 V)

6.5 Tracker 1 QT1 and tracker 2 QT2

6.5.1 Functional description tracker 1 and tracker 2

The linear trackers 1 and 2 offer a sensor supply with a very high accuracy referred to voltage reference output (pin QVR).

Both trackers are supplied by the intermediate circuit voltage V_{PREREG}, which provides a stabilized voltage. The output voltage V_{QTx} at pin QTx is controlled by the error amplifier. The actual value is compared to a reference voltage provided by the reference voltage V_{QVR} at pin QVR. The tracker output voltages follow the QVR output with a very small drop. The stability of the control loop depends on the load current, the characteristics of the output capacitor and the chip temperature. To ensure a stable operation the output capacitor for each tracker should be chosen according the specified requirements (capacitance value and electrical series resistance ESR) in Table 13. The input capacitor shown in figure below is the output filter capacitor of the step down pre regulator.

Protection circuitry is installed to prevent damage to both trackers and the application:

- To protect the pass element of a tracker from overstress the current limitation limits the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current condition is reached, the current is limited and in consequence the output voltage decreases. A tracker is protected against short circuit to ground and short circuit to battery voltage.
- The output voltage is monitored by the voltage monitoring.

  In case of overvoltage at pin QTx, the corresponding tracker is switched off, the event is stored in an SPI status register (**MONSF1**) and an interrupt is generated.

  In case of undervoltage at pin QTx, the event is stored in an SPI status register (**MONSF2**) and an interrupt is generated. The tracker is not switched off in case of output undervoltage, which is shorter than the short to ground detection time t_{StG}. If the undervoltage should be present for more than t_{StG}, the tracker is switched off. This event is stored in an SPI status register (**MONSF0**) and an interrupt is generated.
- The tracker is capable to withstand a short circuit either to ground or to battery voltage without receiving a damage.

  In case of a short circuit to battery voltage and if the battery voltage is above the tracker overvoltage threshold, the tracker is switched off, the event is stored in the SPI status register (**MONSF1**).
- There is no dedicated temperature sensor for this regulator. The temperature is sensed on the chip by other temperature sensors located at QUC and step down pre regulator. In case of the chip temperature exceeds the pre warning threshold, the event is stored in an SPI status register (**OTWRNSF**) and an interrupt is generated. If the chip temperature exceeds the temperature shutdown threshold, the tracker is switched off. The temperature switch off time is at least one second.

Both trackers are switched off in STANDBY and FAILSAFE. In INIT, NORMAL, SLEEP and WAKE-state each tracker is ON or OFF depending on the SPI configuration.

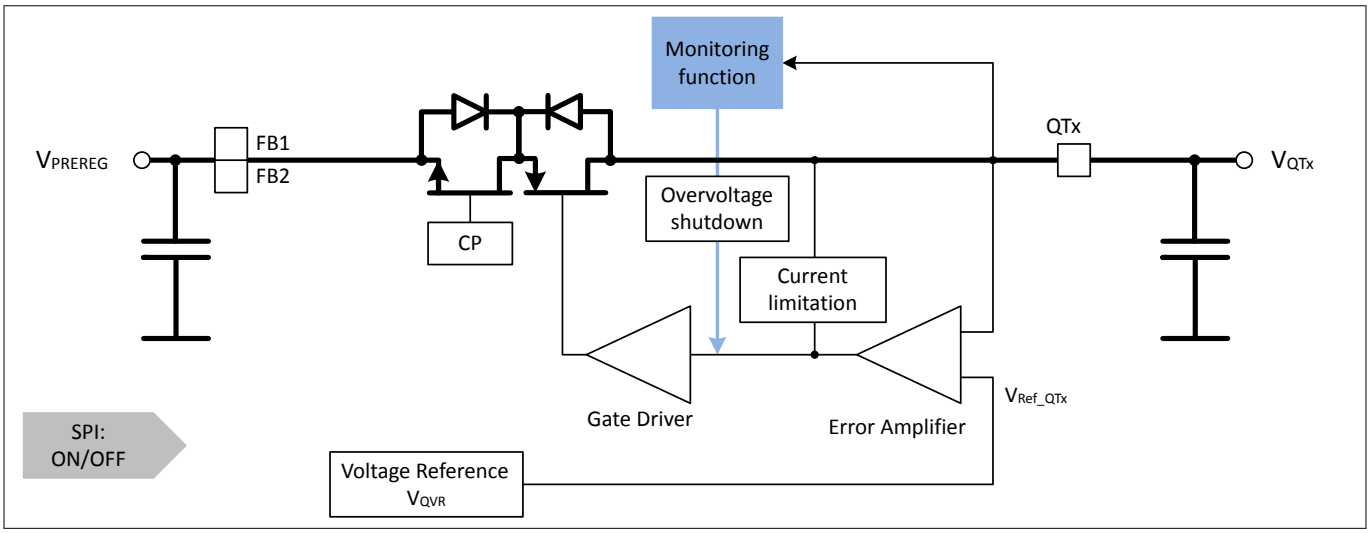


Figure 13 **Tracker 1 QT1 and tracker 2 QT2 for sensor supply**

6.5.2 Electrical characteristics tracker 1 and tracker 2

Table 13 **Electrical characteristics tracker 1 and tracker 2**

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Tracker 1 QT1 and tracker 2 QT2							
Output voltage tracking accuracy to voltage reference [25]	ΔV_{QTx}	– 10	–	10	mV	0 mA ≤ I_{QT1} ≤ 150 mA	P_7.5.2.1
Output current limitation	$I_{QTx, max}$	170	–	320	mA	–	P_7.5.2.2
Drop voltage	$V_{dr, QTx}$	–	–	400	mV	[26]	P_7.5.2.3
Power supply ripple rejection	$PSRR_{QTx}$	26	–	–	dB	[27] V_{PREREG} = 5.8 V ; $ESRC_{QTx}$ ≤ 100 mΩ	P_7.5.2.4
Output capacitor	C_{QTx}	1	–	10	µF	[27]	P_7.5.2.5

(table continues...)

25 The output voltage of the tracker (pin QTx) is derived from the output voltage of the voltage reference (pin QVR). If the voltage reference supply is switched off (voltage at pin QVR drops to 0V), then the output voltage at pin QTx decreases to 0V as well, if the tracker should be switched on as the tracker output voltage is derived from pin QVR. Still if the tracker is switched on and its output voltage drops to 0V (because voltage at pin QVR drops), an undervoltage at pin QTx is detected and an interrupt is issued.

26 Dropout voltage is defined as the difference between input and output voltage when the output voltage decreases 100 mV from output voltage measured at $V_I = V_{Q,nom} + V_{dr,max}$ + 100 mV.

27 Specified by design, not subject to production test

Table 13 (continued) Electrical characteristics tracker 1 and tracker 2

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Output capacitor, ESR	*ESR* C_{QTx}	0	–	200	mΩ	[27] Relevant ESR at capacitors self-resonance frequency.	P_7.5.2.6
Softstart time	$t_{SS,QTx}$	130	200	270	µs	[27] I_{QTx} ≤ 75 mA; V_{QTx} rising from 5 % to 95 % of typ. V_{QTx}	P_7.5.2.7

[27] Specified by design, not subject to production test

6.5.3 Typical performance characteristics tracker 1 and tracker 2

QTx output voltage V_{QTx} versus junction temperature T_j

QTx output voltage V_{QTx} versus load current I_{QTx}

QTx dropout voltage $V_{dr,QTx}$ versus load current I_{QTx}

QTx dynamic load response (1 mA to 100 mA) ($V_{QTx,nom}$ = 5.0 V)

6.6 External post regulator for core supply (optional)

An additional external post regulator may be added to the TLF35585QV to provide the core supply voltage V_{Core_Supply} for the MCU if needed. In this case the configuration pin SEC has to be left open to indicate that the external core voltage supply option is active. The configuration of the SEC pin is only read during the power sequencing at the point the core supply would be started (Movements to INIT, please refer to Figure 15 and Figure 16).

The regulator is fed from the intermediate circuit voltage V_{PREREG}.The post regulator is enabled by a high signal at pin EVC and switched off by a low signal at pin EVC. The EVC signal is controlled by the state machine. For example a detection of overvoltage at pin VCI creates a low signal at pin EVC and shut down the post regulator to protect the MCU core. In case the external post regulator uses a softstart function, the start-up time has to be aligned with the short to ground detection time $t_{StG,VCI}$.

The device offers a synchronization signal of 50% duty cycle at pin SYN equal in phase (only with a very small delay) and frequency or shifted by 180 degree to the internal step down pre regulator (the selection is done via SPI command). It is highly recommended to synchronize the external switch mode post regulator to this signal to avoid interferences. The external post regulator is enabled as soon as the pre regulator output voltage V_{PREREG} is present and the QUC output voltage V_{QUC} is above the lower reset threshold.

The output voltage of the post regulator V_{Core_Supply} is monitored by the reset function of the device. To obtain a proper monitoring the output voltage of the post regulator has to be connected to the voltage monitoring input at pin VCI via a resistor divider. The resistor divider should be dimensioned to adjust the post regulator output voltage V_{Core_Supply} to the internal reset reference voltage V_{VCI}.

The synchronization signal at pin SYN can be switched on via SPI command, default configuration is off.

Protection circuitry should be installed to prevent the external regulator and the application from damage:

- To protect the pass device(s) of the external post regulator from overstress a current limitation function should limit the output current to the maximum specified limit. The regulator should be protected against short circuit to ground.
- The output voltage is monitored by the voltage monitoring of the TLF35585QV, no further reset function is required on the external post regulator. In case such a reset function should be present, it is not used or supported by the reset function of the TLF35585QV.

  In case of overvoltage at pin, VCI the external post regulator is switched off by pulling pin EVC to low and the TLF35585QV moves into FAILSAFE-state. The event is stored in an SPI status register (**MONSF1**).

  In case of undervoltage at pin VCI, the device moves into INIT-state, pin ROT is pulled low and the event is stored in an SPI status register (**MONSF2**). The external post regulator is not switched off in case of output undervoltage, which is shorter than the short to ground detection time $t_{StG,VCI}$. If the undervoltage is present for more than $t_{StG,VCI}$, the device moves into FAILSAFE-state. This event is stored in an SPI status register as well (**MONSF0**).
- There should be a temperature shutdown function at the external post regulator. If the power stage temperature should exceed the temperature shutdown threshold, the post regulator should be switched off by its own temperature shutdown. The TLF35585QV recognizes this as an undervoltage and react as described above.

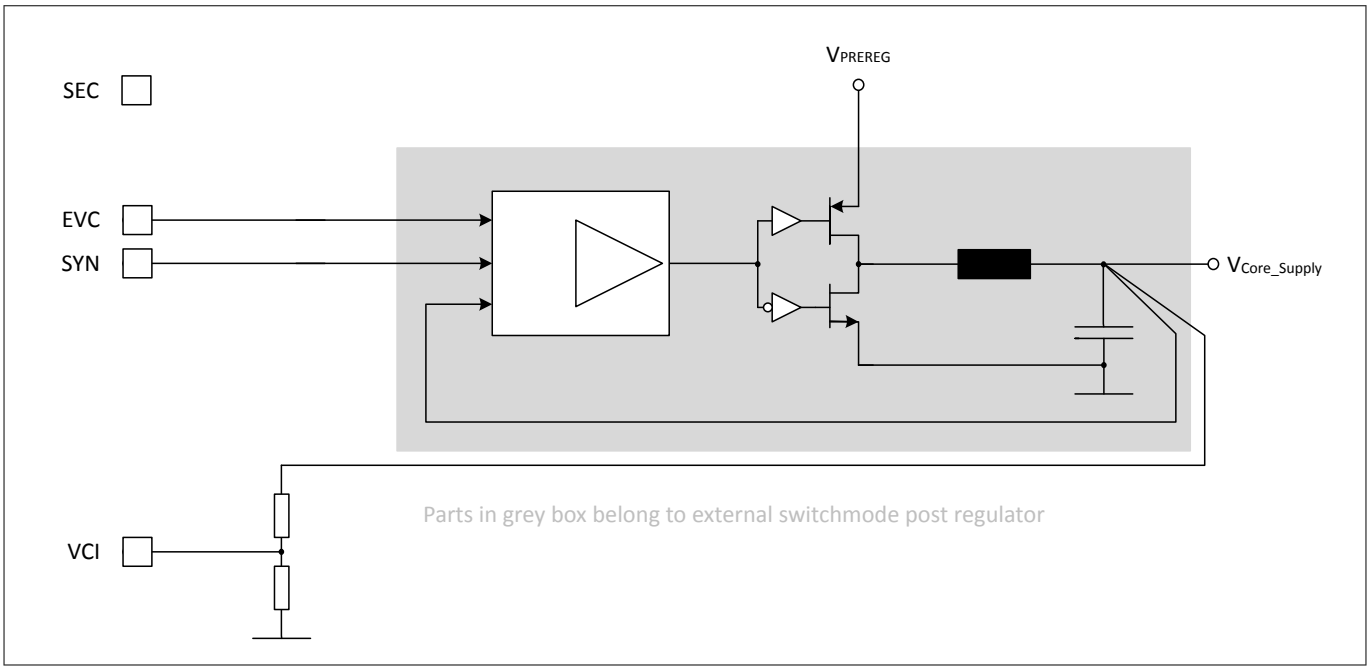


Figure 14 **External switch mode post regulator for core supply**

Table 14 **Electrical characteristics external post regulator**

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Enable output signal, pin EVC							
Enable output high level TLF35585QVS01	$V_{EVC, high}$	4.0	–	–	V	V_{QUC} = 5.0 V; I_{EVC} = -9 mA	P_7.6.0.1
Enable output high level TLF35585QVS01	$V_{EVC, high}$	4.6	–	–	V	V_{QUC} ≥ 4.7 V; I_{EVC} = -0.5 mA	P_7.6.0.2
Enable output low level TLF35585QVS01	$V_{EVC, low}$	–	–	0.7	V	V_{QUC} = 5.0 V; I_{EVC} = 7 mA	P_7.6.0.3
Enable output high level TLF35585QVS02	$V_{EVC, high}$	2.3	–	–	V	V_{QUC} = 3.3 V; I_{EVC} = -7 mA	P_7.6.0.4
Enable output high level TLF35585QVS02	$V_{EVC, high}$	3.0	–	–	V	V_{QUC} ≥ 3.1 V; I_{EVC} = -0.5 mA	P_7.6.0.5
Enable output low level TLF35585QVS02	$V_{EVC, low}$	–	–	0.7	V	V_{QUC} = 3.3 V; I_{EVC} = 5.5 mA	P_7.6.0.6
Enable output rise time	$t_{EVC, rise}$	–	–	25	ns	$C_{EVC, load}$ = 50 pF [28]	P_7.6.0.7

(table continues...)

[28] specified by design, not subject to production test

Table 14 (continued) Electrical characteristics external post regulator

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Enable output fall time	$t_{EVC, fall}$	–	–	25	ns	$C_{EVC, load}$ = 50 pF [28]	P_7.6.0.8
Synchronization output signal, pin SYN							
Synchronization output high level TLF35585QVS01	$V_{SYN, high}$	4.0	–	–	V	V_{QUC} = 5.0 V; I_{SYN} = -9 mA	P_7.6.0.9
Synchronization output high level TLF35585QVS01	$V_{SYN, high}$	4.6	–	–	V	V_{QUC} ≥ 4.7 V; I_{SYN} = -0.5 mA	P_7.6.0.10
Synchronization output low level TLF35585QVS01	$V_{SYN, low}$	–	–	0.7	V	V_{QUC} = 5.0 V; I_{SYN} = 7 mA	P_7.6.0.11
Synchronization output high level TLF35585QVS02	$V_{SYN, high}$	2.3	–	–	V	V_{QUC} = 3.3 V; I_{SYN} = -7 mA	P_7.6.0.12
Synchronization output high level TLF35585QVS02	$V_{SYN, high}$	3.0	–	–	V	V_{QUC} ≥ 3.1 V; I_{SYN} = -0.5 mA	P_7.6.0.13
Synchronization output low level TLF35585QVS02	$V_{SYN, low}$	–	–	0.7	V	V_{QUC} = 3.3 V; I_{SYN} = 5.5 mA	P_7.6.0.14
Synchronization output signal duty cycle	D_{SYN}	–	50	–	%	–	P_7.6.0.15
Synchronization output signal rise time	$t_{SYN, rise}$	–	–	25	ns	$C_{SYN ,load}$ = 50 pF [28]	P_7.6.0.16
Synchronization output signal fall time	$t_{SYN, fall}$	–	–	25	ns	$C_{SYN, load}$ = 50 pF [28]	P_7.6.0.17
Core voltage supply monitoring input, pin VCI							
Core voltage monitoring input pull-up current	I_{VCI}	–	100	130	nA	V_{VCI} = 0.8 V	P_7.6.0.18

28 specified by design, not subject to production test

6.7 Power sequencing

The TLF35585QV includes a power sequencing function to ensure a proper ramp-up of all output voltages. After the internal Power-On-Reset (POR) is released to move out of POWERDOWN and the voltage at pin VSx V_{VS} increased above $V_{PS,start}$, the standby regulator and the pre regulator(s) start to operate.

In case of one of the non microcontroller related voltages (QVR, QCO, QT1 or QT2) cannot be ramped up (e.g. short to GND), the power sequence is stopped, but the reset output is still released after the power on reset delay time t_{rd}. The microcontroller should check the status of the outputs by reading the SPI status register (**VMONSTAT**).

In case the microcontroller is sending a SPI request to enable or disable any non microcontroller related supply (QVR, QCO, QT1 or QT2) during the power sequencing, the sequence is stopped and the requested configuration is executed.

6.7.1 Power sequencing from POWERDOWN to INIT-state

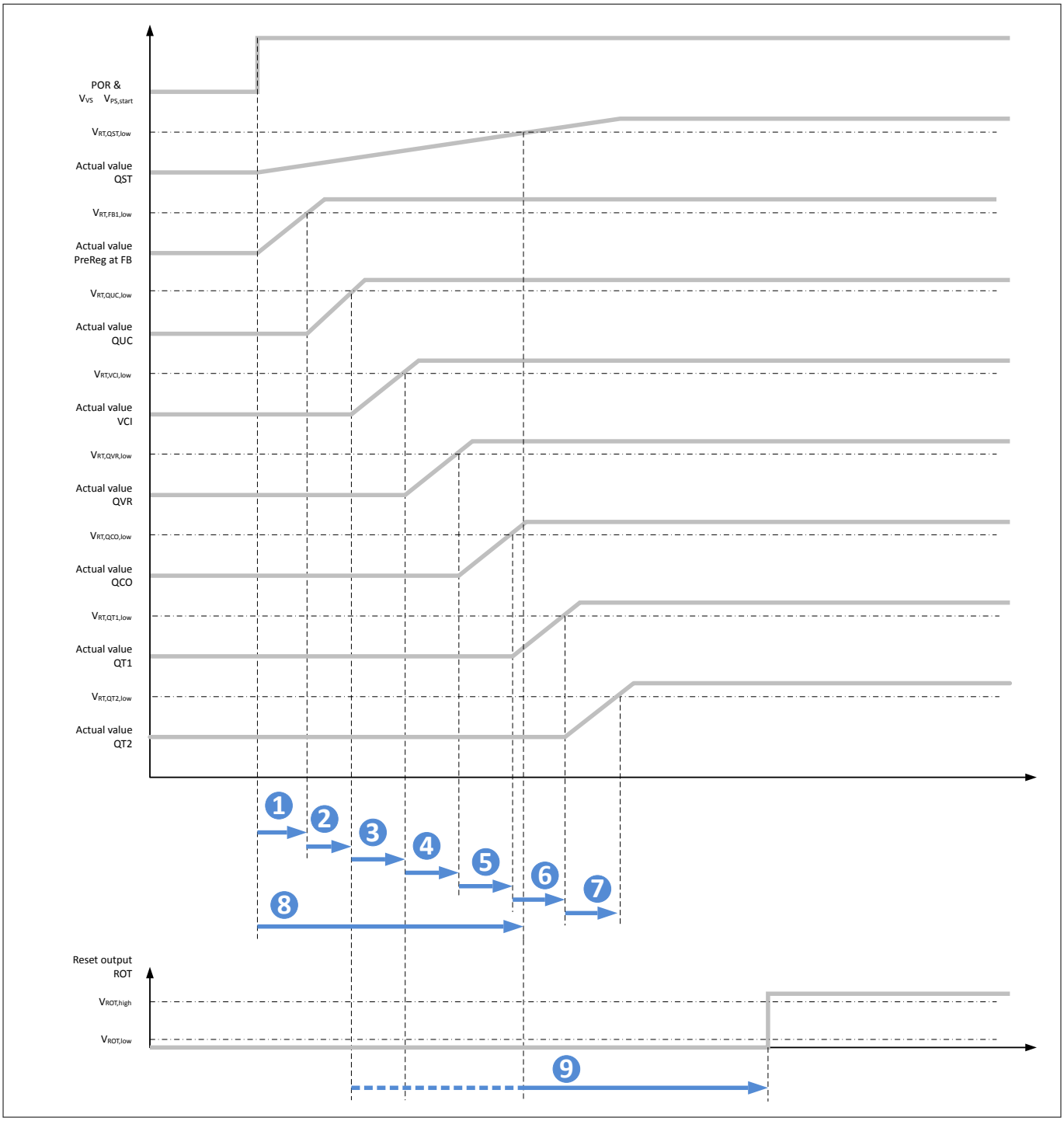


Figure 15 **Power sequencing POWERDOWN to INIT-state**

Description:

1. After POR is released to move out of POWERDOWN and V_{VS} is above $V_{PS,start}$, the standby supply (QST) and the pre regulator start to operate.
2. When V_{FB} is above the lower reset threshold $V_{RT,FB,low}$+$V_{RT,FB,UV\ hyst}$, the QUC starts to operate.
3. When V_{QUC} is above the lower reset threshold $V_{RT,QUC,low}$+$V_{RT,QUC,UV\ hyst}$, the external core supply is enabled via EVC pin, when selected. If the external core supply is not selected, the QVR starts to operate.

4. If the external core supply is selected and V_{VCI} is above the lower reset threshold $V_{RT,VCI,low}+V_{RT,VCI,UV\ hyst}$, the QVR starts to operate.
5. When V_{QVR} is above the lower reset threshold $V_{RT,QVR,low}+V_{RT,QVR,UV\ hyst}$, the QCO starts to operate.
6. When V_{QCO} is above the lower reset threshold $V_{RT,QCO,low}+V_{RT,QCO,UV\ hyst}$, the QT1 starts to operate.
7. When V_{QT1} is above the lower reset threshold $V_{RT,QT1,low}+V_{RT,QT1,UV\ hyst}$, the QT2 starts to operate.
8. This is the time from the enabling of the standby supply until its output V_{QST} is above the lower reset threshold $V_{RT,QST,low}$.
9. The reset delay time t_{RD} starts after QST, QUC and VCI (if external core supply selected by pin SEC) have reached their lower monitoring threshold $V_{RT,xxx,low}+V_{RT,xxx,UV\ hyst}$. The reset delay time is programmable via SPI. After the rest delay time is expired, the reset signal at pin ROT pin is released. The figure shows the possibilities of the t_{RD} starting time.

Once the ROT is high, the microcontroller can change the configuration of the selectable supplies, which might change the power sequencing accordingly.

6.7.2 Power sequencing STANDBY to INIT-state

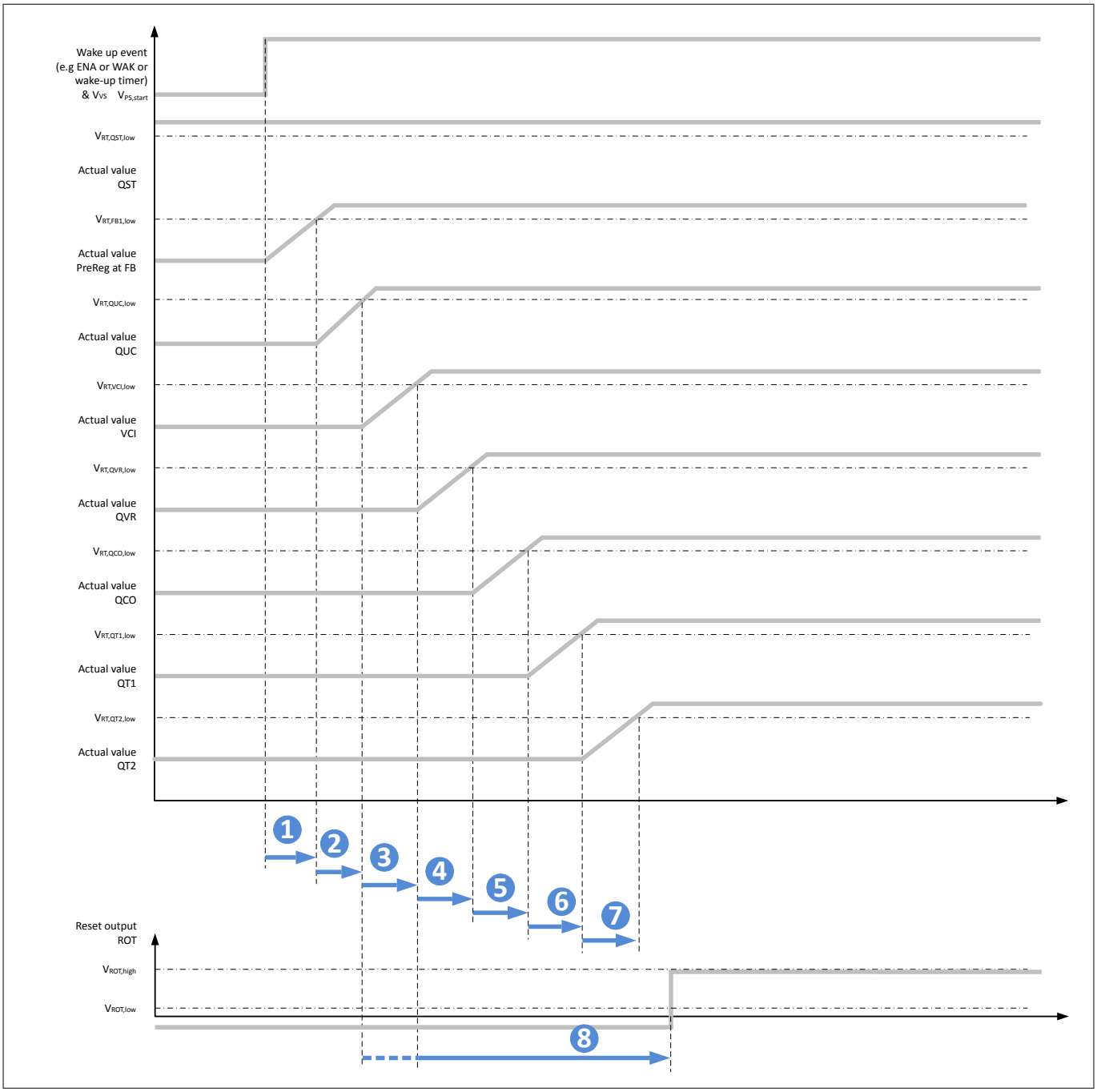


Figure 16 **Power sequencing STANDBY to INIT-state**

Description: Input voltage is present, device is in STANDBY-state, QST is active.

1. After a valid Wake-Signal or an expired wake-up timer the pre regulator starts to operate when V_{VS} is above $V_{PS,start}$.
2. When V_{FB} is above the lower reset threshold $V_{RT,FB,low}$+$V_{RT,FB,UV\ hyst}$, the QUC starts to operate.
3. When V_{QUC} is above the lower reset threshold $V_{RT,QUC,low}$+$V_{RT,QUC,UV\ hyst}$, the external core supply is enabled via EVC pin, when selected. If the external core supply is not selected, the QVR starts to operate.
4. If the external core supply is selected and V_{VCI} is above the lower reset threshold $V_{RT,VCI,low}$+$V_{RT,VCI,UV\ hyst}$, the QVR starts to operate.
5. When V_{QVR} is above the lower reset threshold $V_{RT,QVR,low}$+$V_{RT,QVR,UV\ hyst}$, the QCO starts to operate.

6. When V_{QCO} is above the lower reset threshold $V_{RT,QCO,low}$+$V_{RT,QCO,UV\ hyst}$, the QT1 starts to operate.
7. When V_{QT1} is above the lower reset threshold $V_{RT,QT1,low}$+$V_{RT,QT1,UV\ hyst}$, the QT2 starts to operate.
8. The reset delay time t_{RD} starts after QUC and VCI (if external core supply selected by pin SEC) have reached their lower monitoring threshold $V_{RT,xxx,low}$+$V_{RT,xxx,UV\ hyst}$. The reset delay time is programmable via SPI. After the rest delay time is expired, the reset signal at pin ROT pin is released. The figure shows the possibilities of the t_{RD} starting time.

6.7.3 Power sequencing SLEEP to WAKE-state

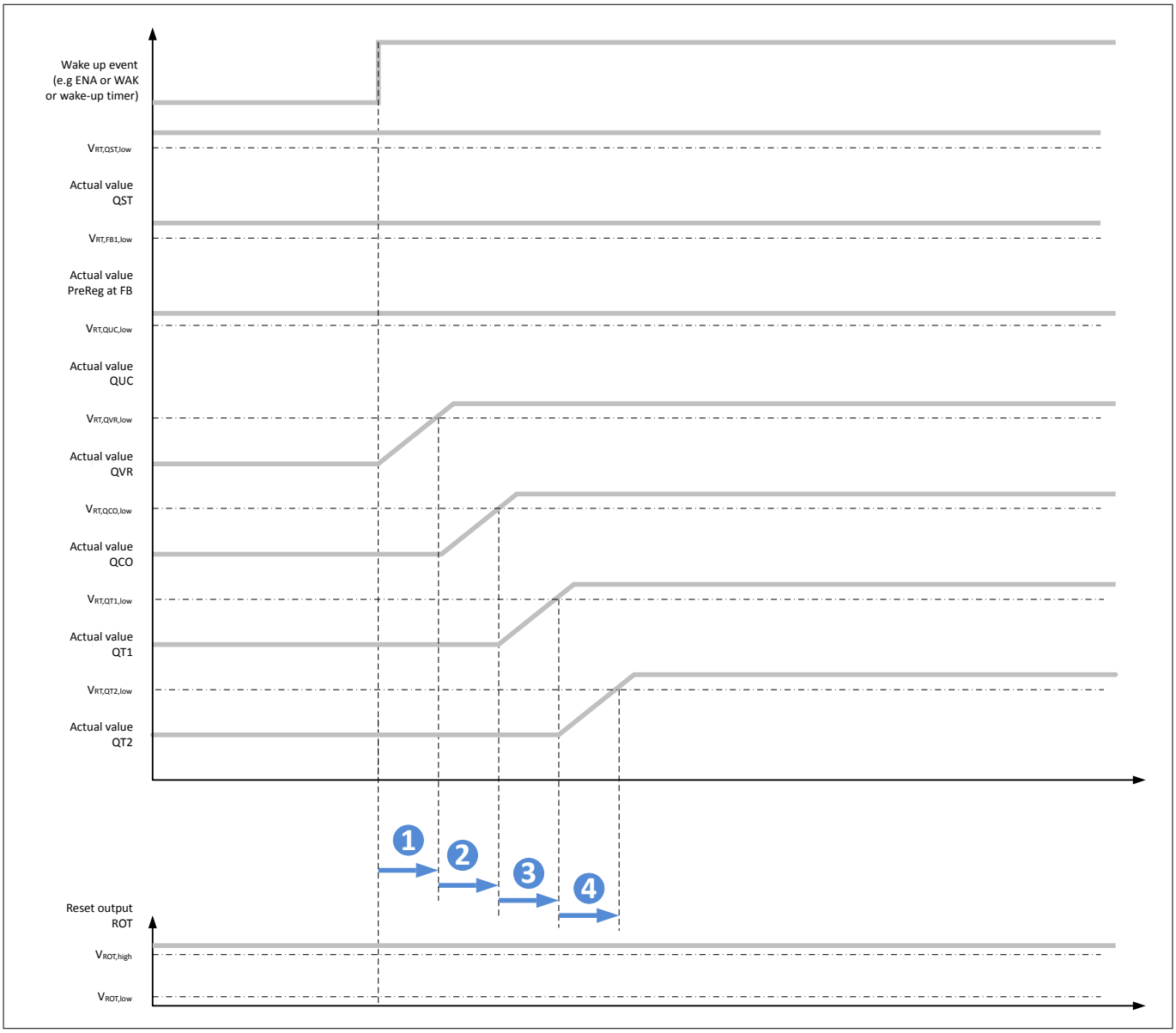


Figure 17 Power sequencing SLEEP to WAKE-state

Description: Input voltage is present, device is in SLEEP-state, all selectable supplies switched off in SLEEP-state, all selectable supplies were switched on in previous NORMAL-state:

1. After a valid Wake-Signal or an expired wake-up timer the voltage reference starts to operate.
2. When V_{QVR} is above the lower reset threshold $V_{RT,QVR,low}$+$V_{RT,QVR,UV\ hyst}$, the QCO starts to operate.
3. When V_{QCO} is above the lower reset threshold $V_{RT,QCO,low}$+$V_{RT,QCO,UV\ hyst}$, the QT1 starts to operate.
4. When V_{QT1} is above the lower reset threshold $V_{RT,QT1,low}$+$V_{RT,QT1,UV\ hyst}$, the QT2 starts to operate.

The reset output ROT is high in SLEEP-state and is kept high for WAKE-state.

In case a selectable LDO was switched off in the previous NORMAL-state, it is not enabled during the transition from SLEEP to WAKE, the power sequencing follows up with the next LDO. In case a LDO was enabled during SLEEP-state and was enabled in the previous NORMAL-state, it is kept enabled.

7 Monitoring function

7.1 Introduction monitoring function

The TLF35585QV includes an independent voltage monitoring function of all output voltages, including the optional external post regulator for MCU core supply, if in use.

The monitoring function consists of two comparators for each output voltage. One is for detecting overvoltage, the other is for detecting undervoltage. Both comparators get their reference value from an independent bandgap only used for the voltage monitoring block. This bandgap is independent from the voltage regulator bandgap. The bandgap provides the reference value for overvoltage detection (high voltage reset threshold $V_{RT,xxx,high}$) and for undervoltage detection (low voltage reset threshold $V_{RT,xxx,low}$). Under normal operation conditions the output voltage of the related regulator has to stay within the voltage window defined by the upper limit $V_{RT,xxx,high}$ and the lower limit $V_{RT,xxx,low}$.

There is a dedicated temperature sensor for the monitoring block. If the power stage temperature exceeds the temperature shutdown threshold, the device moves into FAILSAFE-state, the regulator is switched off and the event is stored in an SPI status register (**OTFAIL**). The off time due to temperature shut down is at least one second.

Characteristics

The behavior of the over and undervoltage comparators is as following:

- The upper limits $V_{RT,xxx,high}$ and the lower limits $V_{RT,xxx,low}$ are fixed for every regulator and cannot be programmed or varied by SPI command.
- An overvoltage is detected if the regulator output voltage is higher than the related overvoltage reset threshold $V_{RT,xxx,high}$ for more than the reset reaction time t_{RR}. An overvoltage higher than the related overvoltage reset threshold $V_{RT,xxx,high}$ which is present for shorter than the reset reaction time t_{RR} is regarded as a spike and is not detected.

  An undervoltage is detected if the regulator output voltage is lower than the related undervoltage reset threshold $V_{RT,xxx,low}$ for more than the reset reaction time t_{RR}. An undervoltage lower than the related undervoltage reset threshold $V_{RT,xxx,low}$ which is present for shorter than the reset reaction time t_{RR} is regarded as a spike and is not detected.
- The reset reaction time t_{RR} is not valid for the internal voltage supplies in case of under and overvoltage.
- The detection of an overvoltage shuts down the related regulator immediately to protect the loads from harm or destruction.

  This shut down may lead (depending on the affected regulator) to further action, please refer to chapter State machine for details.
- The detection of an undervoltage does not shut down the related regulator.
- The post regulators (including the optional external post regulator for MCU core supply) have a short to ground detection.

  If the detected undervoltage is present for more than the short to ground detection time t_{StG}, the related regulator is shut down to protect himself and the chip from over heating. This shut down may lead (depending on the affected regulator) to further action, please refer to chapter State machine for details. (It is mandatory that the external post regulator for MCU core supply has an enable or inhibit function).
- The over and undervoltage detection is active only if the related regulator is in use (including the external post regulator for MCU core supply) and switched on.

Indication of over and undervoltage

Depending on the related regulator the indication of over and undervoltage is different, either by reset signal or by interrupt indication:

- Every over and undervoltage detection is stored in the SPI status register (**MONSF0**, **MONSF1**, **MONSF2**).
- For MCU related output voltages (V_{QST} , V_{QUC} , V_{VCI}), over and undervoltage are indicated by the hardware reset pin ROT. In case of an over or undervoltage, pin ROT is pulled to low.
- In case of overvoltage or a detection of a short to ground at the external post regulator for MCU core supply, the pin EVC is pulled to low to shut down the regulator.
- For the pre regulator output (V_{FB}) and the voltage reference output (V_{QVR}) only overvoltage is indicated by the hardware reset pin ROT. In case of an overvoltage, pin ROT is pulled to low.
- For the pre regulator output and the voltage reference output, only undervoltage is indicated by an interrupt.
- For all not MCU related output voltages (V_{QCO} , V_{QT1} , V_{QT2}), over and undervoltage are indicated by an interrupt.
- For the internal supply voltages, over and undervoltage are indicated by the hardware reset pin ROT. In case of an over or undervoltage, pin ROT is pulled to low.

This introduction is an overview, for details please refer to the following sub chapters.

7.2 Shutdown function

A short to ground detection time t_{StG} at the pre regulator output is only active during the power sequence in INIT-state. If the output voltage of the pre regulator should not be within the specified limits within a certain time frame, the device moves into FAILSAFE-state. There is no reaction on a detected short to ground once the $V_{PREREG,BUCK}$ is in a valid range after crossing the first time its UV threshold (step 1 completed according to the power sequencing described in Chapter 6.7). If the output voltage of the pre regulator should be too low in other cases, the behavior of the device depends on the voltage monitoring of the post regulators.

The detection of an overvoltage at output voltages V_{QUC}, V_{VCI}, V_{QST}, V_{QVR} or V_{FB} shuts down all regulators to protect the loads from harm or destruction and moves the device to FAILSAFE.

The detection of an overvoltage at output voltages V_{QCO}, V_{QT1} and V_{QT2} shuts down the related regulator to protect the loads from harm or destruction and generate an interrupt event.

If the detected undervoltage at output voltages V_{QUC}, V_{VCI} or V_{QST} should be present for more than the short to ground detection time t_{StG}, all regulators are shut down to protect themselves and the chip from over heating and move the device to FAILSAFE.

If the detected undervoltage at output voltages V_{QVR}, V_{QCO}, V_{QT1} or V_{QT2} should be present for more than the short to ground detection time t_{StG}, the related regulator shuts down to protect himself and the chip from over heating and generate an interrupt event.

If the step up pre regulator operates in current limitation (based on $V_{RSH-RSL}$)for more than the short to ground detection time $t_{StG,boost}$, all regulators are shut down to protect the external boost components and the chip from over heating and move the device to FAILSAFE.

7.3 Reset function

The reset generator starts to operate as soon as the device moves out of POWERDOWN.

Distinguish between "Soft Reset" and "Hard Reset"

It is called a "Soft Reset" if pin ROT goes below $V_{ROT,low}$, but the pre and post regulator output voltages are not switched off.

It is called a "Hard Reset" if pin ROT goes below $V_{ROT,low}$ and the post regulator output voltages are switched off. The power sequencing is restarted after a delay of t_{SDT}.(Applicable to the second initialization timeout in a row)

Safe State Control trigger event

The Safe State Control function is connected to the monitoring block. In case of a Safe State Control trigger event is detected, pins Safe State Control outputs (SS1 and SS2) and ROT is pulled to ground. The Safe State Control trigger event is stored in a SPI register (respective bits in **SYSFAIL**, **INITERR**, **MONSF1**, **MONSF2**, **MONSF3** or **OTFAIL**). For trigger conditions of safe state signal SS1 please refer to chapter Safe State Control function.

Reset output pin

The reset output pin ROT is an open drain structure. As soon as a reset condition occurs, the ROT pin is pulled below $V_{ROT,low}$. An internal pull up current is pulling the output towards V_{QUC}.

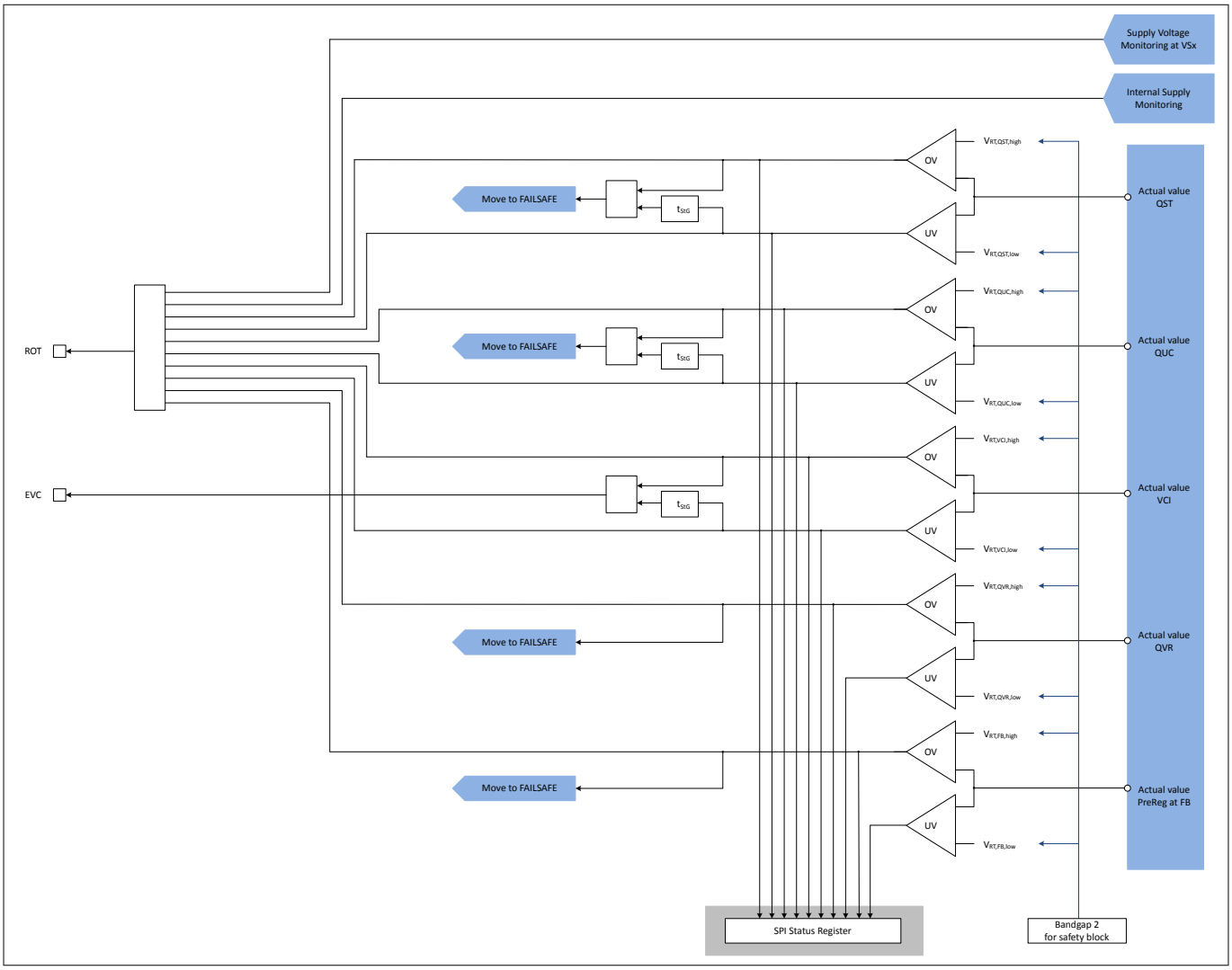


Figure 18 **Principle reset function**

Detailed description of the reset function (Figure 18):

The following regulators contribute to the reset function:

- Internal supply monitoring (not visible externally)
- The standby supply (QST): V_{QST}
- The microcontroller main supply (QUC): V_{QUC}
- The external post regulator for MCU core supply (VCI): V_{VCI}
- The voltage reference supply (QVR): V_{QVR} - only overvoltage, not undervoltage, not short to ground

- The pre regulator (FB): V_{FB} - only overvoltage, not undervoltage
- The step up pre regulator short to ground (overpower) detection

The actual values of these outputs are taken directly at the output pins and are monitored by two comparators for each regulator, one for overvoltage (named OV), the other for undervoltage (named UV). The reference values $V_{RT,xxx,high}$ and $V_{RT,xxx,low}$ are provided by an independent bandgap 2 only related to the monitoring functions.

The "Internal supply voltage regulator monitoring" of over and undervoltage events and IBIAS monitoring are contributing to trigger a reset. If one or both of the internal supply voltages should be out of their specified windows, the proper function of the device cannot be guaranteed any more. The IBIAS monitor fault is stored in a status bit (**ABIST_SELECT2** or BIASLOW). The fault of the internal supplies triggers a "Move to POWERDOWN" event (please refer to chapter State machine for details).

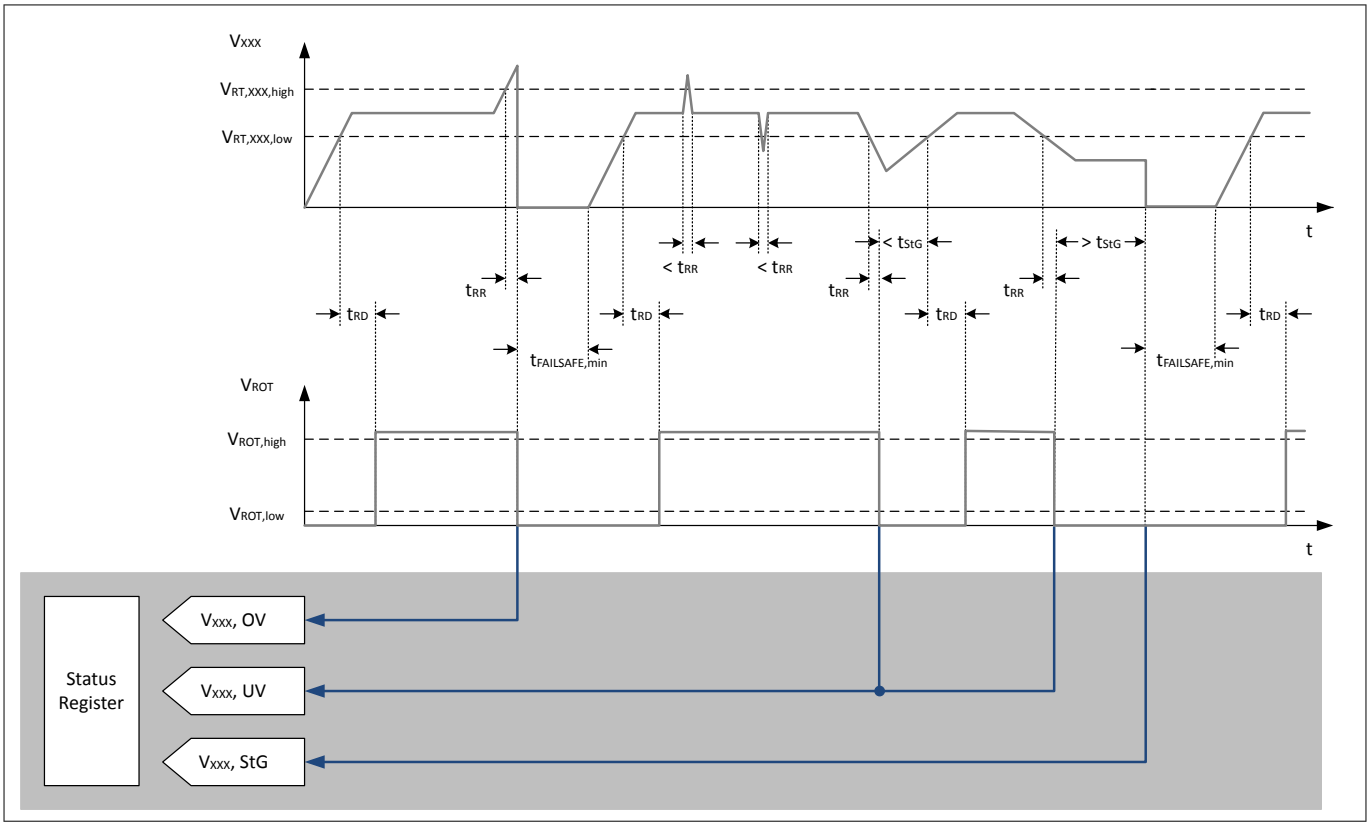


Figure 19 Timing diagram hardware reset signal ROT for output voltages

Description:

- V_{xxx} = Output voltage monitored by reset generator: V_{QUC} , V_{VCI},V_{QST}, V_{QVR} or V_{FB}
- $V_{RT,xxx,high}$= Overvoltage reset threshold: $V_{RT,QUC,high}$, $V_{RT,VCI,high}$, $V_{RT,QST,high}$, $V_{RT,QVR,high}$ or $V_{RT,FB,high}$
- $V_{RT,xxx,low}$= Undervoltage reset threshold: $V_{RT,VCI,low}$, $V_{RT,QUC,low}$ or $V_{RT,QST,low}$
- t_{RD} = Reset delay time, adjustable by SPI command
- t_{RR} = Reset reaction time, time between detecting overvoltage and pulling ROT to low
- < t_{RR} = Not detectable, because shorter than reset reaction time
- > t_{StG} = Short to ground detection time, time after an undervoltage is considered as a short to ground
- $t_{FAILSAFE,min}$ = System shutdown time (FAILSAFE), time between pulling ROT to low and restart of the device, for details please refer to chapter State machine
- V_{ROT} = Hardware reset signal, ROT
- $V_{ROT,high}$ = Hardware reset signal, high level
- $V_{ROT,low}$ = Hardware reset signal, low level

- $V_{xxx,OV}$ = Overvoltage detected for V_{xxx} and stored in SPI register (**MONSF1**)
- $V_{xxx,UV}$ = Undervoltage detected for V_{xxx} and stored in SPI register (**MONSF2**)
- $V_{xxx,StG}$ = Short to ground detected for V_{xxx} and stored in SPI register (**MONSF0**)
- Applies as well to bias current violations, supply overvoltage (**MONSF3**), temperature shutdown (**OTFAIL**) contributing to the reset function. Please refer to Figure 42 and Figure 49

7.4 Interrupt function

The interrupt generator starts to operate as soon as the internal POR is released, still the interrupt signal (pin INT) is only indicated when reset is released (pin ROT high).

The voltage monitoring function supervises the values of the non MCU related post regulator output voltages V_{QCO}, V_{QT1} and V_{QT2}, the pre regulator output voltage V_{FB} (undervoltage only) and the voltage reference output V_{QVR} (undervoltage and short to ground only). The result is written in a SPI status register (**IF** and **MONSF0**, **MONSF1** or **MONSF2**) and indicated via interrupt (pin INT). The connection of all these monitoring signals is a logic OR.

The interrupt pin INT does not only indicate the result of the voltage monitoring, but also interrupts due to other events in the device.

Interrupt output pin

The interrupt output pin INT is a push pull structure. An interrupt is indicated by pulling the INT pin to ground.

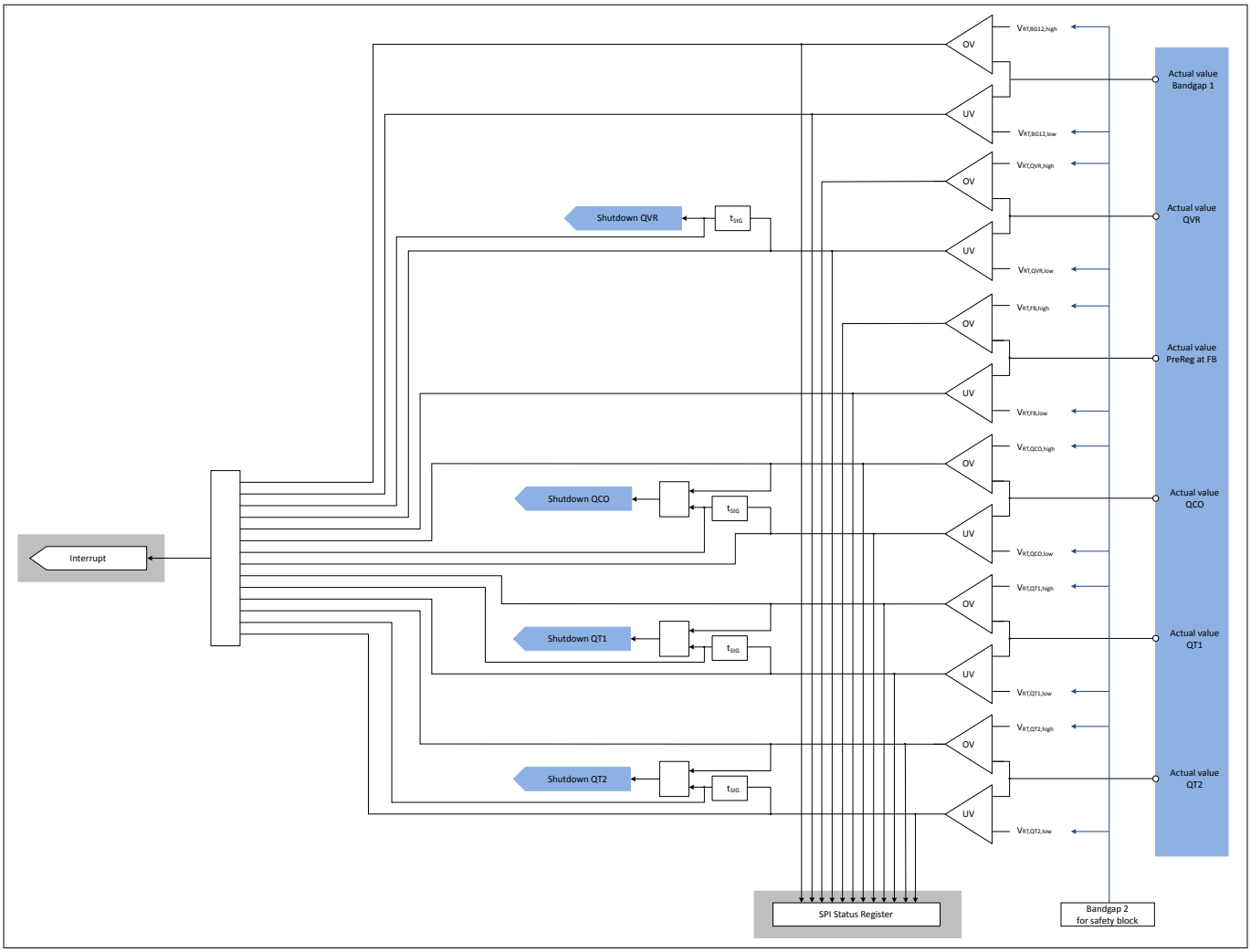


Figure 20 Principle indication of voltage monitoring via interrupt

Detailed description of the voltage monitoring via interrupt function (Figure 20)

The following regulators contribute to the voltage monitoring via interrupt function:

- The pre regulator (FB): V_{FB} , just undervoltage
- The voltage reference supply (QVR): V_{QVR} , just undervoltage and short to GND

- The communication supply (QCO): V_{QCO}
- The tracker 1 for supplying sensors (QT1): V_{QT1}
- The tracker 2 for supplying sensors (QT2): V_{QT2}

The actual values of these outputs are taken directly at the output pins and monitored by two comparators for each regulator, one for overvoltage (named OV), the other for undervoltage (named UV). The reference values $V_{RT,xxx,high}$ and $V_{RT,xxx,low}$ are provided by an independent bandgap 2 only related to the monitoring functions.

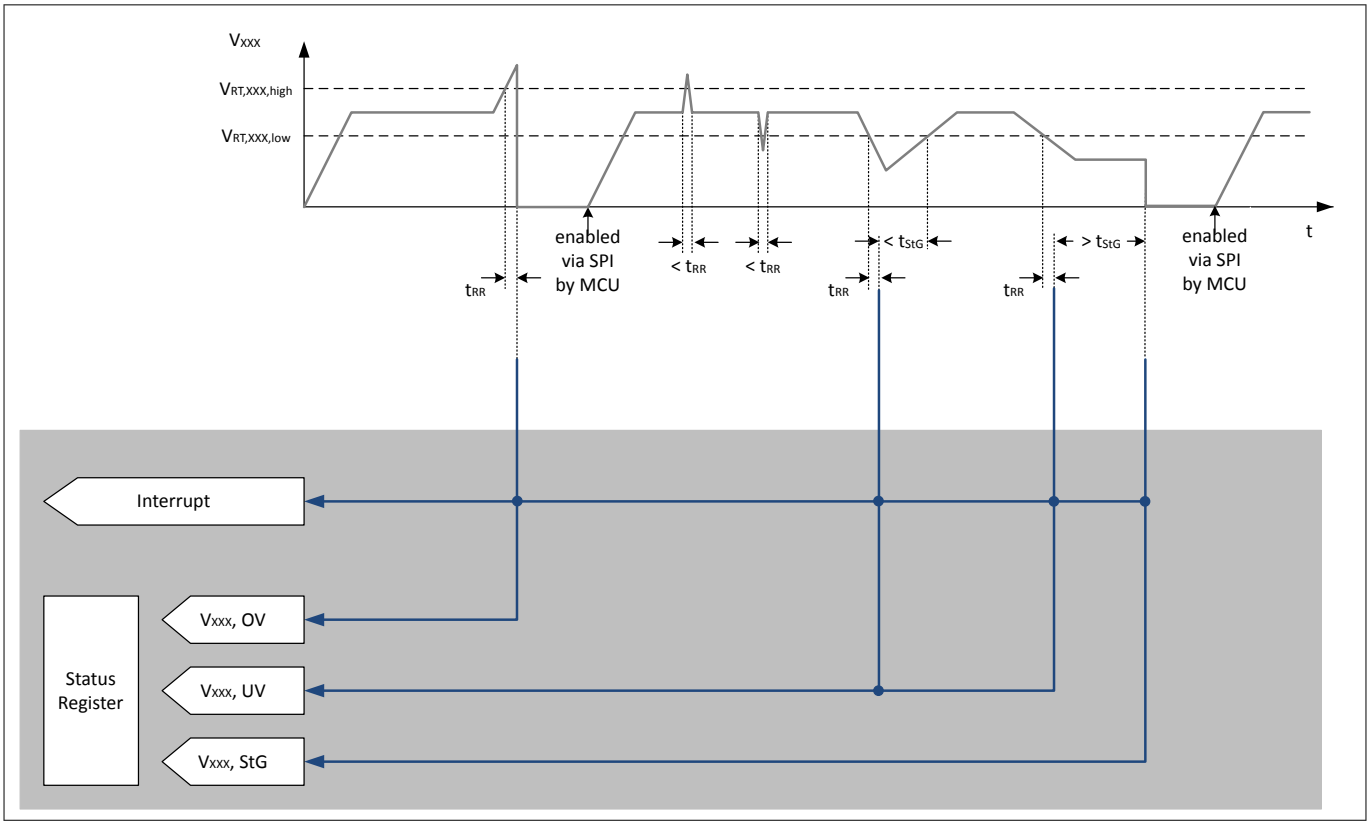


Figure 21 Timing diagram interrupt indication for output voltages

Description:

- V_{xxx} = Output voltage monitored by interrupt indication: V_{FB} , V_{QVR}, V_{QCO} , V_{QT1} or V_{QT2}
- $V_{RT,xxx,high}$= Overvoltage interrupt indication: $V_{RT,QCO,high}$, $V_{RT,QT1,high}$ or $V_{RT,QT2,high}$
- $V_{RT,xxx,low}$= Undervoltage interrupt indication: $V_{RT,FB,low}$, $V_{RT,QVR,low}$, $V_{RT,QCO,low}$, $V_{RT,QT1,low}$ or $V_{RT,QT2,low}$
- t_{RR} = Reset reaction time, time between detecting overvoltage and an interrupt is generated
- < t_{RR} = Not detectable, because shorter than reset reaction time
- > t_{StG} = Short to ground detection time, time after an undervoltage is considered as a short to ground
- $V_{xxx,OV}$ = Overvoltage detected for V_{xxx} and stored in SPI register (**MONSF1**)
- $V_{xxx,UV}$ = Undervoltage detected for V_{xxx} and stored in SPI register (**MONSF2**)
- $V_{xxx,StG}$ = Short to ground detected for V_{xxx} and stored in SPI register (**MONSF0**)
- Applies as well to detection of bandgap 1 to 2 variations (**MONSF3**), over load and temperature events (**OTWRNSF**, **OTFAIL**) contributing to the interrupt function. Please refer to Figure 41

7.5 Electrical characteristics voltage monitoring and reset function

Table 15 Electrical characteristics voltage monitoring and reset function

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Timing							
Reset cycle time	t_{CYCLE}	9.4	10	10.65	µs	–	P_8.5.1
Reset delay time, default value	t_{RD}	–	1000	–	t_{CYCLE}	–	P_8.5.2
Reset delay time, adjustable range by SPI command	t_{RD}	20	–	1500	t_{CYCLE}	[29]	P_8.5.3
Monitoring reaction time	t_{RR}	8	–	20	µs	–	P_8.5.4
Monitoring reaction time, standby regulator	$t_{RR, STBY}$	8	–	40	µs	–	P_8.5.5
Short to ground detection time	t_{StG}	2.7	3	3.3	ms		P_8.5.6
Step-down regulator short to ground detection time	$t_{StG,HF}$	2.7	3	3.3	ms	step down pre regulator 2.2 MHz switching frequency	P_8.5.7
Step-down regulator short to ground detection time	$t_{StG,LF}$	5.4	6	6.6	ms	step down pre regulator 400 kHz switching frequency	P_8.5.8
VCI short to ground detection time	$t_{StG,VCI}$	5.4	6	6.6	ms	–	P_8.5.9
Boost short to ground detection time	$t_{StG,boost}$	5.4	6	6.6	ms	–	P_8.5.10
System shutdown time	t_{SDT}	9	–	20	ms	––	P_8.5.11
Monitoring thresholds standby regulator, pin QST							
Overvoltage monitoring threshold TLF35585QVS01	$V_{RT,QST,high}$	5.25	5.35	5.45	V	V_{QST} increasing	P_8.5.10
Overvoltage monitoring hysteresis TLF35585QVS01	$V_{RT,QST,OV\ hyst}$	30	–	90	mV	–	P_8.5.11
Undervoltage monitoring threshold TLF35585QVS01	$V_{RT,QST,low}$	4.25	4.35	4.45	V	V_{QST} decreasing	P_8.5.12
Undervoltage monitoring hysteresis TLF35585QVS01	$V_{RT,QST,UV\ hyst}$	30	–	70	mV	–	P_8.5.13

(table continues...)

29 Due to internal delays the reset delay time can be enlarged by max 50 µs. Please consider the transition time into INIT-state $t_{r,INIT}$ specified in Table 25 prior to the power sequencing started by entering INIT-state.

Table 15 (continued) Electrical characteristics voltage monitoring and reset function

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Overvoltage monitoring threshold TLF35585QVS02	$V_{RT,QST,high}$	3.46	3.53	3.6	V	V_{QST} increasing	P_8.5.14
Overvoltage monitoring hysteresis TLF35585QVS02	$V_{RT,QST,OV\ hyst}$	20	–	55	mV	–	P_8.5.15
Undervoltage monitoring threshold TLF35585QVS02	$V_{RT,QST,low}$	2.97	3.04	3.1	V	V_{QST} decreasing	P_8.5.16
Undervoltage monitoring hysteresis TLF35585QVS02	$V_{RT,QST,UV\ hyst}$	20	–	50	mV	–	P_8.5.17
Monitoring thresholds microcontroller supply, pin QUC							
Overvoltage monitoring threshold TLF35585QVS01	$V_{RT,QUC,high}$	5.25	5.35	5.45	V	V_{QUC} increasing	P_8.5.18
Overvoltage monitoring hysteresis TLF35585QVS01	$V_{RT,QUC,OV\ hyst}$	30	–	90	mV	[30]	P_8.5.19
Undervoltage monitoring threshold TLF35585QVS01	$V_{RT,QUC,low}$	4.5	4.6	4.7	V	V_{QUC} decreasing	P_8.5.20
Undervoltage monitoring hysteresis TLF35585QVS01	$V_{RT,QUC,UV\ hyst}$	30	–	70	mV	[30]	P_8.5.21
Overvoltage monitoring threshold TLF35585QVS02	$V_{RT,QUC,high}$	3.46	3.53	3.6	V	V_{QUC} increasing	P_8.5.22
Overvoltage monitoring hysteresis TLF35585QVS02	$V_{RT,QUC,OV\ hyst}$	20	–	55	mV	[30]	P_8.5.23
Undervoltage monitoring threshold TLF35585QVS02	$V_{RT,QUC,low}$	2.97	3.04	3.1	V	V_{QUC} decreasing	P_8.5.24
Undervoltage monitoring hysteresis TLF35585QVS02	$V_{RT,QUC,UV\ hyst}$	20	–	50	mV	[30]	P_8.5.25
Monitoring thresholds external core supply, pin VCI							
Overvoltage monitoring threshold	$V_{RT,VCI,high}$	848	864	880	mV	V_{VCI} increasing	P_8.5.26
Overvoltage monitoring hysteresis	$V_{RT,VCI,OV\ hyst}$	5	–	15	mV	[30]	P_8.5.27
Undervoltage monitoring threshold	$V_{RT,VCI,low}$	720	736	752	mV	V_{VCI} decreasing	P_8.5.28
Undervoltage monitoring hysteresis	$V_{RT,VCI,UV\ hyst}$	5	–	15	mV	[30]	P_8.5.29

(table continues...)

30 Specified by design, not subject to production test

Table 15 (continued) Electrical characteristics voltage monitoring and reset function

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Monitoring thresholds pre regulator, pins FBx							
Overvoltage monitoring threshold	$V_{RT,FB,high}$	6.46	6.58	6.7	V	V_{FB} increasing	P_8.5.30
Overvoltage monitoring hysteresis	$V_{RT,FB,OV\ hyst}$	40	–	120	mV	–	P_8.5.31
Undervoltage monitoring threshold	$V_{RT,FB,low}$	5.0	5.1	5.2	V	V_{FB} decreasing	P_8.5.32
Undervoltage monitoring hysteresis	$V_{RT,FB,UV\ hyst}$	30	–	90	mV	–	P_8.5.33
Monitoring thresholds communication supply, pin QCO							
Overvoltage monitoring threshold	$V_{RT,QCO,high}$	5.15	5.25	5.35	V	V_{QCO} increasing	P_8.5.34
Overvoltage monitoring hysteresis	$V_{RT,QCO,OV\ hyst}$	20	–	50	mV	–	P_8.5.35
Undervoltage monitoring threshold	$V_{RT,QCO,low}$	4.65	4.75	4.85	V	V_{QCO} decreasing	P_8.5.36
Undervoltage monitoring hysteresis	$V_{RT,QCO,UV\ hyst}$	20	–	50	mV	–	P_8.5.37
Monitoring thresholds voltage reference supply, pin QVR							
Overvoltage monitoring threshold	$V_{RT,QVR,high}$	5.10	5.20	5.30	V	V_{QVR} increasing	P_8.5.38
Overvoltage monitoring hysteresis	$V_{RT,QVR,OV\ hyst}$	20	–	50	mV	–	P_8.5.39
Undervoltage monitoring threshold	$V_{RT,QVR,low}$	4.70	4.80	4.90	V	V_{QVR} decreasing	P_8.5.40
Undervoltage monitoring hysteresis	$V_{RT,QVR,UV\ hyst}$	20	–	50	mV	–	P_8.5.41
Monitoring thresholds tracker 1, pin QT1							
Overvoltage monitoring threshold	$V_{RT,QT1,high}$	5.30	5.40	5.50	V	V_{QT1} increasing	P_8.5.42
Overvoltage monitoring hysteresis	$V_{RT,QT1,OV\ hyst}$	20	–	50	mV	–	P_8.5.43
Undervoltage monitoring threshold	$V_{RT,QT1,low}$	4.50	4.60	4.70	V	V_{QT1} decreasing	P_8.5.44
Undervoltage monitoring hysteresis	$V_{RT,QT1,UV\ hyst}$	20	–	50	mV	–	P_8.5.45

(table continues...)

Table 15 (continued) Electrical characteristics voltage monitoring and reset function

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Monitoring thresholds tracker 2, pin QT2							
Overvoltage monitoring threshold	$V_{RT,QT2,high}$	5.30	5.40	5.50	V	V_{QT2} increasing	P_8.5.46
Overvoltage monitoring hysteresis	$V_{RT,QT2,OV\ hyst}$	20	–	50	mV	–	P_8.5.47
Undervoltage monitoring threshold	$V_{RT,QT2,low}$	4.50	4.60	4.70	V	V_{QT2} decreasing	P_8.5.48
Undervoltage monitoring hysteresis	$V_{RT,QT2,UV\ hyst}$	20	–	50	mV	–	P_8.5.49
Input voltage VSx monitoring, pin VSx							
Input overvoltage monitoring threshold	$V_{VS,OV}$	40.5	42	43.5	V		P_8.5.50
Overtemperature protection of monitoring							
Overtemperature shutdown threshold	$T_{j,OT,\ shutdown}$	176	190	200	°C	T_j increasing [30]	P_8.5.51
Overtemperature shutdown hysteresis	$T_{j,OT,\ hyst}$	–	10	–	°C	[30]	P_8.5.52
Reset output ROT							
Reset output, pull-up current	$I_{ROT,\ pu}$	-175	-110	-15	µA	V_{ROT} <= 2.0 V	P_8.5.53
Reset output, low level TLF35585QVS01	$V_{ROT,\ low}$	–	–	0.7	V	1 V ≤ V_{QUC} ≤ 5.1 V; I_{ROT} = 7 mA	P_8.5.54
Reset output, low level TLF35585QVS01	$V_{ROT,\ low}$	–	–	0.4	V	1 V ≤ V_{QUC} ≤ 5.1 V; I_{ROT} = 3.5 mA	P_8.5.55
Reset output, low level TLF35585QVS02	$V_{ROT,\ low}$	–	–	0.7	V	1 V ≤ V_{QUC} ≤ 3.37 V; I_{ROT} = 5.5 mA	P_8.5.56
Reset output, low level TLF35585QVS02	$V_{ROT,\ low}$	–	–	0.4	V	1 V ≤ V_{QUC} ≤ 3.37 V; I_{ROT} = 3 mA	P_8.5.57
Reset output fall time	$t_{ROT,\ fall}$	–	–	25	ns	[30] $C_{ROT,load}$ = 50 pF	P_8.5.58
Interrupt output INT							
Interrupt output, high level TLF35585QVS01	$V_{INT,\ high}$	4.0	–	–	V	V_{QUC} = 5.0 V; I_{INT} = -9 mA	P_8.5.59

(table continues...)

30 Specified by design, not subject to production test

Table 15 (continued) Electrical characteristics voltage monitoring and reset function

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Interrupt output, low level TLF35585QVS01	$V_{INT, low}$	–	–	0.7	V	V_{QUC} = 5.0 V; I_{INT} = 7 mA	P_8.5.60
Interrupt output, high level TLF35585QVS02	$V_{INT, high}$	2.3	–	–	V	V_{QUC} = 3.3 V; I_{INT} = -7 mA	P_8.5.61
Interrupt output, low level TLF35585QVS02	$V_{INT, low}$	–	–	0.7	V	V_{QUC} = 3.3 V; I_{INT} = 5.5 mA	P_8.5.62
Interrupt output rise time	$t_{INT, rise}$	–	–	25	ns	[30] $C_{INT,load}$ = 50 pF	P_8.5.63
Interrupt output fall time	$t_{INT, fall}$	–	–	25	ns	[30] $C_{INT,load}$ = 50 pF	P_8.5.64

30 Specified by design, not subject to production test

8 Standby supply and internal supplies

8.1 Standby supply QST

8.1.1 Functional description standby supply

The standby supply QST is independent from the pre regulator stage and the other post regulators. It might be switched ON or OFF in all states (for details please refer to chapter State machine). The linear low drop regulator QST offers a precise 3.3 V (or 5.0 V, equal to QUC) output voltage for standby supply.

The QST keeps its configuration by leaving the STANDBY-state according to its previous configuration. For STANDBY-state, the status of QST (ON or OFF) has to be defined in previous states.

The regulator is supplied from pin VST. Depending on the needs of the application pin VST might be connected directly to battery voltage (protected by reverse polarity diode) or to the output of the step up pre regulator (pin VSx). The output voltage V_{QST} (at pin QST) is controlled by the error amplifier. The actual value is compared to a reference voltage derived from bandgap 1 for regulators or optionally based on voltage at pin QUC with an offset. The stability of the control loop is depending on the load current, the characteristics of the output capacitor and the chip temperature. To ensure stable operation the output capacitor should be chosen according the specified requirements (capacitance value and electrical series resistance ESR) in Table 16.

Protection circuitry is installed to prevent the regulator and the application from damage:

- To protect the pass element from overstress the current limitation limits the output current to the maximum specified limit. Current sensing is done via a current mirror, no sense resistor is used. In case the maximum current should occur, it is limited., thus the output voltage decreases. The regulator is protected against short circuit to ground.
- The output voltage is monitored by the voltage monitoring.

  In case of overvoltage at pin QST, the QST is switched off and the device moves into FAILSAFE-state. The event is stored in an SPI status register (**MONSF1**).

  In case of undervoltage at pin QST, the device moves into INIT-state, pin ROT is pulled low and the event is stored in an SPI status register (**MONSF2**). The regulator is not switched off in case of output undervoltage, which is shorter than the short to ground detection time t_{StG}. If the undervoltage should be present for more than t_{StG}, the device moved into FAILSAFE-state. This event is stored in an SPI status register as well (**MONSF0**).
- There is no dedicated temperature sensor for this regulator. The temperature is sensed on the chip by other temperature sensors located at QUC and step down pre regulator. In case of the chip temperature exceeds the pre warning threshold, an interrupt indicates this event and it is stored in an SPI status register (**OTFAIL**). If the chip temperature exceeds the temperature shutdown threshold, the post regulator is switched off. The temperature switch off time is at least one second.
- An overload at QST (overcurrent detected for more than 1 ms) is indicated by interrupt, except if the device is in STANDBY-state and the event is stored in SPI status register (**OTWRNSF**).

The regulator QST may be configured to be ON or OFF in every state, except FAILSAFE. The selection for STANDBY-state shall be done by SPI command before entering this state.

For further details please refer to Chapter 10 State machine.

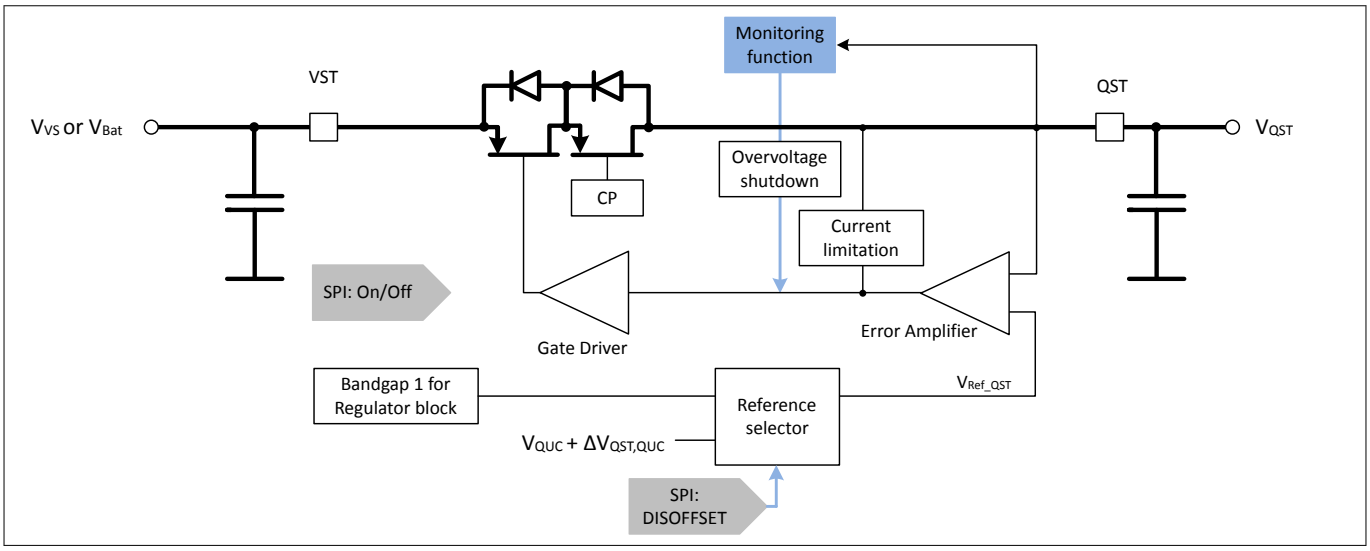


Figure 22 **Low drop linear regulator for standby supply QST**

8.1.2 Electrical characteristics standby supply

Table 16 **Electrical characteristics standby supply**

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Standby supply QST							
Output voltage TLF35585QVS01	V_{QST}	4.9	5.0	5.1	V	when QUC is off or when DISOFFSET is set to 0b0; 0 mA ≤ I_{QST} ≤ 10 mA	P_9.1.1
Output voltage offset QST to QUC TLF35585QVS01	$\Delta V_{QST,QUC}$	-200	-125	-75	mV	when QST and QUC are active with DISOFFSET being set to 0b1; 0 mA ≤ I_{QST} ≤ 10 mA	P_9.1.2
Output voltage TLF35585QVS02	V_{QST}	3.23	3.30	3.37	V	when QUC is off or when DISOFFSET is set to 0b0; 0 mA ≤ I_{QST} ≤ 10 mA	P_9.1.3
Output voltage offset QST to QUC TLF35585QVS02	$\Delta V_{QST,QUC}$	-145	-90	-50	mV	when QST and QUC are active with DISOFFSET being set to 0b1; 0 mA ≤ I_{QST} ≤ 10 mA	P_9.1.4
Output current limitation	$I_{QST,max}$	25	–	45	mA	–	P_9.1.5

(table continues...)

Table 16 (continued) Electrical characteristics standby supply

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Drop voltage	$V_{dr,QST}$	–	–	400	mV	Limited to $V_{PD,lo}$ at pin VST	P_9.1.6
Load regulation TLF35585QVS01	$\Delta V_{QST,load}$	–	25	40	mV	I_{QST} = 100 µA to 10 mA	P_9.1.7
Load regulation TLF35585QVS02	$\Delta V_{QST,load}$	–	20	40	mV	I_{QST} = 100 µA to 10 mA	P_9.1.8
Line regulation TLF35585QVS01	$\Delta V_{QST,line}$	–	0.1	0.5	mV/V	–	P_9.1.9
Line regulation TLF35585QVS02	$\Delta V_{QST,line}$	–	0.1	0.5	mV/V	–	P_9.1.10
Power supply ripple rejection	$PSRR_{QST}$	40	–	–	dB	[31] f_{ripple} = 100 kHz ESRC_{QST} ≤ 100 mΩ	P_9.1.11
Output capacitor	C_{QST}	0.47	–	10	µF	[31]	P_9.1.12
Output capacitor, ESR	ESR C_{QST}	0	–	200	mΩ	[31]	P_9.1.13
Softstart time	$t_{SS,QST}$	130	200	700	µs	[31] C_{QST} ≤ 3 µF; V_{QST} rising from 5 % to 95 % of $V_{QST,nominal}$	P_9.1.14

31 Specified by design, not subject to production test

8.1.3 Typical performance characteristics standby supply

QST output voltage V_{QST} versus junction temperature T_j (TLF35585QVS01)

QST output voltage V_{QST} versus junction temperature T_j (TLF35585QVS02)

QST output voltage V_{QST} versus supply voltage V_{VS} (TLF35585QVS01)

QST output voltage V_{QST} versus supply voltage V_{VS} (TLF35585QVS02)

QST output voltage V_{QST} versus load current I_{QST} (TLF35585QVS01)

QST output voltage V_{QST} versus load current I_{QST} (TLF35585QVS02)

QST dropout voltage $V_{dr,QST}$ versus load current I_{QST} (TLF35585QVS01)

QST dropout voltage $V_{dr,QST}$ versus load current I_{QST} (TLF35585QVS02)

QST dynamic load response (0 mA to 5 mA) TLF35585QVS01 ($V_{QST,nom}$ = 5.0 V)

QST dynamic load response (0 mA to 5 mA) TLF35585QVS02 ($V_{QST,nom}$ = 3.3 V)

8.2 Internal supplies

The TLF35585QV includes internal voltage supplies and bias currents to operate all regulators, monitoring and logic functions. These internal supplies are monitored internally to ensure proper functionality of the functional blocks the TLF35585QV provides. The device reacts on internal failure conditions as described in the State machine, Monitoring function, Interrupt generation and Safe State Control function. The internal regulators do not require external components (i.e capacitors). The internal voltages are not visible at any pin.

9 Wake-up timer

9.1 Description of wake-up timer

The wake-up timer is a function to wake up the TLF35585QV.

The wake-up timer value may be set by SPI in INIT, NORMAL and WAKE-state. The value is stored in the 24 bit wide wake-up timer register (**WKTIMCFG0**, **WKTIMCFG1**, **WKTIMCFG2**).The wake-up timer is implemented as a 24 bit counter which is clocked by a 100 kHz or 100 Hz clock (time-base). The time-base may be selected via SPI (WKTIMCYC). For the chosen time-base of 100 kHz the timer resolution is 10 µs and a wake-up time between 10 µs to 168 s can be configured via SPI.[32] For the chosen time-base of 100 Hz the timer resolution is 10 ms and a wake-up time between 10 ms to 1.9 days can be configured via SPI. An additional pre-scaler of 100 can be activate via SPI (WKTIMPRESC) to further increase the timebase allowing to increase the wake-up time up to 190 days.

When entering STANDBY or SLEEP state, the counter is loaded with the value of the wake-up timer register and starts decrementing. At underflow, the timer wakes-up the device from either SLEEP or STANDBY-state. When leaving SLEEP-state, an interrupt is generated.

In case of a wake-up trigger event independent from the wake-up timer, the wake-up timer is stopped and the remaining timer value can be read back via SPI in order to evaluate the theoretical time left and the corresponding time elapsed.

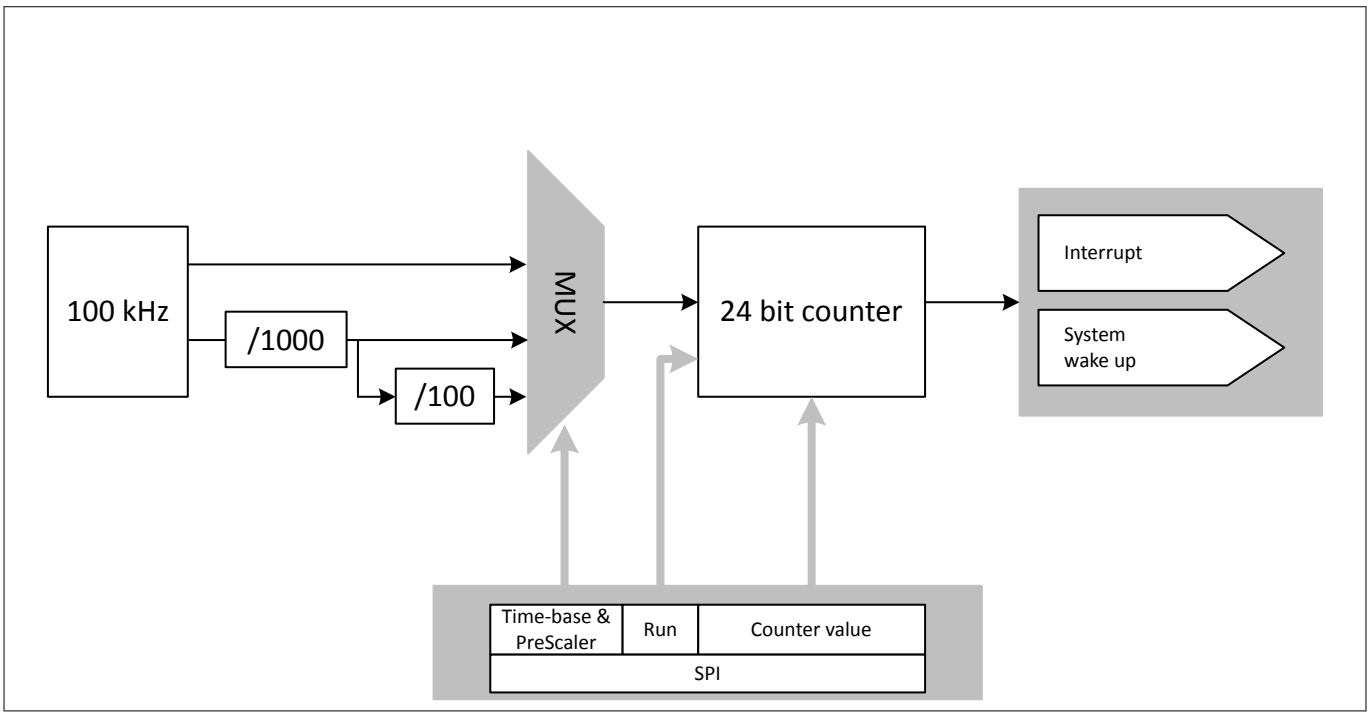


Figure 23 **Wake-up timer principle**

[32] An additional activation delay time for the start of the wake-up timer of max. 40 µs has to be considered after entering SLEEP or STANDBY-state.

9.2 Electrical characteristics wake-up timer

Table 17 Electrical characteristics wake-up timer

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Wake-up timer							
Time base, resolution	$t_{WakeUpTimer}$	9.5	10	10.5	µs	[33] WKTIMCYC = 0 & WKTIMPRESC = 0	P_10.2.1
Time base, resolution	$t_{WakeUpTimer}$	9.5	10	10.5	ms	WKTIMCYC = 1 & WKTIMPRESC = 0	P_10.2.2
Time base, resolution	$t_{WakeUpTimer}$	0.95	1	1.05	s	WKTIMCYC = 1 & WKTIMPRESC = 1	P_10.2.3
Counter	C	-	24	-	bit	[34]	P_10.2.4

33 Due to internal delays the wake-up time can be enlarged by max 50µs.
34 Specified by design, not subject to production test

10 State machine

10.1 Introduction state machine

The state machine describes the different states of operation, the device may get into. The following figure shows the state machine flow diagram, for detailed information please refer to following pages.

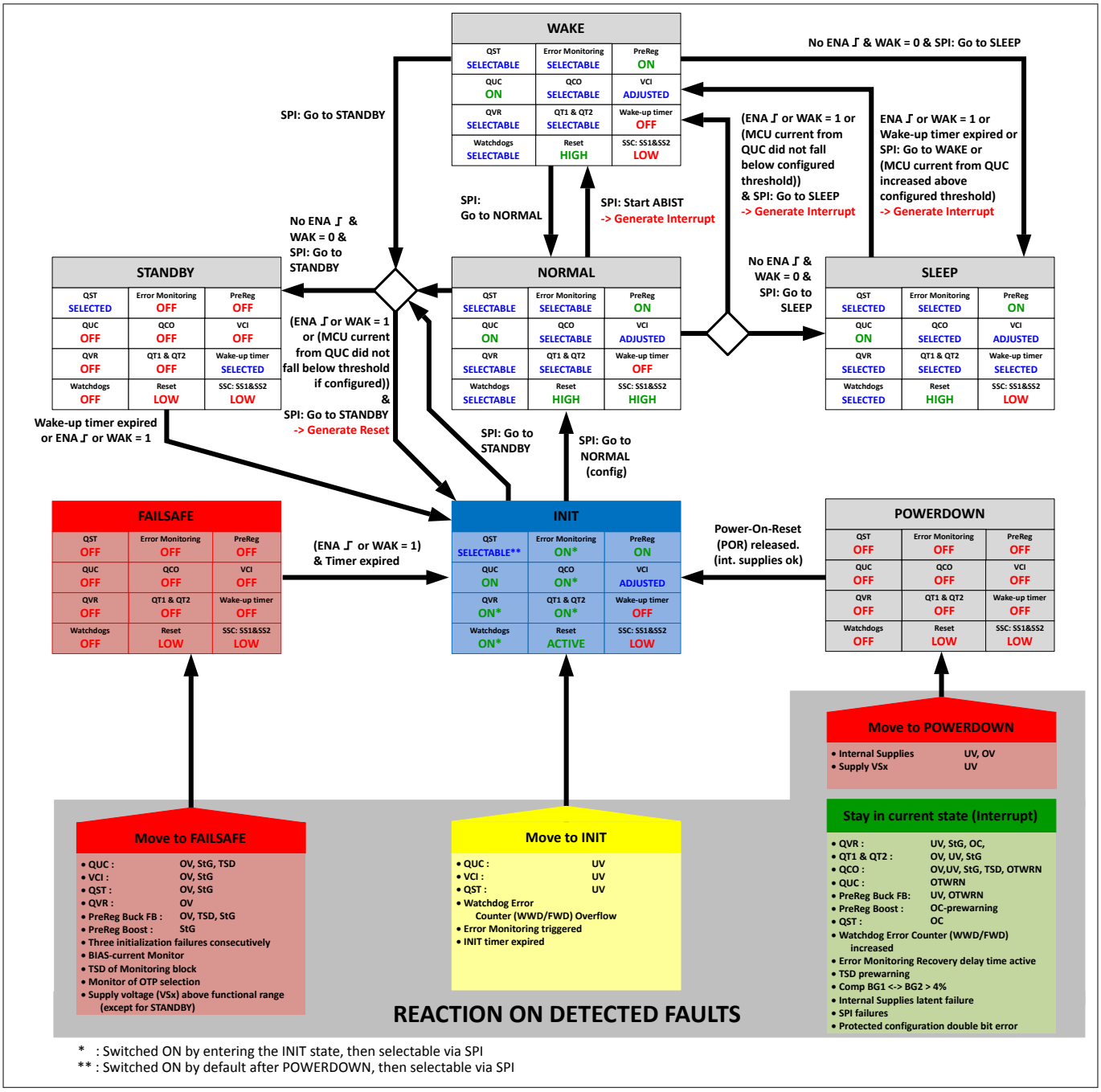


Figure 24 Flow diagram state machine

Description

- ON /OFF:= Switched ON or OFF, not configurable by SPI command
- ON*:= Switched ON by movement into INIT-state, then selectable via SPI

- SELECTED:= May be configured (switched ON or OFF) by SPI command in previous state or is selected by the state transition request (DEVCTRL) in case of supply configuration for SLEEP-state.
- SELECTABLE:= May be switched ON or OFF by SPI command in this state
- SELECTABLE**:= Switched ON by default after POWERDOWN, then selectable via SPI
- ADJUSTED:= Defined present or not present by configuration pin, not configurable by SPI command
- ACTIVE:= as described in INIT-state
- SSC, SS1&2:= Safe State Control signals 1 and 2
- LOW:= Signal is low
- HIGH:= Signal is high
- OV:= Overvoltage
- UV:= Undervoltage
- StG:= Short to ground
- TSD:= Thermal shut down
- OC:= Overcurrent
- ABIST:= Analog built in self test
- Comp BG1 <-> BG2 > 4%: The difference between both bandgaps 1 and 2 is more than 4%

10.2 Description of states

10.2.1 POWERDOWN-state

The device is in POWERDOWN-state as long the Power-on-Reset (POR) is not released.

POWERDOWN		
QST OFF	Error Monitoring OFF	PreReg OFF
QUC OFF	QCO OFF	VCI OFF
QVR OFF	QT1 & QT2 OFF	Wake-up timer OFF
Watchdogs OFF	Reset LOW	SSC: SS1&SS2 LOW

Figure 25 **POWERDOWN-state**

Table 18 **POWERDOWN-state settings**

Part/Function	Value	Description
QST	OFF	• The standby supply QST is off
PreReg	OFF	• The pre regulators are off
QUC	OFF	• The microcontroller main supply QUC is off
QCO	OFF	• The communication supply QCO is off
VCI	OFF	• The function external output voltage monitoring VCI is off
QVR	OFF	• The voltage reference supply QVR is off
QT1 & QT2	OFF	• Both trackers QT1 & QT2 are off
Wake-up timer	OFF	• The wake-up timer is off
Watchdogs	OFF	• The watchdogs are off
Error monitoring	OFF	• The Error monitoring is off
Reset	LOW	• The reset output is low
SSC: SS1&SS2	LOW	• Both safe state signals are LOW and the application is in safe state

10.2.2 INIT-state

During INIT-state the device expects valid communication with the MCU within the INIT timer. Otherwise an initialization timeout occurs. The initialization timer starts with the rising edge of ROT.

The initialization timer is stopped as soon as three boundary conditions are fulfilled:

- Valid SPI communication received from MCU
- Watchdog(s) serviced once according to default configuration or according to reconfiguration
- ERR monitoring serviced properly (minimum 3 periods provided) or configured to be OFF

Alternatively the initialization is stopped by activation of microcontroller programming support (MPS). For details please refer to Chapter 10.7

INIT		
QST SELECTABLE**	Error Monitoring ON*	PreReg ON
QUC ON	QCO ON*	VCI ADJUSTED
QVR ON*	QT1 & QT2 ON*	Wake-up timer OFF
Watchdogs ON*	Reset ACTIVE	SSC: SS1&SS2 LOW

Figure 26 **INIT-state**

Table 19 **INIT-state settings**

Part/Function	Value	Description
QST	SELECTABLE**	• The standby supply QST is switched on when entering from POWERDOWN-state • It may be switched on or off by SPI command. This configuration is kept through all states, except POWERDOWN-state
PreReg	ON	• The step down pre regulator is on • Step up pre regulator is active depending on the input voltage and this option is selected by pin STU.
QUC	ON	• The microcontroller main supply QUC is on
QCO	ON*	• The communication supply QCO is switched on per default • The QCO may be switched off and on by SPI
VCI	ADJUSTED	• The external output voltage monitoring VCI is switched ON or OFF depending on pin SEC (SEC pin considered only during power-sequencing)
QVR	ON*	• The voltage reference supply QVR is switched on per default • The QVR may be switched off and on by SPI
QT1 & QT2	ON*	• Both trackers QT1 & QT2 are switched on per default • Both trackers QT1 & QT2 may be switched off and on by SPI independently

(table continues...)

Table 19 (continued) INIT-state settings

Part/Function	Value	Description
Wake-up timer	OFF	• The wake-up timer is off
Watchdogs	ON*	• The window watchdog is switched on per default in SPI triggered mode • The functional watchdog is switched off per default • The watchdogs may be configured and switched ON or OFF by SPI
Error monitoring	ON	• The Error monitoring is switched on per default • The Error monitoring may be configured and switched ON or OFF by SPI
Reset	ACTIVE	• The reset output goes HIGH as soon as all MCU related output voltages V_{QST} , V_{QUC} and V_{VCI} are above their undervoltage reset threshold,$V_{RT,xxx,low}$ delayed by the reset delay time t_{RD}.
SSC: SS1&SS2	LOW	• Both safe state signals are LOW and the application is in safe state

10.2.3 NORMAL-state

In NORMAL-state the device is supplying the MCU and the applications. Safety and monitoring functions (like reset-block and Safe State Control) are active. The MCU may configure several post regulators of the device and the wake-up timer via SPI command for this state.

NORMAL		
QST SELECTABLE	Error Monitoring SELECTABLE	PreReg ON
QUC ON	QCO SELECTABLE	VCI ADJUSTED
QVR SELECTABLE	QT1 & QT2 SELECTABLE	Wake-up timer OFF
Watchdogs SELECTABLE	Reset HIGH	SSC: SS1&SS2 HIGH

Figure 27 **NORMAL-state**

Table 20 **NORMAL-state settings**

Part/Function	Value	Description
QST	SELECTABLE	• The standby supply QST may be switched on or off by SPI command.
PreReg	ON	• The step down pre regulator is on • Step up pre regulator is active depending on the input voltage and this option is selected by pin STU.
QUC	ON	• The microcontroller main supply QUC is on
QCO	SELECTABLE	• The communication supply QCO may be switched on of off by SPI command
VCI	ADJUSTED	• The external output voltage monitoring VCI is switched ON or OFF depending on pin SEC (SEC pin considered only during power-sequencing)
QVR	SELECTABLE	• The voltage reference supply QVR may be switched on of off by SPI command
QT1 & QT2	SELECTABLE	• Both trackers QT1 & QT2 may be switched off and on by SPI independently
Wake-up timer	OFF	• The wake-up timer is switched off
Watchdogs	SELECTABLE	• The watchdogs may be configured and switched ON or OFF by SPI
Error monitoring	SELECTABLE	• The Error monitoring may be configured and switched ON or OFF by SPI
Reset	HIGH	• The reset output is HIGH
SSC: SS1&SS2	HIGH	• Both safe state signals are HIGH

10.2.4 STANDBY-state

The STANDBY-state is a low power state which the MCU may enter to reduce the current consumption to a minimum when the application is not used for a long time. The application is in a safe state.

STANDBY		
QST SELECTED	Error Monitoring OFF	PreReg OFF
QUC OFF	QCO OFF	VCI OFF
QVR OFF	QT1 & QT2 OFF	Wake-up timer SELECTED
Watchdogs OFF	Reset LOW	SSC: SS1&SS2 LOW

Figure 28 **STANDBY-state**

Table 21 **STANDBY-state settings**

Part/Function	Value	Description
QST	SELECTED	• The standby supply QST is ON or OFF depending on its configuration
PreReg	OFF	• The pre regulator are off
QUC	OFF	• The microcontroller main supply QUC is off
QCO	OFF	• The communication supply QCO is off
VCI	OFF	• The function external output voltage monitoring VCI is off
QVR	OFF	• The voltage reference supply QVR is off
QT1 & QT2	OFF	• Both trackers QT1 & QT2 are off
Wake-up timer	SELECTED	• The wake-up timer is ON or OFF depending on its configuration
Watchdogs	OFF	• The watchdogs are off
Error monitoring	OFF	• The Error monitoring is off
Reset	LOW	• The reset output is low
SSC: SS1&SS2	LOW	• Safe state signals 1 and 2 are low • The application is in a safe state

10.2.5 SLEEP-state

The SLEEP-state is a low power state which the MCU may enter to reduce the current consumption when the application is not used (e.g. microcontroller is in STOP mode). The MCU may configure the status of regulators and the safety functions via SPI command in the previous state. The application is in a safe state

SLEEP		
QST SELECTED	Error Monitoring SELECTED	PreReg ON
QUC ON	QCO SELECTED	VCI ADJUSTED
QVR SELECTED	QT1 & QT2 SELECTED	Wake-up timer SELECTED
Watchdogs SELECTED	Reset HIGH	SSC: SS1&SS2 LOW

Figure 29 **SLEEP-state**

Table 22 **SLEEP-state settings**

Part/Function	Value	Description
QST	SELECTED	• The standby supply QST is switched ON or OFF according to previous configuration.
PreReg	ON	• The step down pre regulator is on • Step up pre regulator is active depending on the input voltage and this option is selected by pin STU
QUC	ON	• The microcontroller main supply QUC is switched on • In SLEEP-state the device is monitoring the output current of QUC: If the QUC current exceeds a certain threshold $I_{QUC,att}$, an interrupt is generated and the device moves to WAKE-state
QCO	SELECTED	• The communication supply QCO is switched ON or OFF depending on the configuration by the state transition request to move into SLEEP and cannot be changed in SLEEP-state.
VCI	ADJUSTED	• The external output voltage monitoring VCI is switched ON or OFF depending on pin SEC (SEC pin considered only during power-sequencing)
QVR	SELECTED	• The voltage reference supply QVR is switched ON or OFF depending on the configuration by the state transition request to move into SLEEP and cannot be changed in SLEEP-state.
QT1 & QT2	SELECTED	• The trackers QT1 & QT2 are switched ON or OFF depending on the configuration by the state transition request to move into SLEEP and cannot be changed in SLEEP-state
Wake-up timer	SELECTED	• The wake-up timer is ON or OFF depending on its configuration
Watchdogs	SELECTED	• The watchdogs are ON or OFF depending on their configuration for SLEEP

(table continues...)

Table 22 (continued) SLEEP-state settings

Part/Function	Value	Description
Error monitoring	SELECTED	• The Error monitoring is ON or OFF depending on its configuration for SLEEP
Reset	HIGH	• The reset output is HIGH
SSC: SS1&SS2	LOW	• Both safe state signals are LOW and the application is in safe state

10.2.6 WAKE-state

The WAKE-state is an intermediate state between NORMAL and the low power states SLEEP and STANDBY. This state provides the same functionality as the NORMAL-state, but shall ensure the application being in safe state by keeping low the safe state outputs. It should be used to prepare the system for a correct and safe reentry to the NORMAL-state by servicing the watchdogs and the error monitoring (minimum 3 periods) according to the selected configuration. Furthermore it provides the possibility to move the device into the low power states SLEEP and STANDBY.

The TLF35585QV moves from SLEEP or from the transition to SLEEP into WAKE-state, if the output current from QUC exceeds a certain threshold $I_{QUC,att}$, an valid ENA or WAK signal is recognized or the SPI command "Go to WAKE" is sent. Another transition into WAKE-state is initiated by the usage of the ABIST in NORMAL-state.

By entering the state an interrupt is generated and the supervision functions (watchdogs and ERR monitoring) become active according to their previous configuration in NORMAL-state. Upon entering the WAKE-state the configuration of the supplies resumes to the one of the previous NORMAL-state. The application is in a safe state

WAKE		
QST SELECTABLE	Error Monitoring SELECTABLE	PreReg ON
QUC ON	QCO SELECTABLE	VCI ADJUSTED
QVR SELECTABLE	QT1 & QT2 SELECTABLE	Wake-up timer OFF
Watchdogs SELECTABLE	Reset HIGH	SSC: SS1&SS2 LOW

Figure 30 **WAKE-state**

Table 23 **WAKE-states settings**

Part/Function	Value	Description
QST	SELECTABLE	• The standby supply QST may be switched ON or OFF by SPI command.
PreReg	ON	• The step down pre regulator is on • Step up pre regulator is active depending on the input voltage and this option is selected by pin STU.
QUC	ON	• The microcontroller main supply QUC is on
QCO	SELECTABLE	• The communication supply QCO is switched ON or OFF depending on its configuration in the NORMAL-state prior to SLEEP-state when entering WAKE-state • It may be switched on of off by SPI command
VCI	ADJUSTED	• The external output voltage monitoring VCI is switched ON or OFF depending on pin SEC (SEC pin considered only during power-sequencing)
QVR	SELECTABLE	• The voltage reference supply QVR is switched ON or OFF depending on its configuration in NORMAL-state prior to SLEEP-state when entering WAKE-state • It may be switched on of off by SPI command

(table continues...)

Table 23 (continued) WAKE-states settings

Part/Function	Value	Description
QT1 & QT2	SELECTABLE	• Both trackers QT1 & QT2 is switched ON or OFF depending on their configuration in NORMAL-state prior to SLEEP-state when entering WAKE-state • It may be switched on of off by SPI command
Wake-up timer	OFF	• The wake-up timer is switched off
Watchdogs	SELECTABLE	• The watchdogs is switched ON or OFF depending on their configuration in NORMAL-State prior to SLEEP-state when entering WAKE-State • The watchdogs may be configured and switched ON or OFF by SPI
Error monitoring	SELECTABLE	• The Error monitoring is switched ON or OFF depending on the configuration in NORMAL-state prior to SLEEP-state when entering WAKE-state • The Error monitoring may be configured and switched ON or OFF by SPI
Reset	HIGH	• The reset output is HIGH
SSC: SS1&SS2	LOW	• Both safe state signals are LOW and the application is in safe state

10.2.7 FAILSAFE-state

FAILSAFE-state occurs after the detection of a severe failure. In FAILSAFE-state all regulators are switched off. The application is in a safe state.

FAILSAFE		
QST OFF	Error Monitoring OFF	PreReg OFF
QUC OFF	QCO OFF	VCI OFF
QVR OFF	QT1 & QT2 OFF	Wake-up timer OFF
Watchdogs OFF	Reset LOW	SSC: SS1&SS2 LOW

Figure 31 **FAILSAFE-state**

Table 24 **FAILSAFE-state settings**

Part/Function	Value	Description
QST	OFF	• The standby supply QST is off
PreReg	OFF	• The pre regulators are off
QUC	OFF	• The microcontroller main supply QUC is off
QCO	OFF	• The communication supply QCO is off
VCI	OFF	• The function external output voltage monitoring VCI is off
QVR	OFF	• The voltage reference supply QVR is off
QT1 & QT2	OFF	• Both trackers QT1 & QT2 are off
Wakeup-Timer	OFF	• The wake-up timer is off
Watchdogs	OFF	• The watchdogs are off
Error monitoring	OFF	• The Error monitoring is off
Reset	LOW	• The reset output is low
SSC: SS1&SS2	LOW	• Both safe state signals are LOW and the application is in safe state

10.3 Transition between states

State transitions requested via SPI command are initiated with a valid positive going edge of the chip select (SCS).

10.3.1 POWERDOWN → INIT-state

The device moves from POWERDOWN to INIT-state when the Power-on-Reset (POR) is released and starts the power-sequencing when all of the following conditions are met:

- V_{VS} above $V_{PS,start}$ when increasing
- no under or overvoltage on internal supplies

10.3.2 INIT → NORMAL-state

Prerequisites

- Watchdog(s) need to be serviced once according to default configuration or according to reconfiguration within the INIT timer
- ERR monitor needs to be serviced with a valid signal (minimum 3 periods) or disabled within the INIT timer.
- If functional watchdog is activated, a valid FWD triggering needs to be provided.
- A delay of 60µs after the provided services has to be considered to ensure proper release of internal validation signals.

Triggering events

- State transition is only initiated by the SPI command "Go to NORMAL".

Exceptions

- none

Timing diagram

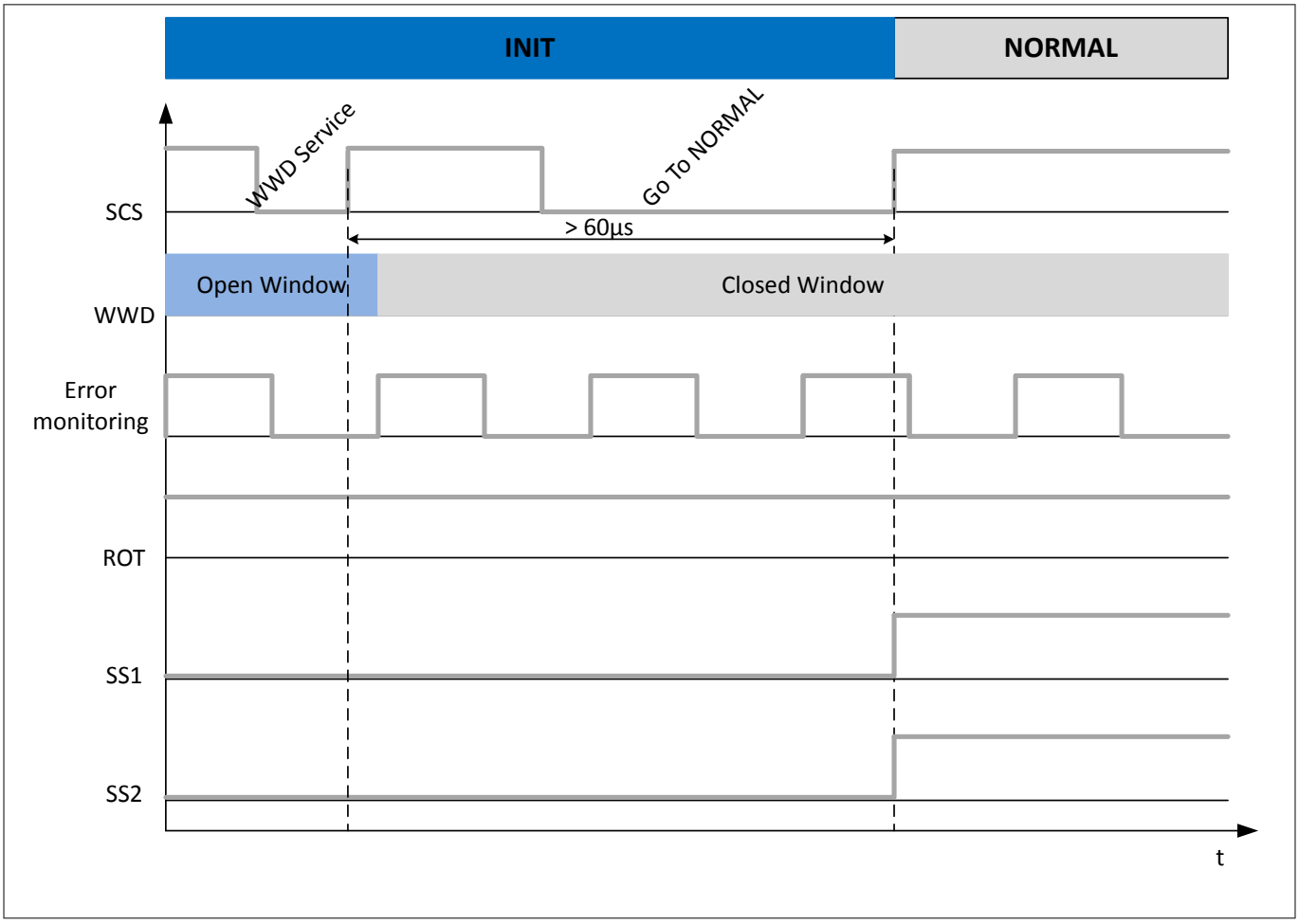


Figure 32 Transition from INIT to NORMAL-state

- A valid SPI command "Go to NORMAL" (valid with chip select high at pin SCS) moves the device from INIT-state to NORMAL-state.

- Reset pin ROT stays HIGH as the post regulators are already active in INIT-state.
- With the positive edge of chip select high (at pin SCS) the safe state signals SS1 and SS2 are pulled to HIGH at same time. (Internal reaction time for the safe state outputs according to Table 28 has to be considered)

10.3.3 Movements between NORMAL and SLEEP-state

10.3.3.1 NORMAL → SLEEP-state

Prerequisites

- Selection of QUC current monitor or absolute transition timer.
- Transition delay timer $t_{tr,del}$ needs to be configured or default is used.
- Optionally QUC current threshold needs to be defined or default is used.

Triggering events

- State transition is only initiated by the SPI command "Go to SLEEP".

Exceptions

- If a valid ENA (edge) or WAK (level) signal is detected in the transition state to SLEEP-state, the devices moves to the WAKE-state and send an interrupt (at pin INT)
- If the QUC current monitor is activated and the current consumption of the microcontroller is not below the selected QUC current threshold before the transition delay timer $t_{tr,del}$ has expired, the device moves to the WAKE-state and send an interrupt (at pin INT)

Timing diagram

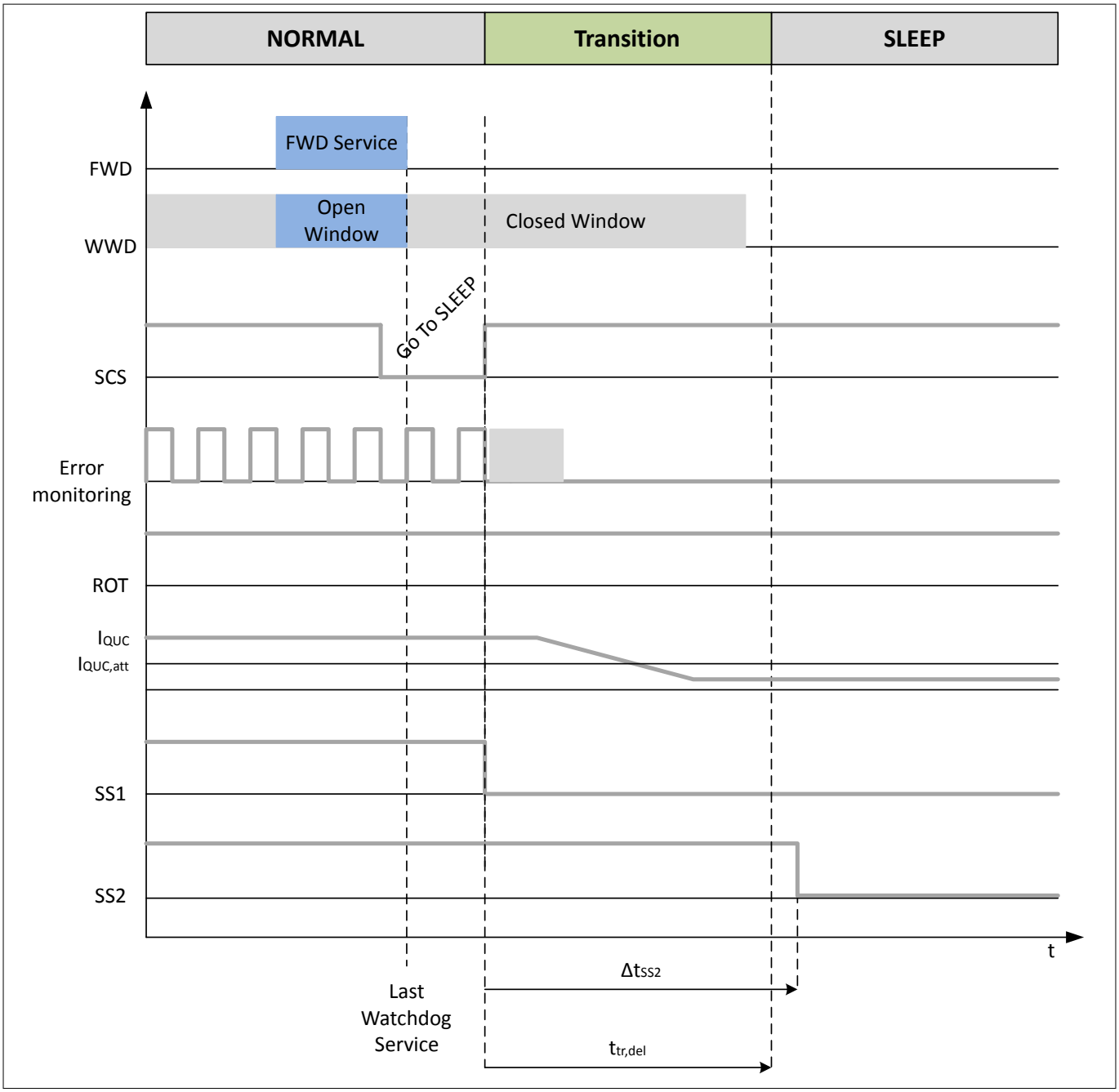


Figure 33 Transition from NORMAL to SLEEP-state

- Before the SPI command "Go to SLEEP" is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of SCS signal is well in between the "closed window" of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command "Go to SLEEP"
- The positive edge of chip select (pin SCS) after the SPI command "Go to SLEEP" initiates the transition. With chip select high the safe state signal SS1 is pulled to zero and the device leaves NORMAL-state and enters the transition state (to SLEEP-state). (Internal reaction time for the safe state outputs according to Table 28 has to be considered)
- With chip select (pin SCS) high the error monitoring (pin ERR) is stopped - the toggling may end with the positive edge at pin SCS. If the error monitoring should be selected to be active in SLEEP-state continuous toggling is mandatory.

- The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin SCS. If one or both watchdogs should be selected to be active in SLEEP-state continuous watchdog service is mandatory.
- Reset pin ROT stays HIGH as the post regulators are not switched off.
- In case the absolute transition timer is selected, the device moves from transition state to SLEEP-state after the transition delay time $t_{tr,del}$. The transition time $t_{tr,del}$ can be determined by SPI command between 100 µs to 1.6 ms, the default setting is 900 µs. After this transition time it should be ensured that the MCU current consumption has fallen below the QUC monitoring threshold $I_{QUC,att}$ to keep the device in SLEEP-state.
- If the QUC current monitor is enabled the MCU current out of pin QUC must fall below the QUC monitoring threshold $I_{QUC,att}$ within the configured maximum transition time $t_{tr,del}$ in **DEVCFG0**.TRDEL. The time for the transition is depending, how long it takes that the MCU current falls below the QUC monitoring threshold $I_{QUC,att}$, if it is below the transition is done.
- After delay time Δt_{SS2} the safe state signal SS2 goes to zero. The adjusted delay time Δt_{SS2} is independent from the transition delay time $t_{tr,del}$.

10.3.3.2 SLEEP → WAKE-state

Prerequisites

- none

Triggering events

- SPI command "Go to WAKE".
- Valid Wake-Signal (ENA or WAK).
- Current of QUC exceeding the configured threshold.
- Wake-up timer expired, if enabled

Exceptions

- none

Timing diagram

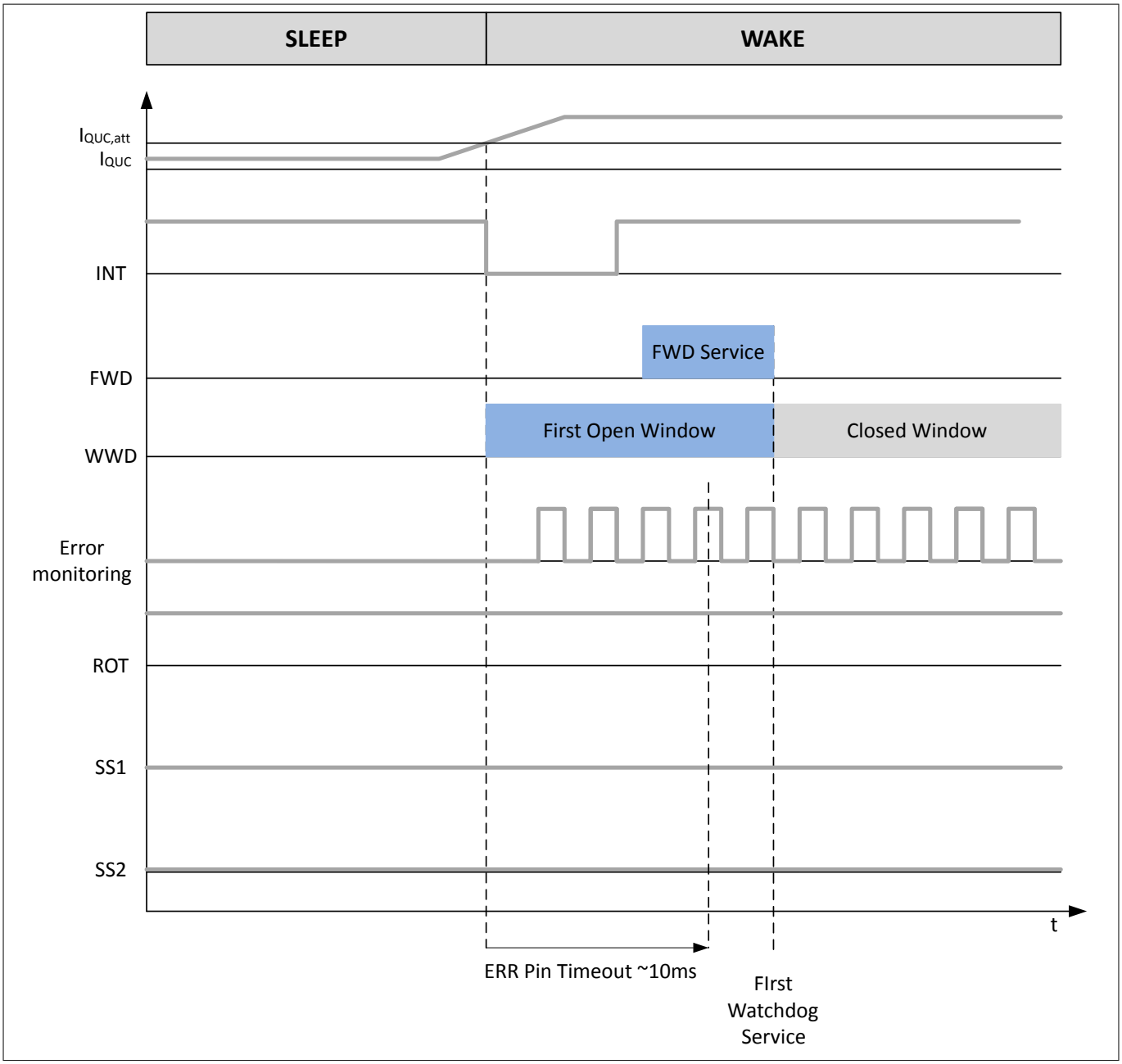


Figure 34 **Transition from SLEEP to WAKE-state**

- The state transition is completed without a transition time and is indicated by an interrupt at pin INT. The triggering event for the transition from SLEEP can be read from the status register **WKSF**.
- All three monitoring functions (window watchdog, functional watchdog and error monitoring) recover to the condition active or inactive (switched off) as they were in the NORMAL-state previous to the SLEEP-state.
- The configuration of the supplies recover to the condition active or inactive (switched off) as they were in the NORMAL-state previous to the SLEEP-state.
- In case the window watchdog was active in the previous NORMAL-state, with the negative edge of interrupt signal (at pin INT) the window watchdog opens the first Open Window, the time of this first Open Window depends on the configured cycle time and is 600 ms (WDCYC = 1) or 60 ms (WDCYC = 0) (if the window watchdog has not been active in SLEEP-state) and requires service. If the window watchdog has been active in SLEEP-state continuous service is mandatory.

- In case the functional watchdog was active in the previous NORMAL-state, with the negative edge of interrupt signal (at pin INT) the functional watchdog starts the heartbeat timer and require service. If the functional watchdog has been active in SLEEP-state continuous service is mandatory.
- In case the ERR pin monitoring was active in the previous NORMAL-state, with the negative edge of interrupt signal (at pin INT) the error monitoring becomes active again. Latest 10 ms after the activation a toggling signal (with at least three periods past) at pin ERR is required. If the error monitoring has been active in SLEEP-state continuous toggling is mandatory.
- Reset pin ROT stays HIGH as the post regulators are active in SLEEP-state and in WAKE-state.
- The safe signals SS1 and SS2 stays LOW in SLEEP and in WAKE-state.
- If all active monitoring functions (window watchdog, functional watchdog and error monitoring) are serviced properly in WAKE-state, you may stay in WAKE-state as long as you want.
- If all three monitoring functions (window watchdog, functional watchdog and error monitoring) are inactive (switched off) in WAKE-state, you may stay in WAKE-state as long as you want.

10.3.3.3 WAKE → SLEEP-state

Prerequisites

- Selection of QUC current monitor or absolute transition timer.
- Transition delay timer $t_{tr,del}$ needs to be configured or default is used.
- Optionally QUC current threshold needs to be defined or default is used.

Triggering events

- State transition is only initiated by the SPI command "Go to SLEEP".

Exceptions

- If a valid ENA (edge) or WAK (level) signal is detected in the transition state to SLEEP-state, the device moves back to the WAKE-state and send an interrupt (at pin INT)
- If the QUC current monitor is activated and the current consumption of the microcontroller is not below the selected QUC current threshold before the transition delay timer $t_{tr,del}$ has expired, the device moves back to the WAKE-state and send an interrupt (at pin INT)

Timing diagram

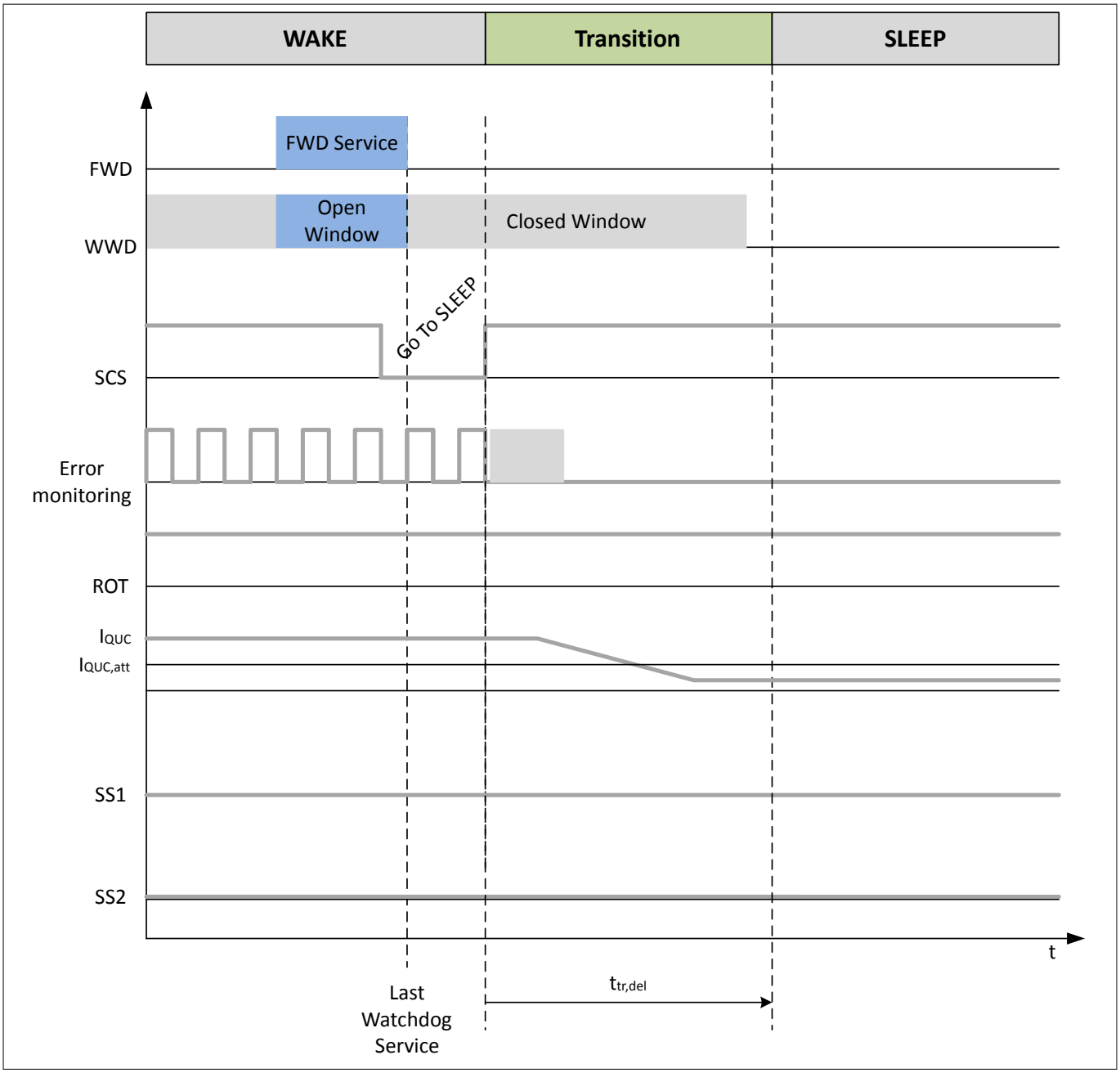


Figure 35 **Transition from WAKE to SLEEP-state**

- Before the SPI command "Go to SLEEP" is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of SCS signal is well in between the "closed window" of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command "Go to SLEEP"
- The positive edge of chip select (pin SCS) after the SPI command "Go to SLEEP" initiates the transition. With chip select high the device leaves WAKE-state and enters the transition state (to SLEEP-state).
- With chip select (pin SCS) high the error monitoring (pin ERR) is stopped - the toggling may end with the positive edge at pin SCS. If the error monitoring should be selected to be active in SLEEP-state continuous toggling is mandatory.

- The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin SCS. If one or both watchdogs should be selected to be active in SLEEP-state continuous watchdog service is mandatory.
- Reset pin ROT stays HIGH as the post regulators are not switched off.
- If the QUC current monitor is enabled the MCU current out of pin QUC must fall below the QUC monitoring threshold $I_{QUC,att}$ within the configured maximum transition delay time $t_{tr,del}$. The time for the transition is depending, how long it takes that

  the MCU current falls below the QUC monitoring threshold $I_{QUC,att}$, if it is below the transition is done.
- Safe state signals SS1 and SS2 stay LOW all the time.

10.3.4 Movements between NORMAL and STANDBY-state

10.3.4.1 NORMAL → STANDBY-state

Prerequisites

- Selection of QUC current monitor or absolute transition timer.
- Transition timer needs to be configured or default is used.
- Optionally QUC current threshold needs to be defined or default is used.

Triggering events

- State transition is only initiated by the SPI command "Go to STANDBY".

Exceptions

- If a valid ENA (edge) or WAK (level) signal is detected in the transition state to STANDBY-state, the device moves to the INIT-state and a reset (ROT) is generated.
- If the QUC current monitor is activated and the current consumption of the microcontroller is not below the selected QUC current threshold before the transition delay timer $t_{tr,del}$ has expired, the device moves to the INIT-state and a reset (ROT) is generated.

Timing diagram

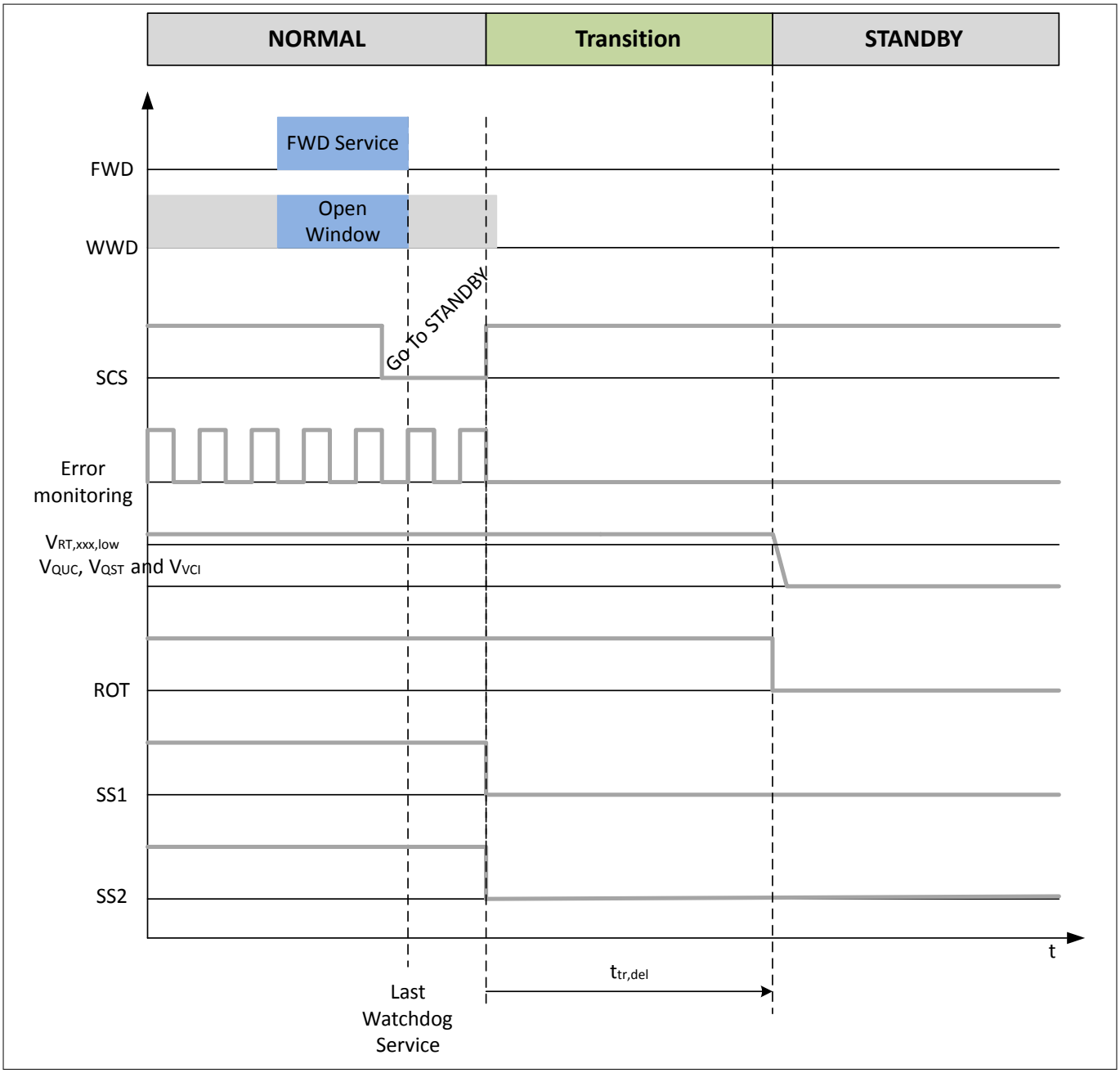


Figure 36 **Transition from NORMAL to STANDBY-state**

- Before the SPI command "Go to STANDBY" is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of SCS signal is well in between the "closed window" of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command "Go to STANDBY"
- The positive edge of chip select (pin SCS) after the SPI command "Go to STANDBY" initiates the transition. With chip select high the safe state signals SS1 and SS2 are pulled to zero without delay between SS1 and SS2. The device leaves NORMAL-state and enters the transition state (to STANDBY-state).

  (Internal reaction time for the safe state outputs according to Table 28 has to be considered)
- With chip select (pin SCS) high the error monitoring (pin ERR) is stopped - the toggling may end with the positive edge at pin SCS.
- The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin SCS.

- With a successful transition from NORMAL to STANDBY-state the reset (ROT) is pulled to LOW after the transition time after chip select (pin SCS) going high.
- All pre regulators and all post regulators (with the exception of the standby supply - it may be ON or OFF in STANDBY-state) are switched off at the point when the transition is completed after the reset (ROT) is pulled low.
- In case the absolute transition timer is selected, the device moves from transition state to STANDBY-state after the transition delay time $t_{tr,del}$. The transition time $t_{tr,del}$ can be determined by SPI command between 100 µs to 1.6 ms, the default setting is 900 µs.
- In case the QUC current monitor is selected for the transition, the device moves from transition state to STANDBY-state at the point the current consumption measured at the QUC drops below the selected threshold before the transition delay timer $t_{tr,del}$ has expired.

10.3.4.2 STANDBY → INIT-state

Prerequisites

- none

Triggering events

- Valid ENA (edge) or WAK (level) signal.
- Wake-up timer expired, if enabled

Exceptions

- none

Timing diagram

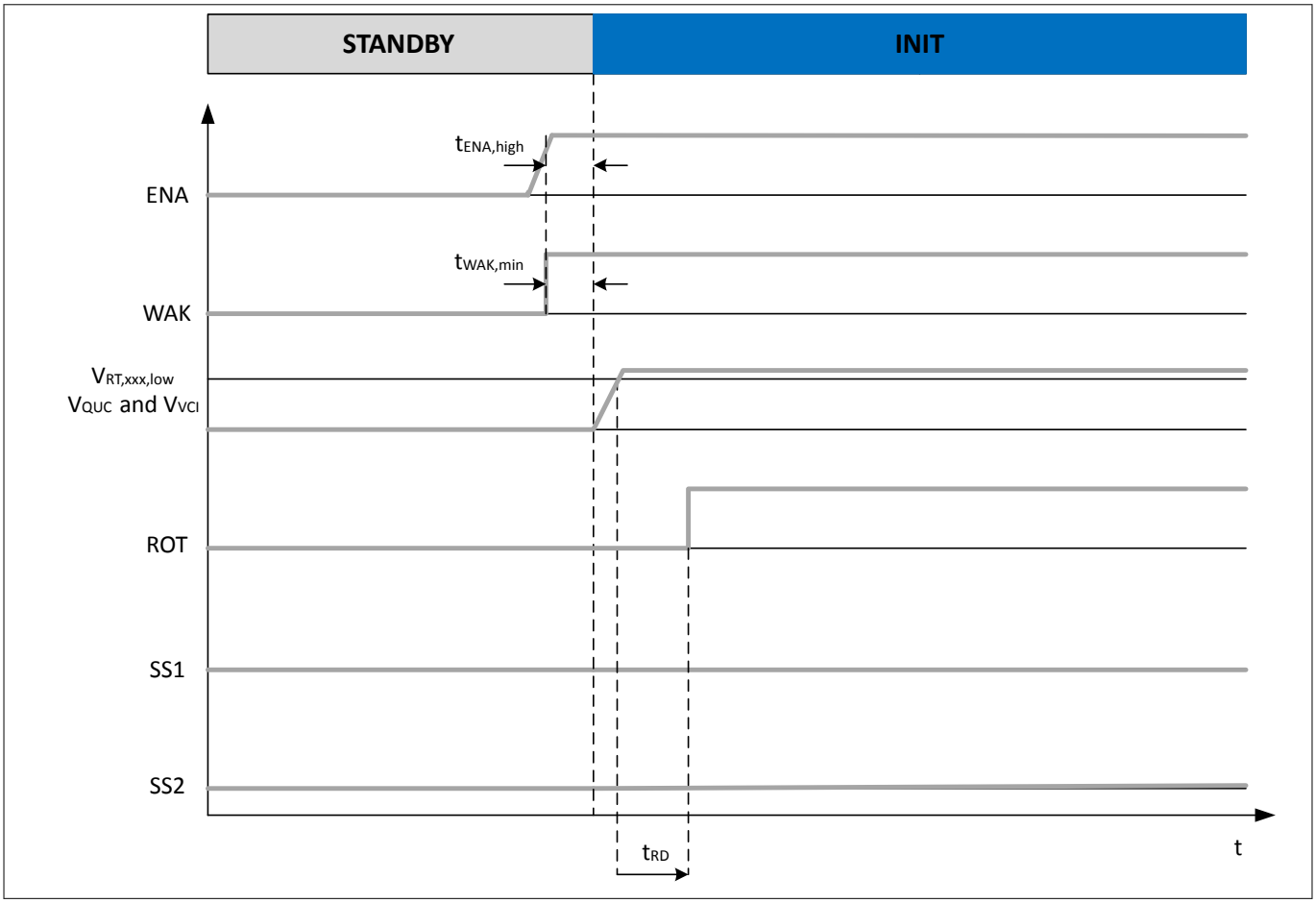


Figure 37 Transition from STANDBY to INIT-state

- All pre regulators and all post regulators are switched on according to the power sequencing, except the QST is kept ON or OFF according to its configuration (simplified in figure above).
- The power on reset delay time is started as soon as the latest of the MCU related regulators V_{QUC} or V_{VCI} (if enabled) crosses the related undervoltage reset threshold $V_{RT,xxx,low}$ on the way up.
- After the power on reset delay time has expired the reset (ROT) is set to HIGH.
- The safe signals SS1 and SS2 stay LOW in STANDBY-state and in INIT-state.

10.3.4.3 INIT → NORMAL-state

For this state transition please refer to the Chapter 10.3.2.

10.3.5 NORMAL → WAKE-state

For this state transition please refer to the description of ABIST in Chapter 10.6.1.

10.3.6 WAKE → NORMAL-state

Prerequisites

- The activated supervision functions (e.g. window watchdog, functional watchdog, ERR pin monitoring) need to be serviced at least once (minimum 3 periods for ERR monitoring) in the active WAKE-state, if they are restarted/reinitialized in WAKE-state (e.g. watchdog being inactive in previous SLEEP-state)

Triggering events

- State transition is only initiated by the SPI command "Go to NORMAL".

Exceptions

- none

Timing diagram

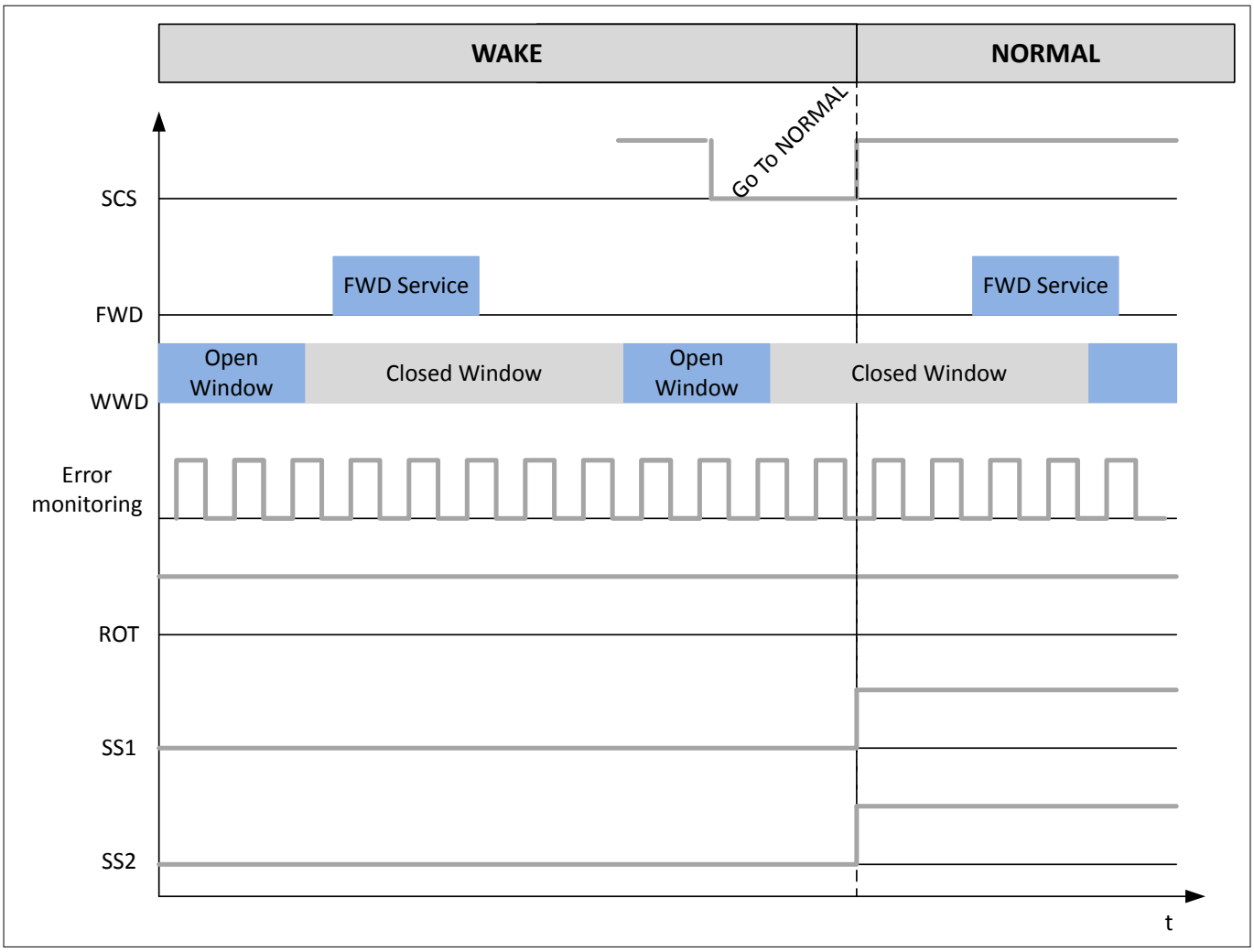


Figure 38 **Transition from WAKE to NORMAL-state**

- The enable signal is disregarded. A valid enable (edge) signal does not move the device from WAKE to NORMAL-state.
- The state of wake signal is disregarded. A valid wake (level) signal does not move the device from WAKE to NORMAL-state.
- The window watchdog (if active in WAKE-state) requires continuous service - not synchronized to the transition from WAKE-state to NORMAL-state.
- The functional watchdog (if active in WAKE-state) requires continuous service - not synchronized to the transition from WAKE-state to NORMAL-state.
- The error monitoring (at pin ERR) (if active in WAKE-state) requires a continuous toggling signal - not synchronized to the transition from WAKE-state to NORMAL-state - but minimum 3 periods detected to enter accept the movement into NORMAL-state.
- Reset pin ROT stays HIGH as the post regulators are active in WAKE-state and in NORMAL-state.
- With the positive edge of chip select high (at pin SCS) the safe state signals SS1 and SS2 are pulled to HIGH at same time. (Internal reaction time for the safe state outputs according to Table 28 has to be considered)

10.3.7 INIT/WAKE → STANDBY-state

Prerequisites

- Selection of QUC current monitor or absolute transition timer.
- Transition timer needs to be configured or default is used.
- Optionally QUC current threshold needs to be defined or default is used.

Triggering events

- State transition is only initiated by the SPI command "Go to STANDBY".

Exceptions

- If a valid ENA (edge) or WAK (level) signal is detected in the transition state to STANDBY-state, the device moves to the INIT-state and a reset (ROT) is generated.
- If the QUC current monitor is activated and the current consumption of the microcontroller is not below the selected current threshold before the transition timer has expired, the device moves to the INIT-state and a reset (ROT) event is generated.

Timing diagram

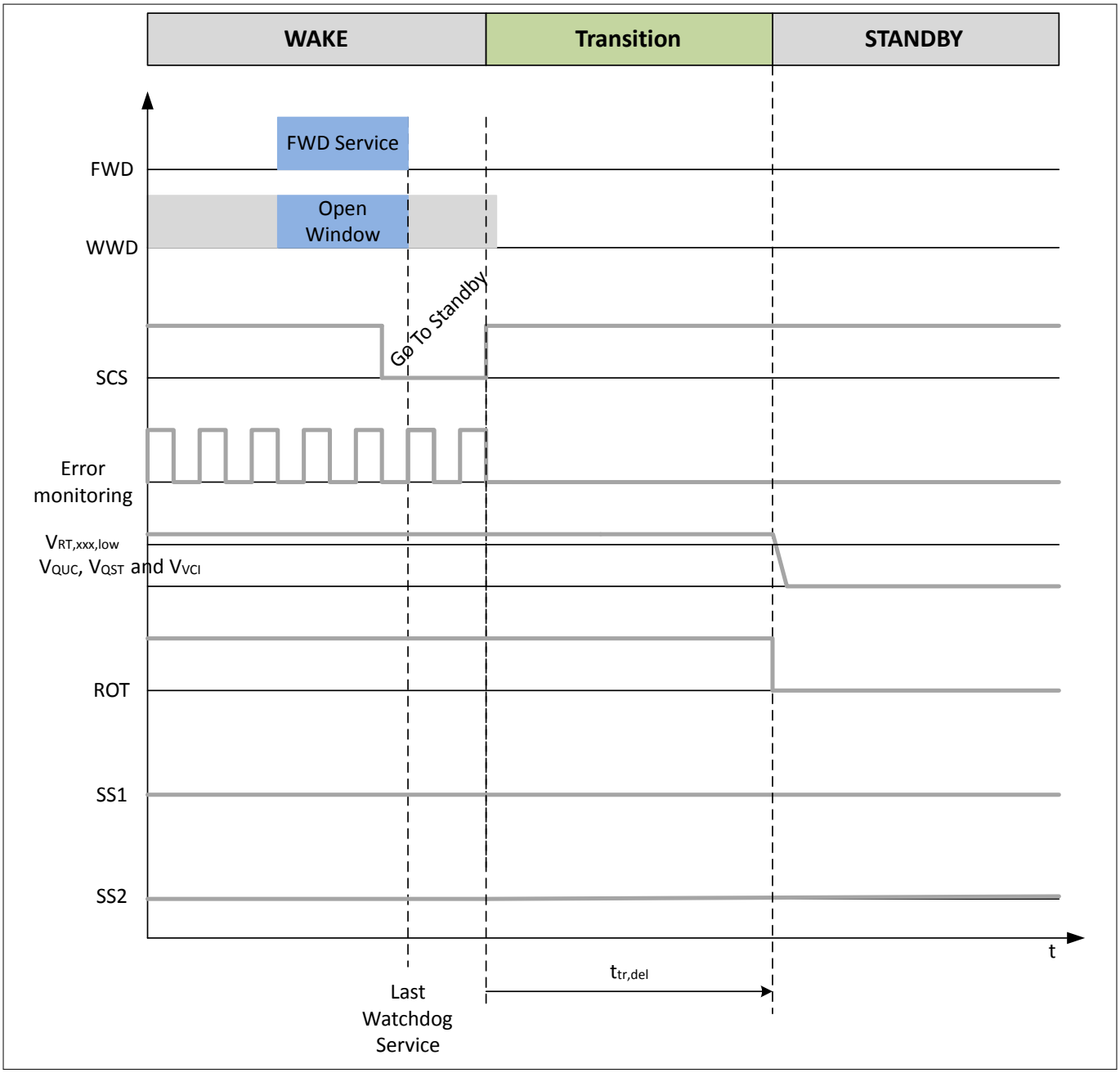


Figure 39 **Transition from INIT or WAKE to STANDBY-state**

- Before the SPI command "Go to STANDBY" is applied, the watchdog(s) - if in use should be serviced, so that the positive edge of SCS signal is well in between the "closed window" of the window watchdog. This is recommended to avoid interference between a missing watchdog trigger and the transition command "Go to STANDBY"
- The positive edge of chip select (pin SCS) after the SPI command "Go to STANDBY" initiates the transition. In the INIT or WAKE-state the safe state signals SS1 and SS2 are LOW and is kept LOW for the transition to STANDBY. The device leaves INIT or WAKE-state and enters the transition state (to STANDBY-state).
- With chip select (pin SCS) high the error monitoring (pin ERR) is stopped - the toggling may end with the positive edge at pin SCS.
- The monitoring of window watchdog and functional watchdog is stopped with the positive edge at pin SCS.

- With a successful transition from INIT or WAKE to STANDBY-state the reset (ROT) is pulled to LOW after the transition time after chip select (pin SCS) going high.
- All pre regulators and all post regulators (with the exception of the standby supply - it may be ON or OFF in STANDBY-state) are switched off at the point when the transition is completed after the reset (ROT) is pulled low.
- In case the absolute transition timer is selected, the device moves from transition state to STANDBY-state after the transition time $t_{tr,del}$. The transition time $t_{tr,del}$ can be determined by SPI command between 100 µs to 1.6 ms, the default setting is 900 µs.
- In case the QUC current monitor is selected for the transition, the device moves from transition state to STANDBY-state at the point the current consumption measured at the QUC drops below the selected threshold before the transition delay timer $t_{tr,del}$ has expired.

10.3.8 FAILSAFE → INIT-state

Prerequisites

- FAILSAFE timer has expired.
- V_{VS} above $V_{PS,start}$

Triggering events

- Self triggered transition after the prerequisite is fulfilled.
- Valid ENA (edge) or WAK (level) signal (only needed if exception true)

Exceptions

- In case the FAILSAFE is entered three times in a row with the same failure the self-triggered transition is blocked.

Timing diagram

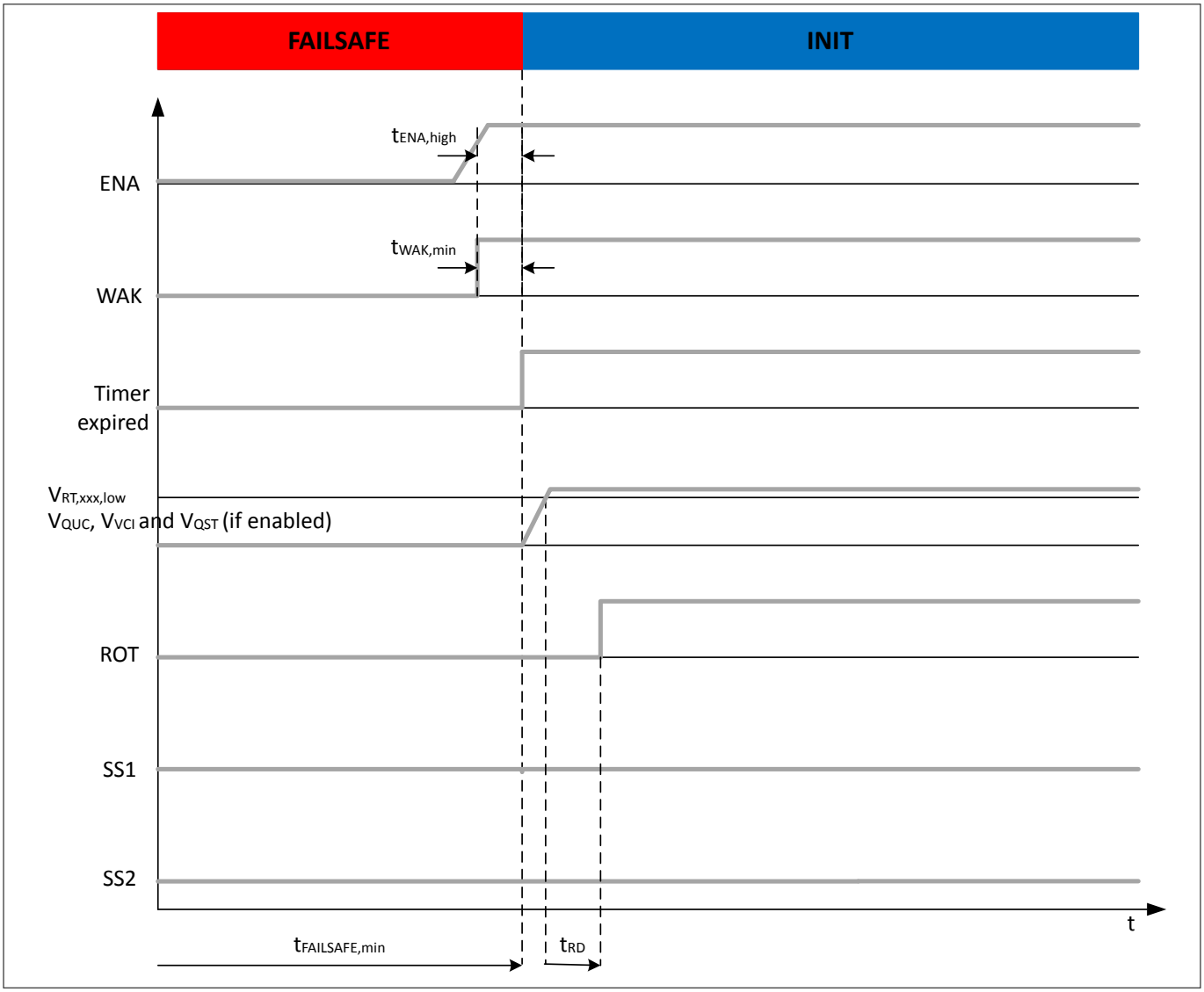


Figure 40 **Transition from FAILSAFE to INIT-state**

- The device transition from FAILSAFE-state to INIT-state happens earliest after the minimum FAILSAFE time $t_{FAILSAFE,min}$, which is 20 ms for all failures except a thermal shutdown. In case of a thermal shutdown the minimum FAILSAFE time $t_{FAILSAFE,min}$ is 1s. A command to transition before the minimum FAILSAFE time $t_{FAILSAFE,min}$ has expired, is not executed.
- After entering INIT-state the voltage regulators ramps up according to the power sequencing.
- The power on reset delay time is started as soon as the latest of the MCU related regulators V_{QUC}, V_{VCI} or V_{QST} (according to the previous configuration) crosses the related undervoltage reset threshold $V_{RT,xxx,low}$ on the way up.
- After the power on reset delay time has expired the reset (ROT) is set to HIGH.
- The device needs to be configured and initiated. All settings done in the configuration registers before the device went into FAILSAFE-state are lost, except the configuration of the QST (**RSYSPCFG0**) and the reset delay time (**DEVCFG1**).
- The safe state signal SS1 and SS2 are LOW in FAILSAFE-state and is LOW in INIT-state

10.4 Reaction on detected faults

Errors are classified according to their severity into 4 different error classes:

- Stay in Current State - Failures affecting peripherals without direct risk for the microcontroller, that are indicated by an interrupt to allow analysis by the microcontroller without changing the state.
- Move to INIT - Medium severity errors that brings the device back to INIT-state and generate a reset for the microcontroller.
- Move to FAILSAFE - Critical error with high risk of damaging the microcontroller.
- Move to POWERDOWN - Most critical error with high risk of damaging the device itself and the microcontroller

The error classes are overruled according to their severity, e.g. movement to POWERDOWN takes precedence over movement to FAILSAFE which takes precedence over movement to INIT.

The move to INIT, FAILSAFE and POWERDOWN errors are named "error triggered state transitions" in this document.

10.4.1 Stay in current state (Interrupt event)

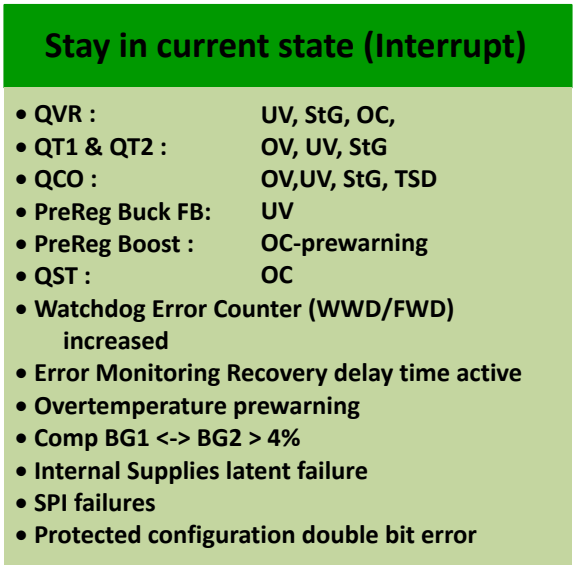


Figure 41 Stay in current state (Interrupt event)

The following failures does not trigger a movement of the device to another state by themselves, but indicates the failure by an interrupt event:

- Detection of undervoltage or a short to ground or overload detection at voltage reference, if in use
- Detection of overvoltage, undervoltage or a short to ground at trackers 1 or 2, if in use
- Detection of overvoltage, undervoltage, a short to ground or thermal shutdown at QCO, if in use
- Detection of undervoltage at step down pre regulator, if in use
- Detection of overcurrent prewarning of step up pre regulator, if in use
- Detection of overload at standby regulator, if in use
- Increase of window/functional watchdog error counter, but actual value still stays below the threshold
- Error monitoring recovery delay time is active and ERR signal stops toggling
- Thermal shutdown pre warning (Step down pre regulator or/and QUC or/and QCO), if in use (except for STANDBY and SLEEP state)

- Bandgap monitoring: If the deviation between both bandgaps is larger than 4% (except for STANDBY and SLEEP state)
- Detection of internal supplies latent failure
- SPI failures according to **SPISF**
- Protected configuration double bit error (CFGE)

The interrupt may not be visible on the INT pin in STANDBY and FAILSAFE-state due to microcontroller supplies being switched off. The event is stored in the status flags (**IF**, **SYSSF**, **MONSF0**, **MONSF1**, **MONSF2**, **OTWRNSF**, **OTFAIL**, **CEFUMON**).

10.4.2 Transition to INIT-state

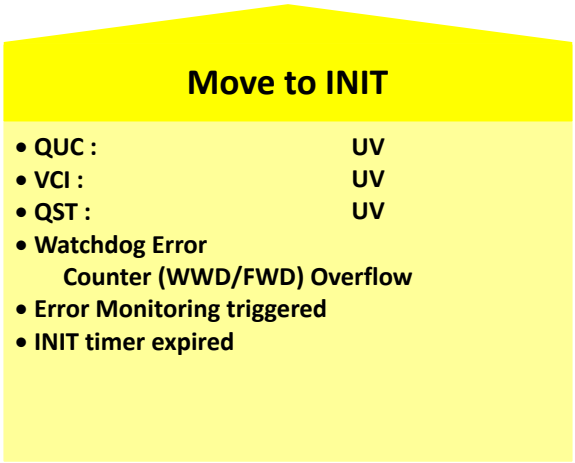


Figure 42 Move to INIT

The following failures moves the device from any state to INIT-state:

- Detection of undervoltage at QUC, VCI or QST, if in use
- Detection of window/functional watchdog error counter overflow
- Stop of error signal detected (immediate reaction mode) or stop or error signal detected for more than recovery delay time (recovery mode)
- One or two consecutive expires of the INIT timer (configuration in INIT-state failed). The initialization timer can be stopped by the MPS function described in Chapter 10.7.

10.4.2.1 INIT → INIT-state due to detected fault

10.4.2.1.1 INIT → INIT-state due to INIT timer expired for the first time

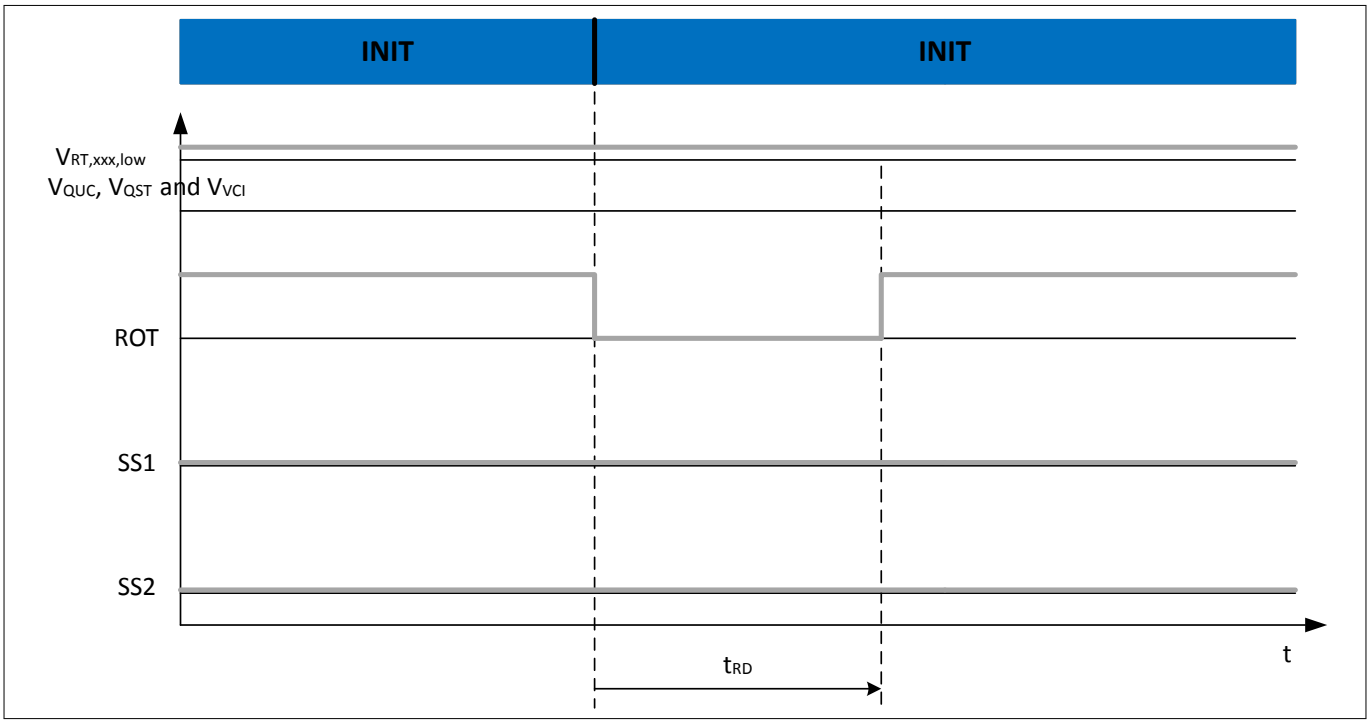


Figure 43 **Transition from INIT to INIT-state - first movement**

Description:

- The device transition from INIT to INIT-state (or stays in INIT-state) for the first time is issuing a "soft reset". Pin ROT is pulled to LOW for the reset delay time t_{RD} in case all MCU related voltages are in valid range. The power sequence is started after entering the INIT-state: the disabled outputs are re-activated, the other ones are kept enabled, except the QST keeps its configuration being ON or OFF.

10.4.2.1.2 INIT → INIT-state due to INIT timer expired for the second time

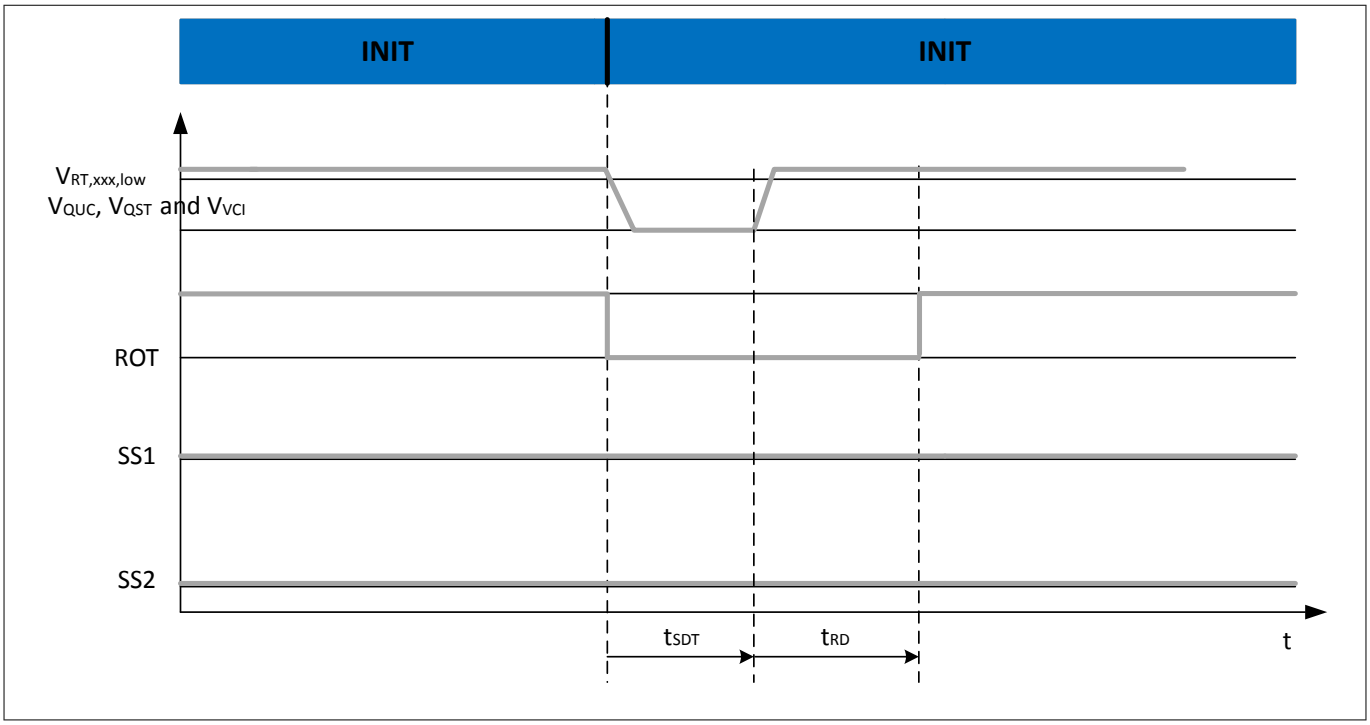


Figure 44 **Transition from INIT to INIT-state - second movement**

Description:

- The device transition from INIT to INIT-state (or stays in INIT-state) for the second time is issuing a "hard reset" - pin ROT is pulled to LOW and all outputs are disabled for the time *t* and restarted according to the power sequencing (Please refer to Chapter 7.3), except the QST restores its configuration being ON or OFF.
- The ROT pin is released according to the power sequencing using the reset delay time t_{rd}.

Note: *Please refer also to the transition INIT to FAILSAFE*

10.4.2.2 NORMAL → INIT-state due to detected fault

Timing diagram

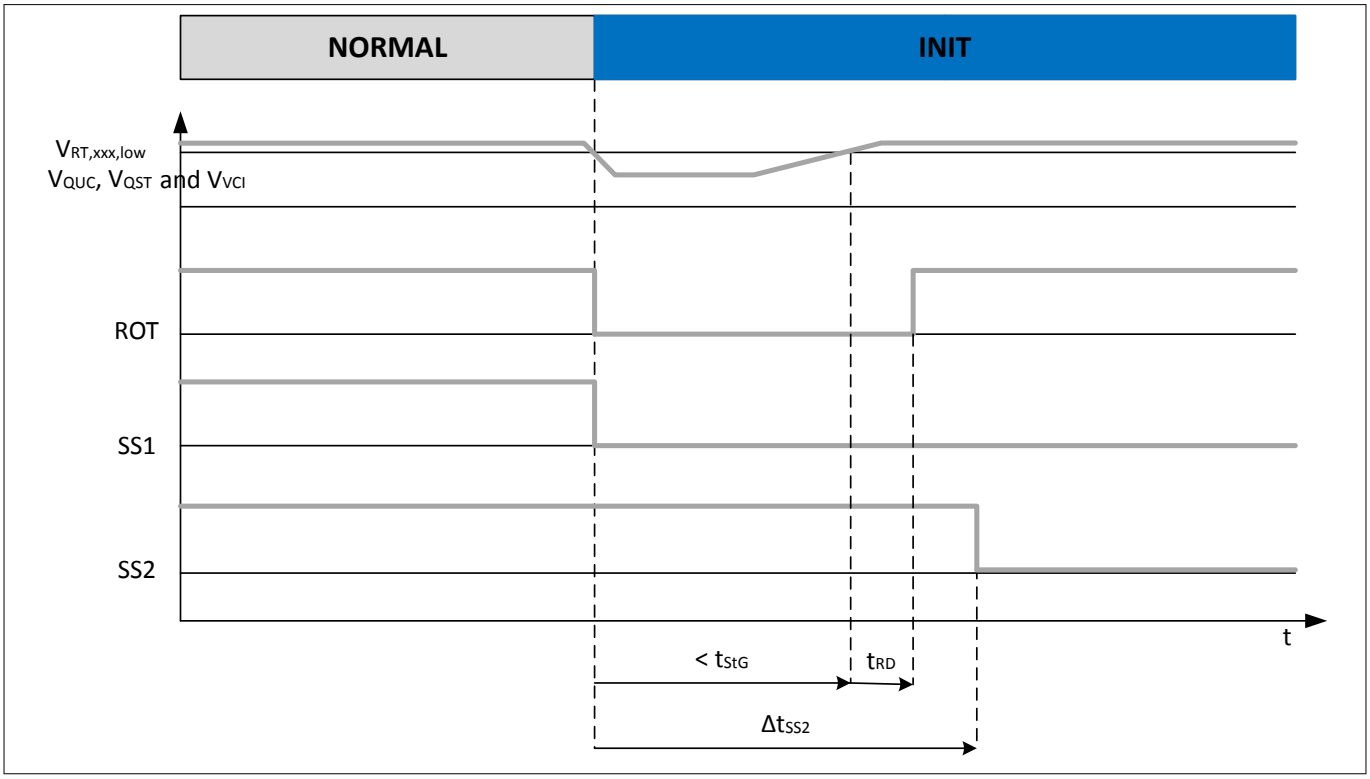


Figure 45 Transition from NORMAL to INIT-state

Description:

- The device transitions from NORMAL into INIT-state issuing a "soft reset" - pin ROT is pulled to LOW and all the outputs are enabled, except the QST keeps its configuration being ON or OFF. Outputs that where disabled in NORMAL-state get switched on again.
- This might be issued by an undervoltage of the MCU related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the figure. The undervoltage is shorter than the short to ground detection time t_{StG}. The reset delay time t_{RD} is started as soon as all MCU related voltages V_{QUC}, V_{QST} or V_{VCI} are back in the valid range. The ROT pin is released accordingly. An undervoltage longer than the short to ground detection time t_{StG} would first lead to a transition from NORMAL to INIT-state and then, after the short to ground detection time t_{StG} has expired, to a transition from INIT to FAILSAFE-state.
- The "soft reset" can also be initiated by a window watchdog error counter overflow (> ΣWWO), a functional watchdog error counter overflow (> ΣFWO), an error indication (immediate or recovery delay time mode), if these monitoring functions are in use. In this case the reset delay time t_{RD} is started at the falling edge of the ROT pin. Please consider the state transition time to INIT-state in Table 25.
- SS1 is pulled to LOW immediately with pin ROT, SS2 is pulled to LOW after the selected Δt_{SS2}.
- Please mind that in case of an UV event on QUC, a delayed SS2 signal will follow V_{QUC} as it is supplied from QUC.

Note: In case the device is sent back to NORMAL-state before the configured Δt_{SS2} has expired the SS2 is kept HIGH without being set to LOW.

10.4.2.3 STANDBY → INIT-state due to detected fault

Timing diagram

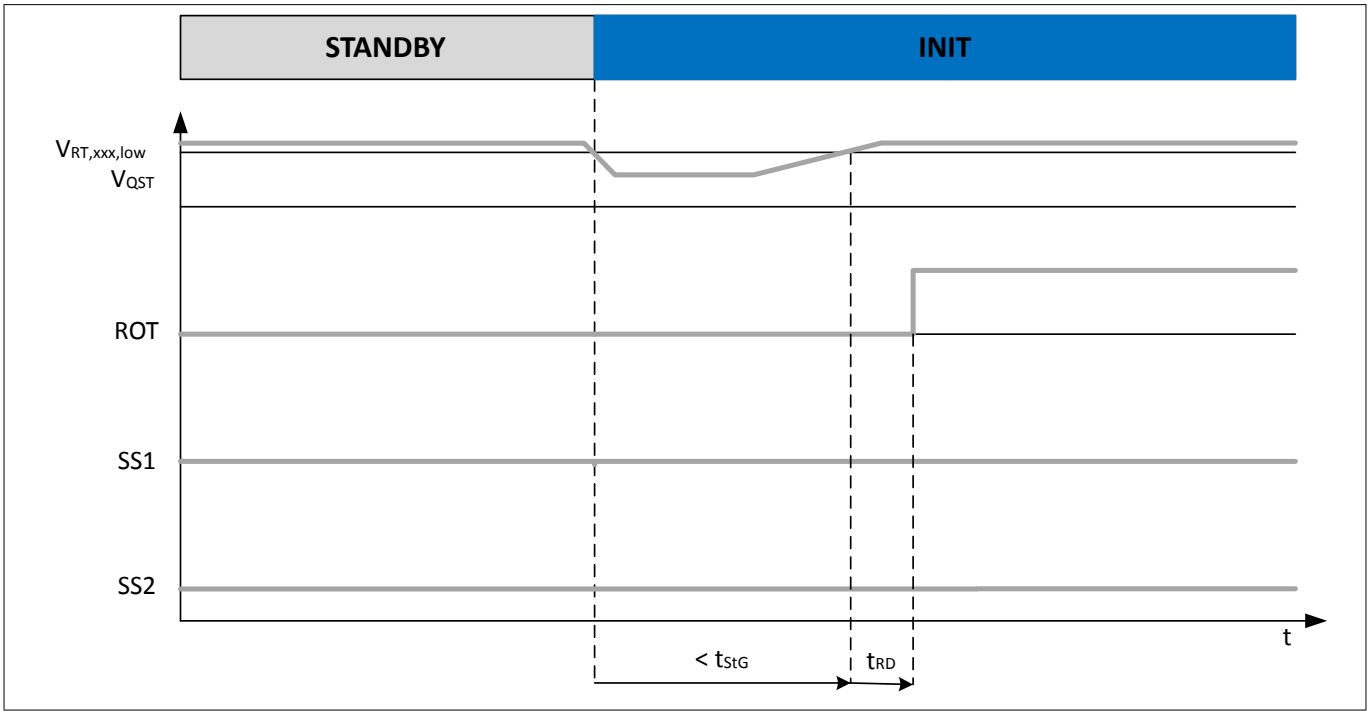


Figure 46 Transition from STANDBY to INIT-state

Description:

- The device transitions from STANDBY into INIT because of an undervoltage of the MCU related voltage V_{QST} as shown in the figure. The undervoltage is shorter than the short to ground detection time t_{StG}. An undervoltage longer than the short to ground detection time t_{StG} would first lead to a transition from STANDBY to INIT-state and then, after the short to ground detection time t_{StG} has expired, to a transition from INIT to FAILSAFE-state.
- The power sequence is started after entering the INIT-state: the disabled outputs are re-activated, except the QST keeps its configuration being ON or OFF.
- The power on reset delay time is started according to the power sequencing and releases the ROT accordingly.
- The safe state signals SS1 and SS2 are LOW in STANDBY-state and is LOW in INIT-state

Exception:

- Exception: In case of an over or undervoltage of the internal supply voltages a "hard reset" is always initiated. Please refer to Chapter 7.3.

10.4.2.4 SLEEP → INIT-state due to detected fault

Timing diagram

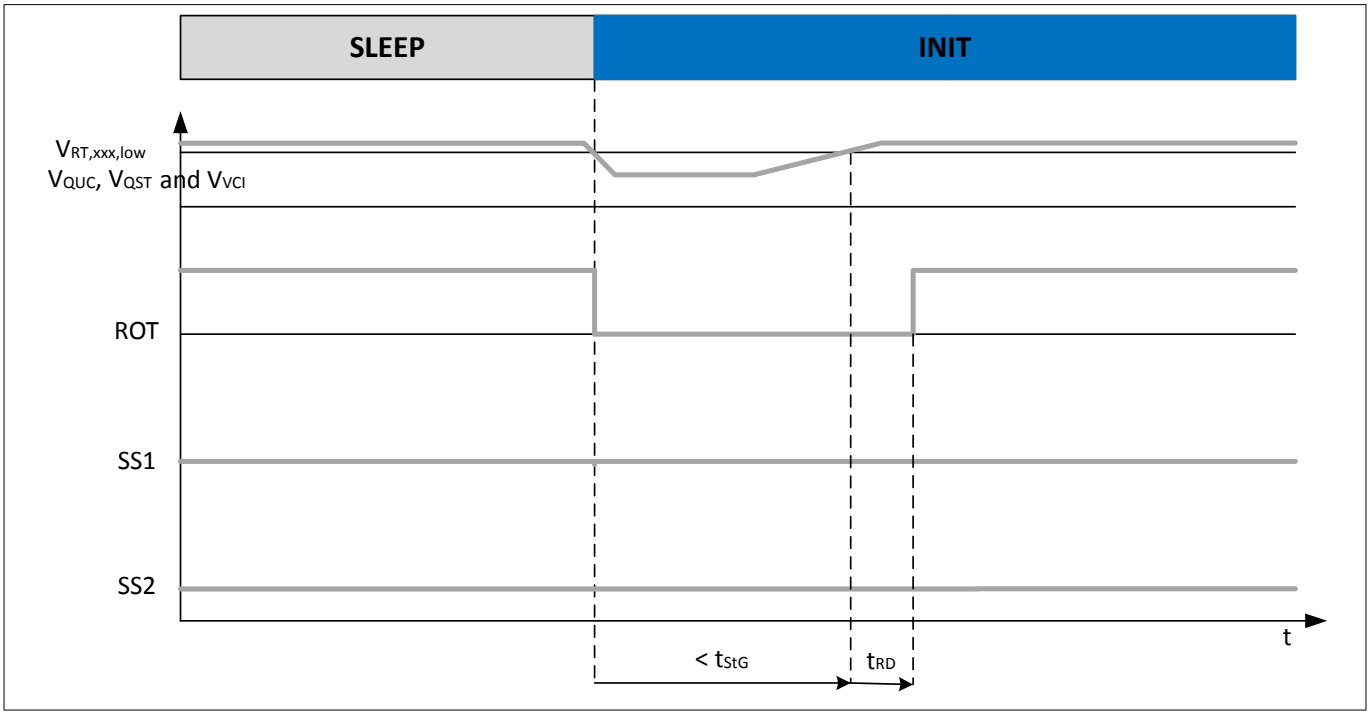


Figure 47 Transition from SLEEP to INIT-state

Description:

- The device transitions from SLEEP into INIT-state issuing a "soft reset" - pin ROT is pulled to LOW for a certain time t_{RD} and all the outputs are kept enabled. Outputs that where disabled in SLEEP-state get switched on again, except the QST keeps its configuration being ON or OFF.
- This might be issued by an undervoltage of the MCU related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the figure. The undervoltage is shorter than the short to ground detection time t_{StG}. The reset delay time t_{RD} is started as soon as all MCU related voltages V_{QUC}, V_{QST} or V_{VCI} are back in the valid range. The ROT pin is released accordingly. An undervoltage longer than the short to ground detection time t_{StG} would first lead to a transition from SLEEP to INIT-state and then, after the short to ground detection time t_{StG} has expired, to a transition from INIT to FAILSAFE-state
- The "soft reset" can also be initiated by a window watchdog error counter overflow (> ΣWWO), a functional watchdog error counter overflow (> ΣFWO), an error indication (immediate or recovery delay time mode), if these monitoring functions are in use. In this case the reset delay time t_{RD} is started at the falling edge of the ROT pin. Please consider the state transition time to INIT-state in Table 25.
- The safe state signals SS1 and SS2 are LOW in SLEEP-state and is LOW in INIT-state

Exception:

- Exception: In case of an over or undervoltage of the internal supply voltages a "hard reset" is always initiated. Please refer to Chapter 7.3.

10.4.2.5 WAKE → INIT-state due to detected fault

Timing diagram

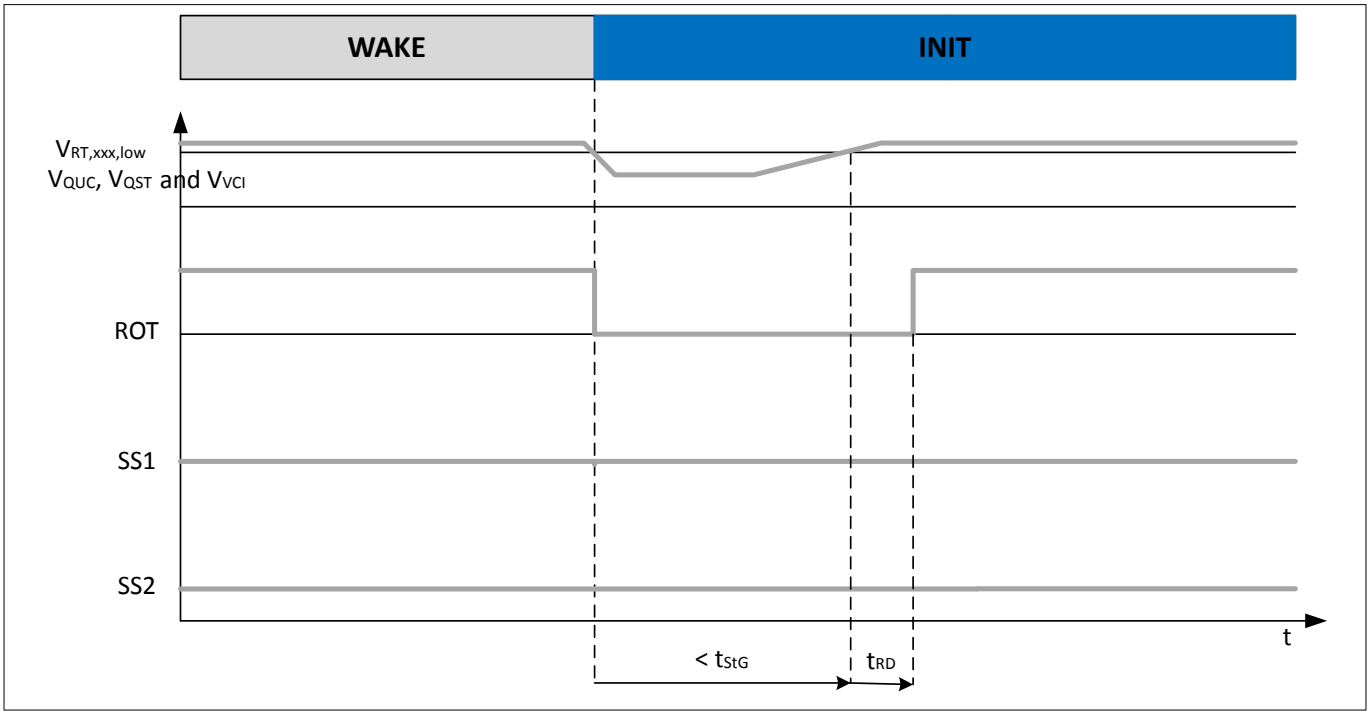


Figure 48 Transition from WAKE to INIT-state

Description:

- The device transitions from WAKE into INIT-state issuing a "soft reset" - pin ROT is pulled to LOW for a certain time t_{RD} and all the outputs are kept enabled. Outputs that where disabled in WAKE-state get switched on again, except the QST keeps its configuration being ON or OFF.
- This might be issued by an undervoltage of the MCU related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the figure. The undervoltage is shorter than the short to ground detection time t_{StG}. The reset delay time t_{RD} is started as soon as all MCU related voltages V_{QUC}, V_{QST} or V_{VCI} are back in the valid range. The ROT pin is released accordingly. An undervoltage longer than the short to ground detection time t_{StG} would first lead to a transition from WAKE to INIT-state and then, after the short to ground detection time t_{StG} has expired, to a transition from INIT to FAILSAFE-state.
- The "soft reset" can also be initiated by a window watchdog error counter overflow (> ΣWWO), a functional watchdog error counter overflow (> ΣFWO), an error indication (immediate or recovery delay time mode), if these monitoring functions are in use. In this case the reset delay time t_{RD} is started at the falling edge of the ROT pin. Please consider the state transition time to INIT-state in Table 25.
- The safe state signals SS1 and SS2 are LOW in WAKE-state is be LOW in INIT-state.

Exception:

- Exception: In case of an over or undervoltage of the internal supply voltages a "hard reset" is always initiated. Please refer to Chapter 7.3.

10.4.3 Transition to FAILSAFE-state

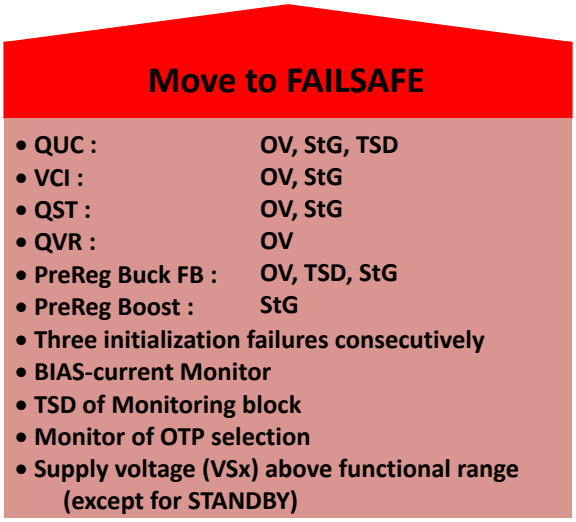


Figure 49 Move to FAILSAFE

The following failures move the device from any state to FAILSAFE-state:

- Detection of overvoltage, a short to ground at QUC, if in use
- Detection of thermal shutdown of QUC (except for STANDBY and SLEEP state)
- Detection of overvoltage or a short to ground at VCI or QST, if in use
- Detection of overvoltage at voltage reference, if in use
- Detection of overvoltage or short to ground (during start-up) at the step down pre regulator, if in use. Short to ground detection is only active during start-up phase in INIT-state until the output increases above the UV threshold and hysteresis.
- Detection of thermal shutdown of the step down pre regulator (except for STANDBY and SLEEP state)
- Detection of short to ground (long term operation in current limit) of the step up pre regulator, if in use
- Three consecutive initialization failures(e.g. configuration in INIT-state failed)
- A BIAS current monitor failure (except for STANDBY and SLEEP state)
- A overtemperature shutdown due to exceeded temperature in the monitoring block (except for STANDBY and SLEEP state)
- A OTP selection monitor failure due to wrong and not correctable reading of internal one-time-programmed(OTP) information for trimming and output voltage configurations.
- An overvoltage at the supply pins (VSx) triggers the overvoltage protection and moves the device into FAILSAFE-state (except for STANDBY-state)

10.4.3.1 INIT → FAILSAFE-state due to detected fault

Timing diagram

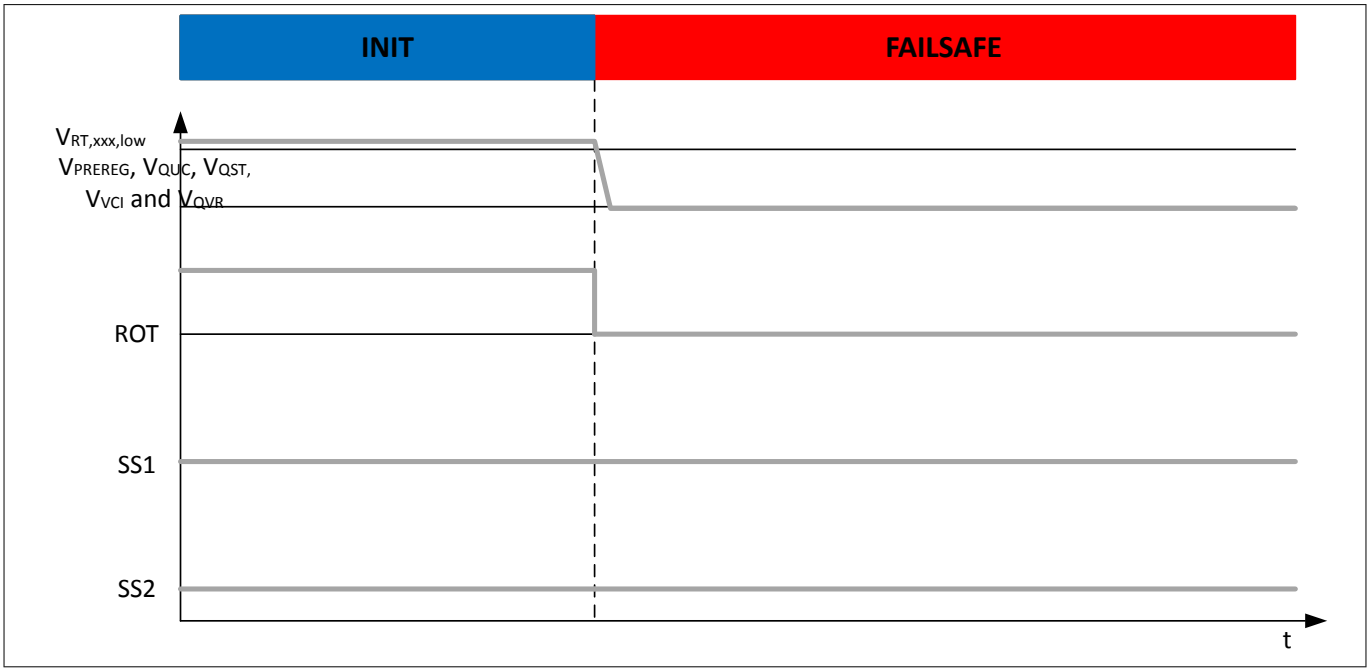


Figure 50 Transition from INIT to FAILSAFE-state

Description:

- The transition from INIT-state into FAILSAFE-state is initiated by any failure (external or internal) case mentioned in Chapter 10.4.3.
- Pin ROT is pulled to LOW as soon as one of the "Move to FAILSAFE" failures is detected, if is not already LOW due to an undervoltage on a MCU related regulator.
- All regulators are switched off, when the device turns from INIT into FAILSAFE-state, regardless if they are in overvoltage condition or not.
- The safe state signals SS1 and SS2 are LOW in INIT-state and are LOW in FAILSAFE-state.

10.4.3.2 XXXX → INIT → FAILSAFE-state due to detected fault

Timing diagram

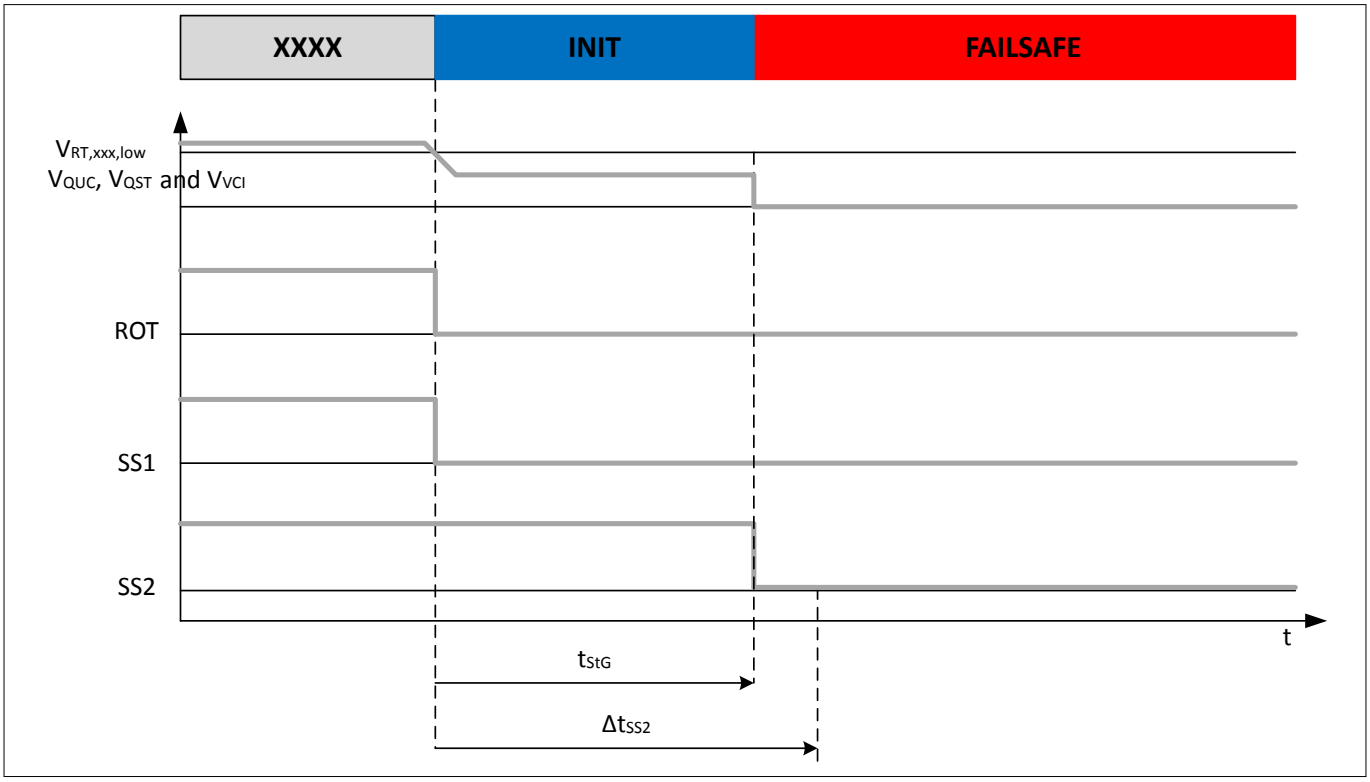


Figure 51 **Transition from XXXX to INIT to FAILSAFE-state after detection of short to ground**

Description:

- The detection of an undervoltage of the MCU related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the figure initiates the transition into INIT-state. (please refer to previous chapter Transition into INIT-state)
- Pin ROT is pulled to LOW as soon as the undervoltage is detected
  (at one or more of the regulators mentioned above - whichever is the first)
- The safe state signal SS1 is pulled to LOW together with pin ROT going to low
- If the short to ground maintains for longer than the short to ground detection time t_{StG} a short to ground event is detected.
- All regulators are switched off as soon as the short to GND is detected, regardless if they are in undervoltage condition or not.
- The device moves from INIT-state to FAILSAFE-state
- The safe state signal SS2 is pulled to LOW together with the transition from INIT to FAILSAFE-state, even if the delay time Δt_{SS2} has not expired yet, because QUC is switched off (QUC is switched on in INIT-state, but switched off in FAILSAFE-state).

10.4.3.3 NORMAL → FAILSAFE-state due to detected fault

Timing diagram

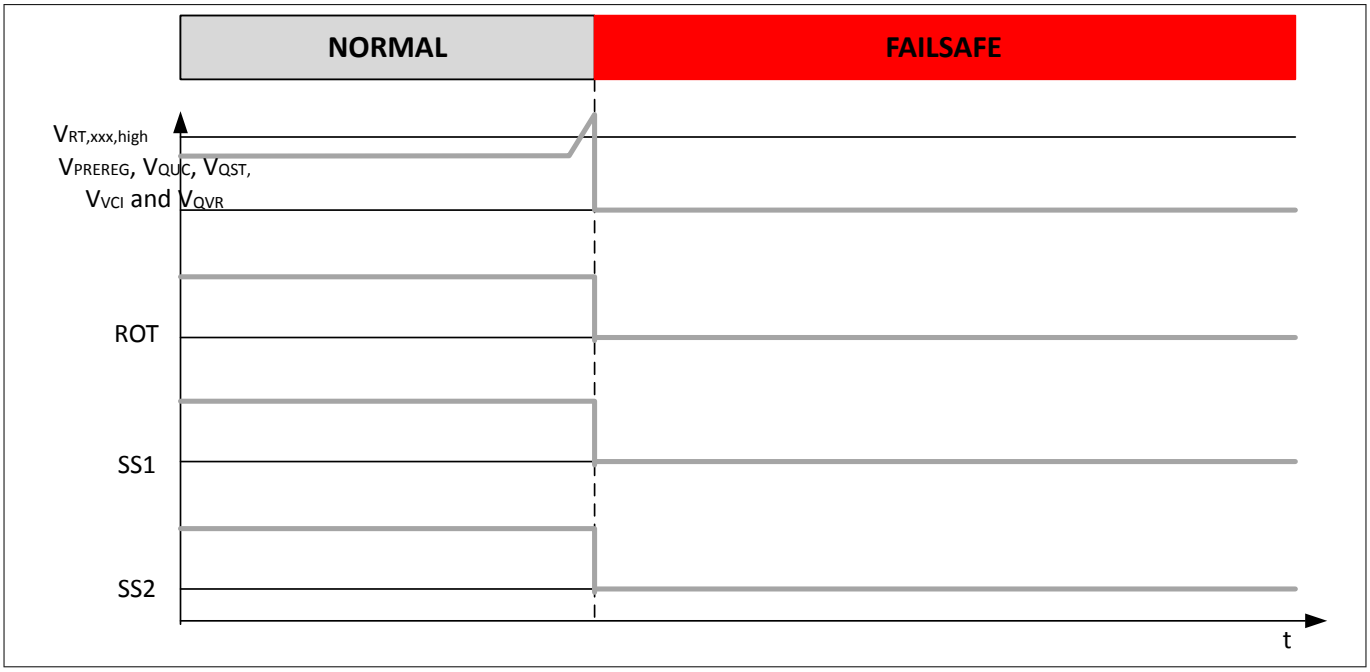


Figure 52 Transition from NORMAL to FAILSAFE-state

Description:

- The detection of an overvoltage of the pre regulator voltage V_{PREREG} or the MCU related voltages V_{QUC}, V_{QST}, V_{VCI} or V_{QVR} as shown in the figure initiates the transition from NORMAL-state to FAILSAFE-state.
- Pin ROT is pulled to LOW as soon as the overvoltage event is detected (at one or more of the regulators mentioned above - whichever is the first).
- All regulators are switched off, when the device turns from NORMAL into FAILSAFE-state, regardless if they are in overvoltage condition or not.
- The safe state signals are pulled to LOW immediately with pin ROT going to low, because the QUC is switched off.
- The transition from NORMAL-state into FAILSAFE-state is initiated by any failure (external or internal) case mentioned in Chapter 10.4.3.
- The detection of a short to ground of the MCU related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the Figure 51 is first detected as an undervoltage event and move the device from NORMAL-state to INIT-state. After the short to ground detection time t_{StG} the device then moves from INIT-state to FAILSAFE-state (please refer to transition from INIT-state to FAILSAFE-state).

10.4.3.4 STANDBY → FAILSAFE-state due to detected fault

Timing diagram

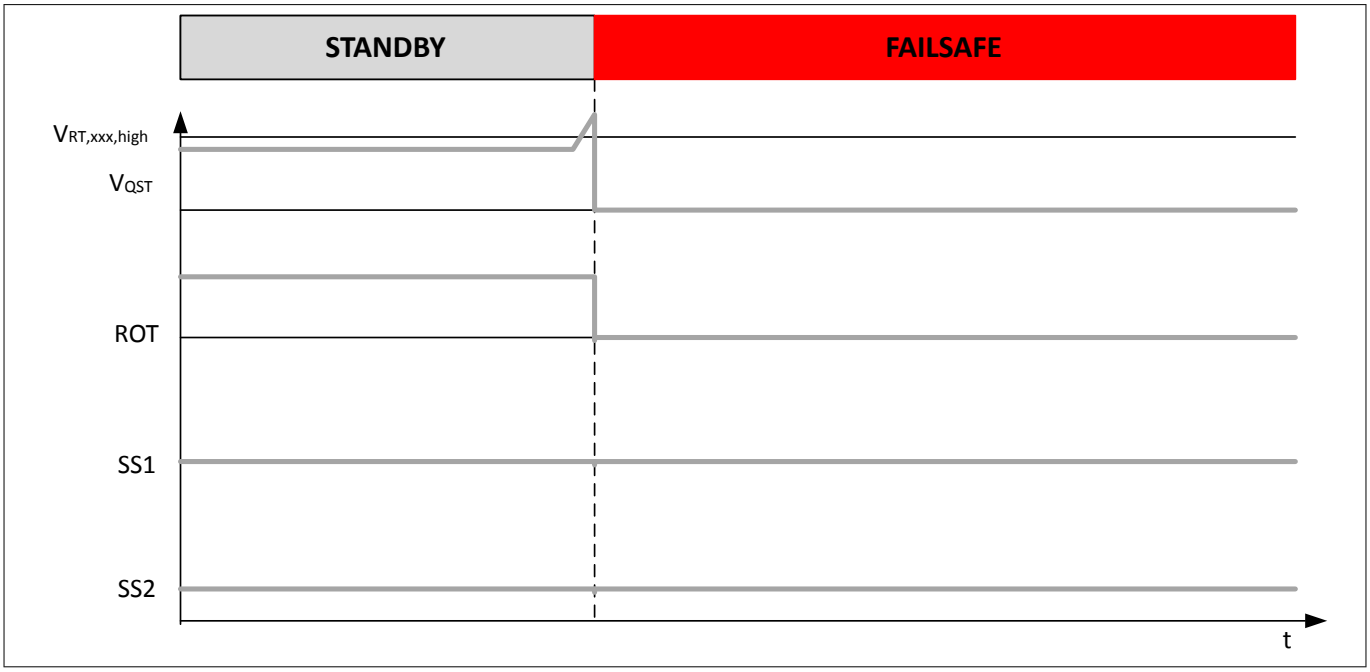


Figure 53 Transition from STANDBY to FAILSAFE-state

Description:

- The detection of an overvoltage of the MCU related voltage V_{QST} as shown in the figure initiates the transition from STANDBY-state to FAILSAFE-state.
- Pin ROT is LOW in STANDBY-state and stays LOW in FAILSAFE-state.
- The safe state signals SS1 and SS2 are LOW in STANDBY-state and are LOW in FAILSAFE-state.
- The detection of a short to ground of the MCU related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the Figure 51 is first detected as an undervoltage event and move the device from STANDBY-state to INIT-state. After the short to ground detection time t_{StG} the device then moves from INIT-state to FAILSAFE-state (please refer to transition from INIT-state to FAILSAFE-state).

10.4.3.5 SLEEP → FAILSAFE-state due to detected fault

Timing diagram

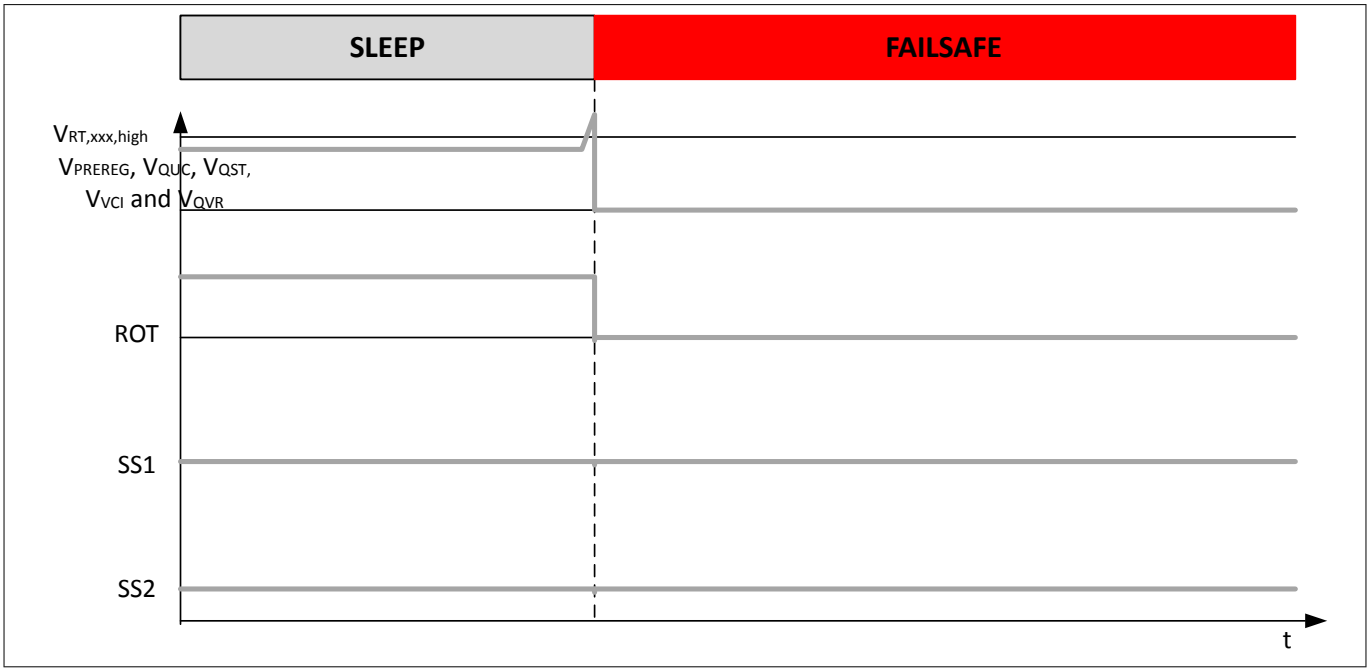


Figure 54 Transition from SLEEP to FAILSAFE-state

Description:

- The detection of an overvoltage of the pre regulator voltage V_{PREREG} or the MCU related voltages V_{QUC}, V_{QST}, V_{VCI} or V_{QVR} as shown in the figure initiates the transition from SLEEP-state to FAILSAFE-state.
- Pin ROT is pulled to LOW as soon as the overvoltage event is detected (at one or more of the regulators mentioned above - whichever is the first).
- All regulators are switched off, when the device turns from SLEEP into FAILSAFE-state., regardless if they are in overvoltage condition or not.
- The safe state signals stay at LOW as in the SLEEP-state.
- The transition from SLEEP-state into FAILSAFE-state is initiated by any failure (external or internal) case mentioned in Chapter 10.4.3.
- The detection of a short to ground of the MCU related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the Figure 51 is first detected as an undervoltage event and move the device from SLEEP-state to INIT-state. After the short to ground detection time t_{StG} the device then moves from INIT-state to FAILSAFE-state (please refer to transition from INIT-state to FAILSAFE-state).

10.4.3.6 WAKE → FAILSAFE-state due to detected fault

Timing diagram

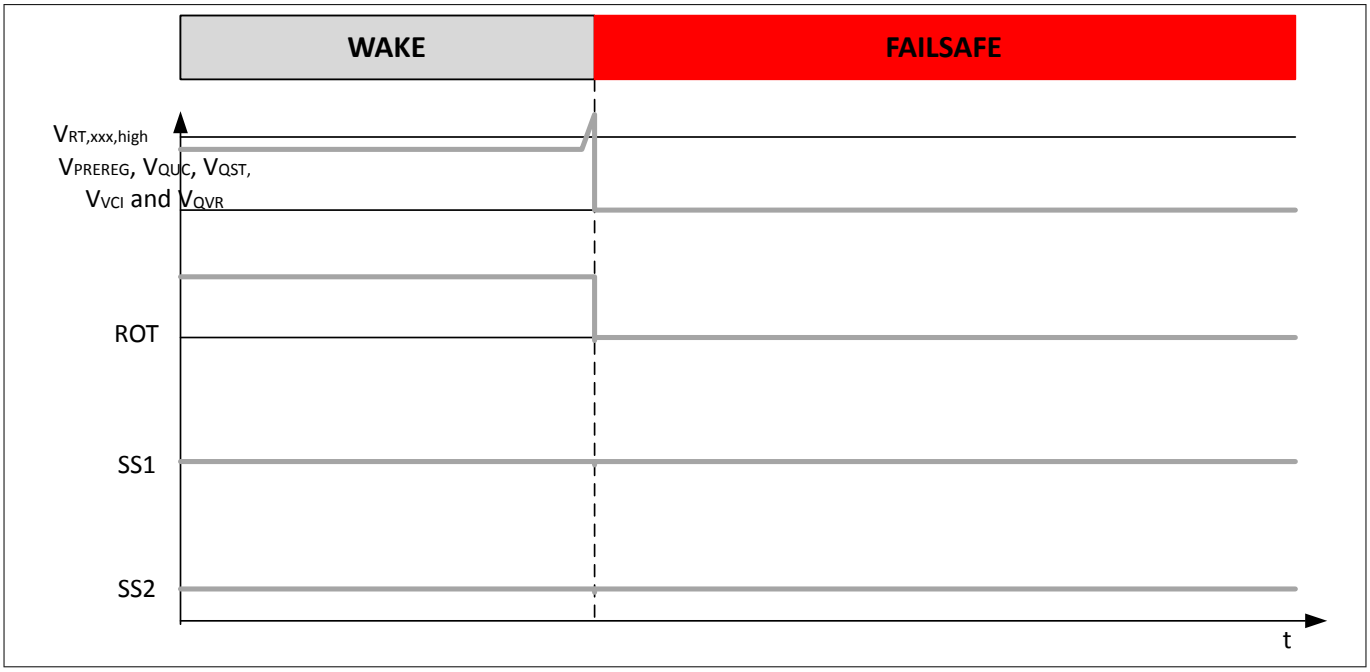


Figure 55 Transition from WAKE to FAILSAFE-state

Description:

- The detection of an overvoltage of the pre regulator voltage V_{PREREG} or the MCU related voltages V_{QUC}, V_{QST}, V_{VCI} or V_{QVR} as shown in the figure initiates the transition from WAKE-state to FAILSAFE-state.
- Pin ROT is pulled to LOW as soon as the overvoltage event is detected (at one or more of the regulators mentioned above - whichever is the first).
- All regulators are switched off, when the device turns from WAKE into FAILSAFE-state., regardless if they are in overvoltage condition or not.
- The safe state signals stay at LOW as in the WAKE-state.
- The transition from WAKE-state into FAILSAFE-state is initiated by any failure (external or internal) case mentioned in Chapter 10.4.3.
- The detection of a short to ground of the MCU related voltages V_{QUC}, V_{QST} or V_{VCI} as shown in the Figure 51 is first detected as an undervoltage event and move the device from WAKE-state to INIT-state. After the short to ground detection time t_{StG} the device then moves from INIT-state to FAILSAFE-state (please refer to transition from INIT-state to FAILSAFE-state).

10.4.3.7 Transition to FAILSAFE-state due to thermal shutdown

Timing diagram

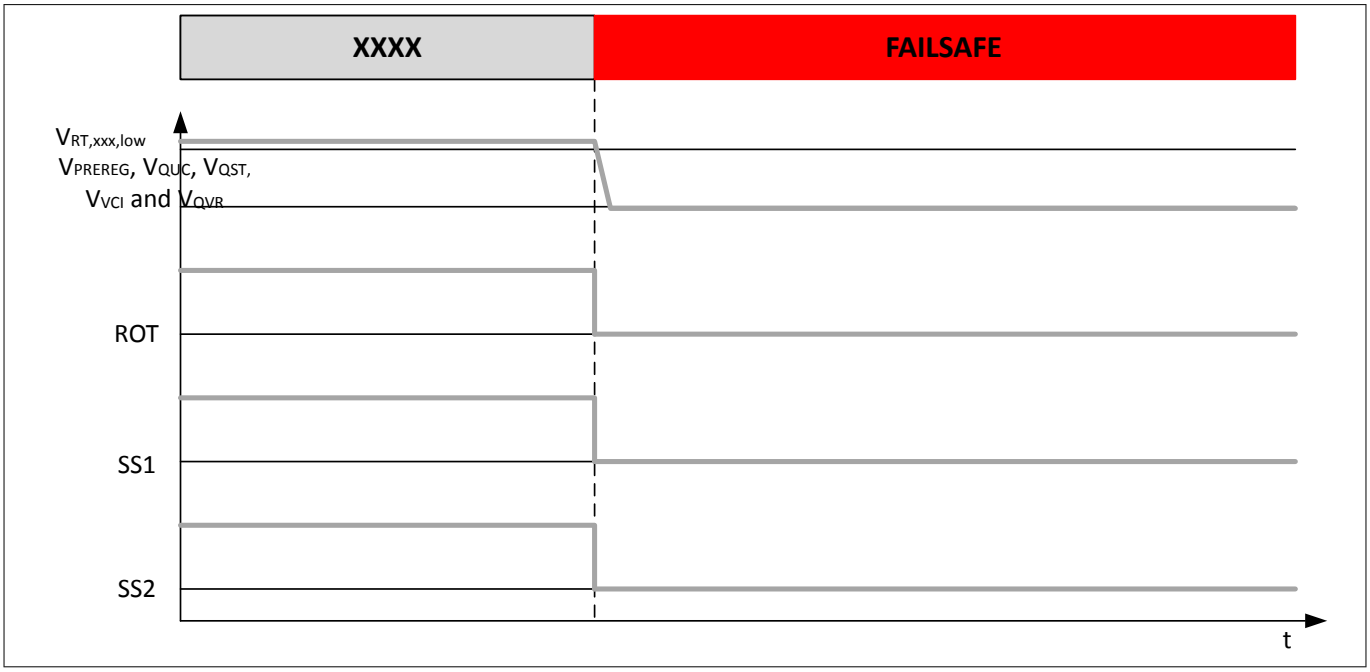


Figure 56 Transition to to FAILSAFE-state due to thermal shutdown

Description:

- The transition from any state into FAILSAFE-state is initiated by a thermal shutdown (TSD).
- Pin ROT is pulled to LOW as soon as the thermal shutdown is detected.
- All regulators are switched off, when the device turns from xxx into FAILSAFE-state. regardless if they are in overtemperature condition or not
- Out of NORMAL-state the safe state signals SS1 and SS2 are pulled to LOW immediately with pin ROT going to low, because the QUC is switched off. Out of any other state the safe state signals SS1 and SS2 are LOW and stay low.
- The device stays in FAILSAFE-state after a thermal shutdown (TSD) at least for 1 s.

10.4.4 Transition to POWERDOWN

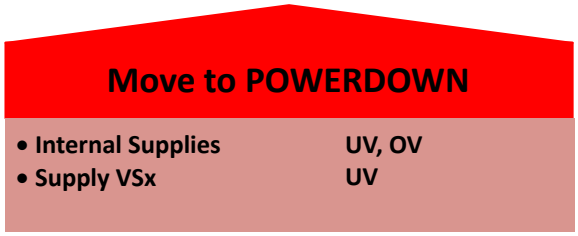


Figure 57 Move to POWERDOWN

The following failures/events move the device always with highest priority to POWERDOWN:

- V_{VS} below $V_{PD,lo,min}$ when decreasing
- Detection of over- or undervoltage on internal supplies

10.5 Electrical characteristics state machine

Table 25 Electrical characteristics state machine

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
INIT timer / Initialization time-out	t_{INIT}	550	600	650	ms	–	P_11.5.1
FAILSAFE time	$t_{FAILSAFE,min}$	18	20	22	ms	–	P_11.5.2
FAILSAFE time TSD	$t_{FAILSAFE,min}$	0.9	1	1.1	s	for thermal shutdown TSD	P_11.5.3
Transition delay timer accuracy	$t_{tr,del}$	-20	–	+20	%	[35] Configurable value **DEVCFG0**.TRDEL	P_11.5.4
QUC current monitoring for low power states	$I_{QUC,att}$	-30	–	+30	%	Configurable value **DEVCFG2**.CTHR ; $V_{PREREG} > V_{QUC} + V_{dr,QUC}$	P_11.5.5
State transition time	t_{tr}	–	–	100	µs	except transitions to SLEEP, to STANDBY [36] or from STANDBY	P_11.5.6
State transition time to INIT	$t_{tr,INIT}$	–	–	200	µs	valid for "Move to INIT" events excluding transitions from STANDBY, FAILSAFE and POWERDOWN	P_11.5.7
State transition time to INIT	$t_{tr,INIT}$	–	–	250	µs	valid for transitions from STANDBY, FAILSAFE and interrupted transition to STANDBY	P_11.5.8

35 Due to internal delays the transition delay time can be enlarged by max 30 µs.
36 For transition times into SLEEP or STANDBY please refer to the transition delay timer configurable by register DEVCFG0.TRDEL and its accuracy specified in Table 25.

10.6 Built In Self Test (BIST) features

TLF35585QV provides the option to test certain observation functions with the assistance of the external MCU via built in self-test features. These features are described in the following chapters.

10.6.1 Analog Built In Self Test (ABIST)

TLF35585QV provides the option to test the comparator and evaluation logic related to the monitoring functions contributing to the activation of the secondary safety shutdown path and the generation of an interrupt. Further on additional comparators and evaluation logic related to the Safe State Control itself can be tested (SSC overvoltage watchdog and toggling monitor). This is accomplished via an internal ABIST controller which performs tests on each comparator generating artificial undervoltage and overvoltage (or current) conditions, is checking the result and generates the information which needs to be evaluated by the MCU to judge, if the ABIST operation has been performed successfully or not.

The following status information on ABIST operation is generated by the system:

- In case an ABIST operation has been requested by the MCU, a status is provided after the ABIST has been performed (**ABIST_CTRL0**.STATUS). This status needs to be evaluated by the MCU. The provided status is just a GO-NOGO information, which means information about a particularly tested path is provided. The basic comparator function is tested, but not the respective threshold values.

The test of the monitoring and safety relevant output functions is run on three different areas in the system:

- The functionality of a comparator and its corresponding deglitching logic can be tested by a "comparator only" test. This test is performed by generating the failure condition for a time shorter than the deglitching time, accordingly the secondary safety shutdown path nor the interrupt is triggered due to the detected failure. During this test only the selected comparator(s) are tested. In case more than one comparator is selected, the test is performed with a fixed sequence of comparators to be tested. The completion of the test is indicated by an interrupt.
- The functionality of a comparator including its corresponding deglitching logic and the contribution to the respective safety measure can be tested. The safety measure is either the activation of the secondary safety shutdown path or the generation of an interrupt. This test is performed in a time longer than the deglitching time.
- While the device provides information about the status for the first and the second ABIST, further microcontroller cooperation is required for the third area. The MCU is responsible to check if the secondary safety shutdown path has been activated successfully (SS1/SS2 are set low) or an interrupt event has been detected by the MCU.

10.6.1.1 How to run the ABIST

During ABIST, servicing of the watchdog(s) and error monitoring is required to be performed according to the configuration by the microcontroller. Error in not doing so will lead to failure events in these functions and will lead to the assertion of interrupt, reset or safe state output events accordingly, which is disturbing the proper analysis of the ABIST results. Optionally watchdog functionality and/or error monitoring can be disabled during ABIST operation via a protected register access. In this case, no servicing is required.

During a performed ABIST including the deglitching logic the FLAG registers (**SYSFAIL**, **INITERR**, **IF**) as well as the status information (**MONSF1**, **MONSF2**, **MONSF3**) are triggered and updated by out of range conditions caused by the ABIST functionality, which has to be considered beside the results provided in the ABIST related registers (**ABIST_CTRL0** to **ABIST_SELECT2**).

During the time, when the ABIST is performed by internal hardware, the assertion of ROT due to the occurrence of any event which is supposed to trigger the respective action and is part of the logic which is affected by the ABIST control is blocked. In addition, the state machine does not change its state according to the reaction on detected faults described in Chapter 10.4. In case an ABIST contributing to the secondary safety shutdown path is started and the device is in NORMAL-state, the state machine moves from NORMAL to WAKE-state. Furthermore, all voltages are kept enabled regardless of any out of range detection caused by ABIST itself.

The test of a single functionality is basically always performed in the same way:

- All comparators are assumed to be enabled in case they are selected to be tested, while this is true for any MCU related voltage it might not be the case for non MCU related voltages. Accordingly, configurable supplies have to be enabled before they can be tested. On the other hand the ABIST test on a comparator which is not used by the system is not required to be performed.
- The comparators to be tested shall be selected by setting the individual bit(s) in the respective register(s) (**ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**). For this selection it is necessary to differentiate by the contribution to the different safety measure. The differentiation can be derived from Table 26.
- The microcontroller shall configure the register **ABIST_CTRL0** according to the functionality to be tested. The configuration consist of the tested safety measure (**ABIST_CTRL0**.INT), the tested area/coverage by the ABIST (**ABIST_CTRL0**.PATH) and the configuration whether a sequence or a single comparator shall be tested (**ABIST_CTRL0**.SINGLE).
- The microcontroller shall set the global ABIST start bit (**ABIST_CTRL0**.START) to start the ABIST.The global ABIST start bit shall be read by the MCU. If this bit is still set, ongoing ABIST functionality is performed. Upon completion of the selected ABIST operation(s) the start bit is cleared and an interrupt event is generated.Each bit which has been set to select the test of a dedicated comparator (**ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**) is cleared once a successful ABIST operation has been performed on the particular comparator. Each bit which has been set to select the test of a dedicated comparator is kept unchanged if the ABIST operation on this particular comparator has not been performed successfully.

In this way the MCU can determine which comparator failed in case the ABIST status information shows a failing ABIST operation.

Table 26 Contribution of comparators to safety measures

Comparator	Secondary safety shutdown Path	Interrupt	ABIST_Select register bit
QUC Overvoltage	X		**ABIST_SELECT0**.UCOV
Core_Sup Overvoltage	X		**ABIST_SELECT0**.VCOREOV
QST Overvoltage	X		**ABIST_SELECT0**.STBYOV
QVR Overvoltage	X		**ABIST_SELECT0**.VREFOV
PreReg Overvoltage	X		**ABIST_SELECT0**.PREGOV

(table continues...)

Table 26 (continued) Contribution of comparators to safety measures

Comparator	Secondary safety shutdown Path	Interrupt	ABIST_Select register bit
QUC Undervoltage	X		**ABIST_SELECT1**.UCUV
Core_Sup Undervoltage	X		**ABIST_SELECT1**.VCOREUV
QST Undervoltage	X		**ABIST_SELECT1**.STBYUV
BIAS current low	X		**ABIST_SELECT2**.BIASLOW
BIAS current high	X		**ABIST_SELECT2**.BIASHI
Supply VS Overvoltage	X		**ABIST_SELECT2**.VBATOV
Tracker 1 Overvoltage		X	**ABIST_SELECT0**.TRK1OV
Tracker 2 Overvoltage		X	**ABIST_SELECT0**.TRK2OV
QCO Overvoltage		X	**ABIST_SELECT0**.COMOV
QVR Undervoltage		X	**ABIST_SELECT1**.VREFUV
Tracker 1 Undervoltage		X	**ABIST_SELECT1**.TRK1UV
Tracker 2 Undervoltage		X	**ABIST_SELECT1**.TRK2UV
QCO Undervoltage		X	**ABIST_SELECT1**.COMUV
Pre_Reg Undervoltage		X	**ABIST_SELECT1**.PREGUV
V_{BG1} - 4% ≤ V_{BG2}		X	**ABIST_SELECT2**.BG12UV
V_{BG1} + 4% ≥ V_{BG2}		X	**ABIST_SELECT2**.BG12OV

10.6.1.2 Testing the comparator logic only

During the ABIST operation the comparators are triggered by the ABIST controller for a time shorter than the internal deglitching time t_{rr} (reset reaction time). A properly working comparator signals an out of range condition to its output for the time the failure condition is applied.

The provided information of each comparator is checked against the expected value. If the comparator output value matches the expected value this is considered as a passing test by the ABIST controller. If any of the provided output values do not match the expected value, this is considered as a failing test. The general result of the ABIST is provided by the STATUS in the register **ABIST_CTRL0**. The detailed result for each selected comparator can be checked by the registers **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**. In case the previously selected bits are reset after the test is finished, it can be considered as pass. A bit which is still set, would indicated the failing comparator(s), that makes the overall STATUS to be failed.

Accordingly the maximum selection[37] (including possible ones) for the comparator test would be the following:

Secondary safety shutdown path (SS1/2) related:

- **ABIST_SELECT0**: 00101111_B ($2F_H$)
- **ABIST_SELECT1**: 00001110_B ($0E_H$)
- **ABIST_SELECT2**: 11000001_B ($C1_H$)
- Start of the test by **ABIST_CTRL0**: 00000001_B (01_H)

Interrupt (INT) related:

- **ABIST_SELECT0**: 11010000_B ($D0_H$)
- **ABIST_SELECT1**: 11110001_B ($F1_H$)
- **ABIST_SELECT2**: 00110000_B (30_H)
- Start of the test by **ABIST_CTRL0**: 00001001_B (09_H)

This type of ABIST can be performed in the following states of the State machine: INIT, NORMAL, WAKE. In case of an successful ABIST there shall be no reaction of secondary safety shutdown path SS1/2 and only an interrupt generated due to the finished ABIST (**IF**.ABIST set and **IF**.MON not set, considering cleared interrupt flags prior to the ABIST and no real failure events during the ABIST).

37 Please mind that for a test of a comparators the corresponding output has to be enabled.

10.6.1.3 Testing the comparator logic and the corresponding deglitching logic

During the ABIST operation the comparators are triggered by the ABIST controller for a time longer than the internal deglitching time t_{rr} (reset reaction time). A properly working comparator signals an out of range condition to its output for the time the failure condition is applied. The deglitching logic forwards the failure trigger after t_{rr} and makes the device react on the recognized failure event. This reaction consists the storage of the respective monitoring failure flags and as well the triggering of the respective output function, which is either the interrupt INT or the secondary safety shutdown path SS1/2. The reaction of the safe state outputs SS1/2 can only be observed in case the test is started in NORMAL-state.

Furthermore the provided information of each deglitching logic output is checked against the expected value. If the deglitching logic output value matches the expected value this is considered as a passing test by the ABIST controller. If any of the provided output values do not match the expected value, this is considered as a failing test. The general result of the ABIST is provided by the STATUS in the register **ABIST_CTRL0**. The detailed result for each selected comparator can be checked by the registers **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2**. In case the previously selected bits are reset after the test is finished, it can be considered as pass recognized by the ABIST controller. A bit which is still set, would indicated the failing comparator(s), that makes the overall STATUS to be failed.

Beside the results read from the ABIST controller related registers, the result provided in the failure/interrupt flags (**SYSFAIL**, **INITERR** and **IF**) and monitoring status flags (**MONSF1**, **MONSF2** or **MONSF3**) have to be read and checked by the microcontroller against the expected result considering the configuration set before the start of the ABIST.

The maximum selection[38)] for the comparator and deglitching logic test would be the following:

Secondary safety shutdown path (SS1/2) related:

- **ABIST_SELECT0**: 00101111_B ($2F_H$)
- **ABIST_SELECT1**: 00001110_B ($0E_H$)
- **ABIST_SELECT2**: 11000001_B ($C1_H$)
- Start of the test by **ABIST_CTRL0**: 00000011_B (03_H)

Interrupt (INT) related:

- **ABIST_SELECT0**: 11010000_B ($D0_H$)
- **ABIST_SELECT1**: 11110001_B ($F1_H$)
- **ABIST_SELECT2**: 00110000_B (30_H)
- Start of the test by **ABIST_CTRL0**: 00001011_B ($0B_H$)

38 Please mind that for a test of a comparators the corresponding output has to be enabled.

The analysis based on the maximum possible selection would consist the following:

Secondary safety shutdown path (SS1/2) related:

- **IF**: 01000000_B (40_H)
- **INITERR**: 00000100_B (04_H)
- **SYSFAIL**: 00000100_B (04_H)
- **MONSF1**: 00101111_B ($2F_H$)
- **MONSF2**: 00001110_B ($0E_H$)
- **MONSF3**: 11000001_B ($C1_H$)
- Start of the test by **ABIST_CTRL0**: 00000011_B (03_H)

Interrupt (INT) related:

- **IF**: 01001000_B (48_H)
- **INITERR**: 00000000_B (00_H)
- **SYSFAIL**: 00000000_B (00_H)
- **MONSF1**: 11010000_B ($D0_H$)
- **MONSF2**: 11110001_B ($F1_H$)
- **MONSF3**: 00110000_B (30_H)
- Start of the test by **ABIST_CTRL0**: 00001011_B ($0B_H$)

This type of ABIST can be performed in the following states of the State machine: INIT, WAKE, NORMAL. If this test is run in NORMAL-state on comparators contributing to the secondary safety shutdown path the device switches low the safe state outputs SS1/2 and the State machine moves to WAKE-state, without triggering a reset ROT.

It has to be considered that testing the complete monitoring chain till the respective output (SS1/2 or INT) in this way covers only the first comparator in the sequence, as this one triggers the output reaction. For further details, please refer to Chapter 10.6.1.4.

If this test is run in INIT or WAKE-state, contribution to activation of the secondary safety shutdown path cannot be tested. The system is in a safe state already and the secondary safety shutdown path is already activated.

In any way the proper behavior of the secondary shutdown path as well as the interrupt signal needs to be checked by the microcontroller.

10.6.1.4 Testing the complete monitoring chain (comparators, deglitching and output)

The testing of the complete monitoring chain from the comparator till the respective output function has to be divided into the two functions available in TLF35585QV. First the secondary safety shutdown path called SS1/2 for severe microcontroller related failure events and secondly the interrupt function INT for peripheral related failure events in terms of voltage and current monitoring.

10.6.1.4.1 Testing the activation of the secondary safety shutdown path

To test the activation of the secondary safety shutdown path, the device has to be brought into NORMAL-state. The MCU shall check if the secondary safety shutdown path has been de-activated successfully (SS1/2 high).

Once in NORMAL-state a single comparator contributing to the secondary safety shutdown path shall be selected. A single bit ('x') has to be set for a corresponding comparator in registers **ABIST_SELECT0** ($00x0xxxx_B$), **ABIST_SELECT1** ($0000xxx0_B$) or **ABIST_SELECT2** ($xx00000x_B$). A randomized selection by the microcontroller ensures maximum coverage of the contributions to the secondary safety shutdown path. Then a single comparator ABIST operation on the full path of the secondary safety shutdown path needs to be started (register **ABIST_CTRL0**: 00000111_B (07_H)). Upon completion of the requested ABIST operation the device moves autonomously into WAKE-state and an interrupt event is generated. An interrupt event indicates the completion of the ABIST (**IF**.ABIST). Furthermore the respective monitoring failure flag for the selected comparator is set (either **INITERR**.VMONF for "Figure 42" failures or **SYSFAIL**.VMONF for "Figure 49" failures) which has to be checked and cleared by the microcontroller.

The secondary safety shutdown path shall be activated (SS1/2 low), it is the responsibility of the MCU to check the activation of the secondary safety shutdown path. If SS2 delay is enabled, this delay is applied when the ABIST operation is performed, i.e. the activation of the shutdown path connected to SS2 is delayed according to the programmed value for failure cases not leading to FAILSAFE. The MCU needs to read and check the status of the requested ABIST operation (**ABIST_CTRL0**.STATUS), the respective monitoring status flag (**MONSF1**, **MONSF2** or **MONSF3**) to be set according to the previous selection and **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2** bits to be cleared.

Furthermore, the microcontroller has to proceed with the following steps to check the Safe State Control and the safe state outputs:

- Check that the secondary safety shutdown path has been activated successfully (SS1/2 low)
- Enable overvoltage trigger of the Safe State Control (set **ABIST_CTRL1**.OV_TRIG)
- Wait for 50µs and check that the secondary safety shutdown path is still activated successfully (SS1/2 low)
- Select generation of valid toggling signal for the Safe State Control (set **ABIST_CTRL1**.ABIST_CLK_EN)
- Wait for 50µs and check that the secondary safety shutdown path is still activated successfully (SS1/2 low)
- De-select generation of toggling signal for the Safe State Control (reset **ABIST_CTRL1**.ABIST_CLK_EN)
- Wait for 50µs and check that the secondary safety shutdown path is still activated successfully (SS1/2 low)
- Disable overvoltage trigger of the Safe State Control (set **ABIST_CTRL1**.OV_TRIG)
- Wait for 50µs and check that the secondary safety shutdown path is still activated successfully (SS1/2 low)

Afterwards a test of all comparators which contribute to the activation of the secondary safety shutdown path shall be configured and started according to Chapter 10.6.1.3.

10.6.1.4.2 Testing the generation of an interrupt event

The test of the generation of an interrupt event can be done in the states INIT, NORMAL and WAKE-state. Even though it is recommended to have the application in safe state (INIT or WAKE-state).

For this test first a single comparator contributing to the interrupt function shall be selected. A single bit ('x') has to be set for a corresponding comparator in registers **ABIST_SELECT0** ($xx0x0000_B$), **ABIST_SELECT1** ($xxxx000x_B$) or **ABIST_SELECT2** ($00xx0000_B$). A randomized selection by the microcontroller ensures maximum coverage of the contributions to the interrupt function. Then a single comparator ABIST operation on the full path of the interrupt needs to be started (register **ABIST_CTRL0**: 00001111_B ($0F_H$)). The artificial failure, triggered by the ABIST controller, on the selected comparator generates an interrupt (INT) event. It is the responsibility of the MCU to check the generation of this interrupt event on the triggered failure. As this is a test of the generation of an interrupt based on a failure event, there is no dedicated ABIST completion event, nor the ABIST bit in the interrupt flags is set. Accordingly it is recommended to store the information about the started ABIST in the firmware. After the interrupt has been generated the interrupt flag register shall be checked for the monitoring bit (**IF**.MON) set and the ABIST completion bit (**IF**.ABIST) not set.

The MCU needs to read and check the status of the requested ABIST operation (**ABIST_CTRL0**.STATUS), the respective monitoring status flag (**MONSF1**, **MONSF2** or **MONSF3**) to be set according to the previous selection and **ABIST_SELECT0**, **ABIST_SELECT1** and **ABIST_SELECT2** bits to be cleared.

Afterwards a test of all comparators which contribute to the interrupt generation shall be configured and started according to Chapter 10.6.1.3.

10.6.1.5 Abort conditions for ABIST operation

In case of an severe monitoring failure event (contribution to the secondary safety shutdown path) detected on a not selected comparator[39] or a severe failure event not related to the voltage or bias current monitoring function during the proceeding of an ABIST operation on the comparators only (**ABIST_CTRL0**.PATH not set), the device reacts as it is supposed to do in normal operation. Accordingly the monitoring, reset and Safe State Control are reacting. Bringing the device into safe state and trigger the State machine to move into FAILSAFE or INIT-state. The ABIST is aborted in this case.

In case of an ABIST operation on the full path (**ABIST_CTRL0**.PATH set) the comparators for voltage and bias current monitoring are blind for the time of the ABIST operation. Therefore it is recommended to do the test in safe state unless it is needed to start the test in NORMAL-state (e.g. test of activation of secondary safety shutdown path described in Chapter 10.6.1.4.1). Severe failure events not related to the voltage and bias current monitoring trigger the same device reaction as in usual condition. Bringing the device into safe state and trigger the State machine to move into FAILSAFE or INIT-state. The ABIST is aborted in this case.

This ABIST abort is shown by the TLF35585QV in the register **SYSFAIL**.ABISTERR. The artificial failure events, that have been generated until the abort of the ABIST due to the detected real failure, is stored as well in the monitoring registers.

[39] Please mind that selected comparators might be blind for the time of the ABIST operation. Therefore it is recommended to do the test in safe state unless it is needed to start the test in NORMAL-state (e.g. test of activation of secondary safety shutdown path described in Chapter 10.6.1.4.1).

10.6.2 Logic supervision self test

No dedicated Built In Self Test for the digital monitoring functions exists in the device. It is therefore assumed that any test which is related to the digital monitoring functions is performed by the MCU in a functional way.

The following blocks inside the digital supervision functions can be tested by the MCU:

- FWD/WWD
- Error monitoring

In order to verify correct functionality of these blocks and to check their contribution to ROT/INT and finally SS1/2 the MCU shall generate an error condition on the particular block and check for the occurrence of the expected system behavior.

- For the watchdog functionality this basically means either stop triggering the WD(s) and/or generate false trigger events. This generates either an interrupt or even assert the reset. Finally the secondary safety shutdown path is activated (SS1/2 set to low), the MCU is reset and the device moves into INIT-state. In order to verify the activation of the secondary shutdown path, this kind of test shall only be executed after the device has been moved into NORMAL-state.
- For the error monitoring block, this means that the toggling at the ERR pin needs to be stopped in order to observe the required system behavior. It is up to the MCU to make use of the error recovery mechanism or not.

The microcontroller programming support function provides capabilities to suppress the reset (ROT) event for the supervision functions mentioned above keeping still the interrupt and safe state contribution unchanged. This may be used to optimize the logic supervision self test focusing on the safety relevant output functions (INT and SSx). For details please refer to Chapter 10.7.

10.7 Microcontroller programming support

The TLF35585QV offers a microcontroller programming support feature, that can be used to avoid periodic reset triggering due to missing triggering of the window watchdog and error monitoring within the INIT timer.

The activation of the microcontroller programming support feature is supported by:

- by pulling the MPS pin to a voltage $V_{MPS,hi}$. The voltage shall be provided earliest with the enabling of the microcontroller supply QUC . Therefore during microcontroller programming or debugging, it would be one option to connect the MPS pin to the output QVR or QUC.
- via SPI command to **MCSMON**.MPS

The status bit field **MCSMON**.MPSPIN represents the actual activation status controlled by the MPS pin.

The active microcontroller programming support (MPS) feature includes the following changes to the normal operation of the device:

- The initialization timer is stopped.
- The contribution of the window watchdog error counter overflow to the reset ROT output is blocked.
- The contribution of the functional watchdog failure counter overflow to the reset output ROT is blocked.
- The contribution of the error monitoring to the reset output ROT is blocked.

Only the above mentioned functional influences are activated by the MPS function, the state machine, interrupt function and Safe State Control(SSC) function are not affected. An invalid watchdog service warning or an ERR monitoring warning (if recovery delay configured) still issues an interrupt event. An overflow of a watchdog failure counter and a detected ERR monitoring failure triggers a "Move to INIT" event and the corresponding SSC reaction to set SS1/SS2 to low, but without issuing a reset (ROT) of the microcontroller. This feature may be used for time-optimized fault-injection tests of the digital supervision functions (WWD, FWD, ERR) as well as for application boundary conditions where no reset of the microcontroller is desired for watchdog or error monitoring failures, whilst keeping active the safety related supervision functions.

E.g. in case MPS pin is high or bitfield MPSPIN is set in NORMAL and there is a watchdog error counter overflow the device would move into INIT without issuing a reset, but still transitioning SS1/SS2 to low.

Table 27 Electrical characteristics: microcontroller programming support

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
MPS valid high level	$V_{MPS,hi}$	2.0	–	–	V	–	P_11.7.1
MPS valid low level	$V_{MPS,lo}$	–	–	0.8	V	–	P_11.7.2

11 Safe State Control function

11.1 Introduction Safe State Control function

The Safe State Control monitors safety related signals and controls the safe state signals SS1 and SS2.

The following description summarizes the contributors to the Safe State Control function and the possibilities to adjust them.

Principle of operation

The Safe State Control function monitors the following inputs:

- Result of the Error Monitoring. "Error"-signal at pin ERR is expected to be a toggling signal. A permanent low or high signal is detected as an error.
- Over and undervoltage of the microcontroller related regulators (for details please refer to chapter Monitoring function)
- Result of Window Watchdog Failure Counter Threshold Comparator. Whether threshold ΣWWO for "Invalid window watchdog triggering" has been exceeded.
- Result of Functional Watchdog Failure Counter Threshold Comparator: Whether threshold ΣFWO for "Invalid functional watchdog triggering" has been exceeded.
- Thermal shutdown signal (TSD) for relevant events moving the device into FAILSAFE-state.
- Internal clock
- SPI state transition request. A valid "Go to NORMAL" command triggers the signals SS1/2 to switch high in case the other boundary conditions are fulfilled. Moving the device out of NORMAL-state by SPI command switches the signals SS1 and SS2 (optionally delayed by Δt_{SS2}) to low.

The following parameters of the Safe State Control function are programmable via SPI, this settings can be done during INIT, NORMAL, SLEEP and WAKE-state, WWD and FWD configuration and error pin configuration including disabling of individual functionality via protected register (for description of states please refer to chapter State machine):

- Number of invalid watchdog triggers, that lead to activating SS1 and SS2: There are two watchdog trigger failure counters implemented, one for the window watchdog the other for the functional watchdog. Every counter increments by two at every invalid watchdog triggering and decrements by one at every valid watchdog triggering. (valid and invalid triggering is described in chapter functional and window watchdog). An incrementing change is indicated by an interrupt. A decrementing change is not indicated by an interrupt. The thresholds can be programmed by SPI command for each counter individually. This function might be used to test the watchdog function.
- Immediate reaction or recovery delay reaction, only related to input signal ERR: This parameter determines whether the Safe State Control reacts immediately to an error indicated by SMU or react after a certain delay, if the error indication is still present. In recovery delay reaction the Safe State Control generates an interrupt and start the programmed recovery delay time. If within this time the error should disappear (means the error signal should toggle again, before the recovery delay time has ended), the Safe State Control keeps the safe state output SS1/2 high. If within this time the error signal should not disappear and maintain the error indication (means the error signal should not toggle again, before the recovery delay time has ended), the Safe State Control activates the safe state signals SS1 and SS2 after the recovery delay time has ended. Immediate reaction means reaction after signal detection delay time.
- Recovery delay time Δt_{REC}, only related to input signal ERR: An error (violation of valid ERR signal) has to be longer than this delay time to lead to activating the safe state signals SS1 and SS2. This delay time is only active if recovery delay time mode was selected.
- Delay time Δt_{SS2} between safe state signal 1 and safe state signal 2

The safe state function offers two output signals, both of them as output stages to drive external switches (additional driver stage is necessary):

- Safe state signal 1 (present at pin SS1)
- Safe state signal 2 (present at pin SS2), it may be delayed to safe state signal 1 by an adjustable delay time Δt_{SS2} (via SPI)

Error signal from microcontroller safety management unit (SMU) at pin ERR

The error monitoring function requires a toggling signal at pin ERR with a determined timing in case of fault-free operation of the microcontroller by its SMU. This toggling signal is considered as a "being alive" indication. An error should be indicated by a constant low signal. A constant high signal is regarded as a failure indication as well, probably caused by a short circuit. The result is given to the Safe State Control.

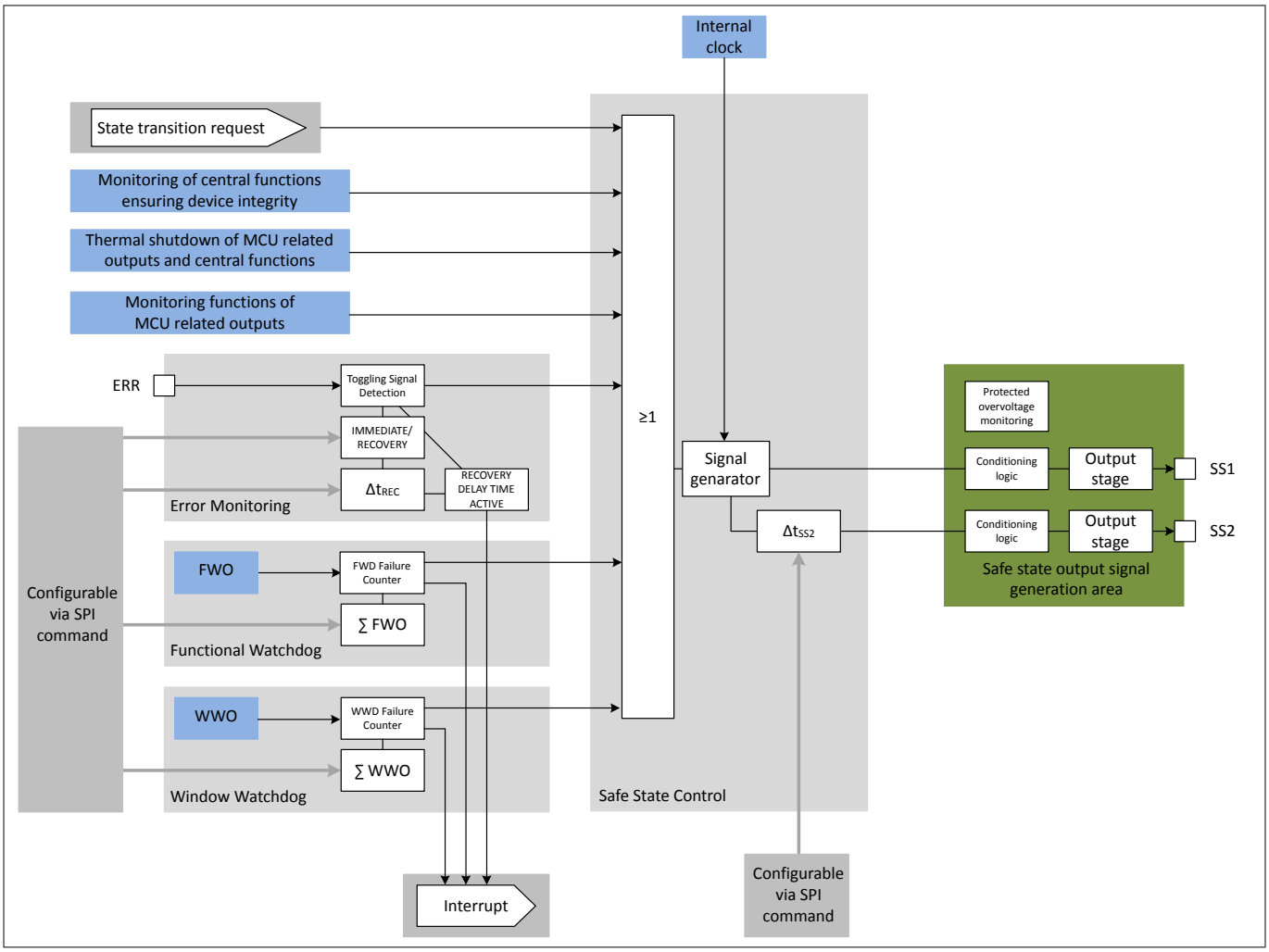


Figure 58 Principle Safe State Control function

Description:

- State transition request = Microcontroller can request a deactivation of the secondary safety shutdown path (SS1/2 high) via SPI. Being in NORMAL-state the micro processor can activate the Secondary Safety Shutdown path (SS1/2 low) by moving the device out of NORMAL-state via SPI.
- Monitoring of central functions ensuring device integrity
- TSD = Thermal shutdown
- Monitoring functions of MCU related outputs
- ERR monitoring = Error pin connected to safety management unit (SMU) of microcontroller
- ΣWWO = Number of "Invalid WWD triggering", after Safe State Control shall activate the safe state signal SS1 and SS2, located in window watchdog block

- ΣFWO = Number of "Invalid FWD triggering", after Safe State Control shall activate the safe state signal SS1 and SS2, locked in functional watchdog block
- IMMEDIATE/RECOVERY = Distinguish between immediate reaction to SMU signal or recovery delay time, located in error monitoring block
- Δt_{REC} = Recovery delay time for SMU signal at pin ERR, located in error monitoring block
- Δt_{SS2} = Delay time between safe state signal 1 and safe state signal 2
- SS1 = Safe state signal 1
- SS2 = Safe state signal 2

11.2 Electrical characteristics Safe State Control

Table 28 Electrical characteristics Safe State Control

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
ERR pin							
ERR valid high level TLF35585QVS01	$V_{ERR,hi}$	3.6	–	–	V	V_{ERR} increasing; V_{QUC} = 5.0 V	P_12.2.1
ERR valid low level TLF35585QVS01	$V_{ERR,lo}$	–	–	0.8	V	V_{ERR} decreasing; V_{QUC} = 5.0 V	P_12.2.2
ERR hysteresis TLF35585QVS01	$V_{ERR,hyst}$	200	600	1200	mV	V_{QUC} = 5.0 V	P_12.2.3
ERR valid high level TLF35585QVS02	$V_{ERR,hi}$	2.0	–	–	V	V_{ERR} increasing; V_{QUC} = 3.3 V	P_12.2.4
ERR valid low level TLF35585QVS02	$V_{ERR,lo}$	–	–	0.8	V	V_{ERR} decreasing; V_{QUC} = 3.3 V	P_12.2.5
ERR hysteresis TLF35585QVS02	$V_{ERR,hyst}$	100	300	600	mV	V_{QUC} = 3.3 V	P_12.2.6
ERR pull-down current	I_{ERR}	–	150	330	µA	$V_{ERR} = V_{QUC}$	P_12.2.7
ERR input capacitance	C_{ERR}	–	4	15	pF	[40]	P_12.2.8
Valid ERR input signal frequency	$f_{ERR,valid}$	10	–	45	kHz	considering a duty cycle of 50 %	P_12.2.9
Invalid ERR input signal frequency (low frequency)	$f_{ERR,invalid,LF}$	0	–	5	kHz	considering a duty cycle of 50 %	P_12.2.10
Invalid ERR input signal frequency (high frequency)	$f_{ERR,invalid,HF}$	96.2	–	500	kHz	considering a duty cycle of 50 %	P_12.2.11
Invalid ERR input signal detection time (low frequency)	$\Delta t_{DET,LF}$	50.1	–	99.9	µs	derived from $f_{ERR,valid}$ and $f_{ERR,invalid,LF}$	P_12.2.12
Invalid ERR input signal detection time (high frequency)	$\Delta t_{DET,HF}$	5.2	–	11.1	µs	derived from $f_{ERR,valid}$ and $f_{ERR,invalid,HF}$	P_12.2.13
ERR reactivation time-out	$t_{ERR,TO}$	9	10	11	ms	after SLEEP	P_12.2.14
ERR reactivation time-out (first edge expected)	$t_{ERR,ren}$	50.1	–	110	µs	after re-enabling via SPI [41]	P_12.2.15

(table continues...)

40 Specified by design, not subject to production test
41 It is recommended to provide the ERR signal to the ERR pin before activating the function again via SPI.

Table 28 (continued) Electrical characteristics Safe State Control

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Safe state signal 1 pin SS1							
SS1 output, high level TLF35585QVS01	$V_{SS1,hi}$	3.6	4.8	V_{QUC}	V	$I_{SS1} \geq$ -1 mA; V_{QUC} = 5.0 V	P_12.2.16
SS1 output, high level TLF35585QVS01	$V_{SS1,hi}$	3.0	4.3	V_{QUC}	V	$I_{SS1} \geq$ -5 mA; V_{QUC} = 5.0 V	P_12.2.17
SS1 output, high level TLF35585QVS02	$V_{SS1,hi}$	2.9	3.2	V_{QUC}	V	$I_{SS1} \geq$ -1 mA; V_{QUC} = 3.3 V	P_12.2.18
SS1 output, high level TLF35585QVS02	$V_{SS1,hi}$	2.0	2.8	V_{QUC}	V	$I_{SS1} \geq$ -5 mA; V_{QUC} = 3.3 V	P_12.2.19
SS1 pull-down resistor	$R_{SS1,pd}$	70	100	130	kΩ		P_12.2.20
SS1 output, low level	$V_{SS1,lo}$	–	0	0.8	V	42)43) $R_{SS1,pd,ext} \leq$ 100 kΩ; $C_{SS1,ext} \geq$ 50 pF; QUC active ; $V_{QUC} \geq$ 2 V	P_12.2.21
SS1 internal reaction time	$t_{SS1,act}$	–	12	30	µs		P_12.2.22
Safe state signal 2 pin SS2							
SS2 output, high level TLF35585QVS01	$V_{SS2,hi}$	3.6	4.8	V_{QUC}	V	$I_{SS2} \geq$ -1 mA; V_{QUC} = 5.0 V	P_12.2.23
SS2 output, high level TLF35585QVS01	$V_{SS2,hi}$	3.0	4.3	V_{QUC}	V	$I_{SS2} \geq$ -5 mA; V_{QUC} = 5.0 V	P_12.2.24
SS2 output, high level TLF35585QVS02	$V_{SS2,hi}$	2.9	3.2	V_{QUC}	V	$I_{SS2} \geq$ -1 mA; V_{QUC} = 3.3 V	P_12.2.25
SS2 output, high level TLF35585QVS02	$V_{SS2,hi}$	2.0	2.8	V_{QUC}	V	$I_{SS2} \geq$ -5 mA; V_{QUC} = 3.3 V	P_12.2.26
SS2 pull-down resistor	$R_{SS2,pd}$	70	100	130	kΩ		P_12.2.27
SS2 output, low level	$V_{SS2,lo}$	–	0	0.8	V	42)43) $R_{SS2,pd,ext} \leq$ 100 kΩ; $C_{SS2,ext} \geq$ 50 pF; QUC active ; $V_{QUC} \geq$ 2 V	P_12.2.28
SS2 internal reaction time	$t_{SS2,act}$	–	12	30	µs		P_12.2.29

(table continues...)

42 Internal and external pull-down resistors have to be considered for failure cases with QUC being off.

Table 28 (continued) Electrical characteristics Safe State Control

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Adjustable parameters							
SSC time base accuracy	t_{SSC}	-10	–	10	%	timebase for Δt_{REC} and Δt_{SS2}	P_12.2.30
adjustable recovery delay time	Δt_{REC}	0	–	10	ms	selectable 0, 1.0, 2.5, 5.0 and 10 ms; t_{SSC} to be considered	P_12.2.31
adjustable delay time between SS1 and SS2	Δt_{SS2}	0	–	250	ms	selectable 0, 10,50, 100 and 250 ms; t_{SSC} to be considered	P_12.2.32

43 Considering loss of analog safety ground (AGS1 and AGS2).
42 Internal and external pull-down resistors have to be considered for failure cases with QUC being off.

11.3 Reaction on microcontroller Safety Management Unit (SMU - pin ERR):

11.3.1 Immediate reaction on ERR monitoring failure

The microcontroller safety management unit (SMU) indicates a serious error by stopping the toggling signal at pin ERR, immediate reaction to error signal is set:

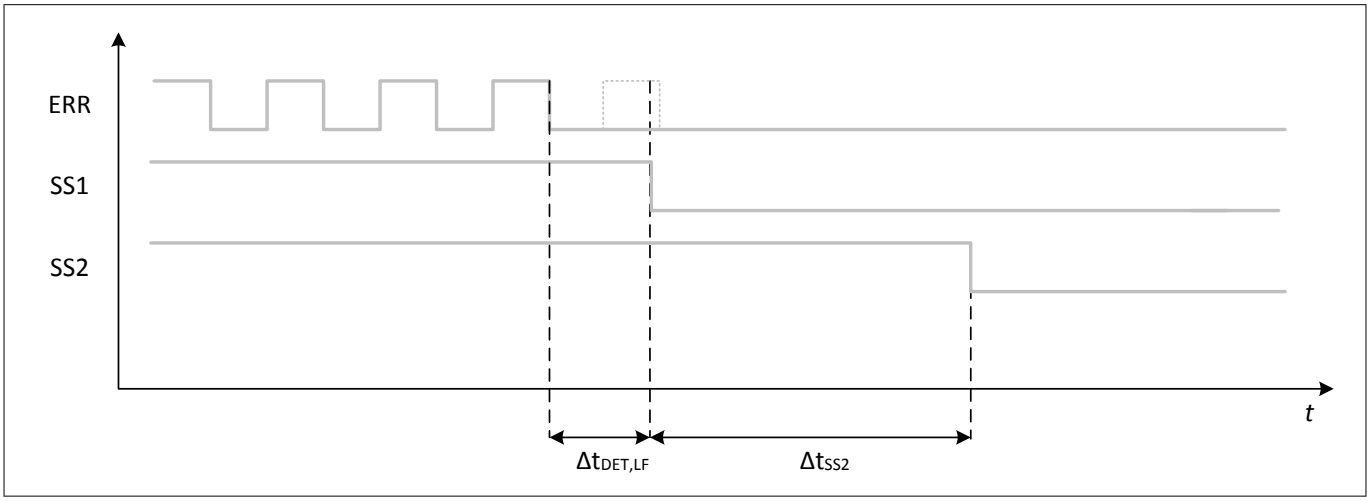


Figure 59 Flow diagram reaction on SMU signal (ERR signal remains low)

Description:

- The ERR signal stops toggling and remains low.
- This is detected as an error after the expiration of the detection time $\Delta t_{DET,LF}$.
- $\Delta t_{DET,LF}$ is measured from the last recognized falling edge.
- The safe state signal 1 (at pin SS1) is pulled to low
- The safe state signal 2 (at pin SS2) is pulled to low after an optional delay time Δt_{SS2}

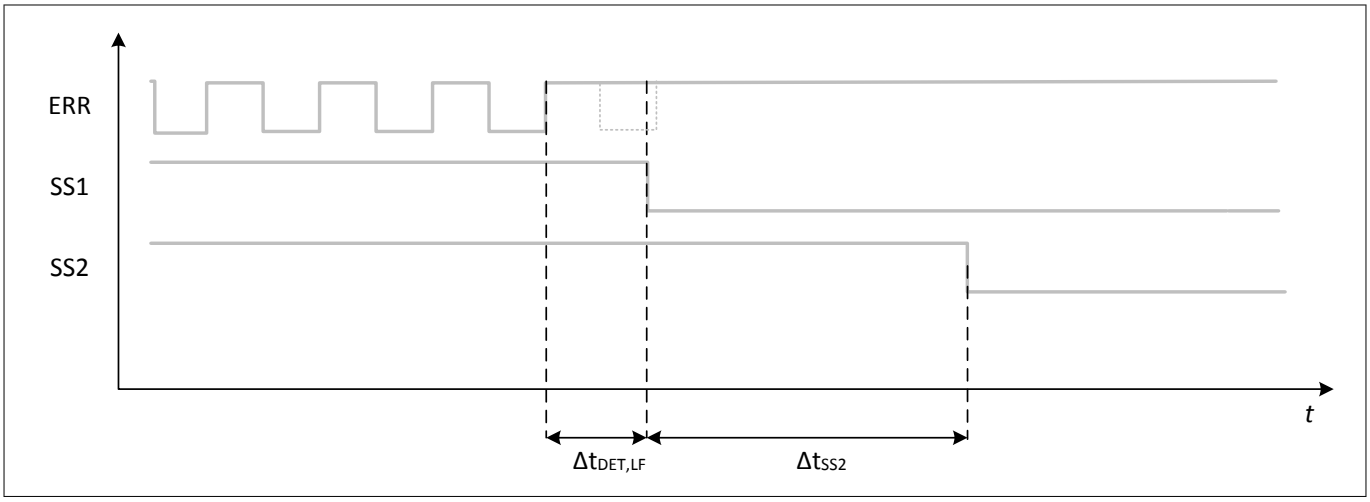


Figure 60 Flow diagram reaction on SMU signal (ERR signal remains high)

Description:

- The ERR signal stops toggling and remains high.
- This is detected as an error after the expiration of the detection time $\Delta t_{DET,LF}$.

- $\Delta t_{DET,LF}$ is measured from the last recognized rising edge.
- The safe state signal 1 (at pin SS1) is pulled to low
- The safe state signal 2 (at pin SS2) is pulled to low after an optional delay time Δt_{SS2}

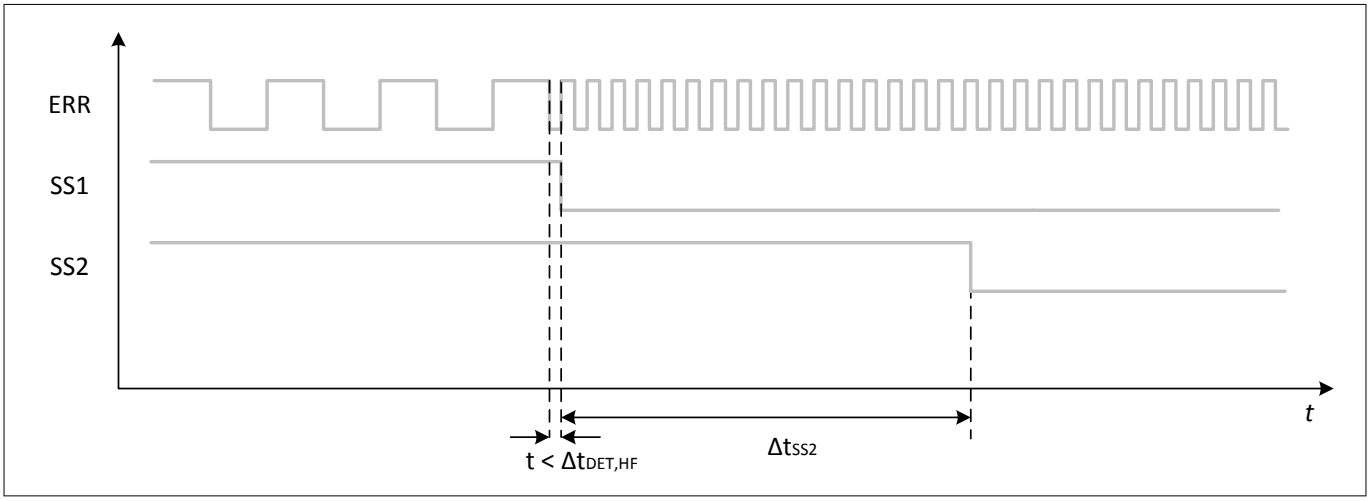


Figure 61 Flow diagram reaction on SMU signal (ERR signal frequency too high)

Description:

- The ERR signal starts toggling with a frequency of $f_{ERR,invalid,HF}$.
- This is detected as an error as soon as the edge-to-edge time is shorter than the detection time $\Delta t_{DET,HF}$.
- The safe state signal 1 (at pin SS1) is pulled to low.
- The safe state signal 2 (at pin SS2) is pulled to low after an optional delay time Δt_{SS2}.

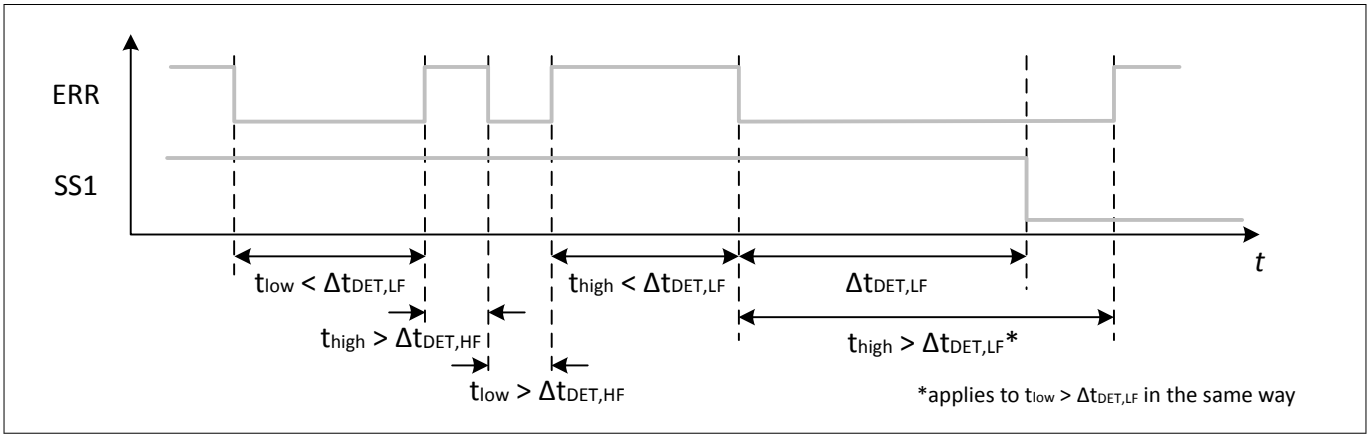


Figure 62 Flow diagram reaction on SMU signal (duty-cycle different than 50%, t_{low} or t_{high} too long)

Description:

- The ERR signal toggles with changing high and low times (duty cycle can vary as well), but t_{low} and t_{high} are in the valid range between $t_{DET,HF}$ and $t_{DET,LF}$ first.
- Then a low pulse of ERR shown in the figure is longer than the detection time $t_{DET,LF}$.
- This is detected as an error as soon as the edge-to-edge time is longer than the detection time $\Delta t_{DET,LF}$.
- The safe state signal 1 (at pin SS1) is pulled to low.
- The safe state signal 2 (at pin SS2) is pulled to low accordingly after an optional delay time Δt_{SS2}.(not in figure)
- The condition can be applied to the high pulse being longer than the detection time $t_{DET,LF}$ in the same way.

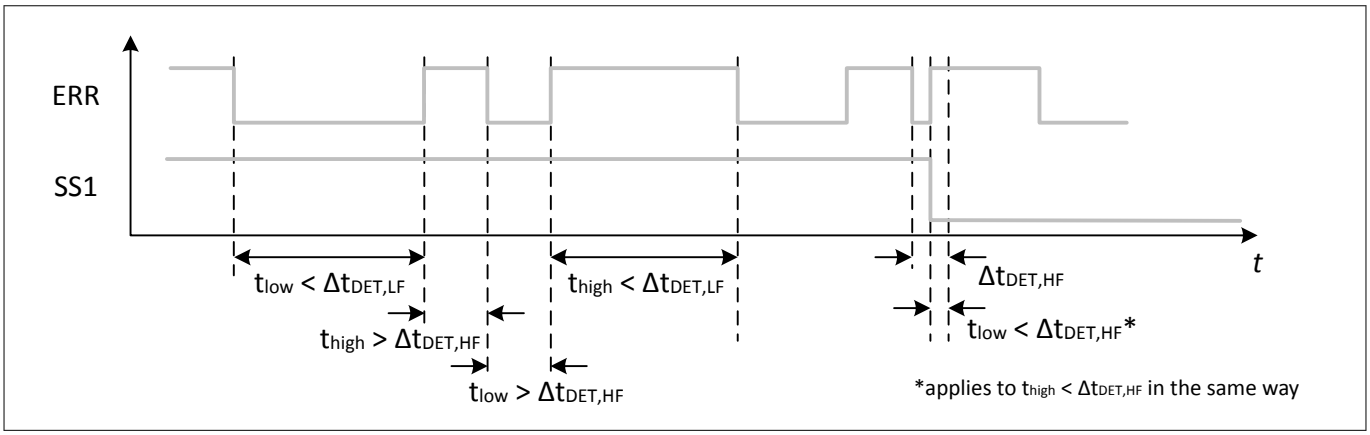


Figure 63 **Flow diagram reaction on SMU signal (duty-cycle different than 50%, t_{low} or t_{high} too short)**

Description:

- The ERR signal toggles with changing high and low times (duty cycle can vary as well), but t_{low} and t_{high} are in the valid range between $t_{DET,HF}$ and $t_{DET,LF}$ first.
- Then a low pulse of ERR shown in the figure is shorter than the detection time $t_{DET,HF}$.
- This is detected as an error as soon as the edge-to-edge time is shorter than the detection time $\Delta t_{DET,HF}$.
- The safe state signal 1 (at pin SS1) is pulled to low.
- The safe state signal 2 (at pin SS2) is pulled to low accordingly after an optional delay time Δt_{SS2}.(not in figure)
- The condition can be applied to the high pulse being shorter than the detection time $t_{DET,HF}$ in the same way.

11.3.2 Recovery delay reaction on ERR monitoring failure

The microcontroller safety management unit (SMU) indicates a serious error by stopping the toggling signal at pin ERR, recovery delay time reaction to error signal is set - the SMU is given time to recover:

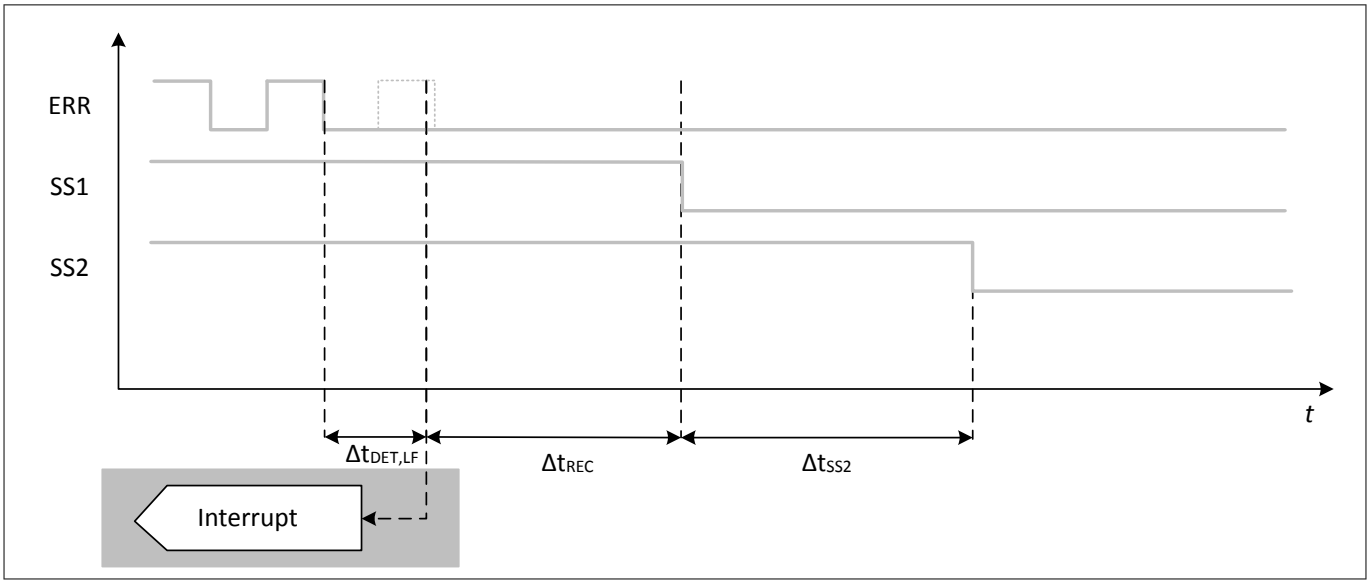


Figure 64 **Flow diagram reaction on SMU signal, error longer than recovery delay time**

Description:

- The ERR signal stops toggling and remains low (or high).
- This is detected as an error after the expiration of the detection time $\Delta t_{DET,LF}$.
- $\Delta t_{DET,LF}$ is measured from the last recognized edge.
- An interrupt is generated after the detection to indicate the start of the recovery delay time Δt_{REC}
- The safe state signal 1 (at pin SS1) is pulled to low after Δt_{REC} has expired
- The safe state signal 2 (at pin SS2) is pulled to low after an optional delay time Δt_{SS2}

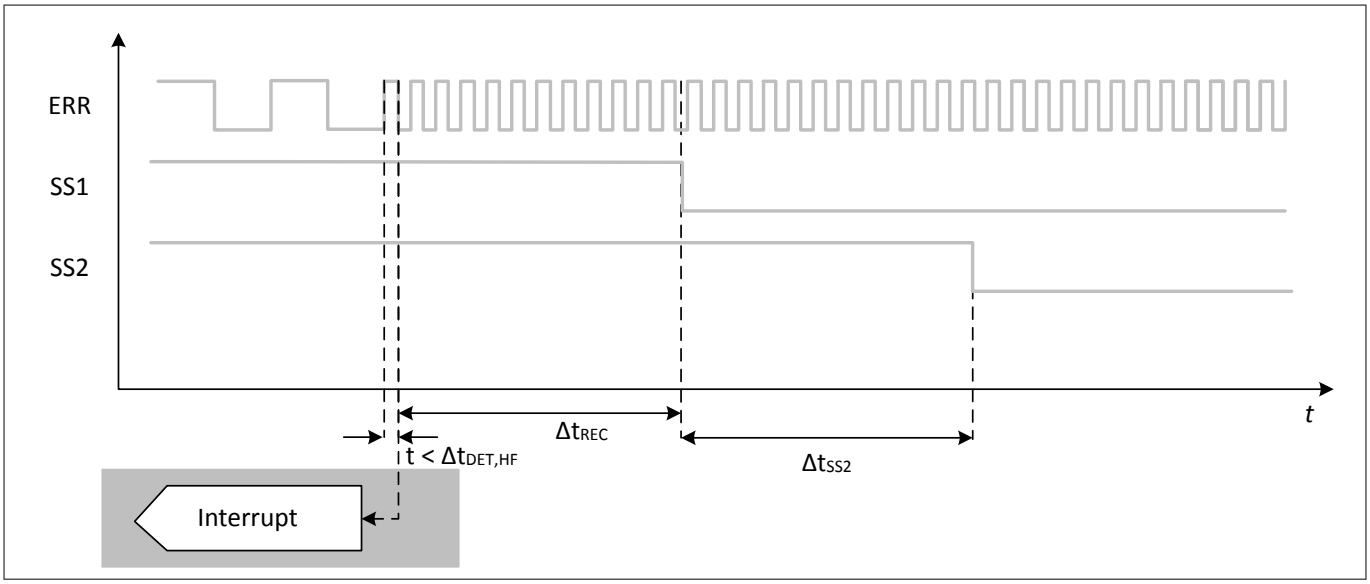


Figure 65 **Flow diagram reaction on SMU signal, error longer than recovery delay time (ERR signal) frequency too high)**

Description:

- The ERR signal starts toggling with a frequency of $f_{ERR,invalid,HF}$.
- This is detected as an error as soon as the edge-to-edge time is shorter than the detection time $\Delta t_{DET,HF}$.
- An interrupt is generated after the detection to indicate the start of the recovery delay time Δt_{REC}
- The safe state signal 1 (at pin SS1) is pulled to low after Δt_{REC} has expired
- The safe state signal 2 (at pin SS2) is pulled to low after an optional delay time Δt_{SS2}

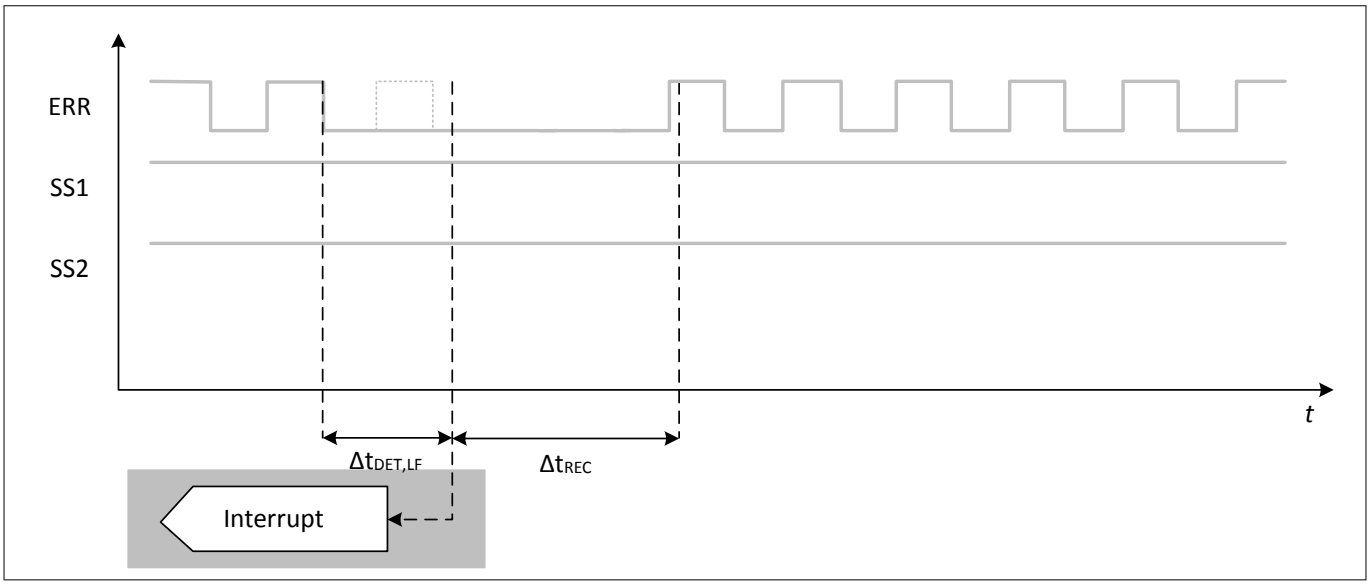


Figure 66 **Flow diagram reaction on SMU signal, error shorter than recovery delay time**

Description:

- The ERR signal stops toggling and remains low (or high).
- This is detected as an error after the expiration of the detection time $\Delta t_{DET,LF}$.
- $\Delta t_{DET,LF}$ is measured from the last recognized edge.
- An interrupt is generated after the detection to indicate the start of the recovery delay time Δt_{REC}
- Before Δt_{REC} has expired the ERR signal resumes toggling.
- The safe state signals 1 (at pin SS1) and 2 (at pin SS2) are kept high all the time.

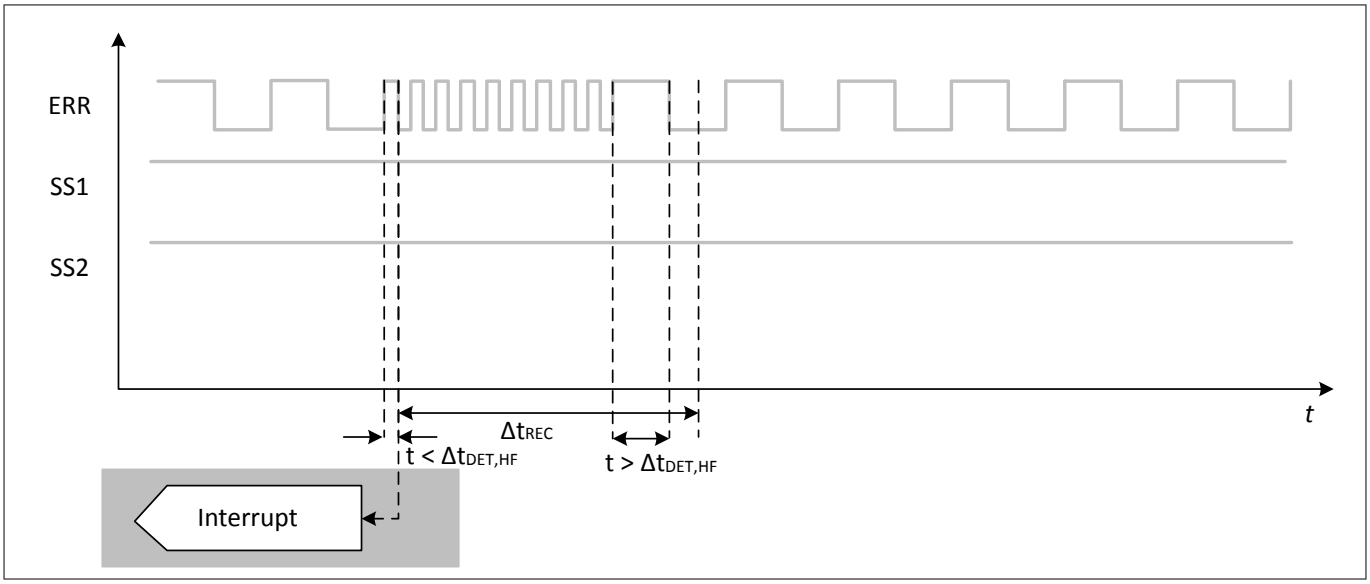


Figure 67 **Flow diagram reaction on SMU signal, error shorter than recovery delay time (ERR signal frequency too high)**

Description:

- The ERR signal starts toggling with a frequency of $f_{ERR,invalid,HF}$.
- This is detected as an error as soon as the edge-to-edge time is shorter than the detection time $\Delta t_{DET,HF}$.
- An interrupt is generated after the detection to indicate the start of the recovery delay time Δt_{REC}

- Before Δt_{REC} has expired the ERR signal resumes toggling with a valid frequency.
- The safe state signals 1 (at pin SS1) and 2 (at pin SS2) are kept high all the time.

11.4 Reaction on error-triggered state transitions

The reset output (ROT) indicates the behavior of the microcontroller related regulators (for details please refer to chapter voltage monitoring and reset function).

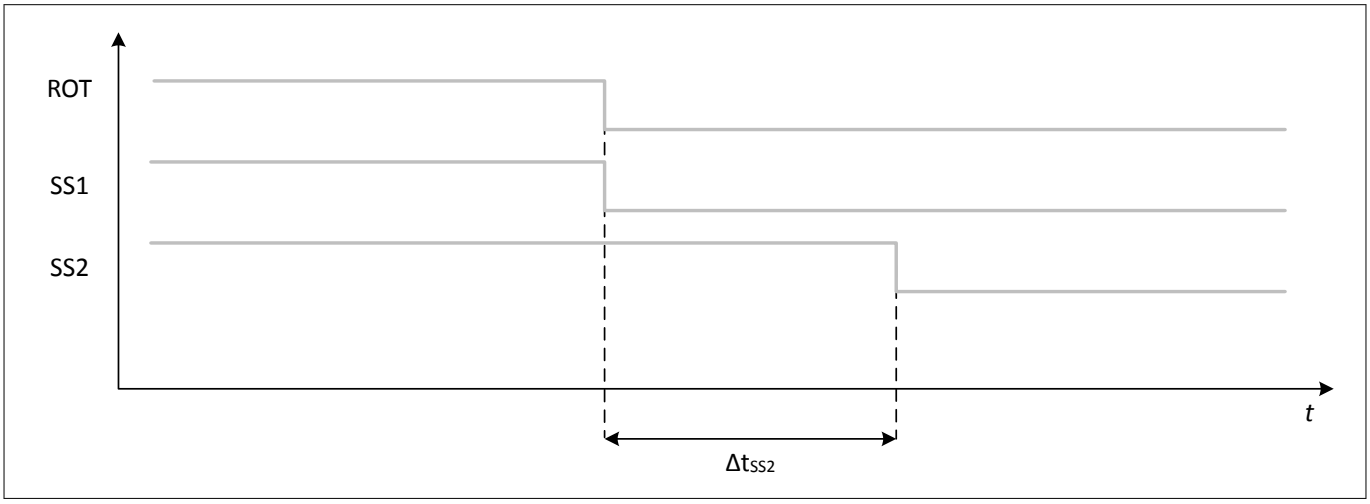


Figure 68 Flow diagram reaction on an error triggered state transition- soft reset

Description:

- The falling edge of ROT signal indicates an error
- Safe state signal 1 (at pin SS1) goes to low immediately with the occurrence of the error
- Safe state signal 2 (at pin SS2) goes to low after a delay time Δt_{SS2} which was set by SPI command
- Please mind that in case of an UV event on QUC, a delayed SS2 signal follows V_{QUC} as it is supplied from QUC.

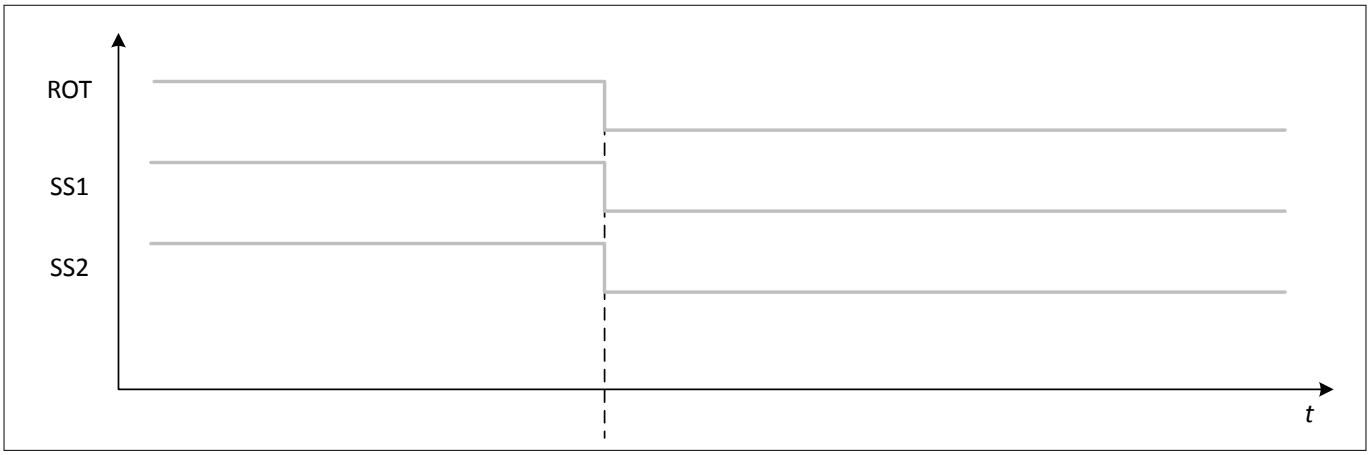


Figure 69 Flow diagram reaction on an error triggered state transitions - hard reset

Description:

- The falling edge of ROT signal indicates an error
- Safe state signal 1 (at pin SS1) goes to low immediately with the occurrence of the error
- Safe state signal 2 (at pin SS2) goes to low together with SS1 as the supplying post regulator QUC is switched off when pin ROT goes to low

11.5 Reaction on Window Watchdog Output (WWO)

The TLF35585QV has an implemented window watchdog failure counter (**WWDSTAT**.WWDECNT). The counter increments by two at every invalid window watchdog triggering and decrements by one at every valid window watchdog triggering. (For specification of valid and invalid triggering please refer to chapter functional and window watchdog).

The status of the window watchdog failure counter is written in the so called window watchdog status counter. Any incrementation of the window watchdog status counter is indicated by an interrupt. Any decrement of the window watchdog status counter is not indicated by an interrupt. The content of the window watchdog status counter cannot be less than zero.

The threshold for activating the safe state signals SS1 and SS2 ΣWWO can be changed in INIT, NORMAL and WAKE-state. (**WDCFG0**.WWDETHR)

The content of the status counter is compared to the programmed threshold ΣWWO (**RWDCFG0**.WWDETHR). If the content of the status counter is equal or higher than ΣWWO, the safe state signals SS1 and SS2 are activated (low).

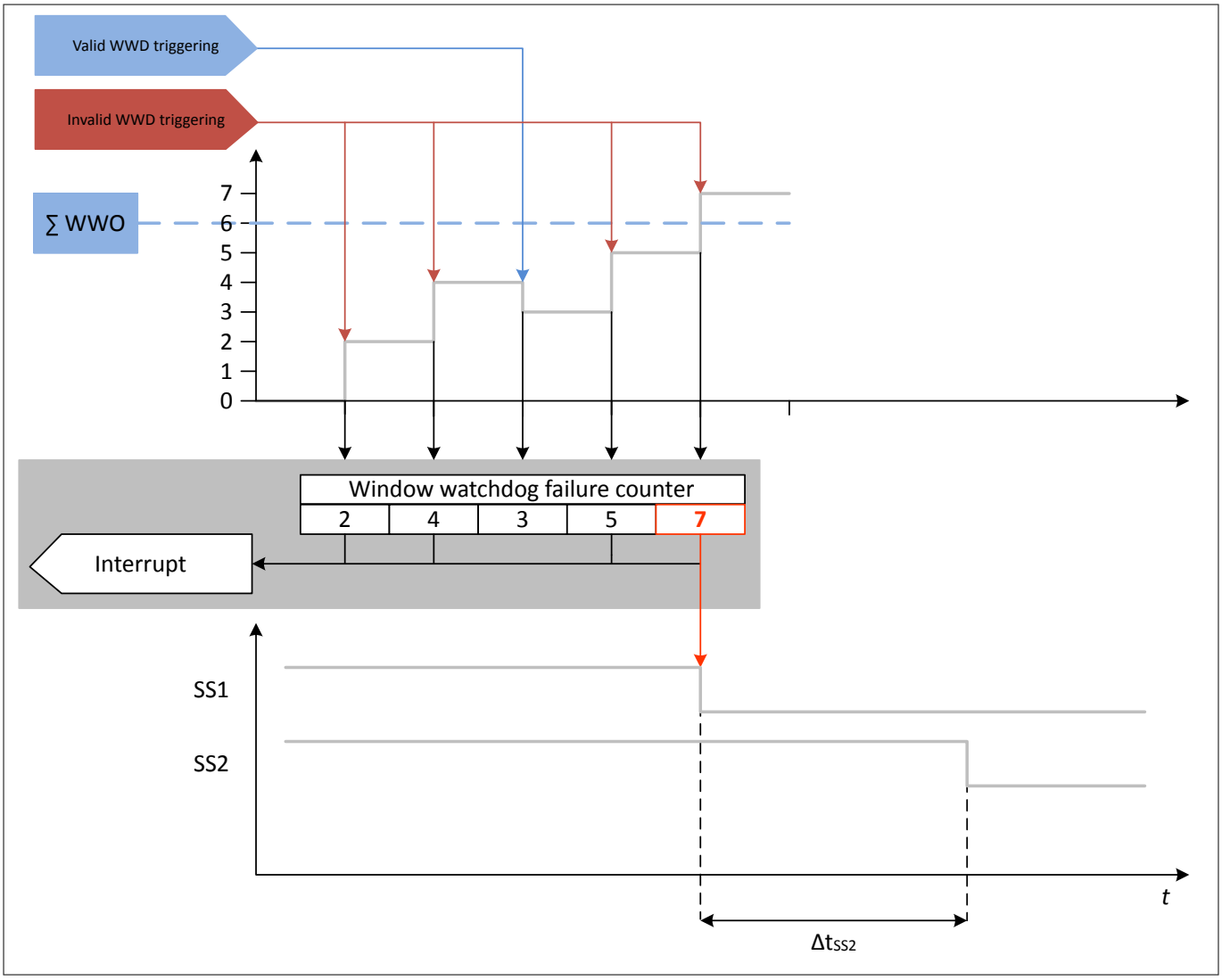


Figure 70 **Flow diagram reaction on WWO**

Description:

- The threshold ΣWWO is set to 6 (example)

- An invalid watchdog triggering increments the window watchdog status counter by two, this is indicated by an interrupt
- A valid watchdog triggering decrements the window watchdog status counter by one, this is not indicated by an interrupt
- The status counter value 7 is recognized as an error
- Safe state signal 1 (at pin SS1) goes to low immediately with the counter status change
- Safe state signal 2 (at pin SS2) goes to low after a delay time Δt_{SS2} which was set by SPI command

11.6 Reaction on Functional Watchdog Output (FWO)

The TLF35585QV has an implemented functional watchdog failure counter (**FWDSTAT1**.FWDECNT). The counter increments by two at every invalid functional watchdog triggering and decrements by one at every valid functional watchdog triggering. (For specification of valid and invalid triggering please refer to chapter functional and window watchdog).

The status of the functional watchdog failure counter is written in the so called functional watchdog status counter. Any incrementation of the functional watchdog status counter is indicated by an interrupt. Any decrement of the functional watchdog status counter is not indicated by an interrupt. The content of the functional watchdog status counter cannot be less than zero.

The threshold for activating the safe state signals SS1 and SS2 ΣFWO can be changed in INIT, NORMAL and WAKE-state. (**WDCFG1**.FWDETHR)

The content of the status counter is compared to the programmed threshold ΣFWO (**RWDCFG1**.FWDETHR). If the content of the status counter is equal or higher than ΣFWO, the safe state signals SS1 and SS2 are activated (low).

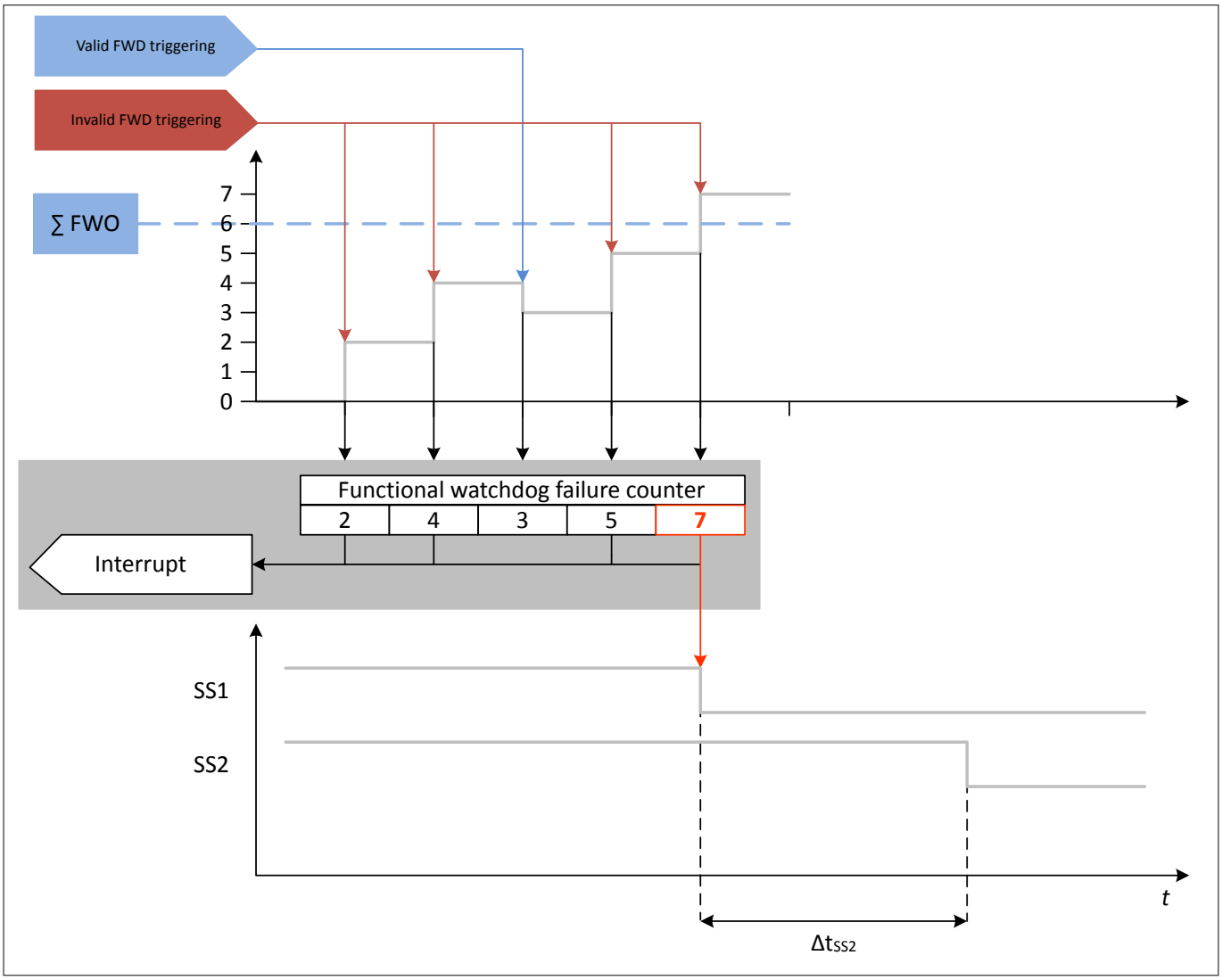


Figure 71 **Flow diagram reaction on FWO**

Description:

- The threshold ΣFWO is set to 6 (example)
- An invalid watchdog triggering increments the functional watchdog status counter by two, this is indicated by an interrupt
- A valid watchdog triggering decrements the functional watchdog status counter by one, this is not indicated by an interrupt
- The status counter value 7 is recognized as an error
- Safe state signal 1 (at pin SS1) goes to low immediately with the counter status change
- Safe state signal 2 (at pin SS2) goes to low after a delay time Δt_{SS2} which was set by SPI command

11.7 Reaction on Thermal Shutdown (TSD)

The thermal shutdown (TSD) indicates temperature overstress: on the chip: As a consequence all pre and post regulators are shut down immediately.

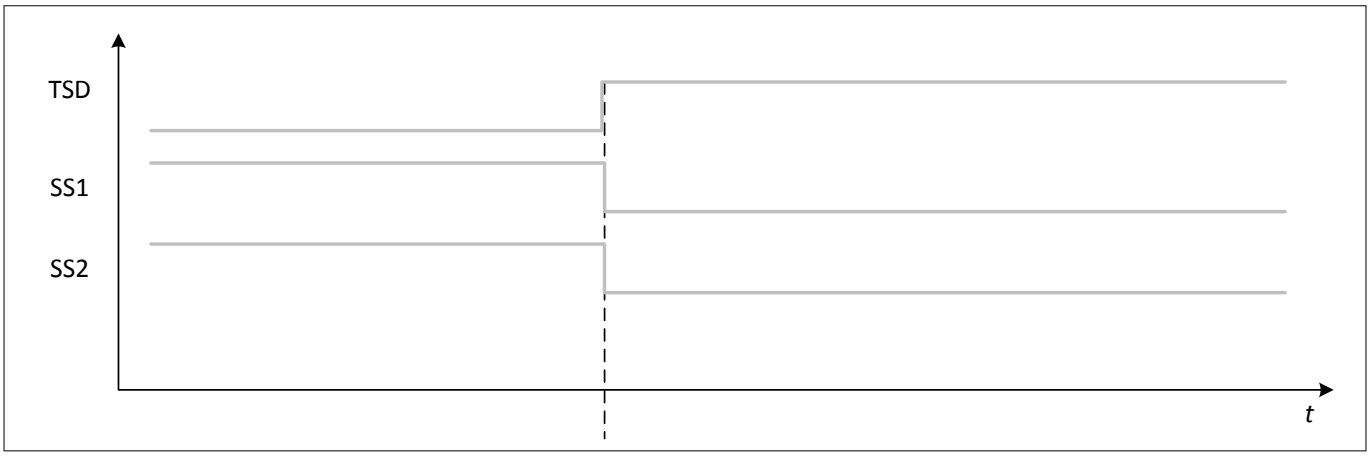


Figure 72 Flow diagram reaction on TSD

Description:

- The rising edge of TSD signal (internal) is recognized as an error
- Safe state signal 1 (at pin SS1) goes to low immediately with the rising edge of TSD
- Safe state signal 2 (at pin SS2) goes to low together with SS1 as the supplying post regulator QUC is switched off when pin ROT goes to low

12 SPI (Serial Peripheral Interface)

12.1 Introduction SPI

Main functions

The serial peripheral interface bus or SPI bus is a synchronous serial data link that operates in full duplex mode. The TLF35585QV communicates in slave mode where the master (MCU) initiates the data frame. The TLF35585QV should be addressed via a dedicated chip select line. This allows a connection of other slave devices to the SPI bus.

Data transmission

To begin a communication, the MCU first configures the clock, using a frequency less than or equal to the maximum frequency the TLF35585QV supports. The MCU pulls down the chip select for the TLF35585QV.

Functional description

SPI basic access: All data on MOSI (pin SDI) is captured on the rising edge of SPI clock signal (pin SCL) and shifted on the falling edge of SPI clock signal (pin SCL). The same methodology needs to be applied in the SPI master for MISO (SDO). A read operation has to start with CMD-bit being 1'b0 and a write operation has to start with CMD-bit being 1'b1.

In case of a write operation is performed the written command to SDI is looped back to SDO.

The parity is calculated for the output data stream in case a read operation is performed. The data for the calculation consists of 1'b1, status [5:0] and rd_data[7:0]. The parity bit is set to '1' if the number of '1' in the output data stream is odd, i.e.XOR function between all 15 bits to send out.

Parity is checked on write data. The parity is calculated on the incoming bit stream for the CMD-bit, the six address bits and the eight data bits.

Configuration via SPI can be done anytime, if the state machine (state machine) is in INIT-state, NORMAL-state, WAKE-state or SLEEP-state. During SLEEP-state the SPI has a decreased maximum clock frequency, for details please refer to Table 29.

SPI access timing can be found in the following diagram:

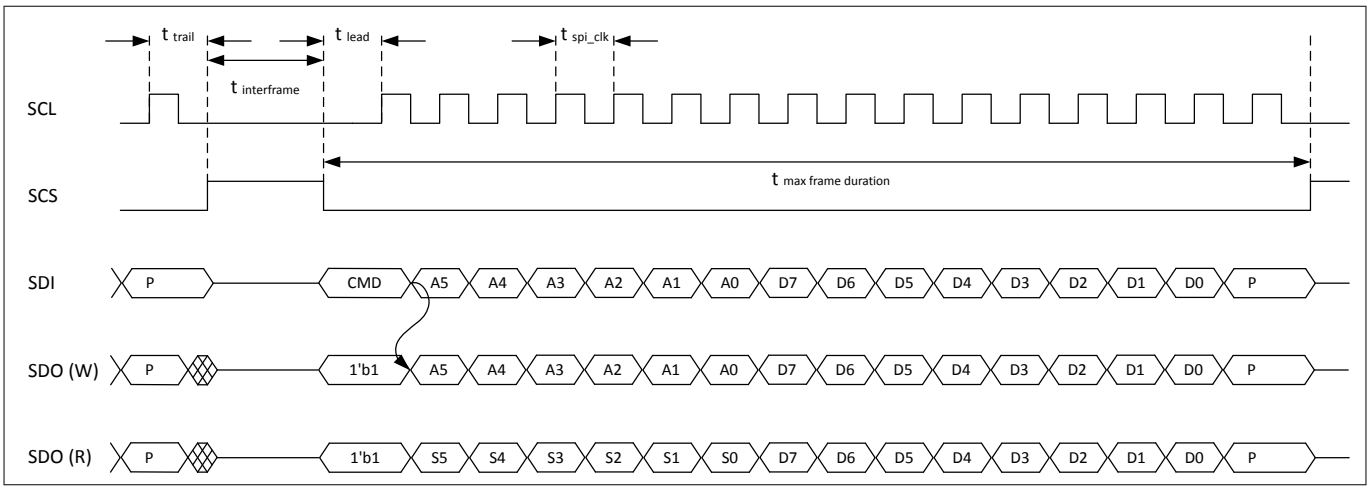


Figure 73 SPI - frame in normal mode

SPI MISO:

- During write, data from MOSI is directly looped back, during read, the addressed register content is provided in the very same SPI frame
- The CMD-bit is always set to 1'b1. All other status bits are set to zero.

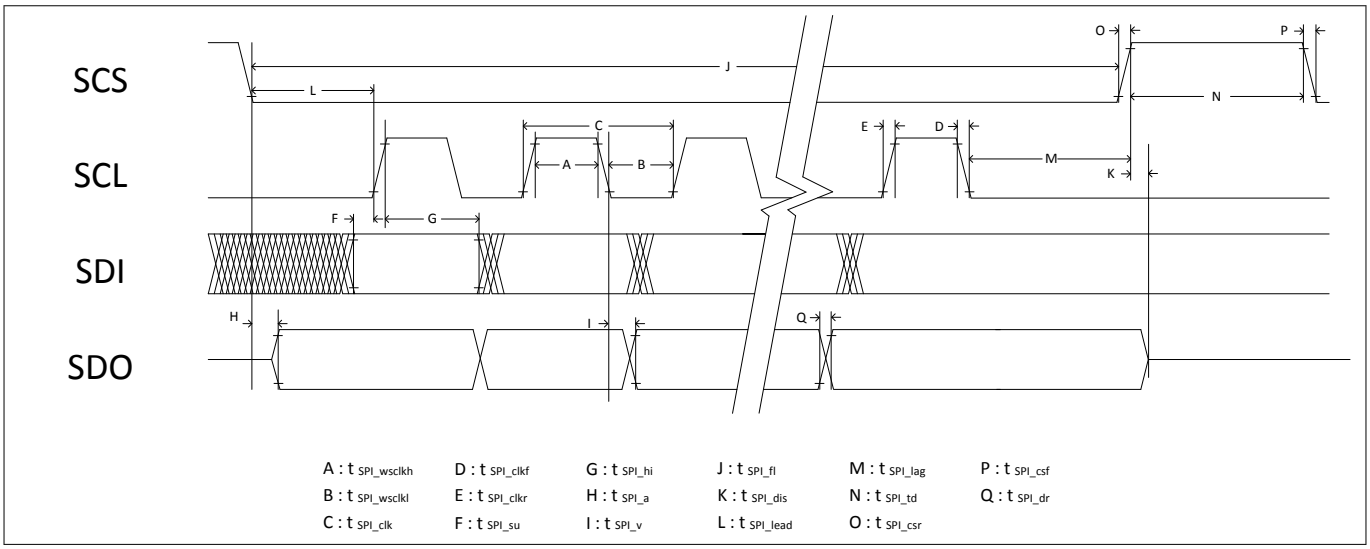


Figure 74 **SPI - timings**

Table 29 **Electrical characteristics SPI - timings**

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
CLK_SPI Operating Frequency	f_{SPI_clk}	–	–	10	MHz	[44]	P_13.1.1
CLK_SPI Operating Frequency	f_{SPI_clk}	–	–	1.5	MHz	SLEEP-state	P_13.1.2
CLK Signal duty cycle	D_{SCL}	45	50	55	%		P_13.1.3
CLK_SPI Operating Period	t_{SPI_clk}	100	–	–	ns		P_13.1.4
CLK_SPI high time	t_{SPI_wsclkh}	45	–	–	ns		P_13.1.5
CLK_SPI low time	t_{SPI_wsclkl}	45	–	–	ns		P_13.1.6
CLK_SPI fall time	t_{SPI_clkf}	–	–	$0.1^{*}t_{SPI_fact}$	[ns]	$t_{SPI_fact} \leq t_{SPI_clk}$; 100 ns ≤ t_{SPI_fact} ≤ 1 µs	P_13.1.7
CLK_SPI rise time	t_{SPI_clkr}	–	–	$0.1^{*}t_{SPI_fact}$	[ns]	$t_{SPI_fact} \leq t_{SPI_clk}$; 100 ns ≤ t_{SPI_fact} ≤ 1 µs	P_13.1.8
CLK_SPI lead time	t_{SPI_lead}	100	–	–	ns	for INIT, NORMAL, WAKE state	P_13.1.9
CLK_SPI lead time (SLEEP state)	t_{SPI_lead}	4	–	–	µs	for SLEEP state	P_13.1.10
CLK_SPI lag time	t_{SPI_lag}	50	–	–	ns		P_13.1.11

(table continues...)

44 For max. achievable CLK_SPI operating frequency, please consider the CLK_SPI rise- and fall times (t_{SPI_clkr} and t_{SPI_clkf}).

Table 29 (continued) Electrical characteristics SPI - timings

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
SPI Chip Select (SCS) rise time	t_{SPI_csr}	–	–	0.2*t_{SPI_fact}	[ns]	$t_{SPI_fact} \leq t_{SPI_lag}$; 50 ns ≤ t_{SPI_fact} ≤ 500 ns	P_13.1.12
SPI Chip Select (SCS) fall time	t_{SPI_csf}	–	–	0.2*t_{SPI_fact}	[ns]	$t_{SPI_fact} \leq t_{SPI_lead}$; 100 ns ≤ t_{SPI_fact} ≤ 1 µs	P_13.1.13
SPI Data Input (SDI) setup	t_{SPI_su}	10	–	–	ns		P_13.1.14
SPI Data Input (SDI) hold time	t_{SPI_hi}	10	–	–	ns		P_13.1.15
SPI Data Output (SDO) valid after CLK_SPI	t_{SPI_v}	–	–	(0.1*t_{SPI_fact}) +36	[ns]	$C_{SDO,load}$= 50 pF; $t_{SPI_fact} \geq t_{SPI_clkf}$; 10 ns ≤ t_{SPI_fact} ≤ 100 ns	P_13.1.16
SPI write propagation delay SDI to SDO	t_{SPI_wpd}	–	–	35	ns		P_13.1.17
SPI Data Output (SDO) access	t_{SPI_a}	–	–	50	ns	$C_{SDO,load}$ = 50 pF	P_13.1.18
SPI Data Output (SDO) disable time	t_{SPI_dis}		–	100	ns	$C_{SDO,load}$ = 50 pF	P_13.1.19
Sequential transfer delay	t_{SPI_td}	350	–	–	ns		P_13.1.20
Sequential transfer delay	t_{SPI_td}	2	–	–	µs	SLEEP-state	P_13.1.21
Frame duration (SCS low)	t_{SPI_fl}		–	1.85	ms		P_13.1.22

SPI errors:

- Wrong parity bit during write, write data is ignored.
- Write to invalid address, write data is ignored.
- Wrong number of SPI clock cycles while SCS is low, write data is ignored, read data is provided by the device with each SPI clock cycle.
- Read from invalid address (all data bits zero returned on MISO for read data). For this case the parity bit is inverted/corrupted after complete calculation by the device.
- Invalid frame duration, write data is ignored and the output driver for SDO is turned off internally by the device after t_{SPI_fl}. Read data is provided with each SPI clock cycle as long as SCS is low for less than t_{SPI_fl}.
- If the number of SPI clock cycles is different than 16 and an invalid frame duration error is detected by the device, the invalid frame duration status flag is set and the wrong number of SPI clock cycle status flag is set.

In case of an SPI error occurs, an interrupt is generated.

Interrupts on SPI errors are initiated only after SCS has been driven high or the frame time-out occurred.

12.2 SPI write access to protected registers

Certain internal registers (**SYSPCFG0**, **SYSPCFG1**, **WDCFG0**, **WDCFG1**, **FWDCFG**, **WWDCFG0**, **WWDCFG1**) need to be protected against being overwritten accidentally. The status of the protection can be checked by reading the LOCK bit in the register **PROTSTAT**.

Write access to these registers is only possible after a dedicated 32 bit UNLOCK sequence has been sent via SPI. The four bytes need to be send without any other SPI write access in between. Error in doing so will reset the sequence detection, i.e. a new UNLOCK sequence has to be send. An interrupt is generated and the number of successfully detected UNLOCK sequence bytes is set to zero if a write access to any other register then **PROTCFG** is detected in between. The access to the protected registers is possible in INIT, NORMAL and WAKE-state.

The UNLOCK sequence consists of a 32-bit sequence of 4 consecutive bytes (1: 0xAB; 2:0xEF; 3:0x56; 4:0x12) which have to be sent with no other SPI write access in between. The correctness of every written byte can be checked by reading the register **PROTSTAT**. Once the UNLOCK sequence has been performed successfully, any protected configuration request register can be written. In order to ensure proper writing to the protected configuration request registers the microcontroller shall read back the register values and verify the correctness by checking data. The data bits written to the protected configuration request registers are send back inverted during read operation, that means the microcontroller can calculate an XOR of the register data read and expected. The results should be 0xFF in case of correct register data. The TLF35585QV does not check the correctness of the values in the register.

All protected configuration request register values are captured by the respective functions only after a successful LOCK sequence has been performed. A successful LOCK sequence consists of a 32-bit sequence of 4 consecutive bytes (1: 0xDF; 2:0x34; 3:0xBE; 4:0xCA) which have to be send with no other SPI write access in between. The correctness of every written byte can be checked by reading the register **PROTSTAT**.

Error in doing so will reset the sequence detection, i.e. a new LOCK sequence has to be sent. In this case (any SPI write access in between LOCK sequence) an interrupt is generated.

Upon detection of a successful LOCK sequence the configuration registers and all internal functions are updated with the values from the protected configuration request registers. It is the responsibility of the microcontroller to ensure all registers are configured properly by either writing a new value into a particular register or by reading back a register which is supposed to be unchanged. Partial reconfiguration of the protected registers, i.e. configuring just a single function and leaving other functions unchanged is not supported as with the successful LOCK sequence all protected configuration request registers are taken over into the configuration (**RSYSPCFG0**, **RSYSPCFG1**, **RWDCFG0**, **RWDCFG1**, **RFWDCFG**, **RWWDCFG0**, **RWWDCFG1**).

After the LOCK sequence an internal configuration time of max. 60 µs has to be considered to ensure that the new configuration is taken over.

Affected functions:

- All watchdog configuration registers for WWD and FWD.
- Enabling of WD while the device is in SLEEP-state
- All Error pin monitoring configuration registers
- Enabling of Error pin monitoring while the state machine is in SLEEP
- A dedicated register to enable or disable the standby supply
- Configuration of SS2 delay time failure events not leading to FAILSAFE-state

Read access to any protected configuration request register is always possible.

12.3 SPI write initiated state transition request and regulator configuration

A State machine transition can be initiated via SPI command(s). In case the state of any selectable voltage source (post regular) is expected to change for the next state, this information has to be sent together with the command into the same register. In case the setting for a particular voltage source (post regulator) is supposed to change but the state needs to be unchanged, the same approach can be applied. This basically means, the SPI command contains the current state of the state machine but a different setting for configurable voltage source (post regulator).

In order to request a state transition and/or a change of the supply configuration the request data have to be written to two separated registers **DEVCTRL** and **DEVCTRLN** after each other consequently. The data written to DEVCTRLN have to be inverted bitwise compared to the data written to DEVCTRL. The request is only accepted when the two registers are written consecutively after each other (first **DEVCTRL** and second **DEVCTRLN**) and is taken over with the rising edge of the CS at the end of the second command.

In case of an invalid request (wrong sequence or DEVCTRLN not inverted to DEVCTRL) it is rejected, an interrupt is generated and the corresponding status flag (NO_OP) is set. In case of an invalid state transition request according to the State machine in Chapter 10 the request is ignored without issuing an interrupt.

12.4 Registers description

Table 30 Abbreviations

*R0)	Registers that are being reset only in case of POWERDOWN state.
*R1)	Registers that are being reset only in case of STANDBY and POWERDOWN state.
*R2)	Registers that are being reset only in case of FAILSAFE, STANDBY and POWERDOWN state.
*R3)	Registers that are being reset in case of "Move to INIT" event, "Move to FAILSAFE" event, STANDBY and POWERDOWN state.
r	Bits that are readable (read)
rw	Bits that are readable and writable (read-write)
rwp	Bits that are readable and writable but protected by register **PROTCFG** (read-write-protected)
rw1c	Bits that are readable and to clear the bit you have to write a 1 to it. (read-write-1-to-clear). Flag-bits are updated based on the occurred condition.
rwhc	Bits that are readable and writable after writing the operation is triggered, once this is done successfully the bit is cleared by hardware. (read-write-hardware-cleared)
rwhu	Bits that are readable and writable, after the operation the bit is updated by hardware. (read-write-hardware-updated)

Table 31 Registers Address Space

Module	Base Address	End Address	Note
Bus Interface	0_H	$3F_H$	Slave interface

Table 32 Registers Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
DEVCFG0	Device configuration 0 *R2)	00_H	08_H
DEVCFG1	Device configuration 1 *R0)	01_H	06_H
DEVCFG2	Device configuration 2 *R2) [45]	02_H	00_H
PROTCFG	Protection register *R2)	03_H	00_H
SYSPCFG0	Protected System configuration request 0 *R1)	04_H	01_H
SYSPCFG1	Protected System configuration request 1 *R2)	05_H	08_H
WDCFG0	Protected Watchdog configuration request 0 *R2)	06_H	$9B_H$
WDCFG1	Protected Watchdog configuration request 1 *R2)	07_H	09_H
FWDCFG	Protected Functional watchdog configuration request *R2)	08_H	$0B_H$
WWDCFG0	Protected Window watchdog configuration request 0 *R2)	09_H	06_H
WWDCFG1	Protected Window watchdog configuration request 1 *R2)	$0A_H$	$0B_H$

(table continues...)

45 Reset class of single bits is different. See register for details.

Table 32 (continued) Registers Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
RSYSPCFG0	System configuration 0 status *R0)	$0B_H$	01_H
RSYSPCFG1	System configuration 1 status *R3) [45]	$0C_H$	08_H
RWDCFG0	Watchdog configuration 0 status *R3)	$0D_H$	$9B_H$
RWDCFG1	Watchdog configuration 1 status *R3)	$0E_H$	09_H
RFWDCFG	Functional watchdog configuration status *R3)	$0F_H$	$0B_H$
RWWDCFG0	Window watchdog configuration 0 status *R3)	10_H	06_H
RWWDCFG1	Window watchdog configuration 1 status *R3)	11_H	09_H
WKTIMCFG0	Wake-up timer configuration 0 *R0)	12_H	00_H
WKTIMCFG1	Wake-up timer configuration 1 *R0)	13_H	00_H
WKTIMCFG2	Wake-up timer configuration 2 *R0)	14_H	00_H
DEVCTRL	Device control request *R2)	15_H	00_H
DEVCTRLN	Device control inverted request *R2)	16_H	00_H
WWDSCMD	Window watchdog service command *R2)	17_H	00_H
FWDRSP	Functional watchdog response command *R2)	18_H	00_H
FWDRSPSYNC	Functional watchdog response command with synchronization *R2)	19_H	00_H
SYSFAIL	FAILSAFE error status flags *R1)	$1A_H$	00_H
INITERR	INIT error status flags *R2)	$1B_H$	00_H
IF	Interrupt flags *R2)	$1C_H$	00_H
SYSSF	System status flags *R2)	$1D_H$	00_H
WKSF	Wake-up status flags *R2)	$1E_H$	00_H
SPISF	SPI status flags *R2)	$1F_H$	00_H
MONSF0	Monitor status flags 0 *R1)	20_H	00_H
MONSF1	Monitor status flags 1 *R1)	21_H	00_H
MONSF2	Monitor status flags 2 *R2)	22_H	00_H
MONSF3	Monitor status flags 3 *R1)	23_H	00_H
OTFAIL	Overtemperature failure status flags *R1)	24_H	00_H
OTWRNSF	Overtemperature warning status flags *R2)	25_H	00_H
VMONSTAT	Voltage monitor status	26_H	00_H
DEVSTAT	Device status	27_H	00_H
PROTSTAT	Protection status *R1)	28_H	01_H
WWDSTAT	Window watchdog status *R3)	29_H	00_H
FWDSTAT0	Functional watchdog status 0 *R3)	$2A_H$	30_H

(table continues...)

45 Reset class of single bits is different. See register for details.

Table 32 (continued) Registers Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
FWDSTAT1	Functional watchdog status 1 *R3)	$2B_H$	00_H
ABIST_CTRL0	ABIST control 0 *R2) [45]	$2C_H$	00_H
ABIST_CTRL1	ABIST control 1 *R2)	$2D_H$	00_H
ABIST_SELECT0	ABIST select 0 *R2)	$2E_H$	00_H
ABIST_SELECT1	ABIST select 1 *R2)	$2F_H$	00_H
ABIST_SELECT2	ABIST select 2 *R2)	30_H	00_H
BCK_FREQ_CHANGE	Buck switching frequency change *R2)	31_H	00_H
BCK_FRE_SPREAD	Buck Frequency spread *R2)	32_H	00_H
CEFUMON	Central functions monitor status flags *R2)	$3B_H$	00_H
MCSMON	Microcontroller supervision monitor *R2)	$3C_H$	40_H
DEVINFO	Device info *R2)	$3D_H$	00_H
GTM	Global testmode *R1)	$3F_H$	02_H

Registers Access

The registers are addressed word-wise

12.4.1 Device registers

12.4.1.1 Device configuration 0 *R2)

DEVCFG0 Address: 00_H

Device configuration 0 *R2) Reset value: 08_H

7	6	5	4	3	2	1	0
WKTIMEN	**WKTIMCYC**	**WKTIM PRESC**	**nu**	**TRDEL**			
rw	rw	rw	none	rw			

Field	Bits	Type	Description
WKTIMEN	7	rw	**Wake timer enable** 0_D Wake timer disabled 1_D Wake timer enabled in SLEEP or STANDBY-state Reset: 0_H
WKTIMCYC	6	rw	**Wake timer cycle period** 0_D 10 us 1_D 10 ms

(table continues...)

45 Reset class of single bits is different. See register for details.

(continued)

Field	Bits	Type	Description
			Reset: 0_H
WKTIMPRESC	5	rw	**Wake timer cycle period pre-scaler** 0_D 1 1_D 100 Reset: 0_H
nu	4	none	Reset: 0_H
TRDEL	3:0	rw	**Transition delay into low power states** For STANDBY and SLEEP transition. Defined as a step of 100 us. 0_D 100 us 1_D 200 us 2_D 300 us $..._D$ ... 15_D 1600 us Reset: 8_H

12.4.1.2 Device configuration 1 *R0)

DEVCFG1 Address: 01_H

Device configuration 1 *R0) Reset value: 06_H

7	6	5	4	3	2	1	0
nu					**RESDEL**		
none					rw		

Field	Bits	Type	Description
nu	7:3	none	Reset: 00_H
RESDEL	2:0	rw	**Reset release delay time** 0_D 200 us 1_D 400 us 2_D 800 us 3_D 1ms 4_D 2 ms 5_D 4 ms 6_D 10 ms 7_D 15 ms Reset: 6_H

12.4.1.3 Device configuration 2 *R2) [46]

DEVCFG2 Address: 02_H

Device configuration 2 *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
EVCEN	**STU**	**FRE**	**CMONEN**	**CTHR**		**ESYNPHA**	**ESYNEN**
r	r	r	rw	rw		rw	rw

Field	Bits	Type	Description
EVCEN	7	r	**External core supply enable status** Bitfield does not follow the reset class as it indicates the status of a hardware configuration (pin SEC). 0_D External core supply disabled 1_D External core supply enabled Reset: 0_H
STU	6	r	**Step-up converter enable status** Bitfield does not follow the reset class as it indicates the status of a hardware configuration (pin STU). 0_D Disabled 1_D Enabled Reset: 0_H
FRE	5	r	**Step-down converter frequency selection status** Bitfield does not follow the reset class as it indicates the status of a hardware configuration (pin FRE). 0_D Step-down converter runs on low frequency range 1_D Step-down converter runs on high frequency range Reset: 0_H
CMONEN	4	rw	**QUC current monitor enable for transition to a low power state** For STANDBY and SLEEP transition. The setting is overwritten in SLEEP as current monitoring is always enabled. 0_D Disabled 1_D Enabled Reset: 0_H
CTHR	3:2	rw	**QUC current monitoring threshold value** 0_D 10 mA 1_D 30 mA 2_D 60 mA 3_D 100 mA Reset: 0_H

(table continues...)

46 Reset class of single bits is different. See register for details.

(continued)

Field	Bits	Type	Description
ESYNPHA	1	rw	**External synchronization output phase** 0_D No phase shift 1_D 180 phase shift Reset: 0_H
ESYNEN	0	rw	**Synchronization output for external switchmode regulator enable** 0_D Disable 1_D Enable Reset: 0_H

12.4.1.4 Protection register *R2)

PROTCFG Address: 03_H

Protection register *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
KEY							
rw							

Field	Bits	Type	Description
KEY	7:0	rw	**Protection key** Protection key register to request write access to protected registers. Unlock: write 32-bit sequence of 4 consecutive bytes (1: 0xAB 2:0xEF 3:0x56 4:0x12) to unlock access to protected registers. Lock: write 32-bit sequence of 4 consecutive bytes (1: 0xDF 2:0x34 3:0xBE 4:0xCA) to lock access to protected registers. All configured values are applied to SSC and WD module after the lock. AB_H Key 1 to unlock protected registers. EF_H Key 2 to unlock protected registers. 56_H Key 3 to unlock protected registers. 12_H Key 4 to unlock protected registers. DF_H Key 1 to lock protected registers. 34_H Key 2 to lock protected registers. BE_H Key 3 to lock protected registers. CA_H Key 4 to lock protected registers. Reset: 00_H

12.4.1.5 Protected system configuration request 0 *R1)

SYSPCFG0 Address: 04_H

Protected System configuration request 0 *R1) Reset value: 01_H

7	6	5	4	3	2	1	0
DISOFFSET	**nu**						**STBYEN**
rwp	none						rwp

Field	Bits	Type	Description
DISOFFSET	7	rwp	**Request for offset regulation of regulator QST related to QUC disable.** Valid for all device states except FAILSAFE and STANDBY. Data bits are sent inverted to SPI upon read access. 0_D Offset regulation enabled 1_D Offset regulation disabled Reset: 0_H
nu	6:1	none	**Not used bits shall be written as 0 and will always return 1 upon read** Reset: 00_H
STBYEN	0	rwp	**Request standby regulator QST enable** Valid for all device states except FAILSAFE. Data bits are sent inverted to SPI upon read access. 0_D Disabled 1_D Enabled Reset: 1_H

12.4.1.6 Protected system configuration request 1 *R2)

SYSPCFG1 Address: 05_H

Protected System configuration request 1 *R2) Reset value: 08_H

7	6	5	4	3	2	1	0
SS2DEL			**ERRSLPEN**	**ERREN**	**ERRRECEN**	**ERRREC**	
rwp			rwp	rwp	rwp	rwp	

Field	Bits	Type	Description
SS2DEL	7:5	rwp	**Request safe state 2 delay** Applied for transitions from NORMAL to INIT, WAKE and SLEEP-state. Data bits are sent inverted to SPI upon read access. 0_D no delay 1_D 10 ms 2_D 50 ms 3_D 100 ms 4_D 250 ms 5_D 1250 ms 6_D 2500 ms 7_D RESERVED Reset: 0_H
ERRSLPEN	4	rwp	**Request ERR pin monitor functionality enable while the system is in SLEEP** Data bits are sent inverted to SPI upon read access. 0_D ERR pin monitor is disabled in SLEEP 1_D ERR pin monitor can be active in SLEEP depending on ERREN bit value. Reset: 0_H
ERREN	3	rwp	**Request ERR pin monitor enable** Data bits are sent inverted to SPI upon read access. 0_D Disabled 1_D Enabled Reset: 1_H
ERRRECEN	2	rwp	**Request ERR pin monitor recovery enable** Data bits are sent inverted to SPI upon read access. 0_D Disabled 1_D Enabled Reset: 0_H
ERRREC	1:0	rwp	**Request ERR pin monitor recovery time** Data bits are sent inverted to SPI upon read access.

(table continues...)

(continued)

Field	Bits	Type	Description
			0_D 1 ms 1_D 2.5 ms 2_D 5 ms 3_D 10 ms Reset: 0_H

12.4.1.7 Protected watchdog configuration request 0 *R2)

WDCFG0 Address: 06_H

Protected Watchdog configuration request 0 *R2) Reset value: $9B_H$

7	6	5	4	3	2	1	0
WWDETHR				**WWDEN**	**FWDEN**	**WWDTSEL**	**WDCYC**
rwp				rwp	rwp	rwp	rwp

Field	Bits	Type	Description
WWDETHR	7:4	rwp	**Request window watchdog error threshold** WWD error threshold to generate reset and enter into INIT-state. Data bits are sent inverted to SPI upon read access. Reset: 9_H
WWDEN	3	rwp	**Request window watchdog enable** Data bits are sent inverted to SPI upon read access. 0_D Disabled 1_D Enabled Reset: 1_H
FWDEN	2	rwp	**Request functional watchdog enable** Data bits are sent inverted to SPI upon read access. 0_D Disabled 1_D Enabled Reset: 0_H
WWDTSEL	1	rwp	**Request window watchdog trigger selection** This is ignored when window watchdog is disabled. Data bits are sent inverted to SPI upon read access. 0_D External WDI input used as a WWD trigger 1_D WWD is triggered by SPI write to WWDSCMD register Reset: 1_H
WDCYC	0	rwp	**Request watchdog cycle time** Data bits are sent inverted to SPI upon read access. 0_D 0,1 ms tick period 1_D 1 ms tick period Reset: 1_H

12.4.1.8 Protected watchdog configuration request 1 *R2)

WDCFG1 Address: 07_H

Protected Watchdog configuration request 1 *R2) Reset value: 09_H

7	6	5	4	3	2	1	0
nu	**WDCYCDIV**	**nu**	**WDSLPEN**	**FWDETHR**			
none	rwp	none	rwp	rwp			

Field	Bits	Type	Description
nu	7	none	**not used bits shall be written as 0 and will always return 1 upon read** Reset: 0_H
WDCYCDIV	6	rwp	**Request enable of additional divider by 10 for watchdog cycle time (WDCYC) configuration** Data bits are sent inverted to SPI upon read access. 0_D Disabled 1_D Enabled, additional divider by 10 for watchdog cycle time (WDCYC) configuration is enabled Reset: 0_H
nu	5	none	**not used bits shall be written as 0 and will always return 1 upon read** Reset: 0_H
WDSLPEN	4	rwp	**Request watchdog functionality enable while the device is in SLEEP** Data bits are sent inverted to SPI upon read access. 0_D Disabled 1_D Enabled, the watchdogs work based on individual configuration (WWDEN & FWDEN) settings while the system is in SLEEP mode Reset: 0_H
FWDETHR	3:0	rwp	**Request functional watchdog error threshold** FWD error threshold to generate reset and enter into INIT-state. Data bits are sent inverted to SPI upon read access. Reset: 9_H

12.4.1.9 Protected Functional watchdog configuration request *R2)

FWDCFG Address: 08_H

Protected Functional watchdog configuration request *R2) Reset value: $0B_H$

7	6	5	4	3	2	1	0
nu			**WDHBTP**				
none			rwp				

Field	Bits	Type	Description
nu	7:5	none	**not used bits shall be written as 0 and will always return 1 upon read** Reset: 0_H
WDHBTP	4:0	rwp	**Request functional watchdog heartbeat timer period** Defined as a multiple of 50 watchdog cycles (**RWDCFG0**.WDCYC). Data bits are sent inverted to SPI upon read access. 0_D 50 wd cycles 1_D 100 wd cycles 2_D 150 wd cycles $..._D$ ... 31_D 1600 wd cycles Reset: $0B_H$

12.4.1.10 Protected window watchdog configuration request 0 *R2)

WWDCFG0 Address: 09_H

Protected Window watchdog configuration request 0 *R2) Reset value: 06_H

7	6	5	4	3	2	1	0
nu			**CW**				
none			rwp				

Field	Bits	Type	Description
nu	7:5	none	**not used bits shall be written as 0 and will always return 1 upon read** Reset: 0_H
CW	4:0	rwp	**Request window watchdog closed window time** Defined as a multiple of 50 watchdog cycles (**RWDCFG0**.WDCYC). Data bits are sent inverted to SPI upon read access. 0_D 50 wd cycles 1_D 100 wd cycles 2_D 150 wd cycles $..._D$ ... 31_D 1600 wd cycles Reset: 06_H

12.4.1.11 Protected window watchdog configuration request 1 *R2)

WWDCFG1 Address: $0A_H$

Protected Window watchdog configuration request 1 *R2) Reset value: $0B_H$

7	6	5	4	3	2	1	0
nu			**OW**				
none			rwp				

Field	Bits	Type	Description
nu	7:5	none	**not used bits shall be written as 0 and will always return 1 upon read** Reset: 0_H
OW	4:0	rwp	**Request window watchdog open window time** Defined as a multiple of 50 watchdog cycles (**RWDCFG0**.WDCYC). Data bits are sent inverted to SPI upon read access. 0_D 50 wd cycles 1_D 100 wd cycles 2_D 150 wd cycles $..._D$ ... 31_D 1600 wd cycles Reset: $0B_H$

12.4.1.12 System configuration 0 status *R0)

RSYSPCFG0 Address: $0B_H$

System configuration 0 status *R0) Reset value: 01_H

7	6	5	4	3	2	1	0
DISOFFSET	**nu**						**STBYEN**
r	none						r

Field	Bits	Type	Description
DISOFFSET	7	r	**Offset regulation of regulator QST related to QUC disable status.** Valid for all device states except FAILSAFE and STANDBY. 0_D Offset regulation enabled 1_D Offset regulation disabled Reset: 0_H
nu	6:1	none	Reset: 00_H
STBYEN	0	r	**Standby regulator QST enable status** Current configuration of standby regulator QST enable. Valid for all device states except FAILSAFE. 0_D Disabled 1_D Enabled Reset: 1_H

12.4.1.13 System configuration 1 status *R3) [47)]

RSYSPCFG1 Address: $0C_H$

System configuration 1 status *R3) Reset value: 08_H

7	6	5	4	3	2	1	0
SS2DEL			ERRSLPEN	ERREN	ERRRECEN	ERRREC	
r			r	r	r	r	

Field	Bits	Type	Description
SS2DEL	7:5	r	**Safe state 2 delay status** Current configuration of safe state 2 delay applied for transitions from NORMAL to INIT, WAKE and SLEEP-state. Bitfield has different reset class than whole register. The bitfield is reset according to *R2). 0_D no delay 1_D 10 ms 2_D 50 ms 3_D 100 ms 4_D 250 ms 5_D 1250 ms 6_D 2500 ms 7_D RESERVED Reset: 0_H
ERRSLPEN	4	r	**ERR pin monitor functionality enable status while the device is in SLEEP** Current configuration of ERR pin monitor functionality enable for SLEEP. 0_D ERR pin monitor is disabled in SLEEP 1_D ERR pin monitor can be active in SLEEP depending on ERREN bit value. Reset: 0_H
ERREN	3	r	**ERR pin monitor enable status** Current configuration of ERR pin monitor enable. 0_D Disabled 1_D Enabled Reset: 1_H
ERRRECEN	2	r	**ERR pin monitor recovery enable status** Current configuration of ERR pin monitor recovery enable. 0_D Disabled 1_D Enabled

(table continues...)

47 Reset class of single bits is different. See register for details.

(continued)

Field	Bits	Type	Description
			Reset: 0_H
ERRREC	1:0	r	**ERR pin monitor recovery time status** Current configuration of ERR pin monitor recovery time. 0_D 1 ms 1_D 2.5 ms 2_D 5 ms 3_D 10 ms Reset: 0_H

12.4.1.14 Watchdog configuration 0 status *R3)

RWDCFG0 Address: $0D_H$

Watchdog configuration 0 status *R3) Reset value: $9B_H$

7	6	5	4	3	2	1	0
WWDETHR				WWDEN	FWDEN	WWDTSEL	WDCYC
r				r	r	r	r

Field	Bits	Type	Description
WWDETHR	7:4	r	**Window watchdog error threshold status** Current configuration of WWD error threshold to generate reset and enter into INIT-state. Reset: 9_H
WWDEN	3	r	**Window watchdog enable status** Current configuration of WWD enable. 0_D Disabled 1_D Enabled Reset: 1_H
FWDEN	2	r	**Functional watchdog enable status** Current configuration of FWD enable. 0_D Disabled 1_D Enabled Reset: 0_H
WWDTSEL	1	r	**Window watchdog trigger selection status** Current configuration of WWD trigger selection. This is ignored when window watchdog is disabled. 0_D External WDI input used as a WWD trigger 1_D WWD is triggered by SPI write to WWDSCMD register Reset: 1_H
WDCYC	0	r	**Watchdog cycle time status** Current configuration of watchdog cycle time. 0_D 0,1 ms tick period 1_D 1 ms tick period Reset: 1_H

12.4.1.15 Watchdog configuration 1 status *R3)

RWDCFG1 Address: $0E_H$

Watchdog configuration 1 status *R3) Reset value: 09_H

7	6	5	4	3	2	1	0
nu	**WDCYCDIV**	**nu**	**WDSLPEN**	**FWDETHR**			
none	r	none	r	r			

Field	Bits	Type	Description
nu	7	none	Reset: 00_H
WDCYCDIV	6	r	**Additional divider by 10 for watchdog cycle time (WDCYC) configuration enable status** 0_D Disabled 1_D Enabled, additional divider by 10 for watchdog cycle time (WDCYC) configuration is enabled Reset: 0_H
nu	5	none	Reset: 00_H
WDSLPEN	4	r	**Watchdog functionality enable status while the device is in SLEEP** Current configuration of WD functionality enable for SLEEP. 0_D Disabled 1_D Enabled, the watchdogs work based on individual configuration (WWDEN & FWDEN) settings while the system is in SLEEP mode Reset: 0_H
FWDETHR	3:0	r	**Functional watchdog error threshold status** Current configuration of FWD error threshold to generate reset and enter into INIT-state. Reset: 9_H

12.4.1.16 Functional watchdog configuration status *R3)

RFWDCFG Address: $0F_H$

Functional watchdog configuration status *R3) Reset value: $0B_H$

7	6	5	4	3	2	1	0
nu			**WDHBTP**				
none			r				

Field	Bits	Type	Description
nu	7:5	none	Reset: 0_H
WDHBTP	4:0	r	**Functional watchdog heartbeat timer period status** Current configuration of FWD heartbeat timer period defined as a multiple of 50 watchdog cycles (**RWDCFG0**.WDCYC). 0_D 50 wd cycles 1_D 100 wd cycles 2_D 150 wd cycles $..._D$ ... 31_D 1600 wd cycles Reset: $0B_H$

12.4.1.17 Window watchdog configuration 0 status *R3)

RWWDCFG0 Address: 10_H

Window watchdog configuration 0 status *R3) Reset value: 06_H

7	6	5	4	3	2	1	0
nu			**CW**				
none			r				

Field	Bits	Type	Description
nu	7:5	none	Reset: 0_H
CW	4:0	r	**Window watchdog closed window time status** Current configuration of WWD closed window time defined as a multiple of 50 watchdog cycles (**RWDCFG0**.WDCYC). 0_D 50 wd cycles 1_D 100 wd cycles 2_D 150 wd cycles $..._D$ ... 31_D 1600 wd cycles Reset: 06_H

12.4.1.18 Window watchdog configuration 1 status *R3)

RWWDCFG1 Address: 11_H

Window watchdog configuration 1 status *R3) Reset value: $0B_H$

7	6	5	4	3	2	1	0
nu			**OW**				
none			r				

Field	Bits	Type	Description
nu	7:5	none	Reset: 0_H
OW	4:0	r	**Window watchdog open window time status** Current configuration of WWD open window time defined as a multiple of 50 watchdog cycles (**RWDCFG0**.WDCYC). 0_D 50 wd cycles 1_D 100 wd cycles 2_D 150 wd cycles $..._D$ ... 31_D 1600 wd cycles Reset: $0B_H$

12.4.1.19 Wake-up timer configuration 0 *R0)

WKTIMCFG0 Address: 12_H

Wake-up timer configuration 0 *R0) Reset value: 00_H

7	6	5	4	3	2	1	0
TIMVALL							
rw							

Field	Bits	Type	Description
TIMVALL	7:0	rw	**Wake-up timer value lower bits** Bits (7:0) of wake-up time defined as a multiple of wake-up timer cycles (**DEVCFG0**.WKTIMCYC). Reset: 00_H

12.4.1.20 Wake-up timer configuration 1 *R0)

WKTIMCFG1 Address: 13_H

Wake-up timer configuration 1 *R0) Reset value: 00_H

7	6	5	4	3	2	1	0
TIMVALM							
rw							

Field	Bits	Type	Description
TIMVALM	7:0	rw	**Wake-up timer value middle bits** Bits (15:8) of wake time-up defined as a multiple of wake-up timer cycles (**DEVCFG0**.WKTIMCYC). Reset: 00_H

12.4.1.21 Wake-up timer configuration 2 *R0)

WKTIMCFG2 Address: 14_H

Wake-up timer configuration 2 *R0) Reset value: 00_H

7	6	5	4	3	2	1	0
TIMVALH							
rw							

Field	Bits	Type	Description
TIMVALH	7:0	rw	**Wake-up timer value higher bits** Bits (23:16) of wake-up time defined as a multiple of wake-up timer cycles (**DEVCFG0**.WKTIMCYC). Reset: 00_H

12.4.1.22 Device control request *R2)

DEVCTRL Address: 15_H

Device control request *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
TRK2EN	**TRK1EN**	**COMEN**	**nu**	**VREFEN**	**STATEREQ**		
rw	rw	rw	none	rw	rwhc		

Field	Bits	Type	Description
TRK2EN	7	rw	**Request tracker 2 QT2 enable** 0_D QT2 is disabled after valid request 1_D QT2 is enabled after valid request Reset: 0_H
TRK1EN	6	rw	**Request tracker 1 QT1 enable** 0_D QT1 is disabled after valid request 1_D QT1 is enabled after valid request Reset: 0_H
COMEN	5	rw	**Request communication supply QCO enable** 0_D QCO is disabled after valid request 1_D QCO is enabled after valid request Reset: 0_H
nu	4	none	Reset: 0_H
VREFEN	3	rw	**Request voltage reference supply QVR enable** 0_D QVR is disabled after valid request 1_D QVR is enabled after valid request Reset: 0_H
STATEREQ	2:0	rwhc	**Request for device state transition** Cleared to 000 by the HW after the request is processed. After writing a new state value a user should not change the value before it's cleared by HW. 7_D RESERVED 6_D RESERVED 5_D WAKE 4_D STANDBY 3_D SLEEP 2_D NORMAL 1_D INIT 0_D NONE Reset: 0_H

12.4.1.23 Device control inverted request *R2)

DEVCTRLN Address: 16_H

Device control inverted request *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
TRK2EN	**TRK1EN**	**COMEN**	**nu**	**VREFEN**	**STATEREQ**		
rw	rw	rw	none	rw	rwhc		

Field	Bits	Type	Description
TRK2EN	7	rw	**Request tracker 2 QT2 enable** 1_D QT2 is disabled after valid request 0_D QT2 is enabled after valid request Reset: 0_H
TRK1EN	6	rw	**Request tracker 1 QT1 enable** 1_D QT1 is disabled after valid request 0_D QT1 is enabled after valid request Reset: 0_H
COMEN	5	rw	**Request communication supply QCO enable** 1_D QCO is disabled after valid request 0_D QCO is enabled after valid request Reset: 0_H
nu	4	none	Reset: 0_H
VREFEN	3	rw	**Request voltage reference supply QVR enable** 1_D QVR is disabled after valid request 0_D QVR is enabled after valid request Reset: 0_H
STATEREQ	2:0	rwhc	**Request for device state transition** Cleared to 000 by the HW after the request is processed. After writing a new state value a user should not change the value before it's cleared by HW. 7_D NONE 6_D INIT 5_D NORMAL 4_D SLEEP 3_D STANDBY 2_D WAKE 1_D RESERVED 0_D RESERVED Reset: 0_H

12.4.1.24 Window watchdog service command *R2)

WWDSCMD Address: 17_H

Window watchdog service command *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
TRIG_STATUS	**nu**						**TRIG**
r	none						rw

Field	Bits	Type	Description
TRIG_STATUS	7	r	**Last SPI trigger received** Reset: 0_H
nu	6:1	none	Reset: 00_H
TRIG	0	rw	**Window watchdog SPI trigger command** Read TRIG_STATUS bit first and write inverted value to TRIG bit. Reset: 0_H

12.4.1.25 Functional watchdog response command *R2)

FWDRSP Address: 18_H

Functional watchdog response command *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
FWDRSP							
rw							

Field	Bits	Type	Description
FWDRSP	7:0	rw	**Functional watchdog response** Write functional watchdog response bytes to this field. Reset: 00_H

12.4.1.26 Functional watchdog response command with synchronization *R2)

FWDRSPSYNC Address: 19_H

Functional watchdog response command with synchronization *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
FWDRSPS							
rw							

Field	Bits	Type	Description
FWDRSPS	7:0	rw	**Functional watchdog heartbeat synchronization response** Write the last functional watchdog response byte to this field to synchronize/restart the heartbeat. Reset: 00_H

12.4.1.27 FAILSAFE error status flags *R1)

SYSFAIL Address: $1A_H$

FAILSAFE error status flags *R1) Reset value: 00_H

7	6	5	4	3	2	1	0
INITF	**ABISTERR**	**nu**		**BUCKHS**	**VMONF**	**OTF**	**VOLTSELERR**
rw1c	rw1c	none		rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
INITF	7	rw1c	**3rd initialization timeout failure flag** 3rd initialization timeout failure due to the third consecutive initialization timeout failure. i.e. The device restarts INIT phase from FAILSAFE. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H
ABISTERR	6	rw1c	**ABIST operation interrupted flag** ABIST interrupted by any fault/event which is not part of ABIST. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H
nu	5:4	none	Reset: 0_H
BUCKHS	3	rw1c	**Buck converter monitor failure flag** Buck converter failure occurred which lead to FAILSAFE. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H
VMONF	2	rw1c	**Voltage monitor failure flag** Voltage monitor failure occurred which lead to FAILSAFE. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags, read **MONSF0**, **MONSF1** and **MONSF3** for details Reset: 0_H
OTF	1	rw1c	**Overtemperature failure flag** 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags, read **OTFAIL** for details Reset: 0_H
VOLTSELERR	0	rw1c	**Double Bit error on voltage selection flag** Device entered FAILSAFE-state due to internal voltage selection failure.

(table continues...)

(continued)

Field	Bits	Type	Description
			0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H

12.4.1.28 INIT error status flags *R2)

INITERR Address: $1B_H$

INIT error status flags *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
HARDRES	**SOFTRES**	**ERRF**	**FWDF**	**WWDF**	**VMONF**	**nu**	
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	

Field	Bits	Type	Description
HARDRES	7	rw1c	**Hard reset flag** Hard reset has been generated due to the second consecutive initialization timeout failure. i.e. The device restarts INIT phase for the third time. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H
SOFTRES	6	rw1c	**Soft reset flag** Soft reset has been generated due to the first initialization timeout failure. i.e. The device restarts INIT phase for the 2nd time. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H
ERRF	5	rw1c	**Error monitoring failure flag** 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H
FWDF	4	rw1c	**Functional watchdog error counter overflow failure flag** Functional watchdog error counter reached the error threshold. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H
WWDF	3	rw1c	**Window watchdog error counter overflow failure flag** Window watchdog error counter reached the error threshold. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags Reset: 0_H
VMONF	2	rw1c	**Voltage monitor failure flag** Voltage monitor failure occurred which lead to INIT. 0_D No fault, write 0 - no action 1_D Fault occurred, write 1 to clear the flags, read **MONSF2** for details

(table continues...)

(continued)

Field	Bits	Type	Description
			Reset: 0_H
nu	1:0	rw1c	Reset: 0_H

12.4.1.29 Interrupt flags *R2)

IF Address: $1C_H$

Interrupt flags *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
INTMISS	**ABIST**	**OTF**	**OTW**	**MON**	**SPI**	**WK**	**SYS**
r	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
INTMISS	7	r	**Interrupt not serviced in time flag** Interrupt has not been serviced within $t_{INT,TO}$ time 0_D No interrupt timeout happened 1_D Interrupt timeout happened, cleared by hardware when all other flags in IF are cleared. Reset: 0_H
ABIST	6	rw1c	**Requested ABIST operation performed flag** 0_D No interrupt, write 0 - no action 1_D Interrupt flag active, write 1 to clear the flag Reset: 0_H
OTF	5	rw1c	**Overtemperature failure interrupt flag** 0_D No interrupt, write 0 - no action 1_D Interrupt flag active, write 1 to clear the flag, read **OTFAIL** for details Reset: 0_H
OTW	4	rw1c	**Overtemperature warning interrupt flag** 0_D No interrupt, write 0 - no action 1_D Interrupt flag active, write 1 to clear the flag, read **OTWRNSF** for details Reset: 0_H
MON	3	rw1c	**Monitor interrupt flag** 0_D No interrupt, write 0 - no action 1_D Interrupt flag active, write 1 to clear the flag, read **MONSF0**, **MONSF1**, **MONSF2** and **MONSF3** for details Reset: 0_H
SPI	2	rw1c	**SPI interrupt flag** 0_D No interrupt, write 0 - no action 1_D Interrupt flag active, write 1 to clear the flag, read **SPISF** for details Reset: 0_H
WK	1	rw1c	**Wake interrupt flag** Only set if device generates an interrupt when leaving SLEEP-state.

(table continues...)

(continued)

Field	Bits	Type	Description
			0_D No interrupt, write 0 - no action 1_D Interrupt flag active, write 1 to clear the flag, read **WKSF** for details Reset: 0_H
SYS	0	rw1c	**System interrupt flag** 0_D No interrupt, write 0 - no action 1_D Interrupt flag active, write 1 to clear the flag, read **SYSSF** for details Reset: 0_H

12.4.1.30 System status flags *R2)

SYSSF Address: $1D_H$

System status flags *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
nu		**NO_OP**	**TRFAIL**	**ERRMISS**	**FWDE**	**WWDE**	**CFGE**
none		rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
nu	7:6	none	Reset: 0_H
NO_OP	5	rw1c	**State transition request failure flag** Requested state transition via DEVCTRL & DEVCTRLN could not be performed because of wrong protocol. 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
TRFAIL	4	rw1c	**Transition to low power failed flag** Transition to low power failed either due to the QUC current monitor, WAK high level or a rising edge on ENA during TRDEL time. 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
ERRMISS	3	rw1c	**MCU error miss status flag** Set only when SYSPCFG1.ERRRECEN='1' 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
FWDE	2	rw1c	**Functional watchdog error interrupt flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
WWDE	1	rw1c	**Window watchdog error interrupt flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
CFGE	0	rw1c	**Protected configuration double bit error flag** Double bit error occurred on protected configuration register. Status registers shall be read in order to determine which configuration has changed. 0_D Write 0 - no action

(table continues...)

(continued)

Field	Bits	Type	Description
			1_D Event detected, write 1 to clear the flag Reset: 0_H

12.4.1.31 Wake-up status flags *R2)

WKSF Address: $1E_H$

Wake-up status flags *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
WAKST	**ENAST**	**nu**	**WKSPI**	**WKTIM**	**CMON**	**ENA**	**WAK**
r	r	none	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
WAKST	7	r	**WAK input status** 0_D Voltage at pin WAK is in low level signal range 1_D Voltage at pin WAK is in high level signal range Reset: 0_H
ENAST	6	r	**ENA input status** 0_D Voltage at pin ENA is in low level signal range 1_D Voltage at pin ENA is in high level signal range Reset: 0_H
nu	5	none	Reset: 0_H
WKSPI	4	rw1c	**Wake-up from SLEEP by SPI flag ("Go to WAKE" command)** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
WKTIM	3	rw1c	**Wake-up by wake-up timer expiry flag** Bit is set as well if STANDBY-state left because of wake timer expired. 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
CMON	2	rw1c	**QUC current monitor threshold wake-up flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
ENA	1	rw1c	**Wake-up by ENA signal flag** Bit is set as well if FAILSAFE or STANDBY-state left because of ENA. 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
WAK	0	rw1c	**Wake-up by WAK signal flag** Bit is set as well if FAILSAFE or STANDBY-state left because of WAK.

(table continues...)

(continued)

Field	Bits	Type	Description
			0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

12.4.1.32 SPI status flags *R2)

SPISF Address: $1F_H$

SPI status flags *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
nu			**LOCK**	**DURE**	**ADDRE**	**LENE**	**PARE**
none			rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
nu	7:5	none	Reset: 0_H
LOCK	4	rw1c	**LOCK or UNLOCK procedure error flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
DURE	3	rw1c	**SPI frame duration error flag** SCS low for more than 2 ms. 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
ADDRE	2	rw1c	**SPI address invalid flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
LENE	1	rw1c	**SPI frame length invalid flag** Number of detected SPI clock cycles different than 16. 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
PARE	0	rw1c	**SPI frame parity error flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

12.4.1.33 Monitor status flags 0 *R1)

MONSF0 Address: 20_H

Monitor status flags 0 *R1) Reset value: 00_H

7	6	5	4	3	2	1	0
TRK2SG	**TRK1SG**	**VREFSG**	**COMSG**	**VCORESG**	**STBYSG**	**UCSG**	**PREGSG**
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
TRK2SG	7	rw1c	**Tracker 2 (QT2) short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
TRK1SG	6	rw1c	**Tracker 1 (QT1) short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
VREFSG	5	rw1c	**Voltage reference supply (QVR) short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
COMSG	4	rw1c	**Communication supply (QCO) short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
VCORESG	3	rw1c	**Core voltage monitor (VCI) short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
STBYSG	2	rw1c	**Standby supply (QST) short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
UCSG	1	rw1c	**MCU supply (QUC) short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
PREGSG	0	rw1c	**Pre regulator (FB) short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag

(table continues...)

(continued)

Field	Bits	Type	Description
			Reset: 0_H

12.4.1.34 Monitor status flags 1 *R1)

MONSF1 Address: 21_H

Monitor status flags 1 *R1) Reset value: 00_H

VR

7	6	5	4	3	2	1	0
TRK2OV	**TRK1OV**	**VREFOV**	**COMOV**	**VCOREOV**	**STBYOV**	**UCOV**	**PREGOV**
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
TRK2OV	7	rw1c	**Tracker 2 (QT2) overvoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
TRK1OV	6	rw1c	**Tracker 1 (QT1) supply overvoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
VREFOV	5	rw1c	**Voltage reference supply (QVR) overvoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
COMOV	4	rw1c	**Communication supply (QCO) overvoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
VCOREOV	3	rw1c	**Core voltage monitor (VCI) overvoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
STBYOV	2	rw1c	**Standby supply (QST) overvoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
UCOV	1	rw1c	**MCU supply (QUC) overvoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
PREGOV	0	rw1c	**Pre regulator (FB) overvoltage status flag** 0_D Write 0 - no action

(table continues...)

(continued)

Field	Bits	Type	Description
			1_D Event detected, write 1 to clear the flag Reset: 0_H

12.4.1.35 Monitor status flags 2 *R2)

MONSF2 Address: 22_H

Monitor status flags 2 *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
TRK2UV	**TRK1UV**	**VREFUV**	**COMUV**	**VCOREUV**	**STBYUV**	**UCUV**	**PREGUV**
rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
TRK2UV	7	rw1c	**Tracker 2 (QT2) undervoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
TRK1UV	6	rw1c	**Tracker 1 (QT1) undervoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
VREFUV	5	rw1c	**Voltage reference supply (QVR) undervoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
COMUV	4	rw1c	**Communication supply (QCO) undervoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
VCOREUV	3	rw1c	**Core voltage monitor (VCI) undervoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
STBYUV	2	rw1c	**Standby supply (QST) undervoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
UCUV	1	rw1c	**MCU supply (QUC) undervoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
PREGUV	0	rw1c	**Pre-regulator (FB) undervoltage status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag

(table continues...)

(continued)

Field	Bits	Type	Description
			Reset: 0_H

12.4.1.36 Monitor status flags 3 *R1)

MONSF3 Address: 23_H

Monitor status flags 3 *R1) Reset value: 00_H

7	6	5	4	3	2	1	0
BIASHI	**BIASLOW**	**BG12OV**	**BG12UV**	**nu**	**PREGBIST**	**STUSG**	**VBATOV**
rw1c	rw1c	rw1c	rw1c	none	rw1c	rw1c	rw1c

Field	Bits	Type	Description
BIASHI	7	rw1c	**Bias current too high flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
BIASLOW	6	rw1c	**Bias current too low flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
BG12OV	5	rw1c	**Bandgap comparator overvoltage condition flag** (VBG1 ≥ VBG2 + 4%) 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
BG12UV	4	rw1c	**Bandgap comparator undervoltage condition flag** (VBG1 ≤ VBG2 - 4%) 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
nu	3	none	Reset: 0_H
PREGBIST	2	rw1c	**Step-down regulator BIST failure status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
STUSG	1	rw1c	**Step-up regulator short to ground status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
VBATOV	0	rw1c	**Supply voltage VSx overvoltage flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

12.4.1.37 Overtemperature failure status flags *R1)

OTFAIL Address: 24_H

Overtemperature failure status flags *R1) Reset value: 00_H

7	6	5	4	3	2	1	0
MON	**nu**		**COM**	**nu**		**UC**	**PREG**
rw1c	none		rw1c	none		rw1c	rw1c

Field	Bits	Type	Description
MON	7	rw1c	**Monitoring overtemperature flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
nu	6:5	none	Reset: 0_H
COM	4	rw1c	**Communication supply (QCO) overtemperature flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
nu	3:2	none	Reset: 0_H
UC	1	rw1c	**MCU supply (QUC) overtemperature flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
PREG	0	rw1c	**Pre-regulator overtemperature flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

12.4.1.38 Overtemperature warning status flags *R2)

OTWRNSF Address: 25_H

Overtemperature warning status flags *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
nu		**VREF**	**COM**	**nu**	**STBY**	**UC**	**PREG**
none		rw1c	rw1c	none	rw1c	rw1c	rw1c

Field	Bits	Type	Description
nu	7:6	none	Reset: 0_H
VREF	5	rw1c	**Voltage reference supply (QVR) over load flag** (overcurrent for more than 1ms) 0_D Write 0 no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
COM	4	rw1c	**Communication supply (QCO) overtemperature warning flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
nu	3	none	Reset: 0_H
STBY	2	rw1c	**Standby supply (QST) over load flag** (overcurrent for more than 1ms) 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
UC	1	rw1c	**MCU supply (QUC) overtemperature warning flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
PREG	0	rw1c	**Pre-regulator overtemperature warning flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

12.4.1.39 Voltage monitor status

VMONSTAT Address: 26_H

Voltage monitor status Reset value: 00_H

7	6	5	4	3	2	1	0
TRK2ST	**TRK1ST**	**VREFST**	**COMST**	**VCOREST**	**STBYST**	**nu**	**PREGST**
r	r	r	r	r	r	none	r

Field	Bits	Type	Description
TRK2ST	7	r	**Tracker 2 (QT2) voltage status** 0_D Voltage is out of range or not enabled 1_D Voltage is OK Reset: 0_H
TRK1ST	6	r	**Tracker 1 (QT1) voltage status** 0_D Voltage is out of range or not enabled 1_D Voltage is OK Reset: 0_H
VREFST	5	r	**Voltage reference supply (QVR) voltage status** 0_D Voltage is out of range or not enabled 1_D Voltage is OK Reset: 0_H
COMST	4	r	**Communication supply (QCO) voltage status** 0_D Voltage is out of range or not enabled 1_D Voltage is OK Reset: 0_H
VCOREST	3	r	**Core voltage monitor (VCI) voltage status** 0_D Voltage is out of range or not enabled 1_D Voltage is OK Reset: 0_H
STBYST	2	r	**Standby supply (QST) voltage status** 0_D Voltage is out of range or not enabled 1_D Voltage is OK Reset: 0_H
nu	1	none	Reset: 0_H
PREGST	0	r	**Pre regulator (FB) voltage status** 0_D Voltage is out of range or not enabled 1_D Voltage is OK Reset: 0_H

12.4.1.40 Device status

DEVSTAT Address: 27_H

Device status Reset value: 00_H

7	6	5	4	3	2	1	0
TRK2EN	**TRK1EN**	**COMEN**	**STBYEN**	**VREFEN**	**STATE**		
r	r	r	r	r	r		

Field	Bits	Type	Description
TRK2EN	7	r	**Tracker 2 (QT2) enable status** 0_D Voltage is disabled 1_D Voltage is enabled Reset: 0_H
TRK1EN	6	r	**Tracker 1 (QT1) enable status** 0_D Voltage is disabled 1_D Voltage is enabled Reset: 0_H
COMEN	5	r	**Communication supply (QCO) enable status** 0_D Voltage is disabled 1_D Voltage is enabled Reset: 0_H
STBYEN	4	r	**Standby supply (QST) enable status** 0_D Voltage is disabled 1_D Voltage is enabled Reset: 0_H
VREFEN	3	r	**Reference voltage supply (QVR) enable status** 0_D Voltage is disabled 1_D Voltage is enabled Reset: 0_H
STATE	2:0	r	**Device state** 7_D RESERVED 6_D RESERVED 5_D WAKE 4_D STANDBY 3_D SLEEP 2_D NORMAL 1_D INIT 0_D NONE Reset: 0_H

12.4.1.41 Protection status *R1)

PROTSTAT Address: 28_H

Protection status *R1) Reset value: 01_H

7	6	5	4	3	2	1	0
KEY4OK	**KEY3OK**	**KEY2OK**	**KEY1OK**	**nu**			**LOCK**
r	r	r	r	none			r

Field	Bits	Type	Description
KEY4OK	7	r	**Key4 ok status** Information about validity of the 4th received protection key byte 0_D Key not valid 1_D Key valid Reset: 0_H
KEY3OK	6	r	**Key3 ok status** Information about validity of the 3rd received protection key byte 0_D Key not valid 1_D Key valid Reset: 0_H
KEY2OK	5	r	**Key2 ok status** Information about validity of the 2nd received protection key byte 0_D Key not valid 1_D Key valid Reset: 0_H
KEY1OK	4	r	**Key1 ok status** Information about validity of the 1st received protection key byte 0_D Key not valid 1_D Key valid Reset: 0_H
nu	3:1	none	Reset: 0_H
LOCK	0	r	**Protected register lock status** 0_D Access is unlocked 1_D Access is locked Reset: 1_H

12.4.1.42 Window watchdog status *R3)

WWDSTAT Address: 29_H

Window watchdog status *R3) Reset value: 00_H

7	6	5	4	3	2	1	0
nu				**WWDECNT**			
none				r			

Field	Bits	Type	Description
nu	7:4	none	Reset: 0_H
WWDECNT	3:0	r	**Window watchdog error counter status** Reset: 0_H

12.4.1.43 Functional watchdog status 0 *R3)

FWDSTAT0 Address: $2A_H$

Functional watchdog status 0 *R3) Reset value: 30_H

7	6	5	4	3	2	1	0
nu	**FWDRSPOK**	**FWDRSPC**		**FWDQUEST**			
none	r	r		r			

Field	Bits	Type	Description
nu	7	none	Reset: 0_H
FWDRSPOK	6	r	**Functional watchdog response check error status** 0_D Response message is wrong 1_D All received bytes in response message are correct Reset: 0_H
FWDRSPC	5:4	r	**Functional watchdog response counter value** Reset: 3_H
FWDQUEST	3:0	r	**Functional watchdog question** Reset: 0_H

12.4.1.44 Functional watchdog status 1 *R3)

FWDSTAT1 Address: $2B_H$

Functional watchdog status 1 *R3) Reset value: 00_H

7	6	5	4	3	2	1	0
nu				**FWDECNT**			
none				r			

Field	Bits	Type	Description
nu	7:4	none	Reset: 0_H
FWDECNT	3:0	r	**Functional watchdog error counter value** Reset: 0_H

12.4.1.45 ABIST control 0 *R2) [48)]

ABIST_CTRL0 Address: $2C_H$

ABIST control0 *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
STATUS				**INT**	**SINGLE**	**PATH**	**START**
r				rw	rw	rw	rwhc

Field	Bits	Type	Description
STATUS	7:4	r	**ABIST global error status** ABIST status information after requested operation has been performed, information shall only be considered valid, once START bit is cleared. Bits have different reset class than whole register. Bitfield has different reset class than whole register. The bitfield is reset according to *R1). 5_D Selected ABIST operation performed with no errors 10_D Selected ABIST operation performed with errors, check respective SELECT registers Reset: 0_H
INT	3	rw	**Safety path selection** Select whether safe state or interrupt related comparator shall be tested. 0_D safe state related comparators shall be tested 1_D interrupt related comparators shall be tested Reset: 0_H
SINGLE	2	rw	**ABIST Sequence selection** Select whether a single comparator shall be tested or all comparators in predefined sequence 0_D Predefined sequence 1_D Single comparator test Reset: 0_H
PATH	1	rw	**Full path test selection** Select the path which should be covered by ABIST operation 0_D Comparator only 1_D Comparator and corresponding deglitching logic, shall be selected in case contribution to respective safety measure needs to be tested Reset: 0_H
START	0	rwhc	**Start ABIST operation** The ABIST operation itself is started. This bit is cleared after ABIST operation has been performed

(table continues...)

48 Reset class of single bits is different. See register for details.

(continued)

Field	Bits	Type	Description
			0_D Operation done 1_D Start operation Reset: 0_H

12.4.1.46 ABIST control 1 *R2)

ABIST_CTRL1 Address: $2D_H$

ABIST control1 *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
nu						**ABIST_CLK_EN**	**OV_TRIG**
none						rw	rw

Field	Bits	Type	Description
nu	7:2	none	Reset: 00_H
ABIST_CLK_EN	1	rw	**ABIST clock check enable** Select ABIST clock to check its functionality 0_D Disable 1_D Enable Reset: 0_H
OV_TRIG	0	rw	**Overvoltage trigger for secondary internal monitor enable** 0_D Disable 1_D Enable Reset: 0_H

12.4.1.47 ABIST select 0 *R2)

ABIST_SELECT0 Address: $2E_H$

ABIST select 0 *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
TRK2OV	**TRK1OV**	**VREFOV**	**COMOV**	**VCOREOV**	**STBYOV**	**UCOV**	**PREGOV**
rwhu	rwhu	rwhu	rwhu	rwhu	rwhu	rwhu	rwhu

Field	Bits	Type	Description
TRK2OV	7	rwhu	**Select tracker 2 (QT2) OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
TRK1OV	6	rwhu	**Select tracker 1 (QT1) OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
VREFOV	5	rwhu	**Select voltage reference supply (QVR) OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
COMOV	4	rwhu	**Select communication supply (QCO) OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
VCOREOV	3	rwhu	**Select core voltage monitor (VCI) OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
STBYOV	2	rwhu	**Select standby supply (QST) OV comparator for ABIST operation**

(table continues...)

(continued)

Field	Bits	Type	Description
			0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
UCOV	1	rwhu	**Select MCU supply (QUC) OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
PREGOV	0	rwhu	**Select pre regulator (FB) OV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H

12.4.1.48 ABIST select 1 *R2)

ABIST_SELECT1 Address: $2F_H$

ABIST select 1 *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
TRK2UV	**TRK1UV**	**VREFUV**	**COMUV**	**VCOREUV**	**STBYUV**	**UCUV**	**PREGUV**
rwhu	rwhu	rwhu	rwhu	rwhu	rwhu	rwhu	rwhu

Field	Bits	Type	Description
TRK2UV	7	rwhu	**Select tracker 2 (QT2) UV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
TRK1UV	6	rwhu	**Select tracker 1 (QT1) UV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this voltage Reset: 0_H
VREFUV	5	rwhu	**Select voltage reference supply (QVR) UV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
COMUV	4	rwhu	**Select communication supply (QCO) UV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
VCOREUV	3	rwhu	**Select core voltage monitor (VCI) UV comparator for ABIST operation** 0_D Not selected 1_D selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
STBYUV	2	rwhu	**Select standby supply (QST) UV comparator for ABIST operation**

(table continues...)

(continued)

Field	Bits	Type	Description
			0_D Not selected 1_D selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
UCUV	1	rwhu	**Select MCU supply (QUC) UV comparator for ABIST operation** 0_D Not selected 1_D selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
PREGUV	0	rwhu	**Select pre regulator (FB) UV comparator for ABIST operation** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H

12.4.1.49 ABIST select 2 *R2)

ABIST_SELECT2 Address: 30_H

ABIST select 2 *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
BIASHI	**BIASLOW**	**BG12OV**	**BG12UV**	**nu**			**VBATOV**
rwhu	rwhu	rwhu	rwhu	none			rwhu

Field	Bits	Type	Description
BIASHI	7	rwhu	**Select bias current too high** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
BIASLOW	6	rwhu	**Select bias current too low** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
BG12OV	5	rwhu	**Select bandgap comparator OV condition** (VBG1 ≥ VBG2 + 4%) 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
BG12UV	4	rwhu	**Select bandgap comparator UV condition** (VBG1 ≤ VBG2 - 4%) 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H
nu	3:1	none	Reset: 0_H
VBATOV	0	rwhu	**Select supply VSx overvoltage** 0_D Not selected 1_D Selected, bit will be cleared upon successful ABIST operation on comparator, bit will be set in case of ABIST fail for this comparator Reset: 0_H

12.4.1.50 Buck switching frequency change *R2)

BCK_FREQ_CHANGE Address: 31_H

Buck switching frequency change *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
BCK_DRV_STGE	**nu**				**BCK_FREQ_SEL**		
rw	none				rw		

Field	Bits	Type	Description
BCK_DRV_STGE	7	rw	**BUCK driving stage selection** The switching speed of the step down regulator power stages can be adjusted in two configurations to optimize for efficiency or emissions. 1_D Weak driving stage for slower switching 0_D Strong driving stage for faster switching Reset: 0_H
nu	6:3	none	Reset: 00_H
BCK_FREQ_SEL	2:0	rw	**BUCK switching frequency change** For manual adjustment of buck frequency in fixed variations from the nominal frequency $f_{OSC,step\text{-}down}$ 7_D Change buck frequency by approx. -5.0% from $f_{OSC,step\text{-}down}$ 6_D Change buck frequency by approx. -3.3% from $f_{OSC,step\text{-}down}$ 5_D Change buck frequency by approx. -1.7% from $f_{OSC,step\text{-}down}$ 4_D No change 3_D Change buck frequency by approx. +5.0% from $f_{OSC,step\text{-}down}$ 2_D Change buck frequency by approx. +3.3% from $f_{OSC,step\text{-}down}$ 1_D Change buck frequency by approx. +1.7% from $f_{OSC,step\text{-}down}$ 0_D No Change Reset: 0_H

12.4.1.51 Buck Frequency spread *R2)

BCK_FRE_SPREAD Address: 32_H

Buck Frequency spread *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
FRE_SP_THR							
rw							

Field	Bits	Type	Description
FRE_SP_THR	7:0	rw	**Spread spectrum** Select the percentage of frequency spread(±). The mean frequency is reduced by the percentage as well keeping the maximum frequency at the nominal frequency selected by FRE. 00_H No spread 55_H +0% / -2.5% frequency spread 80_H +/-2.5% frequency spread AA_H +/-5.0% frequency spread $D5_H$ +/-7.5% frequency spread FF_H +7.5% / -10.0% frequency spread others not used Reset: 00_H

12.4.1.52 Central functions monitor status flags *R2)

CEFUMON Address: $3B_H$

Central functions monitor status flags *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
STUOC	**nu**			**CEFU3**	**CEFU2**	**CEFU1**	**CEFU0**
rw1c	none			rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
STUOC	7	rw1c	**Step-up regulator over current prewarning status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
nu	6:4	none	Reset: 0_H
CEFU3	3	rw1c	**Internal regulator backup for switchable power domain failure status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
CEFU2	2	rw1c	**Internal regulator for switchable power domain failure status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
CEFU1	1	rw1c	**Internal regulator backup for always on power domain failure status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H
CEFU0	0	rw1c	**Internal regulator for always on power domain failure status flag** 0_D Write 0 - no action 1_D Event detected, write 1 to clear the flag Reset: 0_H

12.4.1.53 Microcontroller supervision monitor *R2)

MCSMON Address: $3C_H$

Microcontroller supervision monitor *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
MPS	**MPSPIN**	**CYCMON**					
rw	r	r					

Field	Bits	Type	Description
MPS	7	rw	**Microcontroller programming support enable (OR combination with MPS pin)** 0_D Disabled via SPI (unless enabled by MPS pin high) 1_D Enabled via SPI (independent of MPS pin) Reset: 0_H
MPSPIN	6	r	**Microcontroller programming support enable (OR combination with MPS bitfield)** 0_D Disabled via pin MPS (unless enabled by MPS bitfield being set) 1_D Enabled via SPI (independent of MPS bitfield) Reset: 0_H
CYCMON	5:0	r	**Watchdog cycle timer monitor** 0_D 0 wd cycles passed 1_D 1 wd cycles passed 2_D 2 wd cycles passed 50_D 50 wd cycles passed 51_D not used 63_D not used Reset: 0_H

12.4.1.54 Device info *R2)

DEVINFO Address: $3D_H$

Device info *R2) Reset value: 00_H

7	6	5	4	3	2	1	0
nu	**CHIPSTEP**						
none	r						

Field	Bits	Type	Description
nu	7	none	Reset: 0_H
CHIPSTEP	6:0	r	**Chip design step (Hamming [7,4] coded: p1p2d1p3d2d3d4)** 00_H Blocked for predecessor device TLF35584 33_H TLF35585xxS01 (5V0) B21-Step $5A_H$ TLF35585xxS02 (3V3) B21-Step Reset: 0_H

12.4.1.55 Global testmode *R1)

GTM Address: $3F_H$

Global testmode *R1) Reset value: 02_H

7	6	5	4	3	2	1	0
nu						**NTM**	**TM**
none						r	r

Field	Bits	Type	Description
nu	7:2	none	Reset: 00_H
NTM	1	r	**Test mode inverted status** 0_D Device is in test mode 1_D Device is in normal mode Reset: 1_H
TM	0	r	**Test mode status** 0_D Device is in normal mode 1_D Device is in test mode Reset: 0_H

12.5 Electrical characteristics SPI signals

Table 33 Electrical characteristics SPI signals

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Pin SCS, Chip Select							
Chip select valid high level TLF35585QVS01	$V_{SCS, hi}$	3.6	–	–	V	V_{SCS} increasing; V_{QUC} = 5.0 V	P_13.5.1
Chip select valid low level TLF35585QVS01	$V_{SCS, lo}$	–	–	0.8	V	V_{SCS} decreasing; V_{QUC} = 5.0 V	P_13.5.2
Chip select hysteresis TLF35585QVS01	$V_{SCS, hyst}$	200	600	1200	mV	V_{QUC} = 5.0 V	P_13.5.3
Chip select valid high level TLF35585QVS02	$V_{SCS, hi}$	2.0	–	–	V	V_{SCS} increasing; V_{QUC} = 3.3 V	P_13.5.4
Chip select valid low level TLF35585QVS02	$V_{SCS, lo}$	–	–	0.8	V	V_{SCS} decreasing; V_{QUC} = 3.3 V	P_13.5.5
Chip select hysteresis TLF35585QVS02	$V_{SCS, hyst}$	100	300	600	mV	V_{QUC} = 3.3 V	P_13.5.6
Chip select pull-up current	I_{SCS}	-175	-120	–	µA	V_{SCS} = 0 V	P_13.5.7
Chip select input capacitance	C_{SCS}	–	4	15	pF	[49]	P_13.5.8
Pin SCL, Clock							
Clock signal valid high level TLF35585QVS01	$V_{SCL, hi}$	3.6	–	–	V	V_{SCL} increasing; V_{QUC} = 5.0 V	P_13.5.9
Clock signal valid low level TLF35585QVS01	$V_{SCL, lo}$	–	–	0.8	V	V_{SCL} decreasing; V_{QUC} = 5.0 V	P_13.5.10
Clock hysteresis TLF35585QVS01	$V_{SCL, hyst}$	200	600	1200	mV	V_{QUC} = 5.0 V	P_13.5.11
Clock signal valid high level TLF35585QVS02	$V_{SCL, hi}$	2.0	–	–	V	V_{SCL} increasing; V_{QUC} = 3.3 V	P_13.5.12
Clock signal valid low level TLF35585QVS02	$V_{SCL, lo}$	–	–	0.8	V	V_{SCL} decreasing; V_{QUC} = 3.3 V	P_13.5.13
Clock hysteresis TLF35585QVS02	$V_{SCL, hyst}$	100	300	600	mV	V_{QUC} = 3.3 V	P_13.5.14
Clock signal pull-down current	I_{SCL}	–	150	330	µA	$V_{SCL} = V_{QUC}$	P_13.5.15
Clock input capacitance	C_{SCL}	–	4	15	pF	[49]	P_13.5.16

(table continues...)

[49] Specified by design, not subject to production test

Table 33 (continued) Electrical characteristics SPI signals

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Pin SDI, data input, MOSI							
Data input valid high level TLF35585QVS01	$V_{SDI, hi}$	3.6	–	–	V	V_{SDI} increasing; V_{QUC} = 5.0 V	P_13.5.17
Data input valid low level TLF35585QVS01	$V_{SDI, lo}$	–	–	0.8	V	V_{SDI} decreasing; V_{QUC} = 5.0 V	P_13.5.18
Data input hysteresis TLF35585QVS01	$V_{SDI, hyst}$	200	600	1200	mV	V_{QUC} = 5.0 V	P_13.5.19
Data input valid high level TLF35585QVS02	$V_{SDI, hi}$	2.0	–	–	V	V_{SDI} increasing; V_{QUC} = 3.3 V	P_13.5.20
Data input valid low level TLF35585QVS02	$V_{SDI, lo}$	–	–	0.8	V	V_{SDI} decreasing; V_{QUC} = 3.3 V	P_13.5.21
Data input hysteresis TLF35585QVS02	$V_{SDI, hyst}$	100	300	600	mV	V_{QUC} = 3.3 V	P_13.5.22
Data input signal pull-down current	I_{SDI}	–	150	330	µA	$V_{SDI} = V_{QUC}$	P_13.5.23
Data input capacitance	C_{SDI}	–	4	15	pF	[49]	P_13.5.24
Pin SDO, data output, MISO							
Data output high level TLF35585QVS01	$V_{SDO, hi}$	4.0	–	–	V	V_{QUC} = 5.0 V; I_{SDO} = -9 mA	P_13.5.25
Data output low level TLF35585QVS01	$V_{SDO, lo}$	–	–	0.7	V	V_{QUC} = 5.0 V; I_{SDO} = 7 mA	P_13.5.26
Data output high level TLF35585QVS02	$V_{SDO, hi}$	2.3	–	–	V	V_{QUC} = 3.3 V; I_{SDO} = -7 mA	P_13.5.27
Data output low level TLF35585QVS02	$V_{SDO, lo}$	–	–	0.7	V	V_{QUC} = 3.3 V; I_{SDO} = 5.5 mA	P_13.5.28
Data output rise time	$t_{SDO, rise}$	–	–	25	ns	[49] $C_{SDO,load}$ = 50 pF	P_13.5.29
Data output fall time	$t_{SDO, fall}$	–	–	25	ns	[49] $C_{SDO,load}$ = 50 pF	P_13.5.30
Data output tristate capacitance	$C_{SDO, tri}$	–	4	15	pF	[49]	P_13.5.31
Data output tristate leakage	$I_{SDO, tri, leak}$	-10	–	10	µA	–	P_13.5.32

[49] Specified by design, not subject to production test

13 Interrupt generation

A dedicated interrupt generation block is implemented which is handling requests from independent sources to generate an interrupt. The different requesters are as follows:

- State machine in case:
  - A requested state transition has not been performed successfully, e.g. SLEEP-state could not be entered because of QUC current consumption above the selected threshold level.
  - A requested state transition from SLEEP has been performed successfully, i.e. the system has either successfully entered WAKE-state. The MCU may only send (additional) SPI commands after an interrupt event has been generated by the system. The purpose of the interrupt event is to inform the MCU that a state transition has been performed successfully and that the system is capable of performing SPI communication at full SPI speed.
- Watchdog, an interrupt request is generated if the Watchdog is not serviced properly and configured in a way to allow service errors to occur, i.e. an error counter threshold value of more than 2 is configured. In this case an interrupt is generated only if the error counter threshold is not exceeded due to this error.
- Error pin monitoring, an interrupt request is generated if the error pin monitoring block detects an error and is configured in a way to allow occurrence of this error for a certain amount of time (recovery delay action enabled). In this case an interrupt is requested if an error is detected by the error pin monitoring and the recovery delay has not expired.
- Monitoring Block, an interrupt request is generated based on the defined system reaction described in Chapter 10.4.
- Overtemperature warnings and overtemperature shutdown of communication supply (QCO)
- Overcurrent conditions of voltage reference or standby supply (QST)
- SPI block in case an SPI error has occurred
- ABIST operation has been completed
- Double bit error in the protected configuration

An interrupt is generated to inform a connected MCU that a non-severe system condition has occurred. This allows the MCU to perform proper action based on the source of the interrupt. A single interrupt line exists, which is high on default. All Internal interrupt sources are enabled by default and cannot be disabled.

An interrupt is signaled by pulling the interrupt line low for at least t_{INT} (interrupt min. pulse width) after an internal interrupt condition occurs. The interrupt line is driven high if all of the **IF** register flag(s) has/have been cleared via SPI operation earliest after t_{INT} has expired but latest after t_{INTTO} has expired.

Special cases:

- If an interrupt is signaled by pulling INT low and not all interrupt status flags are cleared by the MCU within t_{INTTO}, the INT stays low until t_{INTTO} has expired, but no additional interrupt event is generated. Information about a pending interrupt event can be derived via the INTMISS status flag. This status flag is cleared each time the interrupt line is driven low.
- If an interrupt is signaled by pulling INT low and an additional bit is set in the **IF** register interrupt flag after the interrupt bits have been read by the MCU and this outdated information is used to clear the interrupt flags, the interrupt line stays low until t_{INTTO} has expired, but no additional interrupt event is generated. Information about a pending interrupt event can be derived via a status flag.
- After releasing the interrupt line to high, the interrupt line stays high for at least t_{INTTO} regardless if any additional internal interrupt condition has occurred or not. If a new interrupt event occurs during the delay time out (t_{INTTO}), this is signaled by generating a new pulse after the delay time out t_{INTTO}.

All interrupt sources can only be cleared by a "write-1-to-clear" (w1c) SPI operation, i.e. writing a logic one to the corresponding bit(s) in the interrupt register clears the event.

Interrupt events are organized in a two level approach. The first level (interrupt flag) provides information about different groups of interrupt events. The second level (status flags) provides detailed information about which

particular event(s) generated the interrupt. To service an interrupt one would only need to write the interrupt flag register (**IF**). The status flag registers are only meant to provide detailed information. However all status flags can be cleared as well.

Recommended interrupt service routine

After an interrupt has been detected by an MCU, the recommended interrupt service routine would need to perform the following tasks via SPI:

1. Read interrupt flag register (**IF**)
2. Read status flag register(s) based on information from first read
3. Take the proper action based on interrupt flag(s) and status flag(s)
4. Write back the status flag register(s) to clear particular status flag(s)
5. Write back the interrupt flag register (**IF**) with the previously read value to clear
6. Recommended: Read interrupt flag register (**IF**) again to check for occurrence of another interrupt event. In case step back to 2).
7. Writing back the interrupt register (**IF**) releases the interrupt line INT if all bits are cleared (interrupt timing requirements is fulfilled).

An interrupt is only generated after the reset signal to the MCU has been released. An interrupt event which occurred while the reset line for the MCU is still active is not signaled at the interrupt line but the particular status bit for this event is set.

Details about the timing of the interrupt line are depicted in the following figure:

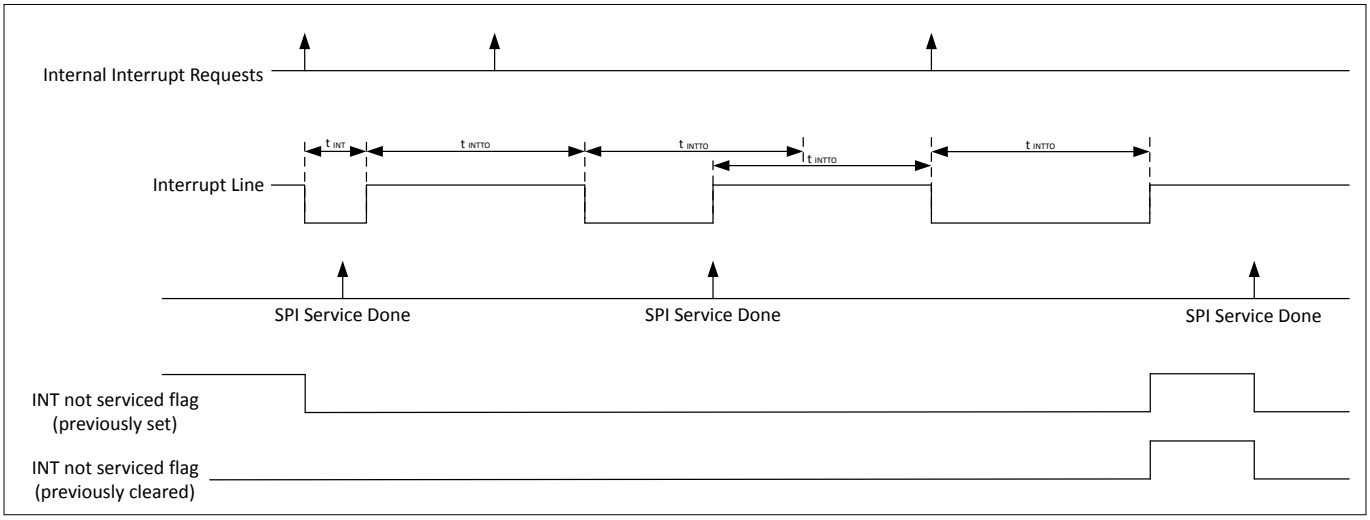


Figure 75 **Interrupt timing**

Table 34 **Electrical characteristics interrupt - timings**

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
Minimum interrupt pulse width	$t_{INT,min}$	90	100	150	µs	–	P_14.1
Interrupt time out	t_{INTTO}	270	300	350	µs	–	P_14.2

Details about the system behavior in case not all interrupt status flags have been cleared are depicted in the following figure:

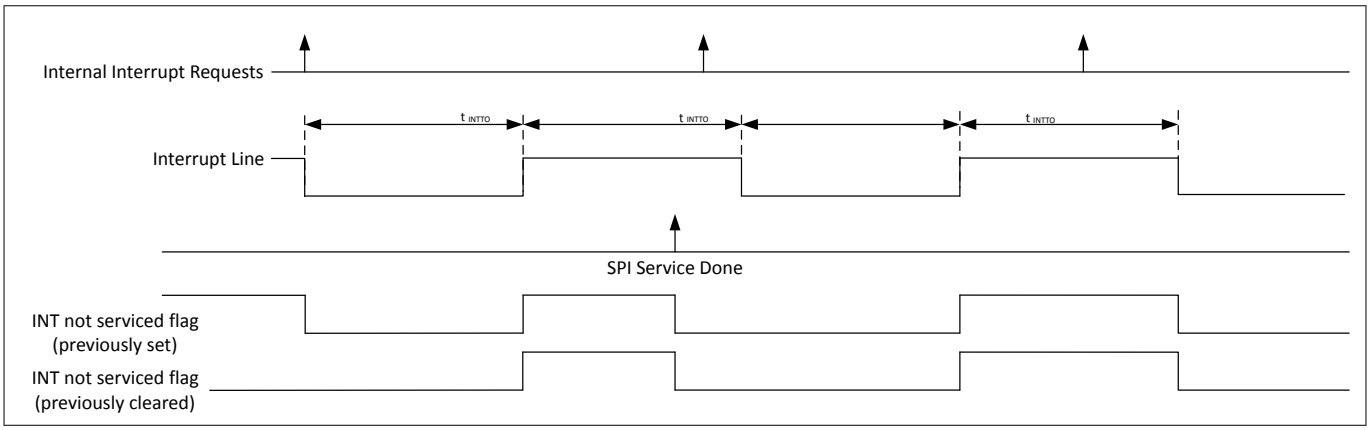


Figure 76 Interrupt timing without service in time

An interrupt is always generated if an internal status flag is set, irrespective of the current state of this status flag. For example, if a parity error on SPI communication is detected for the first time, the flag SPISF.PARE is set and an interrupt is generated. This flag sets the corresponding SPI interrupt flag (IF.SPI) as well. If the flag IF.SPI is not cleared, but a second SPI parity error occurs, a new interrupt is generated regardless. The timings shown in the two figures above are fulfilled for generating a new interrupt.

14 Watchdog supervision

14.1 Introduction window watchdog and functional watchdog

Two independent types of watchdogs are implemented in the TLF35585QV:

- A standalone window watchdog (WWD) with programmable input trigger signal (either pin WDI or trigger via SPI command to **WWDSCMD** register)
- A standalone functional question/answer based watchdog (FWD).

The watchdogs have independent timers and error counters, which allows to run both watchdogs in parallel.

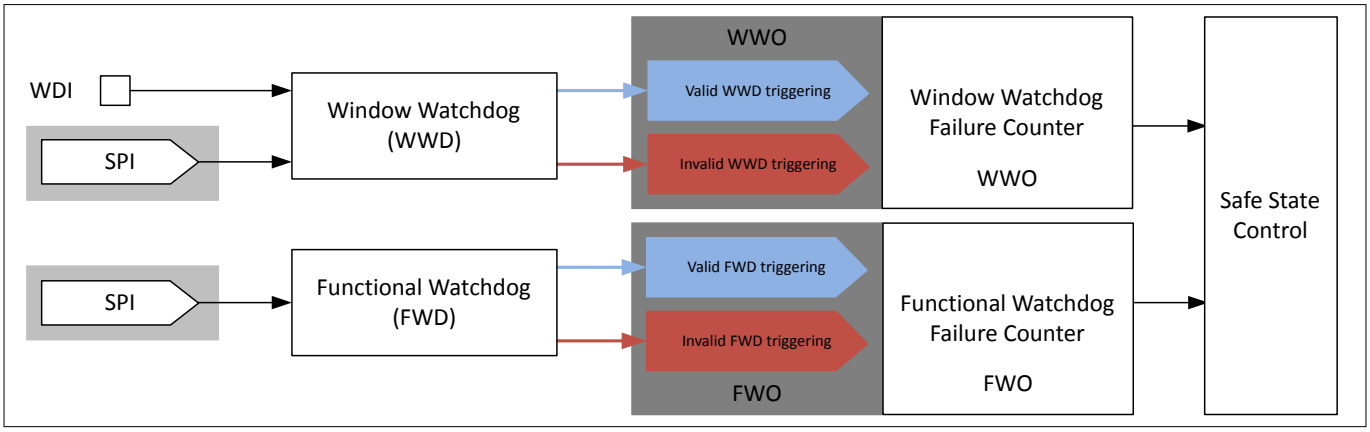


Figure 77 Window watchdog and functional watchdog

Description:

- The functional watchdog is not synchronized to the window watchdog, both are independent.
- The functional watchdog and the window watchdog can be activated and deactivated independently.
- The result of the watchdogs (valid or invalid triggering) are monitored independently by the related watchdog failure counters.
- The status of the window watchdog is WWO, it may have the values "Valid WWD triggering" or "Invalid WWD triggering"
- The status of the functional watchdog is FWO, it may have the values "Valid FWD triggering" or "Invalid FWD triggering
- The influence of the settings of both watchdogs on Safe State Control is described in chapter Safe State Control for better understanding

14.2 Window watchdog

Principle of operation

The window watchdog is integrated in the TLF35585QV to monitor the microcontroller. The microcontroller that is being monitored has to provide periodical triggering within the "Open Windows". A triggering can consist of a falling edge on the WDI pin or writing to the register **WWDSCMD** by an SPI command depending on the configuration. This triggering terminates the "Open Window".The watchdog output indicates a "Valid" or "Invalid" WWD triggering to the WWD failure counter. In case of a "Valid" triggering a "Closed Window" is started.In case there is no triggering during the "Open Window" or a triggering during a "Closed Window", the watchdog output indicates an "Invalid WWD triggering" to the WWD failure counter and a new "Open Window" is started.

In case the microcontroller is not able to trigger the window watchdog with a correct timing, it is assumed that the microcontroller does not work as expected. The microcontroller is informed by the TLF35585QV and a reset in case of multiple failure events.

Configuration

The following parameters of the window watchdog can be configured in INIT, NORMAL and WAKE-state:

- The triggering can be set either to pin triggering (pin WDI) or triggering via SPI command (register **WWDSCMD**). The default configuration is the triggering via SPI.
- The length of open and closed window can be modified according to the application needs by SPI. (combination of cycle time WDCYC, cycle time divider WDCYCDIV and number of cycles for open OW and closed CW window)
- The threshold for the window watchdog failure counter overflow can defined by SPI

Initialization

The window watchdog becomes active in INIT-state as soon as reset output pin ROT turns from low to high. After activation the watchdog opens a so called "Long Open Window" (LOW) of duration of t_{LOW}. During the "Long Open Window" the window watchdog expects a valid triggering, which has to be provided via SPI in case the default configuration is kept, since any signal to watchdog trigger pin WDI is ignored. This is to avoid wrong triggering at pin WDI due to glitches at the microcontroller outputs during start-up and initialization.

The microcontroller can change the configuration of the window watchdog during the "Long Open Window" to change the trigger selection as well as the times for the "Open" and "Closed Window". With a reconfiguration the window watchdog is restarted with the new configuration. A "Open Window" is started accordingly, expecting a valid triggering by the selected triggering input.

If no valid triggering or configuration of the watchdog takes place during the "Long Open Window", the window watchdog recognizes an "invalid WWD triggering". If the INIT timer expires with an invalid WWD triggering present, a so-called "Soft Reset" is issued. After the so-called "Soft-Reset" the window watchdog opens a new "Long Open Window". This is not indicated by interrupt. The repetition of "Long Open Windows" is limited. Should within the second "Long Open Window" the window watchdog not be triggered correctly, a normal or "hard" reset occurs, which means that pin ROT goes to zero and the post regulator output voltages are switched off. After the third "Long Open Window" without valid triggering in a row the state machine moves the device into "FAILSAFE-state (for details please refer to chapter State machine).

Normal operation

A trigger signal within the "Long Open Window" terminates the "Long Open Window" and start the "Closed Window".The "Closed Window" has a fixed duration for operation without invalid triggering.. During normal operation no valid trigger signal is allowed during the "Closed Window". If a valid trigger signal is received within the "Closed Window", the window watchdog recognizes "invalid WWD triggering". The "Closed Window" is terminated with this invalid triggering and an "Open Window" is started.

An "invalid WWD triggering" increments the window watchdog failure counter by two. This is indicated by interrupt.

After the "Closed Window" has ended, the window watchdog starts an "Open Window".

Within the "Open Window" a valid trigger signal is expected. If a valid trigger signal is received within the "Open Window" the watchdog terminates the "Open Window" and starts the "Closed Window". "Valid WWD triggering" decrements the window watchdog failure counter by one in case it is greater than zero, this is not indicated by interrupt.

If no valid triggering should be received during the "Open Window", the window watchdog recognizes "Invalid WWD triggering" and increments the window watchdog failure counter by two and a new "Open Window" is started. This is indicated by interrupt.

In normal operation, the watchdog continues to cycle between the "Open Window" and "Closed Window" as long as valid triggering is received.

Window watchdog output WWO

The window watchdog output WWO is an internal signal: It is connected to the safe window watchdog failure counter. The value of WWO is either "Valid WWD triggering" or "Invalid WWD Triggering".

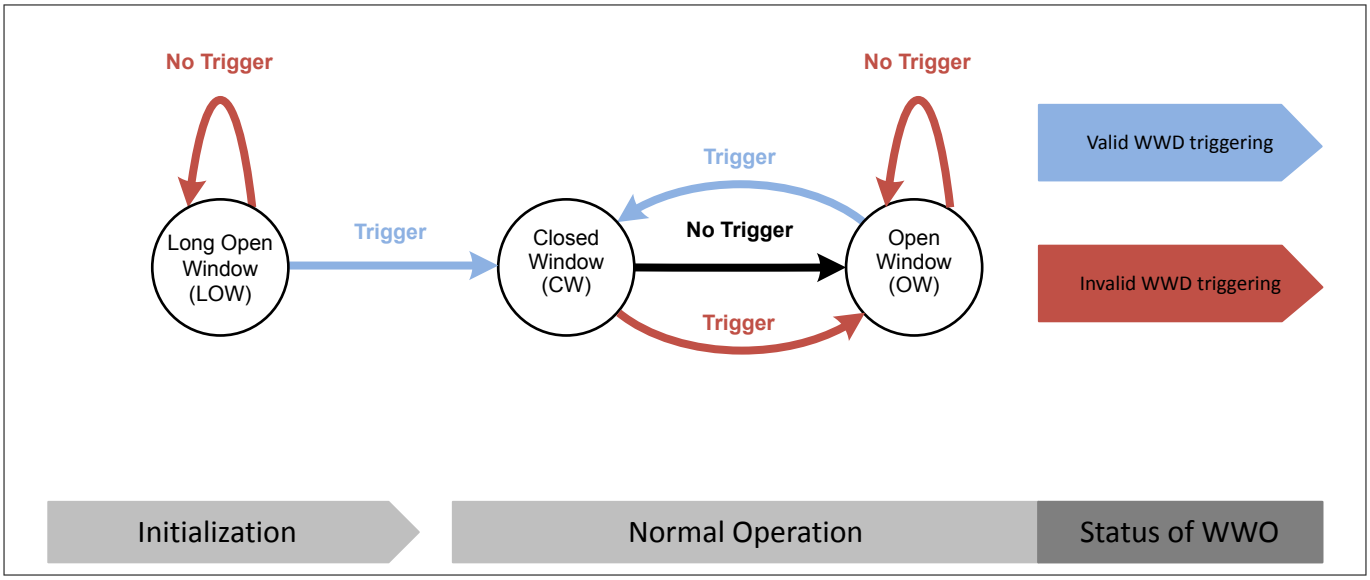


Figure 78 Watchdog state diagram

Description:

- "Trigger" is either a SPI command to **WWDSCMD** register or a valid watchdog trigger at pin WDI
- "No Trigger" in the "Long open Window" is considered as "Invalid WWD triggering", the watchdog opens again a "Long Open Window"
- "Trigger" within the "Long Open Window" is considered as "Valid WWD triggering", the watchdog closes the "Long Open Window" and opens the "Closed Window"
- "Trigger" within the "Closed Window" is considered as "Invalid WWD triggering"
- "No Trigger" within the "Closed Window" moves the watchdog to the "Open Window", after the "Closed Window" has ended.
- "Trigger" within the "Open Window" is considered as "Valid WWD triggering", the watchdog closes the "Open Window" and opens the "Closed Window"
- "No Trigger" in the "Open Window" is considered as "Invalid WWD triggering",.

Window watchdog trigger pin WDI

The watchdog input pin WDI has an integrated pull-down current I_{WDI}. The watchdog input WDI can transition to high within the "Closed Window" or during the following "Open Window".

Valid trigger signal at WDI

Watchdog input WDI is periodically sampled with a period of T_{SAM}. A valid trigger signal is a falling edge from $V_{WDI,high}$ to $V_{WDI,low}$. To improve immunity against noise or glitches on the WDI input, at least two high samples followed by two low samples are required for a valid trigger signal, the valid triggering is considered with the second consecutive sampling point measuring low signal. For example, if the first three samples (two high one low) of the trigger pulse at pin WDI are inside the "Closed Window" and only the fourth sample (the second low sample) is taken in the "Open Window" then the watchdog output WWO indicates "valid WWD triggering".

Invalid triggering at WDI

No trigger signal detected during the "Open Window" or a trigger signal detected during the "Closed Window", is considered invalid triggering. Watchdog output WWO indicates "invalid triggering" immediately after no valid trigger during the "Open Window" or immediately if a trigger signal is detected during the "Closed Window".

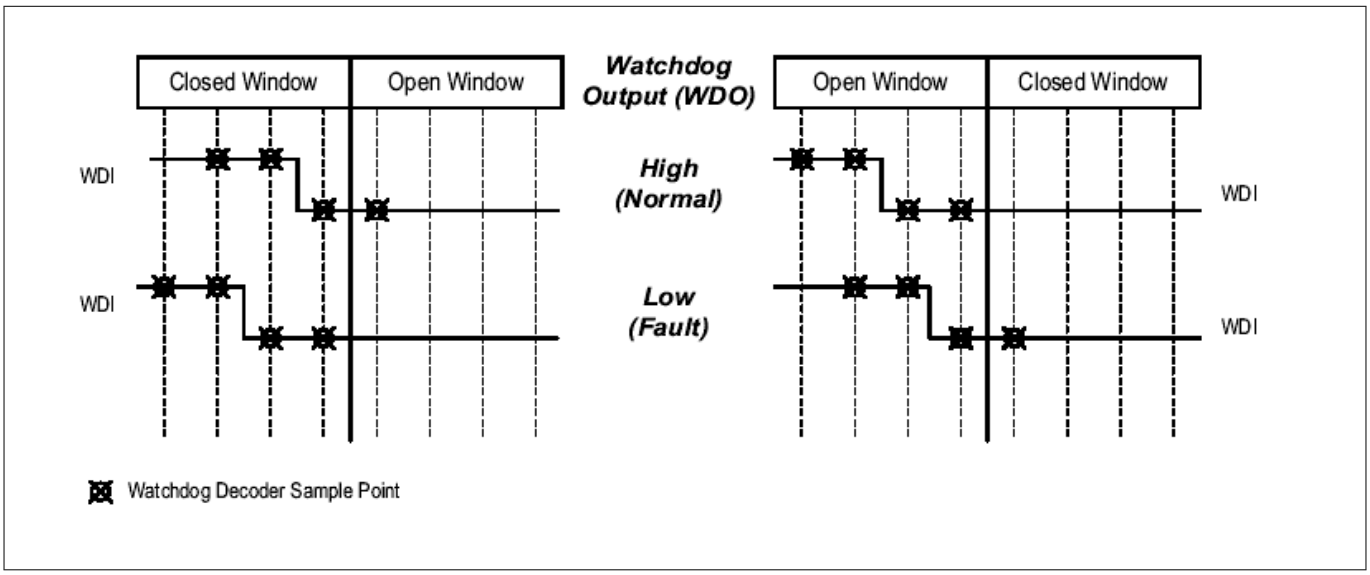


Figure 79 **Valid and invalid trigger pulses at pin WDI**

14.2.1 Timing diagrams window watchdog

14.2.1.1 Normal operation: correct triggering

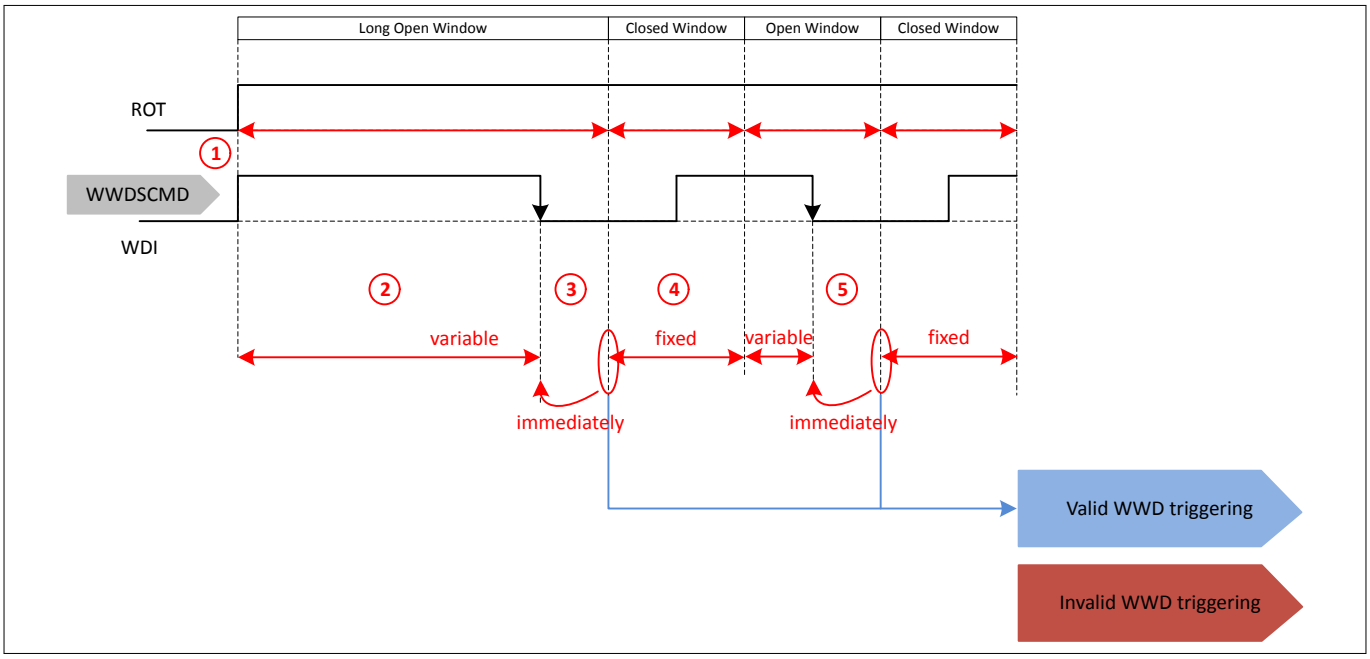


Figure 80 **Normal operation: correct triggering**

1. The "Long Open Window" starts in INIT-state if the reset output of ROT (monitoring the microcontroller related voltages) turned high. In case the window watchdog was deactivated in SLEEP, the first Open Window starts with the transition from SLEEP-state to WAKE-state which is indicated by interrupt. The time of this first Open Window after SLEEP depends on the configured cycle time and cycle time divider, it is 600 ms (WDCYC = 1 and WDCYCDIV = 0) or 60 ms (WDCYC = 0 and WDCYCDIV = 0) or 6 ms (WDCYC = 0 and WDCYCDIV = 1)
2. During the "Long Open Window" valid triggering of the WWD according to the configured trigger selection is expected. The maximum time of the "Long Open Window" is fixed, but it is terminated as soon as a "Valid WWD triggering" is recognized.
3. The window watchdog enters now the "Closed Window". After receiving this first valid trigger the device is allowed to move from INIT to NORMAL-state or from WAKE to NORMAL-state.
4. The "Closed Window" has a fixed duration $t_{WD,CW}$ (can be determined by SPI command). It starts right after the valid trigger signal, that closes the "Open Window" or the "Long Open Window". During the "Closed Window" no trigger signal should be applied. A transition from low to high at the WDI pin is not detected and does not lead to a trigger event,
5. A valid trigger signal terminates the "Open Window" immediately, thus the time of the "Open Window" is variable and depending on the time the microcontrollers schedules the triggering. This is counted as a "Valid WWD triggering"

14.2.1.2 Fault operation: no trigger in open window after initialization

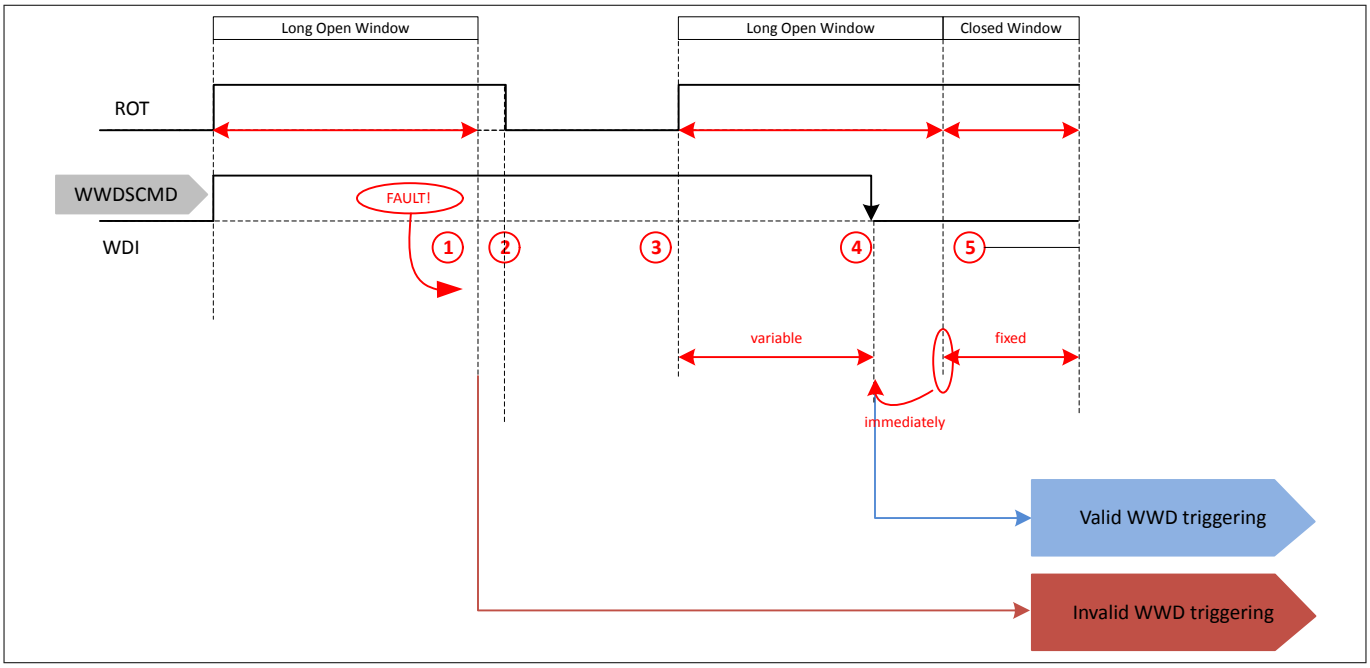


Figure 81 **Fault operation: no trigger in open window after initialization**

1. The initialization timeout and the long open window (LOW) do have the same typical length. Usually this leads to the initialization timeout finishing at the slightly before or at same time as the LOW, which would skip the interrupt event (1). Even though due to the given accuracy, the missing valid triggering within the "Long Open Window" might lead to an interrupt event after the LOW has ended which is increasing the window watchdog failure counter by two.
2. The INIT-state timer expires for the first time. As no valid triggering of the window watchdog was received during INIT-state as expected, a so-called "Soft-Reset" is issued: Pin ROT goes to zero, but the output voltages of the post regulators remain on.

   Additional information: In case the window watchdog should not be triggered correctly within the next "Long Open Window" of the following INIT phase, a "Hard-Reset" is issued, which means pin ROT goes to zero and the output voltages are switched off. After a third invalid triggering during INIT phase the device transitions into FAILSAFE-state.
3. After the so-called "Soft-Reset" pin ROT turns high again after the power-on reset delay time t_{rd} and the watchdog opens a "Long Open Window" to give the microcontroller the chance to trigger and synchronize to the watchdog period.
4. A valid triggering terminates the "Long Open Window", which makes the duration of the "Long Open Window" variable and depending on the triggering. This is counted as a "Valid WWD triggering" and a "Closed Window" is started. The window watchdog failure counter is decremented by one without an interrupt issued.
5. The following "Closed Window" lasts for the time $t_{WD,CW}$. Triggering within this time is considered as an "Invalid WWD triggering".

14.2.1.3 Fault operation: no trigger in open window in steady state

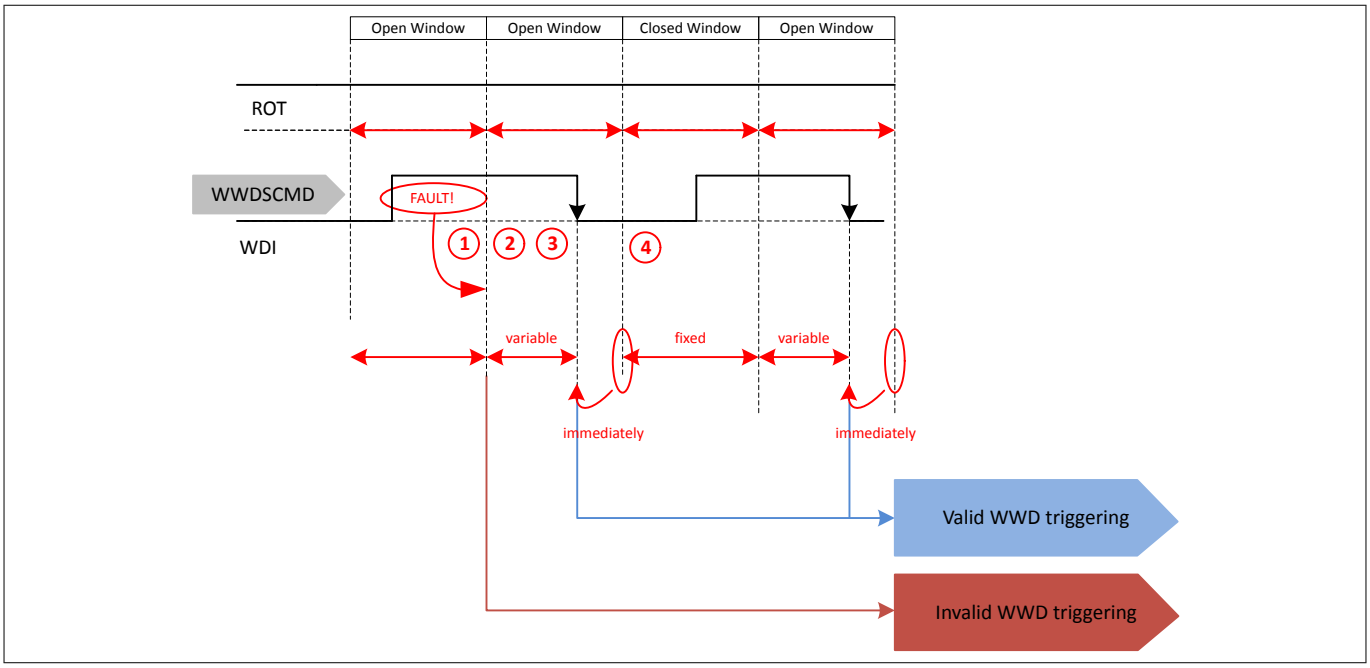


Figure 82 **Fault operation: no trigger in open window in steady state**

1. A missing valid triggering within the "Open Window" leads after the window has ended to an "Invalid WWD triggering". This event is indicated by an interrupt, the window watchdog failure counter increases by two.
2. Having detected an "Invalid WWD triggering" the watchdog starts a new "Open Window" with duration $t_{WD,OW}$ to give the microcontroller the chance to trigger and synchronize to the watchdog period.
3. A valid triggering terminates the "Open Window", which makes the duration of the "Open Window" variable and depending on the triggering. This is counted as a "Valid WWD triggering" and a "Closed Window" is started. The window watchdog failure counter is decremented by one without an interrupt issued.

   Additional informations: In case of multiple "Invalid WWD triggering" within the "Open Windows", the window watchdog failure counter would be incremented again by two until it reaches the configured threshold. In this case a reset is issued.
4. The following "Closed Window" lasts for the time $t_{WD,CW}$. Triggering within this time is considered as an "Invalid WWD triggering".

The behavior of pin ROT is depending on the value of ΣWWO. In the example above it was assumed, that the invalid triggering does not lead to exceed the threshold ΣWWO.

14.2.1.4 Fault operation: false trigger in closed window after initialization

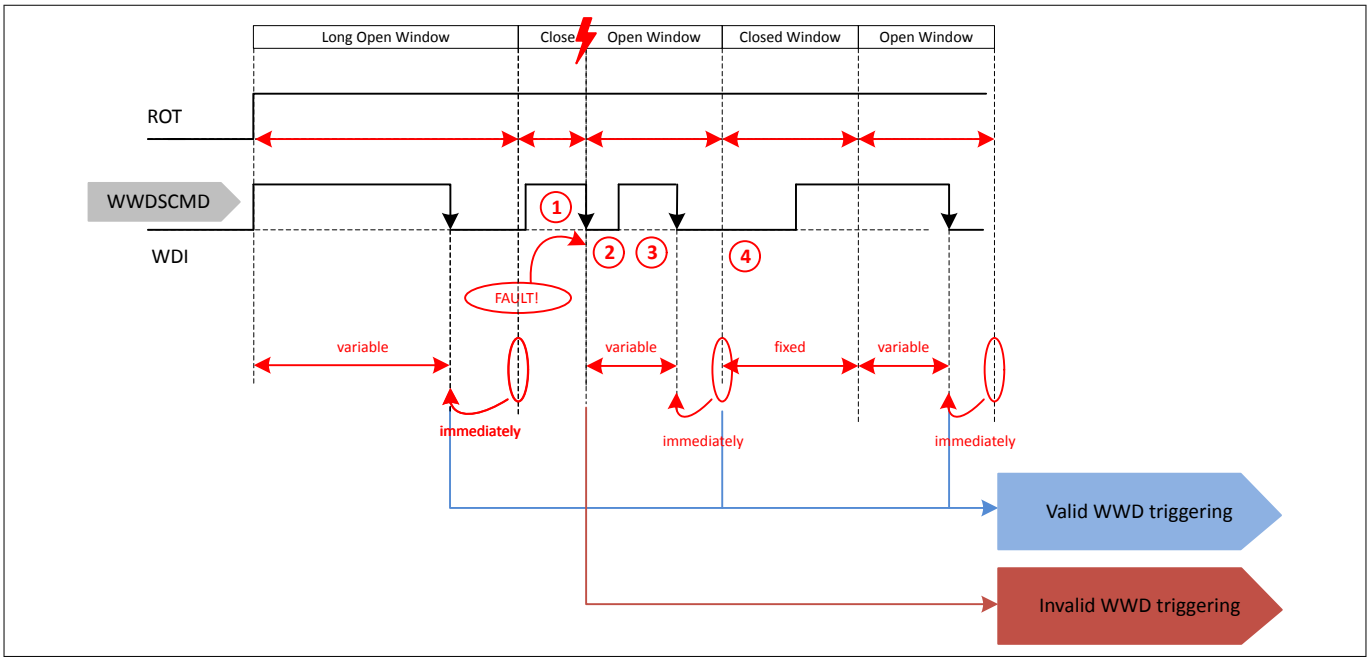


Figure 83 **Fault operation: False trigger in closed window after initialization**

1. A triggering during the "Closed Window" is indicated as "Invalid WWD triggering". This event is indicated by an interrupt and the window watchdog failure counter increases by two.
2. The "Closed Window" is closed with the "Invalid WWD triggering". Originally it would last for the time $t_{WD,CW}$. The false triggering terminates the "Closed Window" and starts an "Open Window" to give the microcontroller the opportunity to synchronize to the window watchdog period.
3. Within this "Open Window" a valid triggering is expected. A valid triggering terminates the "Open Window", which makes the duration of the "Open Window" variable and depending on the triggering. This is counted as a "Valid WWD triggering" and a "Closed Window" is started. The window watchdog failure counter is decremented by one without an interrupt issued.
4. The following "Closed Window" lasts for the time $t_{WD,CW}$. Triggering within this time is considered as an "Invalid WWD triggering".

The behavior of pin ROT is depending on the value of ΣWWO. In the example above it was assumed, that the invalid triggering does not lead to exceed the threshold ΣWWO.

14.2.1.5 Fault operation: false trigger in closed window in steady state

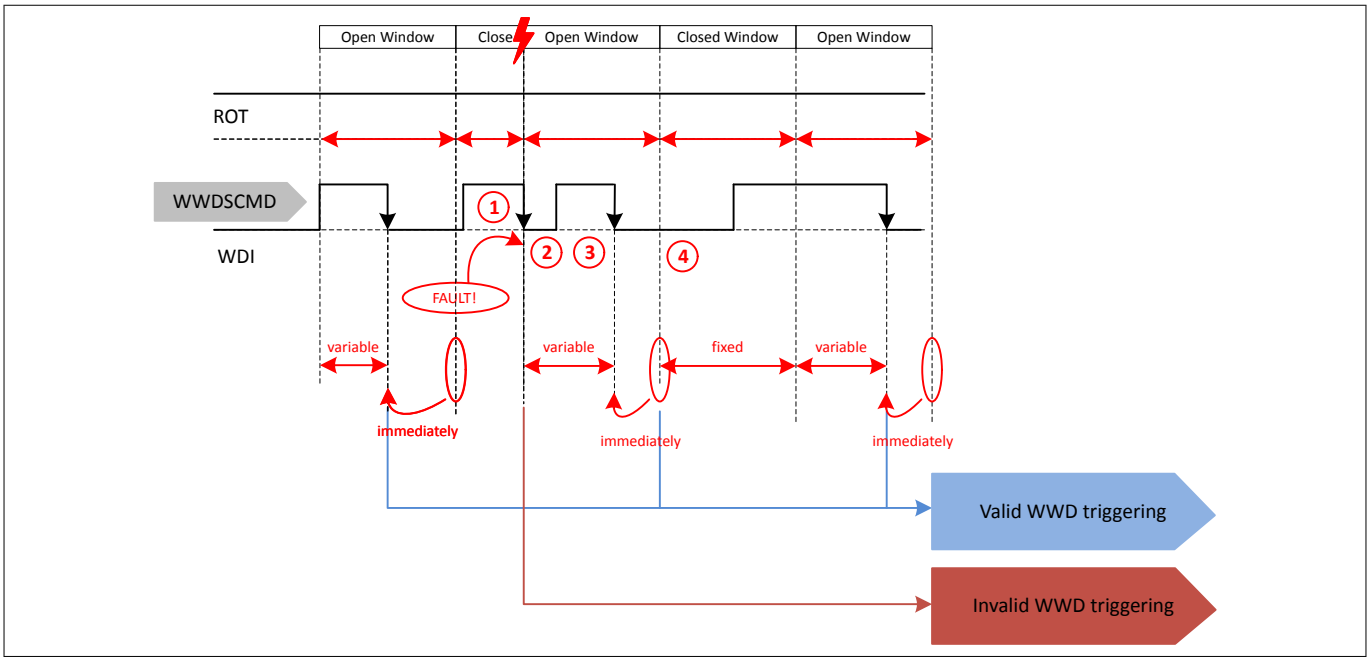


Figure 84 **Fault operation: false trigger in closed window**

1. A triggering during the "Closed Window" is indicated as "Invalid WWD triggering". This event is indicated by an interrupt and the window watchdog failure counter increases by two.
2. The "Closed Window" is closed with the "Invalid WWD triggering". Originally it would last for the time $t_{WD,CW}$. The false triggering terminates the "Closed Window" and starts an "Open Window" to give the microcontroller the opportunity to synchronize to the window watchdog period.
3. Within this "Open Window" a valid triggering is expected. A valid triggering terminates the "Open Window", which makes the duration of the "Open Window" variable and depending on the triggering. This is counted as a "Valid WWD triggering" and a "Closed Window" is started. The window watchdog failure counter is decremented by one without an interrupt issued.
4. The following "Closed Window" lasts for the time $t_{WD,CW}$. Triggering within this time is considered as an "Invalid WWD triggering".

The behavior of pin ROT is depending on the value of ΣWWO. In the example above it was assumed, that the invalid triggering does not lead to exceed the threshold ΣWWO.

14.2.2 Electrical characteristics window watchdog

Table 35 Electrical characteristics window watchdog function

V_{VS} = 6 V to 40 V, T_j = -40°C to 175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	Number
		Min.	Typ.	Max.			
General timing parameters watchdog (WWD and FWD)							
Watchdog cycle time	t_{CYCLE}	94	100	106.5	µs	selectable by SPI command	P_15.2.2.1
Watchdog cycle time, default setting	t_{CYCLE}	940	1000	1065	µs	selectable by SPI command	P_15.2.2.2
Long open window time	t_{LOW}	564	600	639	ms	–	P_15.2.2.3
Watchdog input WDI							
Watchdog sampling time	t_{SAM}	188	200	213	µs	–	P_15.2.2.4
WDI valid high level TLF35585QVS01	$V_{WDI, high}$	3.6	–	–	V	V_{WDI} increasing; V_{QUC} = 5.0 V	P_15.2.2.5
WDI valid low level TLF35585QVS01	$V_{WDI, low}$	–	–	0.8	V	V_{WDI} decreasing; V_{QUC} = 5.0 V	P_15.2.2.6
WDI hysteresis TLF35585QVS01	$V_{WDI, hyst}$	200	600	1200	mV	V_{QUC} = 5.0 V	P_15.2.2.7
WDI valid high level TLF35585QVS02	$V_{WDI, high}$	2.0	–	–	V	V_{WDI} increasing; V_{QUC} = 3.3 V	P_15.2.2.8
WDI valid low level TLF35585QVS02	$V_{WDI, low}$	–	–	0.8	V	V_{WDI} decreasing; V_{QUC} = 3.3 V	P_15.2.2.9
WDI hysteresis TLF35585QVS02	$V_{WDI, hyst}$	100	200	600	mV	V_{QUC} = 3.3 V	P_15.2.2.10
WDI pull-down current	I_{WDI}	–	150	330	µA	$V_{WDI} = V_{QUC}$	P_15.2.2.11
WDI input capacitance	C_{WDI}	–	4	15	pF	[50]	P_15.2.2.12

50 Specified by design, not subject to production test

14.3 Functional watchdog

Principle of operation

A functional or question/answer watchdog is integrated in the to monitor the microcontroller. In a steady state a question is generated (taken out of table), in parallel the so called heartbeat counter starts counting from zero. The heartbeat counter counts up, until the heartbeat period has ended. The duration of the heartbeat period is set to a default value, but can be adjusted via SPI command. The question consists of 4 bits, the expected answer consists of 4 responses of 8 bits each. The four responses shall be sent before the heartbeat period has ended. The last response shall be written to the synchronized response register to reset the heartbeat counter.

Initialization

The functional watchdog is off per default when the device is powered up for the first time. It can be enabled by SPI writing to **WDCFG0**.FWDEN.

Configuration

The functional watchdog can be configured in INIT, NORMAL and WAKE-state. "Configured" means:

- Modify the length of the heartbeat period by SPI command, depending on the needs of the application. (combination of cycle time WDCYC, cycle time divider WDCYCDIV and number of cycles for heartbeat WDHBTP)
- The threshold for the functional watchdog failure counter overflow can defined by SPI

The heartbeat period is based on the cycle time t_{CYCLE} specified in Table 35.

Normal operation

The question is taken out of the Table 36, the correct responses are listed in the same row. The sequence of responses must be kept and can be derived from the response counter **FWDSTAT0**.FWDRSPC before sending the response.

The response to the actual question defined in the table shall be composed by four subsequent response bytes. A correct response to the given question in **FWDSTAT0**.FWDQUEST register shall be done in the following way.

- The first three responses shall be written into **FWDRSP**
- The last response should be written into **FWDRSPSYNC** to reset the heartbeat timer

All four responses must be written before the heartbeat period expires.

If the complete response (32 bits) is correct and if the last response byte was sent with synchronized respond, the heartbeat counter is reset and set to zero. If the complete answer (all four responses - 32 bits) is correct, it is regarded as "Valid FWD triggering", the functional watchdog error counter ΣFWO is decremented by 1. If the last response was sent with synchronized response, the heartbeat counter is reset, but if the answer is wrong, this is regarded as "Invalid FWD triggering" and the functional watchdog error counter ΣFWO is incremented by 2.

An overflow of the functional watchdog error counter ΣFWO triggers a "Move to INIT" event, reset the heartbeat counter and set the functional watchdog error counter ΣFWO to zero.

Table 36 Functional watchdog response definition

QUESTION	RESP3	RESP2	RESP1	RESP0
0	FF	0F	F0	00
1	B0	40	BF	4F
2	E9	19	E6	16
3	A6	56	A9	59
4	75	85	7A	8A
5	3A	CA	35	C5

(table continues...)

Table 36 (continued) Functional watchdog response definition

QUESTION	RESP3	RESP2	RESP1	RESP0
6	63	93	6C	9C
7	2C	DC	23	D3
8	D2	22	DD	2D
9	9D	6D	92	62
A	C4	34	CB	3B
B	8B	7B	84	74
C	58	A8	57	A7
D	17	E7	18	E8
E	4E	BE	41	B1
F	01	F1	0E	FE

Functional watchdog output FWO

The functional watchdog output FWO is an internal signal: It is connected to the FWD failure counter. The value of the functional watchdog FWO output is either "Valid FWD triggering" or "Invalid FWD Triggering".

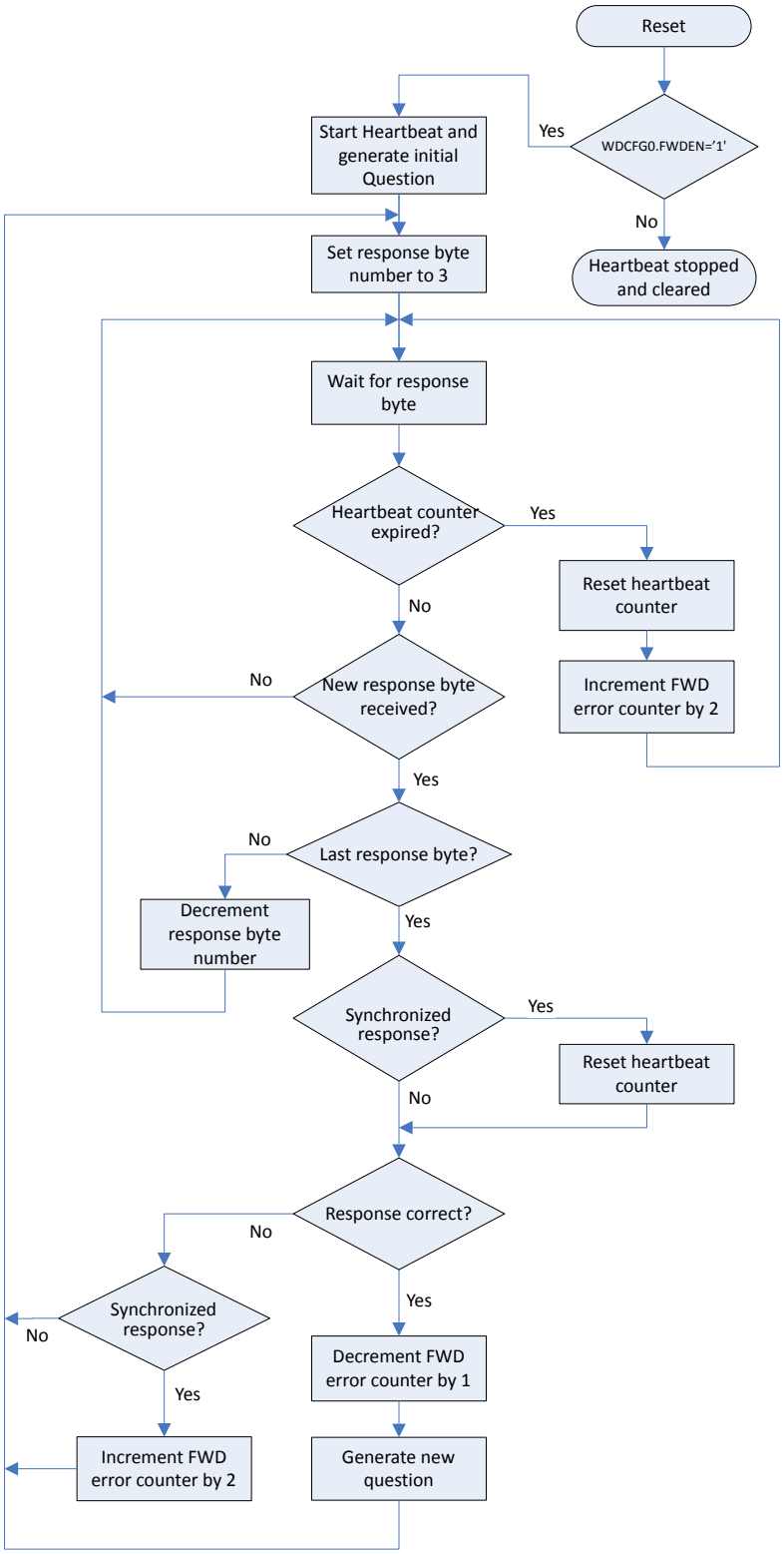


Figure 85 **Functional watchdog flowchart diagram**

14.3.1 Timing diagrams functional watchdog

14.3.1.1 Normal operation: correct triggering

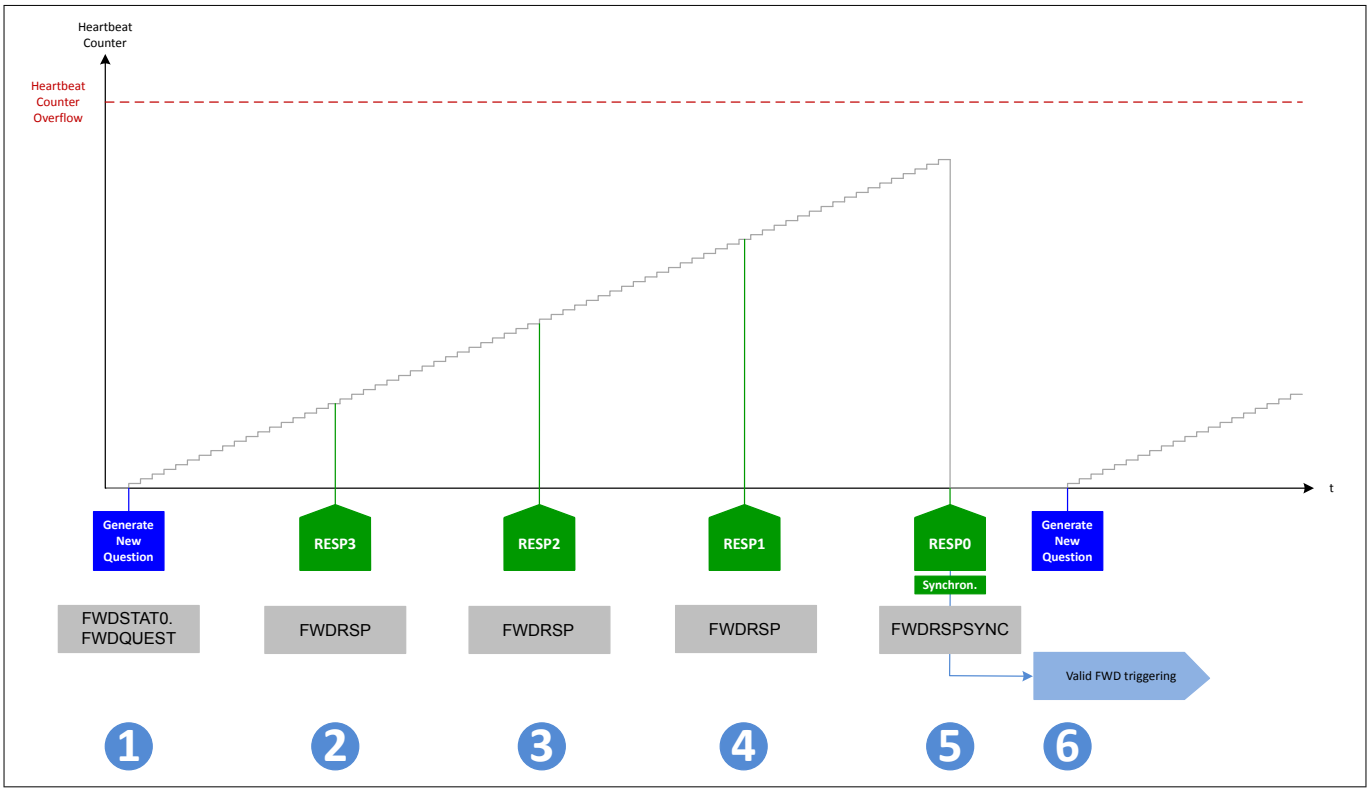


Figure 86 **Normal operation: correct triggering**

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a "Valid FWD triggering" has happened before).
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. A correct response is received (RESP1)
5. A correct synchronized response is received (RESP0). All responses are correct, the sequence of responses is correct and the last synchronized response was received before the heartbeat counter overflowed. The heartbeat counter is reset (set to zero). This is regarded as "Valid FWD triggering", the functional watchdog error counter ΣFWO is decremented by 1 (if the functional watchdog error counter value is higher than zero).
6. A new question is generated, in parallel the heartbeat counter starts counting up

14.3.1.2 Fault operation: missing synchronization

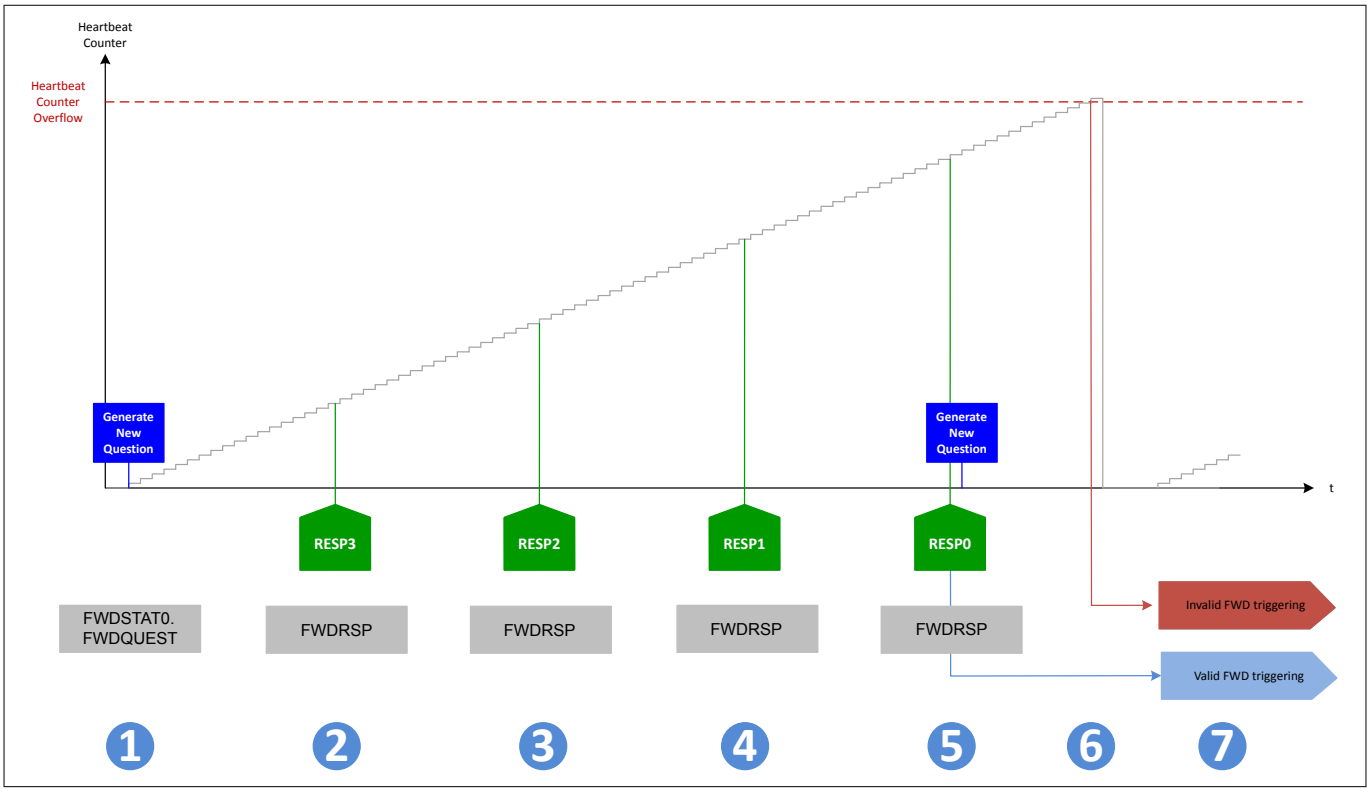


Figure 87 **Fault operation: synchronization is missing**

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a "Valid FWD triggering" has happened before).
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. A correct response is received (RESP1)
5. A correct response is received (RESP0), but not synchronized (written in wrong register). So far, all responses are correct, the sequence of responses is correct and the last not synchronized response was received before the heartbeat counter overflow occurred. The heartbeat counter is not reset and continues to count. This is regarded as "Valid FWD triggering", the functional watchdog error counter ΣFWO is decremented by 1 (if the functional watchdog error counter value is higher than zero). A new question is generated.
6. The heartbeat counter is still counting up, waiting for the answer on the new question. Later in time the heartbeat counter expires and an overflow occurs. This is regarded as "Invalid FWD triggering". The functional watchdog error counter ΣFWO is incremented by 2. The heartbeat counter is reset.
7. The heartbeat counter starts counting up. No new question is generated.

14.3.1.3 Fault operation: wrong answer

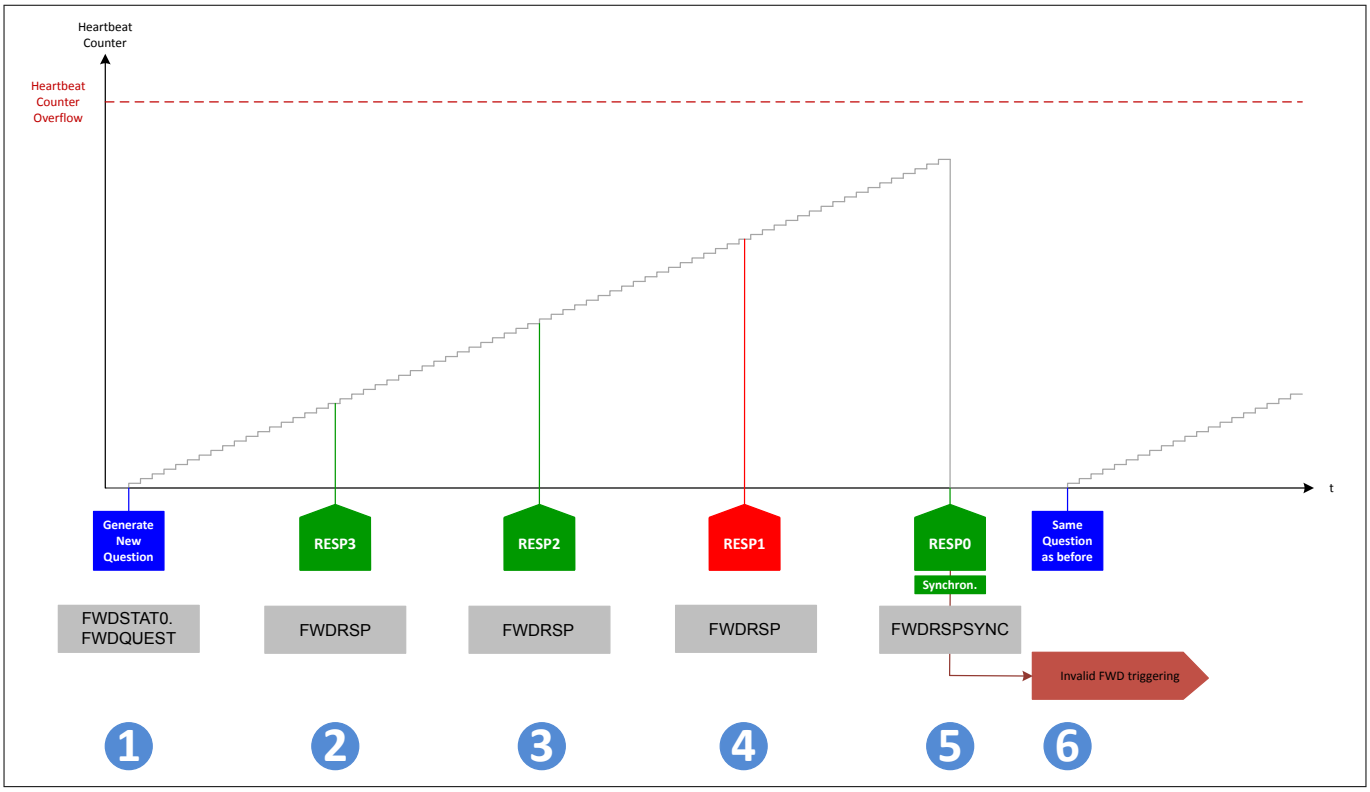


Figure 88 Fault operation: answer is wrong

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a "Valid FWD triggering" has happened before)
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. An incorrect response is received (RESP1)
5. A correct response is received (RESP0). The heartbeat counter is reset (set to zero). The complete answer is not correct. This is regarded as "Invalid FWD triggering". The functional watchdog error counter ΣFWO is incremented by 2. The heartbeat counter is reset.
6. No new question is generated, but the heartbeat counter starts counting up.

Note: If i.e. RESP2 and RESP1 would be mixed, than both responses would be regarded as incorrect - the responses have to be sent in correct order.

14.3.1.4 Fault operation: missing response

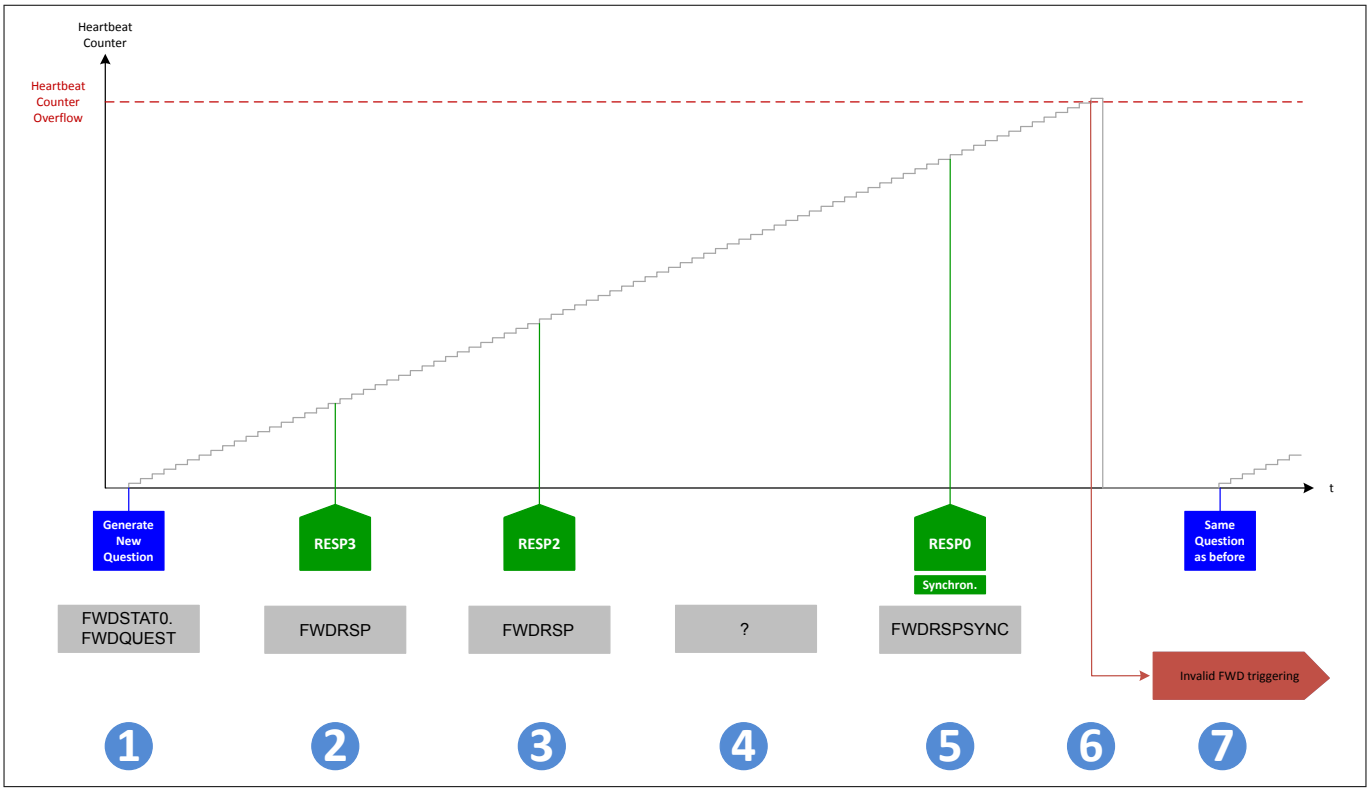


Figure 89 **Fault operation: answer is not complete**

1. A new question is generated, in parallel the heartbeat counter starts counting up (It is assumed, that a "Valid FWD triggering" has happened before).
2. A correct response is received (RESP3)
3. A correct response is received (RESP2)
4. A response is missing (RESP1)
5. A correct response is received (RESP0). So the last response is not the last response but the second last due to the missing response (in this example RESP1). The functional watchdog waits for all four responses to be written, while the heartbeat counter keeps on counting. There is no fixed time for all four responses, but they must be sent in correct order before the heartbeat counter expires.
6. The complete answer is not correct due to missing response RESP1. Although the last response is synchronized, the heartbeat counter is not reset and continue counting up until an overflow occurs. This is regarded as "Invalid FWD triggering". The functional watchdog error counter ΣFWO is incremented by 2. The heartbeat counter is reset.
7. No new question is generated and the heartbeat counter starts counting up.

15 Application information

The following figure describes how the IC is used in its environment.

Note: The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

- Please contact us for additional supportive documentation.
- For further information you may contact http://www.infineon.com/

Note: This figure is a simplified example of an application circuit. The function must be verified in the application.

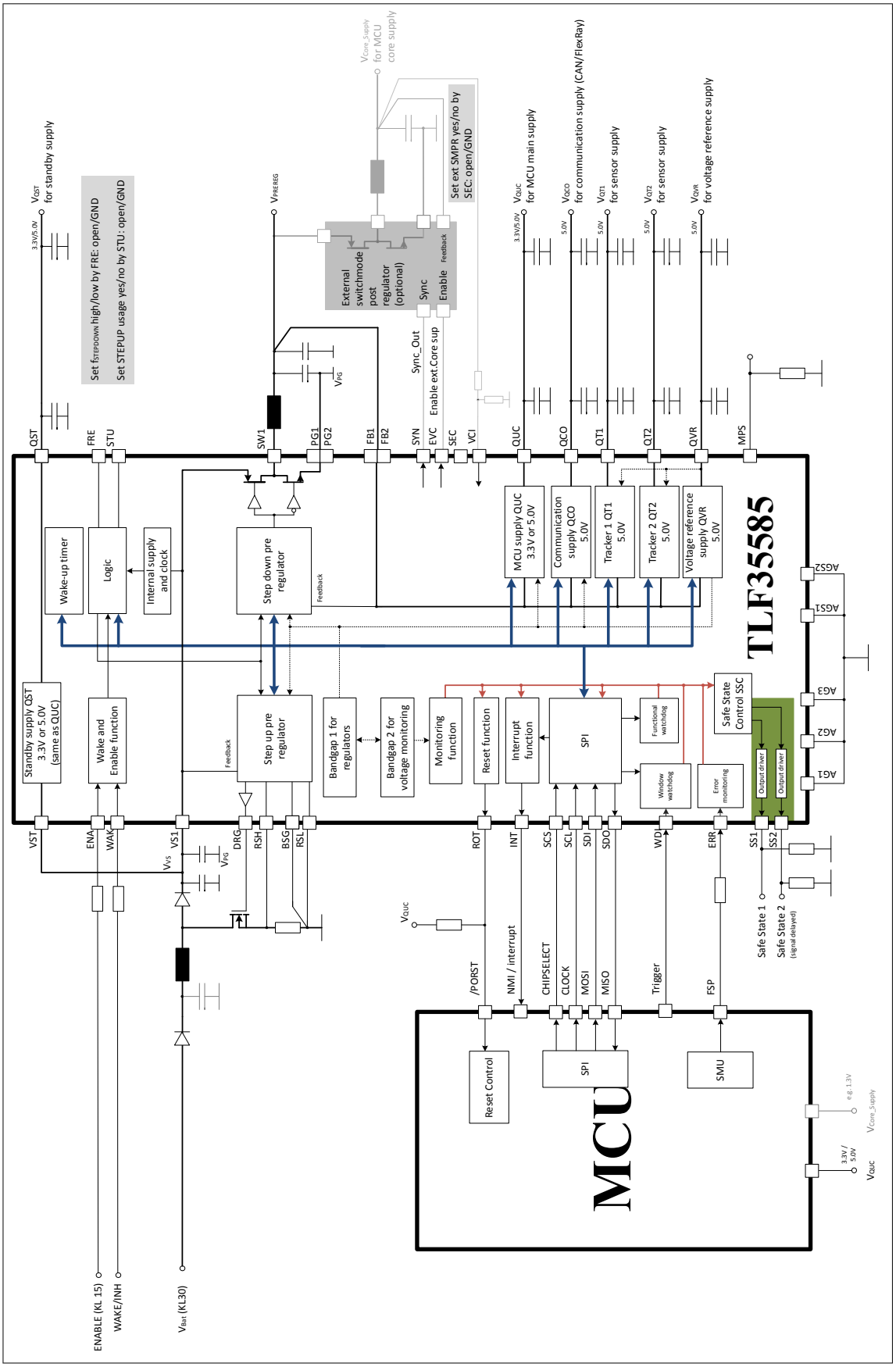


Figure 90 Application diagram

16 Package information

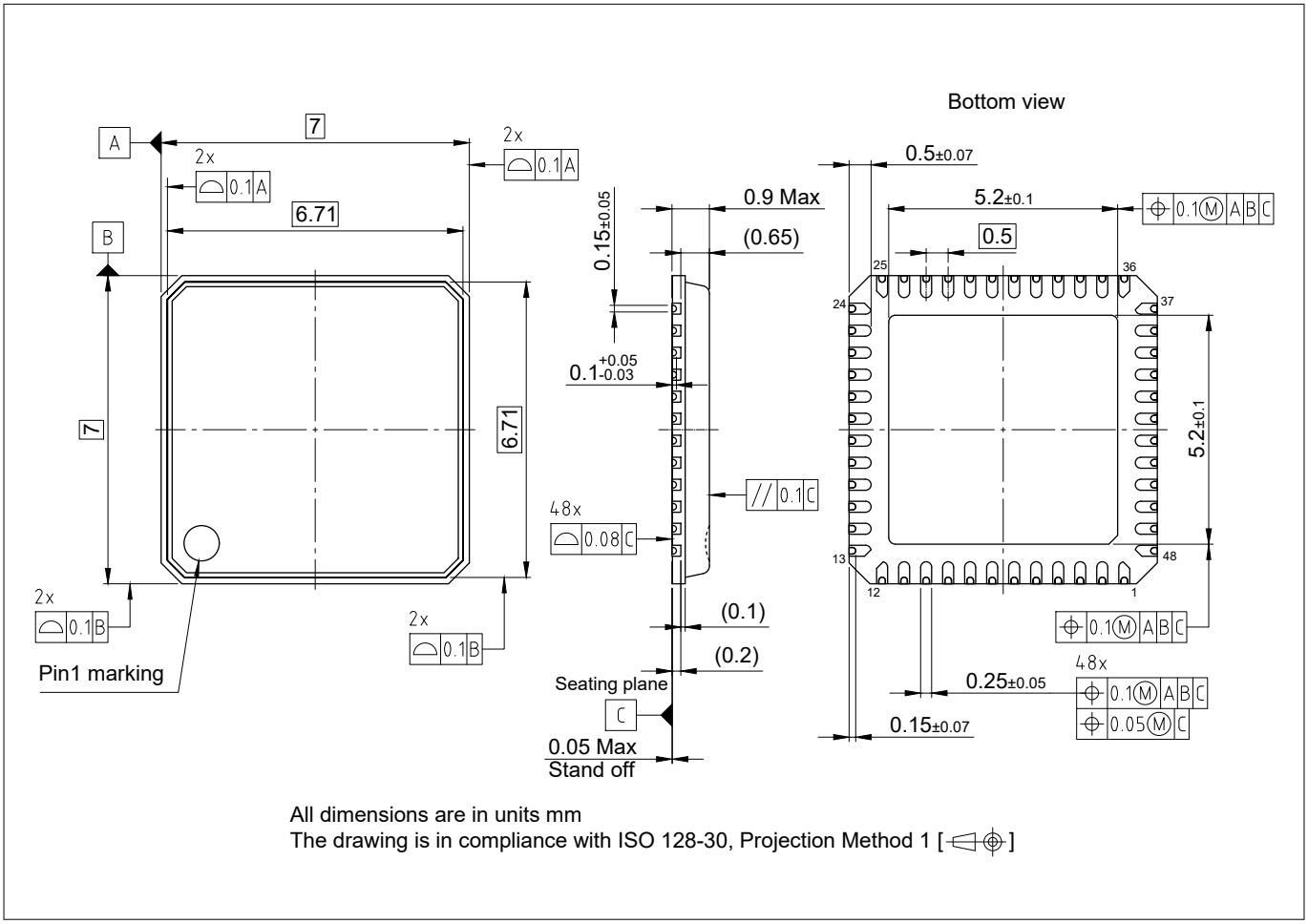


Figure 91 **PG-VQFN-48**

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Information on alternative packages

Please visit www.infineon.com/packages.

Revision history

Revision	Date	Changes
0.2	2021-07-16	• Editorial changes. • Corrected reset value of register SYSPCFG1 and RSYSPCFG1 shown in register overview Chapter 12.4 • Corrected typo (TLF35585QVS02 → TLF35585QVS01) in P_8.5.19. • Removed INTOV Bit in ABIST_SELECT2. • Parameter symbol in condition of $V_{SS1,lo}$ & $V_{SS2,lo}$ corrected to $R_{SS1,pd,ext}$ & $R_{SS2,pd,ext}$ • Register description of bitfield BCK_FRE_SPREAD.FRE_SP_THR updated • Register description of bitfield BCK_FREQ_CHANGE.BCK_FREQ_SEL updated • Junction temperature range for TLF35585QVSxx (PG-VQFN-48) extended to 175 °C • Output maximum ratings of regulators updated. • VST, VS1, SW1, DRG, RSH, ENA and WAK pin max rating specification beyond 40 V updated. • Input voltage VSx overvoltage threshold (P_8.5.50) adjusted • Specification of active pull down at FBx updated (P_6.3.2.23) • Bitfield SYSFAIL.CLKFF and MONSF3.CLOCKBIST removed • Figures regarding wake-signals interpretation and impact by ENA and WAK updated • ENA and WAK pin specification for upper threshold and hysteresis updated • Added configuration bitfield for step down converter driving strength • Removed register BCK_MAIN_CTRL • MPS related bitfields in register MCSMON changed to support enhanced functionality. Description of microcontroller programming support in chapter 10.7 updated accordingly. • Quiescent current specification updated for STANDBY, SLEEP and FAILSAFE state. • Step up pre regulator functional description updated with enhanced feature set description • Conditions of QTx softstart time updated. • Descriptions about $V_{PS,start}$ introduced to chapter 6.7, chapter 10.3.1 and chapter 10.3.8 • Monitoring thresholds of tracking regulators updated • Step up pre regulator external component specification added. • Specification for POWERDOWN shutdown threshold for STANDBY state added. • Bandgap monitoring, bias monitoring and thermal shutdown exceptions added for SLEEP and STANDBY state. • Specification for SPI lead time in SLEEP state added. • Standby regulator (QST) softstart specification condition updated. • Standby regulator (QST) output voltage specification with offset between QST and QUC updated.

Revision	Date	Changes
		• Step down pre regulator specification conditions updated. • Hysteresis specification of digital interface input pins (ERR, WDI, SCS, SCL and SDI) updated. • Absolute maximum rating of pins FBx extended to 8.0V (P_4.1.30 and P_4.1.31). • Absolute maximum rating of pins RSL reduced to 2.5V (P_4.1.6). • Reset class of bitfield RSYSPCFG1.SS2DEL changed to *R2). • Two additional configuration options added to register bitfields SYSPCFG1.SS2DEL and RSYSPCFG1.SS2DEL. Corresponding update of P_12.2.32 to reflect the increased configurable range. • Chapter 14.2.1.1 description of first open window after SLEEP state updated. • Transition time to INIT in case of "Move to INIT"-failure P_11.5.7 increased to a maximum of 200 µs. • Chapter 10.4.3 adjusted in the description for short to ground of FBx detection during start-up phase. • Package related pictures updated.
0.1	2020-05-11	• Initial TLF35585QV Target Data Sheet

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