Bhavishya Gupta

+1(919) 670-9187 | bgupta5@ncsu.edu | https://www.linkedin.com/in/bhavishya-gupta-82084839/

OBJECTIVE

Pursuing full-time opportunities starting May 2026 in hardware design or verification, with interests spanning IP blocks, SoCs, CPU/GPU architectures, and memory subsystems.

EDUCATION

North Carolina State University Aug 2024 – May 2026

Master of Science, Computer Engineering **GPA: 3.95/4.0**

Related Coursework: Fall 2024 (Advanced Functional Verification with UVM, Microprocessor Architecture, ASIC Verification, Architecture of Parallel Computers, FPGA and ASIC Design)

BML Munjal University Aug 2016 – June 2020

Bachelor of Technology, ECE **GPA: 8.59/10**

PROFESSIONAL EXPERIENCE

Intern - Design Verification, Micron Technology, San Jose, California, USA May 2025 – Dec 2025

- **Designed and built an automated Assertion Triaging tool from scratch**, reviewing and analyzing **20+ assertion categories** and assertion implementation logic to cluster failures by root cause and **reduce regression debug volume from ~10–12k to ~3–4k failures.** Co-led **Power Management** (PPM) feature verification, updating directed sequences, refining hardware and firmware-aware SVA assertions, and analyzing coverage; implemented and restructured hardware assertions across multiple RTL modules, actively participating in RCA reviews, and contributed to netlist regression bring-up through cross-functional collaboration with RTL, Firmware, and QA teams

Design Verification Engineer II, Micron Technology, India Nov 2020 - Aug 2024

- **Verified NAND flash features across 176-, 232-, and 276-layer technologies (QLC & TLC)**, debugging complex corner cases and supporting feature development across multiple swim-lanes. **Owned multiple features end-to-end**, including test planning, UVM sequence development, assertion strategy, regression execution, and debug. **Drove assertion-based verification** by designing, reviewing, restructuring, and debugging **2,000+ System Verilog assertions** across Datapath, timing, hardware, firmware, and feature-specific checks to improve robustness and enable early bug detection in RTL and netlist regressions. **Led coverage closure** by analyzing functional and code coverage, identifying hard-to-hit corner cases, developing targeted directed scenarios, and creating/updating **50+ test vectors**, collaborating cross-functionally to improve testbench quality and accelerate verification sign-off.

TECHNICAL SKILLS

Programming Languages/Methodology: Verilog, System Verilog, SVA, UVM, UVMF, Python, C, C++, Shell

Protocols: Memory Protocols like 3D Nand Flash (RG Technology), DDR, Cache Coherence Protocols, I2C, SPI, Wishbone, APB, AHB

Tools/Software: Cadence Virtuoso, Synopsys VCS, Questa Sim, Cadence Xcelium, Git, Bitbucket, Make, Jira, Confluence, JasperGold

Hardware & Verification Skills: Formal verification, UVM/SV testbench development, Constrained Random Verification, Assertion-based verification, CDC, STA, cache & memory hierarchy, CPU/GPU Architecture, Low Power Verification (UPF), Test Planning, Memory Controller Verification

PROJECT EXPERIENCE

I²C Multi-Bus Controller Verification (System Verilog, Questa Sim, XML) : Link

- **SV-based verification** of a Wishbone–to–I²C controller using directed and constrained-random stimulus, **SVA for protocol/FSM/register checking**, and functional coverage (**~99.5% test-plan coverage**).

LC-3 Microcontroller Verification (UVMF, System Verilog): Link

- **UVMF-based verification** of a 5-stage LC-3 pipeline with stage-level environments, **end-to-end predictor/scoreboard**, constrained-random instruction streams, and functional/branch coverage.

Hardware Implementation of Scaled Dot-Product Self-Attention for Transformer Networks — Design & Synthesis (Verilog):

- **RTL design and synthesis** of scaled dot-product attention with SRAM-mapped interfaces, valid/ready handshaking, DesignWare FP integration, and timing/area optimization.

YAPP Packet Router Verification (System Verilog, UVM): Link

- **UVM-based verification** of a YAPP packet router using **multiple protocol UVCs** (TX/RX agents, HBUS, output-channel), **UVM RAL for register access**, constrained-random generation of legal/illegal packets, and a **TLM-based scoreboard** to verify routing correctness, parity/length error handling, and functional coverage.

Out-of-Order Superscalar Processor with Dynamic Instruction Scheduling (C++): Link

- Designed a 9-stage simulator implementing dynamic scheduling with a Reorder Buffer (ROB), Rename Map Table (RMT), and Issue Queue (IQ). Successfully validated against all 8 test cases and analyzed IPC trends to determine optimal IQ and ROB configurations using multiple benchmarks

ACHIEVEMENTS

Micron Technology, India Jan 2021- Aug 2023

- Recognized twice as a Culture Champion for outstanding performance and timely, flawless project execution at the All Hands Meet. Successfully debugged multiple design issues, including critical ones, and developed test-benches to enhance individual assertion modules, improving overall assertion coverage.