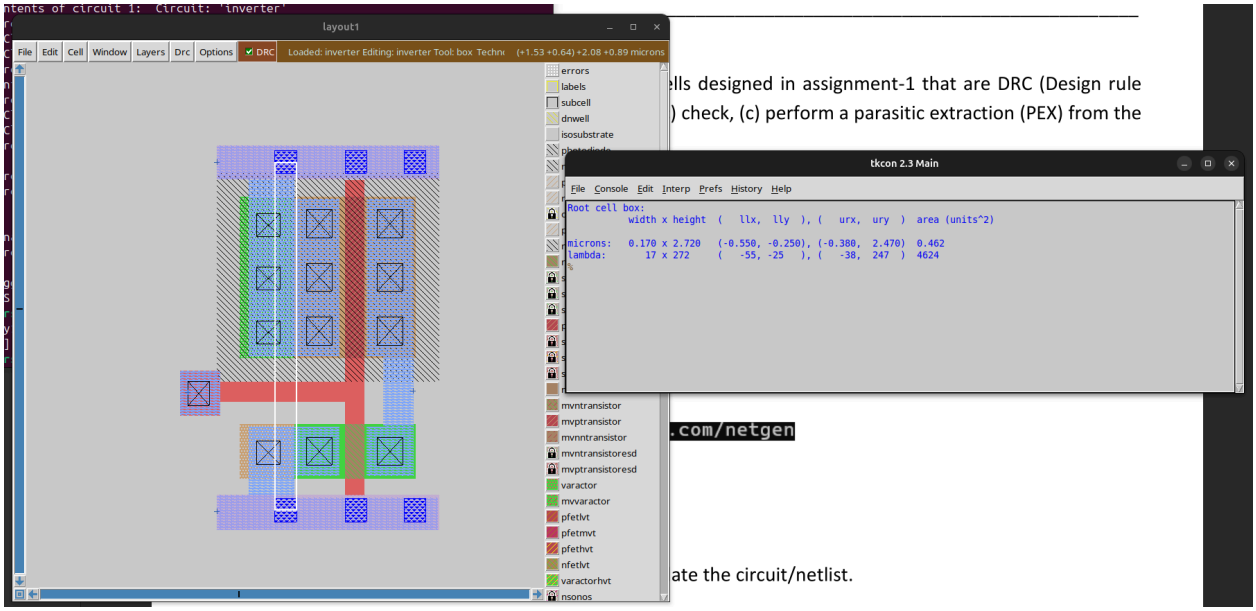
EE671 : VLSI Design
Assignment 2 Report Submission
Harshil Singla (22b1260)

Q1. Inverter of Strength 1

1. Screenshot of layout with the height of the layout annotated
2. DRC clean screenshot

The following screenshot shows the box height (exactly 2.72um from the midpoint of metal contacts) as well as the green check on DRC.



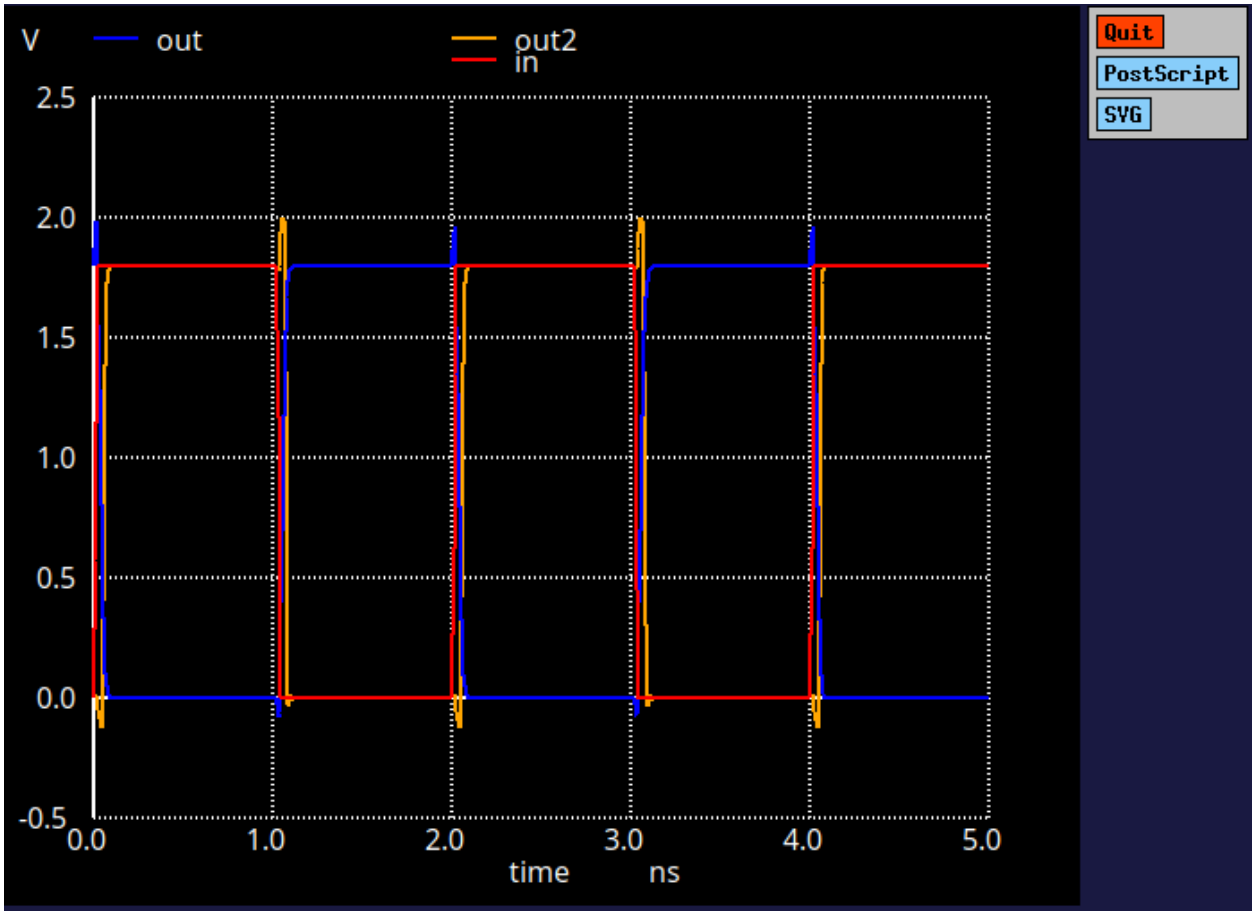
3. LVS clean screenshot

```
Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.
Circuit 1 contains 4 nets,    Circuit 2 contains 4 nets.


Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.
```

4. Table with Inverter characteristics:

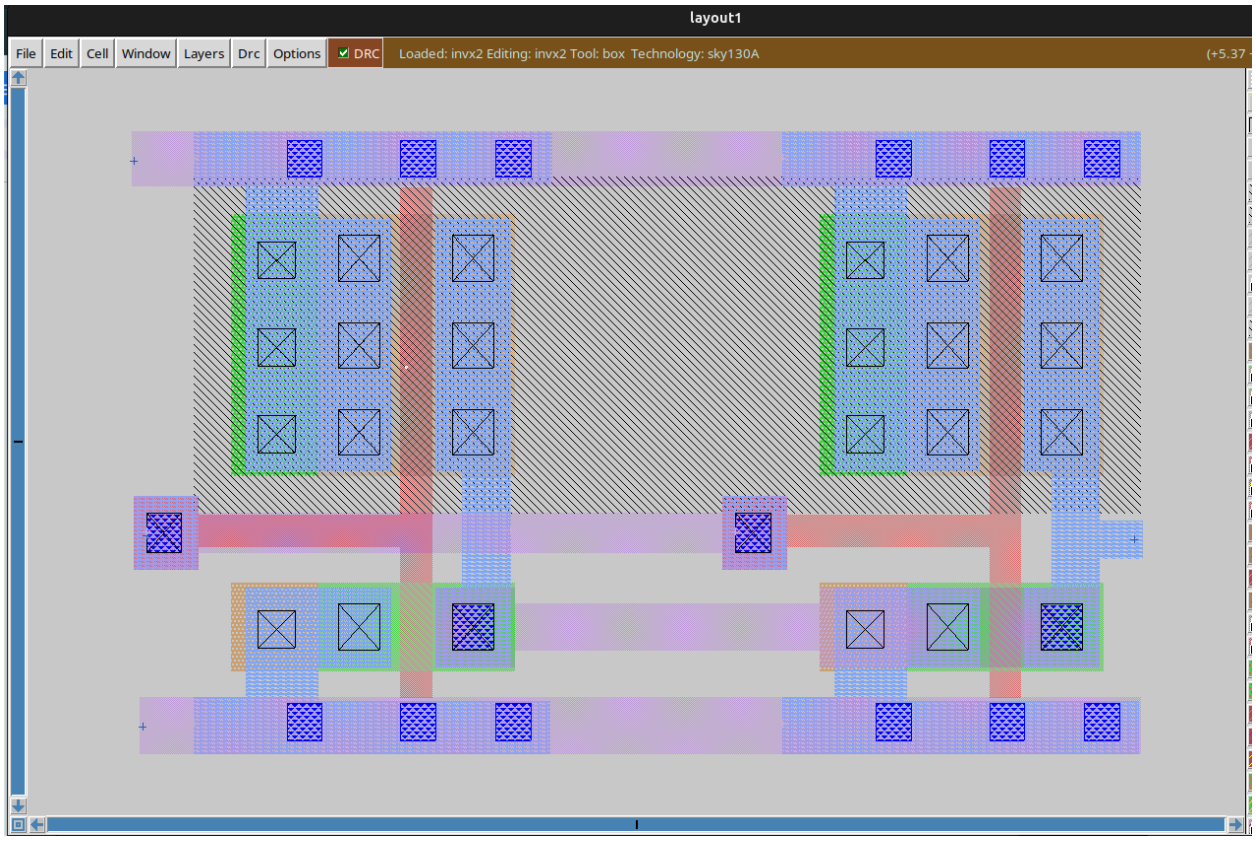
Inverter Dynamic Characteristics	Value
Rise Time (ps)	20.83
Fall Time (ps)	19.87
Propagation Delay (ps)	14.37



Q2. Inverter of Strength 2

1. Screenshot of layout with the height of the layout annotated
2. DRC clean screenshot

The following screenshot shows the combined layout as well as the green check on DRC. Since the cells are placed side to side, the strength 2 inverter also has a height of 2.72um.



3. LVS clean screenshot

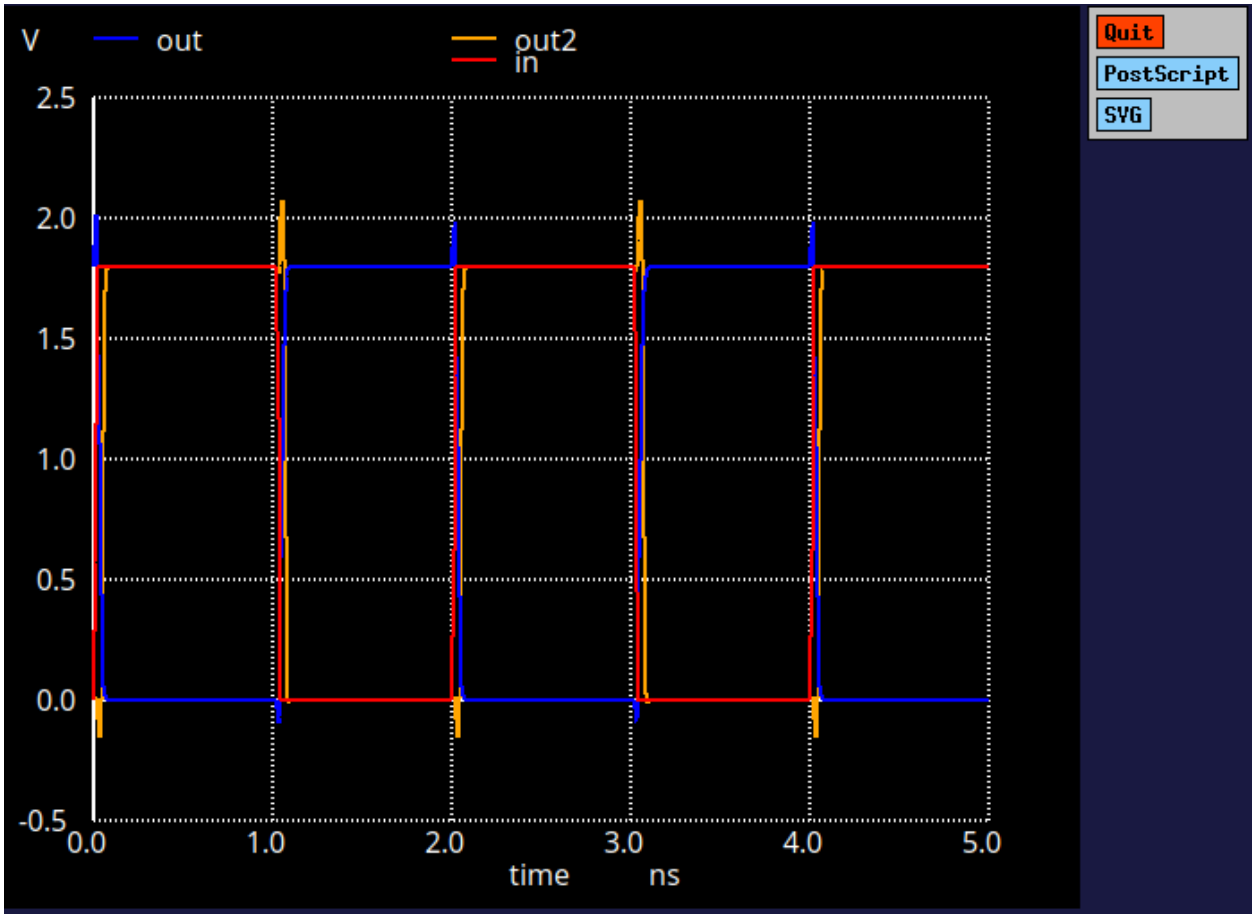
```
Contents of circuit 1:  Circuit: 'invx2'
Circuit invx2 contains 2 device instances.
  Class: inverter             instances:   2
Circuit contains 4 nets.
Contents of circuit 2:  Circuit: 'inv2'
Circuit inv2 contains 2 device instances.
  Class: inverter             instances:   2
Circuit contains 4 nets.

Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.
Circuit 1 contains 4 nets,    Circuit 2 contains 4 nets.


Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.
```

4. Table with Inverter characteristics:

Inverter Dynamic Characteristics	Value
Rise Time (ps)	13.44
Fall Time (ps)	14.15
Propagation Delay (ps)	10.59


V
out
out2
in
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
0.0
1.0
2.0
3.0
4.0
5.0
time
ns
Quit
PostScript
SVG