Saturday Aug 10, 2024	EE 671: VLSI DESIGN 2024/2025 ASSIGNMENT-1	Due On Aug 18, 2024

Note:

1. Submission is **only** through Moodle in the form of a PDF file upload.
2. All plots must be legible/readable in the submission (axes values and units)
3. Kindly install the necessary Tools and the PDK, procedure for which is mentioned in a separate file named "Sky130-Ngspice-Magic_Installation.pdf".
4. For all your simulations, use V_{DD} = 1.8 V.

Introduction:

In this assignment you will design and simulate CMOS inverters using SkyWater 130A PDK.

You will use NGSpice (a spice circuit simulator) tool to simulate the circuit. NGSpice takes a spice netlist file as an input. A sample netlist is given in the Installation guide provided.

You need to create the netlist for the schematic shown in Fig. 1 including the MOSFETs and their dimensions (Width, *W* and Length, *L*). In addition to this, we want to include the MOSFET drain and source capacitance using spice area parameters "as", "ad" and perimeter parameter "pd". These will depend on the transistor geometry. Referring to the Fig. 2, the Width of the diffusion region is *W* while its length is 4λ. Since $\lambda = L_{min}/2$, $4\lambda = 2L_{min}$.

a. The source/drain area parameters are: as = ad = $W \times 2\ L_{min}$
b. The source/drain perimeters are: ps = pd = $2 \times (W + 2L_{min})$.

Notice that the values of area and perimeter of source and drain regions will have to be recalculated when you change the widths.

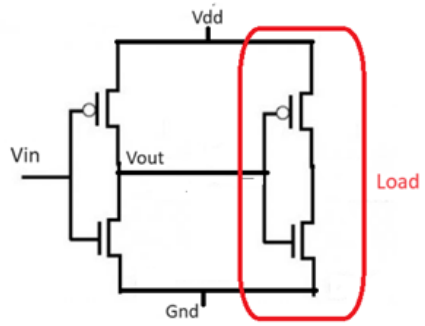

Figure 1: Inverter loaded with another inverter

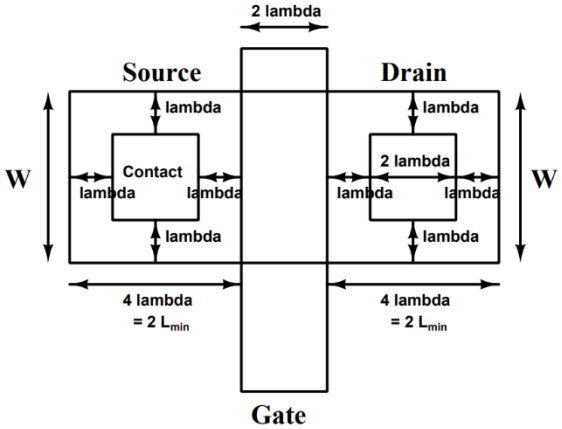

Figure 2: Illustration of diffusion area and perimeter

Q1) Design a minimum size CMOS inverter (minimum possible equal rise and fall time) with fixed NMOS and PMOS channel length of 0.15μm (this is the minimum channel length). The minimum channel width for NMOS is fixed to 0.4μm (restriction from the PDK) and the width of PMOS is to be obtained by design. The input should be a rail-to-rail square wave with rise/fall times of 20 ps, and the inverter will be loaded by another minimum size inverter (as shown in Fig. 1).
Simulate and report the following in the tabular fashion shown below:

Inverter Design Parameter	**Value**
PMOS Width (μm)	
PMOS Length (μm)	0.15
NMOS Width (μm)	0.4
NMOS Length (μm)	0.15

Inverter Dynamic Characteristic	**Value**
Rise time, t_r (ps)	
Fall time, t_f (ps)	
Propagation delay, t_p (ps)	

Once designed, **plot** (in the submission) the static transfer characteristics of this inverter by using a DC sweep on the input from 0 to VDD and report the following in the tabular fashion below:

Inverter Static Characteristic	**Value**
V_{IH} (V)	
V_{IL} (V)	
NM_H (V)	
NM_L (V)	
Switching Voltage, V_M (V)	

Q2) Let's call the inverter in Q1 as **INVX1** (strength-1 inverter). Design a strength-2 inverter (**INVX2**) and report all the tabular parameters above when the **INVX2** is loaded with **INVX1**. Comment on the results obtained.