Saturday	EE 671: VLSI DESIGN 2024/2025	Due On
Aug 29, 2024	COURSE PROJECT-I	Sep 15, 2024

Note:

1. Submission is **only** through Moodle in the form of **a PDF file** upload and **a zipped folder**.
2. All plots must be legible/readable in the submission (axes values and units)
3. For all your simulations, use V_{DD} = 1.8 V.
4. Refer to the lecture notes for definitions on all .lib parameters.

Project Definition:

In this course project, you will characterize and build a few cells in the standard cell library (all strength-1 cells). These is in continuation of what you have done in your two assignments. Each team is assigned three cells. Please check the cells assigned to your group **here**.

As discussed during the lectures, each standard cell in a library has different views: namely, (a) Verilog/VHDL (b) Spice Netlist (c) Layout view (magic files in this case) (d) Liberty files (.lib) and Library Exchange format (.lef file). Your project is to design and produce each of these views for all the cells assigned to your team. The sequence of steps to be followed for each cell are as follows:

(a) **Design** the required circuit in NGSpice to get the same rise/fall as inverter 1x.

(b) **Draw the layout** of the circuit on Magic and ensure zero DRC error and LVS pass. Extract the netlist from the layout (PEX netlist).

(c) **Export the LEF** file from Magic using `% lef write` command on the Magic Terminal. Open the file with a text editor and visually inspect if all layers and coordinates are right (the required cell layout must be open in Magic before you type the command).

(d) **Timing & Power Characterization:** from the PEX netlist, you will perform timing & power simulations.

(e) **Input cap Characterization:** from the PEX netlist, you will perform simulations to find rise_cap and fall_cap and average_cap for all input pins.

(f) **HDL Functional definition:** write a simple Verilog/VHDL file for the cell and compile it with iverilog tool to ensure no compilation errors. To install iverilog, type `sudo apt install iverilog` on your wsl terminal. To check the Verilog file, type `iverilog my_verilog.v` on your wsl terminal.

Project Deliverables:

The Final Submission (one per group) will be (a) Zipped Folder and (b) A final report.

The Folder must maintain the following directory structure:

Team_Number-|

| Spice_Netlist |
| |<Cell-1>.sp
| |<Cell-2>.sp
| |<Cell-3>.sp
| LEF |
| |<Cell-1>.lef
| |<Cell-2>.lef
| |<Cell-3>.lef
| Verilog |
| |<Cell-1>.v or .vhd
| |<Cell-2>.v or .vhd
| |<Cell-3>.v or .vhd
| Layout |
| |<Cell-1>.mag
| |<Cell-2>.mag
| |<Cell-3>.mag
| LIB |
| |<Cell-1>.doc
| |<Cell-2>.doc
| |<Cell-3>.doc

The final report must have the following (Cell-1, Cell-2 followed by Cell-3):

1. Circuit Diagram of the Cell with a table of MOSFET width and length
2. Screenshot of the cell layout (with area mentioned as WIDTH X HEIGHT)
3. Screenshot of the PEX netlist
4. DRC and LVS clean screenshots
5. Waveforms from one simulation (input, outputs and clocks clearly shown) – i.e., one waveform each for propagation delay, rise or fall transition time, set-up time, hold-time
6. A completely filled Timing and Power tables (similar to the .doc files in the LIB folder).
7. Table of contribution of each member of the team.

Note:

1) A combinational and sequential LIB format is provided in the form of .doc files. Edit this file based on your cell.

2) Replace <Cell-1,2,3> with the actual Cell Names.