ADD

$PC \rightarrow mem_i, \rightarrow ir, inc$

↓

$inc \rightarrow PC$

$ir^{(6-9)} \rightarrow rf(a_1)$

$ir^{(3-5)} \rightarrow rf(a_2)$

$rf(d_1) \rightarrow a \rightarrow alu$

$rf(d_2) \rightarrow b \rightarrow alu$

$alu \rightarrow t_1$

↓

$t_1 \rightarrow a \rightarrow rf(d_3)$

$ir^{(6-9)} \rightarrow rf(a_3)$

State names

S_1

S_2

S_3

State names

S_6 ($alu\ op = ADD$)

S_{17} ($C \rightarrow mux^{(sel)}$)

ADC

S_1

↓

$inc \rightarrow PC$

$ir^{(6-9)} \rightarrow rf(a_1)$

$ir^{(3-5)} \rightarrow rf(a_2)$

$rf(d_1) \rightarrow a \rightarrow alu$

$rf(d_2) \rightarrow b \rightarrow alu$

$alu \rightarrow t_1$

↓

$t_1 \rightarrow a \rightarrow mux^{(1)}$

$ir^{(6-9)} \rightarrow rf(a_2)$

$rf(d_2) \rightarrow b \rightarrow mux^{(0)}$

$ir^{(6-9)} \rightarrow rf(a_3)$

$mux^{(o/p)} \rightarrow rf(d_3)$

ADZ

S_1

↓

S_6

↓

$t_1 \rightarrow a \rightarrow mux^{(1)}$

$ir^{(5-3)} \rightarrow rf(a_2)$

$rf(d_2) \rightarrow b \rightarrow mux^{(0)}$

$ir^{(5-3)} \rightarrow rf(a_3)$

$mux^{(0/P)} \rightarrow rf(d_3)$

State names

S_{18}

$(Z \rightarrow mux^{(sel)})$

State names

S_7

ADI

S_1

↓

$inc \rightarrow PC$

$ir^{(6-9)} \rightarrow rf(a_1)$

$ir^{(5-0)} \rightarrow b \rightarrow alu$

$rf(d_1) \rightarrow a \rightarrow alu$

$alu \rightarrow t_1$

↓

S_3

ADL

S_1

↓

S_6

↓

$t_1 \rightarrow a \rightarrow mux^{(1)}$

$ir^{(5-3)} \rightarrow rf(a_2)$

$rf(d_2) \rightarrow b \rightarrow mux^{(0)}$

$ir^{(5-3)} \rightarrow rf(a_3)$

$mux^{(0/P)} \rightarrow rf(d_3)$

S_{20}

$(1 \rightarrow mux^{(sel)})$

NDU

S_1

↓

S_6

↓

S_{20}

(alu op= NAND)

NDC

S_1

↓

S_6

↓

S_{17}

State names

(alu op = NAND)

State names

S_4

LW

S_1

↓

incr → PC

$ir^{(8-6)} \rightarrow rf(a_1)$

$ir^{(5-0)} \rightarrow b \rightarrow alu$

$rf(d_1) \rightarrow a \rightarrow alu$

$alu \rightarrow t_1$

↓

$t_1 \rightarrow a \rightarrow AO$

$di \rightarrow b \rightarrow rf(d_3)$

$ir^{(b-a)} \rightarrow rf(a_3)$

NDZ

S_1

↓

S_6

↓

S_{18}

(alu op = NAND)

S_9

SW

S_1

↓

S_4

↓

$t_1 \rightarrow a \rightarrow AO$

$ir^{(b-a)} \rightarrow rf(a_2)$

$rf(d_2) \rightarrow b \rightarrow do$

LHI

S_1

↓

incr → PC

$ir \rightarrow b \rightarrow alu$

$alu \rightarrow t_1$

↓

S_3

S_8

S_{10}

BEQ

State names

S_1

$ir^{(6-9)} \rightarrow rf(a_1)$

$ir^{(8-6)} \rightarrow rf(a_2)$

$rf(d_1) \rightarrow a \rightarrow alu$

$rf(d_2) \rightarrow b \rightarrow alu$

S_{11}

$alu \rightarrow t_1$

$Z \rightarrow alu$

$PC \rightarrow a \rightarrow alu$

$ir^{(5-0)} \rightarrow b \rightarrow alu$

S_{12}

$alu \rightarrow t_1$

$t_1 \rightarrow a \rightarrow PC$

S_{13}

JAL

S_1

$incr \rightarrow PC$

$PC \rightarrow a \rightarrow rf(d_3)$

S_5

$ir^{(6-9)} \rightarrow rf(a_3)$

$ir^{(8-0)} \rightarrow b \rightarrow alu$

$PC \rightarrow a \rightarrow alu$

S_{14}

$alu \rightarrow t_1$

S_{13}

State names

JLR

S_1

S_5

$ir^{(8-6)} \rightarrow rf(a_1)$

$rf(d_1) \rightarrow a \rightarrow PC$

S_{15}

JRI

S_1

$ir^{(6-9)} \rightarrow rf(a_1)$

$rf(d_1) \rightarrow a \rightarrow alu$

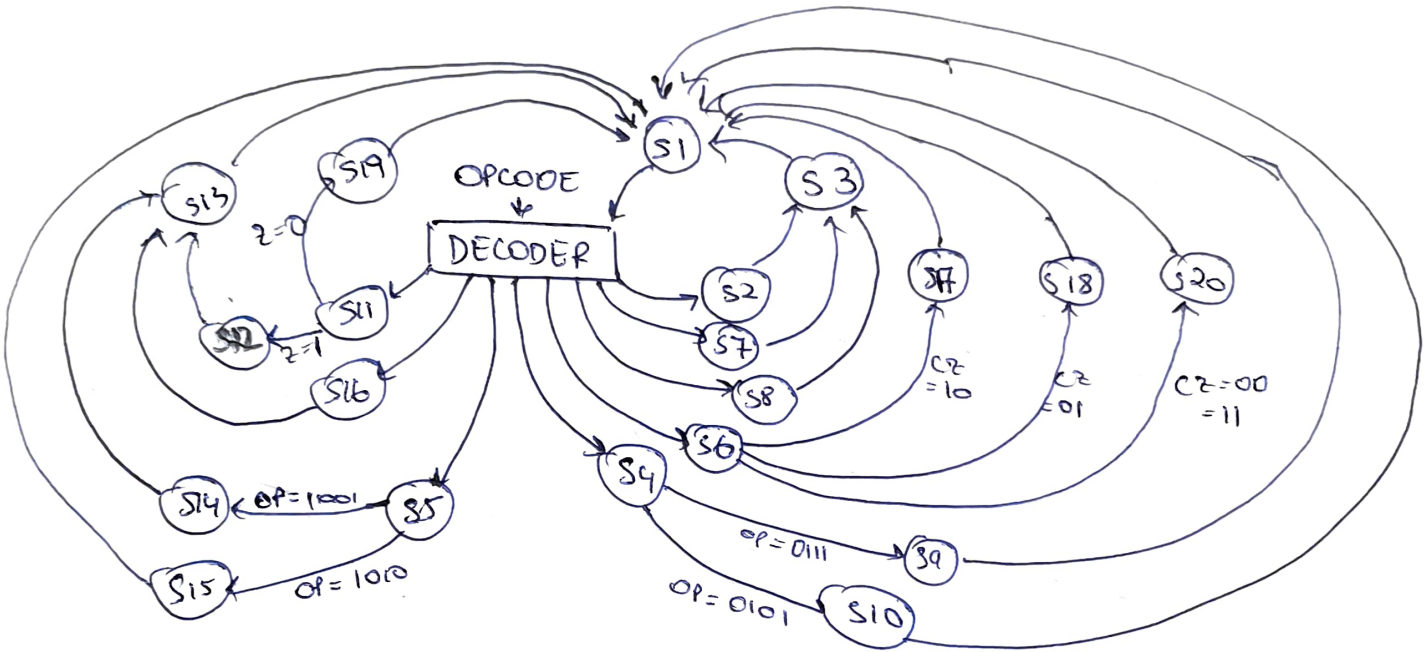
$ir^{(8-0)} \rightarrow b \rightarrow alu$

S_{16}

$alu \rightarrow t_1$

S_{13}

FSM


S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
S19
S20
OPCODE
DECODER
Z=0
Z=1
OP=1001
OP=1010
OP=0111
OP=0101
CZ=10
CZ=01
CZ=00
=11

Control bit logic

w	do	di	ao	IR	tl	rf
(1)	(1)	(2)	(1)	(3)	(2)	(5)

PC	MUX	ALU	CB	czen	rf_wr	(29 bits)
(3)	(4)	(2)	(1)	(2)	(1)	

S_1: PC = 001

S_2: PC = 011, IR = 010, rf = 00011, alu = 11, czen = 11

S_3: tl = 01, IR = 010, rf = 00100

S_7: IR = 011, rf = 00010, alu = 10, czen = 11

S_8: PC = 011, IR = 001, alu = 10

S_4: PC = 011, IR = 011, rf = 00010, alu = 10, czen = 01

S_9: tl = 01, ao = 1, di = 01, rf = 01000, ir = 010

S_{10}: tl = 01, IR = 010, PRf = 0010, do = 1, w = 1

S_{11}: IR = 10, rf = 00011, alu = 11

S_{19}: PC = 011

S_{13}: tl = 01, IC = 010

S_5: IC = 100, rf = 00100, ir = 010

S_{14}: IR = 001, PC = 100, ALU = 11

S_{15}: IR = 010, rf = 00001, PC = 010

S_6: IR = 010, rf = 00011, alu = 11, czen = 11

S_{17}: tl = 01, IR = 010, rf = 10010, mw = 0011

S_{18}: tl = 01, IR = 010, rf = 10010, mw = 0101

S_{20}: tl = 01, IR = 010, rf = 10010, mw = 1001

S_{12}: alu = 11, dir = 010, rf = 00011, cb = 1

S_{16}: ir = 011, rf = 00001, alu = 10

bit encoding.

rf (5):

- 1 bit: connects to mux else disconnects
- 1 to connect to bus A else disconnect
- 1 to conn to bus B else not
- 1 to write to BusB from $rf(d_2)$
- 1 to write to busA from $rf(d_1)$

IR (3):

- enable (1) connection to bus A (IR → bus A) disable (0)
- enable (1) write to rf
- enable write to bus B.

ALU (2):

- (1) enable connection to bus A (0) else not
- (1) read from bus B (0) not.

PC (3):

- enable (1) read from bus A
- enable (1) write to PC
- toggle mux 1 (1) else mux 0 (0).

MUX (4):

- (1) ~~write~~ select connected to 1
- (1) select comm. to 7
- (1) select comm. to C
- enable connection to $rf(d_3)$

t1: (2) (b1)

(1) write to bus B

(0) not

(1) write to A, else, not.

do(1): enable write to RAM

0: disable

di (2):

(1) enable write to A

(1) enable write to B bus

go: 1: write address

0: disable

w: (1) 1: write to Ram enabled

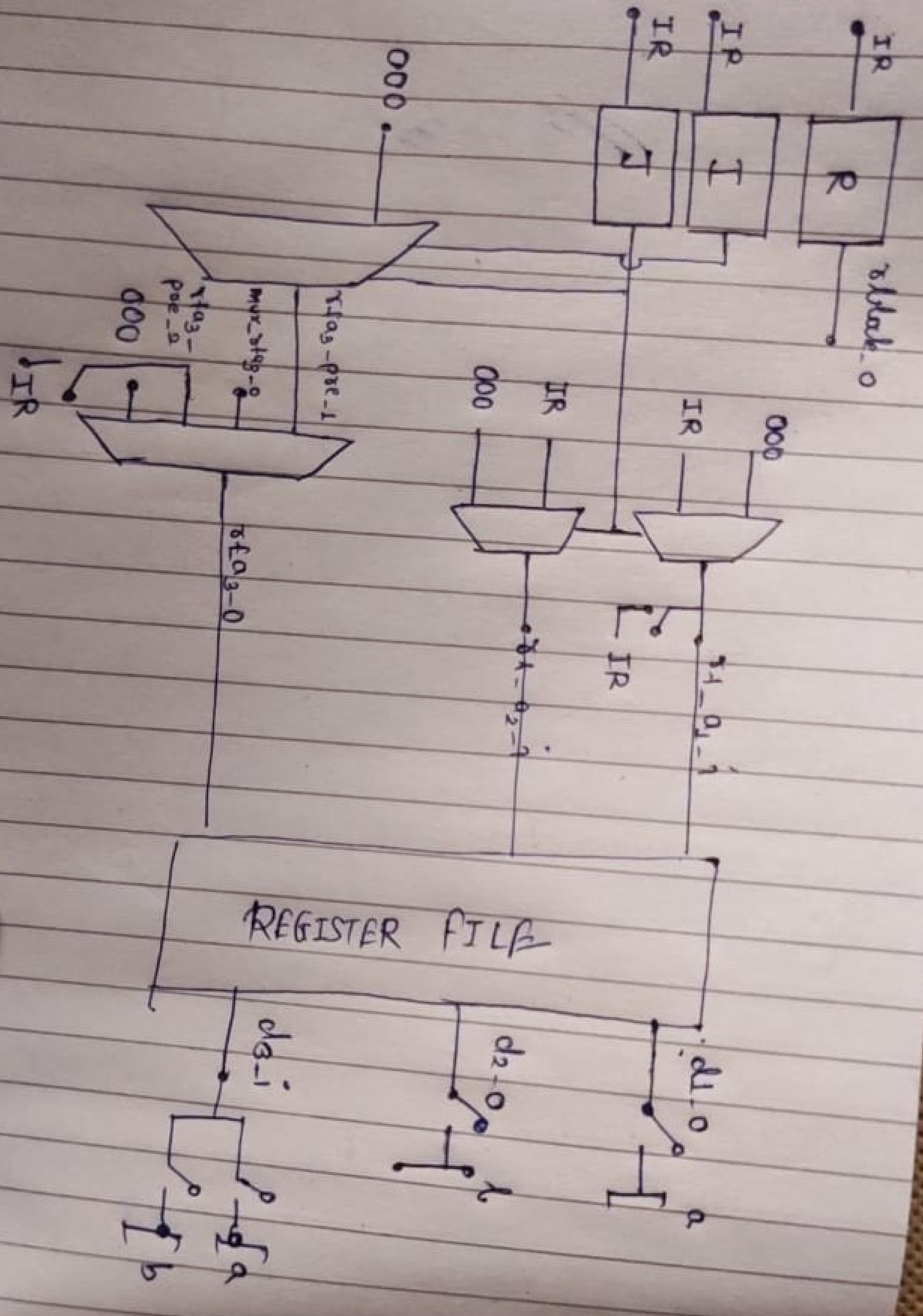
0: disabled

CB: (1) bit to alu.

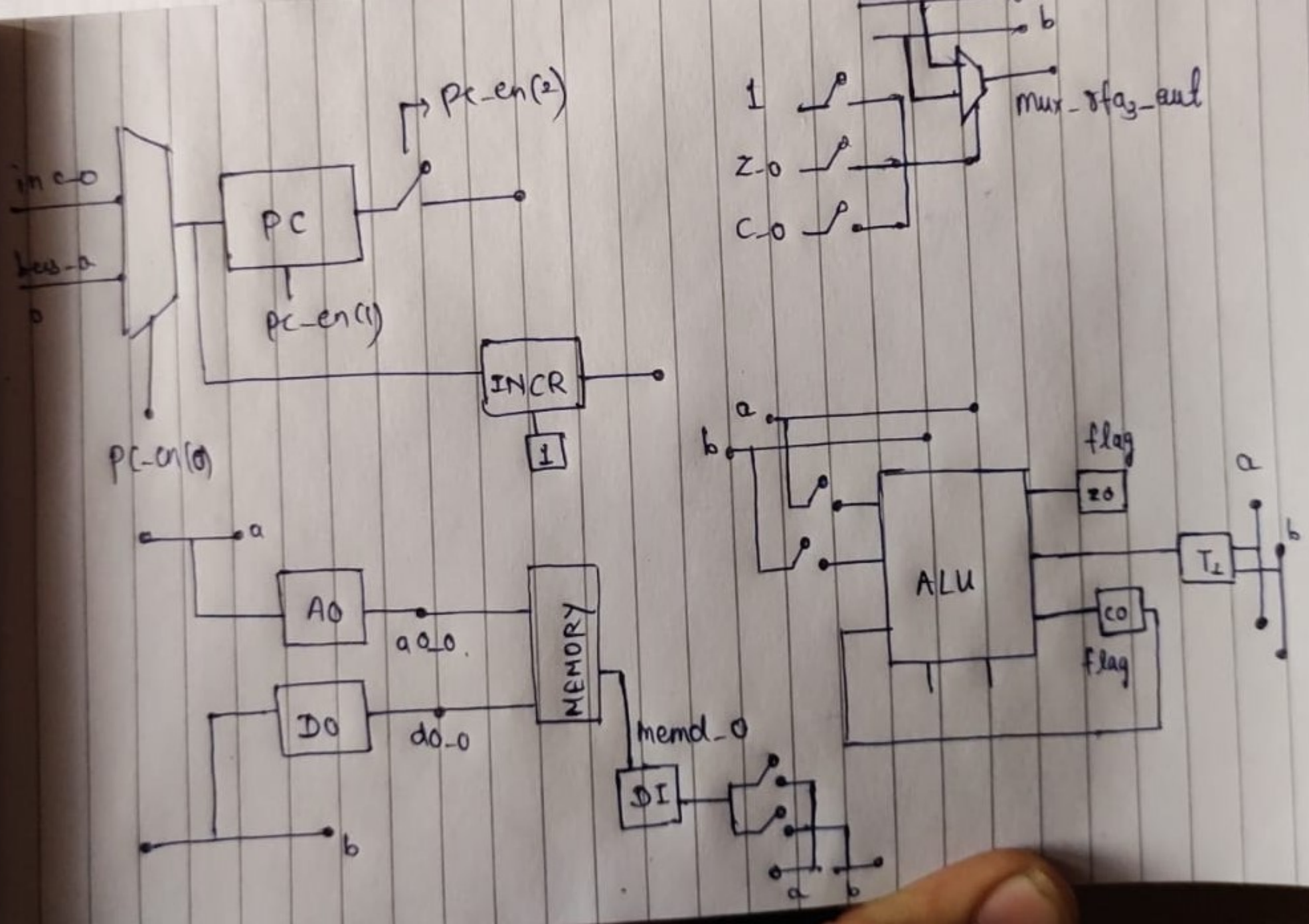
CZ : (2)

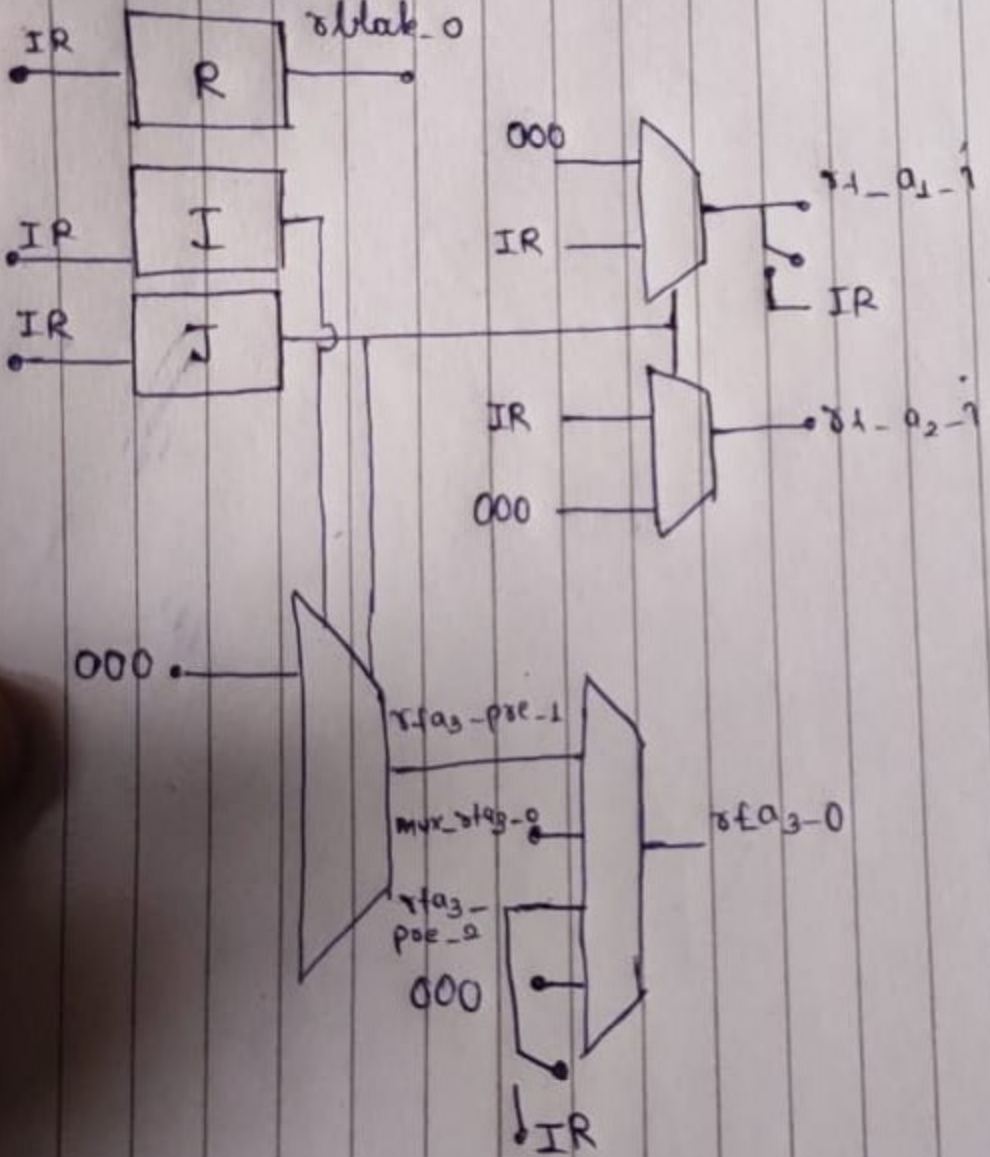
1 if Carry bit should be read else 0

1 if zero should be modified else 0.



IR
R
I
J
000
REGISTER FILE
IR


inc_o
bus_o
o
PC
pc_en(2)
pc_en(1)
pc_en(0)
INCR
1
a
AO
ao_o
DO
do_o
b
MEMORY
memd_o
DI
a
b
1
z_o
c_o
b
mux_rfa3_out
a
b
flag
ALU
zo
co
flag
T2
a
b


IR
R
rblak_0
IR
I
IR
J
000
IR
IR
r1_a1_1
IR
IR
r1_a2_1
000
000
rfa3_pse_1
mux_rfa3_0
rfa3_0
rfa3_poe_0
000
IR