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Academic Performance Summary

Year	Sem	SPI	CPI	Sem Credits Used for SPI	Completed Semester Credits	Cumulative Credits Used for CPI	Completed Cumulative Credits
2021	Spring	9.0	8.88	12.0	12.0	64.0	64.0
2021	Autumn	9.63	8.85	16.0	16.0	52.0	52.0
2020	Spring	8.67	8.5	18.0	18.0	36.0	36.0
2020	Autumn	8.33	8.33	18.0	18.0	18.0	18.0

Semester-wise Details

*This registration is subject to approval(s) from faculty advisor/Course Instructor/Academic office.

Year/Semester: 2022-23/Autumn

Year/Semester: 2021-22/Spring

Course Code	Course Name	Credits	Tag	Grade	Credit/Audit
EE 712	Embedded Systems Design	6.0	Department elective	BB	C
EE 800	High Speed Interconnects: Signaling and Synchronization	6.0	Department elective	AA	C

Year/Semester: 2021-22/Winter / Re-Exam

Course Code	Course Name	Credits	Tag	Grade	Credit/Audit
EE 694	Seminar	4.0	Core course	AA	C

Year/Semester: 2021-22/Autumn

Course Code	Course Name	Credits	Tag	Grade	Credit/Audit
EE 603	Digital Signal Processing and its Applications	6.0	Department elective	AB	C
EE 616	Electronic Systems Design	6.0	Department elective	AA	C
EE 694	Seminar	4.0	Core course	II	C

Year/Semester: 2020-21/Spring

Course Code	Course Name	Credits	Tag	Grade	Credit/Audit
EE 619	Radio Frequency Microelectronics Chip Design	6.0	Department elective	AB	C
EE 699	Delta Sigma Data Converters and their Applications	6.0	Department elective	AB	C
EE 719	Mixed-Signal VLSI Design	6.0	Department elective	BB	C

Year/Semester: 2020-21/Autumn

Course Code	Course Name	Credits	Tag	Grade	Credit/Audit
EE 618	CMOS Analog VLSI Design	6.0	Department elective	BB	C
EE 671	VLSI Design	6.0	Department elective	AB	C
EE 721	Hardware Description	6.0	Department elective	BB	C
EE 792	Communication Skills -II	4.0	Core course	PP	N
HS 791	Communication Skills -I	2.0	Core course	PP	N

High Performance OTA Design

Bhawana Srivastava (Roll no:203079017)

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***Abstract*—This report introduces a high performance operational trans-conductance amplifier which uses multistage feed-forward technique to increase gain and bandwidth. Feed-forward technique introduces left half plane (LHP) zero which provide positive phase shift and improve phase margin. This scheme does not uses miller compensation as it can decrease bandwidth by pole splitting. Multistage amplifier increases dc gain and have high accuracy by reducing error in final value. High unity gain bandwidth from feed-forward method provides fast settling.**

***Index Terms*-Operational trans-conductance amplifier, Miller capacitance, feed-forward technique, compensation methods, gm/id technology.**

I. Introduction

Nowadays most of the applications like Analog to digital converters, Delta sigma modulators, switched capacitors uses high gain, high bandwidth and fast settling amplifiers. A high-performance amplifier must have high gain and high bandwidth. High gain leads to more accuracy as error is inversely proportional to dc gain whereas high bandwidth is required for fast settling as time constant is inversely proportional to pole location. Having high gain as well as high bandwidth is hard to achieve as both have different circuit requirement, a high gain circuit requires multistage amplifier with long channel length but each stage introduces a low frequency LHP pole which further reduces bandwidth and have negative phase shift (which reduces phase margin), whereas a high bandwidth circuit requires single stage with short channel length but single stage amplifier is not able to provide required gain.

Phase compensation is used as phase margin must be greater than 45° for stable circuit. In this scheme of compensation, miller capacitor is not used as it shifts the dominant pole at low frequency due to pole splitting and reduces bandwidth. Right half plane (RHP) zero of miller capacitor has negative phase shift and hence lower the phase margin. Miller compensation scheme also uses nulling resistor which either introduces a pole to cancel RHP zero or shift that zero in LHP.

The proposed compensation is no capacitor feed-forward technique which provide high gain bandwidth product and is discussed in section II. Circuit implantation for two stage and three stage amplifiers using this scheme is discussed in section III. gm/Id methodology based data driven search algorithm is discussed in section IV and V.

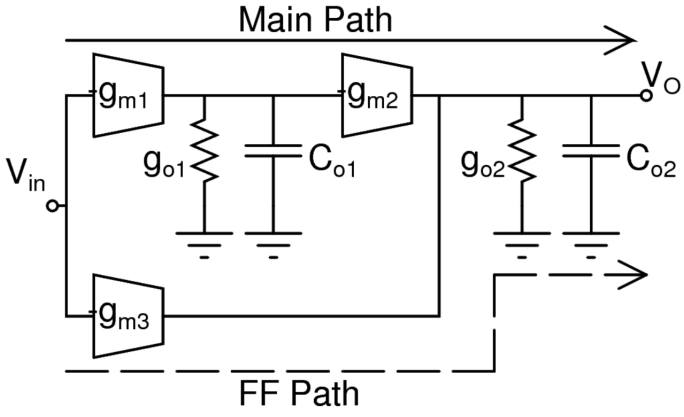

Fig. 1. Block diagram of two stage amplifier with NCFF compensation scheme

II. No-Capacitor Feed-forward (NCFF) Compensation Scheme For Multistage Amplifier

In this scheme, the positive phase shift of LHP zero created by feed-forward path is used to compensate the negative phase shift created by poles.

A. Two Stage amplifier with NCFF Compensation Scheme

Block diagram of two stage feed-forward scheme is shown in Fig. 1. Transfer function of this two-stage amplifier is derived by assuming single pole for all the three blocks. The dc gain of 1^{st} stage, 2^{nd} stage and feed-forward stage is $A_{V1}(=\frac{g_{m1}}{g_{o1}})$, $A_{V2}(=\frac{g_{m2}}{g_{o2}})$ and $A_{V3}(=\frac{g_{m3}}{g_{o2}})$ respectively. Pole location of 1^{st} stage is $\omega_{p1}(=\frac{g_{o1}}{C_{o1}})$ and that of 2^{nd} and feed-forward stage is $\omega_{p2}(=\frac{g_{o2}}{C_{o2}})$. Dominant pole is ω_{p1}. The overall amplifier gain is:

$$\begin{aligned} H(s) &= -\frac{A_{V1}A_{V2}}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} + \frac{A_{V3}}{(1+\frac{s}{\omega_{p2}})} \\ &= -\frac{A_{V1}A_{V2} + A_{V3}(1+\frac{s}{\omega_{p1}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \\ &= -\frac{(A_{V1}A_{V2}+A_{V3})(1+\frac{A_{V3}s}{(A_{V1}A_{V2}+A_{V3})\omega_{p1}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \end{aligned} \quad (1)$$

So the overall transfer function has two poles and one LHP zero. Total DC gain is $A_{V1}A_{V2}+A_{V3}$. From above equation, LHP zero can be given as:

$$\begin{aligned}\omega_z &= -\frac{(A_{V1}A_{V2}+A_{V3})\omega_{p1}}{A_{V3}} \\ &= -(1+\frac{A_{V1}A_{V2}}{A_{V3}})\omega_{p1} \\ &= -(1+\frac{\frac{g_{m1}}{g_{o1}}\frac{g_{m2}}{g_{o2}}}{\frac{g_{m3}}{g_{o2}}})\frac{g_{o1}}{C_{o1}} \\ &= -\frac{g_{m1}}{C_{o1}}\frac{g_{m2}}{g_{m3}}\end{aligned} \tag{2}$$

LHP zero is nearly equal to the product of gain bandwidth product of first stage $\frac{g_{m1}}{C_{o1}}$ and some constant $\frac{g_{m2}}{g_{m3}}$.
Effectively only one pole is present due to compensation of zero with the other pole and lead to 90° phase margin. Since there are no large capacitors like miller compensation scheme, area and power are much reduced in this technique. If the low impedance pole (non dominant pole) of first stage is considered then there will be total of three poles and two LHP zeros, this can be verified from equation 1. So it can be concluded that number of LHP zero is equal to order of first stage.

B. Three Stage amplifier with NCFF Compensation Scheme

Block diagram of two stage feed-forward scheme is shown in Fig. 2. DC Gain of main path, $A_{v1}A_{v2}A_{v3} = -g_{m1}r_{o1}g_{m2}r_{o2}g_{m3}r_{o3}$. DC Gain of 1^{st} FF path, $A_{vf1}A_{v3} = -g_{mf1}r_{o2}g_{m3}r_{o3}$. DC Gain of 2^{nd} FF path, $A_{vf2} = -g_{mf2}r_{o3}$. Therefore, Overall DC gain = $((A_{v1}A_{v2} + A_{vf1})A_{v3} + A_{vf2})$, which is greater than DC Gain of main path.
First stage has dominant pole at $\omega_{p1} = \frac{1}{r_{o1}C_{o1}}$. Second stage and first FF path has a common pole at $\omega_{p2} = \frac{1}{r_{o2}C_{o2}}$. Third stage and second FF path has a common pole at $\omega_{p3} = \frac{1}{r_{o3}C_{o3}}$.

The overall amplifier gain is:

$$\begin{aligned}H(s) &= -[\frac{A_{V1}A_{V2}}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} + \frac{A_{Vf1}}{(1+\frac{s}{\omega_{p2}})}]\frac{A_{V3}}{(1+\frac{s}{\omega_{p3}})} \\ &\quad + \frac{A_{Vf2}}{(1+\frac{s}{\omega_{p3}})} \\ &= -\frac{A_{V1}A_{V2}A_{V3} + A_{Vf1}A_{V3}(1+\frac{s}{\omega_{p1}}) + A_{Vf2}(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})(1+\frac{s}{\omega_{p3}})} \\ &= -K\frac{1+\frac{s(A_{Vf1}A_{V3}+A_{V3})}{K\omega_{p1}} + \frac{sA_{Vf2}}{K\omega_{p1}}) + \frac{s^2A_{Vf2}}{K\omega_{p1}\omega_{p2}}}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})(1+\frac{s}{\omega_{p3}})}\end{aligned} \tag{3}$$

So the overall transfer function has three poles and two LHP zeros. From above equation, LHP zeros can be given as:

$$\begin{aligned}\omega_{z1}\omega_{z2} &= \frac{A_{V1}A_{V2}A_{V3} + A_{Vf1}A_{V3} + A_{Vf2}}{A_{Vf2}}\omega_{p1}\omega_{p2} \\ &= \frac{A_{V1}A_{V2}A_{V3}}{A_{Vf2}}\omega_{p1}\omega_{p2} \\ &= -A_{V1}\omega_{p1}\frac{A_{V2}}{A_{Vf1}}A_{Vf1}\omega_{p2}\frac{A_{V3}}{A_{Vf2}}\end{aligned} \tag{4}$$

Similarities with two stage FF circuit will lead to the approx. calculated value of both LHP zeros, which are:

$$\begin{aligned}\omega_{z1} &= -\frac{\frac{g_{m1}}{g_{o1}}\frac{g_{o1}}{C_{o1}}\frac{g_{m2}}{g_{o2}}}{\frac{g_{mf1}}{g_o 2}} \\ &= -\frac{g_{m1}}{C_{o1}}\frac{g_{m2}}{g_{mf1}}\end{aligned} \tag{5}$$

$$\omega_{z2} = -\frac{g_{mf1}}{C_{o2}}\frac{g_{m3}}{g_{mf2}} \tag{6}$$

So LHP zero is nearly equal to the product of gain bandwidth product and some constant.

III. Circuit Realization

For higher phase margin, gain crossover frequency must lie before phase crossover frequency, so the non dominant pole ω_{p2} must be placed after the unity gain bandwidth. Pole zero cancellation occurs at higher frequency so that bandwidth is high and response is faster corresponds to lower settling time.

A. Two Stage Amplifier Circuit with NCFF Compensation Scheme

The two stage amplifier circuit with NCFF compensation is shown in Fig. 3. First stage must contribute to high gain as this stage is telescopic amplifier and have high dc gain. Voltage swing of first stage need not to be high. Second stage and feed-forward stage must contribute to high bandwidth. Load capacitance must be low so that pole will get shifted to high frequency and bandwidth increases. Trans-conductance g_{m2} and g_{m3} should also be high to push poles at high frequency.

First stage with M_1, M_4, M_5 and M_6 is single ended Telescopic amplifier. Second stage with M_2 and M_7 and feed-forward stage with M_3 and M_7 are single ended differential amplifiers. The dc gain of all stages are:

$$A_{V1} = g_{m1}[(g_{m4}r_{ds4}r_{ds1})||(g_{m5}r_{ds5}r_{ds6})] \tag{7}$$

$$A_{V2} = g_{m2}(r_{ds2}||r_{ds3}||r_{ds7}) \tag{8}$$

$$A_{V3} = g_{m3}(r_{ds2}||r_{ds3}||r_{ds7}) \tag{9}$$

Load capacitance of first stage and first pole location:

$$C_{o1} = \frac{C_{gs2}}{2} + C_{gd4} + C_{gd5} \tag{10}$$

$$\omega_{p1} = \frac{g_{o1}}{C_{o1}} \tag{11}$$

Output conductance of second stage and second pole location:

$$g_{o2} = g_{ds2} + g_{ds3} + g_{ds7} \tag{12}$$

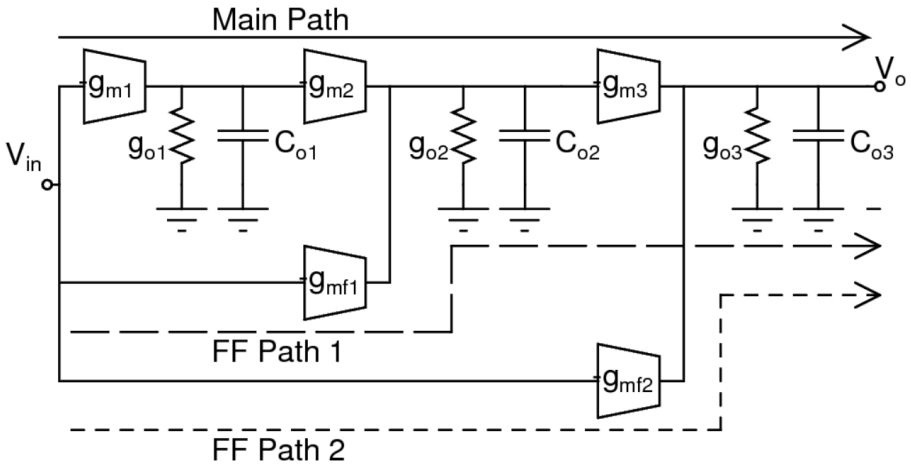

Fig. 2. Block diagram of three stage amplifier with NCFF compensation scheme

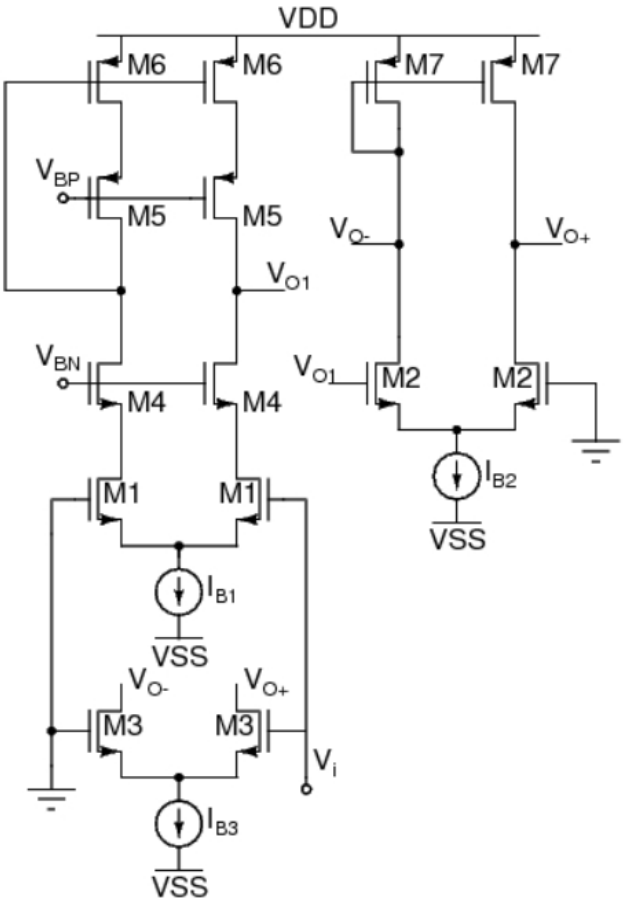

Fig. 3. Circuit implementation of two stage amplifier with NCFF compensation scheme

$$C_{o2} = C_L$$
$$\omega_{p2} = \frac{g_{o2}}{C_{o2}} \tag{13}$$

B. Three Stage Amplifier Circuit with NCFF Compensation Scheme

The circuit shown in Fig.4 is split path implicit FFC scheme. In this, the N-side of CMOS input structure contributes the main signal path and is considered as first, second and third stage whereas P-side of second and third stage contributes the feed-forward path. Since the feed-forward path is implicitly attached with main path hence the name of this circuit is implicit FFC. Explicit FFC structures often introduce significant parasitic and can degrade the high-frequency characteristics and stability of the circuit.

A local Common mode feedback circuit (CMFB) is used in first stage for common mode gain stabilization. Fine tuning is required to get proper gain and bandwidth as both the main and feed-forward path are common. Gain for the main path, the first FF path and second FF path are $-g_{m1}r_{o1}Xg_{m2}r_{o2}Xg_{m3}r_{o3}$, $-g_{mf1}r_{o2}Xg_{m3}r_{o3}$ and $-g_{mf2}r_{o3}$ respectively. The two design concerns are: 1) First stage DC gain should be high so that the error is less and hence noise is less, 2) Since in the second stage, main path and feed-forward path has common bias current and load so sizing the transistors for tuning can lead to trade-off between gain and bandwidth. So to fine-tune them, the second stage NMOS is split into two parts, one of which is used for main path while the other is used for feed-forward path with a transistor size ratio of 4:1. So the name of this technique is split-path implicit FFC.

IV. GM/ID METHODOLOGY BASED DATA DRIVEN SEARCH ALGORITHM

gm/Id method is more effective than traditional square law method as it takes care of short-channel effect. In traditional

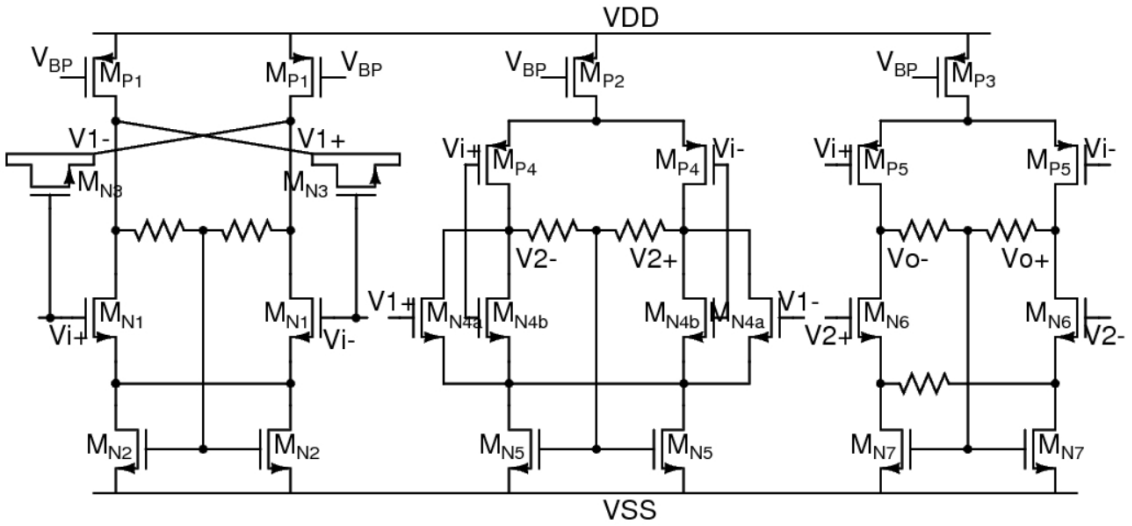

Fig. 4. Three stage split path implicit FFC amplifier with NCFF compensation

transistors, the drain voltage V_{DS}) increases but the drain current is constant in saturation region but in case of short channel, although gate voltage V_{GS}) is less then V_T) than also drain current flows and increases with V_{DS}), because threshold voltage decreases and current flows due to channel charge leakage know as drain induced barrier lowering (DIBL). But in gm/Id Methodology, this short channel effect is taken into account and I_D increases with V_{DS}). Also gm/Id methodology calculate sizes on basis of all the terminal voltages and length of transistor. Gate-induced drain leakage (GIDL) is another short channel effect which fails with traditional equations of current but works well with gm/Id method.

This method has a drawback, as it is based on single-pole model for each stage of amplifier. In feed-forward compensation amplifier gain is low and hence unity gain frequency is decade away from dominant pole ω_{p1}, so non dominant pole and zeros at high frequency doesn't count. With the increase in fu, non dominant poles and zeros also count and this topology fails. To overcome this limitation, changes are done and the effectiveness of this methodology increases. Example is taken to explain this corrective measure. The circuit shown in Fig. 5 is single-stage common-source (CS) amplifier with a Low threshold voltage PMOS transistor as input and an Regular threshold voltage NMOS transistor as active load and Fig. 6 is showing its small-signal equivalent (SSE). Half circuit of differential amplifier is similar to this SSE circuit hence both will behave similarly.

Gate-to-source (Cgs) capacitance and gate-to-body (Cgb) capacitance combined as a single Cin because source and body of PMOS are at same potential. Combining drain-to-source conductance of both NMOS and PMOS into $\frac{1}{R_L}$, the equations are as follows:

$$\begin{aligned} \text{Total drain capacitance, } C_{dd} &= C_{dg} + C_{db} \\ \text{Total gate capacitance, } C_{gg} &= C_{gd} + C_{gs} + C_{gb} \end{aligned} \tag{14}$$

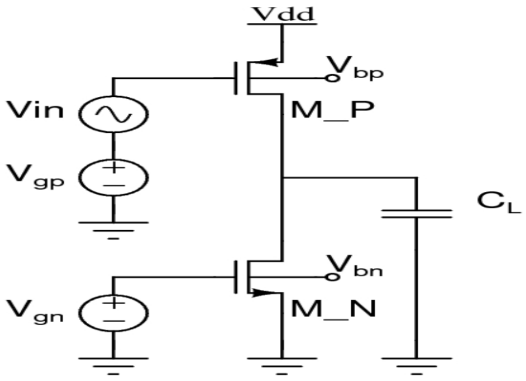

Fig. 5. Common source amplifier

$$C_{Ltot} = C_L + C_{ddp} – C_{dgp} + C_{ddn} = C_L \tag{15}$$

$$C_{in} = C_{ggp} - C_{gdp} = C_{gsp} + C_{gbp} \tag{16}$$

$$\frac{1}{R_L} = g_{dsp} + g_{dsn} \tag{17}$$

$$Z_{tot} = R_L || \frac{1}{sC_{Ltot}} \tag{18}$$

$$P1 = -\frac{1}{R_L} C_{Ltot} + c_{gdp} \tag{19}$$

A. Non dominant Pole and its effect

This exist because of the gate resistance which appears as parasitic. This always lies after the transit frequency (fT) and if unity gain frequency (fu) is smaller than transit frequency (fT) then the effect of this non dominant pole is least.

Also, to minimize its effect the non dominant pole is placed near zero so that they both cancel each other's effect. Hence efforts are made to keep non dominant pole and zero after the fu and to select a phase margin which can tolerate the effect of both of them. Non dominant pole is nearly located at $\frac{g_{mp}}{2\pi C_{gg}}$.

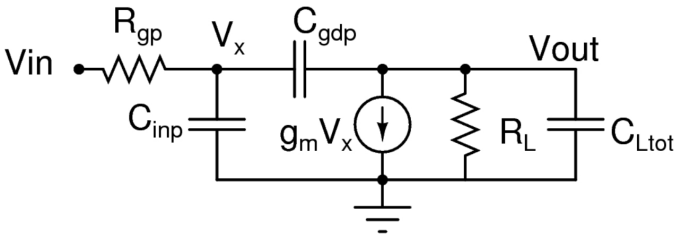

Fig. 6. Small signal equivalent

B. Right half plane Zero and its effect

RHP zero comes into picture when there is direct connection between input and output which happens here because of PMOS gate-to-drain capacitance (C_{gdp}). This affect the transfer function as the gain rises by the factor of 20 dB/decade because of RHP zero. It also decreases 90° from phase margin. Hence in single pole assumption circuit model, RHP zero's effect can be minimized by keeping this at or beyond ten times of the location of fu.

V. Nth order Feed-forward Compensation Circuit

Nth order Feed-forward Compensation Circuit is shown in Fig. 7. Using same pattern as for second and third order, the transfer function of nth order feed-forward compensation circuit can be given as:

$$A_{mi}(s) = \frac{A_{omi}}{1 + \frac{s}{P_i}}, i = 1, 2, ..., n \tag{20}$$

where A_{mi} is transfer function and A_{omi} is DC gain of the ith-stage of main path.

$$A_{fi}(s) = \frac{A_{ofi}}{1 + \frac{s}{P_i}}, i = 1, 2, ..., n \tag{21}$$

where A_{fi} is transfer function and A_{ofi} is DC gain of the ith-stage of feed-forward path.

Overall Transfer function is:

$$\begin{aligned} TF_{S_n}(s) = \prod_{i=1}^{n} A_{mi}(s) + A_{f2}(s) \prod_{i=3}^{n} A_{mi}(s) \\ + A_{f3}(s) \prod_{i=4}^{n} A_{mi}(s) + ... + A_{fn}(s) \end{aligned} \tag{22}$$

Taking into account the single-pole amplifier model, number of poles are n and number of RHP zeros are n-1. From the Fig. 7, ith pole location can be given as:

$$P_i = \frac{1}{R_i C_i} \tag{23}$$

From above equation, it can be concluded that Low pass delta-sigma modulator has its poles at low frequency so by keeping large capacitors at output of each node will shift the poles at low frequency, similarly Band pass delta-sigma modulator should not have its poles at low frequency so there is no requirement of external capacitor.

VI. Description and components of gm/Id methodology

Sizes of the transistors, the current consumption per stage and the body biasing voltages are required for each of the transistors.

This method contains three algorithm which is explained by three blocks as shown in Fig. 8. These blocks are Transfer function generator, DC operating point generator and transistor size (width) generator.

A. First Block

First block is transfer function generator block. It takes four parameters as input:(1) total dc gain (A_o) required, (2) phase margin (PM) required, (3) minimum phase (ϕ_{min}) required for frequencies less then unity gain frequency so as to make sure that system is always stable below fu and phase margin does not crosses 180° line and comes back to it, and (4) gain at center frequency of the BP delta-sigma (A_{fo}) so that gain does not decrease till center frequency and meet the required value. This block generate transfer functions that meet up the requirements. When transfer function is generated then poles and dc gains are generated for each main path and feed-forward amplifier based on single pole model as discussed above. Maximum current consumption per stage and the capacitive load to be driven by the amplifier together will give maximum unity gain frequency per stage which will give maximum pole. Gain start decreasing after minimum pole. Number of stages and total desired dc gain will fix minimum pole. Minimum pole value is set as decades smaller than 3dB frequency (fo) and then algorithm regenerates minimum pole until it became nearly equal to fo such that the gain at fo became equal to 3dB gain. When unity gain frequency of each stage is fixed then:

$$\text{minimum pole} = \frac{f_u}{\text{max dc gain}} \tag{24}$$

(Constant gain bandwidth product)

$$\text{DC gain for each stage} = \frac{\text{the total desired dc gain}}{\text{number of stage of the amplifier}} \tag{25}$$

B. Second Block

Second block is DC operating point generator or solver block. This block find DC operating point for each amplifier according to dc gain required. For biasing transistor, DC operating points are required like V_{GS}, V_{DS}, V_{SB}, and L.

$$\text{DC gain of a one stage (Ami or Afi)} = \frac{(\frac{g_m}{I_d})_{mi/fi}}{(\frac{g_{ds}}{I_d})_{mi} + (\frac{g_{ds}}{I_d})_{fi}} \tag{26}$$

(gm/Id method is used to calculate gain)

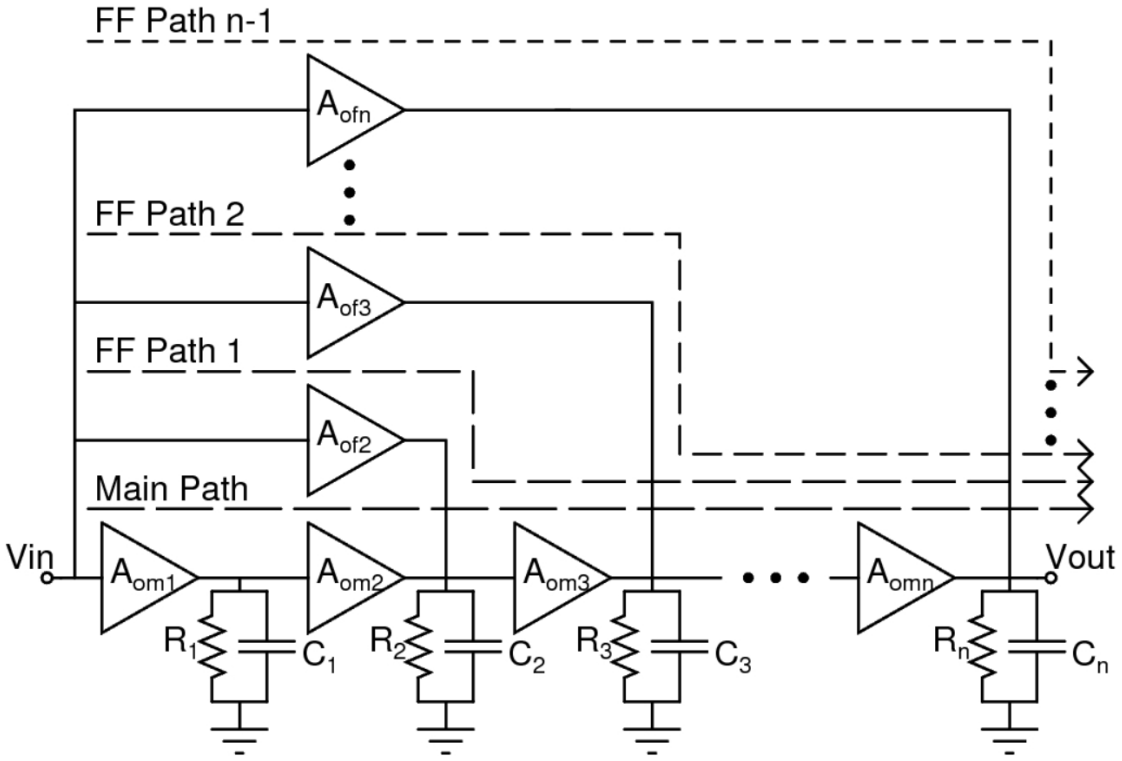

Fig. 7. Block diagram for Nth order amplifier with NCFF compensation scheme

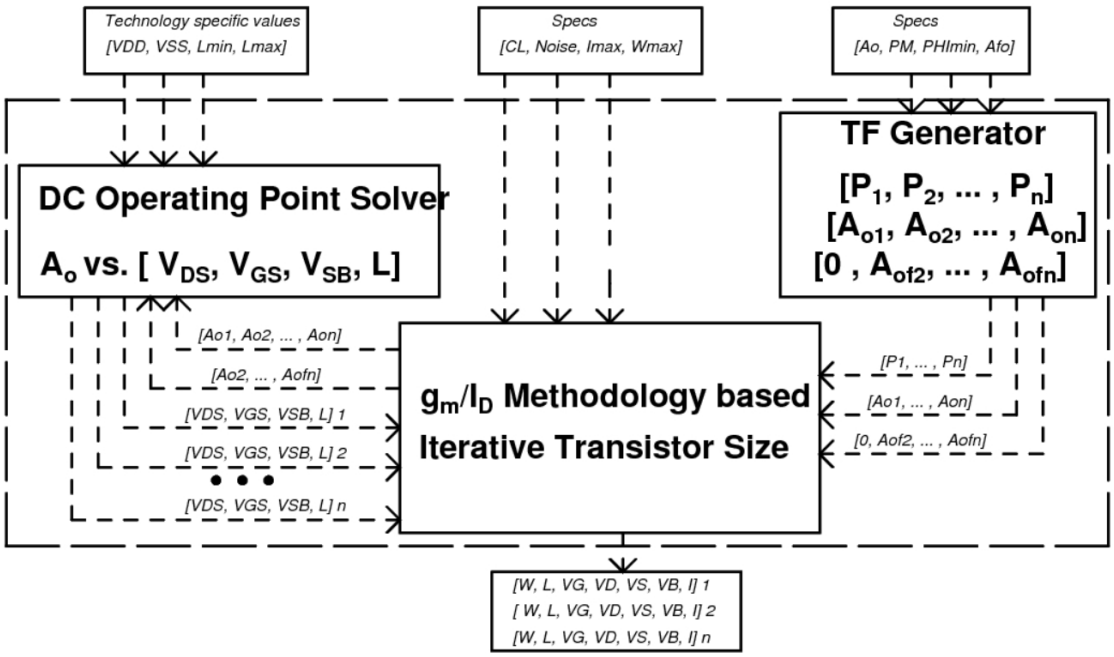

Fig. 8. Block diagram for gm/Id methodology based algorithm

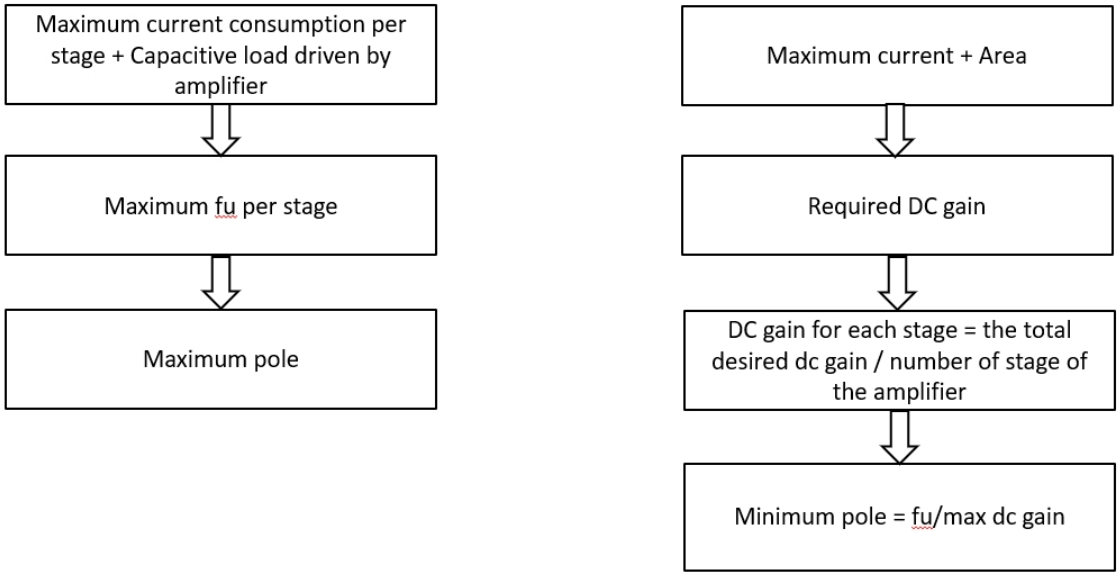

Fig. 9. Flowchart for first algorithm

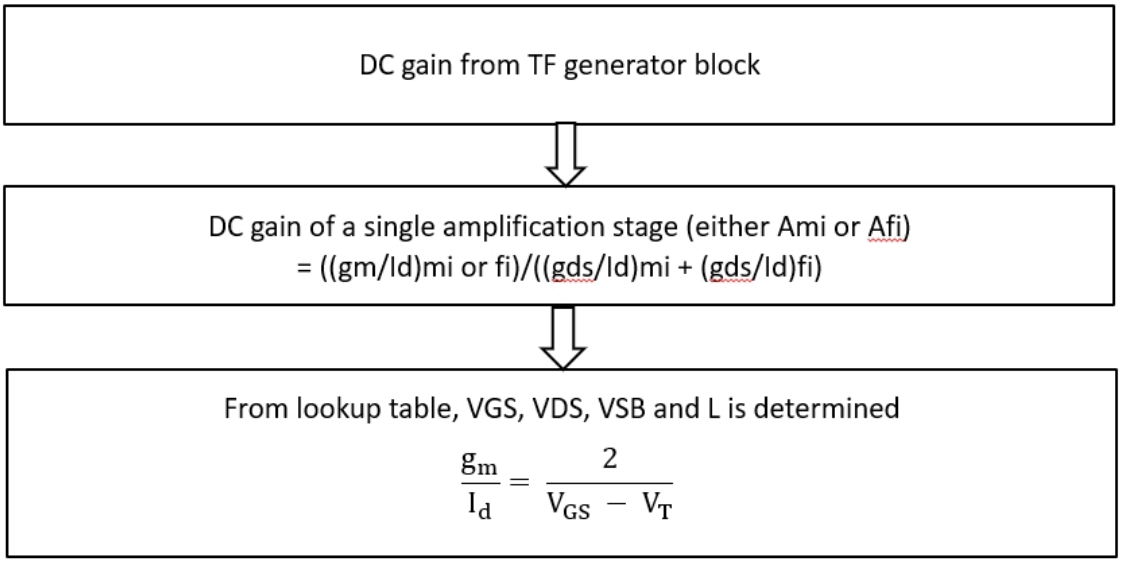

Fig. 10. Flowchart for second algorithm

$$\frac{g_m}{I_d} = \frac{2}{V_{GS} - V_T} = \frac{2}{V_{OV}} \tag{27}$$

A pre-computed lookup table will give above values based on dc operating points but simulation time is large. Algorithm is made for this search purpose where each stage has some limits and can use these values:

1) For different technologies V_{DD}, V_{SS}, L_{min} and L_{max} values are different and hence there is need to set different values for $V_{GS/GD/GB/SD/SB/BD}$ for achieving required specifications like input/output swing etc.

2) Common mode voltage of Input/Output so that there is no or less signal distortion. DC operating point generator block need to be defined in a certain range in accordance with: 1) Saturation voltage (VD_{SAT}) or overdrive voltage (V_{OV}) = gate to source voltage (V_{GS}) - threshold voltage (V_T) 2) Marginal saturation voltage (VDS_{marg}) = drain to source voltage (V_{DS}) — saturation voltage (VD_{SAT}) 3) Input swing or peak to peak voltage 4) output swing or peak to peak voltage First two points are for keeping transistors in active region while last two points are to make sure that the required signal to noise ratio (SNR) is achieved.

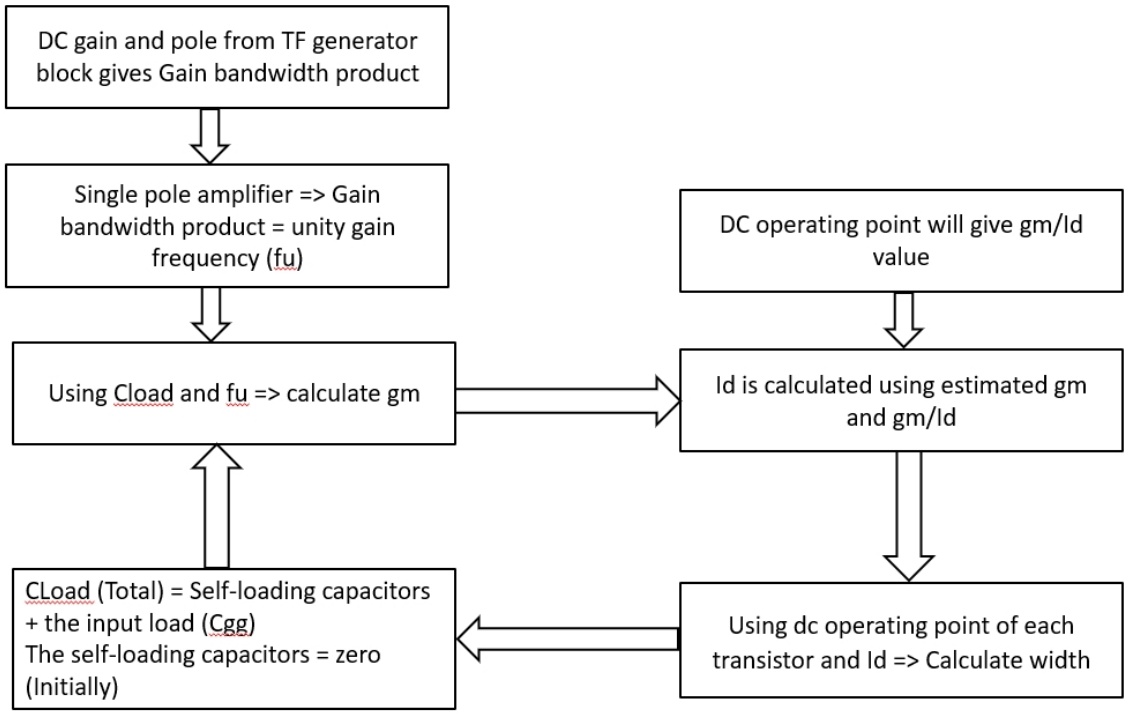

Fig. 11. Flowchart for third algorithm

C. Third Block

This is the main block as it generates size (width) of transistors. Transfer function generator block will give DC gain and pole values of each amplification stage and hence gain bandwidth product of each is known, also DC operating point generator block will give dc values according to required dc gain and both will help in sizing g_m values for each stage. As this is single pole model circuit, hence GBW is fu. By using output load, size of last stage is calculated. For rest of the stages, output load is equal to input load of next stage (C_{gg}) and self loading capacitor value which is zero for initial iteration. According to DC operating values, g_m and g_m/I_d is defined and further used to calculate I_d. This is further used to find width of transistors for given DC values. In the second and further iteration this width is used to calculate self loading capacitors and process repeats till the desired width is obtained which depends on its maximum value, maximum current and noise etc.

VII. Conclusion

Two stage amplifier with no miller capacitor feedforward compensation helps in achieving high gain, high unity gain bandwidth and good phase margin [1]. Three stage amplifier with split path implicit FFC compensation uses 1.5 V power supply has good power efficiency. A Common Mode Feedback circuit is also used to stabilize the CM gain. It gives very high unity gain bandwidth and is unconditionally stable with phase margin greater then 42° [2]. Unlike conventional design methods, the Nth order amplifier with NCFF compensation scheme is designed by using gm/Id methodology and helps in achieving the high unity-gain-frequency and good phase margin [3].

VIII. References

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