Tutorial 3: ALU and HDL Basics

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October 17, 2021

1 Questions

1. One of the main differences between a microcontroller and an FPGA is that an FPGA doesn't have a fixed hardware structure, while a microcontroller does. While FPGAs include fixed logic cells, these, along with the interconnects, can be programmed in parallel by using HDL coding language.

   FPGA Advantages

   - FPGAs can be programmed at logic level. Hence it can implement faster and parallel processing of signals.
   - FPGAs are programmable at software level at any time. Hence FPGA IC can be re-programmed or reused any number of times. FPGA can also be programmed from remote locations.

   FPGA Disadvantages

   - The programming of FPGA requires knowledge of VHDL/Verilog programming languages as well as digital system fundamentals. The programming is not as simple as C programming used in processor based hardware. Moreover engineers need to learn use of simulation tools.
   - Expensive, Volatile, Complex tooling and Slow for general purpose operations.

2. **Blocking:**

   - Blocks following statements until complete.
   - Blocking statements are executed sequentially.
   - Evaluate and update immediately.

   Non-blocking:

   - Statements are execute in parallel.
   - Evaluate immediately but only update after evaluating all statements.

   Comparisons

   - The code snippets on the left uses blocking assignment, and it will always suffer from the problem of race condition when the assignment happen to it from two processes concurrently.
   - While the code snippets on the right uses non-blocking assignment, so it will not suffer from the problem of race condition, since the updated value is assigned after the time step.

3. The output of both program is going to be the same, the difference is the code on the left is instantiating a module by order while code on the left is instantiating a module by name(we can see "." represent port name followed by associated port name in small brackets). Port mapping by name is better method when when instantiating a module with many ports because it is easy to port map for large number of ports in a design where in port mapping by order when ports are increased its very difficult to do "module ports by order".