```
1  ----------------------------------------------------------------------------------
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    15:20:40 08/24/2023
6  -- Design Name:
7  -- Module Name:    shiftregistrer - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 ----------------------------------------------------------------------------------
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22
23 -- Uncomment the following library declaration if using
24 -- arithmetic functions with Signed or Unsigned values
25 --use IEEE.NUMERIC_STD.ALL;
26
27 -- Uncomment the following library declaration if instantiating
28 -- any Xilinx primitives in this code.
29 --library UNISIM;
30 --use UNISIM.VComponents.all;
31
32 entity shiftregistrer is
33     Port ( s : in  STD_LOGIC_VECTOR (3 downto 0);
34            m : in  STD_LOGIC_VECTOR (1 downto 0);
35            y : out  STD_LOGIC_VECTOR (3 downto 0);
36            clk : in  STD_LOGIC;
37            rst : in  STD_LOGIC);
38 end shiftregistrer;
39
40 architecture Behavioral of shiftregistrer is
41  signal t : std_logic_vector(3 downto 0);
42  begin
43  process(clk,rst)
44  begin
45  if rst='1' then
46  y<="0000";
47  elsif clk' event and clk ='1' then
48  case m is
49
50  when "00" =>
51  t(3)<=s(0);
52  t(2)<=t(3);
53  t(1)<=t(2);
54  t(0)<=t(1);
55  y(0)<=t(0);
56
57 when "01" =>
```

```
58     t(3)<=s(0);
59     t(2)<=t(3);
60     t(1)<=t(2);
61     t(0)<=t(1);
62     y<=t;
63
64    when "10" =>
65    t<=s;
66    y<=t;
67
68    when "11" =>
69     t<=s;
70     t(2)<=t(3);
71     t(1)<=t(2);
72     t(0)<=t(1);
73     y(3)<=t(0);
74
75     when others => NULL;
76
77     end case;
78     end if;
79     end process;
80
81    end Behavioral;
82
83
```