```
1   ----------------------------------------------------------------------------------
2   -- Company:
3   -- Engineer:
4   --
5   -- Create Date:   15:51:06 09/21/2023
6   -- Design Name:
7   -- Module Name:   C:/Users/ETC-VLSI LAB/Desktop/vlsi/FIFO/testFIFO.vhd
8   -- Project Name:  FIFO
9   -- Target Device:
10  -- Tool versions:
11  -- Description:
12  --
13  -- VHDL Test Bench Created by ISE for module: fifo_ent
14  --
15  -- Dependencies:
16  --
17  -- Revision:
18  -- Revision 0.01 - File Created
19  -- Additional Comments:
20  --
21  -- Notes:
22  -- This testbench has been automatically generated using types std_logic and
23  -- std_logic_vector for the ports of the unit under test.  Xilinx recommends
24  -- that these types always be used for the top-level I/O of a design in order
25  -- to guarantee that the testbench will bind correctly to the post-implementation
26  -- simulation model.
27  ----------------------------------------------------------------------------------
28  LIBRARY ieee;
29  USE ieee.std_logic_1164.ALL;
30
31  -- Uncomment the following library declaration if using
32  -- arithmetic functions with Signed or Unsigned values
33  --USE ieee.numeric_std.ALL;
34
35  ENTITY testFIFO IS
36  END testFIFO;
37
38  ARCHITECTURE behavior OF testFIFO IS
39
40      -- Component Declaration for the Unit Under Test (UUT)
41
42      COMPONENT fifo_ent
43      PORT(
44           enr : IN  std_logic;
45           enw : IN  std_logic;
46           dataout : OUT  std_logic_vector(3 downto 0);
47           datain : IN  std_logic_vector(3 downto 0);
48           empty : OUT  std_logic;
49           full : OUT  std_logic;
50           clk : IN  std_logic
51          );
52      END COMPONENT;
53
54
55     --Inputs
56     signal enr : std_logic := '0';
57     signal enw : std_logic := '0';
```

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58      signal datain : std_logic_vector(3 downto 0) := (others => '0');
59      signal clk : std_logic := '0';
60
61      --Outputs
62      signal dataout : std_logic_vector(3 downto 0);
63      signal empty : std_logic;
64      signal full : std_logic;
65
66      -- Clock period definitions
67      constant clk_period : time := 10 ns;
68
69   BEGIN
70
71      -- Instantiate the Unit Under Test (UUT)
72      uut: fifo_ent PORT MAP (
73             enr => enr,
74             enw => enw,
75             dataout => dataout,
76             datain => datain,
77             empty => empty,
78             full => full,
79             clk => clk
80           );
81
82      -- Clock process definitions
83      clk_process :process
84      begin
85         clk <= '0';
86         wait for clk_period/2;
87         clk <= '1';
88         wait for clk_period/2;
89      end process;
90
91
92      -- Stimulus process
93      stim_proc: process
94      begin
95
96            enw<='1';
97            datain<="1110";
98            wait for 10 ns;
99            datain<="1100";
100           wait for 10 ns;
101           datain<="1000";
102           wait for 10 ns;
103           datain<="0000";
104           wait for 10 ns;
105           datain<="1111";
106           wait for 10 ns;
107           datain<="0100";
108           wait for 10 ns;
109           datain<="0110";
110           wait for 10 ns;
111           datain<="0011";
112           enw<='0';
113           wait for 10 ns;
114
```

```
115             enr<='1';
116
117
118         wait;
119       end process;
120
121   END;
122
```