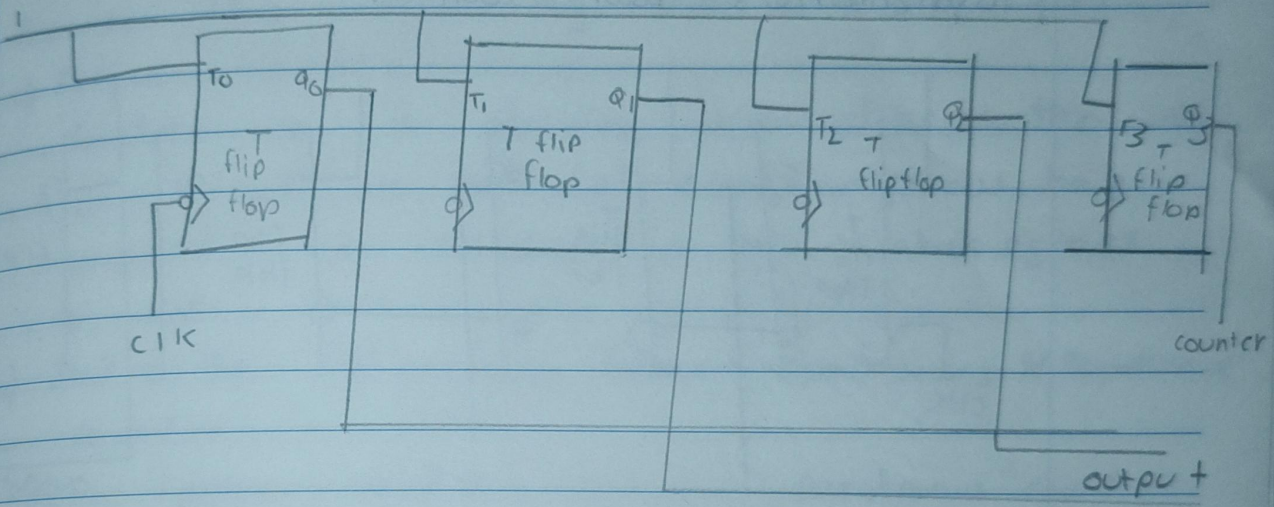
Expt - 05

1 Title :- Verify the ~~truth~~ table of up/down counter

2 Logic diagram & truth table of async. up/down counter

Asynchronus up counter ~~& asynchronous down counter~~

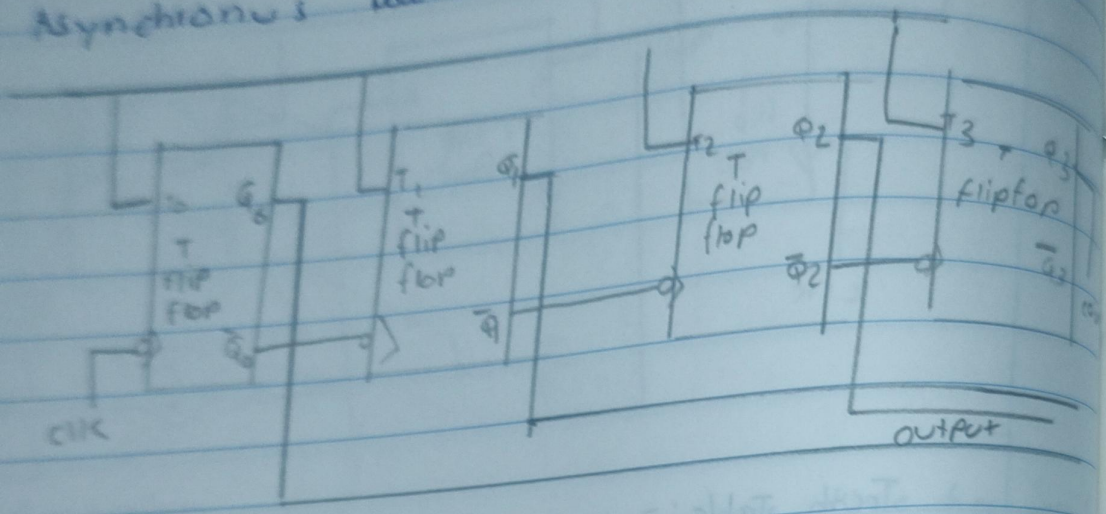


Truth Table :-

State	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
16	1	0	1	0

11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Asynchronous Down Counter



Truth Table

State	Q_3	Q_2	Q_1	Q_0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1

4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

3) Answer the following practical related questions

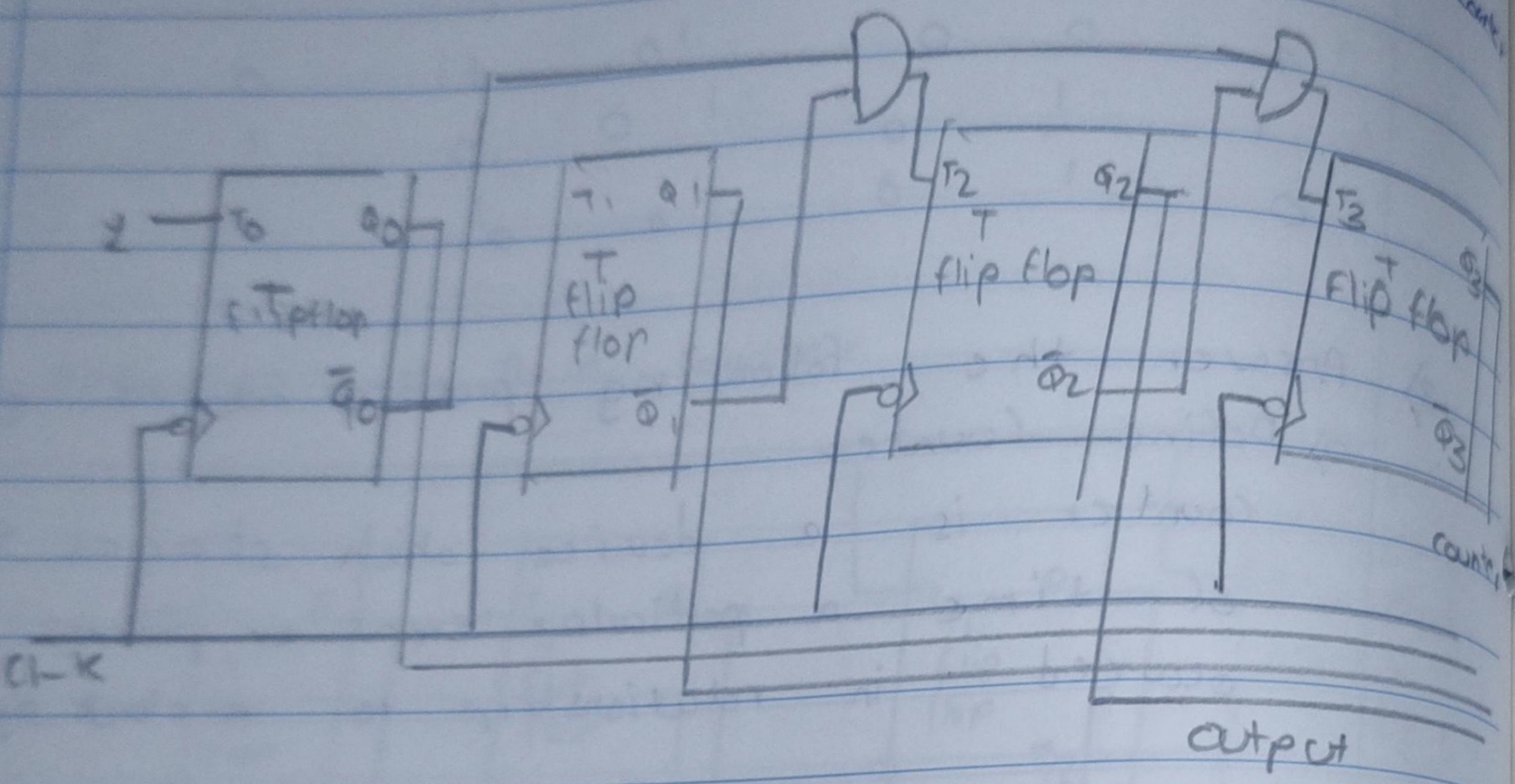
a) Define Counter

Counter is a device which stores the number of time a particular event or process has occured in relationship to a clock signal

b) State the difference between synchronous & Asynchronous counter

key	Synchronous counter	Asynchronous counter
Trigger	All flip flops are triggered with same clock simultaneously.	triggering of different flip flops with different clock
speed	faster than asynchronous counter	slower than synchronous counter
error prone	Less error prone	more error prone
Delay	There is no delay observed	There is subsequent delay observed

4) Draw logic diagram of 4 bit synchronous down counter



4 Conclusion

From the above expt we were able to verify the truth table of up/down counter