CHAPTER

3

Single-Stage Amplifiers

Amplification is an essential function in most analog (and many digital) circuits. We amplify an analog or digital signal because it may be too small to drive a load, overcome the noise of a subsequent stage, or provide logical levels to a digital circuit. Amplification also plays a critical role in feedback systems (Chapter 8).

In this chapter, we study the low-frequency behavior of single-stage CMOS amplifiers. Analyzing both the large-signal and the small-signal characteristics of each circuit, we develop intuitive techniques and models that prove useful in understanding more complex systems. An important part of a designer's job is to use proper approximations so as to create a simple mental picture of a complicated circuit. The intuition thus gained makes it possible to formulate the behavior of most circuits by inspection rather than by lengthy calculations.

Following a brief review of basic concepts, we describe in this chapter four types of amplifiers: common-source and common-gate topologies, source followers, and cascode configurations. In each case, we begin with a simple model and gradually add second-order phenomena such as channel-length modulation and body effect.

3.1 ■ Applications

Do you carry an amplifier? In all likelihood, yes. Your mobile phone, laptop, and digital camera all incorporate various types of amplifiers. The receiver in your phone must sense and amplify small signals received by the antenna, thus requiring a "low-noise" amplifier (LNA) at the front end (Fig. 3.1). As the signal travels down the receive chain, it must be further amplified by additional stages so as to reach an acceptably high level. This proves difficult because, in addition to the small desired signal, the antenna picks up other strong signals ("interferers") that are transmitted by various other users in the same vicinity. Your phone's transmitter, too, employs amplifiers: to amplify the signal generated by the microphone and, eventually, the signal delivered to the antenna. The "power amplifier" (PA) necessary for such delivery draws the most energy from the battery and still presents interesting challenges.

3.2 ■ General Considerations

An ideal amplifier generates an output, $y(t)$, that is a linear replica of the input, $x(t)$:

$$y(t) = \alpha_1 x(t) \tag{3.1}$$

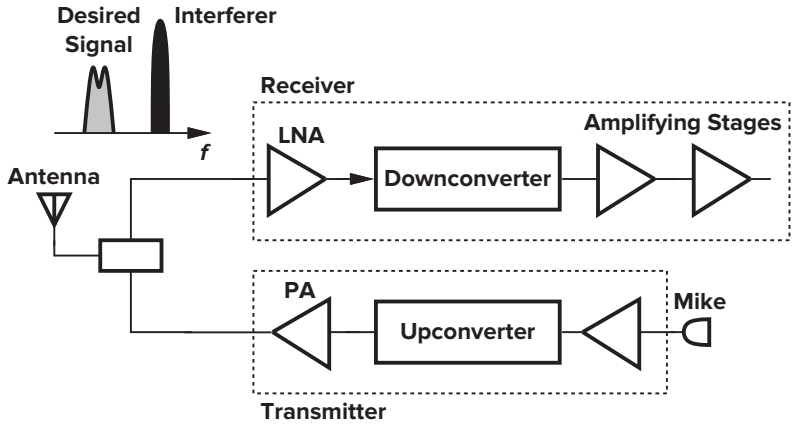


Figure 3.1 General RF transceiver.

where α_1 denotes the gain. Since the output signal is in fact superimposed on a bias (dc operating) point, α_0, we can write the overall output as $y(t) = \alpha_0 + \alpha_1 x(t)$. In this case, the input-output (large-signal) characteristic of the circuit is a straight line [Fig. 3.2(a)]. However, as the signal excursions become larger and the bias point of the transistor(s) is disturbed substantially, the gain (the slope of the characteristic) begins to *vary* [Fig. 3.2(b)]. We approximate this nonlinear characteristic by a polynomial:

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \cdots + \alpha_n x^n(t) \tag{3.2}$$

A nonlinear amplifier distorts the signal of interest or creates unwanted interactions among several signals that may coexist at the input. We return to the problem of nonlinearity in Chapter 14.

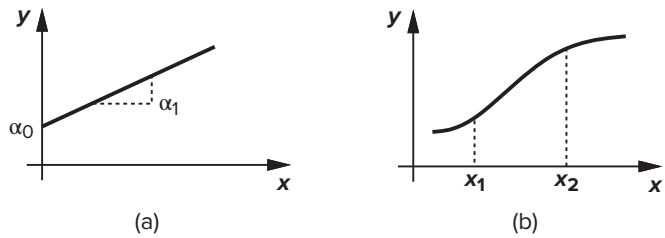


Figure 3.2 Input-output characteristic of a (a) linear and (b) nonlinear system.

What aspects of the performance of an amplifier are important? In addition to gain and speed, such parameters as power dissipation, supply voltage, linearity, noise, or maximum voltage swings may be important. Furthermore, the input and output impedances determine how the circuit interacts with the preceding and subsequent stages. In practice, most of these parameters trade with each other, making the design a multidimensional optimization problem. Illustrated in the "analog design octagon" of Fig. 3.3, such trade-offs present many challenges in the design of high-performance amplifiers, requiring intuition and experience to arrive at an acceptable compromise.

Table 3.1 gives a preview of the amplifier topologies studied in this chapter, indicating the much wider use of the common-source (CS) stage than other circuit configurations. For these amplifiers, we must (1) set up proper bias conditions so that each transistor provides the necessary transconductance and output resistance with certain quiescent currents and voltages, and (2) analyze the circuit's behavior as the input and output signals cause small or large departures from the bias input (small-signal and large-signal analyses, respectively). We deal with the latter task here and defer the former to Chapter 5.

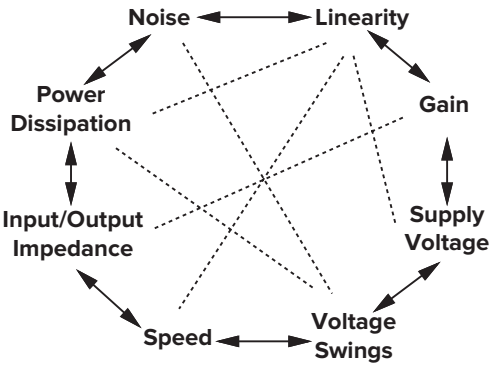


Figure 3.3 Analog design octagon.

Table 3.1 Amplifier categories.

Common-Source Stage	Source Follower	Common-Gate Stage	Cascode
With Resistive Load	With Resistive Bias	With Resistive Load	Telescopic
With Diode-Connected Load	With Current-Source Bias	With Current-Source Load	Folded
With Current-Source Load			
With Active Load			
With Source Degeneration			

3.3 ■ Common-Source Stage

3.3.1 Common-Source Stage with Resistive Load

By virtue of its transconductance, a MOSFET converts changes in its gate-source voltage to a small-signal drain current, which can pass through a resistor to generate an output voltage. Shown in Fig. 3.4(a), the common-source stage performs such an operation.[1] We study both the large-signal and the small-signal behavior of the circuit. Note that the input impedance of the circuit is very high at low frequencies.

If the input voltage increases from zero, M_1 is off and $V_{out} = V_{DD}$ [Fig. 3.4(b)]. As V_{in} approaches V_{TH}, M_1 begins to turn on, drawing current from R_D and lowering V_{out}. Transistor M_1 turns on in saturation regardless of the values of V_{DD} and R_D (why?), and we have

$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2 \tag{3.3}$$

where channel-length modulation is neglected. With further increase in V_{in}, V_{out} drops more, and the transistor continues to operate in saturation until V_{in} exceeds V_{out} by V_{TH} [point A in Fig. 3.4(b)]. At this point,

$$V_{in1} - V_{TH} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{TH})^2 \tag{3.4}$$

from which $V_{in1} - V_{TH}$ and hence V_{out} can be calculated.

For $V_{in} > V_{in1}$, M_1 is in the triode region:

$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2(V_{in} - V_{TH})V_{out} - V_{out}^2\right] \tag{3.5}$$

[1] The common-source topology is identified as receiving the input at the gate and producing the output at the drain.

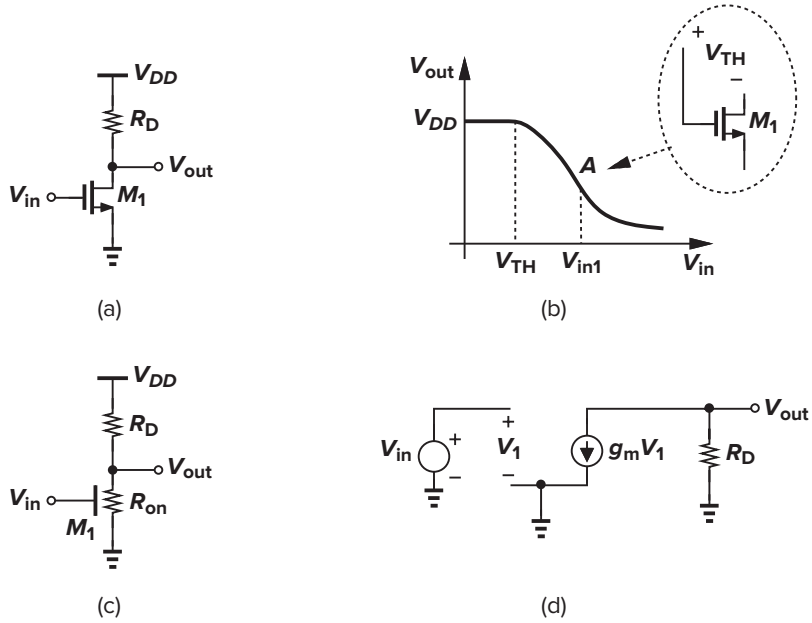


Figure 3.4 (a) Common-source stage, (b) input-output characteristic, (c) equivalent circuit in the deep triode region, and (d) small-signal model for the saturation region.

If V_{in} is high enough to drive M_1 into the deep triode region, $V_{out} \ll 2(V_{in} - V_{TH})$, and, from the equivalent circuit of Fig. 3.4(c),

$$V_{out} = V_{DD}\frac{R_{on}}{R_{on} + R_D} \tag{3.6}$$

$$= \frac{V_{DD}}{1 + \mu_n C_{ox}\dfrac{W}{L}R_D(V_{in} - V_{TH})} \tag{3.7}$$

Since the transconductance drops in the triode region, we usually ensure that $V_{out} > V_{in} - V_{TH}$, and hence the current operates to the left of point A in Fig. 3.4(b). Using (3.3) as the input-output characteristic and viewing its slope as the small-signal gain, we have

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} \tag{3.8}$$

$$= -R_D\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH}) \tag{3.9}$$

$$= -g_m R_D \tag{3.10}$$

This result can be directly derived from the observation that M_1 converts an input voltage change ΔV_{in} to a drain current change $g_m \Delta V_{in}$, and hence an output voltage change $-g_m R_D \Delta V_{in}$. The small-signal model of Fig. 3.4(d) yields the same result: $V_{out} = -g_m V_1 R_D = -g_m V_{in} R_D$. Note that, as mentioned in Chapter 2, V_{in}, V_1, and V_{out} in this figure denote small-signal quantities.

Even though derived for small-signal operation, the equation $A_v = -g_m R_D$ predicts certain effects if the circuit senses a *large* signal swing. Since g_m itself varies with the input signal according to

$g_m = \mu_n C_{ox}(W/L)(V_{GS} - V_{TH})$, the gain of the circuit changes substantially if the signal is large. In other words, if the gain of the circuit *varies* significantly with the signal swing, then the circuit operates in the large-signal mode. The dependence of the gain upon the signal level leads to nonlinearity (Chapter 14), usually an undesirable effect.

A key result here is that to minimize the nonlinearity, the gain equation must be a weak function of signal-dependent parameters such as g_m. We present several examples of this concept in this chapter and in Chapter 14.

▶ Example 3.1

Sketch the drain current and transconductance of M_1 in Fig. 3.4(a) as a function of the input voltage.

Solution

The drain current becomes significant for $V_{in} > V_{TH}$, eventually approaching V_{DD}/R_D if $R_{on1} \ll R_D$ [Fig. 3.5(a)]. Since in saturation, $g_m = \mu_n C_{ox}(W/L)(V_{in} - V_{TH})$, the transconductance begins to rise for $V_{in} > V_{TH}$. In the triode region, $g_m = \mu_n C_{ox}(W/L)V_{DS}$, falling as V_{in} exceeds V_{in1} [Fig. 3.5(b)]. Starting with Eq. (3.5), the reader can show that

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = \frac{-\mu_n C_{ox}(W/L)R_D V_{out}}{1 + \mu_n C_{ox}(W/L)R_D(V_{in} - V_{TH} - V_{out})} \tag{3.11}$$

which reaches a maximum if $V_{out} = V_{in} - V_{TH}$ (point A).

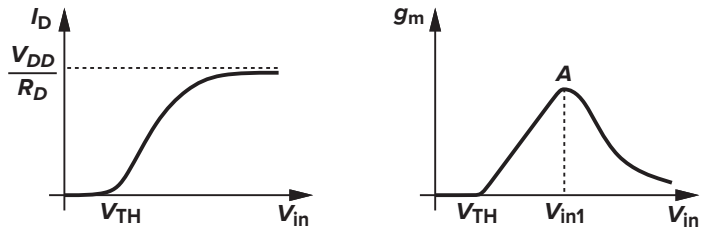
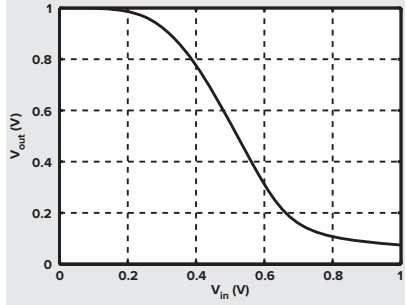


Figure 3.5

Nanometer Design Notes

How does the CS stage behave in nanometer technologies? The figure plots the simulated input-output characteristic for $W/L = 2\ \mu$m/40 nm, $R_D = 2\ \text{k}\Omega$, and $V_{DD} = 1$ V. We observe that the circuit provides a gain of about 3 in the input range of 0.4 V to 0.6 V. The output swing is limited to about 0.3 V–0.8 V for the gain not to drop significantly.



▶ Example 3.2

A CS stage is driven by a sinusoid, $V_{in} = V_1 \cos \omega_1 t + V_0$, where V_0 is the bias value and V_1 is large enough to drive the transistor into the off and triode regions. Sketch the g_m of the transistor as a function of time.

Solution

Let us first sketch the output voltage (Fig. 3.6), noting that when $V_{in} = V_1 + V_0$, V_{out} is low, M_1 is in the triode region, and g_m assumes a small value. As V_{in} falls and V_{out} and g_m rise, M_1 enters saturation at $t = t_1$ (when $V_{in} - V_{out} = V_{TH}$) and g_m reaches its maximum (why?). As V_{in} falls further, so do I_D and g_m. At $t = t_2$, g_m reaches zero.

We observe that (a) since the voltage gain is approximately equal to $-g_m R_D$, it experiences the same variation as the g_m, and (b) g_m varies periodically.[2]

[2]We even express g_m as a Fourier series in more advanced courses.

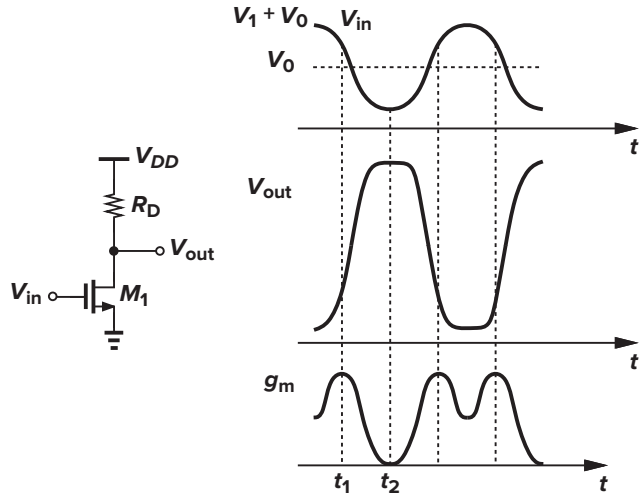


Figure 3.6

How do we maximize the voltage gain of a common-source stage? Writing (3.10) as

$$A_v = -\sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}\frac{V_{RD}}{I_D} \tag{3.12}$$

where V_{RD} denotes the voltage drop across R_D, we have

$$A_v = -\sqrt{2\mu_n C_{ox}\frac{W}{L}}\frac{V_{RD}}{\sqrt{I_D}} \tag{3.13}$$

Thus, the magnitude of A_v can be increased by increasing W/L or V_{RD} or decreasing I_D if other parameters are constant. It is important to understand the trade-offs resulting from this equation. A larger device size leads to greater device capacitances, and a higher V_{RD} limits the maximum voltage swings. For example, if $V_{DD} - V_{RD} = V_{in} - V_{TH}$, then M_1 is at the edge of the triode region, allowing only very small swings at the output (and input). If V_{RD} remains constant and I_D is reduced, then R_D must increase, thereby leading to a greater time constant at the output node. In other words, as noted in the analog design octagon, the circuit exhibits trade-offs between gain, bandwidth, and voltage swings. Lower supply voltages further tighten these trade-offs.

For large values of R_D, the effect of channel-length modulation in M_1 becomes significant. Modifying (3.3) to include this effect,

$$V_{out} = V_{DD} - R_D\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2(1 + \lambda V_{out}) \tag{3.14}$$

we have

$$\begin{aligned}\frac{\partial V_{out}}{\partial V_{in}} &= -R_D\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})(1 + \lambda V_{out}) \\ &\quad -R_D\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2\lambda\frac{\partial V_{out}}{\partial V_{in}}\end{aligned} \tag{3.15}$$

We recognize that $(1/2)\mu_n C_{ox}(W/L)(V_{in} - V_{TH})^2\lambda = 1/r_O$ and

$$A_v = -R_D g_m - \frac{R_D}{r_O} A_v \tag{3.16}$$

Thus,

$$A_v = -g_m \frac{r_O R_D}{r_O + R_D} \tag{3.17}$$

The small-signal model of Fig. 3.7 gives the same result with much less effort. That is, since $g_m V_1 (r_O \| R_D) = -V_{out}$ and $V_1 = V_{in}$, we have $V_{out}/V_{in} = -g_m(r_O \| R_D)$.

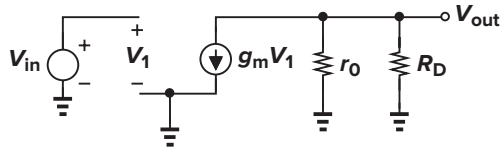


Figure 3.7 Small-signal model of CS stage including the transistor output resistance.

▶ Example 3.3

Assuming that M_1 in Fig. 3.8 is biased in saturation, calculate the small-signal voltage gain of the circuit.

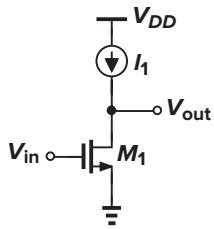


Figure 3.8

Solution

Since I_1 introduces an infinite impedance ($R_D = \infty$), the gain is limited by the output resistance of M_1:

$$A_v = -g_m r_O \tag{3.18}$$

Called the "intrinsic gain" of a transistor, this quantity represents the maximum voltage gain that can be achieved using a single device. In today's CMOS technology, $g_m r_O$ of short-channel devices is between roughly 5 and 10. We usually assume $1/g_m \ll r_O$.

In Fig. 3.8, Kirchhoff's current law (KCL) requires that $I_{D1} = I_1$. Then, how can V_{in} change the current of M_1 if I_1 is constant? Writing the total drain current of M_1 as

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2(1 + \lambda V_{out}) \tag{3.19}$$

$$= I_1 \tag{3.20}$$

we note that V_{in} appears in the square term and V_{out} in the linear term. As V_{in} increases, V_{out} must decrease such that the product remains constant. We may nevertheless say "I_{D1} increases as V_{in} increases." This statement simply refers to the quadratic part of the equation.

◀

An important conclusion here is that, to maximize the voltage gain, we must maximize the (small-signal) load impedance. Why can we not replace the load with an open circuit? This is because the circuit still needs a path from V_{DD} to ground for the bias current of M_1.

▶ **Example 3.4**

It is possible to use the bulk (back gate) of a MOSFET as the terminal controlling the channel. Shown in Fig. 3.9 is an example. Determine the voltage gain if $\lambda = 0$.

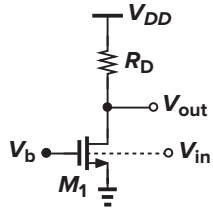


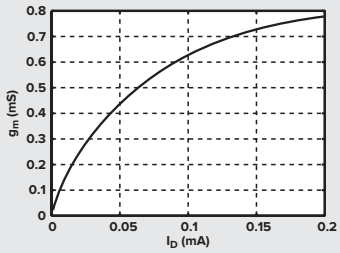
Figure 3.9

Solution

From the small-signal MOS model developed in Chapter 2, we recall that the drain current is given by $g_{mb}V_{in}$. Thus, $A_v = -g_{mb}R_D$. ◀

Nanometer Design Notes

How do we design a CS stage for a given gain and supply voltage? With W/L, I_D, and R_D under our control, we seem to have a wide design space. A good starting point is to choose a small device, $W/L = 0.5\ \mu$m/40 nm, a low bias current, $I_D = 50\ \mu$A, and a sufficiently large load resistance to achieve the required gain. To this end, we use simulations to plot the transconductance of such a device as a function of I_D, obtaining $g_m = 0.45$ mS. Thus, for a voltage gain of , say, 10, R_D must reach 22.2 kΩ if $\lambda = 0$. Is this an acceptable design? The answer depends on the application. In addition to gain, the circuit must also satisfy certain bandwidth, noise, and output swing requirements.

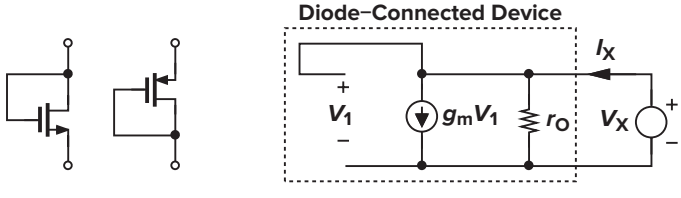


3.3.2 CS Stage with Diode-Connected Load

In some CMOS technologies, it is difficult to fabricate resistors with tightly-controlled values or a reasonable physical size (Chapter 19). Consequently, it is desirable to replace R_D in Fig. 3.4(a) with a MOS transistor.

A MOSFET can operate as a small-signal resistor if its gate and drain are shorted [Fig. 3.10(a)]. Called a "diode-connected" device in analogy with its bipolar counterpart, this configuration exhibits small-signal behavior similar to that of two-terminal resistor. Note that the transistor is always in saturation because the drain and the gate have the same potential. Using the small-signal equivalent shown in Fig. 3.10(b) to obtain the impedance of the device, we write $V_1 = V_X$ and $I_X = V_X/r_O + g_m V_X$. That is, the impedance of the diode is simply equal to $V_X/I_X = (1/g_m)\|r_O \approx 1/g_m$. If body effect exists, we can use the circuit in Fig. 3.11 to write $V_1 = -V_X$, $V_{bs} = -V_X$, and

$$(g_m + g_{mb})V_X + \frac{V_X}{r_O} = I_X \tag{3.21}$$



(a) (b)

Figure 3.10 (a) Diode-connected NMOS and PMOS devices; (b) small-signal equivalent circuit.

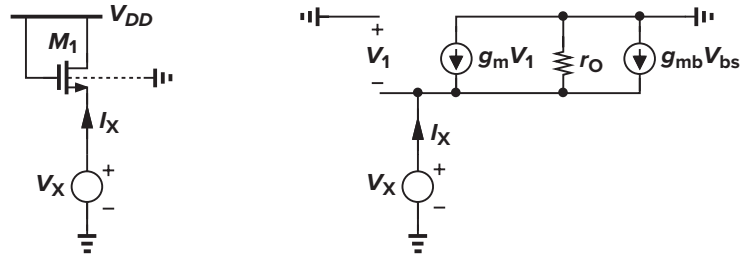


Figure 3.11 (a) Arrangement for measuring the equivalent resistance of a diode-connected MOSFET; (b) small-signal equivalent circuit.

It follows that

$$\frac{V_X}{I_X} = \frac{1}{g_m + g_{mb} + r_O^{-1}} \tag{3.22}$$

$$= \frac{1}{g_m + g_{mb}} \| r_O \tag{3.23}$$

$$\approx \frac{1}{g_m + g_{mb}} \tag{3.24}$$

In the general case, $V_X/I_X = (1/g_m)||r_O||(1/g_{mb})$. Interestingly, the impedance seen at the source of M_1 is *lower* when body effect is included. Intuitive explanation of this effect is left as an exercise for the reader.

From a large-signal point of view, a diode-connected device acts as a "square-root" operator if its current is considered the input and its V_{GS} or $V_{GS} - V_{TH}$ the output (why?). We return to this point later.

▶ Example 3.5

Consider the circuit shown in Fig. 3.12(a). In some cases, we are interested in the impedance seen looking into the source, R_X. Determine R_X if $\lambda = 0$.

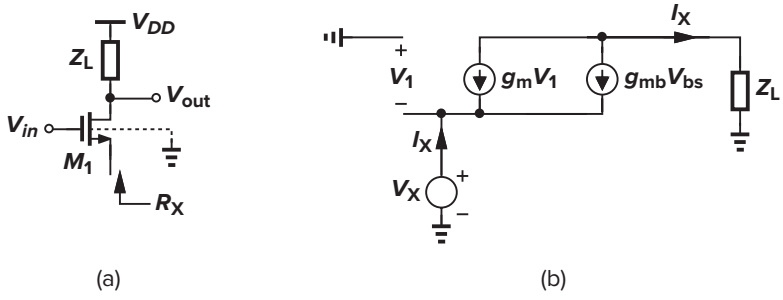


Figure 3.12 Impedance seen at the source with $\lambda = 0$.

Solution

To determine R_X, we set all independent sources to zero, draw the small-signal model, and apply a voltage source as shown in Fig. 3.12(b). Since $V_1 = -V_X$ and $V_{bs} = -V_X$, we have

$$(g_m + g_{mb})V_X = I_X \tag{3.25}$$

and

$$\frac{V_X}{I_X} = \frac{1}{g_m + g_{mb}} \tag{3.26}$$

This result should not be surprising: the topologies in Fig. 3.12(a) and Fig. 3.11(a) are similar except that the drain of M_1 in Fig. 3.12(b) is not at ac ground. This difference does not manifest itself if $\lambda = 0$. We sometimes say, "looking into the source of a MOSFET, we see $1/g_m$," assuming implicitly that $\lambda = \gamma = 0$.

◀

We now study a common-source stage with a diode-connected load (Fig. 3.13). With negligible channel-length modulation, (3.24) can be substituted in (3.10) for the load impedance, yielding

$$A_v = -g_{m1}\frac{1}{g_{m2} + g_{mb2}} \tag{3.27}$$

$$= -\frac{g_{m1}}{g_{m2}}\frac{1}{1+\eta} \tag{3.28}$$

where $\eta = g_{mb2}/g_{m2}$. Expressing g_{m1} and g_{m2} in terms of device dimensions and bias currents, we have

$$A_v = -\frac{\sqrt{2\mu_n C_{ox}(W/L)_1 I_{D1}}}{\sqrt{2\mu_n C_{ox}(W/L)_2 I_{D2}}}\frac{1}{1+\eta} \tag{3.29}$$

and, since $I_{D1} = I_{D2}$,

$$A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}\frac{1}{1+\eta} \tag{3.30}$$

This equation reveals an interesting property: if the variation of η with the output voltage is neglected, the gain is independent of the bias currents and voltages (so long as M_1 stays in saturation). In other words, as the input and output signal levels vary, the gain remains relatively constant, indicating that the input-output characteristic is relatively linear.

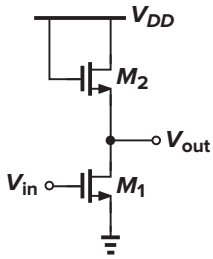


Figure 3.13 CS stage with diode-connected load.

The linear behavior of the circuit can also be confirmed by large-signal analysis. Neglecting channel-length modulation for simplicity, we have in Fig. 3.13

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{in} - V_{TH1})^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{DD} - V_{out} - V_{TH2})^2 \tag{3.31}$$

and hence

$$\sqrt{\left(\frac{W}{L}\right)_1}(V_{in} - V_{TH1}) = \sqrt{\left(\frac{W}{L}\right)_2}(V_{DD} - V_{out} - V_{TH2}) \tag{3.32}$$

Thus, if the variation of V_{TH2} with V_{out} is small, the circuit exhibits a linear input-output characteristic. In essence, the squaring function performed by M_1 (from the input voltage to its drain current) and the square root function performed by M_2 (from its drain current to its overdrive) act as $f^{-1}(f(x)) = x$.

The small-signal gain can also be computed by differentiating both sides with respect to V_{in}:

$$\sqrt{\left(\frac{W}{L}\right)_1} = \sqrt{\left(\frac{W}{L}\right)_2}\left(-\frac{\partial V_{out}}{\partial V_{in}} - \frac{\partial V_{TH2}}{\partial V_{in}}\right) \tag{3.33}$$

which, upon application of the chain rule $\partial V_{TH2}/\partial V_{in} = (\partial V_{TH2}/\partial V_{out})(\partial V_{out}/\partial V_{in}) = \eta(\partial V_{out}/\partial V_{in})$, reduces to

$$\frac{\partial V_{out}}{\partial V_{in}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}\frac{1}{1+\eta} \tag{3.34}$$

It is instructive to study the overall large-signal characteristic of the circuit as well. But let us first consider the circuit shown in Fig. 3.14(a). What is the final value of V_{out} if I_1 drops to zero? As I_1 decreases, so does the overdrive of M_2. Thus, for small I_1, $V_{GS2} \approx V_{TH2}$ and $V_{out} \approx V_{DD} - V_{TH2}$. In reality, the subthreshold conduction in M_2 eventually brings V_{out} to V_{DD} if I_D approaches zero, but at very low current levels, the finite capacitance at the output node slows down the change from $V_{DD} - V_{TH2}$ to V_{DD}. This is illustrated in the time-domain waveforms of Fig. 3.14(b). For this reason, in circuits that have frequent switching activity, we assume that V_{out} remains around $V_{DD} - V_{TH2}$ when I_1 falls to small values.

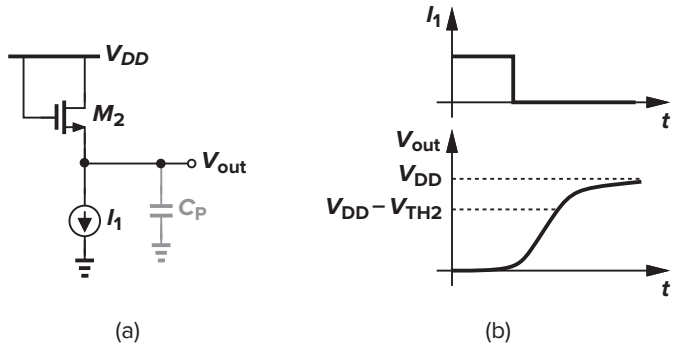


Figure 3.14 (a) Diode-connected device with stepped bias current; (b) variation of source voltage versus time.

Now we return to the circuit of Fig. 3.13. Plotted in Fig. 3.15 versus V_{in}, the output voltage equals $V_{DD} - V_{TH2}$ if $V_{in} < V_{TH1}$. For $V_{in} > V_{TH1}$, Eq. (3.32) holds and V_{out} follows an approximately straight line. As V_{in} exceeds $V_{out} + V_{TH1}$ (beyond point A), M_1 enters the triode region, and the characteristic becomes nonlinear.

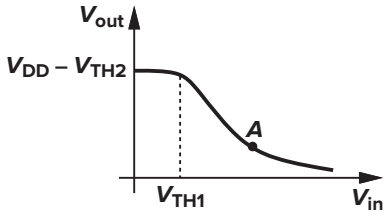


Figure 3.15 Input-output characteristic of a CS stage with diode-connected load.

The diode-connected load of Fig. 3.13 can be implemented with a PMOS device as well. Shown in Fig. 3.16, the circuit is free from body effect, providing a small-signal voltage gain equal to

$$A_v = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}} \tag{3.35}$$

where channel-length modulation is neglected.

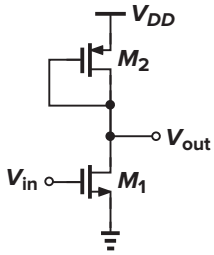


Figure 3.16 CS stage with diode-connected PMOS device.

Equations (3.30) and (3.35) indicate that the gain of a common-source stage with diode-connected load is a relatively weak function of the device dimensions. For example, to achieve a gain of 5, $\mu_n(W/L)_1/[\mu_p(W/L)_2] = 25$, implying that, with $\mu_n \approx 2\mu_p$, we must have $(W/L)_1 \approx 12.5(W/L)_2$. In a sense, a high gain requires a "strong" input device and a "weak" load device. In addition to disproportionately wide or long transistors (and hence a large input or load capacitance), a high gain translates to another important limitation: reduction in allowable voltage swings. Specifically, since in Fig. 3.16, $I_{D1} = |I_{D2}|$,

$$\mu_n \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2 = \mu_p \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2 \tag{3.36}$$

if $\lambda = 0$, revealing that

$$\frac{|V_{GS2} - V_{TH2}|}{V_{GS1} - V_{TH1}} = A_v \tag{3.37}$$

In the above example, the overdrive voltage of M_2 must be 5 times that of M_1. For example, with $V_{GS1} - V_{TH1} = 100$ mV and $|V_{TH2}| = 0.3$ V, we have $|V_{GS2}| = 0.8$ V, severely limiting the output swing. This is another example of the trade-offs suggested by the analog design octagon. Note that, with diode-connected loads, the swing is constrained by both the required overdrive voltage and the threshold voltage. That is, even with a small overdrive, the output level cannot exceed $V_{DD} - |V_{TH}|$.

An interesting paradox arises here if we write $g_m = \mu C_{ox}(W/L)|V_{GS} - V_{TH}|$. The voltage gain of the circuit is then given by

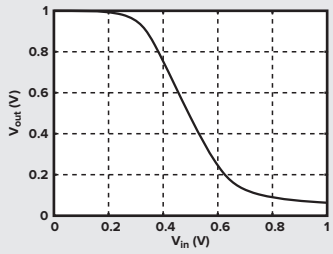
$$|A_v| = \frac{g_{m1}}{g_{m2}} \tag{3.38}$$

$$= \frac{\mu_n C_{ox}(W/L)_1 (V_{GS1} - V_{TH1})}{\mu_p C_{ox}(W/L)_2 |V_{GS2} - V_{TH2}|} \tag{3.39}$$

Equation (3.39) implies that A_v is *inversely* proportional to $|V_{GS2} - V_{TH2}|$. It is left for the reader to resolve the seemingly opposite trends suggested by (3.37) and (3.39).

Nanometer Design Notes

Let us design and simulate a CS stage with a diode-connected PMOS load in 40-nm technology. We select W/L = 5 μm/40 nm for the NMOS device and 1 μm/40 nm for the PMOS device. The large-signal I-V characteristic is shown in the figure. We observe that the circuit provides a small-signal gain of about 1.5 for an input range of roughly 0.4 V to 0.5 V. (In this dc sweep, V_{out} can reach V_{DD} when the input transistor is off.)



▶ Example 3.6

In the circuit of Fig. 3.17, M_1 is biased in saturation with a drain current equal to I_1. The current source $I_S = 0.75I_1$ is added to the circuit. How is (3.37) modified for this case? Assume $\lambda = 0$.

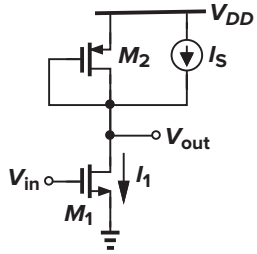


Figure 3.17

Solution

Since $|I_{D2}| = I_1/4$, we have

$$A_v = -\frac{g_{m1}}{g_{m2}} \tag{3.40}$$

$$= -\sqrt{\frac{4\mu_n(W/L)_1}{\mu_p(W/L)_2}} \tag{3.41}$$

Moreover,

$$\mu_n \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2 = 4\mu_p \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2 \tag{3.42}$$

yielding

$$\frac{|V_{GS2} - V_{TH2}|}{V_{GS1} - V_{TH1}} = \frac{A_v}{4} \tag{3.43}$$

Thus, for a gain of 5, the overdrive of M_2 need be only 1.25 times that of M_1. Alternatively, for a given overdrive voltage, this circuit achieves a gain four times that of the stage in Fig. 3.16. Intuitively, this is because for a given $|V_{GS2} - V_{TH2}|$, if the current decreases by a factor of 4, then $(W/L)_2$ must decrease proportionally, and $g_{m2} = \sqrt{2\mu_p C_{ox}(W/L)_2 I_{D2}}$ is lowered by the same factor. ◀

▶ Example 3.7

A student attempts to calculate the voltage gain in the previous example by differentiating both sides of (3.42). Does this approach give a correct result? Why?

Solution

Since $V_{GS2} = V_{out} - V_{DD}$, differentiation and multiplication by C_{ox} yield

$$\mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{in} - V_{TH1})^2 = 4\mu_p C_{ox} \left(\frac{W}{L}\right)_2 (V_{out} - V_{DD} - V_{TH2}) \frac{\partial V_{out}}{\partial V_{in}} \tag{3.44}$$

It follows that $\partial V_{out}/\partial V_{in} = -g_{m1}/(4g_{m2})$. This incorrect result arises because (3.42) is valid for only *one* value of V_{in}. As V_{in} is perturbed by the signal, I_1 departs from $4|I_{D2}|$ and (3.42) cannot be differentiated. ◀

In today's CMOS technology, channel-length modulation is quite significant and, more important, the behavior of transistors notably departs from the square law. Thus, the gain of the stage in Fig. 3.13 must be expressed as

$$A_v = -g_{m1}\left(\frac{1}{g_{m2}} \| r_{O1} \| r_{O2}\right) \tag{3.45}$$

where g_{m1} and g_{m2} must be obtained as described in Chapter 17.

3.3.3 CS Stage with Current-Source Load

In applications requiring a large voltage gain in a single stage, the relationship $A_v = -g_m R_D$ suggests that we should increase the load impedance of the CS stage. With a resistor or diode-connected load, however, increasing the load resistance translates to a large dc drop across the load, thereby limiting the output voltage swing.

A more practical approach is to replace the load with a device that does not obey Ohm's law, e.g., a current source. Described briefly in Example 3.3, the resulting circuit is shown in Fig. 3.18, where both transistors operate in saturation. Since the total impedance seen at the output node is equal to $r_{O1} \| r_{O2}$, the gain is given by is

$$A_v = -g_{m1}(r_{O1} \| r_{O2}) \tag{3.46}$$

The key point here is that the output impedance and the minimum required $|V_{DS}|$ of M_2 are less strongly coupled than the value and voltage drop of a resistor; the former need not satisfy Ohm's law, but the latter must. The voltage $|V_{DS2,min}| = |V_{GS2} - V_{TH2}|$ can be reduced to less than a hundred millivolts by simply increasing the width of M_2. If r_{O2} is not sufficiently high, the length and width of M_2 can be increased to achieve a smaller λ while maintaining the same overdrive voltage. The penalty is the larger capacitance introduced by M_2 at the output node.

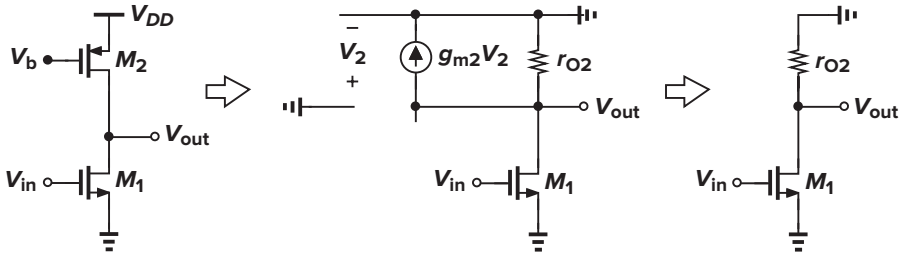


Figure 3.18 CS stage with current-source load.

We should remark that the output bias voltage of the circuit in Fig. 3.18 is not well-defined. Thus, the stage is reliably biased only if a feedback loop forces V_{out} to a known value (Chapter 8). The large-signal analysis of the circuit is left as an exercise for the reader.

As explained in Chapter 2, the output impedance of MOSFETs at a given drain current can be scaled by changing the channel length, i.e., to the first order, $\lambda \propto 1/L$, and hence $r_O \propto L/I_D$. Since the gain of the stage shown in Fig. 3.18 is proportional to $r_{O1} \| r_{O2}$, we may surmise that longer transistors yield a higher voltage gain.

Let us consider M_1 and M_2 separately. If L_1 is scaled up by a factor of α (> 1), then W_1 may need to be scaled proportionally as well. This is because, for a given drain current, $V_{GS1} - V_{TH1} \propto 1/\sqrt{(W/L)_1}$, i.e., if W_1 is not scaled, the overdrive voltage increases, limiting the output voltage swing. Also, since $g_{m1} \propto \sqrt{(W/L)_1}$, scaling up only L_1 lowers g_{m1}.

In applications where these issues are unimportant, W_1 can remain constant while L_1 increases. Thus, the intrinsic gain of M_1 can be written as

$$g_{m1}r_{O1} = \sqrt{2\left(\frac{W}{L}\right)_1 \mu_n C_{ox} I_D}\frac{1}{\lambda I_D} \tag{3.47}$$

indicating that the gain *increases* with L because λ depends more strongly on L than g_m does. Also, note that $g_m r_O$ *decreases* as I_D increases.

Increasing L_2 while keeping W_2 constant increases r_{O2} and hence the voltage gain, but at the cost of a higher $|V_{DS2,min}|$, which is required to maintain M_2 in saturation.

▶ **Example 3.8**

Compare the maximum output voltage swings of CS stages with resistive and current-source loads.

Solution

For the resistively-loaded stage [Fig. 3.19(a)], the maximum output voltage is near V_{DD} (when V_{in} falls to about V_{TH1}). The minimum is the value that places M_1 at the edge of the triode region, $V_{in} - V_{TH1}$.

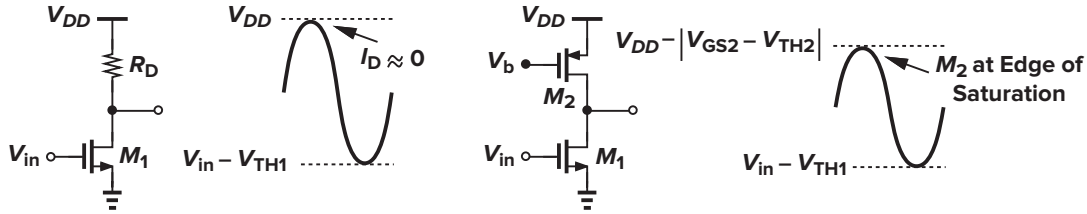


Figure 3.19 Output swing in CS stage with (a) resistive load and (b) current-source load.

For the stage with a current-source load [Fig. 3.19(b)], the maximum output voltage is that which places M_2 at the edge of the triode region, $V_{DD} - |V_{GS2} - V_{TH2}|$. Thus, the latter actually provides *smaller* swings than the former, but can always achieve a *higher* gain if L_1 and L_2 are increased. ◀

3.3.4 CS Stage with Active Load

In the amplifier topology of Fig. 3.19(b), the PMOS device serves as a constant current source. Is it possible for M_2 to operate as an *amplifying* device? Yes; we can apply the input signal to the gate of M_2 as well [Fig. 3.20(a)], converting it to an "active" load. The reader may recognize this topology as a CMOS inverter. Suppose both transistors are in saturation and V_{in} rises by ΔV_0. Two changes now occur: (a) I_{D1} increases, pulling V_{out} lower, and (b) M_2 injects less current into the output node, allowing V_{out} to drop. The two changes thus *enhance* each other, leading to a greater voltage gain. Equivalently, as seen in Fig. 3.20(b), the two transistors operate in parallel and collapse into one as illustrated in Fig. 3.20(c). It follows that $-(g_{m1} + g_{m2})V_{in}(r_{O1}||r_{O2}) = V_{out}$, and hence

$$A_v = -(g_{m1} + g_{m2})(r_{O1}||r_{O2}) \tag{3.48}$$

Compared to the amplifier of Fig. 3.19(b), this circuit exhibits the same output resistance, $r_{O1}||r_{O2}$, but a higher transconductance. This topology is also called a "complementary CS stage."

The amplifier of Fig. 3.20(a) must deal with two critical issues. First, the bias current of the two transistors is a strong function of PVT. In particular, since $V_{GS1} + |V_{GS2}| = V_{DD}$, variations in V_{DD} or the threshold voltages directly translate to changes in the drain currents. Second, the circuit *amplifies*

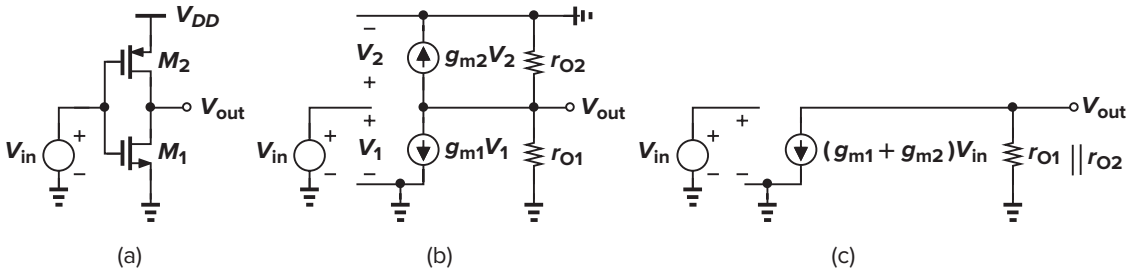


Figure 3.20 (a) CS stage with active load, (b) small-signal model, and (c) simplified model.

supply voltage variations ("supply noise")! To understand this point, consider the arrangement depicted in Fig. 3.21, where V_B is a bias voltage to place M_1 and M_2 in saturation. In Problem 3.31, we prove that the small-signal gain from V_{DD} to V_{out} is given by

$$\frac{V_{out}}{V_{DD}} = \frac{g_{m2}r_{O2}+1}{r_{O2}+r_{O1}} r_{O1} \tag{3.49}$$

$$= \left(g_{m2} + \frac{1}{r_{O2}}\right)(r_{O1}||r_{O2}) \tag{3.50}$$

about half of the A_v found above. These issues are addressed in Chapter 5.

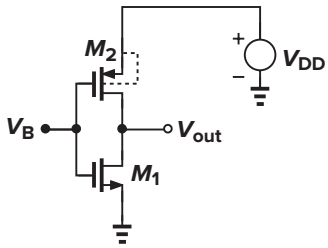
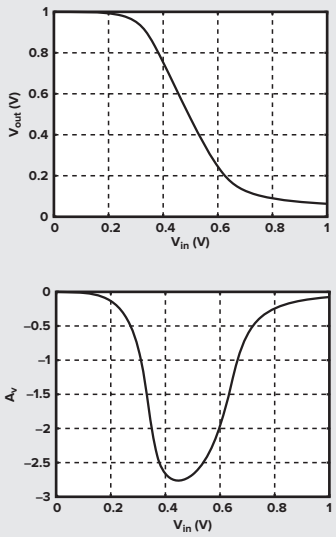


Figure 3.21 Arrangement for studying supply sensitivity of CS stage with active load.

Nanometer Design Notes

With minimum channel lengths, the CS stage with current-source load provides a low gain. For example, if $(W/L)_{NMOS} = 5\ \mu$m/40 nm and $(W/L)_{PMOS} = 10\ \mu$m/40 nm, we obtain the input-output characteristic shown in the figure, where the maximum gain is about 2.5! If we plot the slope, we also see the useful output voltage range to be about 0.7 V with $V_{DD} = 1$ V. Outside this range, the gain drops considerably.



3.3.5 CS Stage with Triode Load

A MOS device operating in the deep triode region behaves as a resistor and can therefore serve as the load in a CS stage. Illustrated in Fig. 3.22, such a circuit biases the gate of M_2 at a sufficiently low level, ensuring that the load is in the deep triode region for all output voltage swings. Since

$$R_{on2} = \frac{1}{\mu_p C_{ox}(W/L)_2(V_{DD} - V_b - |V_{THP}|)} \tag{3.51}$$

the voltage gain can be readily calculated.

The principal drawback of this circuit stems from the dependence of R_{on2} upon $\mu_p C_{ox}$, V_b, and V_{THP}. Since $\mu_p C_{ox}$ and V_{THP} vary with process and temperature, and since generating a precise value for V_b requires additional complexity, this circuit is difficult to use. Triode loads, however, consume less voltage headroom than do diode-connected devices because in Fig. 3.22, $V_{out,max} = V_{DD}$, whereas in Fig. 3.16, $V_{out,max} \approx V_{DD} - |V_{THP}|$.

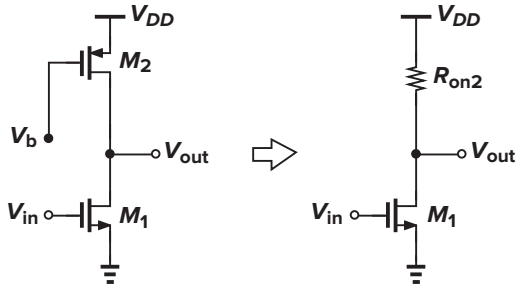


Figure 3.22 CS stage with triode load.

Among the five CS variants studied above, those employing resistive, current-source, or active loads find wider usage than the other two.

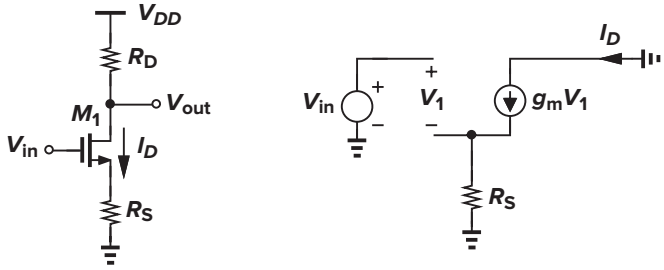


Figure 3.23 CS stage with source degeneration.

3.3.6 CS Stage with Source Degeneration

In some applications, the nonlinear dependence of the drain current upon the overdrive voltage introduces excessive nonlinearity, making it desirable to "soften" the device characteristics. In Sec. 3.3.2, we noted the linear behavior of a CS stage using a diode-connected load, which allows "postcorrection" of the nonlinearity. Alternatively, as depicted in Fig. 3.23(a), this can be accomplished by placing a "degeneration" resistor in series with the source terminal so as to make the input device more linear. Let us neglect channel-length modulation and body effect. Here, as V_{in} increases, so do I_D and the voltage drop across R_S. That is, a fraction of the change in V_{in} appears across the resistor rather than as the gate-source overdrive, thus leading to a smoother variation of I_D. From another perspective, we intend to make the gain equation a weaker function of g_m. Since $V_{out} = V_{DD} - I_D R_D$, the nonlinearity of the circuit arises from the nonlinear dependence of I_D upon V_{in}. We note that $\partial V_{out}/\partial V_{in} = -(\partial I_D/\partial V_{in})R_D$, and define the equivalent transconductance of the circuit as $G_m = \partial I_D/\partial V_{in}$.[3] Now, assuming that $I_D = f(V_{GS})$, we write

$$G_m = \frac{\partial I_D}{\partial V_{in}} \tag{3.52}$$

$$= \frac{\partial f}{\partial V_{GS}} \frac{\partial V_{GS}}{\partial V_{in}} \tag{3.53}$$

[3] As explained later, the output voltage must be kept constant when G_m is calculated.

Since $V_{GS} = V_{in} - I_D R_S$, we have $\partial V_{GS}/\partial V_{in} = 1 - R_S \partial I_D/\partial V_{in}$, obtaining

$$G_m = \left(1 - R_S \frac{\partial I_D}{\partial V_{in}}\right) \frac{\partial f}{\partial V_{GS}} \tag{3.54}$$

But, $\partial f/\partial V_{GS}$ is the transconductance of M_1, and

$$G_m = \frac{g_m}{1 + g_m R_S} \tag{3.55}$$

The small-signal voltage gain is thus equal to

$$A_v = -G_m R_D \tag{3.56}$$

$$= \frac{-g_m R_D}{1 + g_m R_S} \tag{3.57}$$

The same result can be derived using the small-signal model of Fig. 3.23(b) by writing a KVL, $V_{in} = V_1 + I_D R_S$, and noting that $I_D = g_m V_1$. Equation (3.55) implies that as R_S increases, G_m becomes a weaker function of g_m and hence the drain current. In fact, for $R_S \gg 1/g_m$, we have $G_m \approx 1/R_S$, i.e., $\Delta I_D \approx \Delta V_{in}/R_S$, concluding that most of the change in V_{in} appears across R_S. We say that the drain current is a "linearized" function of the input voltage. In Problem 3.30, we examine this effect from a different perspective. The linearization is obtained at the cost of lower gain [and higher noise (Chapter 7)].

For our subsequent calculations, it is useful to determine G_m in the presence of body effect and channel-length modulation. With the aid of the equivalent circuit shown in Fig. 3.24, we recognize that the current through R_S equals I_{out} and, therefore, $V_{in} = V_1 + I_{out} R_S$. Summing the currents at node X, we have

$$I_{out} = g_m V_1 - g_{mb} V_X - \frac{I_{out} R_S}{r_O} \tag{3.58}$$

$$= g_m (V_{in} - I_{out} R_S) + g_{mb}(-I_{out} R_S) - \frac{I_{out} R_S}{r_O} \tag{3.59}$$

It follows that

$$G_m = \frac{I_{out}}{V_{in}} \tag{3.60}$$

$$= \frac{g_m r_O}{R_S + [1 + (g_m + g_{mb}) R_S] r_O} \tag{3.61}$$

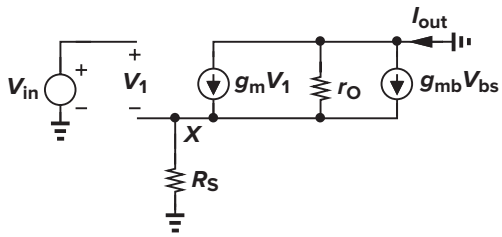


Figure 3.24 Small-signal equivalent circuit of a degenerated CS stage.

Let us now examine the large-signal behavior of the CS stage with $R_S = 0$ and $R_S \neq 0$. For $R_S = 0$, our derivations in Chapter 2 indicate that I_D and g_m vary as shown in Fig. 3.25(a). For $R_S \neq 0$, the turn-on behavior is similar to that in Fig. 3.25(a) because, at low current levels, $1/g_m \gg R_S$, and hence $G_m \approx g_m$ [Fig. 3.25(b)]. As the overdrive and therefore g_m increase, the effect of degeneration, $1 + g_m R_S$ in (3.55), becomes more significant. For large values of V_{in} (if M_1 is still saturated), I_D is approximately a linear function of V_{in} and G_m approaches $1/R_S$.

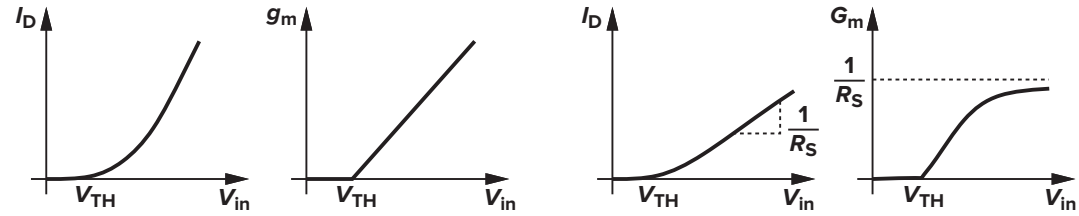


Figure 3.25 Drain current and transconductance of a CS device (a) without and (b) with source degeneration.

▶ Example 3.9

Plot the small-signal voltage gain of the circuit in Fig. 3.23 as a function of the input bias voltage, V_{in}.

Solution

Using the results derived above for the equivalent transconductance of M_1 and R_S, we arrive at the plot shown in Fig. 3.26. For V_{in} slightly greater than V_{TH}, $1/g_m \gg R_S$ and $A_v \approx -g_m R_D$. As V_{in} increases, degeneration becomes more significant and $A_v = -g_m R_D/(1+g_m R_S)$. For large values of V_{in}, $G_m \approx 1/R_S$ and $A_v = -R_D/R_S$. However, if $V_{in} > V_{out} + V_{TH}$, that is, if $R_D I_D > V_{TH} + V_{DD} - V_{in}$, M_1 enters the triode region and A_v drops.

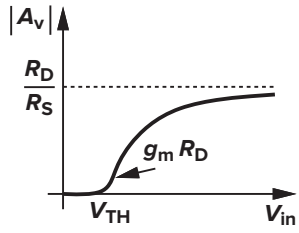


Figure 3.26

◀

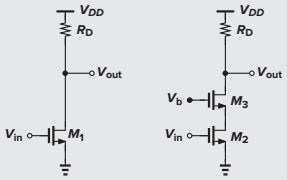
Equation (3.57) can be rewritten as

$$A_v = -\frac{R_D}{\dfrac{1}{g_m} + R_S} \tag{3.62}$$

This result allows formulating the gain by inspection. First, let us examine the denominator of (3.62). The expression is equal to the *series* combination of the inverse transconductance of the device and the explicit resistance seen from the source to ground. We call the denominator "the resistance seen in the source path" because if, as shown in Fig. 3.27, we disconnect the bottom terminal of R_S from ground and calculate the resistance seen "looking up" (while setting the input to zero), we obtain $R_S + 1/g_m$.

Nanometer Design Notes

A common issue in nanometer technologies is that a MOS transistor experiences "stress" if its V_{GS}, V_{DS}, or V_{DG} exceeds certain limits. For example, in 40-nm technology, these voltages should remain below 1 V. Interestingly, the cascode structure can avoid device stress even if V_{DD} is greater than allowed. As can be seen from the diagram below, as the drain current decreases and V_{out} approaches V_{DD}, M_1 experiences $V_{DS} = V_{DD}$, whereas M_2 sees $V_{DS} \approx V_b - V_{TH2}$. Similarly, $V_{DS3} < V_{DD}$ (why?).



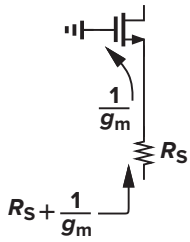


Figure 3.27 Resistance seen in the source path.

Noting that the numerator of (3.62) is the resistance seen at the drain, we view the magnitude of the gain as the resistance seen at the drain node divided by the total resistance in the source path. This method greatly simplifies the analysis of more complex circuits.

▶ Example 3.10

Assuming $\lambda = \gamma = 0$, calculate the small-signal gain of the circuit shown in Fig. 3.28(a).

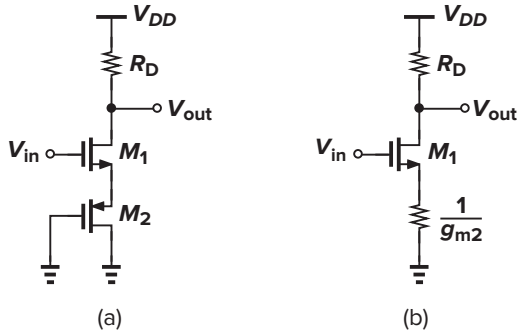


Figure 3.28

Solution

Noting that M_2 is a diode-connected device and simplifying the circuit to that shown in Fig. 3.28(b), we use the above rule to write

$$A_v = -\frac{R_D}{\dfrac{1}{g_{m1}} + \dfrac{1}{g_{m2}}} \tag{3.63}$$

◀

Output Resistance Another important consequence of source degeneration is the increase in the output resistance of the stage. We calculate the output resistance first with the aid of the equivalent circuit shown in Fig. 3.29, where the load resistor, R_D, is excluded for now. Note that body effect is also included to

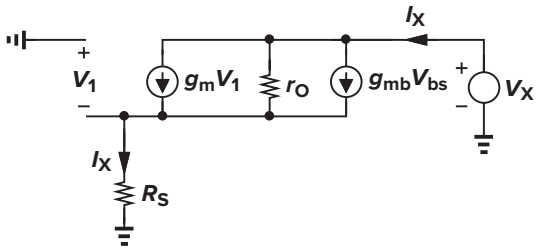


Figure 3.29 Equivalent circuit for calculating the output resistance of a degenerated CS stage.

arrive at a general result. Since the current through R_S is equal to I_X, $V_1 = -I_X R_S$, and the current flowing through r_O is given by $I_X - (g_m + g_{mb})V_1 = I_X + (g_m + g_{mb})R_S I_X$. Adding the voltage drops across r_O and R_S, we obtain

$$r_O[I_X + (g_m + g_{mb})R_S I_X] + I_X R_S = V_X \tag{3.64}$$

It follows that

$$R_{out} = [1 + (g_m + g_{mb})R_S]r_O + R_S \tag{3.65}$$

$$= [1 + (g_m + g_{mb})r_O]R_S + r_O \tag{3.66}$$

Equation (3.65) indicates that r_O is "boosted" by a factor of $1 + (g_m + g_{mb})R_S$ and then added to R_S. As an alternative perspective, Eq. (3.66) suggests that R_S is boosted by a factor of $1 + (g_m + g_{mb})r_O$ (a value close to the transistor's intrinsic gain) and then added to r_O. Both views prove useful in analyzing circuits. Note that the overall output resistance is equal to the parallel combination of R_{out} and R_D. If $(g_m + g_{mb})r_O \gg 1$, we have

$$R_{out} \approx (g_m + g_{mb})r_O R_S + r_O \tag{3.67}$$

$$= [1 + (g_m + g_{mb})R_S]r_O \tag{3.68}$$

To gain more insight, let us consider the circuit of Fig. 3.29 with $R_S = 0$ and $R_S > 0$. If $R_S = 0$, then $g_m V_1 = g_{mb} V_{bs} = 0$ and $I_X = V_X / r_O$. On the other hand, if $R_S > 0$, we have $I_X R_S > 0$ and $V_1 < 0$, obtaining *negative* $g_m V_1$ and $g_{mb} V_{bs}$. Thus, the current supplied by V_X is *less* than V_X / r_O, and hence the output impedance is greater than r_O.

The relationship in (3.65) can also be derived by inspection. As shown in Fig. 3.30(a), we apply a voltage to the output node, change its value by ΔV, and measure the resulting change, ΔI, in the output current. Since the current through R_S must change by ΔI (why?), we first compute the voltage change across R_S. To this end, we draw the circuit as shown in Fig. 3.30(b) and note that the resistance seen looking into the source of M_1 is equal to $1/(g_m + g_{mb})$ [Eq. (3.24)], thus arriving at the equivalent circuit in Fig. 3.30(c). The voltage change across R_S is therefore equal to

$$\Delta V_{RS} = \Delta V \frac{\dfrac{1}{g_m + g_{mb}} \| R_S}{\dfrac{1}{g_m + g_{mb}} \| R_S + r_O} \tag{3.69}$$

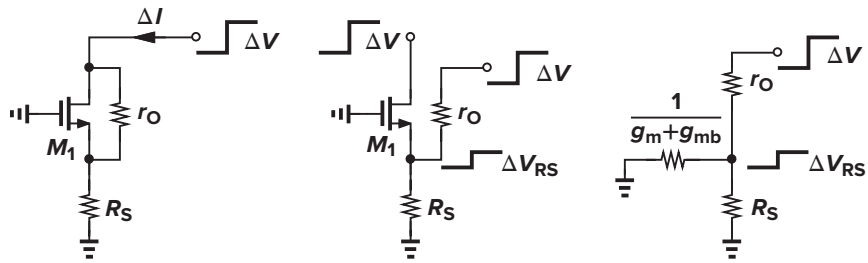


Figure 3.30 (a) Change in drain current in response to change in applied voltage to drain; (b) equivalent of (a); (c) small-signal model.

The change in the current is

$$\Delta I = \frac{\Delta V_{RS}}{R_S} \tag{3.70}$$

$$= \Delta V \frac{1}{[1 + (g_m + g_{mb})]R_S r_O + R_S} \tag{3.71}$$

that is,

$$\frac{\Delta V}{\Delta I} = [1 + (g_m + g_{mb})R_S]r_O + R_S \tag{3.72}$$

With the foregoing developments, we can now compute the gain of a degenerated CS stage in the general case, taking into account both body effect and channel-length modulation. In the equivalent circuit depicted in Fig. 3.31, the current through R_S must equal that through R_D, i.e., $-V_{out}/R_D$. Thus, the source voltage with respect to ground (and the bulk) is equal to $-V_{out}R_S/R_D$, yielding $V_1 = V_{in} + V_{out}R_S/R_D$. The current flowing through r_O from top to bottom can therefore be written as

$$I_{ro} = -\frac{V_{out}}{R_D} - (g_m V_1 + g_{mb} V_{bs}) \tag{3.73}$$

$$= -\frac{V_{out}}{R_D} - \left[g_m \left(V_{in} + V_{out} \frac{R_S}{R_D} \right) + g_{mb} V_{out} \frac{R_S}{R_D} \right] \tag{3.74}$$

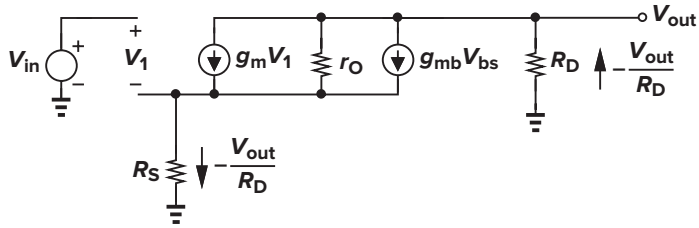


Figure 3.31 Small-signal model of degenerated CS stage with finite output resistance.

Since the voltage drops across r_O and R_S must add up to V_{out}, we have

$$V_{out} = I_{ro} r_O - \frac{V_{out}}{R_D} R_S \tag{3.75}$$

$$= -\frac{V_{out}}{R_D} r_O - \left[g_m \left(V_{in} + V_{out} \frac{R_S}{R_D} \right) + g_{mb} V_{out} \frac{R_S}{R_D} \right] r_O - V_{out} \frac{R_S}{R_D} \tag{3.76}$$

It follows that

$$\frac{V_{out}}{V_{in}} = \frac{-g_m r_O R_D}{R_D + R_S + r_O + (g_m + g_{mb})R_S r_O} \tag{3.77}$$

To gain more insight into this result, we recognize that the last three terms in the denominator, namely, $R_S + r_O + (g_m + g_{mb})R_S r_O$, represent the output resistance of a MOS device degenerated by a resistor R_S, as originally derived in (3.66). Let us now rewrite (3.77) as

$$A_v = \frac{-g_m r_O R_D [R_S + r_O + (g_m + g_{mb})R_S r_O]}{R_D + R_S + r_O + (g_m + g_{mb})R_S r_O} \cdot \frac{1}{R_S + r_O + (g_m + g_{mb})R_S r_O} \tag{3.78}$$

$$= -\frac{g_m r_O}{R_S + r_O + (g_m + g_{mb})R_S r_O} \cdot \frac{R_D [R_S + r_O + (g_m + g_{mb})R_S r_O]}{R_D + R_S + r_O + (g_m + g_{mb})R_S r_O} \tag{3.79}$$

The two fractions in (3.79) represent two important parameters of the circuit: the first is identical to that in (3.61), i.e., the equivalent transconductance of a degenerated MOSFET; and the second denotes the parallel combination of R_D and $R_S + r_O + (g_m + g_{mb})R_S r_O$, i.e., the overall output resistance of the circuit.

The above discussion suggests that in some circuits, it may be easier to calculate the voltage gain by exploiting the following lemma. We recall that the output port of a linear circuit can be represented by a Norton equivalent [Fig. 3.32(a)].

Lemma In a linear circuit, the voltage gain is equal to $-G_m R_{out}$, where G_m denotes the transconductance of the circuit when the output is shorted to ground [Fig. 3.32(b)] and R_{out} represents the output resistance of the circuit when the input voltage is set to zero [Fig. 3.32(c)].

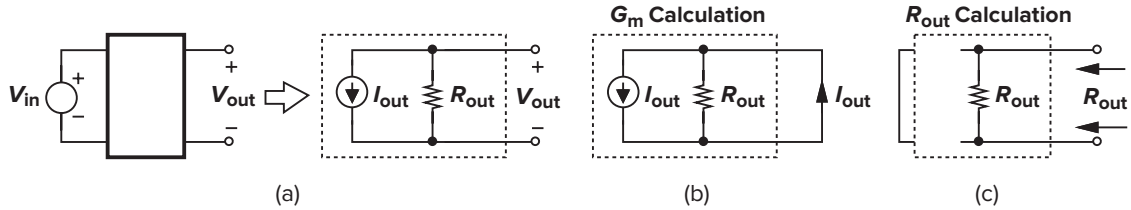


Figure 3.32 (a) Norton equivalent of a linear circuit; (b) G_m calculation; and (c) R_{out} calculation.

The lemma can be proved by noting that the output voltage in Fig. 3.32(a) is equal to $-I_{out}R_{out}$, and I_{out} can be obtained by measuring the short-circuit current at the output. Defining $G_m = I_{out}/V_{in}$, we have $V_{out} = -G_m V_{in} R_{out}$. This lemma proves useful if G_m and R_{out} can be determined by inspection. Note the direction of I_{out}.

▶ Example 3.11

Calculate the voltage gain of the circuit shown in Fig. 3.33. Assume that I_0 is ideal.

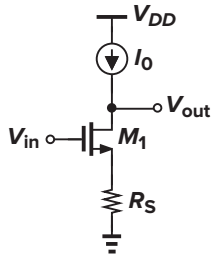


Figure 3.33

Solution

The transconductance and output resistance of the stage are given by Eqs. (3.61) and (3.66), respectively. Thus,

$$A_v = -\frac{g_m r_O}{R_S + [1 + (g_m + g_{mb})R_S]r_O}\{[1 + (g_m + g_{mb})r_O]R_S + r_O\} \tag{3.80}$$

$$= -g_m r_O \tag{3.81}$$

Interestingly, the voltage gain is equal to the intrinsic gain of the transistor and independent of R_S. This is because, if I_0 is ideal, the current through R_S cannot change, and hence the small-signal voltage drop across R_S is zero—as if R_S were zero itself.

◀

3.4 ■ Source Follower

Our analysis of the common-source stage indicates that, to achieve a high voltage gain with limited supply voltage, the load impedance must be as large as possible. If such a stage is to drive a low-impedance load, then a "buffer" must be placed after the amplifier so as to drive the load with negligible reduction in gain. The source follower (also called the "common-drain" stage) can operate as a voltage buffer.

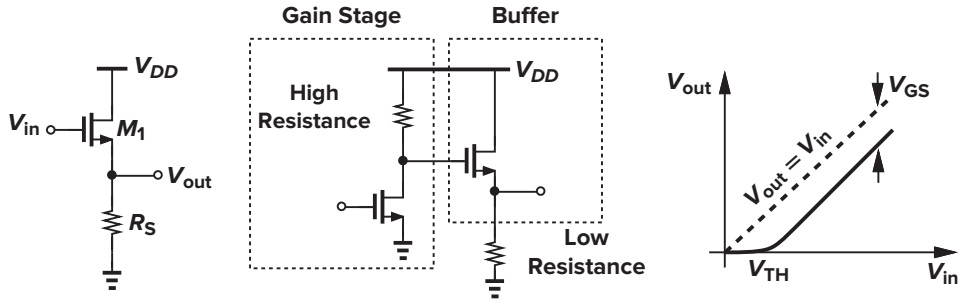


Figure 3.34 (a) Source follower, (b) example of its role as a buffer, and (c) its input-output characteristic.

Illustrated in Fig. 3.34(a), the source follower senses the signal at the gate, while presenting a high input impedance, and drives the load at the source, allowing the source potential to "follow" the gate voltage. Figure 3.34(b) depicts how the circuit can be used to drive a low resistance without degrading the voltage gain of a CS stage. Beginning with the large-signal behavior of the source follower, we note that for $V_{in} < V_{TH}$, M_1 is off and $V_{out} = 0$. As V_{in} exceeds V_{TH}, M_1 turns on in saturation (why?) and I_{D1} flows through R_S [Fig. 3.34(c)]. As V_{in} increases further, V_{out} follows the input with a difference (level shift) equal to V_{GS}. We can express the input-output characteristic as

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH} - V_{out})^2 R_S = V_{out} \tag{3.82}$$

where channel-length modulation is neglected. Let us calculate the small-signal gain of the circuit by differentiating both sides of (3.82) with respect to V_{in}:

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}2(V_{in} - V_{TH} - V_{out})\left(1 - \frac{\partial V_{TH}}{\partial V_{in}} - \frac{\partial V_{out}}{\partial V_{in}}\right) R_S = \frac{\partial V_{out}}{\partial V_{in}} \tag{3.83}$$

Since $\partial V_{TH}/\partial V_{in} = (\partial V_{TH}/\partial V_{SB})(\partial V_{SB}/\partial V_{in}) = \eta \partial V_{out}/\partial V_{in}$,

$$\frac{\partial V_{out}}{\partial V_{in}} = \frac{\mu_n C_{ox}\dfrac{W}{L}(V_{in} - V_{TH} - V_{out})R_S}{1 + \mu_n C_{ox}\dfrac{W}{L}(V_{in} - V_{TH} - V_{out})R_S(1+\eta)} \tag{3.84}$$

Also, note that

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH} - V_{out}) \tag{3.85}$$

Consequently,

$$A_v = \frac{g_m R_S}{1 + (g_m + g_{mb}) R_S} \tag{3.86}$$

The same result is more easily obtained with the aid of a small-signal equivalent circuit. From Fig. 3.35, we have $V_{in} - V_1 = V_{out}$, $V_{bs} = -V_{out}$, and $g_m V_1 - g_{mb} V_{out} = V_{out}/R_S$. Thus, $V_{out}/V_{in} = g_m R_S/[1 + (g_m + g_{mb})R_S]$.

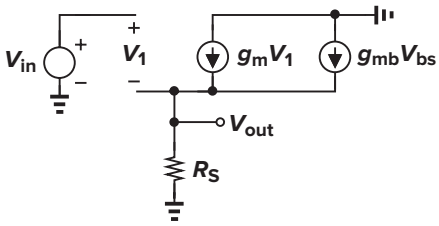


Figure 3.35 Small-signal equivalent circuit of source follower.

Sketched in Fig. 3.36 vs. V_{in}, the voltage gain begins from zero for $V_{in} \approx V_{TH}$ (that is, $g_m \approx 0$) and monotonically increases. As the drain current and g_m increase, A_v approaches $g_m/(g_m + g_{mb}) = 1/(1+\eta)$. Since η itself slowly decreases with V_{out}, A_v would eventually become equal to unity, but for typical allowable source-bulk voltages, η remains greater than roughly 0.2.

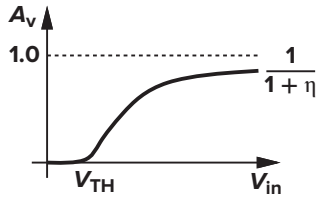


Figure 3.36 Voltage gain of source follower versus input voltage.

An important result of (3.86) is that even if $R_S = \infty$, the voltage gain of a source follower is not equal to one (unless body effect is removed as explained later). We return to this point later. Note that M_1 in Fig. 3.34(a) remains in saturation if V_{in} does not exceed $V_{DD} + V_{TH}$.

In the source follower of Fig. 3.34(a), the drain current of M_1 heavily depends on the input dc level. For example, if V_{in} changes from 0.7 V to 1 V, I_D may increase by a factor of 2, and hence $V_{GS} - V_{TH}$ by $\sqrt{2}$. Even if V_{TH} is relatively constant, the increase in V_{GS} means that V_{out} $(= V_{in} - V_{GS})$ does not follow V_{in} faithfully, thereby incurring nonlinearity. To alleviate this issue, the resistor can be replaced by a constant current source as shown in Fig. 3.37(a). The current source itself is implemented as an NMOS transistor operating in the saturation region [Fig. 3.37(b)].

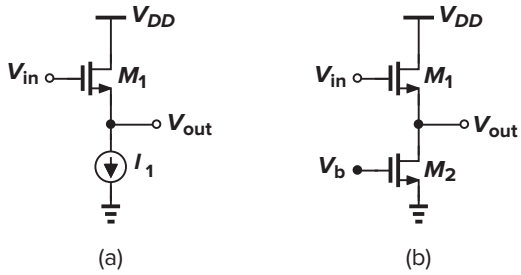


Figure 3.37 Source follower using (a) an ideal current source, and (b) an NMOS transistor as a current source.

▶ Example 3.12

Suppose that in the source follower of Fig. 3.37(a), $(W/L)_1 = 20/0.5$, $I_1 = 200\ \mu$A, $V_{TH0} = 0.6$ V, $2\Phi_F = 0.7$ V, $V_{DD} = 1.2$ V, $\mu_n C_{ox} = 50\ \mu$A/V^2, and $\gamma = 0.4$ V$^{1/2}$.

(a) Calculate V_{out} for $V_{in} = 1.2$ V.

(b) If I_1 is implemented as M_2 in Fig. 3.37(b), find the minimum value of $(W/L)_2$ for which M_2 remains saturated when $V_{in} = 1.2$ V.

Solution

(a) Since the threshold voltage of M_1 depends on V_{out}, we perform a simple iteration. Noting that

$$(V_{in} - V_{TH} - V_{out})^2 = \frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1} \tag{3.87}$$

we first assume that $V_{TH} \approx 0.6$ V, obtaining $V_{out} = 0.153$ V. Now we calculate a new V_{TH} as

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}) \tag{3.88}$$

$$= 0.635\ \text{V} \tag{3.89}$$

This indicates that V_{out} is approximately 35 mV less than that calculated above, i.e., $V_{out} \approx 0.118$ V.

(b) Since the drain-source voltage of M_2 is equal to 0.118 V, the device is saturated only if $(V_{GS}-V_{TH})_2 \leq 0.118$ V. With $I_D = 200\ \mu$A, this gives $(W/L)_2 \geq 287/0.5$. Note the substantial drain junction and overlap capacitance contributed by M_2 to the output node. ◀

▶ Example 3.13

Explain intuitively why the gain of the source follower in Fig. 3.37(a) is equal to unity if I_1 is ideal and $\lambda = \gamma = 0$.

Solution

In this case, the drain current of M_1 remains exactly constant, and so does V_{GS1}. Since $V_{out} = V_{in} - V_{GS1}$, we observe that a change in V_{in} must equally appear in V_{out}. Alternatively, as shown in Fig. 3.38, we can say that the small-signal drain current cannot flow through any path and must be zero, yielding $V_1 = 0$ and $V_{out} = V_{in}$.

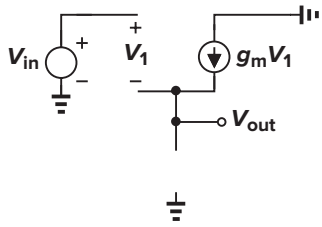


Figure 3.38 ◀

To gain a better understanding of source followers, let us calculate the small-signal output resistance of the circuit in Fig. 3.39(a). Using the equivalent circuit of Fig. 3.39(b) and noting that $V_X = -V_{bs}$, we write

$$I_X - g_m V_X - g_{mb} V_X = 0 \tag{3.90}$$

It follows that

$$R_{out} = \frac{1}{g_m + g_{mb}} \tag{3.91}$$

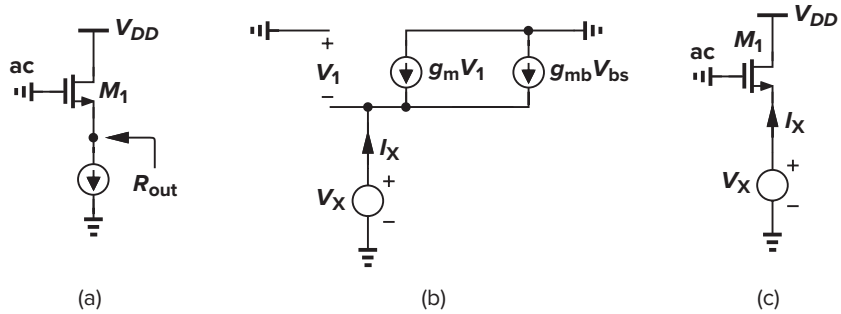


Figure 3.39 Calculation of the output impedance of a source follower.

This result should not come as a surprise: the circuit in Fig. 3.39(b) is similar to that in Fig. 3.11(b). Interestingly, body effect decreases the output resistance of source followers. To understand why, suppose that in Fig. 3.39(c), V_X decreases by ΔV so that the drain current increases. With no body effect, only the gate-source voltage of M_1 would increase by ΔV. With body effect, on the other hand, the threshold voltage of the device decreases as well. Thus, in $(V_{GS} - V_{TH})^2$, the first term increases and the second decreases, resulting in a greater change in the drain current and hence a lower output impedance.

The above phenomenon can also be studied with the aid of the small-signal model shown in Fig. 3.40(a). It is important to note that the magnitude of the current source $g_{mb}V_{bs} = g_{mb}V_X$ is linearly proportional to the voltage across it (because the current source and the voltage source are in parallel). Such a behavior is that of a simple resistor equal to $1/g_{mb}$, yielding the small-signal model shown in Fig. 3.40(b). The equivalent resistor simply appears in parallel with the output, thereby lowering the overall output resistance. Since without $1/g_{mb}$, the output resistance equals $1/g_m$, we conclude that

$$R_{out} = \frac{1}{g_m} \| \frac{1}{g_{mb}} \tag{3.92}$$

$$= \frac{1}{g_m + g_{mb}} \tag{3.93}$$

Modeling the effect of g_{mb} by a resistor—which is valid only for source followers—also helps explain the less-than-unity voltage gain implied by (3.86) for $R_S = \infty$. As shown in the Thevenin equivalent

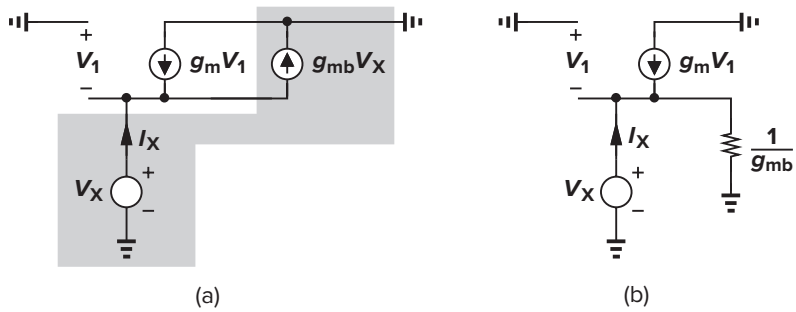


Figure 3.40 Source follower including body effect.

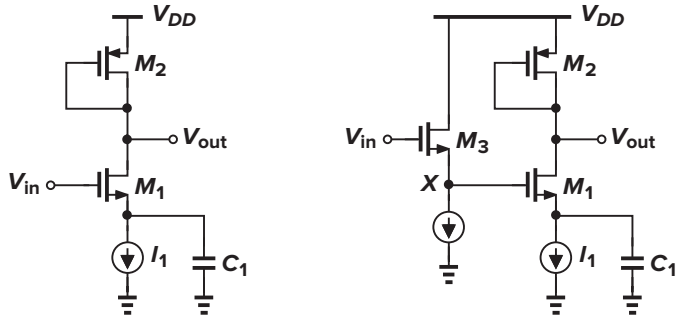


Figure 3.47

Solution

(a) Noting that the source of M_1 is at ac ground, we write the gain as

$$A_v = -g_{m1}[r_{O1} \| r_{O2} \| (1/g_{m2})] \tag{3.101}$$

Since $V_{out} = V_{DD} - |V_{GS2}|$, the maximum allowable dc level of V_{in} is equal to $V_{DD} - |V_{GS2}| + V_{TH1}$.

(b) If $V_{in} = V_{DD}$, then $V_X = V_{DD} - V_{GS3}$. For M_1 to be saturated when $V_{in} = V_{DD}$, we must have $V_{DD} - V_{GS3} - V_{TH1} \leq V_{DD} - |V_{GS2}|$, and hence $V_{GS3} + V_{TH1} \geq |V_{GS2}|$. ◀

As explained in Chapter 7, source followers also introduce substantial noise. For this reason, the circuit of Fig. 3.47(b) is ill-suited to low-noise applications.

3.5 ■ Common-Gate Stage

In common-source amplifiers and source followers, the input signal is applied to the gate of a MOSFET. It is also possible to apply the signal to the source terminal. Shown in Fig. 3.48(a), a common-gate (CG) stage senses the input at the source and produces the output at the drain. The gate is connected to a dc voltage to establish proper operating conditions. Note that the bias current of M_1 flows through the input signal source. Alternatively, as depicted in Fig. 3.48(b), M_1 can be biased by a constant current source, with the signal capacitively coupled to the circuit.

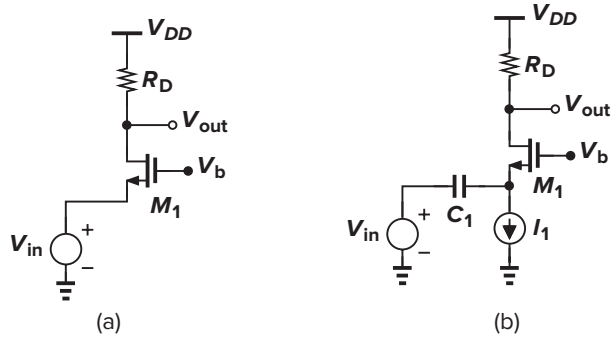


Figure 3.48 (a) Common-gate stage with direct coupling at input; (b) CG stage with capacitive coupling at input.

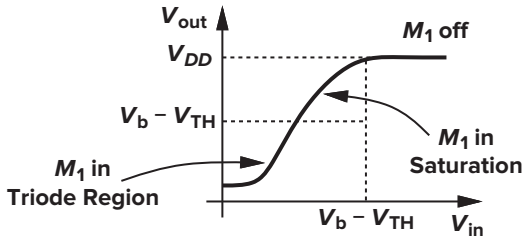


Figure 3.49 Common-gate input-output characteristic.

We first study the large-signal behavior of the circuit in Fig. 3.48(a). For simplicity, let us assume that V_{in} decreases from a large positive value. Also, $\lambda = 0$. For $V_{in} \geq V_b - V_{TH}$, M_1 is off and $V_{out} = V_{DD}$. For lower values of V_{in}, we can write

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 \tag{3.102}$$

if M_1 is in saturation. As V_{in} decreases, so does V_{out}, eventually driving M_1 into the triode region if

$$V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D = V_b - V_{TH} \tag{3.103}$$

The input-output characteristic is shown in Fig. 3.49, illustrating a case in which M_1 enters the triode region as V_{in} decreases. In the region where M_1 is saturated, we can express the output voltage as

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D \tag{3.104}$$

obtaining a small-signal gain of

$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})\left(-1 - \frac{\partial V_{TH}}{\partial V_{in}}\right)R_D \tag{3.105}$$

Since $\partial V_{TH}/\partial V_{in} = \partial V_{TH}/\partial V_{SB} = \eta$, we have

$$\frac{\partial V_{out}}{\partial V_{in}} = \mu_n C_{ox}\frac{W}{L}R_D(V_b - V_{in} - V_{TH})(1+\eta) \tag{3.106}$$

$$= g_m(1+\eta)R_D \tag{3.107}$$

Note that the gain is positive. Interestingly, body effect increases the equivalent transconductance of the stage.

For a given bias current and supply voltage (i.e., a given power budget), how do we maximize the voltage gain of a CG stage? We can increase g_m by widening the input device, eventually reaching subthreshold operation [$g_m \approx I_D/(\xi V_T)$] (why?), and/or we can increase R_D and, inevitably, the dc drop across it. We must bear in mind that the minimum allowable level of V_{out} in Fig. 3.48(b) is equal to $V_{GS} - V_{TH} + V_{I1}$, where V_{I1} denotes the minimum voltage required by I_1.

▶ Example 3.16

(a) Is it possible for M_1 in Fig. 3.48(a) to remain in saturation for the entire range of V_{in} from 0 to V_{DD}?
(b) Is it possible for M_1 to remain in the triode region for the entire range of V_{in} from 0 to V_{DD}?

▶ **Example 3.20**

As seen in Example 3.17, the input signal of a common-gate stage may be a current rather than a voltage. Shown in Fig. 3.58 is such an arrangement. Calculate V_{out}/I_{in} and the output impedance of the circuit if the input current source exhibits an output impedance equal to R_P.

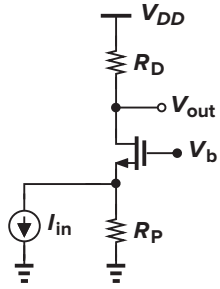


Figure 3.58

Solution

To find V_{out}/I_{in}, we replace I_{in} and R_P with a Thevenin equivalent and use (3.111) to write

$$\frac{V_{out}}{I_{in}} = \frac{(g_m + g_{mb})r_O + 1}{r_O + (g_m + g_{mb})r_O R_P + R_P + R_D} R_D R_P \tag{3.122}$$

The output impedance is simply equal to

$$R_{out} = \{[1 + (g_m + g_{mb})r_O]R_P + r_O\} \| R_D \tag{3.123}$$

◀

3.6 ■ Cascode Stage

As mentioned in Example 3.17, the input signal of a common-gate stage may be a current. We also know that a transistor in a common-source arrangement converts a voltage signal to a current signal. The cascade of a CS stage and a CG stage is called a "cascode"[4] topology, providing many useful properties. Figure 3.59 shows the basic configuration: M_1 generates a small-signal drain current proportional to the small-signal input voltage, V_{in}, and M_2 simply routes the current to R_D. We call M_1 the input device and M_2 the cascode device. Note that in this example, M_1 and M_2 carry equal bias and signal currents. As we describe the attributes of the circuit in this section, many advantages of the cascode topology over a simple common-source stage become evident. This circuit is also known as the "telescopic" cascode.

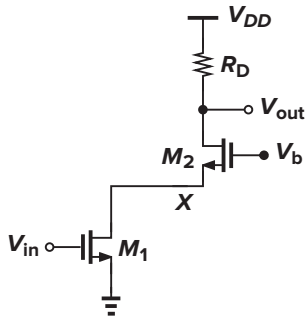


Figure 3.59 Cascode stage.

[4]The term cascode is believed to be the acronym for "cascaded triodes," possibly invented in vacuum tube days.

Before delving into our analysis, it is instructive to explore the circuit qualitatively. We wish to know what happens if the value of V_{in} or V_b changes by a small amount. Assume that both transistors are in saturation and $\lambda = \gamma = 0$. If V_{in} rises by ΔV, then I_{D1} increases by $g_{m1}\Delta V$. This change in current flows through the impedance seen at X, i.e., the impedance seen at the source of M_2, which is equal to $1/g_{m2}$. Thus, V_X falls by an amount given by $g_{m1}\Delta V \cdot (1/g_{m2})$ [Fig. 3.60(a)]. The change in I_{D1} also flows through R_D, producing a drop of $g_{m1}\Delta V R_D$ in V_{out}—just as in a simple CS stage.

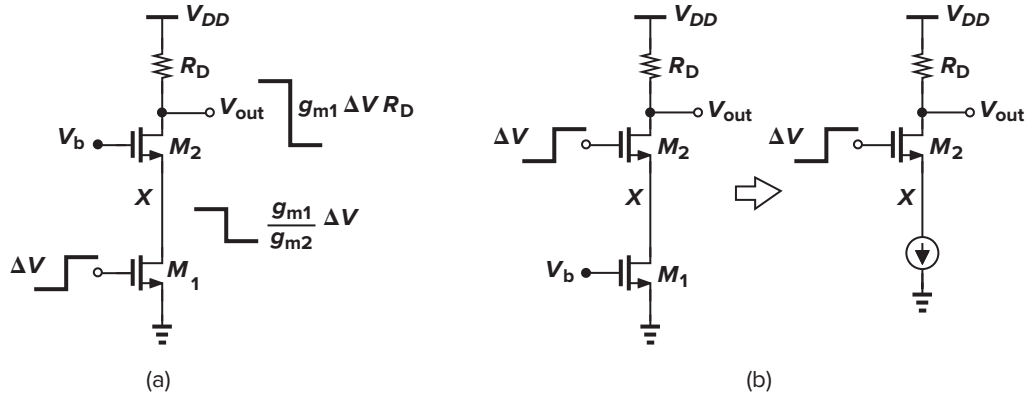


Figure 3.60 Cascode stage sensing a signal at the gate of (a) an input device and (b) a cascode device.

Now, consider the case where V_{in} is fixed and V_b increases by ΔV. Since V_{GS1} is constant and $r_{O1} = \infty$, we simplify the circuit as shown in Fig. 3.60(b). How do V_X and V_{out} change here? As far as node X is concerned, M_2 operates as a *source follower* because it senses an input, ΔV, at its gate and generates an output at X. With $\lambda = \gamma = 0$, the small-signal voltage gain of the follower is equal to unity, regardless of the value of R_D (why?). Thus, V_X rises by ΔV. On the other hand, V_{out} does *not* change because I_{D2} is equal to I_{D1} and hence remains *constant*. We say that the voltage gain from V_b to V_{out} is zero in this case.

Let us now study the bias conditions of the cascode, still assuming that $\lambda = \gamma = 0$. For M_1 to operate in saturation, we must have $V_X \geq V_{in} - V_{TH1}$. If M_1 and M_2 are both in saturation, M_2 operates as a source follower and V_X is determined primarily by V_b: $V_X = V_b - V_{GS2}$. Thus, $V_b - V_{GS2} \geq V_{in} - V_{TH1}$, and hence $V_b > V_{in} + V_{GS2} - V_{TH1}$ (Fig. 3.61). For M_2 to be saturated, $V_{out} \geq V_b - V_{TH2}$; that is,

$$V_{out} \geq V_{in} - V_{TH1} + V_{GS2} - V_{TH2} \tag{3.124}$$

$$= (V_{GS1} - V_{TH1}) + (V_{GS2} - V_{TH2}) \tag{3.125}$$

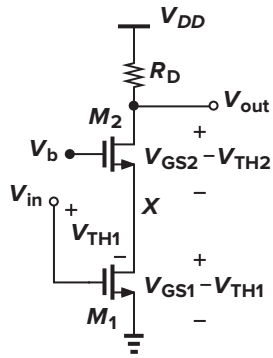


Figure 3.61 Allowable voltages in cascode stage.

if V_b is chosen to place M_1 at the edge of saturation. Consequently, the minimum output level for which both transistors operate in saturation is equal to the overdrive voltage of M_1 plus that of M_2. In other words, addition of M_2 to the circuit reduces the output voltage swing by at least the overdrive voltage of M_2. We say that M_2 is "stacked" on top of M_1. We also loosely say that the minimum output voltage is equal to two overdrives or $2V_{D,sat}$.

We now analyze the large-signal behavior of the cascode stage shown in Fig. 3.59 as V_{in} goes from zero to V_{DD}. For $V_{in} \leq V_{TH1}$, M_1 and M_2 are off, $V_{out} = V_{DD}$, and $V_X \approx V_b - V_{TH2}$ (if subthreshold conduction is neglected) (Fig. 3.62). As V_{in} exceeds V_{TH1}, M_1 begins to draw current, and V_{out} drops. Since I_{D2} increases, V_{GS2} must increase as well, causing V_X to fall. As V_{in} assumes sufficiently large values, two effects can occur: (1) V_X drops below V_{in} by V_{TH1}, forcing M_1 into the triode region; (2) V_{out} drops below V_b by V_{TH2}, driving M_2 into the triode region. Depending on the device dimensions and the values of R_D and V_b, one effect may occur before the other. For example, if V_b is relatively low, M_1 may enter the triode region first. Note that if M_2 goes into the deep triode region, V_X and V_{out} become nearly equal.

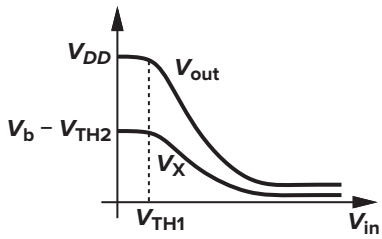


Figure 3.62 Input-output characteristic of a cascode stage.

Let us now consider the small-signal characteristics of a cascode stage, assuming that both transistors operate in saturation. If $\lambda = 0$, the voltage gain is equal to that of a common-source stage because the drain current produced by the input device must flow through the cascode device. Illustrated in the equivalent circuit of Fig. 3.63, this result is independent of the transconductance and body effect of M_2. It can also be verified using $A_v = -G_m R_{out}$.

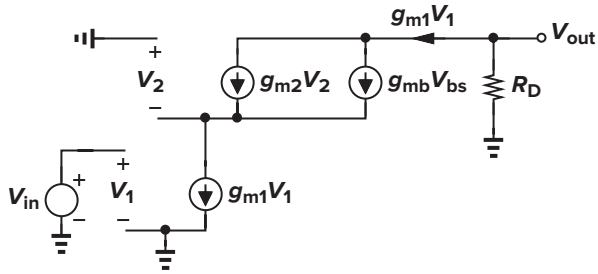


Figure 3.63 Small-signal equivalent circuit of cascode stage.

▶ Example 3.21

Calculate the voltage gain of the circuit shown in Fig. 3.64 if $\lambda = 0$.

Solution

The small-signal drain current of M_1, $g_{m1}V_{in}$, is divided between R_P and the impedance seen looking into the source of M_2, $1/(g_{m2} + g_{mb2})$. Thus, the current flowing through M_2 is

$$I_{D2} = g_{m1} V_{in} \frac{(g_{m2} + g_{mb2}) R_P}{1 + (g_{m2} + g_{mb2}) R_P} \tag{3.126}$$

FETs operating in saturation) for all transistors. If the drain of a device is connected to a high impedance (e.g., the drain of another), then add r_O to its model. At this point, the basic properties of most circuits can be determined by inspection. In a second, more accurate iteration, the body effect of devices whose source or bulk is not at ac ground can be included as well.

For bias calculations, it is usually adequate to neglect channel-length modulation and body effect in the first pass. These effects do introduce some error, but they can be included in the next iteration step—after the basic properties are understood.

In today's analog design, simulation of circuits is essential because the behavior of short-channel MOSFETs cannot be predicted accurately by hand calculations. Nonetheless, if the designer avoids a simple and intuitive analysis of the circuit and hence skips the task of gaining insight, then he/she cannot interpret the simulation results intelligently. For this reason, we say, "Don't let the computer think for you." Some say, "Don't be a SPICE monkey."

Problems

Unless otherwise stated, in the following problems, use the device data shown in Table 2.1 and assume that $V_{DD} = 3$ V where necessary. All device dimensions are effective values and in microns.

3.1. For the circuit of Fig. 3.13, calculate the small-signal voltage gain if $(W/L)_1 = 50/0.5$, $(W/L)_2 = 10/0.5$, and $I_{D1} = I_{D2} = 0.5$ mA. What is the gain if M_2 is implemented as a diode-connected PMOS device (Fig. 3.16)?

3.2. In the circuit of Fig. 3.18, assume that $(W/L)_1 = 50/0.5$, $(W/L)_2 = 50/2$, and $I_{D1} = I_{D2} = 0.5$ mA when both devices are in saturation. Recall that $\lambda \propto 1/L$.
(a) Calculate the small-signal voltage gain.
(b) Calculate the maximum output voltage swing while both devices are saturated.

3.3. In the circuit of Fig. 3.4(a), assume that $(W/L)_1 = 50/0.5$, $R_D = 2\,\text{k}\Omega$, and $\lambda = 0$.
(a) What is the small-signal gain if M_1 is in saturation and $I_D = 1$ mA?
(b) What input voltage places M_1 at the edge of the triode region? What is the small-signal gain under this condition?
(c) What input voltage drives M_1 into the triode region by 50 mV? What is the small-signal gain under this condition?

3.4. Suppose the common-source stage of Fig. 3.4(a) is to provide an output swing from 1 V to 2.5 V. Assume that $(W/L)_1 = 50/0.5$, $R_D = 2\,\text{k}\Omega$, and $\lambda = 0$.
(a) Calculate the input voltages that yield $V_{out} = 1$ V and $V_{out} = 2.5$ V.
(b) Calculate the drain current and the transconductance of M_1 for both cases.
(c) How much does the small-signal gain, $g_m R_D$, vary as the output goes from 1 V to 2.5 V? (Variation of small-signal gain can be viewed as nonlinearity.)

3.5. Calculate the intrinsic gain of an NMOS device and a PMOS device operating in saturation with $W/L = 50/0.5$ and $|I_D| = 0.5$ mA. Repeat these calculations if $W/L = 100/1$.

3.6. Assuming a constant L, plot the intrinsic gain of a satuated device versus the gate-source voltage if **(a)** the drain current is constant, **(b)** W is constant.

3.7. Assuming a constant L, plot the intrinsic gain of a saturated device versus W/L if **(a)** the gate-source voltage is constant, **(b)** the drain current is constant.

3.8. An NMOS transistor with $W/L = 50/0.5$ is biased with $V_G = +1.2$ V and $V_S = 0$. The drain voltage is varied from 0 to 3 V.
(a) Assuming the bulk voltage is zero, plot the intrinsic gain versus V_{DS}.
(b) Repeat part **(a)** for a bulk voltage of -1 V.

3.9. For an NMOS device operating in saturation, plot g_m, r_O, and $g_m r_O$ as the bulk voltage goes from 0 to $-\infty$ while other terminal voltages remain constant.

3.10. Consider the circuit of Fig. 3.13 with $(W/L)_1 = 50/0.5$ and $(W/L)_2 = 10/0.5$. Assume that $\lambda = \gamma = 0$.
(a) At what input voltage is M_1 at the edge of the triode region? What is the small-signal gain under this condition?
(b) What input voltage drives M_1 into the triode region by 50 mV? What is the small-signal gain under this condition?

3.11. Repeat Problem 3.10 if body effect is not neglected.

3.12. In the circuit of Fig. 3.17, $(W/L)_1 = 20/0.5$, $I_1 = 1$ mA, and $I_S = 0.75$ mA. Assuming $\lambda = 0$, calculate $(W/L)_2$ such that M_1 is at the edge of the triode region. What is the small-signal voltage gain under this condition?

3.13. Plot the small-signal gain of the circuit shown in Fig. 3.17 as I_S goes from 0 to $0.75I_1$. Assume that M_1 is always saturated, and neglect channel-length modulation and body effect.

3.14. The circuit of Fig. 3.18 is designed to provide an output voltage swing of 2.2 V with a bias current of 1 mA and a small-signal voltage gain of 100. Calculate the dimensions of M_1 and M_2.

3.15. Sketch V_{out} versus V_{in} for the circuits of Fig. 3.78 as V_{in} varies from 0 to V_{DD}. Identify important transition points.

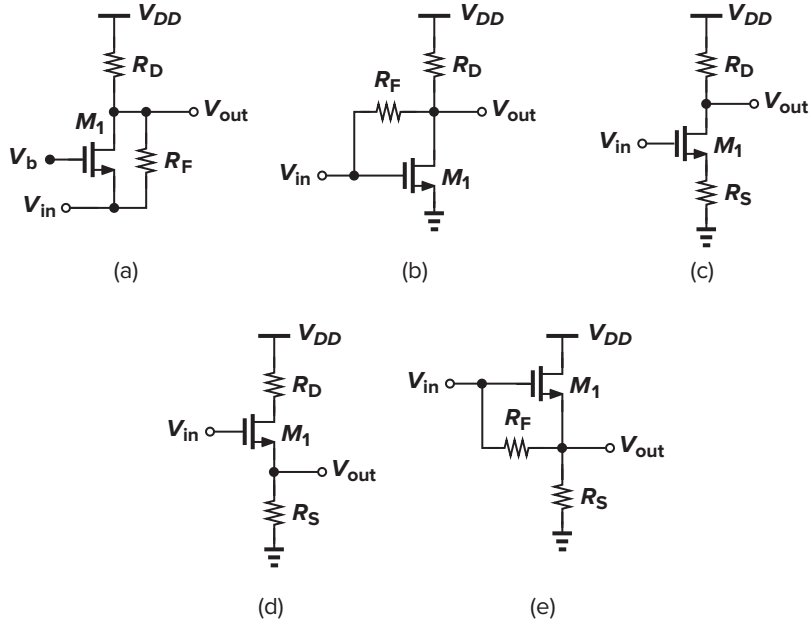


Figure 3.78

3.16. Sketch V_{out} versus V_{in} for the circuits of Fig. 3.79 as V_{in} varies from 0 to V_{DD}. Identify important transition points.

3.17. Sketch V_{out} versus V_{in} for the circuits of Fig. 3.80 as V_{in} varies from 0 to V_{DD}. Identify important transition points.

3.18. Sketch I_X versus V_X for the circuits of Fig. 3.81 as V_X varies from 0 to V_{DD}. Identify important transition points.

3.19. Sketch I_X versus V_X for the circuits of Fig. 3.82 as V_X varies from 0 to V_{DD}. Identify important transition points.

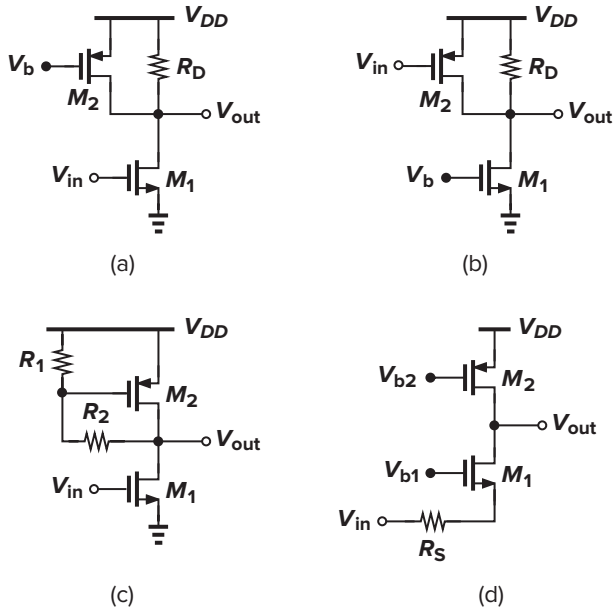


Figure 3.79

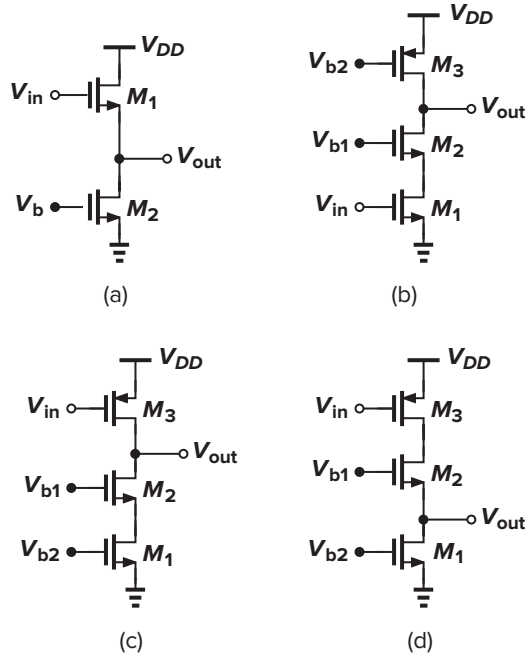
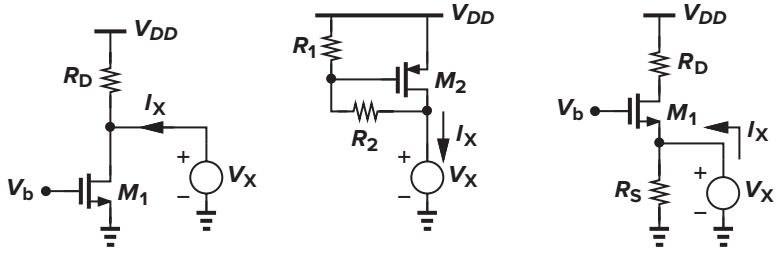
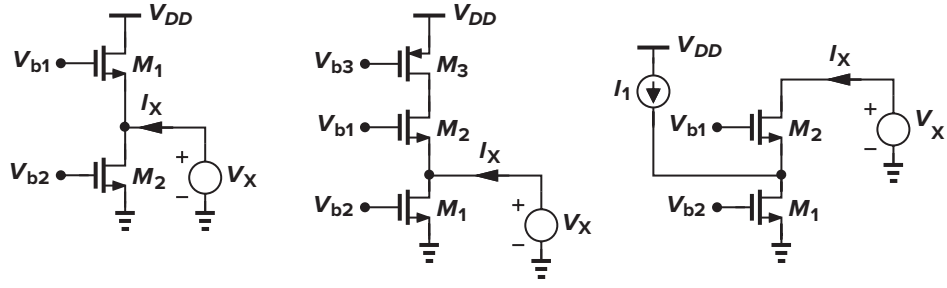


Figure 3.80

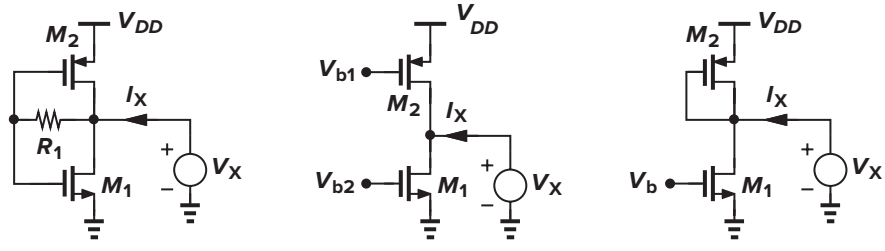


(a) (b) (c)

Figure 3.81



(a) (b) (c)



(d) (e) (f)

Figure 3.82

3.20. Assuming all MOSFETs are in saturation, calculate the small-signal voltage gain of each circuit in Fig. 3.83 ($\lambda \neq 0, \gamma = 0$).

3.21. Assuming all MOSFETs are in saturation, calculate the small-signal voltage gain of each circuit in Fig. 3.84 ($\lambda \neq 0, \gamma = 0$).

3.22. Sketch V_X and V_Y as a function of time for each circuit in Fig. 3.85. The initial voltage across C_1 is equal to V_{DD}.

3.23. In the cascode stage of Fig. 3.59, assume that $(W/L)_1 = 50/0.5$, $(W/L)_2 = 10/0.5$, $I_{D1} = I_{D2} = 0.5$ mA, and $R_D = 1$ kΩ.

(a) Choose V_b such that M_1 is 50 mV away from the triode region.

(b) Calculate the small-signal voltage gain.

(c) Using the value of V_b found in part (a), calculate the maximum output voltage swing. Which device enters the triode region first as V_{out} falls?

(d) Calculate the swing at node X for the maximum output swing obtained above.

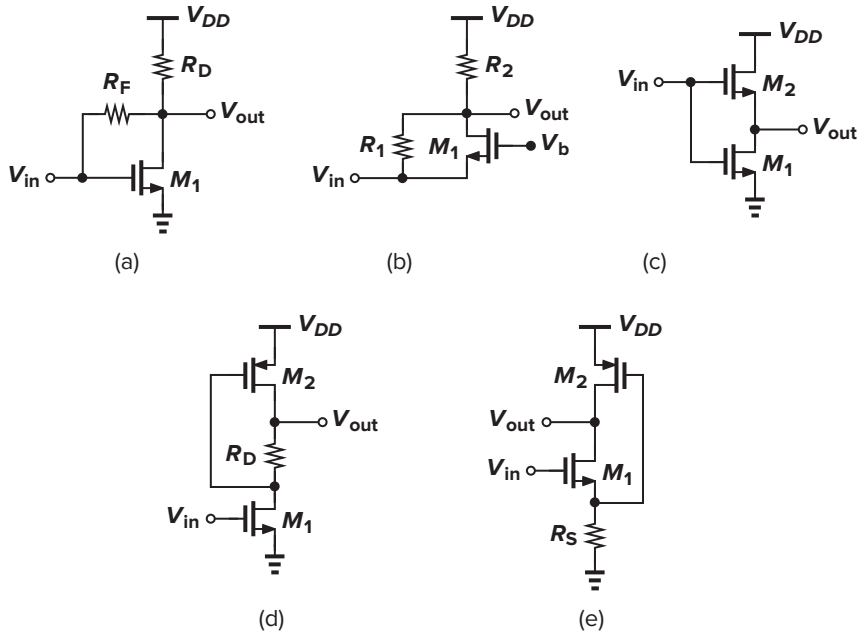


Figure 3.83

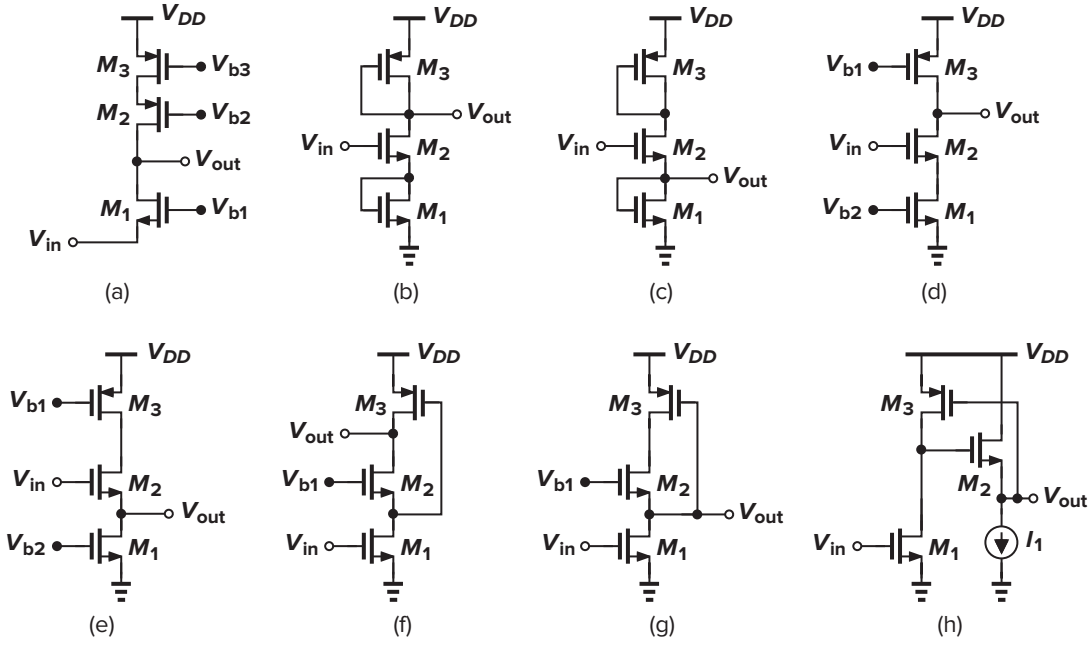


Figure 3.84

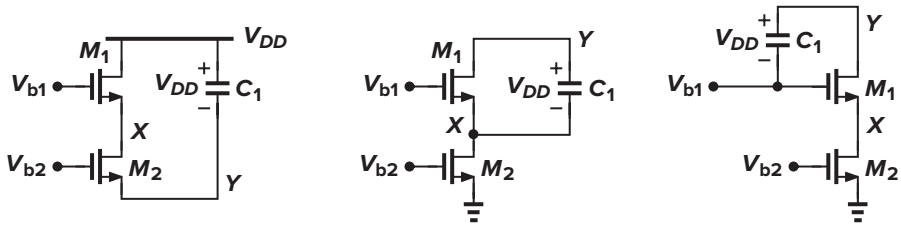


Figure 3.85

3.24. Consider the circuit of Fig. 3.23 with $(W/L)_1 = 50/0.5$, $R_D = 2\ \text{k}\Omega$, and $R_S = 200\ \Omega$.
(a) Calculate the small-signal voltage gain if $I_D = 0.5$ mA.
(b) Assuming $\lambda = \gamma = 0$, calculate the input voltage that places M_1 at the edge of the triode region. What is the gain under this condition?

3.25. Suppose the circuit of Fig. 3.22 is designed for a voltage gain of 5. If $(W/L)_1 = 20/0.5$, $I_{D1} = 0.5$ mA, and $V_b = 0$ V:
(a) Calculate the aspect ratio of M_2.
(b) What input level places M_1 at the edge of the triode region? What is the small-signal gain under this condition?
(c) What input level places M_2 at the edge of the saturation region? What is the small-signal gain under this condition?

3.26. Sketch the small-signal voltage gain of the circuit shown in Fig. 3.22 as V_b varies from 0 to V_{DD}. Consider two cases:
(a) M_1 enters the triode region before M_2 is saturated;
(b) M_1 enters the triode region after M_2 is saturated.

3.27. A source follower can operate as a level shifter. Suppose the circuit of Fig. 3.37(b) is designed to shift the voltage level by 1 V, i.e., $V_{in} - V_{out} = 1$ V.
(a) Calculate the dimensions of M_1 and M_2 if $I_{D1} = I_{D2} = 0.5$ mA, $V_{GS2} - V_{GS1} = 0.5$ V, and $\lambda = \gamma = 0$.
(b) Repeat part (a) if $\gamma = 0.45\ \text{V}^{-1}$ and $V_{in} = 2.5$ V. What is the minimum input voltage for which M_2 remains saturated?

3.28. Sketch the small-signal gain, V_{out}/V_{in}, of the cascode stage shown in Fig. 3.59 as V_b goes from 0 to V_{DD}. Assume that $\lambda = \gamma = 0$.

3.29. The cascode of Fig. 3.70 is designed to provide an output swing of 1.9 V with a bias current of 0.5 mA. If $\gamma = 0$ and $(W/L)_{1-4} = W/L$, calculate V_{b1}, V_{b2}, and W/L. What is the voltage gain if $L = 0.5\ \mu$m?

3.30. Consider the gate-source voltage of M_1 in Fig. 3.23(a): $V_{GS} = V_{in} - I_D R_S$. Determine ΔV_{GS} in response to a change in V_{in} and show that it *decreases* as $g_m R_S$ increases. How does this trend show that the circuit becomes more linear?

3.31. Prove that the voltage gain from V_{DD} to V_{out} in Fig. 3.21 is given by

$$\frac{V_{out}}{V_{in}} = \frac{g_{m2} r_{O2} + 1}{r_{O2} + r_{O1}} r_{O1} \tag{3.147}$$

3.32. In the circuit shown in Fig. 3.86, prove that

$$\frac{V_{out1}}{V_{out2}} = \frac{-R_D}{R_S} \tag{3.148}$$

where V_{out1} and V_{out2} are small-signal quantities and $\lambda,\ \gamma > 0$.

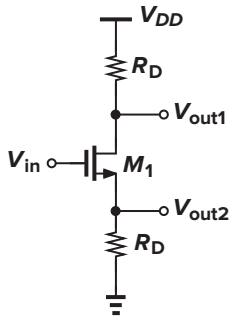


Figure 3.86

3.33. The CG stage of Fig. 3.51(a) is designed such that its input resistance (seen at node X) matches the signal source resistance, R_S. If $\lambda,\ \gamma > 0$, prove that

$$\frac{V_{out}}{V_{in}} = \frac{1 + (g_m + g_{mb})r_O}{2 + \left(1 + \dfrac{r_O}{R_D}\right)} \tag{3.149}$$

Also, prove that

$$\frac{V_{out}}{V_{in}} = \frac{R_D}{2R_S} \tag{3.150}$$

3.34. Calculate the voltage gain of a source follower using the lemma $A_v = -G_m R_{out}$. Assume that the circuit drives a load resistance of R_L and $\lambda,\ \gamma > 0$.

3.35. Calculate the voltage gain of a common-gate stage using the lemma $A_v = -G_m R_{out}$. Assume a source resistance of R_S and $\lambda,\ \gamma > 0$.

3.36. How many amplifier topologies can you create using each of the structures shown in Fig. 3.87 and no other transistors? (The source and drain terminals can be swapped.)

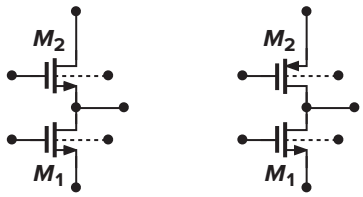


Figure 3.87