CHAPTER

4

Differential Amplifiers

The differential amplifier is among the most important circuit inventions, dating back to the vacuum tube era. Offering many useful properties, differential operation has become the de facto choice in today's high-performance analog and mixed-signal circuits.

This chapter deals with the analysis and design of CMOS differential amplifiers. Following a review of single-ended and differential operation, we describe the basic differential pair and analyze both the large-signal and the small-signal behavior. Next, we introduce the concept of common-mode rejection and formulate it for differential amplifiers. We then study differential pairs with diode-connected and current-source loads as well as differential cascode stages. Finally, we describe the Gilbert cell.

4.1 ■ Single-Ended and Differential Operation

A "single-ended" signal is defined as one that is measured with respect to a fixed potential, usually the ground [Fig. 4.1(a)]. A differential signal is defined as one that is measured between two nodes that have *equal* and *opposite* signal excursions around a fixed potential [Fig. 4.1(b)]. In the strict sense, the two nodes must also exhibit equal impedances to that potential. The "center" potential in differential signaling is called the "common-mode" (CM) level. It is helpful to view the CM level as the bias value of the voltages, i.e., the value in the absence of signals.

The specification of signal swings in a differential system can be confusing. Suppose each single-ended output in Fig. 4.1(b) has a peak amplitude of V_0. Then, the single-ended peak-to-peak swing is $2V_0$ and the differential peak-to-peak swing is $4V_0$. For example, if the voltage at X (with respect to ground) is $V_0 \cos \omega t + V_{CM}$ and that at Y is $-V_0 \cos \omega t + V_{CM}$, then the peak-to-peak swing of $V_X - V_Y$ ($=2V_0 \cos \omega t$) is $4V_0$. It is therefore not surprising that a circuit with a supply voltage of 1 V can deliver a peak-to-peak differential swing of 1.6 V.

An important advantage of differential operation over single-ended signaling is higher immunity to "environmental" noise. Consider the example depicted in Fig. 4.2, where two adjacent lines in a circuit carry a small, sensitive signal and a large clock waveform. Due to capacitive coupling between the lines, transitions on line L_2 corrupt the signal on line L_1. Now suppose, as shown in Fig. 4.2(b), the sensitive signal is distributed as two equal and opposite phases. If the clock line is placed midway between the two, the transitions disturb the differential phases by equal amounts, leaving the *difference* intact. Since the common-mode level of the two phases is disturbed, but the differential output is not corrupted, we say that this arrangement "rejects" common-mode noise.[1]

[1] It is also possible to place a "shield" line between the sensitive line and the clock line (Chapter 19).

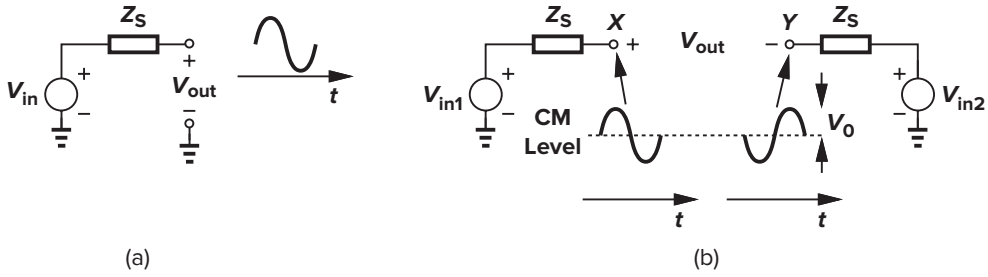


Figure 4.1 (a) Single-ended and (b) differential signals.

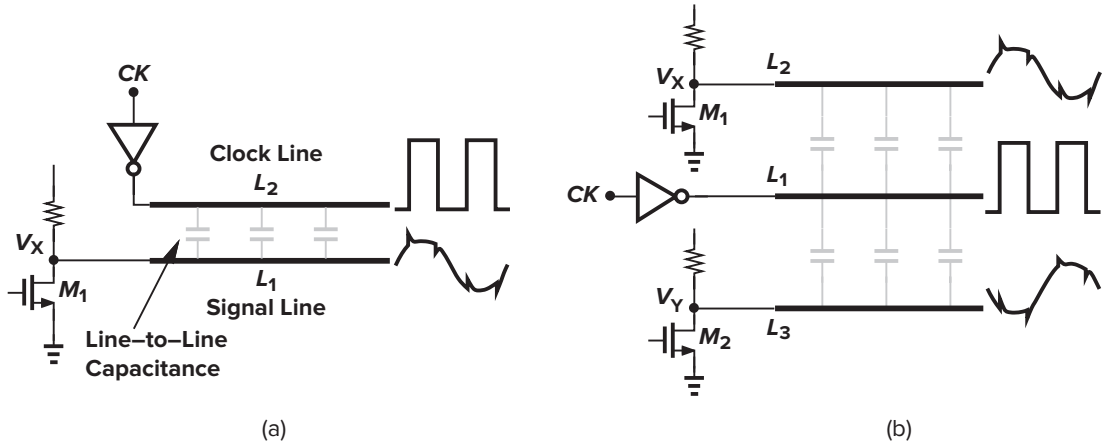


Figure 4.2 (a) Corruption of a signal due to coupling; (b) reduction of coupling by differential operation.

Another example of common-mode rejection occurs with noisy supply voltages. In the CS stage of Fig. 4.3(a), if V_{DD} varies by ΔV, then V_{out} changes by approximately the same amount, i.e., the output is quite susceptible to noise on V_{DD}. Now consider the circuit in Fig. 4.3(b). Here, if the circuit is symmetric, noise on V_{DD} affects V_X and V_Y, but not $V_X - V_Y = V_{out}$. Thus, the circuit of Fig. 4.3(b) is much more robust in dealing with supply noise.

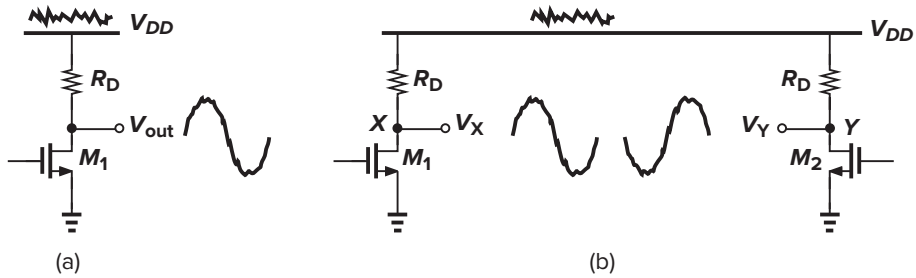


Figure 4.3 Effect of supply noise on (a) a single-ended circuit and (b) a differential circuit.

Thus far, we have seen the importance of employing differential paths for sensitive signals ("victims"). It is also beneficial to employ differential distribution for *noisy lines* ("aggressors"). For example, suppose the clock signal of Fig. 4.2 is distributed in differential form on two lines (Fig. 4.4). Then, with perfect symmetry, the components coupled from CK and $\overline{CK}$ to the signal line cancel each other.

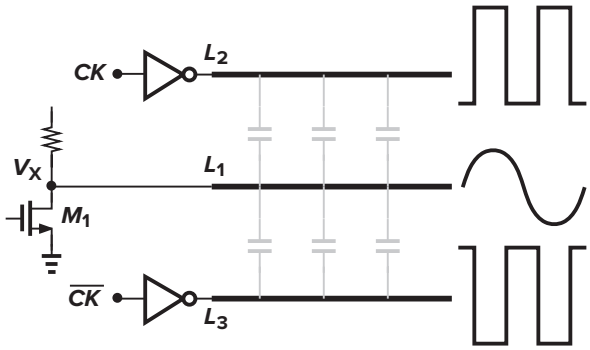


Figure 4.4 Reduction of coupled noise by differential operation.

▶ Example 4.1

If differential victims or differential aggressors improve the overall noise immunity, can we choose differential phases for *both* victims and aggressors?

Solution

Yes, we can. Let us consider the arrangement shown in Fig. 4.5(a), where the differential victims are surrounded by the differential aggressors. Unfortunately, in this case, $V_{out}^{+} - V_{out}^{-}$ is corrupted because V_{out}^{+} and V_{out}^{-} experience *opposite* jumps.

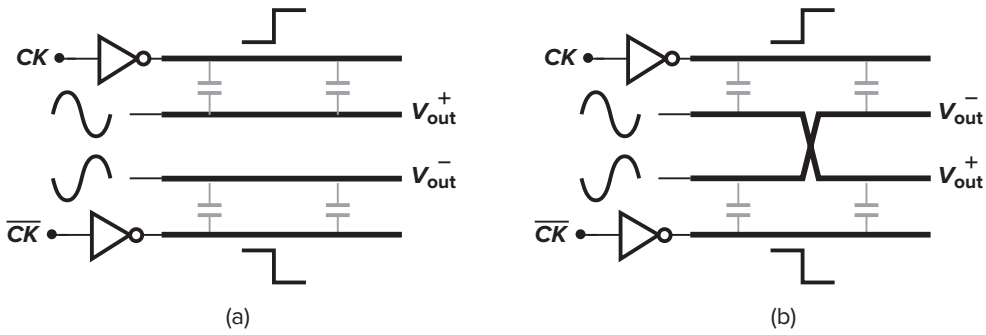


Figure 4.5

Now, suppose we modify the routing as depicted in Fig. 4.5(b), where V_{out}^{+} (V_{out}^{-}) is adjacent to CK ($\overline{CK}$) for half of the distance and to $\overline{CK}$ (CK) for the other half. In this case, the couplings from CK and $\overline{CK}$ cancel each other. Interestingly, V_{out}^{+} and V_{out}^{-} are free from the coupling—and so is their difference. This geometry is an example of "twisted pairs."

◀

Another useful property of differential signaling is the increase in maximum achievable voltage swings. In the circuit of Fig. 4.3, for example, the maximum output swing at X or Y is equal to $V_{DD} - (V_{GS} - V_{TH})$, whereas for $V_X - V_Y$, the peak-to-peak swing is equal to $2[V_{DD} - (V_{GS} - V_{TH})]$. Other advantages of differential circuits over their single-ended counterparts include simpler biasing and higher linearity (Chapter 14).

While differential circuits may occupy about twice as much area as single-ended alternatives, in practice this is a minor drawback. The numerous advantages of differential operation by far outweigh the possible increase in the area.

4.2 ■ Basic Differential Pair

How do we amplify a differential signal? As suggested by the observations in the previous section, we may incorporate two identical single-ended signal paths to process the two phases [Fig. 4.6(a)]. Here, two differential inputs, V_{in1} and V_{in2}, having a certain CM level, $V_{in,CM}$, are applied to the gates. The outputs are also differential and swing around the output CM level, $V_{out,CM}$. Such a circuit indeed offers some of the advantages of differential signaling: high rejection of supply noise, higher output swings, etc. But what happens if V_{in1} and V_{in2} experience a large common-mode disturbance or simply do not have a well-defined common-mode dc level? As the input CM level, $V_{in,CM}$, changes, so do the bias currents of M_1 and M_2, thus varying both the transconductance of the devices and the output CM level. The variation of the transconductance, in turn, leads to a change in the small-signal gain, while the departure of the output CM level from its ideal value lowers the maximum allowable output swings. For example, as shown in Fig. 4.6(b), if the input CM level is excessively low, the minimum values of V_{in1} and V_{in2} may in fact turn off M_1 and M_2, leading to severe clipping at the output. Thus, it is important that the bias currents of the devices have minimal dependence on the input CM level.

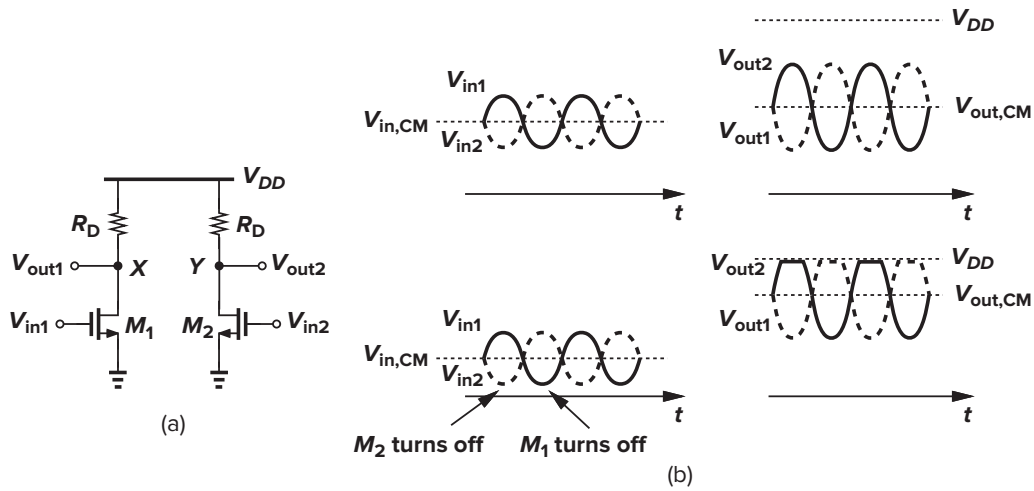


Figure 4.6 (a) Simple differential circuit; (b) illustration of sensitivity to the input common-mode level.

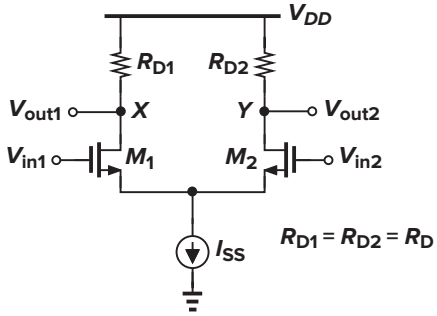


Figure 4.7 Basic differential pair.

A simple modification can resolve the above issue. Shown in Fig. 4.7, the "differential pair"[2] employs a current source I_{SS} to make $I_{D1} + I_{D2}$ independent of $V_{in,CM}$. Thus, if $V_{in1} = V_{in2}$, the bias current of

[2] Also called a "source-coupled" pair or (in the British literature) a "long-tailed" pair.

each transistor equals $I_{SS}/2$ and the output common-mode level is $V_{DD} - R_D I_{SS}/2$. It is instructive to study the large-signal behavior of the circuit for both differential and common-mode input variations. In the large-signal study, we neglect channel-length modulation and body effect.

4.2.1 Qualitative Analysis

Let us assume that in Fig. 4.7, $V_{in1} - V_{in2}$ varies from $-\infty$ to $+\infty$. If V_{in1} is much more negative than V_{in2}, M_1 is off, M_2 is on, and $I_{D2} = I_{SS}$. Thus, $V_{out1} = V_{DD}$ and $V_{out2} = V_{DD} - R_D I_{SS}$. As V_{in1} is brought closer to V_{in2}, M_1 gradually turns on, drawing a fraction of I_{SS} from R_{D1} and hence lowering V_{out1}. Since $I_{D1} + I_{D2} = I_{SS}$, the drain current of M_2 falls and V_{out2} rises. As shown in Fig. 4.8(a), for $V_{in1} = V_{in2}$, we have $V_{out1} = V_{out2} = V_{DD} - R_D I_{SS}/2$, which is the output CM level. As V_{in1} becomes more positive than V_{in2}, M_1 carries a greater current than does M_2 and V_{out1} drops below V_{out2}. For sufficiently large $V_{in1} - V_{in2}$, M_1 "hogs" all of I_{SS}, turning M_2 off. As a result, $V_{out1} = V_{DD} - R_D I_{SS}$ and $V_{out2} = V_{DD}$. Figure 4.8 also plots $V_{out1} - V_{out2}$ versus $V_{in1} - V_{in2}$. Note that the circuit contains three differential quantities: $V_{in1} - V_{in2}$, $V_{out1} - V_{out2}$, and $I_{D1} - I_{D2}$.

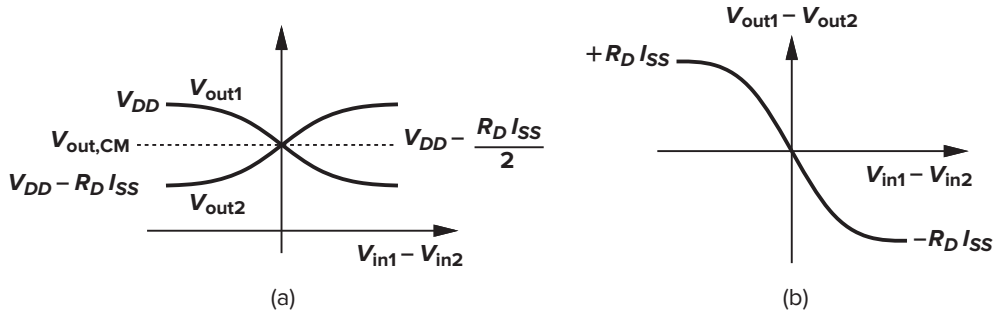


Figure 4.8 Differential input-output characteristics of a differential pair.

The foregoing analysis reveals two important attributes of the differential pair. First, the maximum and minimum levels at the output are well-defined (V_{DD} and $V_{DD} - R_D I_{SS}$, respectively) and independent of the input CM level. Second, as proved later, the small-signal gain (the slope of $V_{out1} - V_{out2}$ versus $V_{in1} - V_{in2}$) is maximum for $V_{in1} = V_{in2}$, gradually falling to zero as $|V_{in1} - V_{in2}|$ increases. In other words, the circuit becomes more nonlinear as the input voltage swing increases. For $V_{in1} = V_{in2}$, we say that the circuit is in "equilibrium."

Now let us consider the common-mode behavior of the circuit. As mentioned earlier, the role of the tail current source is to suppress the effect of input CM level variations on the operation of M_1 and M_2 and the output level. Does this mean that $V_{in,CM}$ can assume arbitrarily low or high values? To answer this question, we set $V_{in1} = V_{in2} = V_{in,CM}$ and vary $V_{in,CM}$ from 0 to V_{DD}. Figure 4.9(a) shows the circuit with I_{SS} implemented by an NFET. Note that the symmetry of the pair requires that $V_{out1} = V_{out2}$.

What happens if $V_{in,CM} = 0$? Since the gate potential of M_1 and M_2 is not more positive than their source potential, both devices are off, yielding $I_{D3} = 0$. This indicates that M_3 operates in the deep triode region because V_b is high enough to create an inversion layer in the transistor. With $I_{D1} = I_{D2} = 0$, the circuit is incapable of signal amplification, $V_{out1} = V_{out2} = V_{DD}$, and $V_P = 0$.

Now suppose $V_{in,CM}$ becomes more positive. Modeling M_3 by a resistor as in Fig. 4.9(b), we note that M_1 and M_2 turn on if $V_{in,CM} \geq V_{TH}$. Beyond this point, I_{D1} and I_{D2} continue to increase, and V_P also rises [Fig. 4.9(c)]. In a sense, M_1 and M_2 constitute a source follower, forcing V_P to track $V_{in,CM}$. For a sufficiently high $V_{in,CM}$, the drain-source voltage of M_3 exceeds $V_{GS3} - V_{TH3}$, allowing the device to operate in saturation. The total current through M_1 and M_2 then remains constant. We conclude that for proper operation, $V_{in,CM} \geq V_{GS1} + (V_{GS3} - V_{TH3})$.

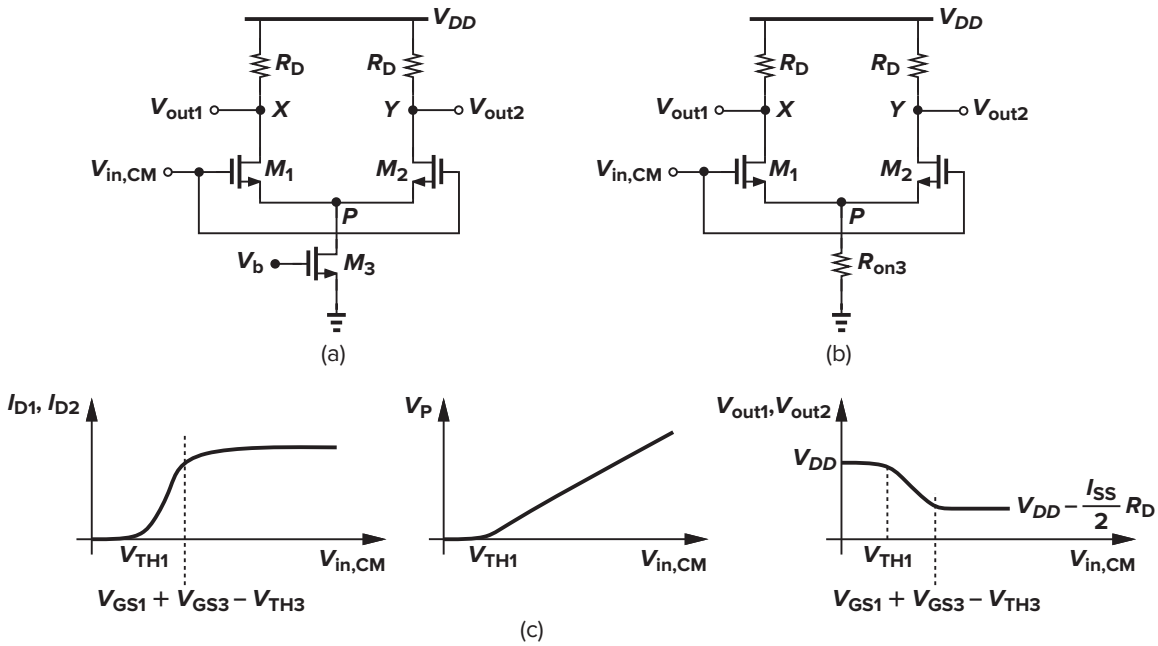


Figure 4.9 (a) Differential pair sensing an input common-mode change; (b) equivalent circuit if M_3 operates in the deep triode region; (c) common-mode input-output characteristics.

What happens if $V_{in,CM}$ rises further? Since V_{out1} and V_{out2} are relatively constant, we expect that M_1 and M_2 enter the triode region if $V_{in,CM} > V_{out1} + V_{TH} = V_{DD} - R_D I_{SS}/2 + V_{TH}$. This sets an upper limit on the input CM level. In summary, the allowable value of $V_{in,CM}$ is bounded as follows:

$$V_{GS1} + (V_{GS3} - V_{TH3}) \leq V_{in,CM} \leq \min\left[V_{DD} - R_D\frac{I_{SS}}{2} + V_{TH},\ V_{DD}\right] \tag{4.1}$$

Beyond the upper bound, the CM characteristics of Fig. 4.9(c) do not change, but the differential gain drops.[3]

▶ Example 4.2

Sketch the small-signal differential gain of a differential pair as a function of the input CM level.

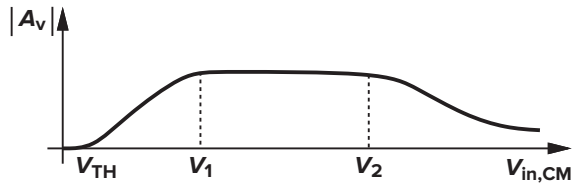


Figure 4.10

Solution

As shown in Fig. 4.10, the gain begins to increase as $V_{in,CM}$ exceeds V_{TH}. After the tail current source enters saturation ($V_{in,CM} = V_1$), the gain remains relatively constant. Finally, if $V_{in,CM}$ is so high that the input transistors enter the triode region ($V_{in,CM} = V_2$), the gain begins to fall.

◀

[3]This bound assumes small differential swings at the input and the output. This point become clear later.

With our understanding of differential and common-mode behavior of the differential pair, we can now answer another important question: How large can the output voltage swings of a differential pair be? Suppose the circuit is biased with input and output bias levels $V_{in,CM}$ and $V_{out,CM}$, respectively, and $V_{in,CM} < V_{out,CM}$. Also, assume that the voltage gain is high, that is, the input swing is much less than the output swing. As illustrated in Fig. 4.11, for M_1 and M_2 to be saturated, each output can go as high as V_{DD} but as low as approximately $V_{in,CM} - V_{TH}$. In other words, the higher the input CM level, the smaller the allowable output swings. For this reason, it is desirable to choose a relatively low $V_{in,CM}$, but, of course, no less than $V_{GS1} + (V_{GS3} - V_{TH3})$. Such a choice affords a single-ended peak-to-peak output swing of $V_{DD} - (V_{GS1} - V_{TH1}) - (V_{GS3} - V_{TH3})$ (why?). The reader is encouraged to repeat this analysis if the voltage gain is around unity.

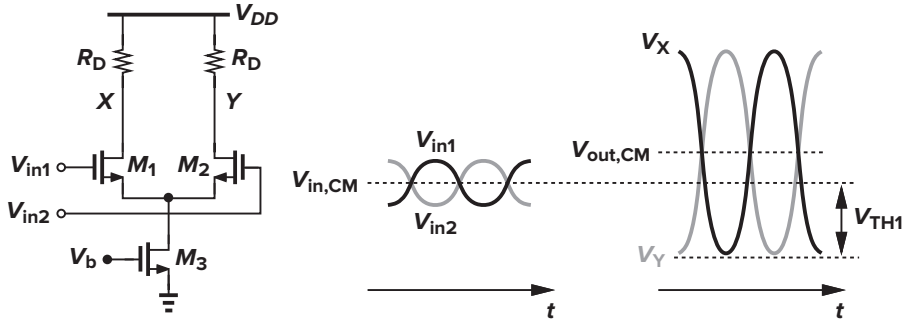


Figure 4.11 Maximum allowable output swings in a differential pair.

▶ **Example 4.3**

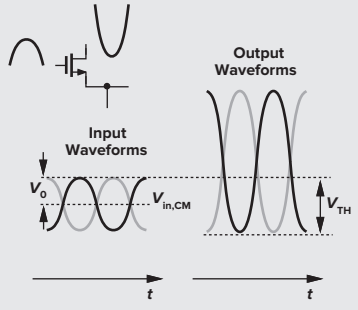
Compare the maximum output voltage swings provided by a CS stage and a differential pair.

Solution

Recall from Chapter 3 that a CS stage (with resistive load) allows an output swing of V_{DD} minus one overdrive ($V_{DD} - V_{D,sat}$). As seen above, with proper choice of the input CM level, a differential pair provides a maximum output swing of V_{DD} minus two overdrives (single-ended) or $2V_{DD}$ minus four overdrives (differential) ($2V_{DD} - 4V_{D,sat}$), which is typically quite a lot larger than $V_{DD} - V_{D,sat}$. ◀

Nanometer Design Notes

Owing to both severe channel-length modulation and limited supply voltages, the voltage gain of nanometer differential pairs hardly exceeds 5. In this case, the peak *input* swing also limits the output swing. As shown below, for a peak input amplitude of V_0, the minimum allowable output is equal to $V_{in,CM} + V_0 - V_{TH}$. This issue arises in any circuit that has a *negative* gain.



4.2.2 Quantitative Analysis

In this section, we quantify both large-signal and small-signal characteristics of MOS differential pairs. We begin with large-signal analysis to arrive at expressions for the plots shown in Fig. 4.8.

Large-Signal Behavior Consider the differential pair shown in Fig. 4.12. Our objective is to determine $V_{out1} - V_{out2}$ as a function of $V_{in1} - V_{in2}$. We have $V_{out1} = V_{DD} - R_{D1}I_{D1}$ and $V_{out2} = V_{DD} - R_{D2}I_{D2}$, that is, $V_{out1} - V_{out2} = R_{D2}I_{D2} - R_{D1}I_{D1} = R_D(I_{D2} - I_{D1})$ if $R_{D1} = R_{D2} = R_D$. Thus, we simply calculate I_{D1} and I_{D2} in terms of V_{in1} and V_{in2}, assuming the circuit is symmetric, M_1 and M_2 are saturated, and $\lambda = 0$. Since the voltage at node P is equal to $V_{in1} - V_{GS1}$ and $V_{in2} - V_{GS2}$,

$$V_{in1} - V_{in2} = V_{GS1} - V_{GS2} \tag{4.2}$$

How does the transconductance of a differential pair compare with that of a common-source stage? For a given *total* bias current, the value of g_m in (4.23) is $1/\sqrt{2}$ times that of a single transistor biased at I_{SS} with the same dimensions. Thus, the total G_m is proportionally less.

Method II If a fully-symmetric differential pair senses differential inputs (i.e., the two inputs change by equal and opposite amounts from the equilibrium condition), then the concept of "half circuit" can be applied. We first prove a lemma.

Lemma Consider the symmetric circuit shown in Fig. 4.20(a), where D_1 and D_2 represent any three-terminal active device. Suppose V_{in1} and V_{in2} change differentially, the former from V_0 to $V_0 + \Delta V_{in}$ and the latter from V_0 to $V_0 - \Delta V_{in}$ [Fig. 4.20(b)]. Then, if the circuit remains linear, V_P does not change. Assume $\lambda = 0$.

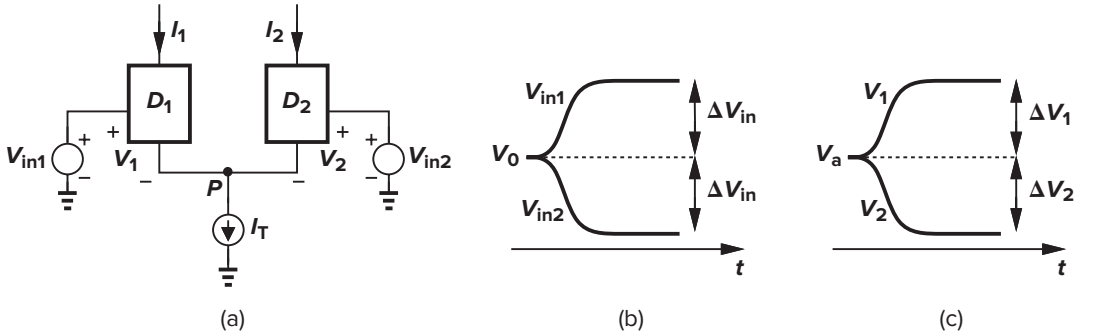


Figure 4.20 Illustration of why node P is a virtual ground.

Proof. The lemma can be proved by invoking symmetry. As long as the operation remains linear, so that the difference between the bias currents of D_1 and D_2 is negligible, the circuit is symmetric. Thus, V_P cannot "favor" the change at one input and "ignore" the other.

From another point of view, the effect of D_1 and D_2 at node P can be represented by Thevenin equivalents (Fig. 4.21). If V_{T1} and V_{T2} change by equal and opposite amounts and R_{T1} and R_{T2} are equal, then V_P remains constant. We emphasize that this is valid if the changes are small enough that we can assume $R_{T1} = R_{T2}$ (e.g., $1/g_{m1} = 1/g_{m2}$).[6] This perspective suggests the lemma's validity even if the tail current source is not ideal. ❑

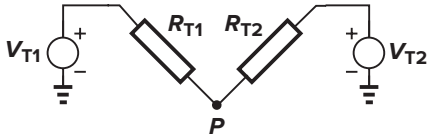


Figure 4.21 Replacing each half of a differential pair by a Thevenin equivalent.

We now offer a more formal proof. Let us assume that V_1 and V_2 have an equilibrium value of V_a and change by ΔV_1 and ΔV_2, respectively [Fig. 4.20(c)]. The output currents therefore change by $g_m \Delta V_1$ and $g_m \Delta V_2$. Since $I_1 + I_2 = I_T$, we have $g_m \Delta V_1 + g_m \Delta V_2 = 0$, i.e., $\Delta V_1 = -\Delta V_2$. We also know that $V_{in1} - V_1 = V_{in2} - V_2$, and hence $V_0 + \Delta V_{in} - (V_a + \Delta V_1) = V_0 - \Delta V_{in} - (V_a + \Delta V_2)$. Consequently, $2\Delta V_{in} = \Delta V_1 - \Delta V_2 = 2\Delta V_1$. In other words, if V_{in1} and V_{in2} change by $+\Delta V_{in}$ and $-\Delta V_{in}$, respectively, then V_1 and V_2 change by the same values, i.e., a differential change in the inputs is simply "absorbed" by V_1 and V_2. In fact, since $V_P = V_{in1} - V_1$, and since V_1 exhibits the same change as V_{in1}, V_P does not change.

[6] It is also possible to derive an expression for the large-signal behavior of V_P and prove that for small $V_{in1} - V_{in2}$, V_P remains constant. We defer this calculation to Chapter 15.

The above lemma greatly simplifies the small-signal analysis of differential amplifiers. As shown in Fig. 4.22, since V_P experiences no change, node P can be considered "ac ground" (or a "virtual ground"), and the circuit can be decomposed into two separate halves. We say that we have applied the "half-circuit concept" [1]. We can write $V_X/V_{in1} = -g_m R_D$ and $V_Y/(-V_{in1}) = -g_m R_D$, where V_{in1} and $-V_{in1}$ denote the voltage *change* on each side. Thus, $(V_X - V_Y)/(2V_{in1}) = -g_m R_D$.

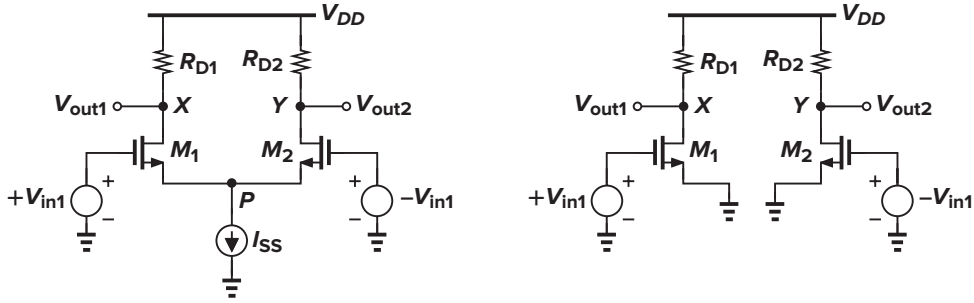


Figure 4.22 Application of the half-circuit concept.

▶ **Example 4.7**

Calculate the differential gain of the circuit of Fig. 4.22(a) if $\lambda \neq 0$.

Solution

Applying the half-circuit concept as illustrated in Fig. 4.23, we have $V_X/V_{in1} = -g_m(R_D \| r_{O1})$ and $V_Y/(-V_{in1}) = -g_m(R_D \| r_{O2})$, thus arriving at $(V_X - V_Y)/(2V_{in1}) = -g_m(R_D \| r_O)$, where $r_O = r_{O1} = r_{O2}$. Note that Method I would require lengthy calculations here.

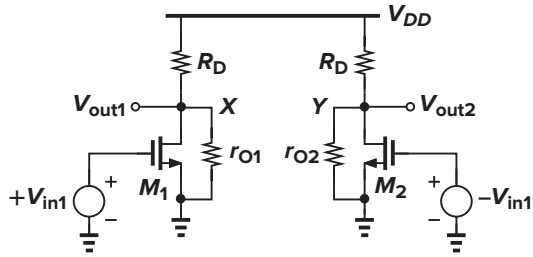


Figure 4.23

◀

The half-circuit concept provides a powerful technique for analyzing symmetric differential pairs with fully differential inputs. But what happens if the two inputs are not fully differential [Fig. 4.24(a)]? As depicted in Figs. 4.24(b) and (c), the two inputs V_{in1} and V_{in2} can be viewed as

$$V_{in1} = \frac{V_{in1} - V_{in2}}{2} + \frac{V_{in1} + V_{in2}}{2} \tag{4.26}$$

$$V_{in2} = \frac{V_{in2} - V_{in1}}{2} + \frac{V_{in1} + V_{in2}}{2} \tag{4.27}$$

Since the second term is common to both inputs, we obtain the equivalent circuit in Fig. 4.24(d), recognizing that the circuit senses a combination of a differential input and a common-mode variation. Therefore, as illustrated in Fig. 4.25, the effect of each type of input can be computed by superposition, with the half-circuit concept applied to the differential-mode operation. We deal with CM analysis in Sec. 4.3.

That is,

$$V_X - V_Y = -g_m(R_D \| r_O)(V_{in1} - V_{in2}) \tag{4.30}$$

which is to be expected.

For common-mode operation, the circuit reduces to that in Fig. 4.26(b). How much do V_X and V_Y change as $V_{in,CM}$ changes? If the circuit is fully symmetric and I_{SS} an ideal current source, the currents drawn by M_1 and M_2 from R_{D1} and R_{D2} are exactly equal to $I_{SS}/2$ and independent of $V_{in,CM}$. Thus, V_X and V_Y remain equal to $V_{DD} - R_D(I_{SS}/2)$ and experience no change as $V_{in,CM}$ varies. Interestingly, the circuit simply amplifies the difference between V_{in1} and V_{in2} while eliminating the effect of $V_{in,CM}$.

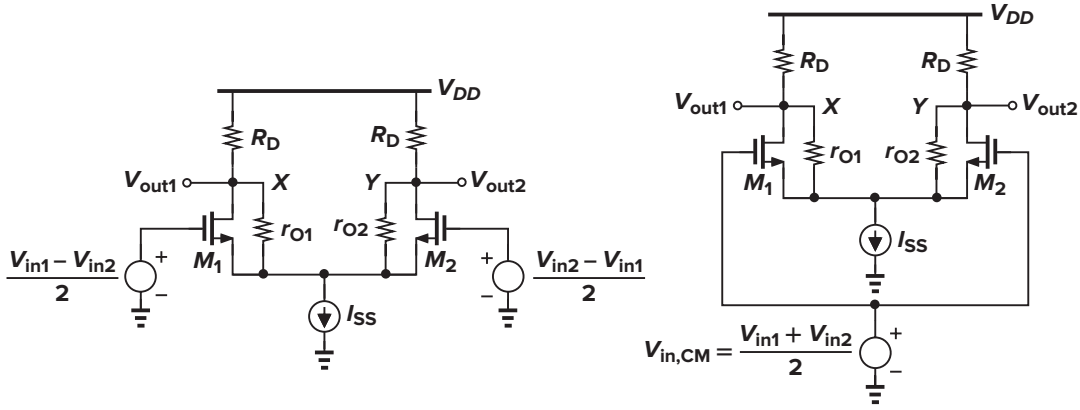


Figure 4.26

4.2.3 Degenerated Differential Pair

As with a simple common-source stage, a differential pair can incorporate resistive degeneration to improve its linearity. Shown in Fig. 4.27(a), such a topology softens the nonlinear behavior of M_1 and M_2 by R_{S1} and R_{S2}. This can be seen from the input-output characteristics of Fig. 4.27(b), where, due to degeneration, the differential voltage necessary to turn off one side increases in magnitude. We can

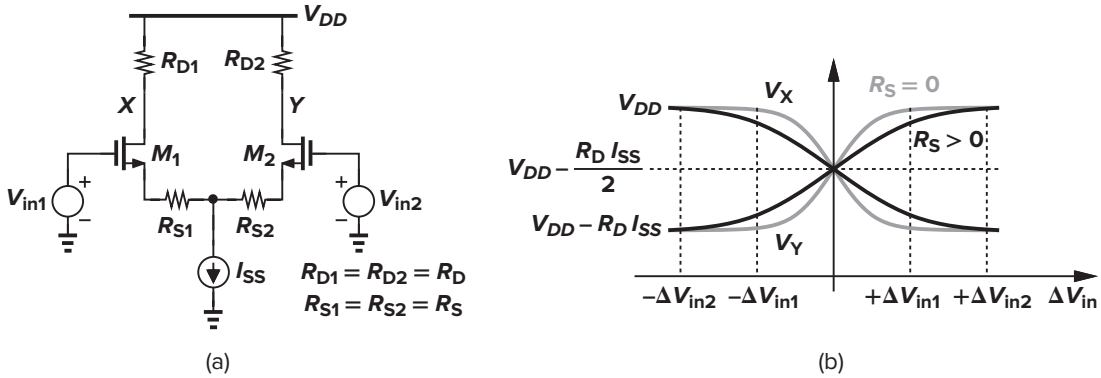


Figure 4.27 (a) Degenerated differential pair, and (b) characteristics with and without degeneration.

4.3 ■ Common-Mode Response

An important attribute of differential amplifiers is their ability to suppress the effect of common-mode perturbations. Example 4.8 portrays an idealized case of common-mode response. In reality, neither is the circuit fully symmetric nor does the current source exhibit an infinite output impedance. As a result, a fraction of the input CM variation appears at the output.

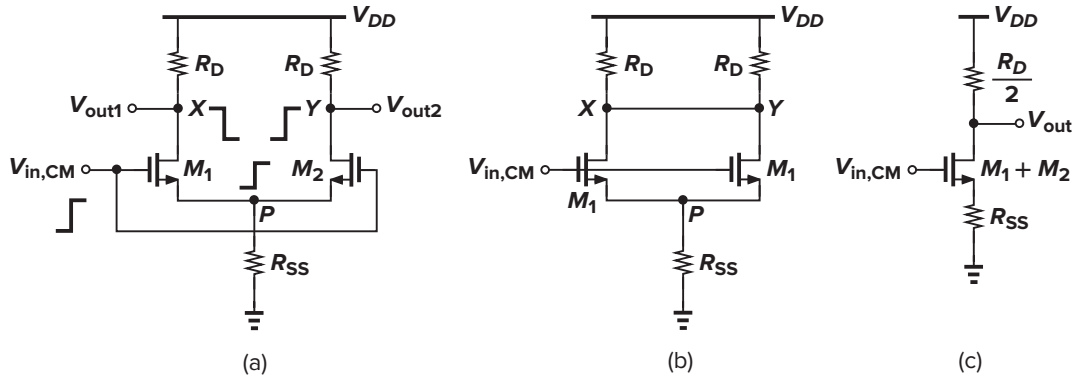


Figure 4.29 (a) Differential pair sensing CM input; (b) simplified version of (a); (c) equivalent circuit of (b).

We first assume that the circuit is symmetric, but the current source has a finite output impedance, R_{SS} [Fig. 4.29(a)]. As $V_{in,CM}$ changes, so does V_P, thereby increasing the drain currents of M_1 and M_2 and lowering both V_X and V_Y. Owing to symmetry, V_X remains equal to V_Y and, as depicted in Fig. 4.29(b), the two nodes can be shorted together. Since M_1 and M_2 are now "in parallel," i.e., they share all of their respective terminals, the circuit can be reduced to that in Fig. 4.29(c). Note that the composite device, $M_1 + M_2$, has twice the width and the bias current of each of M_1 and M_2 and, therefore, twice their transconductance. The "common-mode gain" of the circuit is thus equal to

$$A_{v,CM} = \frac{V_{out}}{V_{in,CM}} \tag{4.36}$$

$$= -\frac{R_D/2}{1/(2g_m) + R_{SS}} \tag{4.37}$$

where g_m denotes the transconductance of each of M_1 and M_2 and $\lambda = \gamma = 0$.

What is the significance of this calculation? In a symmetric circuit, input CM variations disturb the bias points, altering the small-signal gain and possibly limiting the output voltage swings. This can be illustrated by an example.

▶ Example 4.9

The circuit of Fig. 4.30 uses a resistor rather than a current source to define a tail current of 1 mA. Assume that $(W/L)_{1,2} = 25/0.5$, $\mu_n C_{ox} = 50\ \mu$A/V^2, $V_{TH} = 0.6$ V, $\lambda = \gamma = 0$, and $V_{DD} = 3$ V.

(a) What is the required input CM voltage for which R_{SS} sustains 0.5 V?

(b) Calculate R_D for a differential gain of 5.

(c) What happens at the output if the input CM level is 50 mV higher than the value calculated in (a)?

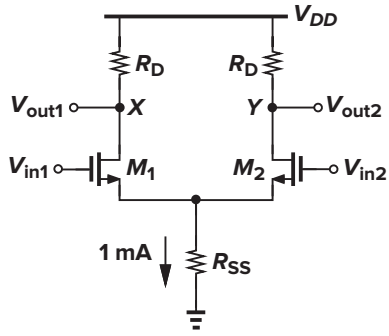


Figure 4.30

Solution

(a) Since $I_{D1} = I_{D2} = 0.5$ mA, we have

$$V_{GS1} = V_{GS2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\dfrac{W}{L}}} + V_{TH} \tag{4.38}$$

$$= 1.23 \text{ V} \tag{4.39}$$

Thus, $V_{in,CM} = V_{GS1} + 0.5 \text{ V} = 1.73$ V. Note that $R_{SS} = 500\ \Omega$.

(b) The transconductance of each device is $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_{D1}} = 1/(632\ \Omega)$, requiring $R_D = 3.16\ \text{k}\Omega$ for a gain of 5.

Note that the output bias level is equal to $V_{DD} - I_{D1}R_D = 1.42$ V. Since $V_{in,CM} = 1.73$ V and $V_{TH} = 0.6$ V, the transistors are 290 mV away from the triode region.

(c) If $V_{in,CM}$ increases by 50 mV, the equivalent circuit of Fig. 4.29(c) suggests that V_X and V_Y drop by

$$|\Delta V_{X,Y}| = \Delta V_{in,CM}\frac{R_D/2}{R_{SS} + 1/(2g_m)} \tag{4.40}$$

$$= 50 \text{ mV} \times 1.94 \tag{4.41}$$

$$= 96.8 \text{ mV} \tag{4.42}$$

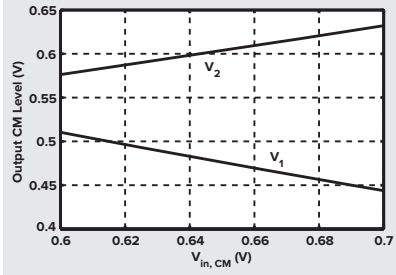
Now, M_1 and M_2 are only 143 mV away from the triode region because the input CM level has increased by 50 mV and the output CM level has decreased by 96.8 mV. ◀

The foregoing discussion indicates that the finite output impedance of the tail current source results in some common-mode gain in a symmetric differential pair. Nonetheless, this is usually a minor concern. More troublesome is the variation of the *differential* output as a result of a change in $V_{in,CM}$, an effect that occurs because in reality the circuit is not fully symmetric, i.e., the two sides suffer from slight mismatches during manufacturing. For example, in Fig. 4.29(a), R_{D1} may not be exactly equal to R_{D2}.

We now study the effect of input common-mode variations if the circuit is asymmetric and the tail current source suffers from a finite output impedance. Suppose, as shown in Fig. 4.31, $R_{D1} = R_D$ and $R_{D2} = R_D + \Delta R_D$, where ΔR_D denotes a small mismatch and the circuit is otherwise symmetric. Assume that $\lambda = \gamma = 0$ for M_1 and M_2. What happens to V_X and V_Y as $V_{in,CM}$ increases? We recognize that M_1 and M_2 operate as one source follower,

Nanometer Design Notes

As a result of the low output impedance of tail current sources in nanometer technologies, a CM level change can "propagate." Plotted below are the output CM levels of two cascaded differential pairs as the main input CM level, $V_{in,CM}$, increases, revealing a drop in the first and a rise in the second.



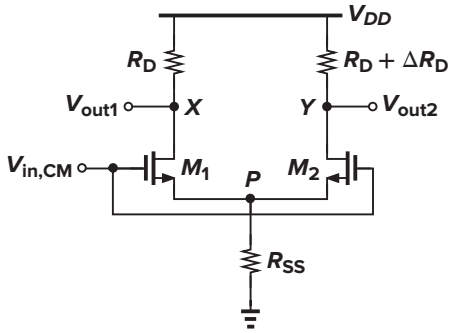


Figure 4.31 Common-mode response in the presence of resistor mismatch.

raising V_P by

$$\Delta V_P = \frac{R_{SS}}{R_{SS} + \dfrac{1}{2g_m}} \Delta V_{in,CM} \tag{4.43}$$

Since M_1 and M_2 are identical, I_{D1} and I_{D2} increase by $[g_m/(1 + 2g_m R_{SS})]\Delta V_{in,CM}$, but V_X and V_Y change by different amounts:

$$\Delta V_X = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} R_D \tag{4.44}$$

$$\Delta V_Y = -\Delta V_{in,CM} \frac{g_m}{1 + 2g_m R_{SS}} (R_D + \Delta R_D) \tag{4.45}$$

Thus, a common-mode change at the input introduces a *differential* component at the output. We say that the circuit exhibits common-mode to differential conversion. This is a critical problem because if the input of a differential pair includes both a differential signal and common-mode noise, the circuit corrupts the amplified differential signal by the input CM change. The effect is illustrated in Fig. 4.32.

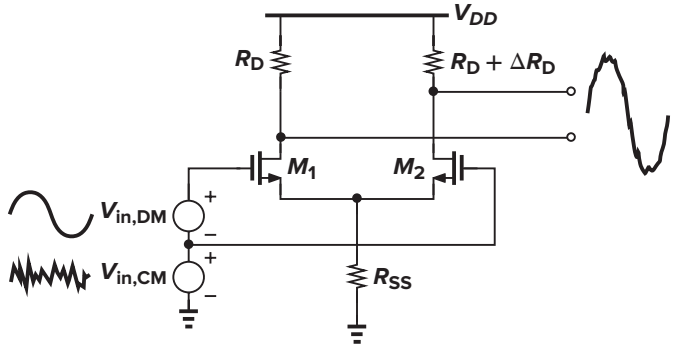


Figure 4.32 Effect of CM noise in the presence of resistor mismatch.

In summary, the common-mode response of differential pairs depends on the output impedance of the tail current source and asymmetries in the circuit, manifesting itself through two effects: variation of the output CM level (in the absence of mismatches) and conversion of input common-mode variations to differential components at the output. In analog circuits, the latter effect is much more severe than the

former. For this reason, the common-mode response should usually be studied with mismatches taken into account.

How significant is common-mode to differential conversion? We make two observations. First, as the *frequency* of the CM disturbance increases, the total capacitance shunting the tail current source introduces larger tail current variations. Thus, even if the output *resistance* of the current source is high, common-mode to differential conversion becomes significant at high frequencies. Shown in Fig. 4.33, this capacitance arises from the parasitics of the current source itself as well as the source-bulk junctions of M_1 and M_2. Second, the asymmetry in the circuit stems from both the load resistors and the input transistors, the latter contributing a typically much greater mismatch.

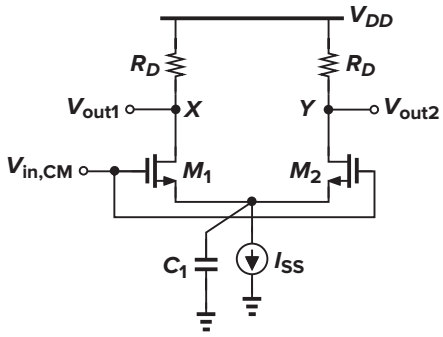


Figure 4.33 CM response with finite tail capacitance.

Let us study the asymmetry resulting from mismatches between M_1 and M_2 in Fig. 4.34(a). Owing to dimension and threshold voltage mismatches, the two transistors carry slightly different currents and exhibit unequal transconductances. We assume that $\lambda = \gamma = 0$. To calculate the small-signal gain from $V_{in,CM}$ to X and Y, we use the equivalent circuit in Fig. 4.34(b), writing $I_{D1} = g_{m1}(V_{in,CM} - V_P)$ and $I_{D2} = g_{m2}(V_{in,CM} - V_P)$. Since $(I_{D1} + I_{D2})R_{SS} = V_P$,

$$(g_{m1} + g_{m2})(V_{in,CM} - V_P)R_{SS} = V_P \tag{4.46}$$

and

$$V_P = \frac{(g_{m1} + g_{m2})R_{SS}}{(g_{m1} + g_{m2})R_{SS} + 1} V_{in,CM} \tag{4.47}$$

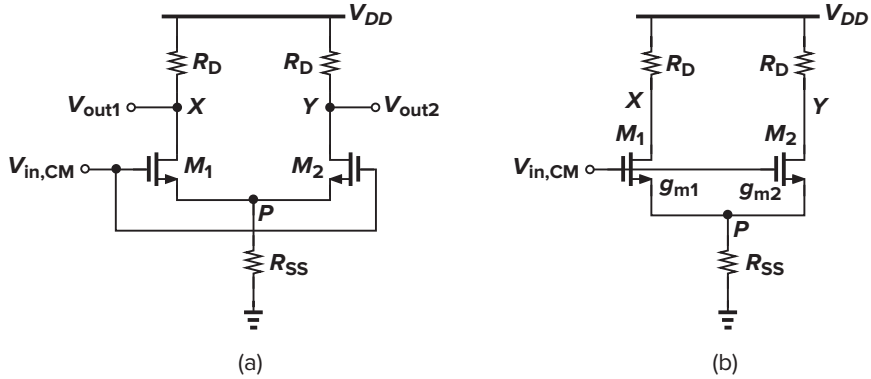


Figure 4.34 (a) Differential pair sensing CM input; (b) equivalent circuit of (a).

We now obtain the output voltages as

$$V_X = -g_{m1}(V_{in,CM} - V_P)R_D \tag{4.48}$$

$$= \frac{-g_{m1}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM} \tag{4.49}$$

and

$$V_Y = -g_{m2}(V_{in,CM} - V_P)R_D \tag{4.50}$$

$$= \frac{-g_{m2}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM} \tag{4.51}$$

The differential component at the output is therefore given by

$$V_X - V_Y = -\frac{g_{m1} - g_{m2}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D V_{in,CM} \tag{4.52}$$

In other words, the circuit converts input CM variations to a differential error by a factor equal to

$$A_{CM-DM} = -\frac{\Delta g_m R_D}{(g_{m1} + g_{m2})R_{SS} + 1} \tag{4.53}$$

where A_{CM-DM} denotes common-mode to differential-mode conversion and $\Delta g_m = g_{m1} - g_{m2}$.

▶ Example 4.10

Two differential pairs are cascaded as shown in Fig. 4.35. Transistors M_3 and M_4 suffer from a g_m mismatch of Δg_m, the total parasitic capacitance at node P is represented by C_P, and the circuit is otherwise symmetric. What fraction of the supply noise appears as a differential component at the output? Assume that $\lambda = \gamma = 0$.

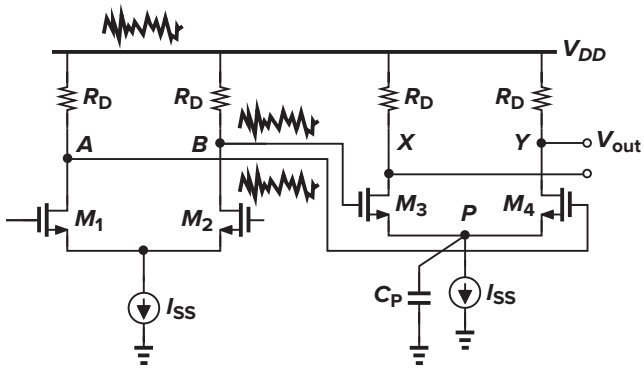


Figure 4.35

Solution

Neglecting the capacitance at nodes A and B, we note that the supply noise appears at these nodes with no attenuation. Substituting $1/(C_P s)$ for R_{SS} in (4.53) and taking the magnitude, we have

$$|A_{CM-DM}| = \frac{\Delta g_m R_D}{\sqrt{1 + (g_{m3} + g_{m4})^2 \left| \frac{1}{C_P \omega} \right|^2}} \tag{4.54}$$

The key point is that the effect becomes more noticeable as the supply noise frequency, ω, increases. ◀

For a meaningful comparison of differential circuits, the undesirable differential component produced by CM variations must be normalized to the wanted differential output resulting from amplification. We define the "common-mode rejection ratio" (CMRR) as the desired gain divided by the undesired gain:

$$\text{CMRR} = \left| \frac{A_{DM}}{A_{CM-DM}} \right| \tag{4.55}$$

If only g_m mismatch is considered, the reader can show from the analysis of Fig. 4.17 that

$$|A_{DM}| = \frac{R_D}{2} \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{1 + (g_{m1} + g_{m2})R_{SS}} \tag{4.56}$$

and hence

$$\text{CMRR} = \frac{g_{m1} + g_{m2} + 4g_{m1}g_{m2}R_{SS}}{2\Delta g_m} \tag{4.57}$$

$$\approx \frac{g_m}{\Delta g_m}(1 + 2g_m R_{SS}) \tag{4.58}$$

where g_m denotes the mean value, that is, $g_m = (g_{m1} + g_{m2})/2$. In practice, all mismatches must be taken into account. Note that $2g_m R_{SS} \gg 1$, and hence CMRR $\approx 2g_m^2 R_{SS}/\Delta g_m$.

▶ **Example 4.11**

Our studies suggest that an ideal tail current source guarantees infinite CM rejection. Is this always true?

Solution

Interestingly, it is not. If the two transistors exhibit body-effect mismatch, then the circuit still converts an input CM change to a differential output component even if the tail impedance is infinite. As illustrated in Fig. 4.36, a change in $V_{in,CM}$ produces a change in V_P, and hence in V_{BS} of both transistors. If $g_{mb1} \neq g_{mb2}$, the change in $I_{D1}(= g_{mb1}V_{BS1})$ is not equal to that in I_{D2}, yielding a differential change at the output.

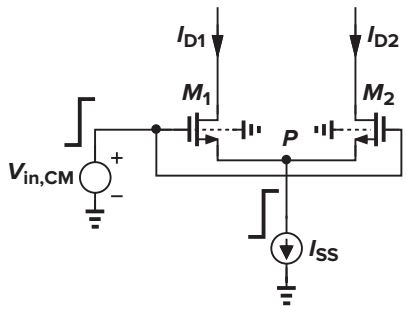


Figure 4.36

◀

4.4 ■ Differential Pair with MOS Loads

The load of a differential pair need not be implemented by linear resistors. As with the common-source stages studied in Chapter 3, differential pairs can employ diode-connected or current-source loads (Fig. 4.37). The small-signal differential gain can be derived using the half-circuit concept. For Fig. 4.37(a),

$$A_v = -g_{mN}\left(g_{mP}^{-1} \| r_{ON} \| r_{OP}\right) \tag{4.59}$$

$$\approx -\frac{g_{mN}}{g_{mP}} \tag{4.60}$$

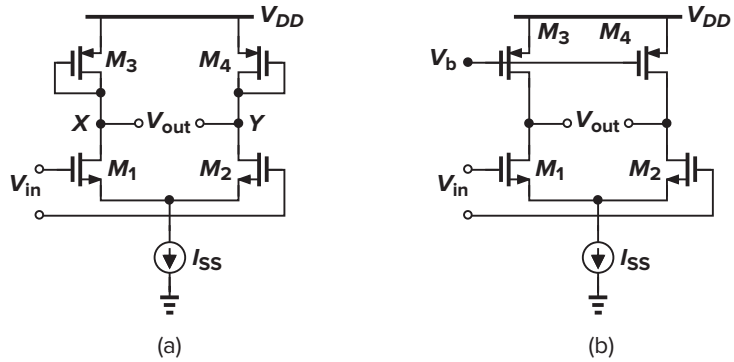


Figure 4.37 Differential pair with (a) diode-connected and (b) current-source loads.

where the subscripts N and P denote NMOS and PMOS, respectively. Expressing g_{mN} and g_{mP} in terms of device dimensions, we have

$$A_v \approx -\sqrt{\frac{\mu_n (W/L)_N}{\mu_p (W/L)_P}} \tag{4.61}$$

For Fig. 4.37(b), we have

$$A_v = -g_{mN}(r_{ON} \| r_{OP}) \tag{4.62}$$

▶ **Example 4.12**

It is possible to obviate the need for V_b in the circuit of Fig. 4.37(b) as shown in Fig. 4.38(a), where R_1 and $R_2 (= R_1)$ are relatively large. In the absence of signals, $V_X = V_Y = V_N = V_{DD} - |V_{GS3,4}|$. That is, M_3 and M_4 are "self-biased." Determine the differential voltage gain of this topology.

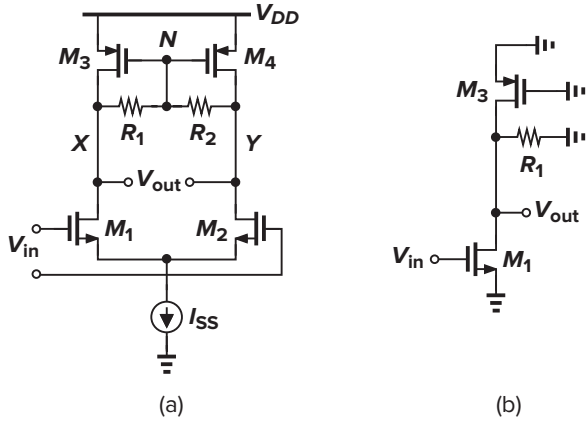


Figure 4.38

Solution

For differential outputs, V_N does not change (why?) and can be considered ac ground. Shown in Fig. 4.38(b), the half-circuit yields

$$|A_v| = g_{m1}(r_{O1} \| R_1 \| r_{O3}) \tag{4.63}$$

If the resistors are much greater than $r_{O1} || r_{O3}$, then they negligibly reduce the gain. ◀

References

[1] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 3d ed. (New York: Wiley, 1993).
[2] B. Gilbert, "A Precise Four-Quadrant Multiplier with Subnanosecond Response," *IEEE J. Solid-State Circuits*, vol. SC-3, pp. 365–373, Dec. 1968.

Problems

Unless otherwise stated, in the following problems, use the device data shown in Table 2.1 and assume that $V_{DD} = 3$ V where necessary. All device dimensions are effective values and in microns.

4.1. Suppose the total capacitance between adjacent lines in Fig. 4.2 is 10 fF and the capacitance from the drains of M_1 and M_2 to ground is 100 fF.
(a) What is the amplitude of the glitches in the analog output in Fig. 4.2(a) for a clock swing of 3 V?
(b) If in Fig. 4.2(b), the capacitance between L_1 and L_2 is 10% less than that between L_1 and L_3, what is the amplitude of the glitches in the differential analog output for a clock swing of 3 V?

4.2. Sketch the small-signal differential voltage gain of the circuit shown in Fig. 4.9(a) if V_{DD} varies from 0 to 3 V. Assume that $(W/L)_{1-3} = 50/0.5$, $V_{in,CM} = 1.3$ V, and $V_b = 1$ V.

4.3. Construct the plots of Fig. 4.9(c) for a differential pair using PMOS transistors.

4.4. In the circuit of Fig. 4.11, $(W/L)_{1,2} = 50/0.5$ and $I_{SS} = 0.5$ mA.
(a) What is the maximum allowable output voltage swing if $V_{in,CM} = 1.2$ V?
(b) What is the voltage gain under this condition?

4.5. A differential pair uses input NMOS devices with $W/L = 50/0.5$ and a tail current of 1 mA.
(a) What is the equilibrium overdrive voltage of each transistor?
(b) How is the tail current shared between the two sides if $V_{in1} - V_{in2} = 50$ mA?
(c) What is the equivalent G_m under this condition?
(d) For what value of $V_{in1} - V_{in2}$ does the G_m drop by 10%? By 90%?

4.6. Repeat Problem 4.5 with $W/L = 25/0.5$ and compare the results.

4.7. Repeat Problem 4.5 with a tail current of 2 mA and compare the results.

4.8. Sketch I_{D1} and I_{D2} in Fig. 4.19 versus $V_{in1} - V_{in2}$. For what value of $V_{in1} - V_{in2}$ are the two currents equal?

4.9. Consider the circuit of Fig. 4.32, assuming $(W/L)_{1,2} = 50/0.5$ and $R_D = 2$ kΩ. Suppose R_{SS} represents the output impedance of an NMOS current source with $(W/L)_{SS} = 50/0.5$ and a drain current of 1 mA. The input signal consists of $V_{in,DM} = 10\ \text{mV}_{pp}$ and $V_{in,CM} = 1.5\ \text{V} + V_n(t)$, where $V_n(t)$ denotes noise with a peak-to-peak amplitude of 100 mV. Assume that $\Delta R/R = 0.5\%$.
(a) Calculate the output differential signal-to-noise ratio, defined as the signal amplitude divided by the noise amplitude.
(b) Calculate the CMRR.

4.10. Repeat Problem 4.9 if $\Delta R = 0$, but M_1 and M_2 suffer from a threshold voltage mismatch of 1 mV.

4.11. Suppose the differential pair of Fig. 4.37(a) is designed with $(W/L)_{1,2} = 50/0.5$, $(W/L)_{3,4} = 10/0.5$, and $I_{SS} = 0.5$ mA. Also, I_{SS} is implemented with an NMOS device having $(W/L)_{SS} = 50/0.5$.
(a) What are the minimum and maximum allowable input CM levels if the differential swings at the input and output are small?
(b) For $V_{in,CM} = 1.2$ V, sketch the small-signal differential voltage gain as V_{DD} goes from 0 to 3 V.

4.12. In Problem 4.11, suppose M_1 and M_2 have a threshold voltage mismatch of 1 mV. What is the CMRR?

4.13. In Problem 4.11, suppose $W_3 = 10\ \mu$m, but $W_4 = 11\ \mu$m. Calculate the CMRR.

4.14. For the differential pairs of Fig. 4.37(a) and (b), calculate the differential voltage gain if $I_{SS} = 1$ mA, $(W/L)_{1,2} = 50/0.5$, and $(W/L)_{3,4} = 50/1$. What is the minimum allowable input CM level if I_{SS} requires at least 0.4 V across it? Using this value for $V_{in,CM}$, calculate the maximum output voltage swing in each case.

4.15. In the circuit of Fig. 4.39(a), assume that $I_{SS} = 1$ mA and $W/L = 50/0.5$ for all the transistors.
(a) Determine the voltage gain.
(b) Calculate V_b such that $I_{D5} = I_{D6} = 0.8(I_{SS}/2)$.
(c) If I_{SS} requires a minimum voltage of 0.4 V, what is the maximum differential output swing?

4.16. Assuming that all the circuits shown in Fig. 4.44 are symmetric, sketch V_{out} as **(a)** V_{in1} and V_{in2} vary differentially from zero to V_{DD}, and **(b)** V_{in1} and V_{in2} are equal and vary from zero to V_{DD}.

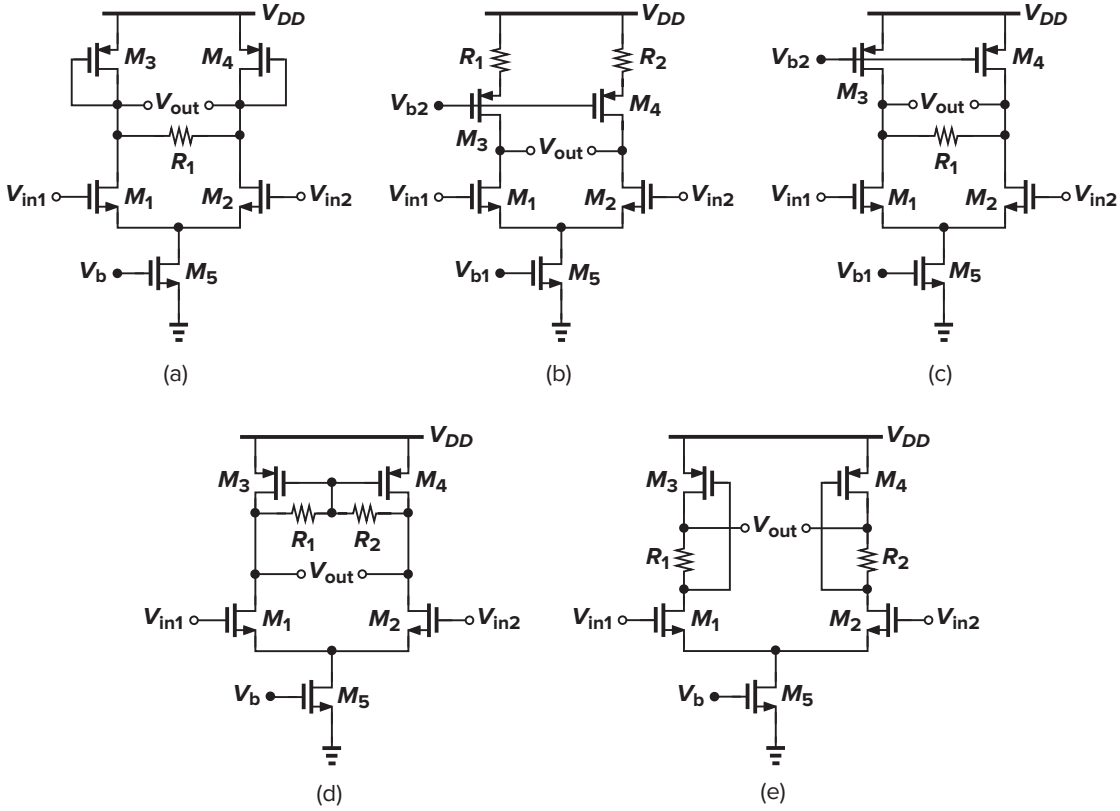


Figure 4.44

4.17. Assuming that all the circuits shown in Fig. 4.45 are symmetric, sketch V_{out} as **(a)** V_{in1} and V_{in2} vary differentially from zero to V_{DD}, and **(b)** V_{in1} and V_{in2} are equal and vary from zero to V_{DD}.

4.18. Assuming that all the transistors in the circuits of Figs. 4.44 and 4.45 are saturated and $\lambda \neq 0$, calculate the small-signal differential voltage gain of each circuit.

4.19. Consider the circuit shown in Fig. 4.46.
(a) Sketch V_{out} as V_{in1} and V_{in2} vary differentially from zero to V_{DD}.
(b) If $\lambda = 0$, obtain an expression for the voltage gain. What is the voltage gain if $W_{3,4} = 0.8W_{5,6}$?

4.20. For the circuit shown in Fig. 4.47,
(a) Sketch V_{out}, V_X, and V_Y as V_{in1} and V_{in2} vary differentially from zero to V_{DD}.
(b) Calculate the small-signal differential voltage gain.

4.21. Assuming no symmetry in the circuit of Fig. 4.48 and using no equivalent circuits, calculate the small-signal voltage gain $(V_{out})/(V_{in1} - V_{in2})$ if $\lambda = 0$ and $\gamma \neq 0$.

4.22. Due to a manufacturing defect, a large parasitic resistance has appeared between the drain and source terminals of M_1 in Fig. 4.49. Assuming $\lambda = \gamma = 0$, calculate the small-signal gain, common-mode gain, and CMRR.

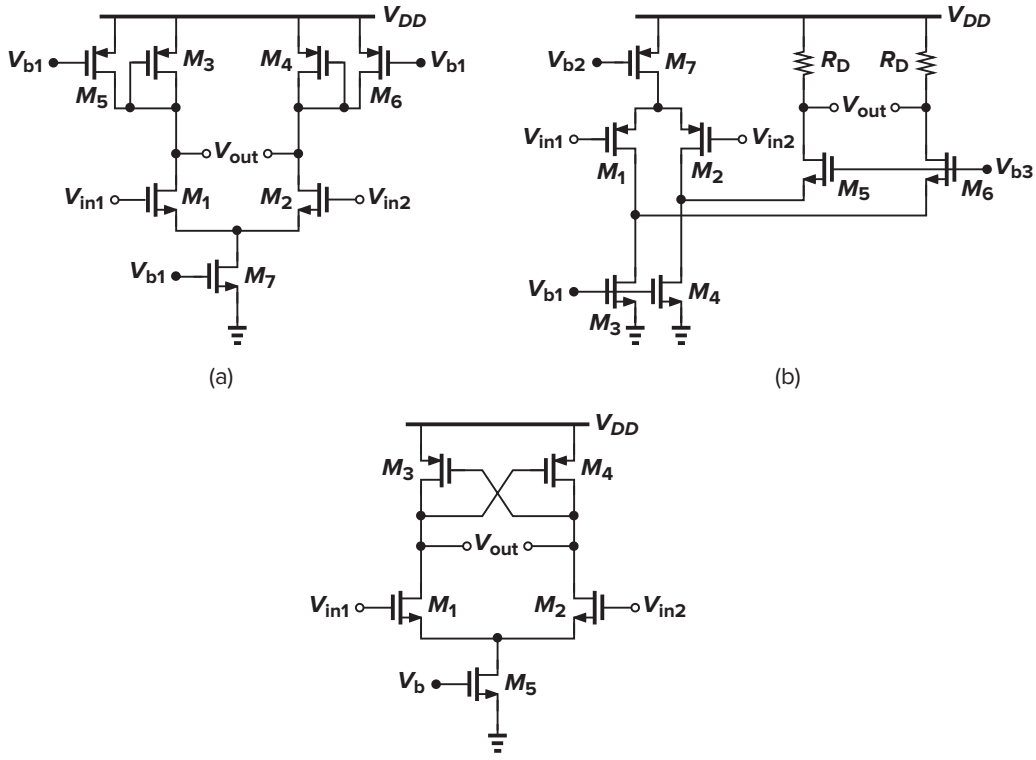


Figure 4.45

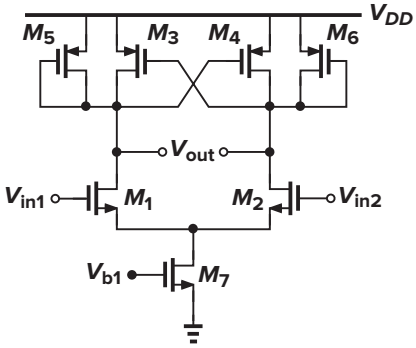


Figure 4.46

4.23. Due to a manufacturing defect, a large parasitic resistance has appeared between the drains of M_1 and M_4 in the circuit of Fig. 4.50. Assuming $\lambda = \gamma = 0$, calculate the small-signal gain, common-mode gain, and CMRR.

4.24. In the circuit of Fig. 4.51, all of the transistors have a W/L of 50/0.5, and M_3 and M_4 are to operate in the deep triode region with an on-resistance of 2 kΩ. Assuming that $I_{D5} = 20\ \mu$A and $\lambda = \gamma = 0$, calculate the input common-mode level that yields such resistance. Sketch V_{out1} and V_{out2} as V_{in1} and V_{in2} vary differentially from 0 to V_{DD}.

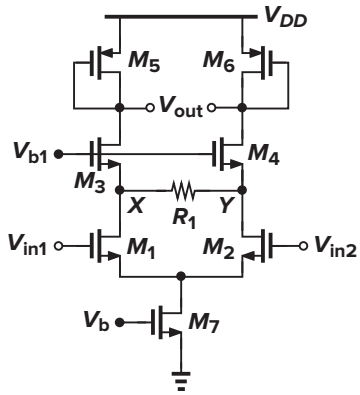


Figure 4.47

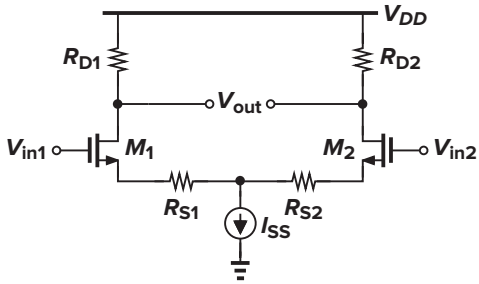


Figure 4.48

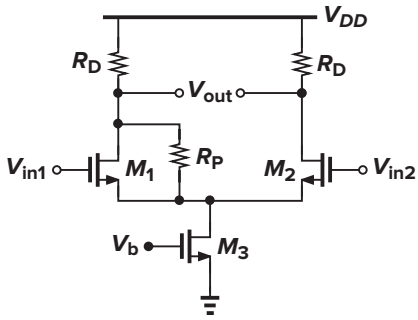


Figure 4.49

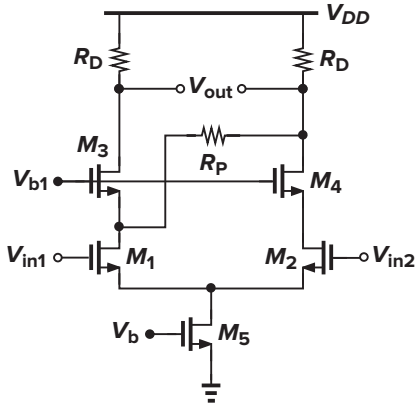


Figure 4.50

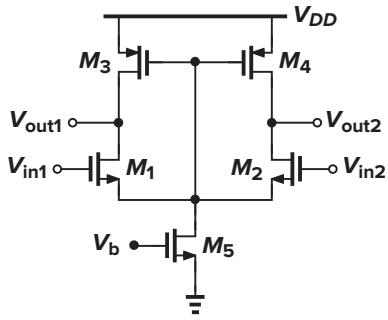


Figure 4.51

4.25. In the circuit of Fig. 4.37(b), $(W/L)_{1-4} = 50/0.5$ and $I_{SS} = 1$ mA.
(a) What is the small-signal differential gain?
(b) For $V_{in,CM} = 1.5$ V, what is the maximum allowable output voltage swing?

4.26. In the circuit of Fig. 4.39, assume that M_5 and M_6 have a small threshold voltage mismatch of ΔV and I_{SS} has an output impedance R_{SS}. Calculate the CMRR.

4.27. What happens if R_{SS} in Eq. (4.56) becomes very large? Can we obtain the same result by analyzing a differential pair having an ideal tail current source but $g_{m1} \neq g_{m2}$?

4.28. In Example 4.5, how much input dc imbalance can be tolerated if the small-signal gain must not drop by more than 5%?

4.29. In the lemma illustrated in Fig. 4.20, suppose channel-length modulation is not neglected. Assuming the two devices are connected to two equal load resistors, explain intuitively why the lemma still holds.

4.30. Does the lemma in Fig. 4.20 still hold if the devices have body effect? Explain.

4.31. Repeat Example 4.7 using Method I.

4.32. Prove the lemma illustrated in Fig. 4.20 if the tail current source is replaced by a resistor R_T.

4.33. What happens to the plots on Fig. 4.13 as W/L increases? Determine the area under the G_m plot and use the result to explain why the peak G_m must increase as W/L increases.

4.34. Assuming that I_1 and I_{SS} in Fig. 4.52 are ideal and $\lambda, \gamma > 0$, determine V_{out1}/V_{in} and V_{out2}/V_{in}.

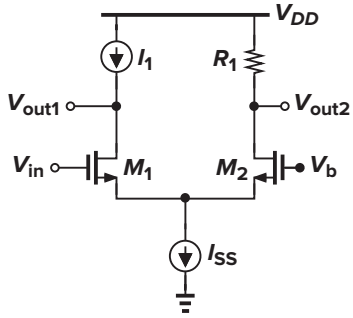


Figure 4.52

4.35. In Problem 4.11, suppose M_3 and M_4 have a threshold voltage mismatch of 1 mV. Calculate the CMRR.