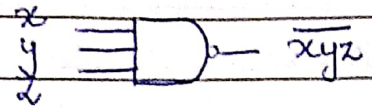
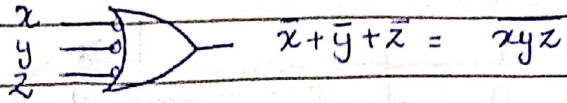
DATE

NAND & NOR Implementation. (Two-Level Implementation)

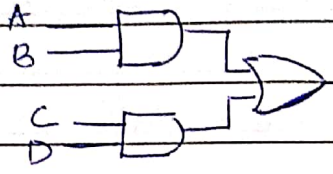
(a) AND-Invert



(b) Invert-OR

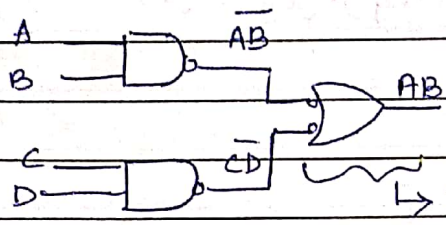


Eg 1 $F = AB + CD$

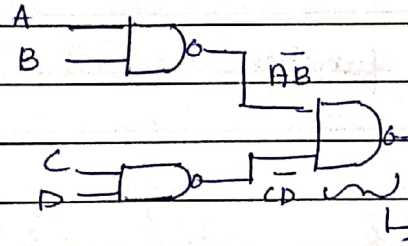


} using basic gates

(a)



(b)

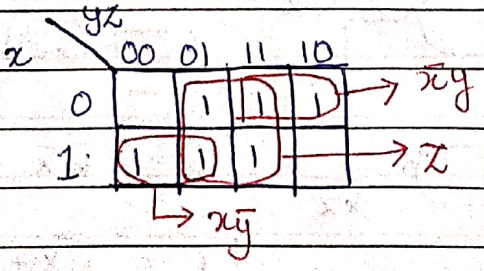


$(\overline{AB}) \cdot (\overline{CD}) = \overline{\overline{AB}} + \overline{\overline{CD}} = AB + CD$.

Eg 2 Implement the following Boolean function with NAND gates.

$F(x,y,z) = (1,2,3,4,5,7)$

* Use K-map and simplify the function into Sum-of-Product form.



$F = x\bar{y} + \bar{x}y + z$.

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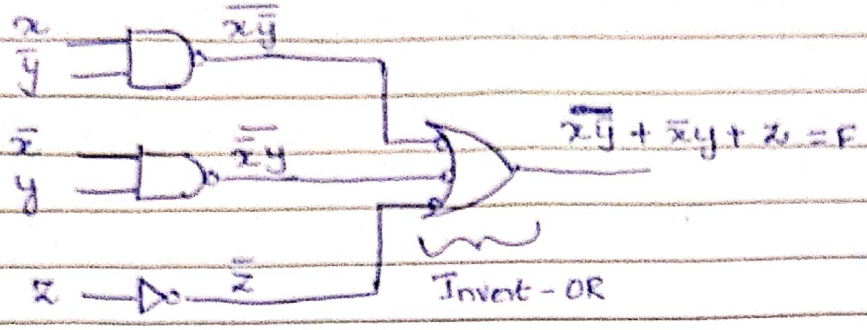
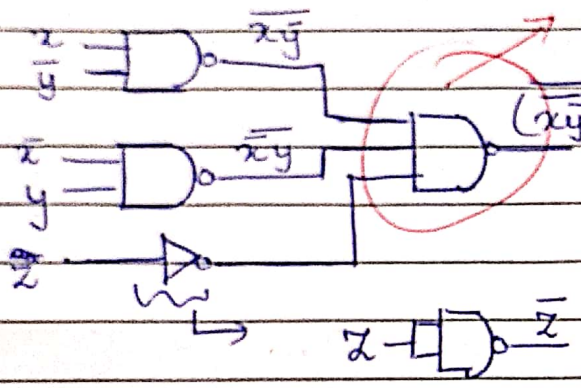
$F = x\bar{y} + \bar{x}y + z$





$= \overline{x\bar{y}} + \overline{\bar{x}y} + \bar{z}$

$= x\bar{y} + \bar{x}y + z$

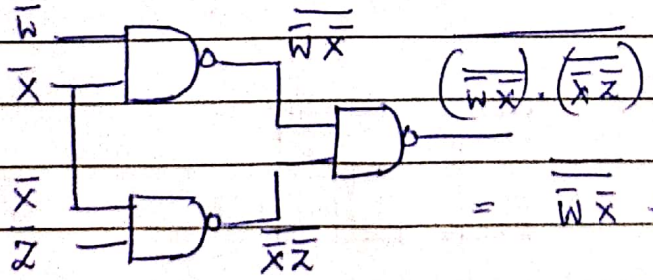
Eg 3 : Implement the function $F = \bar{w}\bar{x} + \bar{x}\bar{z}$ using only NAND gates.

$F = \bar{w}\bar{x} + \bar{x}\bar{z}$

Taking double complement on both sides.

$$\bar{\bar{F}} = \overline{\bar{w}\bar{x} + \bar{x}\bar{z}}$$

$$= \overline{(\bar{w}\bar{x})\cdot(\bar{x}\bar{z})}$$



$= \overline{\bar{w}\bar{x}} + \overline{\bar{x}\bar{z}}$

$$\boxed{F = \bar{w}\bar{x} + \bar{x}\bar{z}}$$

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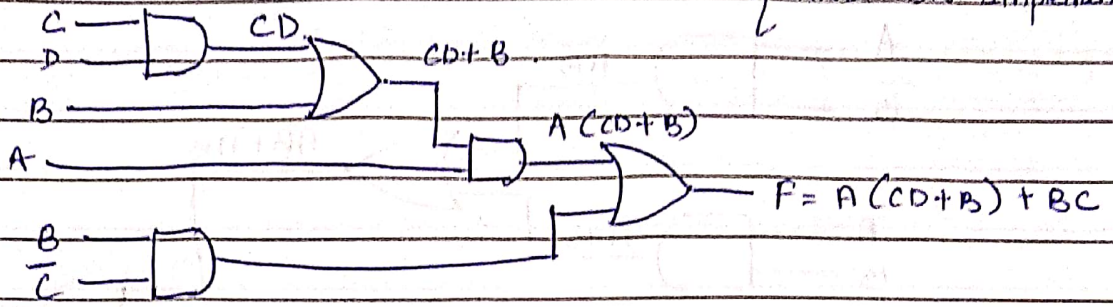
Multi level NAND Circuits

Eg:- 1 $F = A(CD + B) + B\bar{C}$

{ AND - OR Implementation

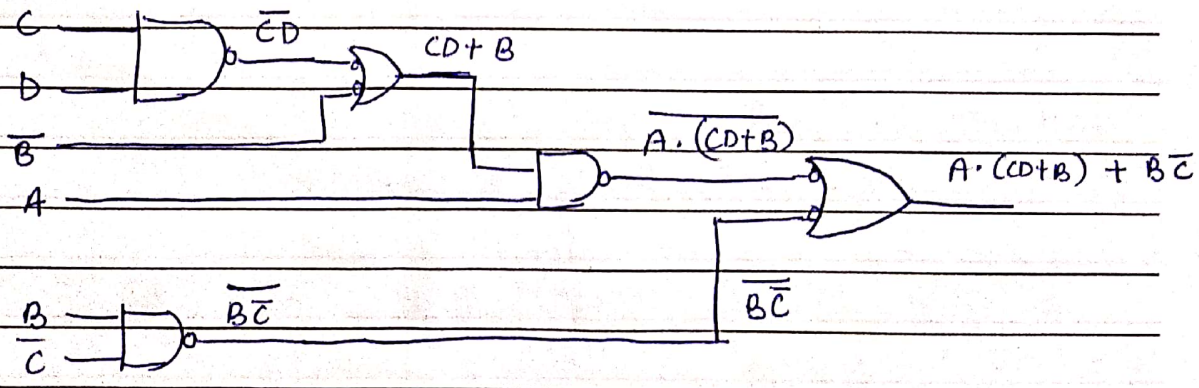


* Procedure to Convert AND-OR diagram into an NAND diagram is as follows-

1. Convert all AND gates to NAND gates with AND-invert graphic symbols.

2. Convert all OR gates to NAND gates with invert-OR graphic symbols.

3. Check all the bubbles in the diagram. For every bubble that is not compensated by another small circle along the same line, insert an inverter.



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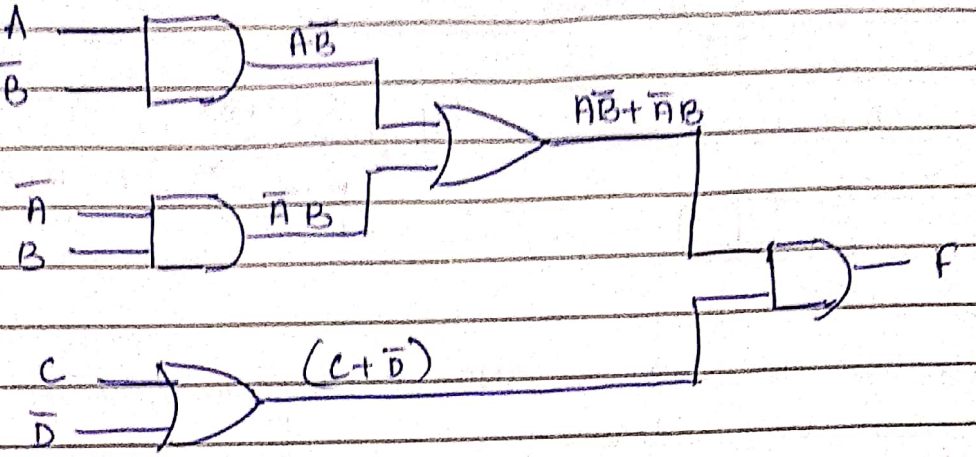
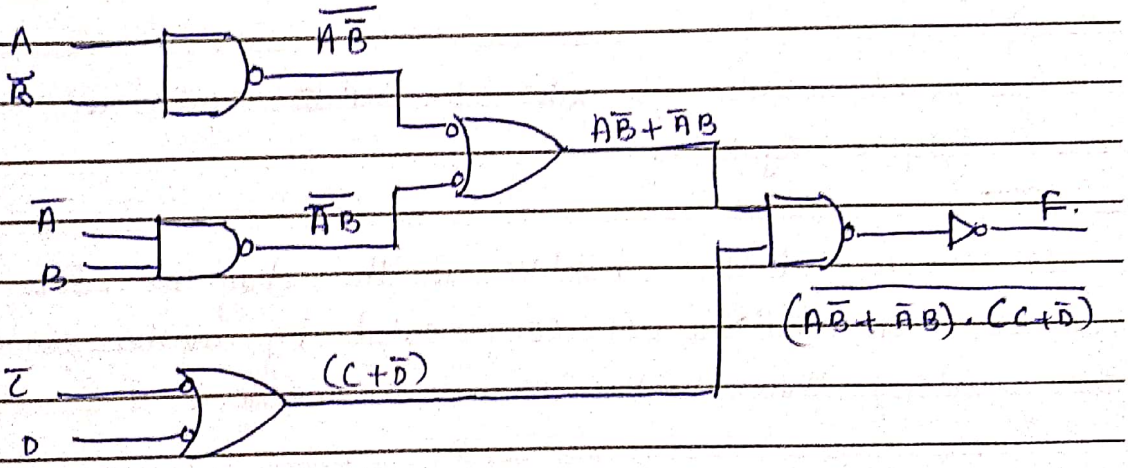
Eg 3 $F = (A\bar{B} + \bar{A}B)(C + \bar{D})$

AND - OR gates

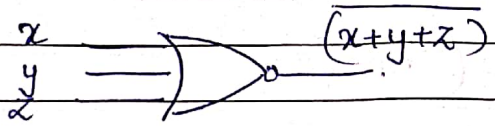


NAND gates.

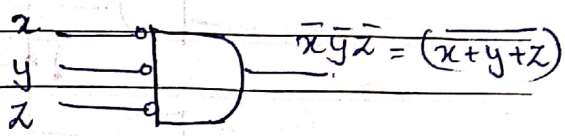


NOR Implementation.

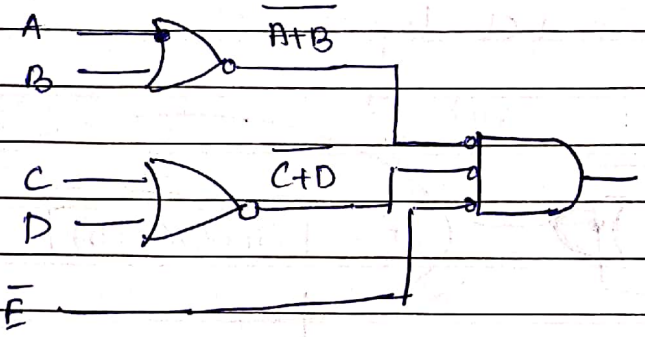
(a) OR - Invert



(b) Invert - AND.



Eg $F = (A+B)(C+D)E$



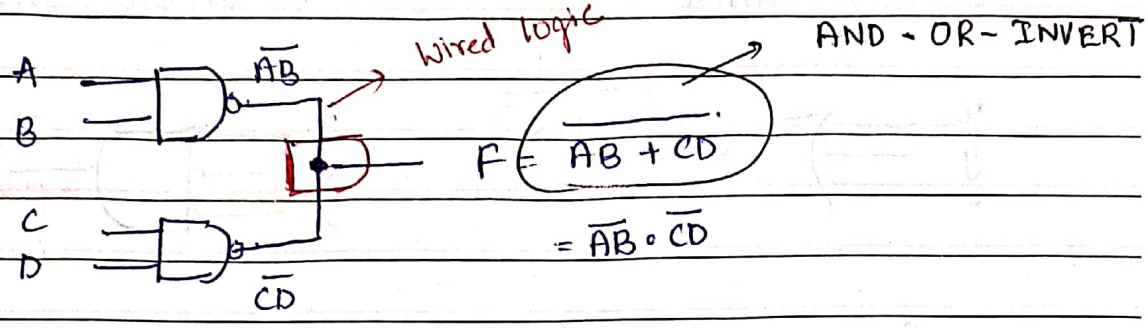
OTHER TWO LEVEL IMPLEMENTATION.

Some NAND or NOR gates allow the possibility of a wire connection between the outputs of two logic functions. This type of logic is called wired Logic.

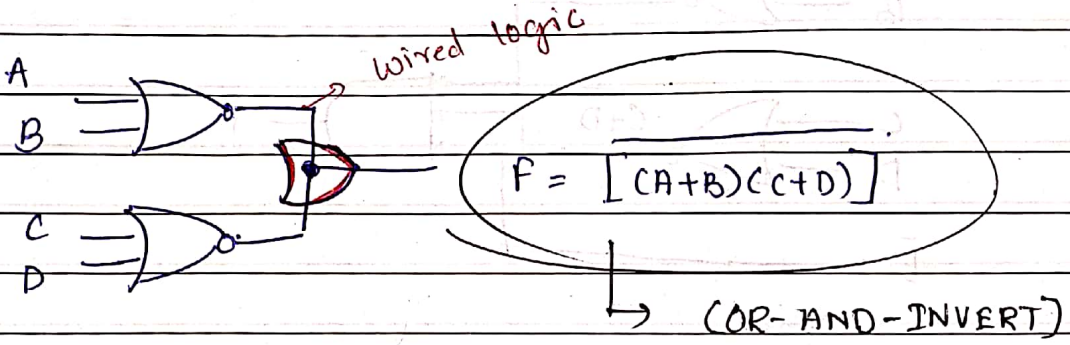
Example:

1. TTL NAND gates when tied togather performs a wired - AND logic.
2. The NOR outputs of ECL gates can be tied togather to perform a wired - OR logic.

(a) A wired TTL NAND gate



(b) Wired - OR in ECL logic



TTL → Transistor Transistor Logic } → Transistor logic families.
ECL → Emitter Coupled Logic

Note:

A wired - Logic does not produce a physical second - level gate, since it is just a wire connection.

Nondegenerate Forms.

When we talk about the two-level combinations. We consider four types of gates

1. AND
2. OR
3. NAND
4. NOR.

} Total no of combinations we get for a two level combination are 16, since we have four gates.

$2^4 = 16$

4 → no of gates

2 → no of level [We consider two level combination]

For combinations such as ~~AND - AND~~, ~~OR - OR~~ :-
It degenerates into single operation.

* Hence 8 Combinations become degenerate forms
* Will the rest 8 Combinations fall under non-degenerate forms.

The eight nondegenerate forms are

AND - OR	~~OR - AND~~
~~NAND - NAND~~	~~AND - NAND~~
NOR - OR	~~OR - NOR~~.
OR - NAND	~~NAND -~~

AND - OR	OR - AND
NAND - NAND	NOR - NOR
NOR - OR	NAND - AND
OR - NAND	AND - NOR

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1) Combinational GATE

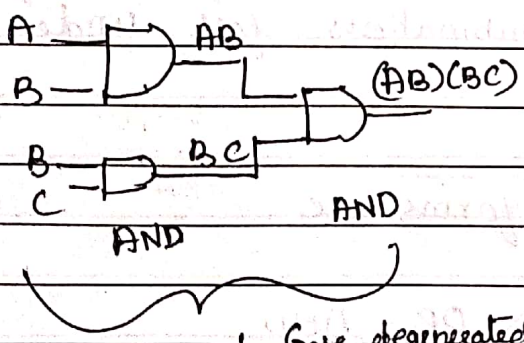
AND – AND
AND – OR ✓
AND – NAND
AND – NOR ✓

OR – AND ✓
OR – OR
OR – NAND ✓
OR – NOR

NAND – AND ✓
NAND – OR
NAND – NAND ✓
NAND – NOR

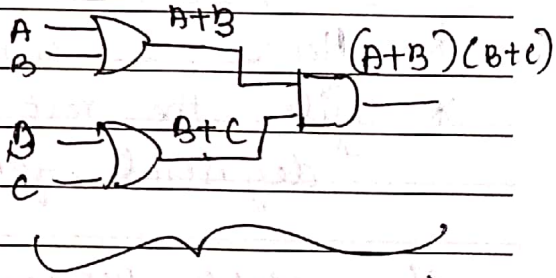
NOR – AND
NOR – OR ✓
NOR – NAND
NOR – NOR ✓

Degenerate forms
↳ Because they degenerate into a single operation.



↳ Gets degenerated into single operation

OR – AND.

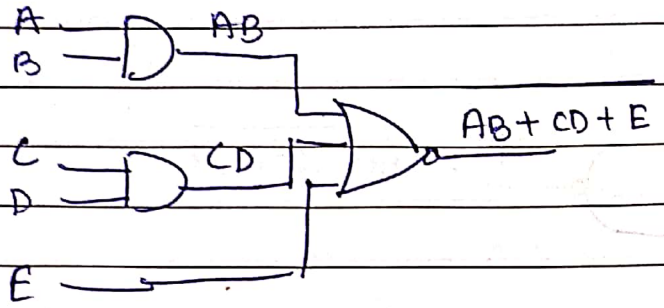


↳ It will not get degenerated into single operation (Non-degenerate form).

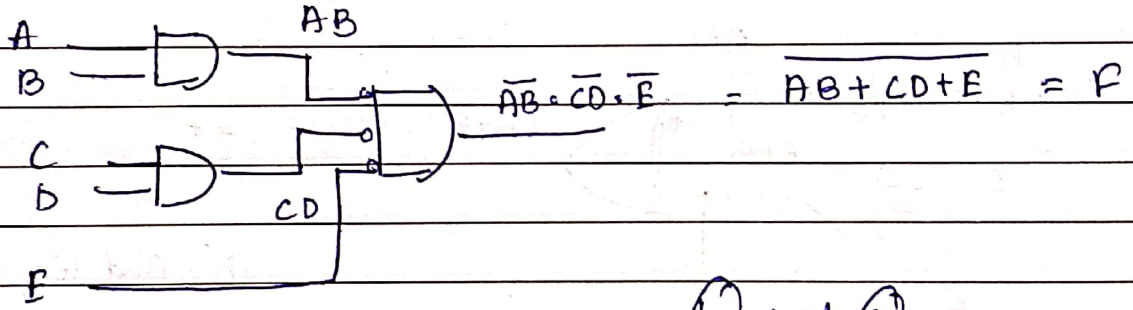
AND - OR - INVERT Implementation.

$$F = \overline{(AB + CD + E)}$$

(a) AND - NOR.

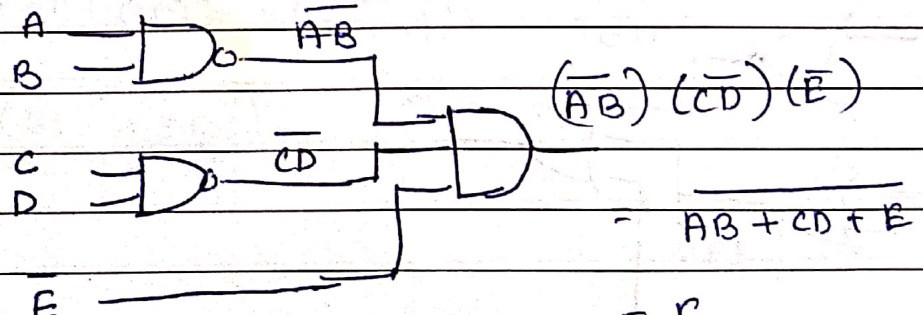


(b) AND - NOR.



(b) and (c) are equivalent Nondegenerate forms.

(c) NAND - AND



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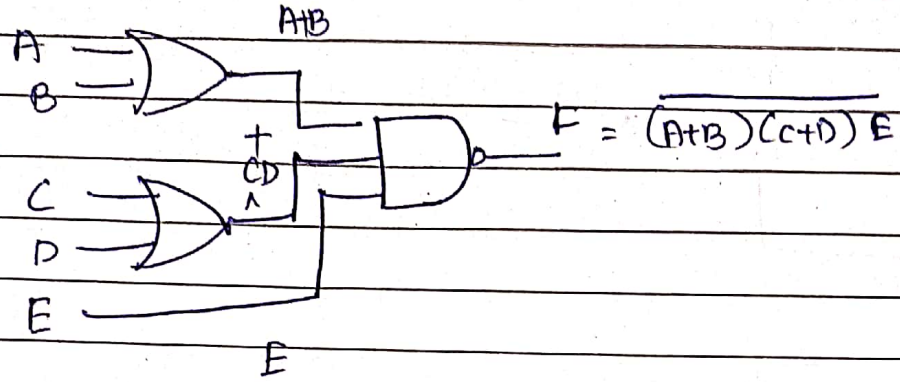
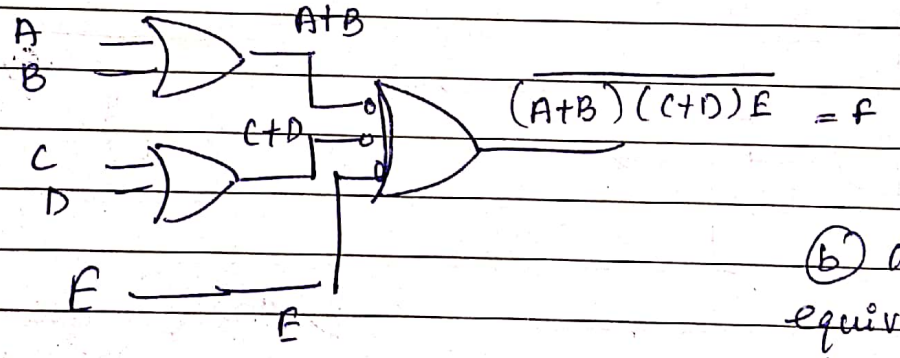
OR-AND-INVERT

$$F = [(A+B)(C+D)E]$$

(a) OR-NAND.



(b) OR-NAND.



(b) and (c) are equivalent non degenerate forms.

(c) NOR-OR.