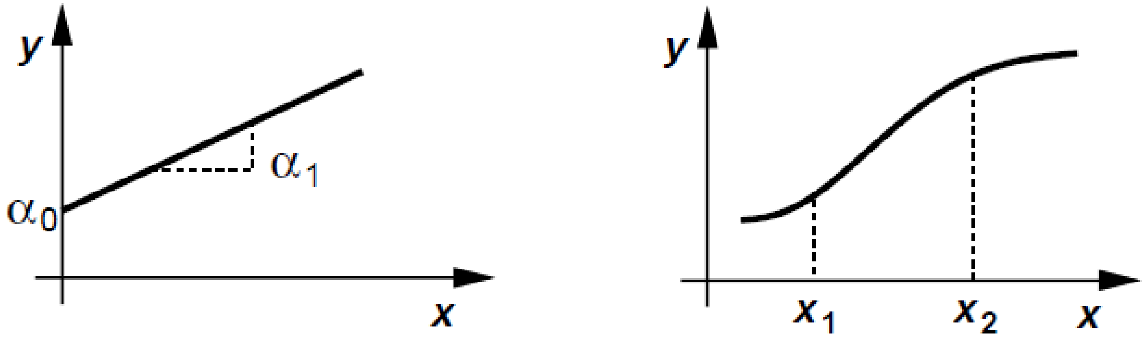
Chapter 3: Single-stage Amplifiers

Ideal vs Non-ideal Amplifier



(a) (b)

- **Ideal amplifier (Fig. a)**

$$y(t) = \alpha_0 + \alpha_1 x(t)$$

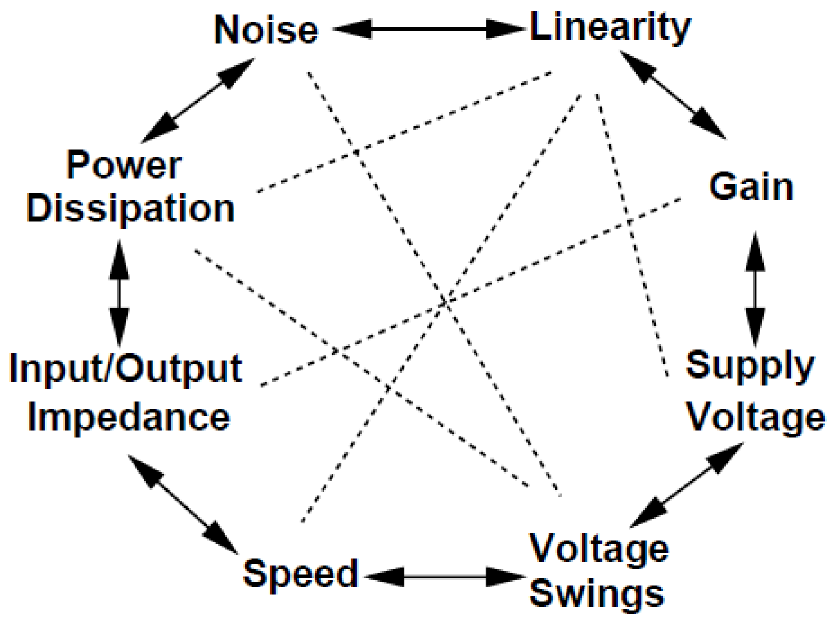
  - **Large-signal characteristic is a straight line**
  - **α_1 is the "gain", α_0 is the "dc bias"**

- **Nonlinear amplifier (Fig. b)**

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \cdots + \alpha_n x^n(t)$$

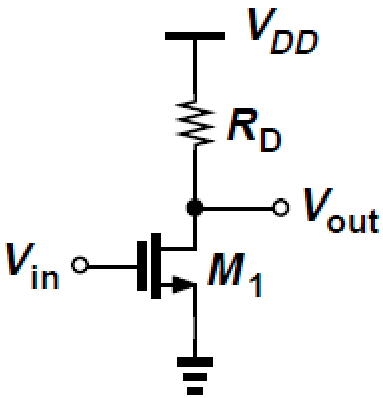
  - **Large signal excursions around bias point**
  - **Varying "gain", approximated by polynomial**
  - **Causes distortion of signal of interest**

Analog Design Tradeoff



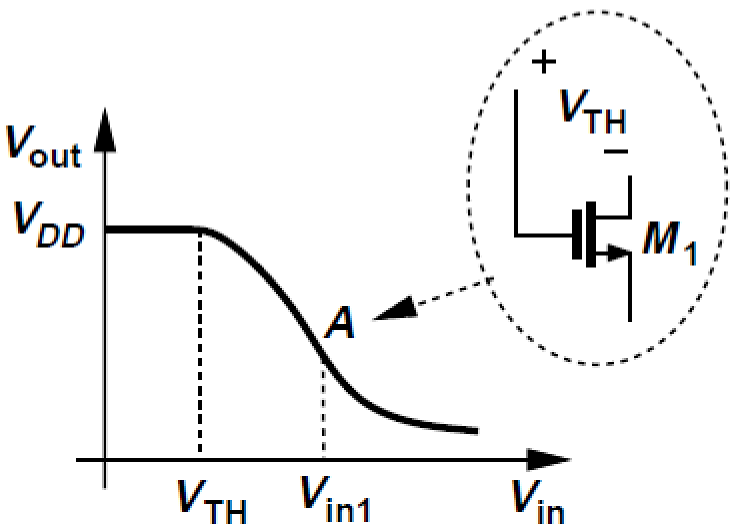
- **Along with gain and speed, other parameters also important for amplifiers**
- **Input and output impedances decide interaction with preceding and subsequent stages**
- **Performance parameters trade with each other**
  - **Multi-dimensional optimization problem**

Common-Source stage with Resistive load



- Very high input impedance at low frequencies
- For $V_{in} < V_{TH}$, M_1 is off and $V_{out} = V_{DD}$

$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2$$

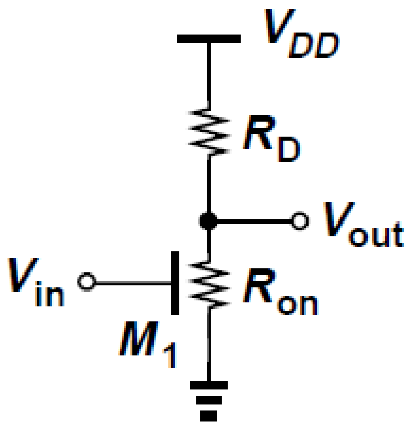


- When $V_{in} > V_{TH}$, M_1 turns on in saturation region, V_{out} falls
- When $V_{in} > V_{in1}$, M_1 enters triode r

$$V_{in1} - V_{TH} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{TH})^2$$

- At point A, $V_{out} = V_{in1} - V_{TH}$

Common-Source stage with Resistive load



- For $V_{in} > V_{in1}$,

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left[2(V_{in} - V_{TH}) V_{out} - V_{out}^2 \right]$$

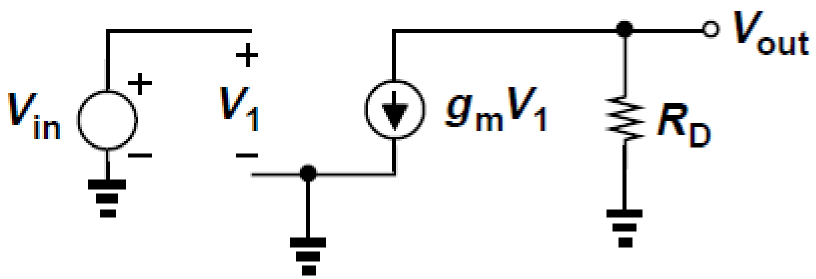
- If V_{in} is high enough to drive M_1 into deep triode region so that

$$\begin{aligned} V_{out} &= V_{DD} \frac{R_{on}}{R_{on} + R_D} \\ &= \frac{V_{DD}}{1 + \mu_n C_{ox} \frac{W}{L} R_D (V_{in} - V_{TH})} \end{aligned}$$

Common-Source stage with Resistive load

$$\begin{aligned} A_v &= \frac{\partial V_{out}}{\partial V_{in}} \\ &= -R_D \mu_n C_{ox} \frac{W}{L}(V_{in} - V_{TH}) \\ &= -g_m R_D. \end{aligned}$$

- **Taking derivative of I_D equation in saturation region, small-signal gain is obtained**



- **Same result is obtained from small-signal equivalent circuit**

$$V_{out} = -g_m V_1 R_D = -g_m V_{in} R_D$$

- ***g_m and A_v* vary for large input signal swings according to**

$$g_m = \mu_n C_{ox}(W/L)(V_{GS} - V_{TH}).$$

- **This causes non-linearity**

Common-Source stage with Resistive load

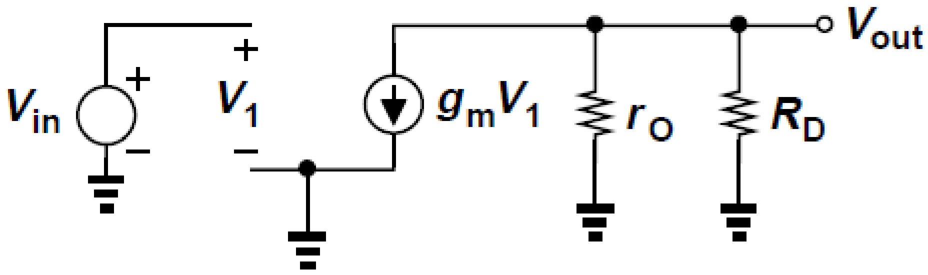
- For large values of R_D, channel-length modulation of M_1 becomes significant, V_{out} equation becomes

$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2(1 + \lambda V_{out})$$

- Voltage gain is

$$A_v = -g_m \frac{r_O R_D}{r_O + R_D}$$

- Above result is also obtained from small-signal equivalent circuit



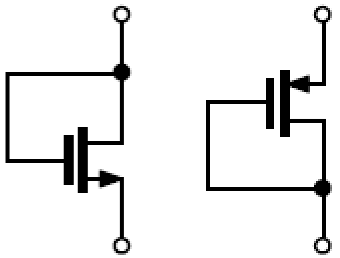
$$V_1 = V_{in}$$

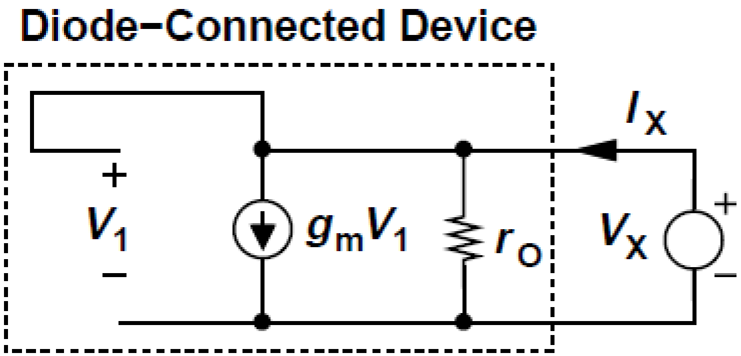
$$g_m V_1 (r_O \| R_D) = -V_{out}$$

$$V_{out}/V_{in} = -g_m (r_O \| R_D)$$

Diode-Connected MOSFET

- **A MOSFET can operate as a small-signal resistor if its gate and drain are shorted, called a "diode-connected" device**
- **Transistor always operates in saturation**



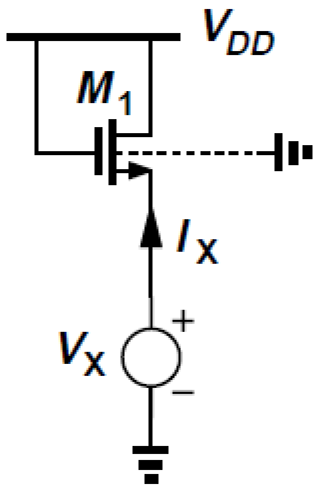


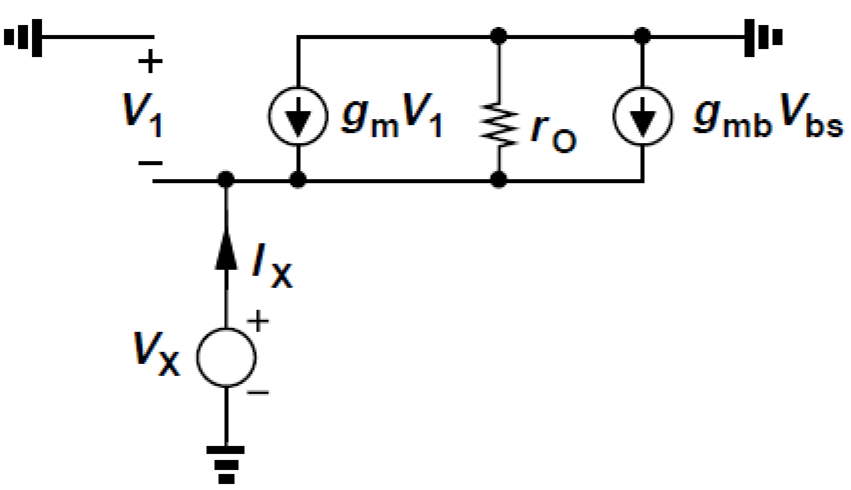
- **Impedance of the device can be found from small-signal equivalent model**

$$V_1 = V_X \qquad I_X = V_X/r_O + g_m V_X$$

$$V_X/I_X = (1/g_m)||r_O \approx 1/g_m$$

Diode-Connected MOSFET





- **Including body-effect, impedance “looking into” the source terminal of diode-connected device is found as**

$$V_1 = -V_X \qquad V_{bs} = -V_X$$

$$(g_m + g_{mb})V_X + \frac{V_X}{r_O} = I_X$$

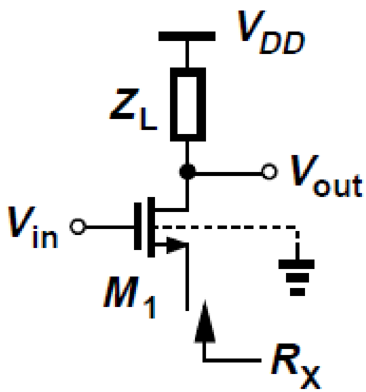
$$\frac{V_X}{I_X} = \frac{1}{g_m + g_{mb} + r_O^{-1}}$$

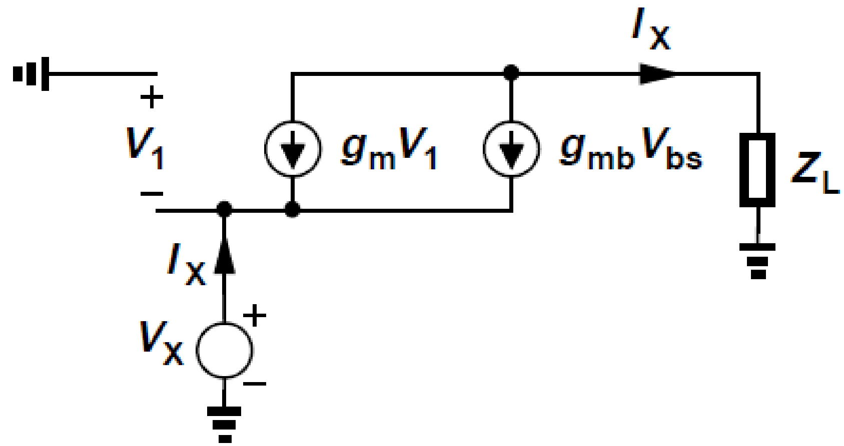
$$= \frac{1}{g_m + g_{mb}} \| r_O$$

$$\approx \frac{1}{g_m + g_{mb}}.$$

Diode-Connected MOSFET: Example

- **Find R_X if $\lambda = 0$**





- **Set independent sources to zero, apply V_X and find resulting I_X**

$$V_1 = V_X$$

$$V_{bs} = -V_X$$

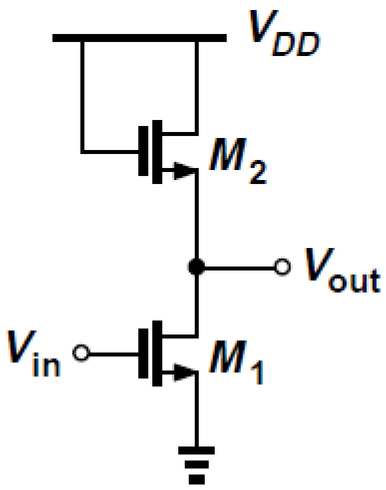
$$(g_m + g_{mb})V_X = I_X$$

$$\frac{V_X}{I_X} = \frac{1}{g_m + g_{mb}}.$$

- **Result is same compared to when drain of M_1 is at ac ground, but only when $\lambda = 0$**

- **Loosely said that looking into source of MOSFET, we see $1/g_m$ when $\lambda = \gamma = 0$**

CS Stage with Diode-Connected Load



- **Neglecting channel-length modulation, using impedance result for diode-connected device,**

$$A_v = -g_{m1}\frac{1}{g_{m2}+g_{mb2}} = -\frac{g_{m1}}{g_{m2}}\frac{1}{1+\eta},$$

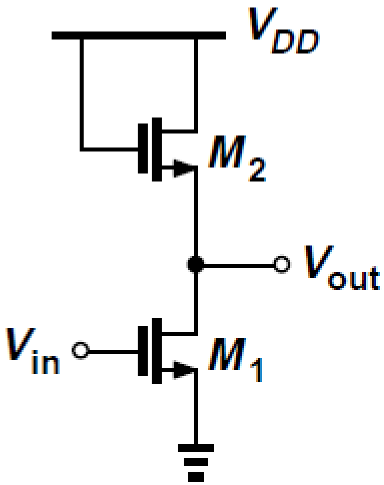
where, $\eta = g_{mb2}/g_{m2}$.

- **Expressing g_{m1} and g_{m2} in terms of device dimensions,**

$$A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}\frac{1}{1+\eta}$$

- **This shows that gain is a weak function of bias currents and voltages, i.e., relatively linear input-output characteristic**

CS Stage with Diode-Connected Load



- From large-signal analysis,

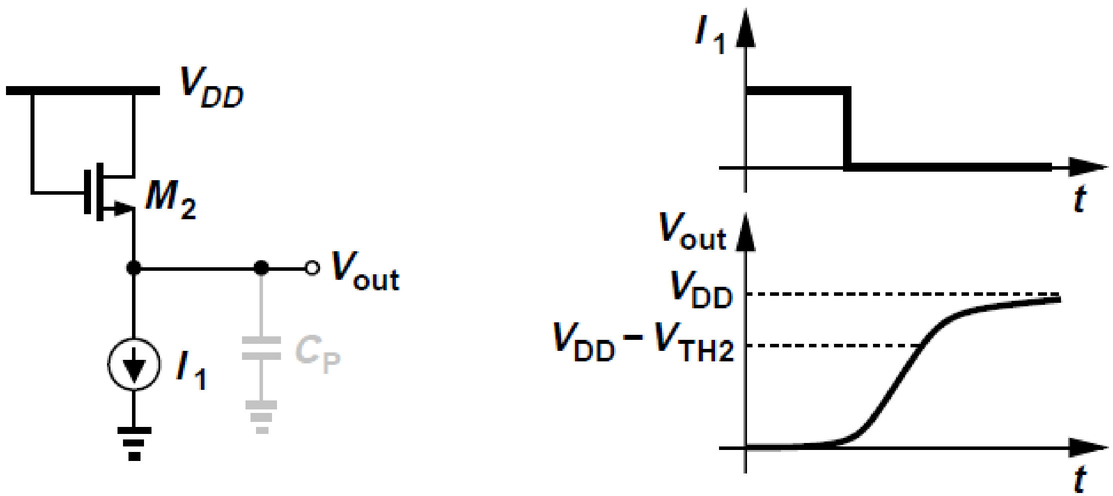
$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{in}-V_{TH1})^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{DD}-V_{out}-V_{TH2})^2$$

$$\sqrt{\left(\frac{W}{L}\right)_1}(V_{in}-V_{TH1}) = \sqrt{\left(\frac{W}{L}\right)_2}(V_{DD}-V_{out}-V_{TH2})$$

- **If V_{TH2} does not vary much with V_{out}, input-output characteristic is relatively linear.**
- **Squaring function of M_1 (from its input voltage to its drain current) and square root function of M_2 (from its drain current to its overdrive) act as inverse functions**

$$f^{-1}(f(x)) = x.$$

CS Stage with Diode-Connected Load

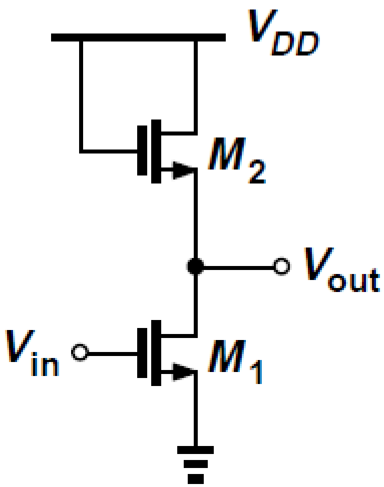


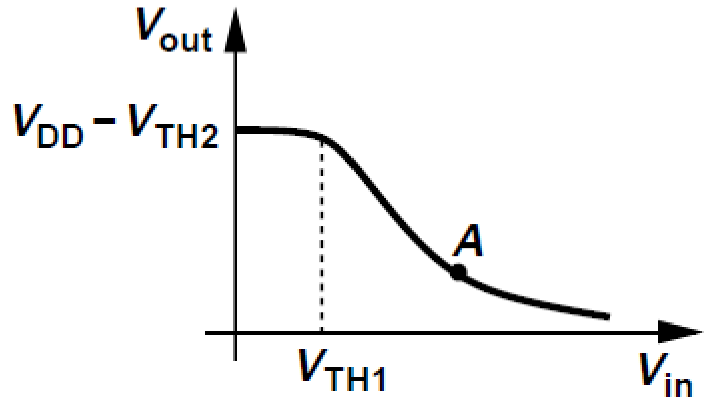
- As I_1 falls, so does overdrive of M_2 so that

$$V_{GS2} \approx V_{TH2} \qquad V_{out} \approx V_{DD} - V_{TH2}$$

- Subthreshold conduction of M_2 eventually brings V_{out} to V_{DD}, but at very low current levels, finite capacitance at output node C_P slows down the change in V_{out} from V_{DD}-V_{TH2} to V_{DD}.
- In high-frequency circuits, V_{out} remains around V_{DD}-V_{TH2} when I_1 falls to small values.

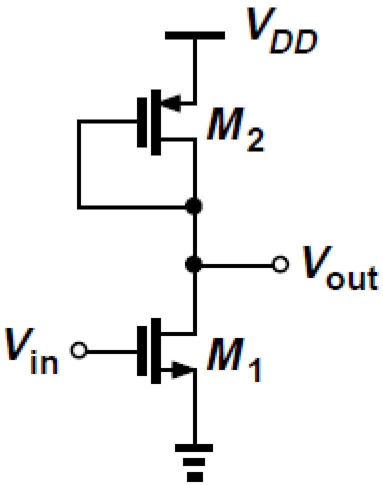
CS Stage with Diode-Connected Load





- **For $V_{in} < V_{TH1}$, $V_{out} = V_{DD} - V_{TH2}$**
- **When $V_{in} > V_{TH1}$, previous large-signal analysis predicts that V_{out} approximately follows a single line**
- **As V_{in} exceeds $V_{out} + V_{TH1}$ (to the right of point A), M_1 enters the triode region and the characteristic becomes nonlinear.**

CS Stage with Diode-Connected PMOS device



- **Diode-connected load can be implemented as a PMOS device, free of body-effect**
- **Small-signal voltage gain neglecting channel-length modulation**

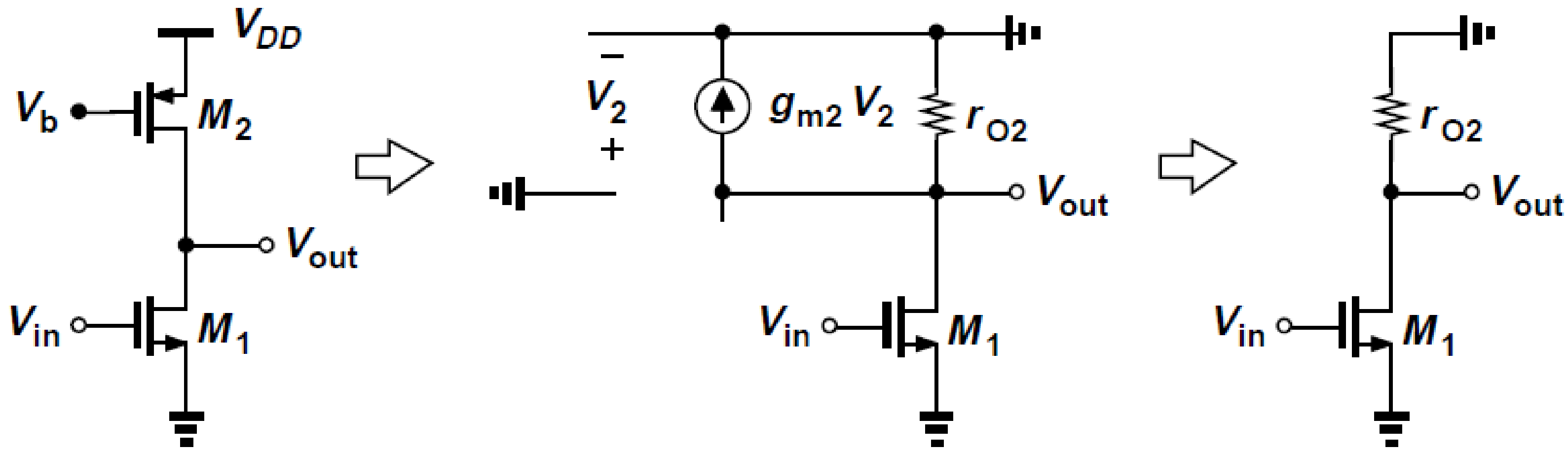
$$A_v = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}}$$

- **Gain is a relatively weak function of device dimensions**
- **Since $\mu_n \approx 2\mu_p$, high gain requires "strong" input device (narrow) and "weak" load device (wide)**
- **This limits voltage swings since for $\lambda = 0$, we get**

$$\frac{|V_{GS2} - V_{TH2}|}{V_{GS1} - V_{TH1}} = A_v$$

- **For diode-connected loads, swing is constrained by both required overdrive voltage and threshold voltage, i.e., for small overdrive, output cannot exceed V_{DD} - $|V_{TH}|$.**

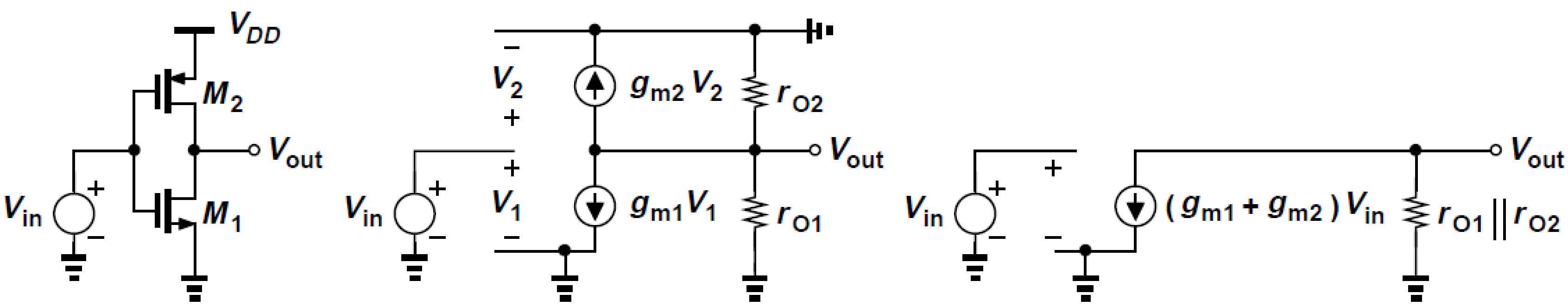
CS Stage with Current-Source Load



- **Current-source load allows a high load resistance without limiting output swing**
- **Voltage gain is** $A_v = -g_{m1}(r_{O1} \| r_{O2})$
- **Overdrive of *M_2* can be reduced by increasing its width, *r_{o2}* can be increased by increasing its length**
- **Output bias voltage is not well-defined**
- **Intrinsic gain of *M_1* increases with *L* and decreases with *I_D***

$$g_{m1}r_{O1} = \sqrt{2\left(\frac{W}{L}\right)_1 \mu_n C_{ox} I_D}\,\frac{1}{\lambda I_D}$$

CS Stage with Active Load



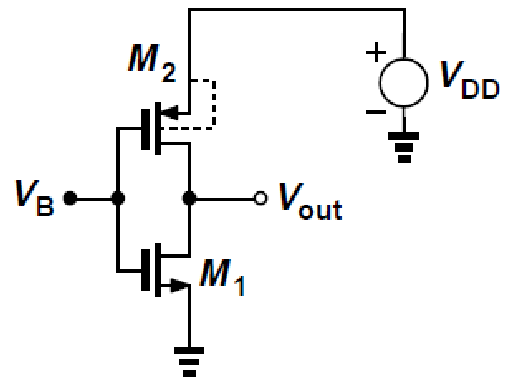
- **Input signal is also applied to gate of load device, making it an "active" load**
- **M_1 and M_2 operate in parallel and enhance the voltage gain**
- **From small-signal equivalent circuit,**

$$-(g_{m1}+g_{m2})V_{in}(r_{O1}||r_{O2}) = V_{out}$$

$$A_v = -(g_{m1}+g_{m2})(r_{O1}||r_{O2})$$

- **Same output resistance as CS stage with current-source load, but higher transconductance**
- **Bias current of M_1 and M_2 is a strong function of PVT**

CS Stage with Active Load: Supply sensitivity



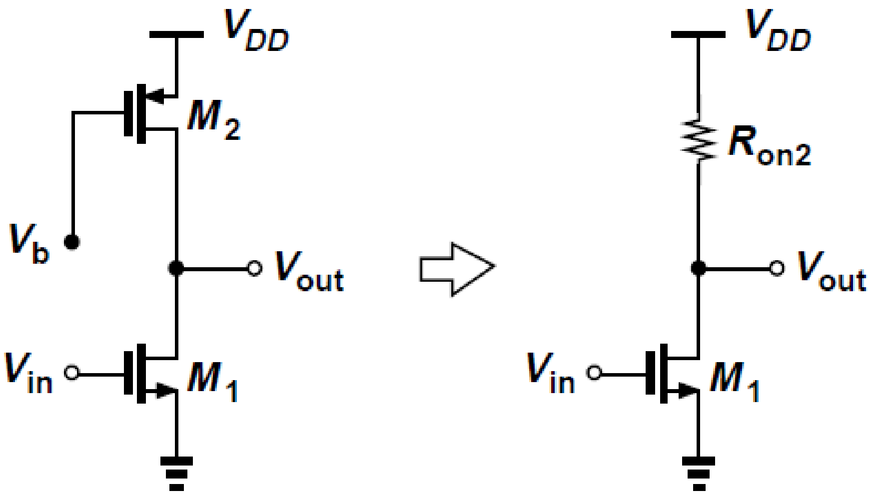
$$V_{GS1} + |V_{GS2}| = V_{DD}$$

- **Variations in V_{DD} or the threshold voltages directly translate to changes in the drain currents**
- **Supply voltage variations "supply noise" are amplified too**
- **Voltage gain from V_{DD} to V_{out} can be found to be**

$$\frac{V_{out}}{V_{DD}} = \frac{g_{m2}r_{O2}+1}{r_{O2}+r_{O1}}r_{O1}$$

$$= \left(g_{m2}+\frac{1}{r_{O2}}\right)(r_{O1}||r_{O2})$$

CS Stage with Triode Load

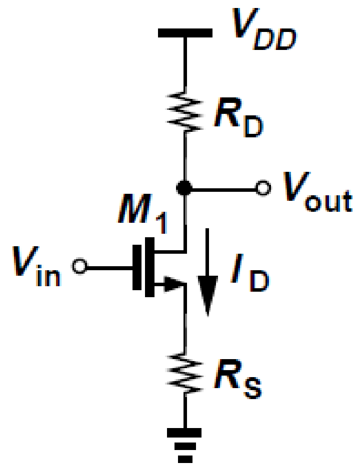


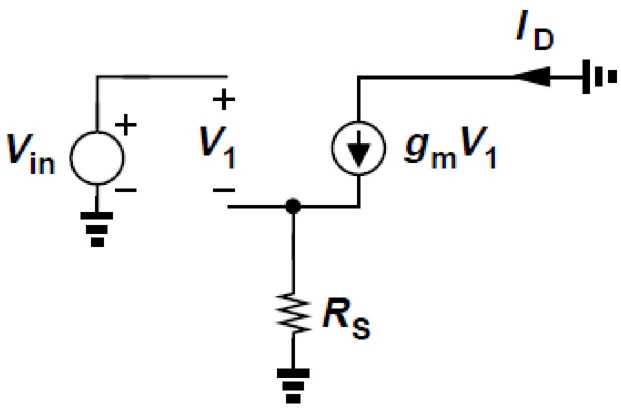
- A MOS device biased in the deep triode region acts as a resistive load in a CS stage
- V_b is sufficiently low to ensure M_2 is in deep triode region for all output voltage swings
- Voltage gain is $A_v = -g_{m1}R_{on2}$, where R_{on2} is the MOS ON resistance given by

$$R_{on2} = \frac{1}{\mu_p C_{ox}(W/L)_2(V_{DD} - V_b - |V_{THP}|)}$$

- R_{on2} depends on $\mu_p C_{ox}$, V_b and V_{THP} which vary with PVT
- Generating a precise value of V_b is complex, which makes circuit hard to use
- Triode loads consume lesser voltage headroom than diode-connected devices since $V_{out,max} = V_{DD}$ for the former

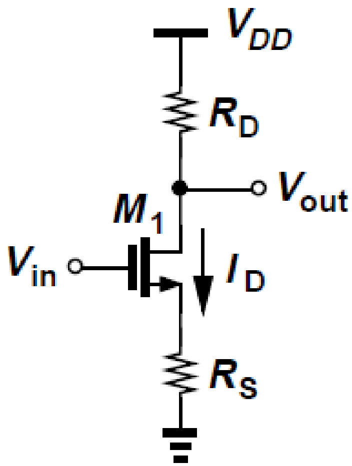
CS Stage with Source Degeneration

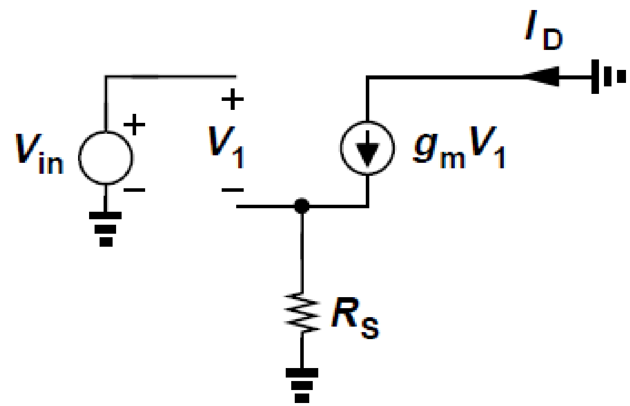




- Degeneration resistor R_S in series with source terminal makes input device more linear
  - As V_{in} increases, so do I_D and the voltage drop across R_S
  - Part of the change in V_{in} appears across R_S rather than gate-source overdrive, making variation in I_D smoother
- Gain is now a weaker function of g_m

CS Stage with Source Degeneration





- **Nonlinearity of circuit is due to nonlinear dependence of I_D upon V_{in}**
- **Equivalent transconductance G_m of the circuit can be defied as** $G_m = \partial I_D / \partial V_{in}$

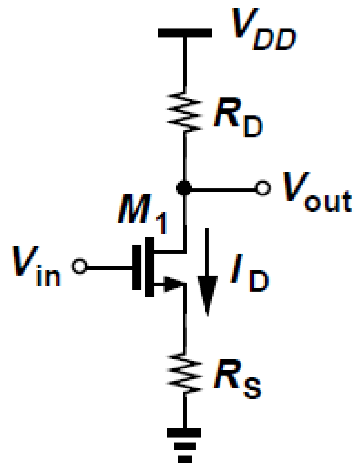
$$V_{out} = V_{DD} - I_D R_D$$

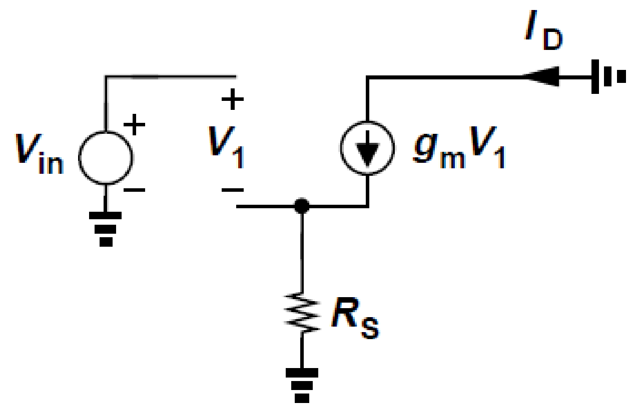
$$\partial V_{out} / \partial V_{in} = -(\partial I_D / \partial V_{in}) R_D$$

$$I_D = f(V_{GS})$$

$$G_m = \frac{\partial I_D}{\partial V_{in}} = \frac{\partial f}{\partial V_{GS}} \frac{\partial V_{GS}}{\partial V_{in}}$$

CS Stage with Source Degeneration





$$V_{GS} = V_{in} - I_D R_S$$

$$\partial V_{GS}/\partial V_{in} = 1 - R_S \partial I_D/\partial V_{in}$$

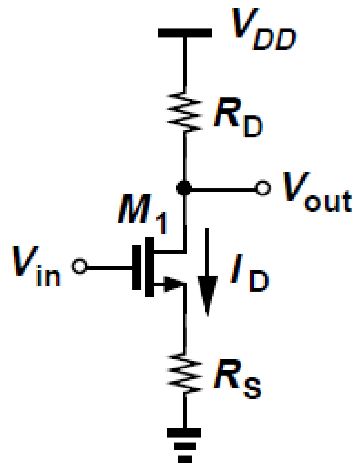
$$G_m = \left(1 - R_S \frac{\partial I_D}{\partial V_{in}}\right) \frac{\partial f}{\partial V_{GS}}$$

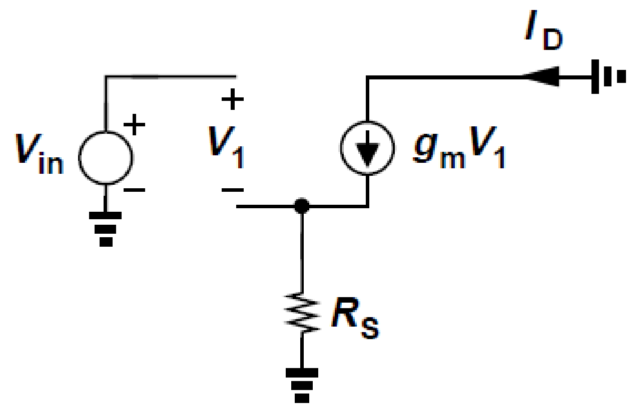
$$G_m = \frac{g_m}{1 + g_m R_S}$$

- g_m **is the transconductance of** M_1
- **Small-signal voltage gain** A_v **is then given by**

$$\begin{aligned} A_v &= -G_m R_D \\ &= \frac{-g_m R_D}{1 + g_m R_S} \end{aligned}$$

CS Stage with Source Degeneration





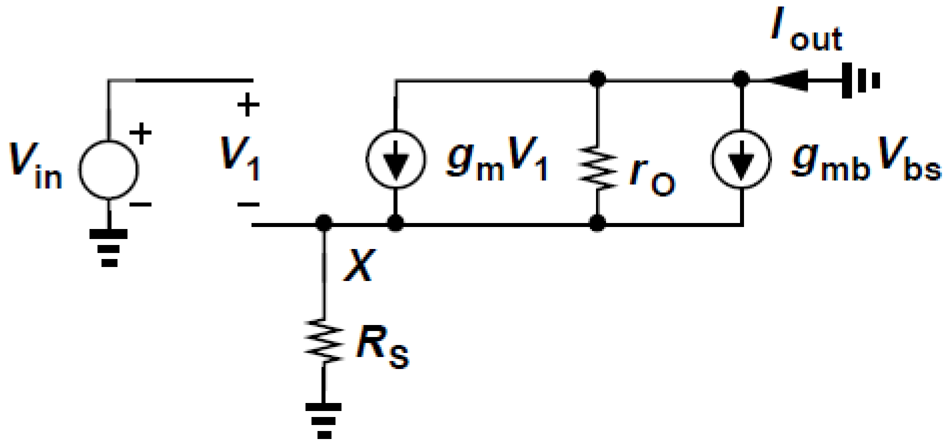
- **Same result for G_m is obtained from small-signal equivalent circuit, by noting that**

$$V_{in} = V_1 + I_D R_S$$

$$I_D = g_m V_1$$

- **As R_S increases, G_m becomes a weaker function of g_m and hence I_D**
- **For $R_S \gg 1/g_m$, $G_m \approx 1/R_S$, i.e., $\Delta I_D \approx \Delta V_{in}/R_S$**
- **Most of the change in V_{in} across R_S and drain current becomes a "linearized" function of input voltage**

CS Stage with Source Degeneration



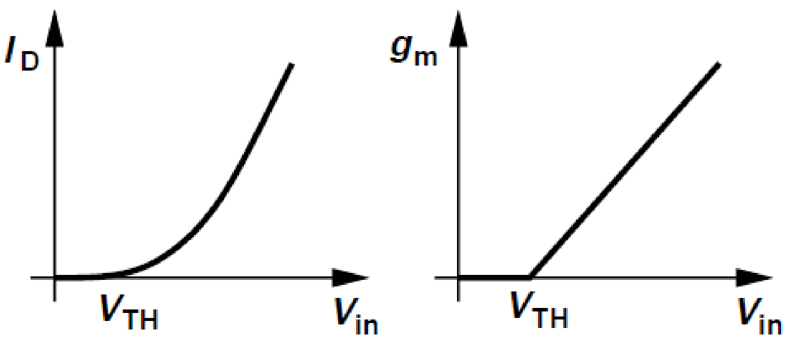
- **Including body-effect and channel-length modulation, G_m is found from modified small-signal equivalent circuit**

$$V_{in} = V_1 + I_{out} R_S$$

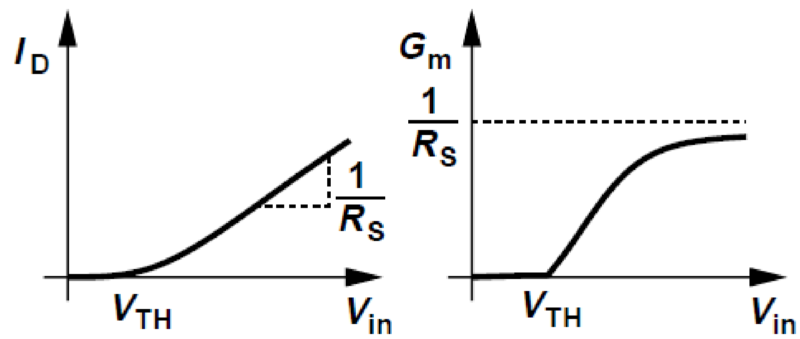
$$\begin{aligned} I_{out} &= g_m V_1 - g_{mb} V_X - \frac{I_{out} R_S}{r_O} \\ &= g_m (V_{in} - I_{out} R_S) + g_{mb}(-I_{out} R_S) - \frac{I_{out} R_S}{r_O} \\ G_m &= \frac{I_{out}}{V_{in}} \\ &= \frac{g_m r_O}{R_S + [1 + (g_m + g_{mb}) R_S] r_O} \end{aligned}$$

CS Stage with Source Degeneration

Large-signal behavior



***R_S*=0**



***R_S*≠0**

- **I_D and g_m vary with V_{in} as derived in calculations in Chapter 2**

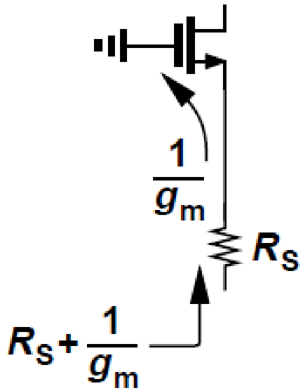
- **At low current levels, turn-on behavior is similar to when R_S=0 since**
  a $1/g_m \gg R_S$
  $G_m \approx g_m$
- **As overdrive and g_m increase, effect of R_S becomes more significant**

CS Stage with Source Degeneration

- Small-signal derived previously can be written as

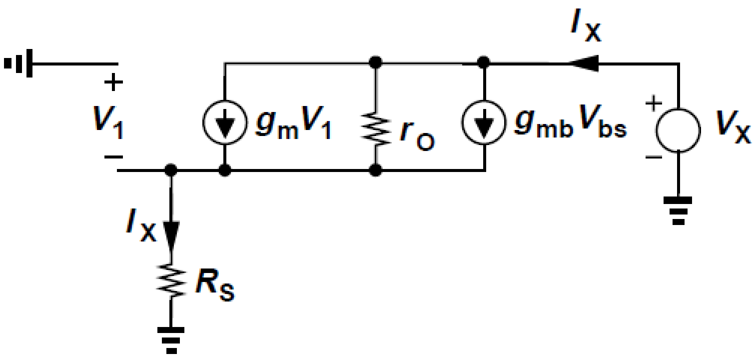
$$A_v = -\frac{R_D}{\dfrac{1}{g_m} + R_S}$$

- Denominator = Series combination of inverse transconductance + explicit resistance seen from source to ground
- Called "resistance seen in the source path"
- Magnitude of gain = Resistance seen at the drain/ Total resistance seen in the source path



CS Stage with Source Degeneration

- **Degeneration causes increase in output resistance**



- **Ignoring R_D and including body effect in small-signal equivalent model,**

$$V_1 = -I_X R_S$$

$$I_X - (g_m + g_{mb})V_1 = I_X + (g_m + g_{mb})R_S I_X$$

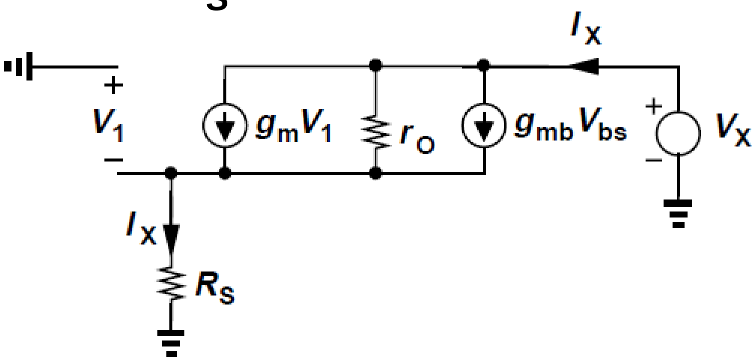
$$R_{out} = [1 + (g_m + g_{mb})R_S]r_O + R_S$$

$$= [1 + (g_m + g_{mb})r_O]R_S + r_O.$$

- **r_o is boosted by a factor of {1 + (g_m+g_{mb})R_S} and then added to R_S**
- **Alternatively, R_S is boosted by a factor of {1 + (g_m+g_{mb})r_o} and then added to r_o**

CS Stage with Source Degeneration

- Compare $R_S = 0$ with $R_S > 0$

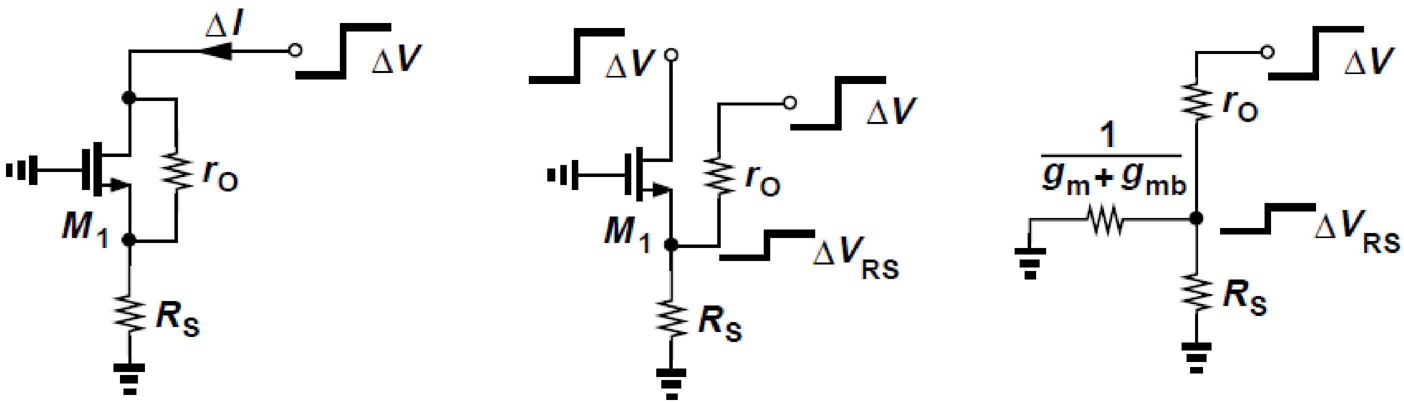


- If $R_S = 0$, $g_m V_1 = g_{mb} V_{bs} = 0$ and $I_X = V_X / r_O$
- If $R_S > 0$, $I_X R_S > 0$ and $V_1 < 0$, obtaining negative $g_m V_1$ and $g_{mb} V_{bs}$
- Thus, current supplied by V_X is less than V_X/r_o and hence output impedance is greater than r_o

CS Stage with Source Degeneration

Intuitive understanding of increased output impedance

- Apply voltage change ***ΔV*** at output and measure resulting change ***ΔI*** in output current, which is also the change in current through R_S

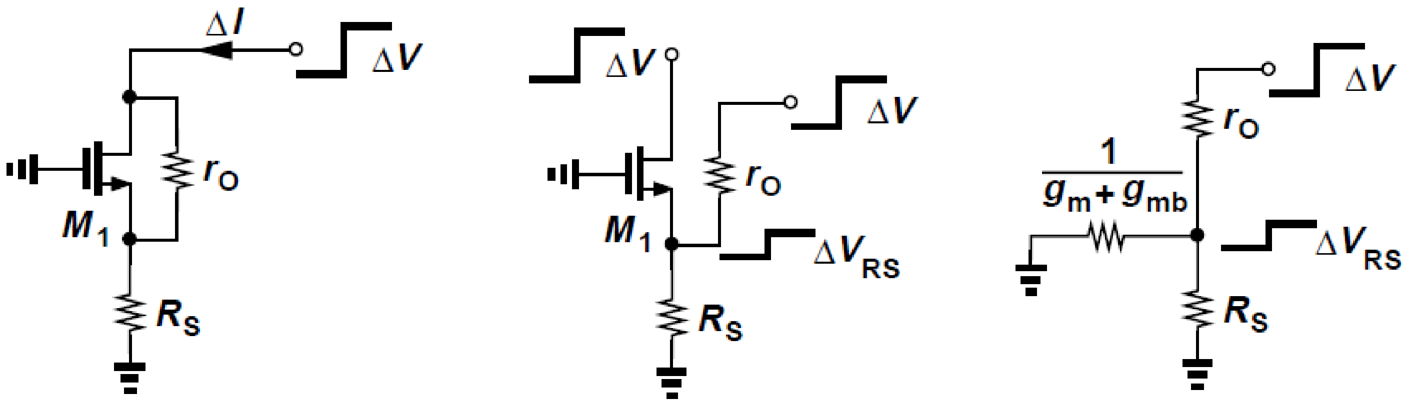


- Resistance seen looking into the source of M_1 is $1/(g_m + g_{mb})$
- Voltage change across R_S is

$$\Delta V_{RS} = \Delta V \frac{\dfrac{1}{g_m + g_{mb}} \| R_S}{\dfrac{1}{g_m + g_{mb}} \| R_S + r_O}$$

CS Stage with Source Degeneration

Intuitive understanding of increased output impedance



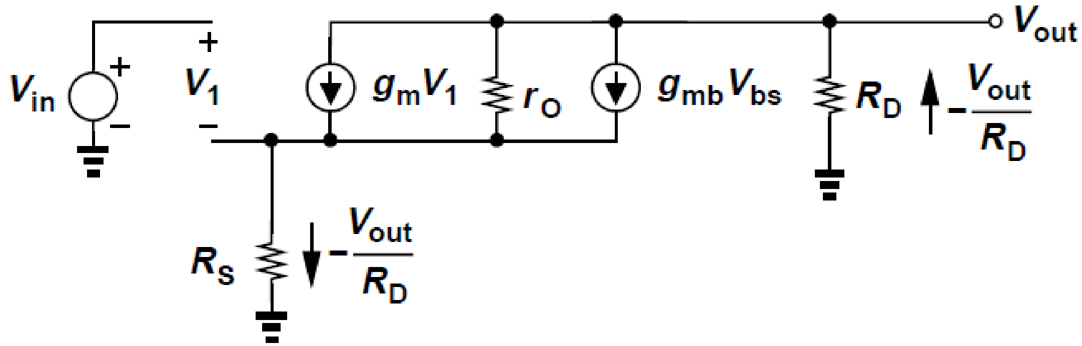
- **Change in current across R_S is**

$$\Delta I = \frac{\Delta V_{RS}}{R_S}$$

$$= \Delta V \frac{1}{[1 + (g_m + g_{mb})]R_S r_O + R_S}.$$

- **Output resistai** $\frac{\Delta V}{\Delta I} = [1 + (g_m + g_{mb})R_S]r_O + R_S$

CS Stage with Source Degeneration



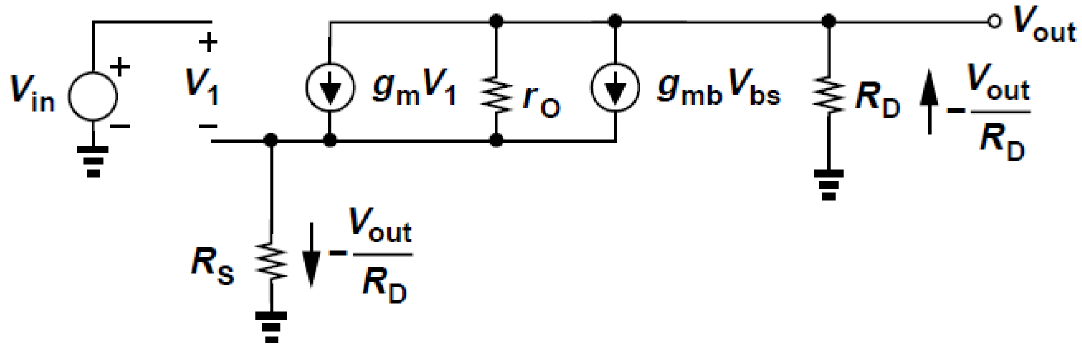
- To compute gain in the general case including body effect and channel-length modulation, consider above small-signal model
- From KVL at input,

$$V_1 = V_{in} + V_{out} R_S / R_D$$

- KCL at output gives

$$\begin{aligned} I_{ro} &= -\frac{V_{out}}{R_D} - (g_m V_1 + g_{mb} V_{bs}) \\ &= -\frac{V_{out}}{R_D} - \left[g_m \left(V_{in} + V_{out} \frac{R_S}{R_D} \right) + g_{mb} V_{out} \frac{R_S}{R_D} \right] \end{aligned}$$

CS Stage with Source Degeneration



- **Since voltage drops across r_o and R_S must add up to V_{out},**

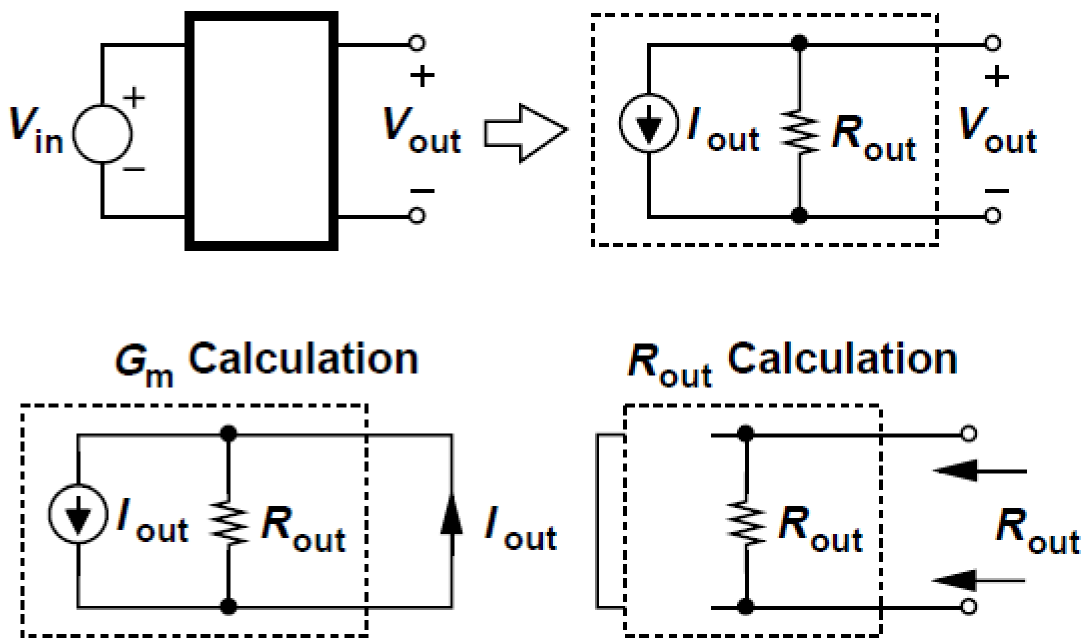
$$\begin{aligned} V_{out} &= I_{ro} r_O - \frac{V_{out}}{R_D} R_S \\ &= -\frac{V_{out}}{R_D} r_O - \left[g_m \left(V_{in} + V_{out} \frac{R_S}{R_D} \right) + g_{mb} V_{out} \frac{R_S}{R_D} \right] r_O - V_{out} \frac{R_S}{R_D} \end{aligned}$$

- **Voltage gain is therefore**

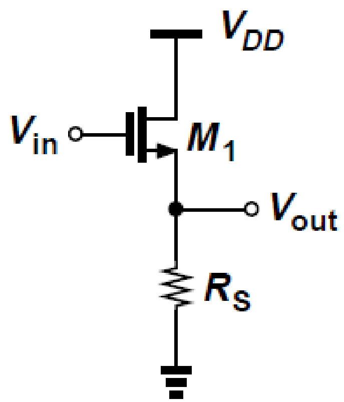
$$\frac{V_{out}}{V_{in}} = \frac{-g_m r_O R_D}{R_D + R_S + r_O + (g_m + g_{mb}) R_S r_O}$$

Lemma

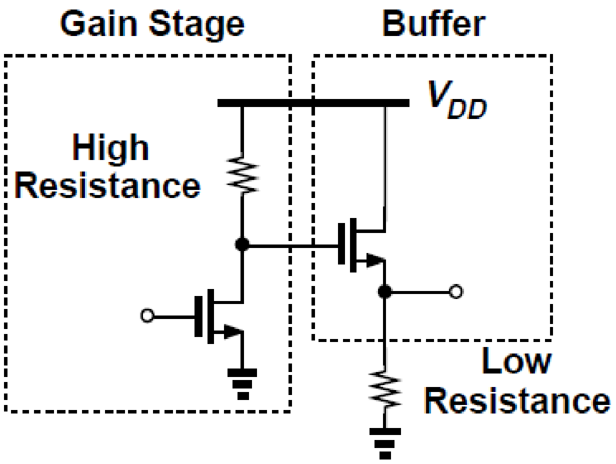
- In a linear circuit, the voltage gain is equal to $-G_m R_{out}$
  - G_m denotes the transconductance of the circuit when output is shorted to ground
  - R_{out} represents the output resistance of the circuit when the input voltage is set to zero
- Norton equivalent of a linear circuit



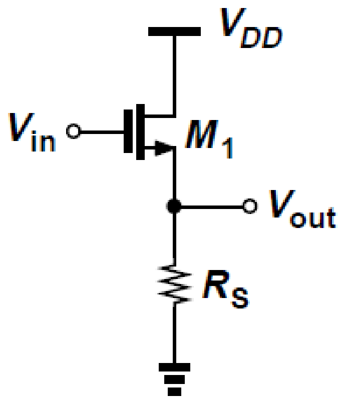
Source Follower

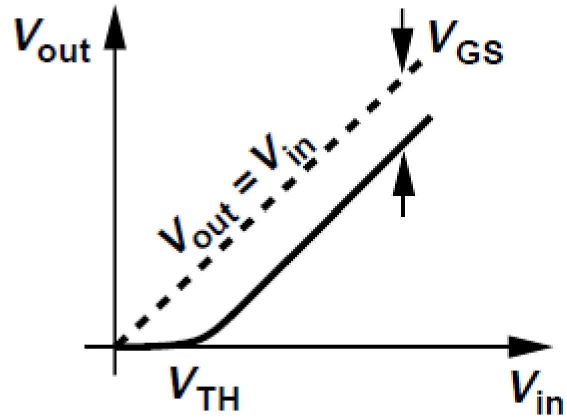


- **Source follower (also called "common-drain" stage) senses the input at the gate and drives load at the source**
- **It presents a high input impedance, allowing source potential to "follow" the gate voltage**
- **Acts as a voltage buffer**



Source Follower

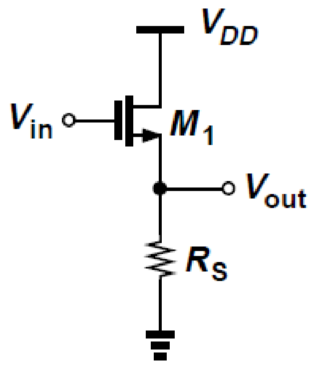


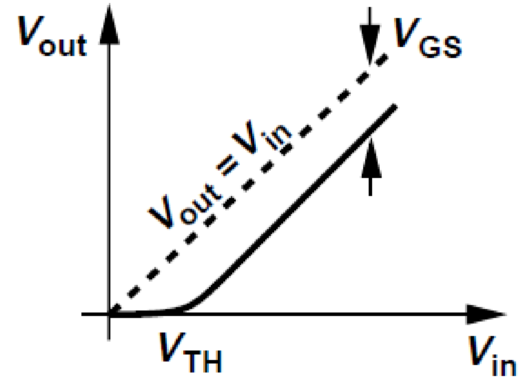


- **For $V_{in} < V_{TH}$, M_1 is off and $V_{out} = 0$**
- **As V_{in} exceeds V_{TH}, M_1 turns on in saturation since $V_{DS} = V_{DD}$ and $V_{GS} - V_{TH} \approx 0$ and I_{D1} flows through R_S**
- **As V_{in} increases further, V_{out} follows the input with a difference (level shift) equal to V_{GS}**
- **Input-output characteristic neglecting channel-length modulation can be expressed as**

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH} - V_{out})^2 R_S = V_{out}$$

Source Follower





- **For $V_{in} < V_{TH}$, M_1 is off and $V_{out} = 0$**
- **Differentiating both sides of large-signal equation for V_{out},**

$$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}2(V_{in} - V_{TH} - V_{out})\left(1 - \frac{\partial V_{TH}}{\partial V_{in}} - \frac{\partial V_{out}}{\partial V_{in}}\right) R_S = \frac{\partial V_{out}}{\partial V_{in}}$$

- **Since** $\partial V_{TH}/\partial V_{in} = (\partial V_{TH}/\partial V_{SB})(\partial V_{SB}/\partial V_{in}) = \eta\partial V_{out}/\partial V_{in}$,
- **Therefore,**

$$\frac{\partial V_{out}}{\partial V_{in}} = \frac{\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH} - V_{out})R_S}{1 + \mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH} - V_{out})R_S(1+\eta)}$$

- **Note that**

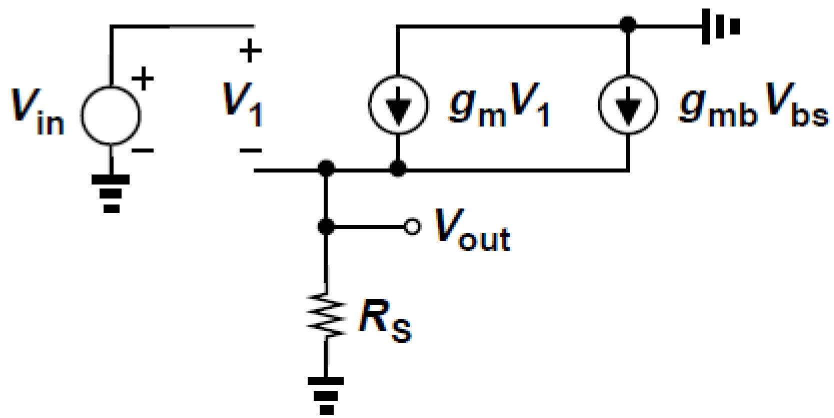
$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH} - V_{out})$$

- **Therefore,**

$$A_v = \frac{g_m R_S}{1 + (g_m + g_{mb})R_S}$$

Source Follower

- Small-signal gain can be obtained more easily using small-signal equivalent model



$$V_{in} - V_1 = V_{out},\ V_{bs} = -V_{out}$$

- We have,
- KVL:

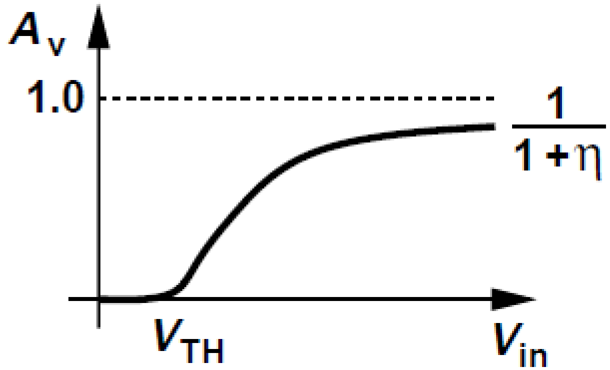
$$g_m V_1 - g_{mb} V_{out} = V_{out}/R_S$$

- KCL:

$$V_{out}/V_{in} = g_m R_S/[1 + (g_m + g_{mb})R_S]$$

- Therefore

Source Follower

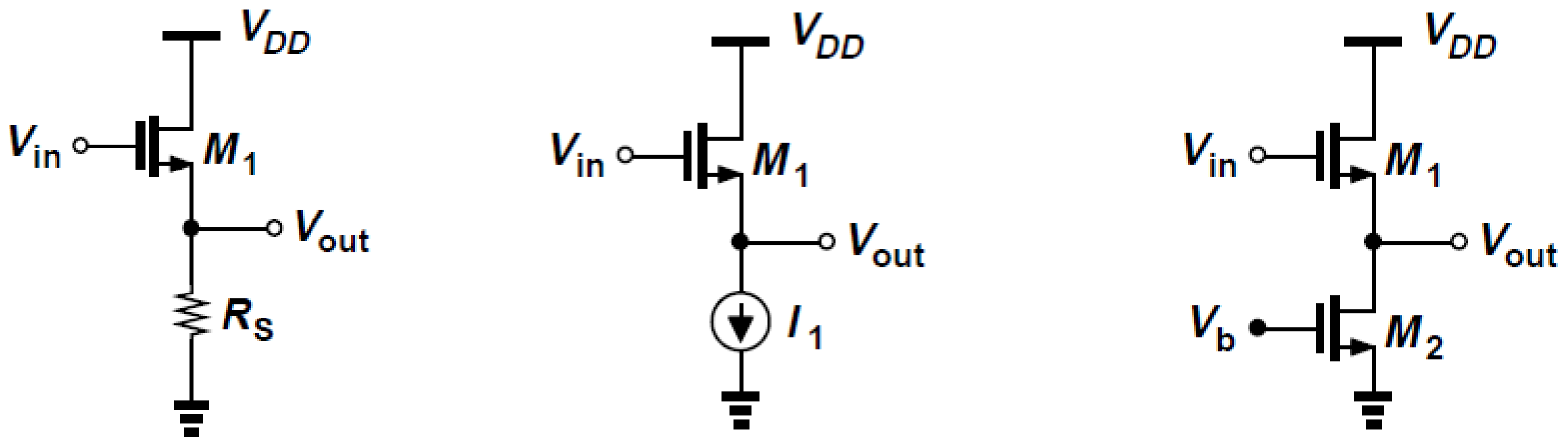


- **Voltage gain begins from zero for $V_{in} \approx V_{TH}$ ($g_m \approx 0$), and monotonically increases**
- **As drain current and g_m increase, A_v approaches**

$$g_m/(g_m + g_{mb}) = 1/(1+\eta)$$

- **Since η itself slowly decreases with V_{out}, A_v would eventually become equal to unity, but for typical allowable source-bulk voltages, η remains greater than roughly than 0.2**
- **Even if $R_S = \infty$, voltage gain of a source follower is not equal to one**

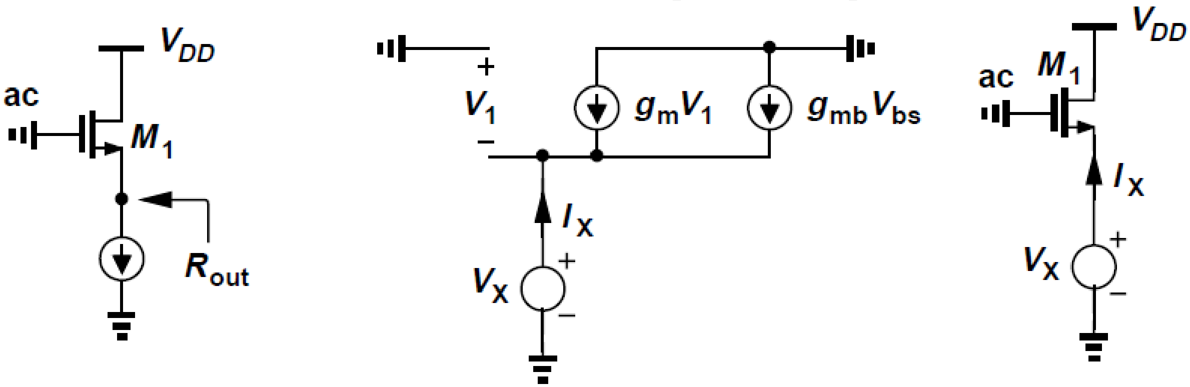
Source Follower



- **Drain current of M_1 depends heavily of input dc level**
- **Even if V_{TH} is relatively constant, the increase in V_{GS} means that V_{out} (=V_{in}-V_{GS}) does not follow V_{in} faithfully, incurring nonlinearity**
- **To alleviate this issue, the resistor can be replaced by a constant current source**
- **Current source is itself is implemented as an NMOS transistor operating in the saturation region**

Source Follower

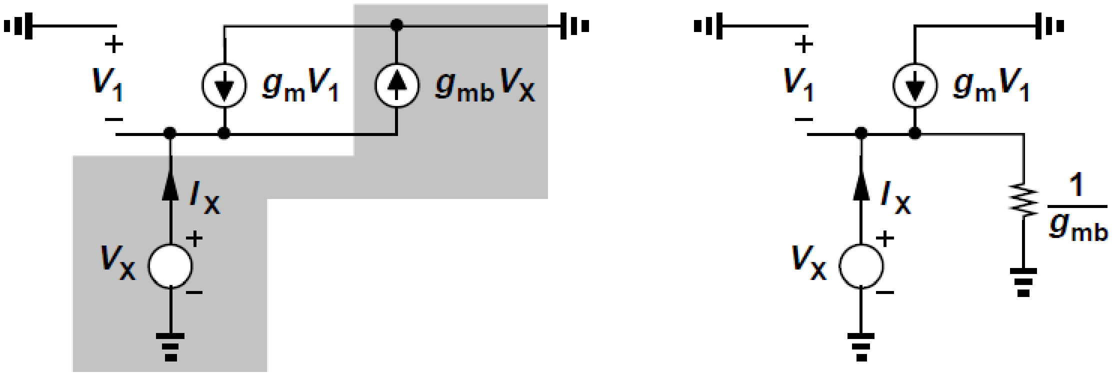
Calculation of output impedance



- From small-signal equivalent circuit, $V_X = -V_{bs}$
- It follows that $I_X - g_m V_X - g_{mb} V_X = 0$ and $R_{out} = \dfrac{1}{g_m + g_{mb}}$

- Body effect decreases output resistance of source followers
- If V_X decreases by ΔV so the drain current increases
  - w/o body effect, V_{GS} increases by ΔV
  - with body effect, V_{TH} decreases as well, thus $(V_{GS}-V_{TH})^2$ and I_{D1} increase by a greater amount, hence lower output impedance

Source Follower

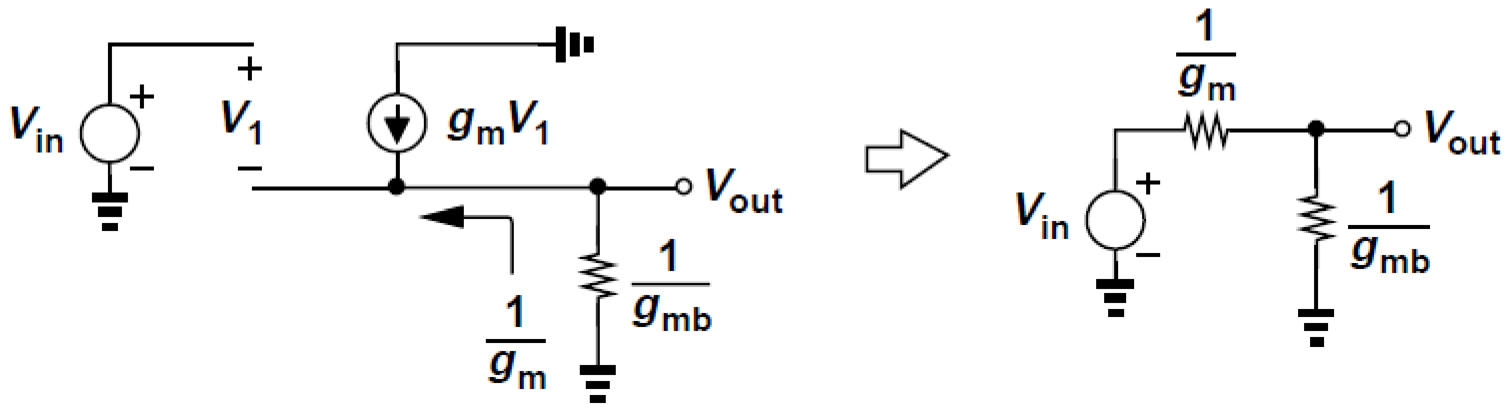


- Magnitude of the current source $g_{mb}V_{bs} = g_{mb}V_X$ is linearly proportional to the voltage across it, can be modelled by a resistor equal to $1/g_{mb}$ (valid only for source followers)
- This appears in parallel with the output, decreasing the overall output resistance
- Since without $1/g_{mb}$, the output resistance is $1/g_m$, we conclude that

$$R_{out} = \frac{1}{g_m} \| \frac{1}{g_{mb}}$$

$$= \frac{1}{g_m + g_{mb}}$$

Source Follower



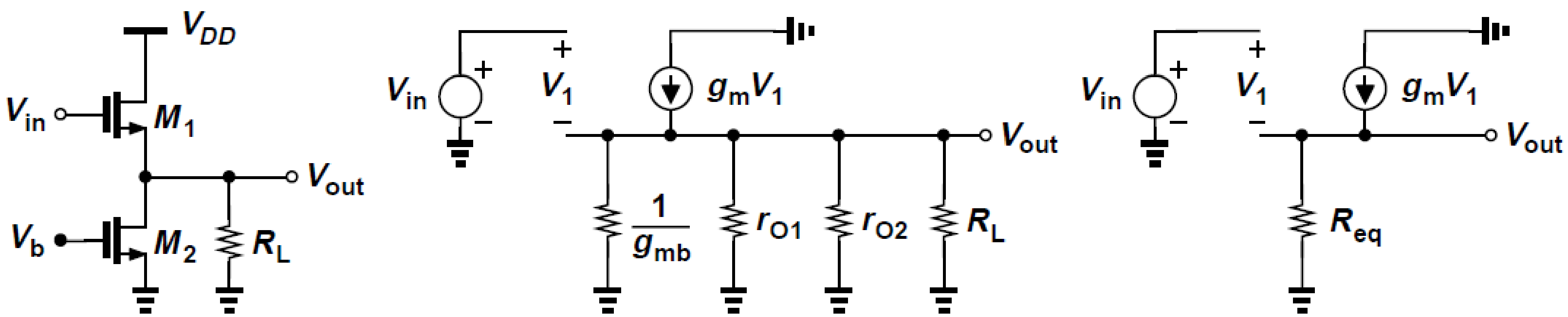
- **Modelling effect of g_{mb} by a resistor helps explain lower than unity gain for $R_S = \infty$**
- **From the Thevenin equivalent circuit**

$$A_v = \frac{\frac{1}{g_{mb}}}{\frac{1}{g_m} + \frac{1}{g_{mb}}}$$

$$= \frac{g_m}{g_m + g_{mb}}.$$

Source Follower

- **Small-signal equivalent circuit with a finite load resistance and channel-length modulation is shown**



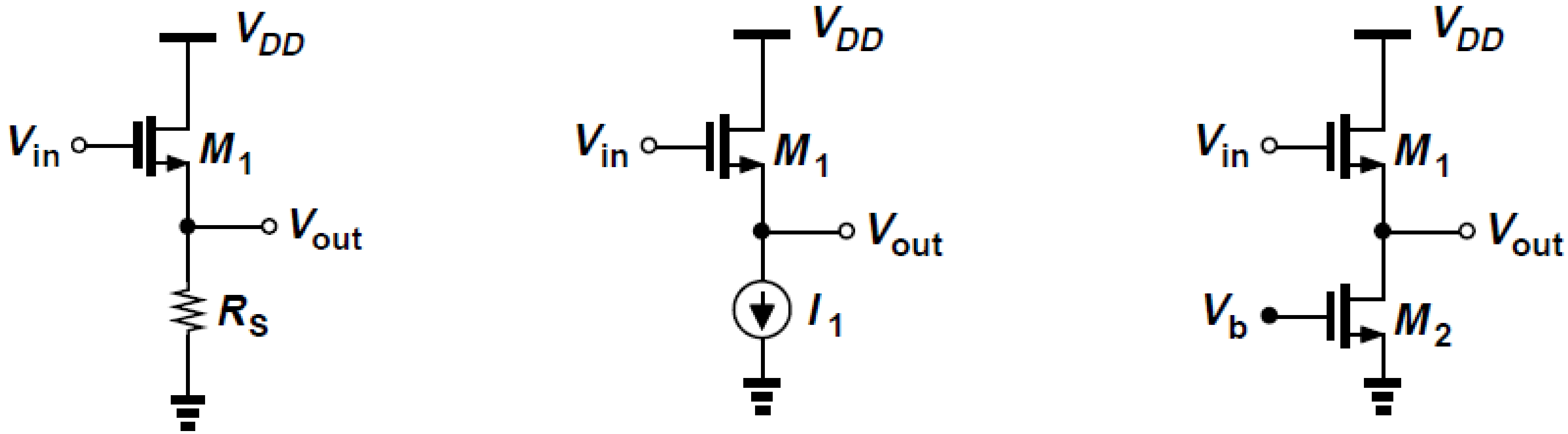
- ***1/g***$_{mb}$**, *r***$_{O1}$**, *r***$_{O2}$ **and *R***$_L$ **are in parallel, therefore,**

$$R_{eq} = (1/g_{mb})||r_{O1}||r_{O2}||R_L$$

- **It follows that**

$$A_v = \frac{R_{eq}}{R_{eq} + \frac{1}{g_m}}$$

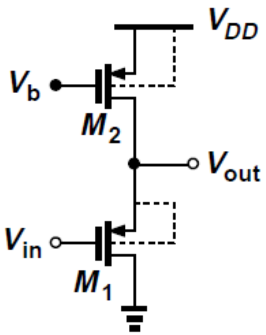
Issues with Source Follower

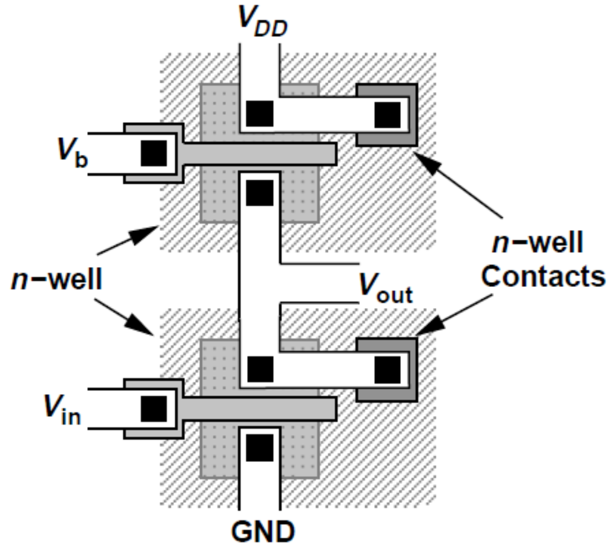


- **Source followers exhibit high input impedance and moderate output impedance, but at the cost of**
  - **Nonlinearity**
  - **Voltage headroom limitation**
- **Even when biased by ideal current source, there is input-output nonlinearity due to nonlinear dependence of V_{TH} on the source potential**
- **In submicron technologies, r_O changes substantially with V_{DS} and introduces additional variation in small-signal gain**

Issues with Source Follower

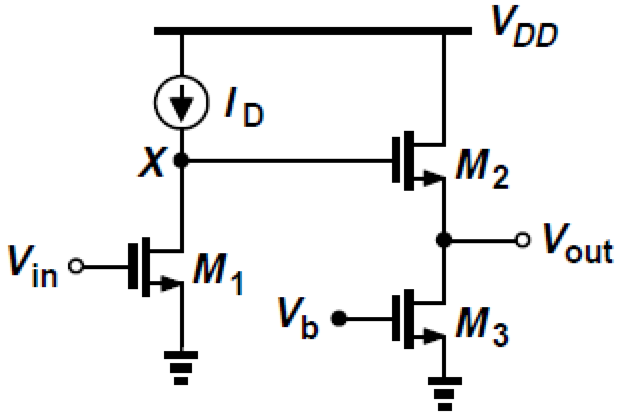
- Nonlinearity can be eliminated if the bulk is tied to the source
  - Possible only for PFETs since all NFETs usually share the same substrate
- PMOS source follower employing two separate n-wells can eliminate the body effect of M_1
- Lower mobility of PFETs yields a higher output impedance than that available in the NMOS counterpart





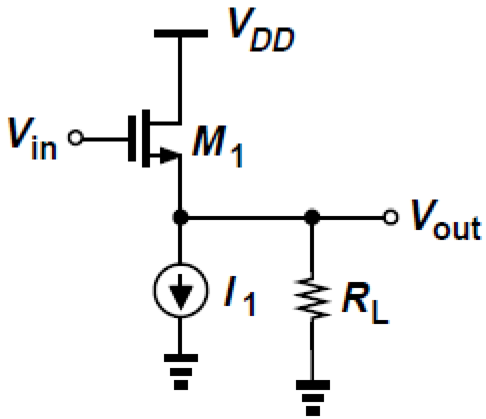
Issues with Source Follower

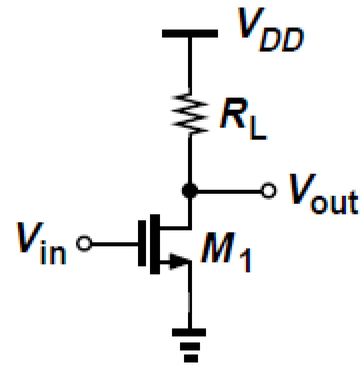
- Source followers also shift the dc level of the signal by V_{GS}, thereby consuming voltage headroom



- In the cascade of CS stage and source follower shown above,
  - w/o source follower, minimum allowable value of V_X would be V_{GS1}-V_{TH1} (for M_1 to remain in saturation)
  - with source follower, V_X must be greater than V_{GS2}+ (V_{GS3}-V_{TH3}) so that M_3 is saturated
- For comparable overdrive voltages in M_1 and M_3, allowable swing at X is reduced by V_{GS2}

Comparison of CS stage and Source Follower

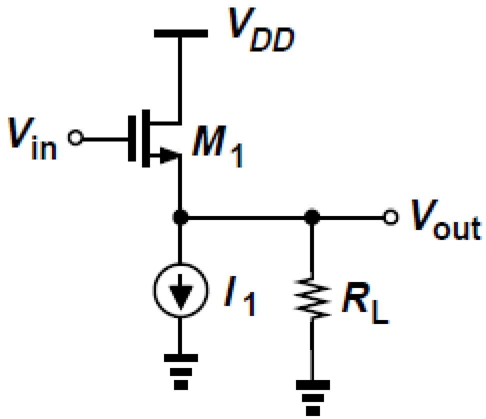


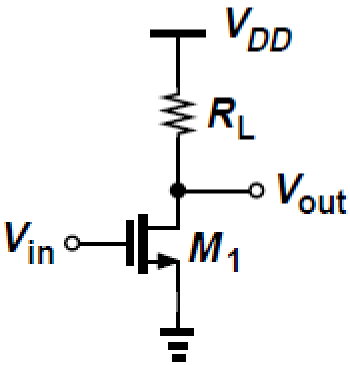


- Comparing the gain of source followers and CS stage with a low load impedance
  - E.g., driving an external 50-Ω termination in a high-frequency environment
- When load is driven by a source follower, overall voltage gain is

$$\frac{V_{out}}{V_{in}}\Big|_{SF} \approx \frac{R_L}{R_L + 1/g_{m1}} \approx \frac{g_{m1}R_L}{1 + g_{m1}R_L}.$$

Comparison of CS stage and Source Follower





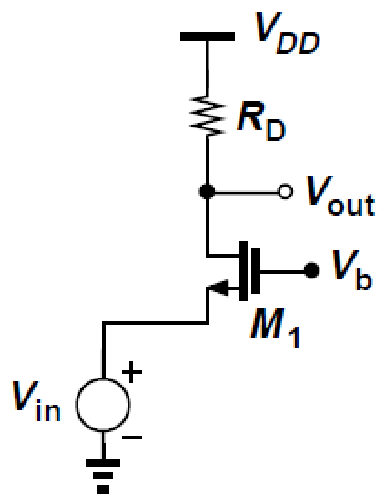
- **Load can be included as part of a common-source stage, providing a gain of**

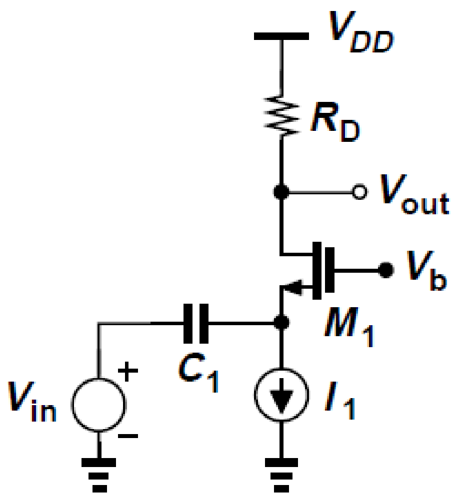
$$\frac{V_{out}}{V_{in}}|_{CS} \approx -g_{m1}R_L.$$

- **Key difference between the two topologies is the achievable voltage gain for a given bias current**
- **For example, if $1/g_{m1} \approx R_L$, source follower exhibits a gain of at most 0.5 whereas the common-source stage provides a gain close to unity**
- **Thus, source followers are not efficient drivers**

Common-Gate Stage

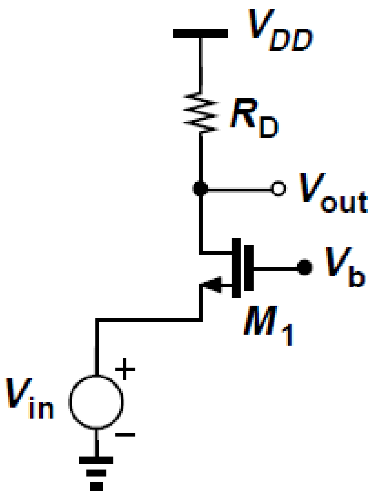
- A common-gate (CG) stage senses the input at the source and produces the output at the drain
- Gate is biased to establish proper operating conditions





- Bias current of M_1 flows through the input signal source
- Alternatively, M_1 can be biased by a constant current source, with the signal capacitively coupled to the circuit

Common-Gate Stage: Large-signal behavior



- Assume V_{in} decreases from a large positive value and that $\lambda=0$
- For $V_{in} \geq V_b - V_{TH}$, M_1 is off and $V_{out} = V_{DD}$
- For lower values of V_{in}, if M_1 is in saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2$$

- As V_{in} decreases further, so does V_{out} driving M_1 into the triode region if

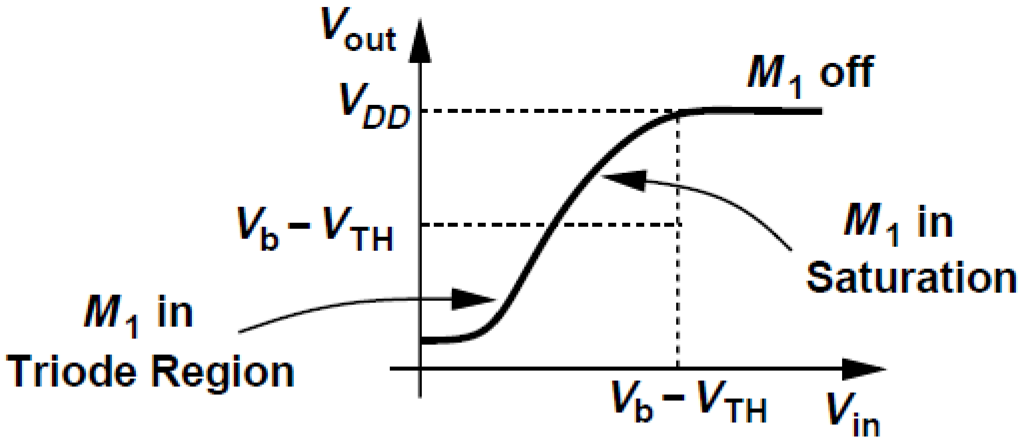
$$V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D = V_b - V_{TH}$$

- In the region where M_1 is saturated, we can express the output voltage as

$$V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D$$

Common-Gate Stage

Input-output characteristic



- **For M_1 in saturation,** $V_{out} = V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})^2 R_D$

- **Small-signal gain can thus be obtained**

$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox}\frac{W}{L}(V_b - V_{in} - V_{TH})\left(-1 - \frac{\partial V_{TH}}{\partial V_{in}}\right) R_D$$

- **Since** $\partial V_{TH}/\partial V_{in} = \partial V_{TH}/\partial V_{SB} = \eta$**, we have**

$$\begin{aligned}\frac{\partial V_{out}}{\partial V_{in}} &= \mu_n C_{ox}\frac{W}{L}R_D(V_b - V_{in} - V_{TH})(1+\eta)\\ &= g_m(1+\eta)R_D.\end{aligned}$$

Common-Gate Stage

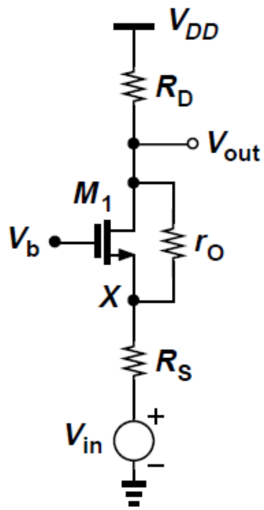
- **Gain of the common-gate (CG) stage is positive**

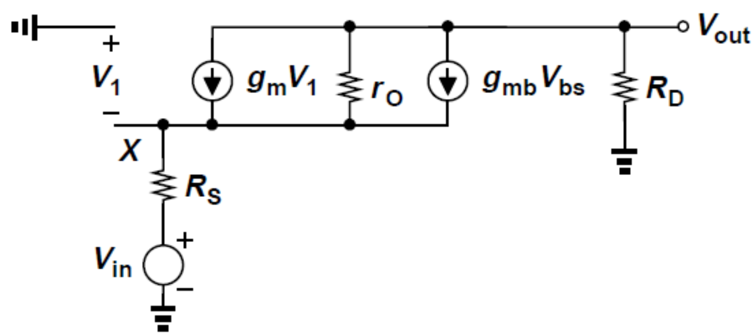
$$\begin{aligned}\frac{\partial V_{out}}{\partial V_{in}} &= \mu_n C_{ox}\frac{W}{L}R_D(V_b - V_{in} - V_{TH})(1+\eta)\\ &= g_m(1+\eta)R_D.\end{aligned}$$

- **Body effect increases the effective transconductance of the stage**
- **For a given bias current and supply voltage (i.e., a given power budget), voltage gain of the CG stage can be maximized by**
  - **Increasing gm by widening the input device, eventually reaching subthreshold operation [$g_m = I_D/\zeta V_T$]**
  - **Increasing R_D and inevitably, the dc drop across it**
- **The minimum allowable value of V_{out} is $V_{GS}-V_{TH}+V_{I1}$, where V_{I1} denotes the minimum voltage required by I_1**

Common-Gate Stage

- **Consider output impedance of transistor and impedance of the signal source**





- **In small-signal equivalent circuit, since current flowing R_S is $-V_{out}/R_D$,**

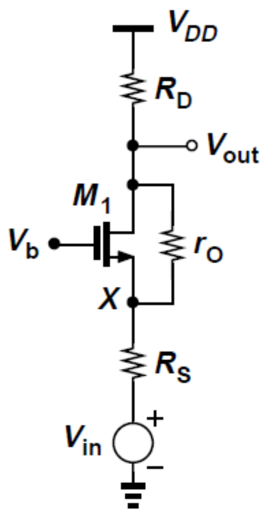
$$V_1 - \frac{V_{out}}{R_D} R_S + V_{in} = 0 \qquad \textbf{(1)}$$

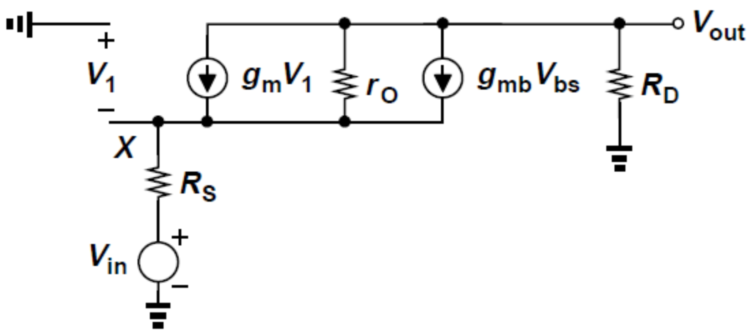
$$-V_{out}/R_D - g_m V_1 - g_{mb} V_1$$

- **Moreove**

$$r_O \left(\frac{-V_{out}}{R_D} - g_m V_1 - g_{mb} V_1 \right) - \frac{V_{out}}{R_D} R_S + V_{in} = V_{out} \qquad \textbf{(2)}$$

Common-Gate Stage





- **Substituting *V*₁ from (1) in (2),**

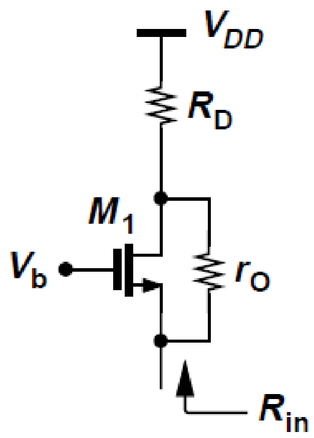
$$r_O\left[\frac{-V_{out}}{R_D}-(g_m+g_{mb})\left(V_{out}\frac{R_S}{R_D}-V_{in}\right)\right]-\frac{V_{out}R_S}{R_D}+V_{in}=V_{out}$$

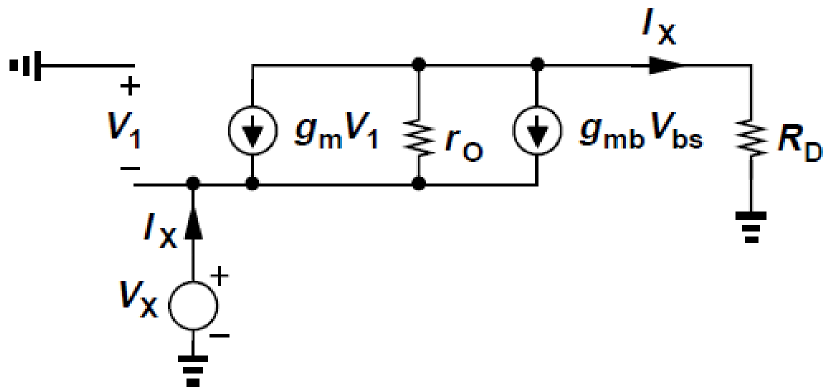
- **Therefore,**

$$\frac{V_{out}}{V_{in}}=\frac{(g_m+g_{mb})r_O+1}{r_O+(g_m+g_{mb})r_OR_S+R_S+R_D}R_D$$

- **The voltage gain expression is similar to that of a degenerated CS stage**

Common-Gate Stage: Input Impedance





- **From the small-signal equivalent circuit for finding input impedance, we have**

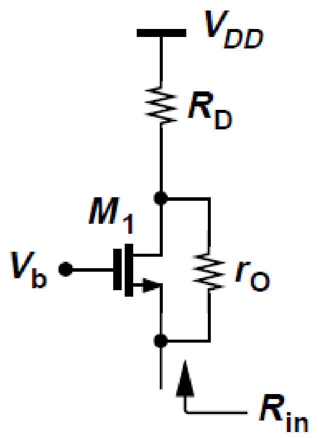
$$V_1 = -V_X$$

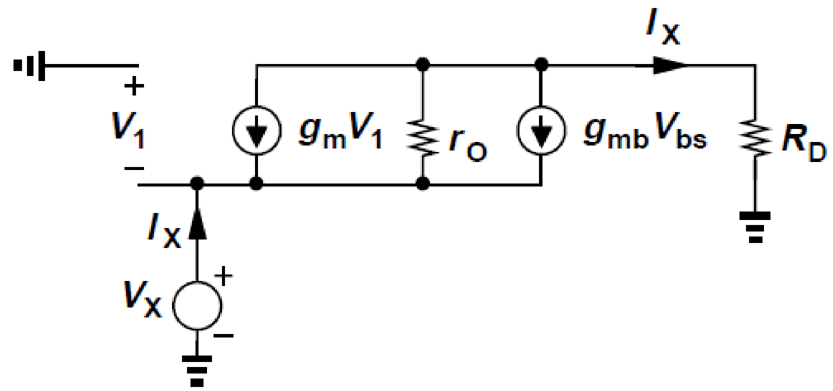
- **The current through r_O is equal to $I_X + g_m V_1 + g_{mb} V_1 = I_X - (g_m + g_{mb}) V_X$**

- **Voltages across r_O and R_D can be added and equated to**

$$R_D I_X + r_O[I_X - (g_m + g_{mb})V_X] = V_X$$

Common-Gate Stage: Input Impedance





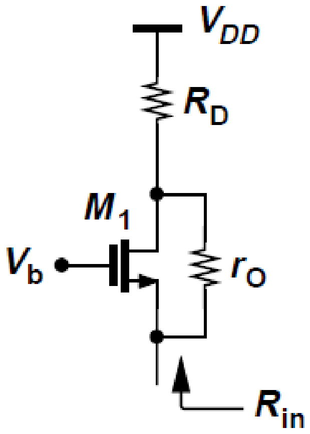
- **Thus,**

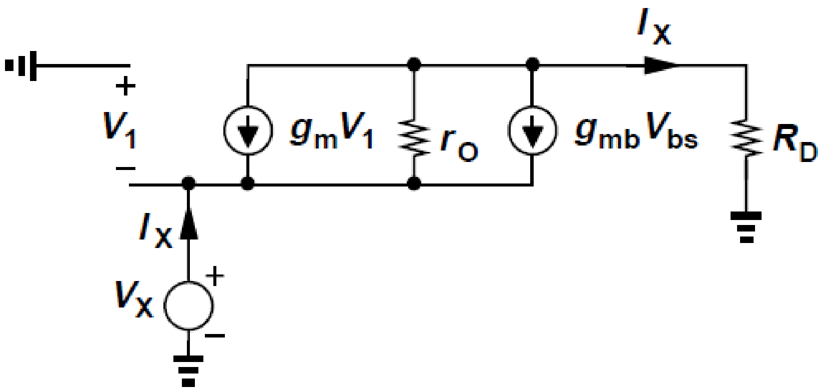
$$\frac{V_X}{I_X} = \frac{R_D + r_O}{1 + (g_m + g_{mb})r_O}$$
$$\approx \frac{R_D}{(g_m + g_{mb})r_O} + \frac{1}{g_m + g_{mb}}.$$

If $(g_m + g_{mb})r_O >> 1$

- **The drain impedance is divided by $(g_m + g_{mb})r_O$ when seen at the source**
  - **Important in short-channel devices because of their low intrinsic gain**

Common-Gate Stage: Input Impedance



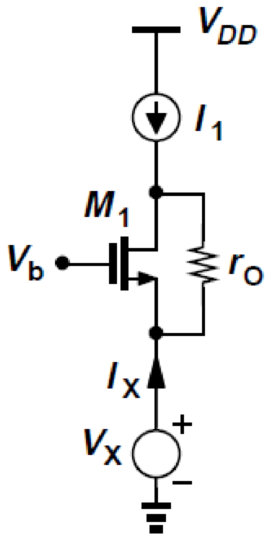


- **Suppose $R_D = 0$, then**

$$\frac{V_X}{I_X} = \frac{r_O}{1 + (g_m + g_{mb})r_O}$$
$$= \frac{1}{\frac{1}{r_O} + g_m + g_{mb}},$$

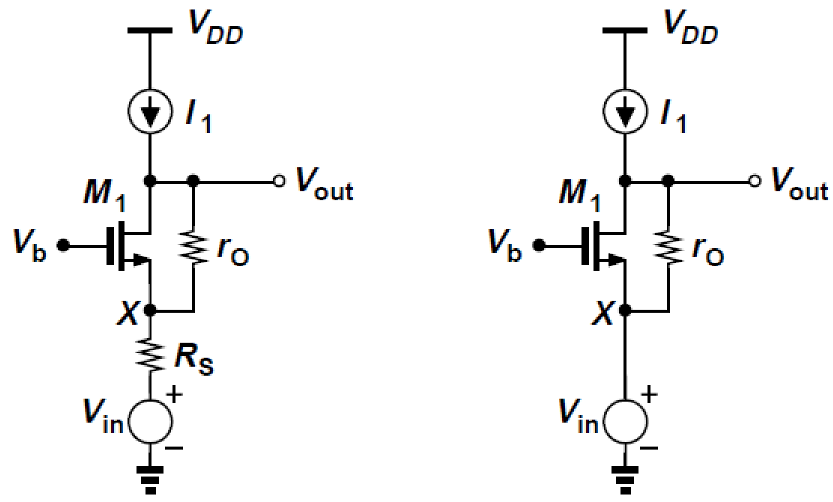
- **This is the impedance seen at the source of a source follower, a predictable result since with $R_D = 0$ the circuit configuration is the same as a source follower**

Common-Gate Stage: Input Impedance



- If R_D is replaced with an ideal current source, earlier result predicts that input impedance approaches infinity
- Total current through the transistor is fixed and is equal to I_1
- Therefore, a change in the source potential cannot change the device current, and hence $I_X = 0$
- The input impedance of a CG stage is relatively low *only* if the load impedance connected to the drain is small

Common-Gate Stage

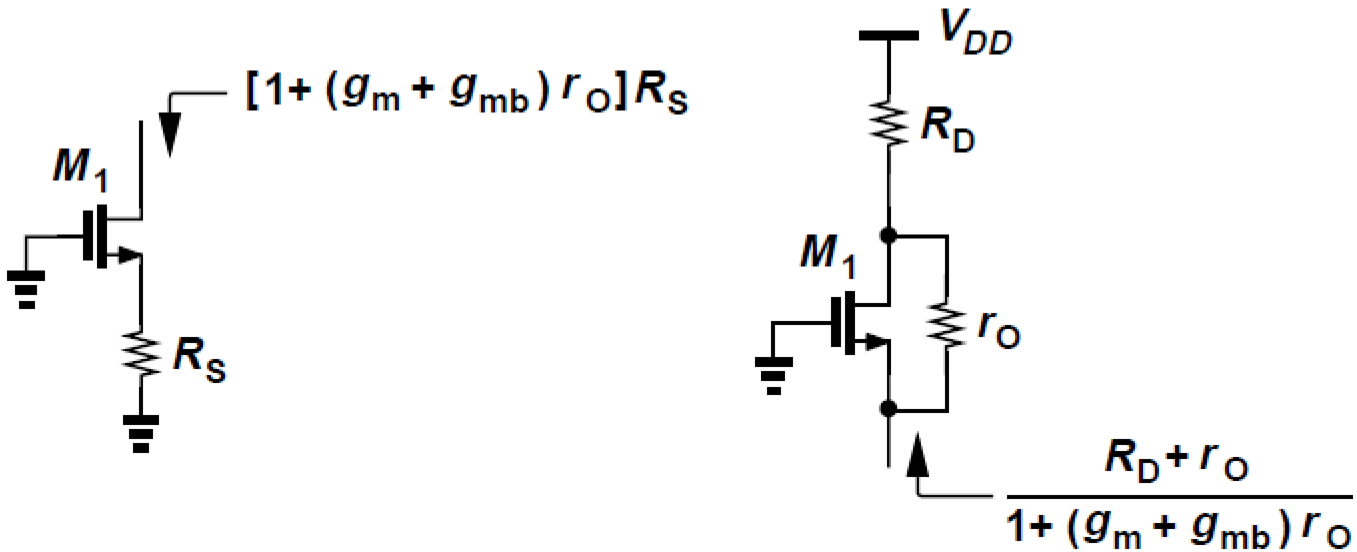


- **In a CG stage with a current source load, substituting R_D=∞ in the voltage gain equation, we get**

$$A_v = (g_m + g_{mb})r_O + 1$$

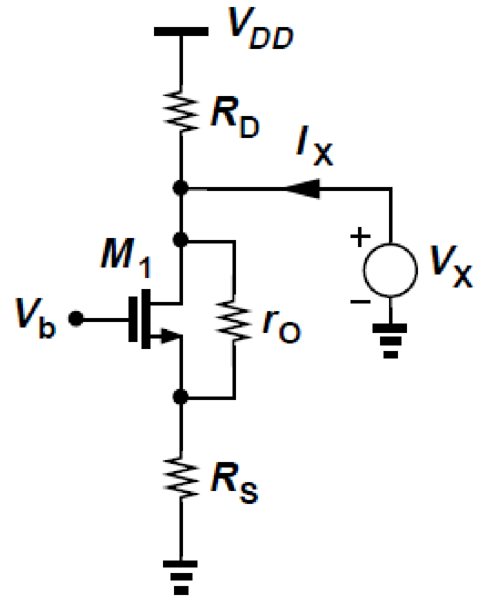
- **Gain does not depend on R_S**
- **From the foregoing discussion, if $R_D \rightarrow \infty$, so does the impedance seen at the source of M_1, and the small-signal voltage at node X becomes equal to V_{in}**

Common-Gate Stage



- **In a degenerated CS stage, we loosely say that a transistor transforms its source resistance *up***
- **In a CG stage, the transistor transforms its drain resistance *down***
- **The MOS transistor can thus be viewed as an resistance transformer**

Common-Gate Stage: Output Impedance



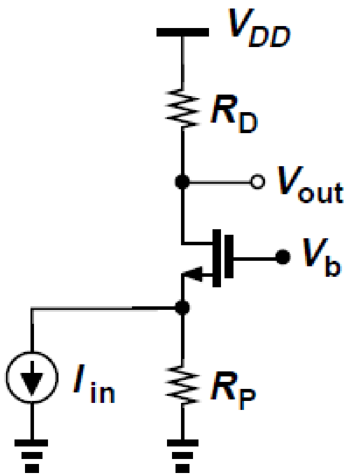
- **From the above small-signal equivalent circuit, we can find output impedance as**

$$R_{out} = \{[1 + (g_m + g_{mb})r_O]R_S + r_O\}||R_D$$

- **Result is similar to that obtained for a degenerated CS stage**

Common-Gate Stage

- Input signal of a common-gate stage may be a current rather than a voltage as shown below



- Input current source exhibits output impedance of R_P
- To find the "gain" V_{out}/I_{in}, replace I_{in} and R_P with a Thevenin equivalent and use derived result to write

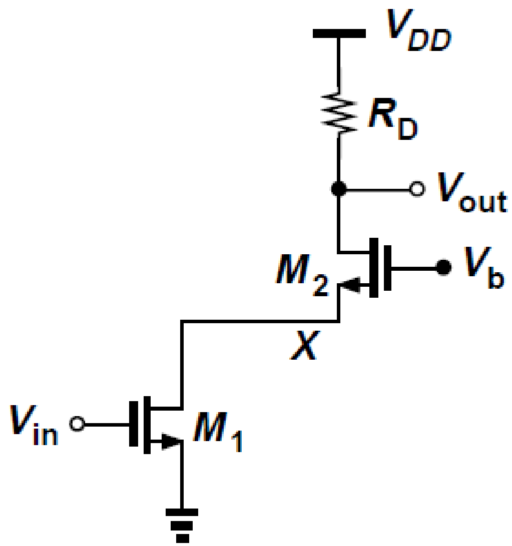
$$\frac{V_{out}}{I_{in}} = \frac{(g_m + g_{mb})r_O + 1}{r_O + (g_m + g_{mb})r_O R_P + R_P + R_D} R_D R_P$$

- Output impedance is simply given by

$$R_{out} = \{[1 + (g_m + g_{mb})r_O]R_P + r_O\} || R_D$$

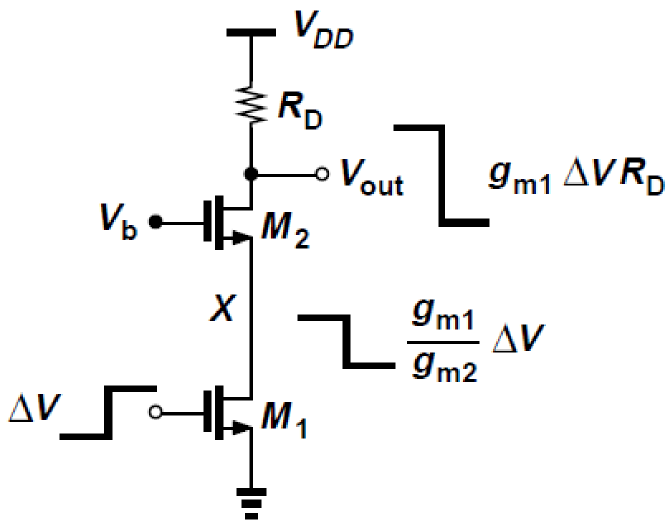
Cascode Stage

- The cascade of a CS stage and a CG stage is called a cascode topology



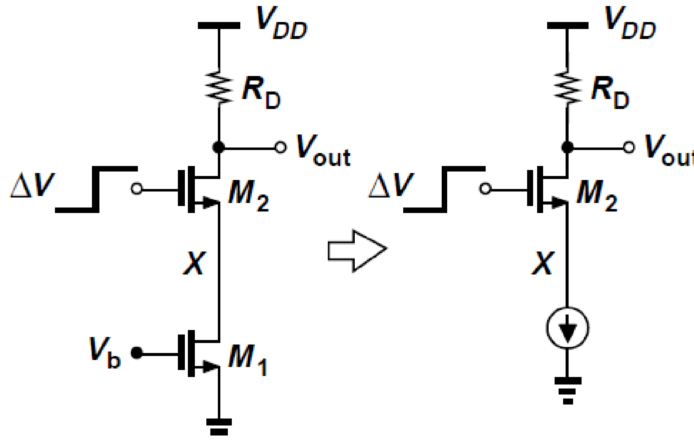
- M_1 generates a small-signal drain current proportional to the small-signal input V_{in} and M_2 simply routes the current to R_D
- M_1 is called the input device and M_2 the cascode device
- M_1 and M_2 in this example carry equal bias and signal currents
  - Topology also called as "telescopic cascode"

Cascode Stage: Qualitative Analysis



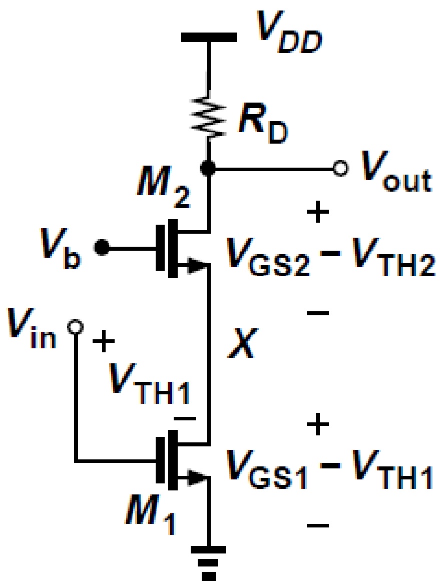
- **Assume both transistors are in saturation and $\lambda = \gamma = 0$**
- **If V_{in} rises by ΔV, then I_{D1} increases by $g_{m1}\Delta V$**
- **This change in current flows through the impedance seen at X, i.e., the impedance seen at the source of M_2, which is equal to $1/g_{m2}$**
- **Thus, V_X falls by an amount given by $g_{m1}\Delta V \cdot (1/g_{m2})$**
- **This change in I_{D1} also flows through R_D, producing a drop of $g_{m1}\Delta V R_D$ in V_{out}, just as in a simple CS stage**

Cascode Stage: Qualitative Analysis



- **Consider the case when V_{in} is fixed and V_b increases by ΔV**
- **Since V_{GS1} is constant and $r_{O1}=\infty$, M_1 can be replaced by an ideal current source**
- **For node X, M_2 operates as a source follower, it senses an input ΔV at its gate and generates an output at X**
- **With $\lambda = \gamma = 0$, the small-signal voltage of the follower is unity regardless of R_D**
- **V_X rises by *ΔV, but* V_{out} does not change since *$I_{D2}=I_{D1}$=constant, thus voltage gain from V_b to* V_{out} *is zero***

Cascode Stage: Bias Conditions



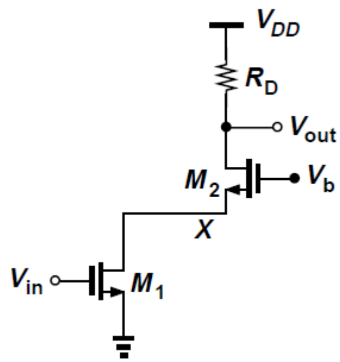
- For M_1 to operate in saturation, we must have $V_X \geq V_{in} - V_{TH1}$
- If M_1 and M_2 are both in saturation, M_2 operates as a source follower and V_X is primarily determined by V_b: $V_X = V_b - V_{GS2}$
- Thus $V_b - V_{GS2} \geq V_{in} - V_{TH1}$ and hence $V_b > V_{in} + V_{GS2} - V_{TH1}$
- For M_2 to be saturated, $V_{out} \geq V_b - V_{TH2}$
- Thus,

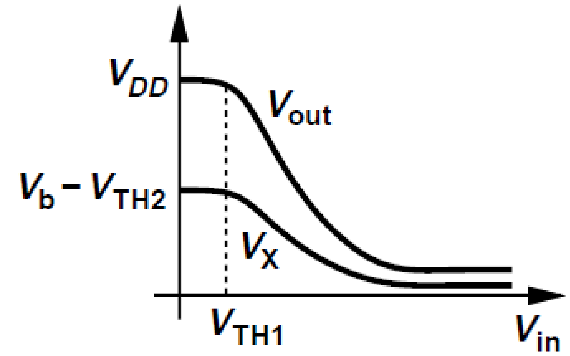
$$\begin{aligned} V_{out} &\geq V_{in} - V_{TH1} + V_{GS2} - V_{TH2} \\ &= (V_{GS1} - V_{TH1}) + (V_{GS2} - V_{TH2}) \end{aligned}$$

if V_b is chosen to place M_1 at the edge of saturation

- Minimum output level for which both transistors are in saturation is equal to the sum of overdrives of M_1 and M_2
- Addition of M_2 to the circuit reduces the output voltage swing by at least its overdrive voltage

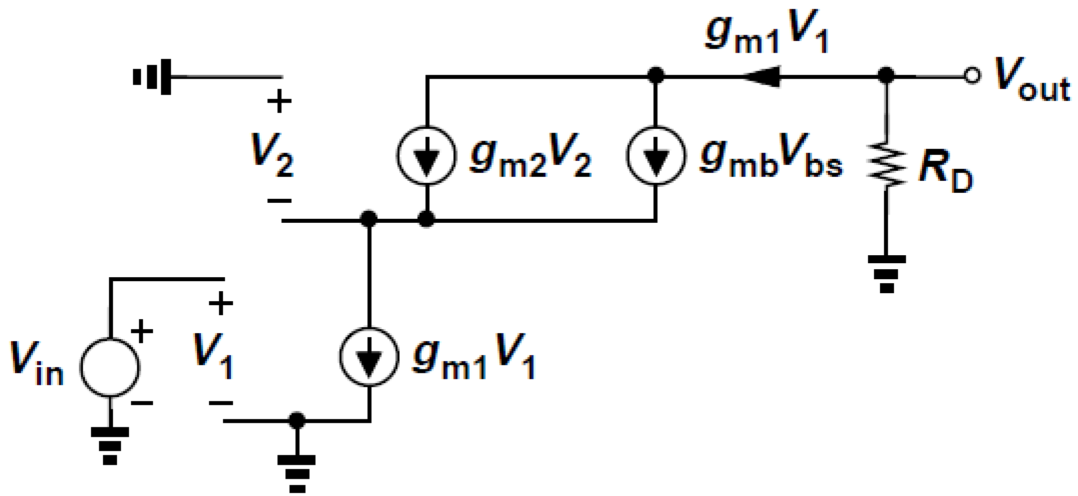
Cascode Stage: Large-Signal Behavior





- **For $V_{in} \leq V_{TH1}$, M_1 and M_2 are off, $V_{out}=V_{DD}$, and $V_X \approx V_b - V_{TH2}$**
- **As V_{in} exceeds V_{TH1}, M_1 draws current, and V_{out} drops**
- **Since I_{D2} increases, V_{GS2} must increase as well, causing V_X to fall**
- **As V_{in} becomes sufficiently large, two effects can occur:**
  - **V_X falls below V_{in} by V_{TH1}, forcing M_1 into the triode region**
  - **V_{out} drops below V_b by V_{TH2}, driving M_2 into triode region**
- **Depending on device dimensions and R_D and V_b, one effect may occur before the other**

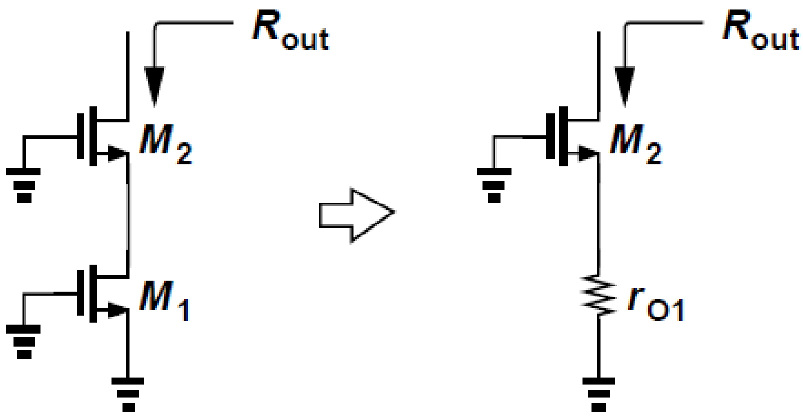
Cascode Stage: Small-signal characteristics



- Assume both transistors operate in saturation and *λ*=0
- Voltage gain is equal to that of a common-source stage because the drain current produced by the input device must flow through the cascode device
- This result is independent of the transconductance and body effect of M_2, the cascode device
- Can be verified using $A_v = -G_m R_{out}$

Cascode Stage: Output Impedance

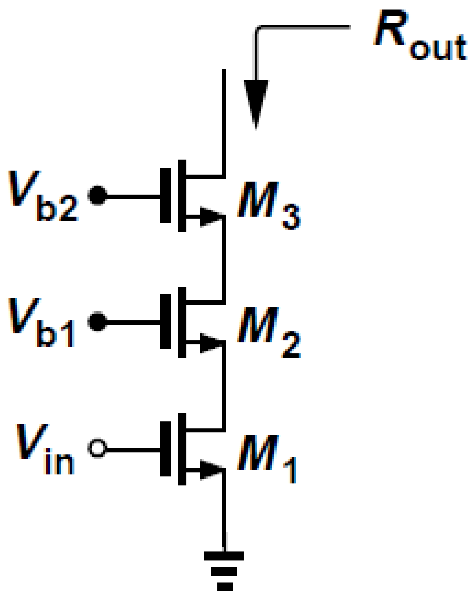
- Important property of the cascode structure is its high output impedance



- For calculation of R_{out}, the circuit can be viewed as a common-source stage with a degeneration resistor equal to r_{O1}
- Thus, $$R_{out} = [1 + (g_{m2} + g_{mb2})r_{O2}]r_{O1} + r_{O2}$$
- Assuming $g_m r_O >> 1$, we have $$R_{out} \approx (g_{m2} + g_{mb2})r_{O2}r_{O1}$$
- M2 boosts the output impedance of M1 by a factor of $(g_{m2}+g_{mb2})r_{O2}$

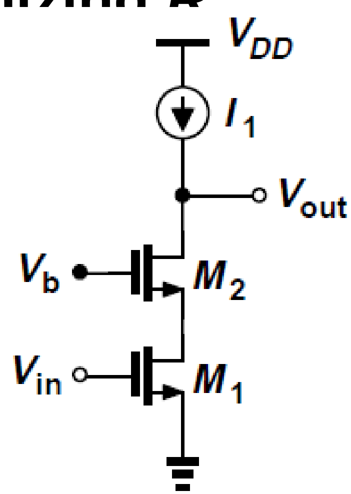
Triple Cascode

- **Cascoding can be extended to three or more stacked devices to achieve higher output impedance**
- **But required additional voltage headroom makes it less attractive**
- **For a triple cascode, the minimum output voltage is equal to the sum of three overdrive voltages**



Cascode stage with current source load

- **Voltage gain can be maximized by maximizing G_m and/or R_{out}**
- **Since G_m is typically determined by the transconductance of a transistor and has trade-offs with the bias current and device capacitances, it is desirable to increase voltage gain by maximizing R**

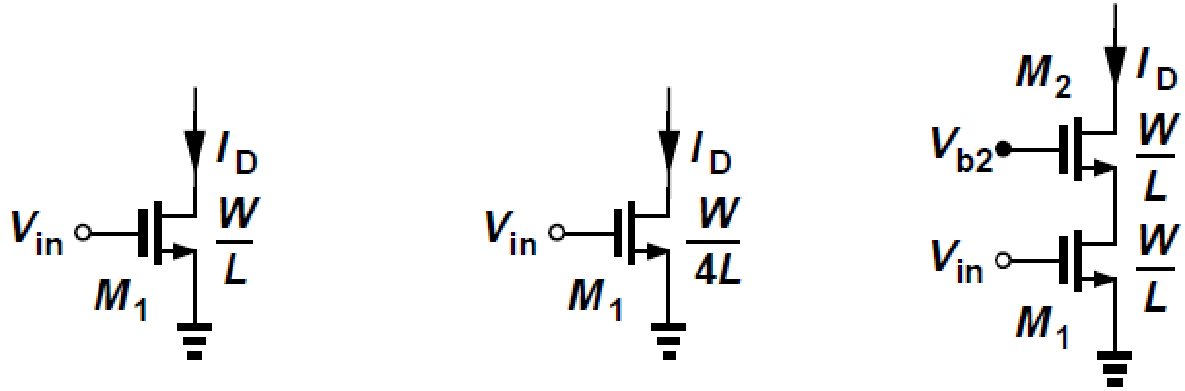


$$G_m \approx g_{m1}$$

$$R_{out} \approx (g_{m2}+g_{mb2})r_{O2}r_{O1}$$

$$A_v = (g_{m2}+g_{mb2})r_{O2}g_{m1}r_{O1}$$

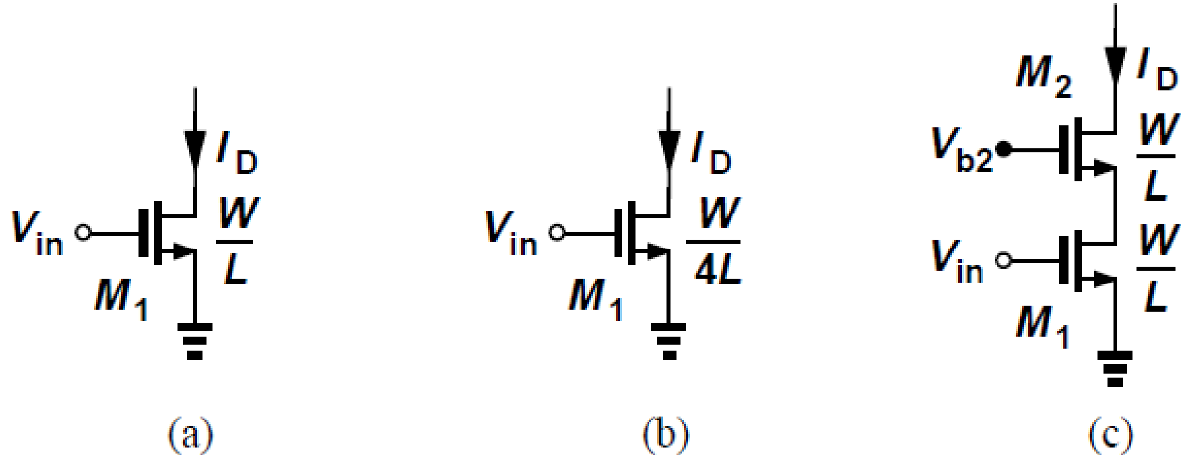
Cascode Stage vs Increasing Length



(a) (b) (c)

- Increasing length of the input transistor for a given bias current increases the output impedance
- Suppose the length of the input transistor is quadrupled while the width remains constant
- Since $I_D = (1/2)\mu_n C_{ox}(W/L)(V_{GS} - V_{TH})^2$, the overdrive voltage is doubled and the transistor consumes the same amount of voltage headroom as does a cascode stage, i.e., circuits in (b) and (c) impose equal voltage swing constraints

Cascode Stage vs Increasing Length

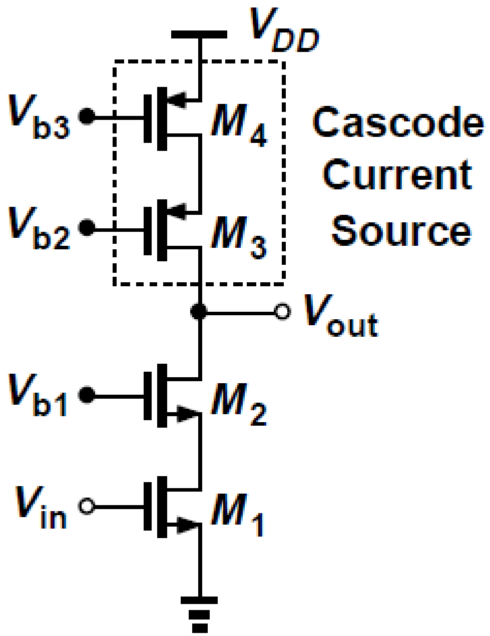


- **Since**

$$g_m r_O = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}\frac{1}{\lambda I_D}$$

- **And $\lambda \propto 1/L$, quadrupling *L* only doubles the value of $g_m r_O$ while cascoding results in an output impedance of roughly $g_m r_O^2$**
- **Transconductance of M_1 in (b) is only half of that in (c), degrading the performance**
- **For a given voltage headroom, the cascode structure provides a higher output impedance**

Cascode Structure as Current Source



- High output impedance of cascode structure yields a current source closer to the ideal, but at the cost of voltage headroom
- The current source load in a cascode stage can be implemented as a PMOS cascode, exhibiting an impedance equal to

$$[1 + (g_{m3} + g_{mb3})r_{O3}]r_{O4} + r_{O3}$$

- To find the voltage gain, $G_m \approx g_{m1}$
- Rout is the parallel combination of the NMOS and PMOS cascode output impedances

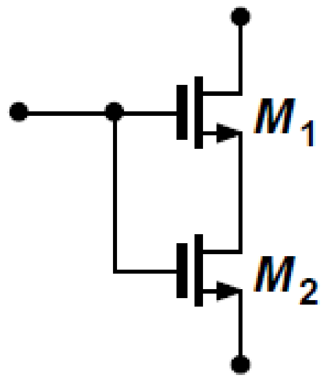
$$R_{out} = \{[1 + (g_{m2} + g_{mb2})r_{O2}]r_{O1} + r_{O2}\}||\{[1 + (g_{m3} + g_{mb3})r_{O3}]r_{O4} + r_{O3}\}$$

- The gain is given by $|A_v| \approx g_{m1} R_{out}$
- For typical values, this is approximated as

$$|A_v| \approx g_{m1}[(g_{m2}r_{O2}r_{O1})||(g_{m3}r_{O3}r_{O4})]$$

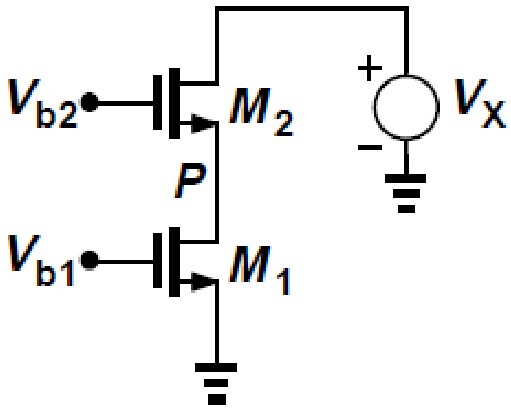
Poor Man's Cascode

- A "minimalist" cascode current source omits the bias voltage necessary for the cascode device



- Called "poor man's cascode", M_2 is placed in the triode region because $V_{GS1}>V_{TH1}$ and $V_{DS2}=V_{GS2}-V_{GS1} < V_{GS2}-V_{TH2}$
- If M_1 and M_2 have the same dimensions, the structure is equivalent to a single transistor having twice the length- not really a cascode
- In modern CMOS technologies, transistors with different threshold voltages are allowable, allowing M_2 to operate in saturation if M_1 has a lower threshold than M_2

Poor Man's Cascode: Shielding Property



- High output impedance arises from the fact that if the output node voltage is changed by ΔV, the resulting change at the source of the cascode device is much less
  - Cascode transistor "shields" the input device from voltage variations at the output

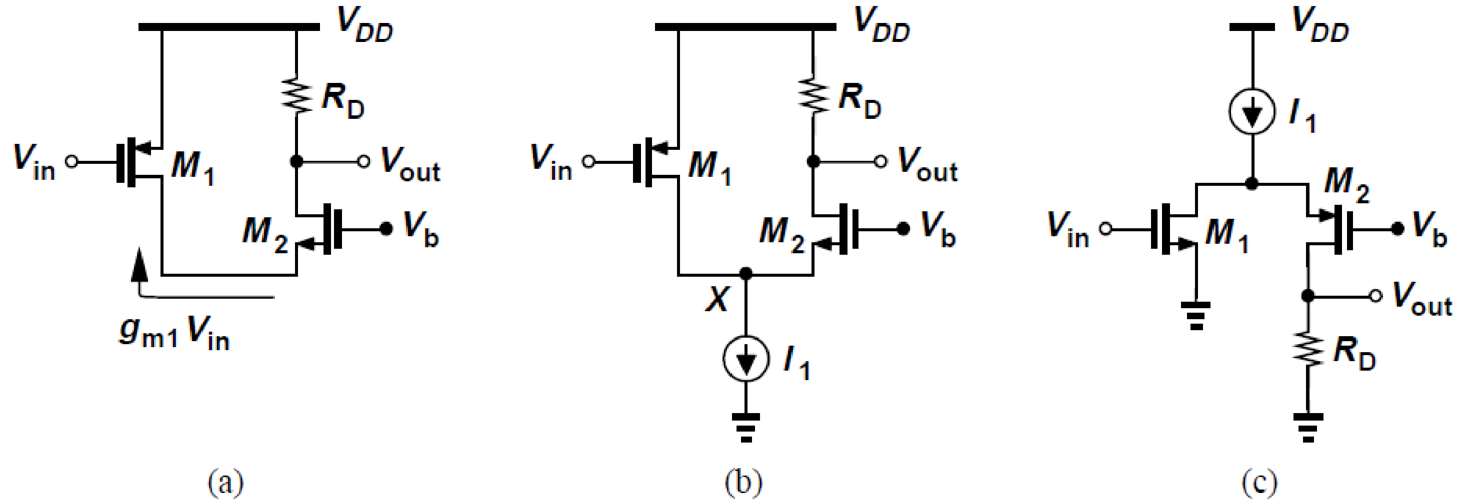
- Shielding property diminishes if cascode device enters triode region
- In above circuit, as V_X falls below V_{b2}-V_{TH2}, M_2 enters triode region and requires a greater gate-source overdrive to sustain the current drawn by M_1 therefore

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 [2(V_{b2} - V_P - V_{TH2})(V_X - V_P) - (V_X - V_P)^2]$$

- As V_X decreases, V_P also drops to keep I_{D2} constant so variation of V_X is less attenuated as it appears at P

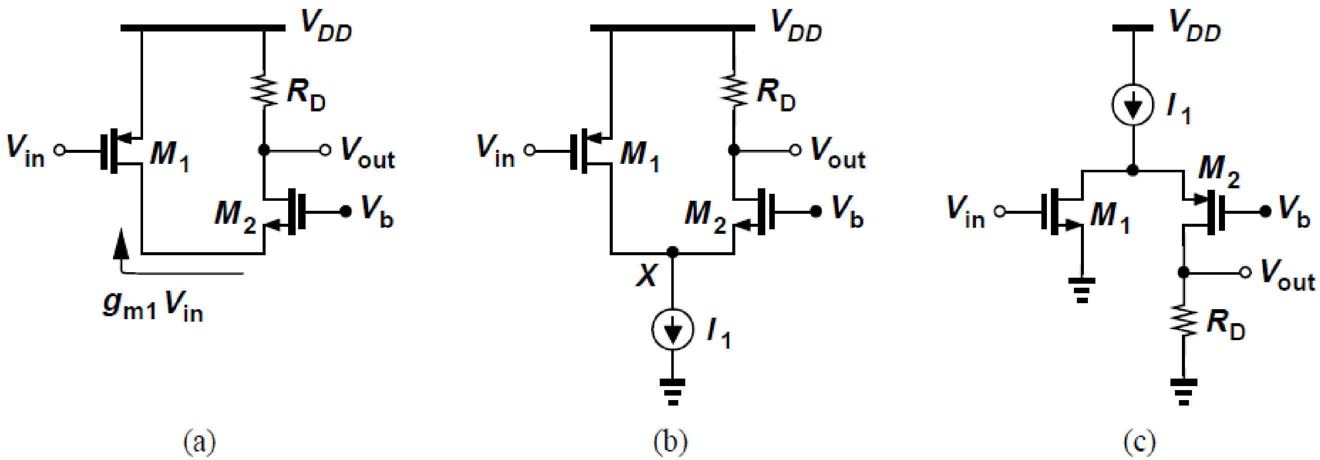
Folded Cascode

- The input device and the cascode device in a cascode structure need not be of the same type



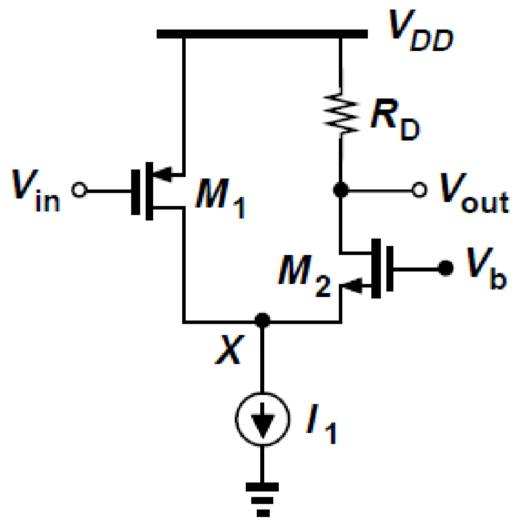
- In the figure above, (a) shows a PMOS-NMOS cascode combination that performs the same function as a telescopic cascode
- In order to bias M_1 and M_2, a current source must be added as shown in (b)
- $|I_{D1}| + I_{D2}$ is equal to I_1 and hence constant
- (c) shows an NMOS-PMOS folded cascode

Folded Cascode: Small-signal operation



- **If V_{in} becomes more positive, $|I_{D1}|$ decreases, forcing I_{D2} to increase and hence V_{out} to drop**
- **The voltage gain and output impedance can be obtained as calculated for the NMOS-NMOS cascode shown earlier**
- **(b) and (c) are called "folded cascode" stages because the small-signal current is "folded" up [in (b)] or down [in (c)]**
- **In the telescopic cascode, the bias current is reused whereas those of M_1 and M_2 add up to I_1 in (b) and (c), leading to a higher bias current**

Folded Cascode: Large-signal operation

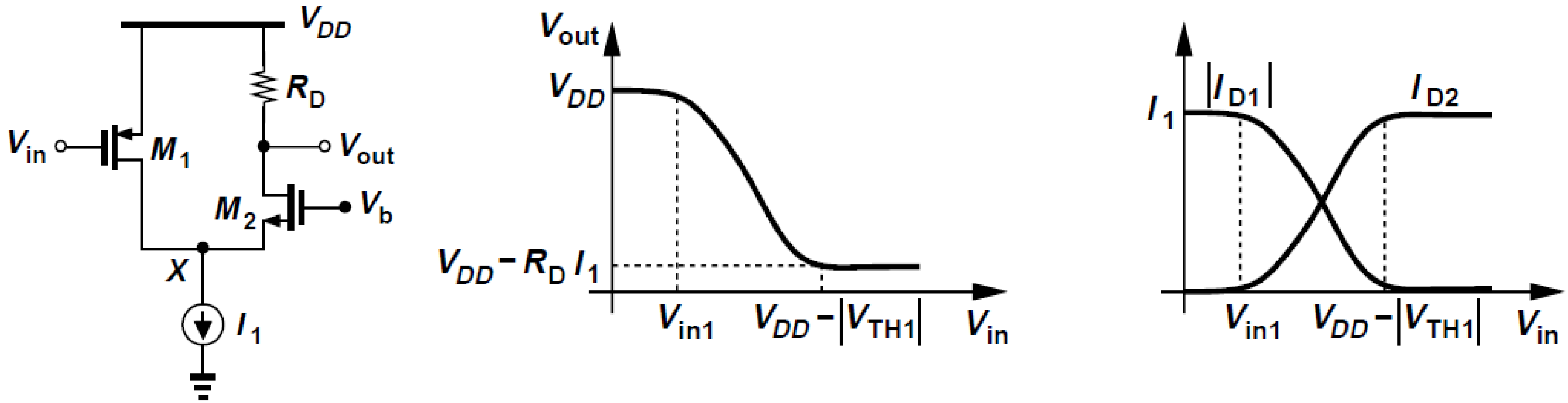


- Suppose V_{in} decreases from V_{DD} to zero
- For $V_{in} > V_{DD}-|V_{TH1}|$, M_1 is off and M_2 carries all of I_1, yielding $V_{out} = V_{DD} - I_1R_D$
- For $V_{in} < V_{DD} - |V_{TH1}|$, M_1 turns on in saturation, giving

$$I_{D2} = I_1 - \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_{DD} - V_{in} - |V_{TH1}|)^2.$$

- As V_{in} drops, I_{D2} decreases further, falling to zero if $I_{D1}=I_1$

Folded Cascode: Large-signal operation



- **This occurs at $V_{in} = V_{in1}$ if**

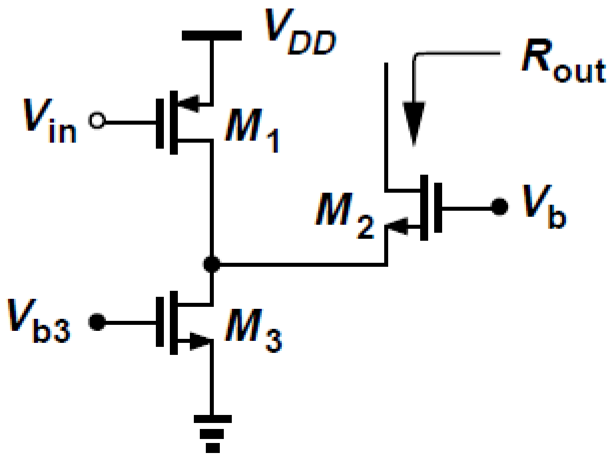
$$\frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_{DD} - V_{in1} - |V_{TH1}|)^2 = I_1$$

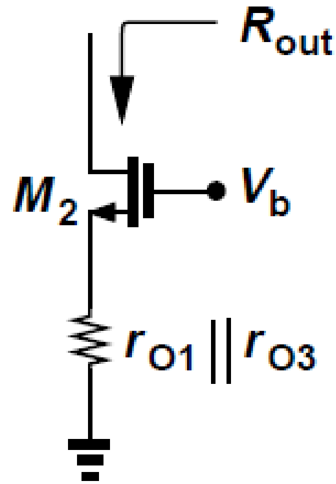
- **Thus,**

$$V_{in1} = V_{DD} - \sqrt{\frac{2I_1}{\mu_p C_{ox}(W/L)_1}} - |V_{TH1}|$$

- **If V_{in} falls below this level, I_{D1} tends to be greater than I_1 and M_1 enters the triode region to ensure I_{D1}=I_1**
- **As I_{D2} drops, V_X rises, reaching V_b-V_{TH2} for I_{D2}=0**
- **As M_1 enters the triode region, V_X approaches V_{DD}**

Folded Cascode: Output Impedance





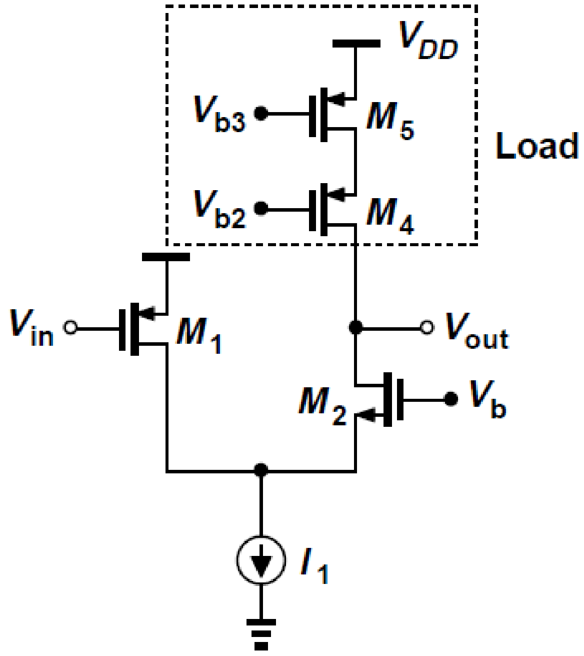
- **M_3 operates as the bias current source**
- **Using earlier results,**

$$R_{out} = [1 + (g_{m2} + g_{mb2}) r_{O2}](r_{O1} || r_{O3}) + r_{O2}$$

- **The circuit exhibits a lower output impedance than a nonfolded (telescopic) cascode**

Folded Cascode with cascode load

- **To achieve a high voltage gain, the load of a folded cascode can be implemented as a cascode itself**



- **Increasing the output resistance of voltage amplifiers to obtain a high gain may make the speed of the circuit susceptible to the load capacitance**
- **A high output impedance itself does not pose a serious issue if the amplifier is placed in a proper feedback loop**