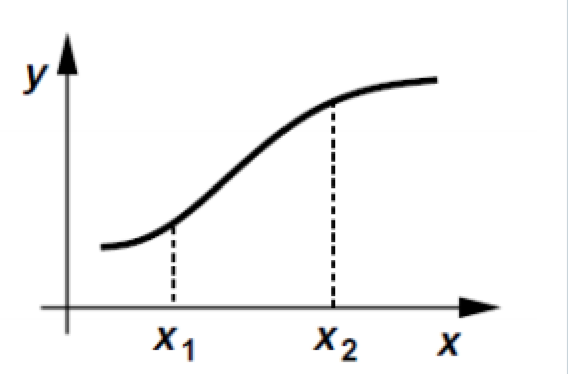
SINGLE STAGE AMPLIFIER

BASIC CONCEPTS, COMMON SOURCE STAGE, SOURCE FOLLOWER, COMMON GATE STAGE, CASCODE STAGE

Ideal vs Non-ideal Amplifier

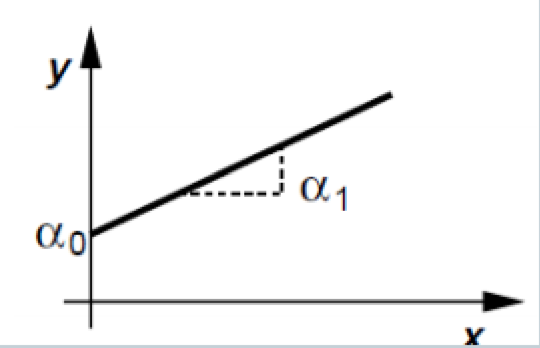
- The input and output characteristics of an amplifier is generally a nonlinear function as shown in fig.(Nonlinear amplifier)

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \cdots + \alpha_n x^n(t)$$



- Input and output may be current or voltage quantities
- For an ideal amplifier

$$y(t) = \alpha_0 + \alpha_1 x(t)$$



- α_o is the "dc bias"(operating point)
- α_1 is the "small signal gain"

$$y(t) = \alpha_0 + \alpha_1 x(t)$$

- As long as $\alpha_1 x(t) << \alpha_o$, the bias point is disturbed negligibly and higher order terms are insignificant.

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \cdots + \alpha_n x^n(t)$$

- $\Delta y = \alpha_1 \Delta x$, indicating a linear relationship between the increments at the input and output.
- As x(t) increases in magnitude, higher order terms manifest themselves. Leading to nonlinearity and necessitating large signal analysis.
- Causes distortion of signal of interest

Analog Design Trade off

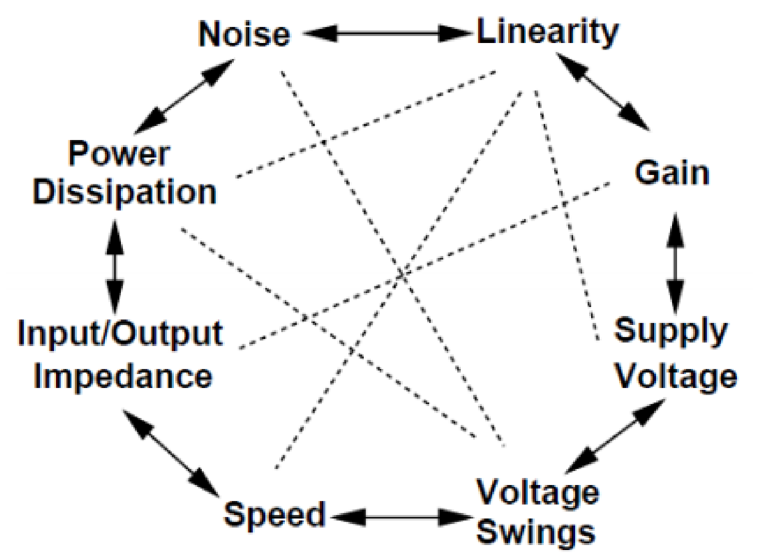
(What aspects of the performance of an amplifier are important?)

- Along with gain and speed, such parameters as power dissipation, supply voltage, linearity, noise or maximum voltage swing may be important.
- Input and output impedances decide interaction with preceding and subsequent stages
- Performance parameters trade with each other

– Multi-dimensional optimization problem

design of analog circuits is the art of finding the right trade-off between conflicting constraints or specifications such as power, noise, linearity, gain, supply voltage, voltage swing, speed and input/output impedance as illustrated by the "analog design octagon"

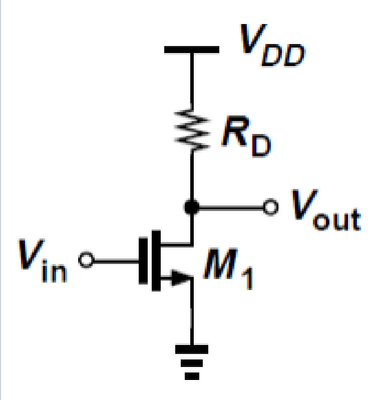
Analog-Design Octagon

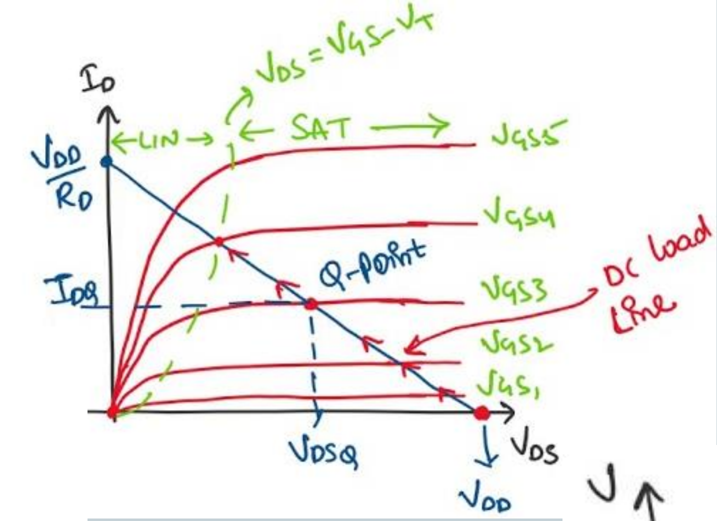


Such trade-offs present many challenges in the design of high-performance amplifiers, requiring intuition and experience to arrive at an acceptable compromise

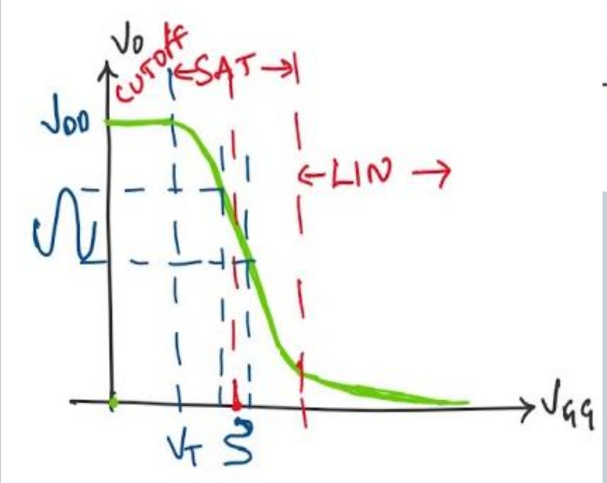
Common-Source stage with Resistive load

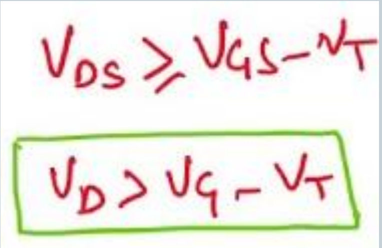
- By virtue of MOSFET's transconductance,, a MOSFET changes in its gate-source voltage to a small-signal drain current, which can pass through a resistor to generate an output voltage
- DC Analysis:

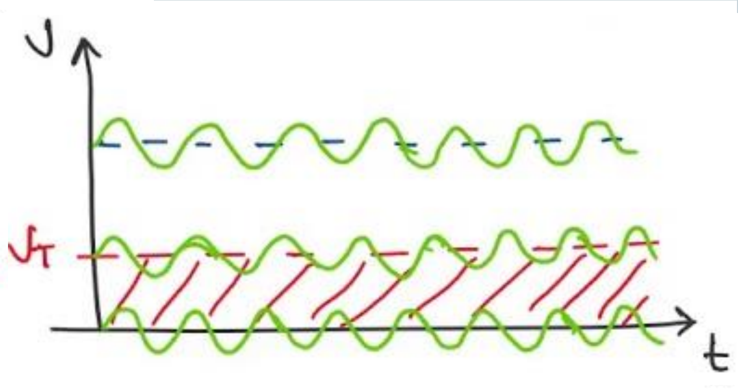




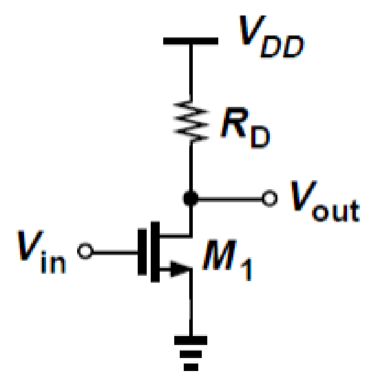
> in Linear region MOSFET works as linear voltage controlled resistor
> so, MOSFET should be in saturation to works as amplifier







Common-Source stage with Resistive load



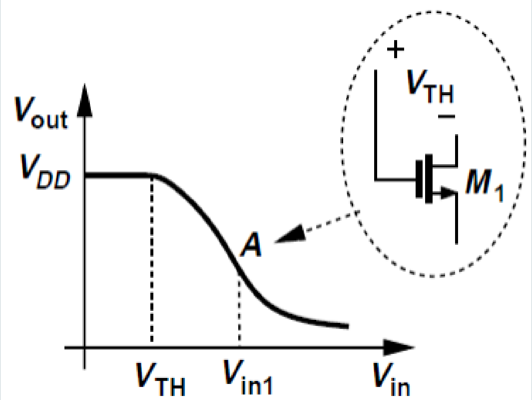
- **For Vin < VTH**,
  - M1is off
  - and Vout = VDD
- **When Vin is slightly greater then Vth,**
  - M1is ON and operates in saturation
  - If Vin is increased in small amount, there will be large amount of Vout decreases

➢ As Vin approaches Vth, M1 begins to turn on, drawing current from Rd and lowering Vout.

➢ M1 turns ON in saturation regardless of the Values of Vdd and Rd.

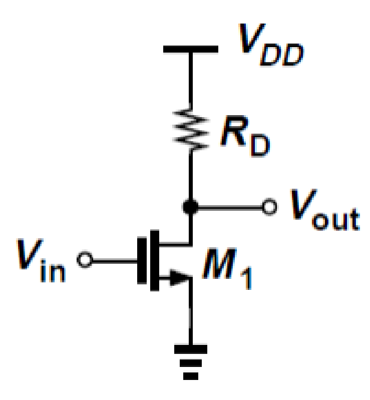
$$Vout = Vdd - IdRd$$

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2 \quad \text{—— } 1$$



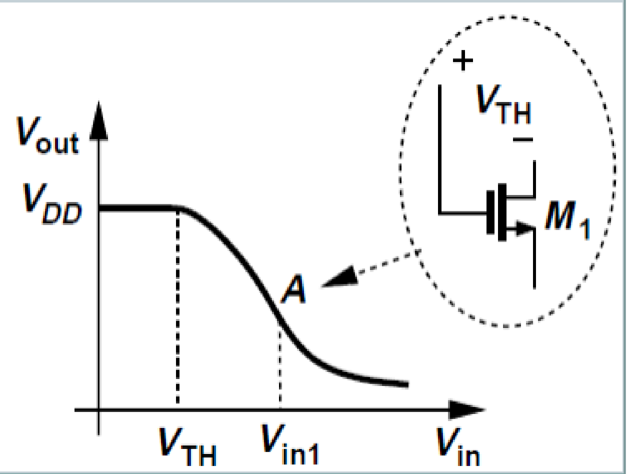
Common-Source stage with Resistive load

- Further increase in Vin, Vout drops more and the transistor continues to operates in saturation until Vin exceeds Vout by Vth.
- **At point A Vout = Vin1 -Vth**
- **<u>When Vin > Vin1</u>**
  - M1is ON and operates in Linear / Triode
  - Vout decreases



$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2(V_{in} - V_{TH})V_{out} - V_{out}^2\right] \quad (2)$$

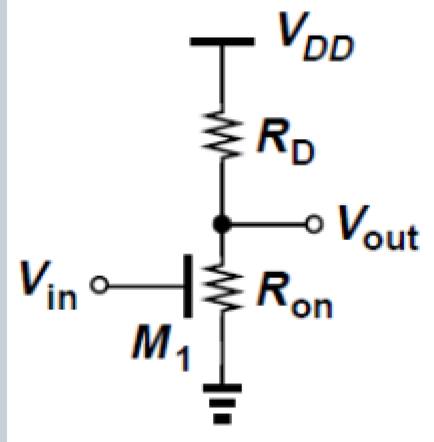
- **When Vin is high enough →**



Common-Source stage with Resistive load

- **When Vin is high enough** →

M1 drive into deep triode region, Vout << 2(vgs-Vth) and the equivalent circuit is



$$V_{out} = V_{DD}\frac{R_{on}}{R_{on}+R_D}$$

$$= \frac{V_{DD}}{1+\mu_n C_{ox}\frac{W}{L}R_D(V_{in}-V_{TH})} \quad \text{—— (3)}$$

But $g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})$

gm = 1/Ron = Ids/Vout

Ron = $\frac{\text{Vout}}{\text{ID}}$

Rout = $\frac{\text{Vout}}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2]}$

Since Vout is very low after point A in input and output characteristics

$$\boxed{R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})}}$$

Common-Source stage with Resistive load

- Taking derivative of ID equation in saturation region,

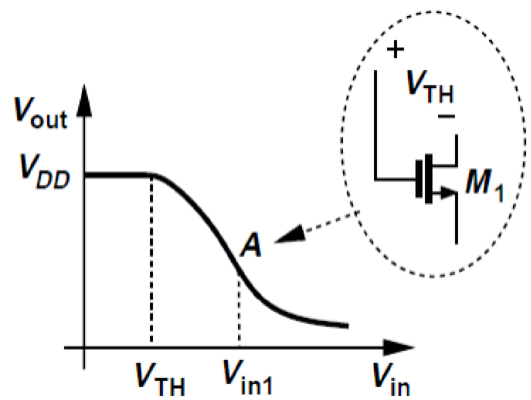
small-signal gain is obtained

$$A_v = \frac{\partial V_{out}}{\partial V_{in}}$$

Using equation (1)

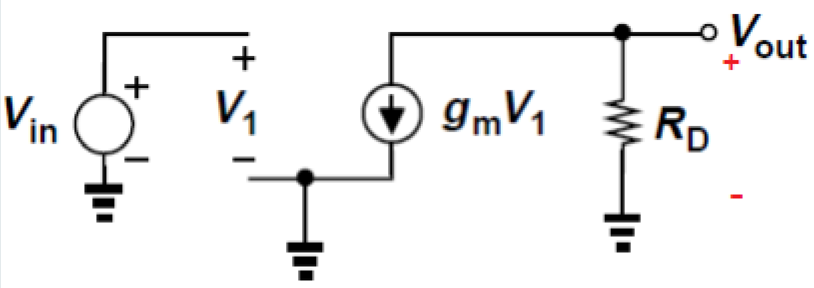
$$A_v = -R_D \mu_n C_{ox} \frac{W}{L}(V_{in} - V_{TH})$$

$$A_v = -g_m R_D. \qquad (4)$$



Common-Source stage with Resistive load

- Same result is obtained from small-signal equivalent circuit



V1 = Vin = Vgs
gmV1 = gmVin = gmVgs

this result can be directly derived from the observation that, M1 converts an input voltage change ΔVin to a drain current change gm ΔVin, and hence an output voltage change

$$V_{out} = -g_m V_1 R_D = -g_m V_{in} R_D$$

$$A_v = -g_m R_D$$

Common-Source stage with Resistive load

- Since gm itself varies with the input signal according to $\mu_n C_{ox} \frac{W}{L}(V_{in} - V_{TH})$ the gain of the circuit changes substantially if the signal is large.
- The dependence of the gain upon the signal level leads to nonlinearity usually an undesirable effect.
- A key result here is that to minimize
  - the nonlinearity,
  - the gain equation must be a weak function of signal dependent parameters such as gm.
- For a good stability, gm should not change
- Input impedance of the circuit is very high at a low frequencies.

Common-Source stage with Resistive load

- **How do we maximize the voltage gain of a common source stage?**

$$A_v = -g_m R_D \qquad A_v = -\sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}\frac{V_{RD}}{I_D} \qquad A_v = -\sqrt{2\mu_n C_{ox}\frac{W}{L}}\frac{V_{RD}}{\sqrt{I_D}}$$

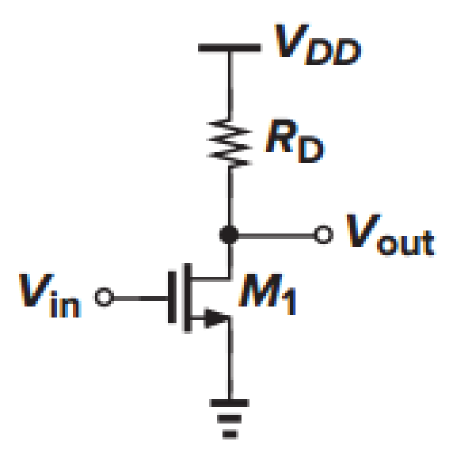
- Thus, the magnitude of Av can be increased by increasing W/L or V_{RD} or decreasing I_D if other parameters are constant.
- It is important to understand the trade-offs resulting from this equation.
- A larger device size leads to greater device capacitances, and
- A higher V_{RD} limits the maximum voltage swings
  - For example, if VDD−VRD = Vin−VTH,
  - then M1is at the edge of the triode region, allowing only very small swings at the output (and input).
- If V_{RD} remains constant and I_D is reduced, then R_D must increase, thereby leading to a greater time constant at the output node.
- In other words, as noted in the analog design octagon, the circuit exhibits trade-offs between gain, bandwidth, and voltage swings.
- Lower supply voltages further tighten these trade-offs

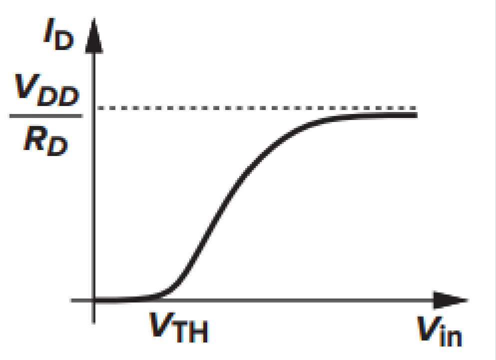
Common-Source stage with Resistive load

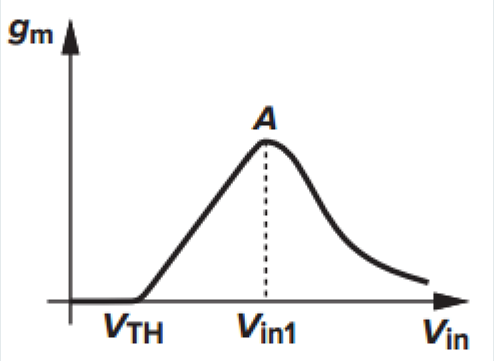
Cut-off	Saturation	Triode / Linear
Vin < Vth	Vin1>Vin > Vth	Vin>Vin1
ID = 0	$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{in} - V_{TH})^2$	$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox} \frac{W}{L}\left[2(V_{in} - V_{TH})V_{out} - V_{out}^2\right]$
	$A_v = \frac{\partial V_{out}}{\partial V_{in}}$ $= -R_D \mu_n C_{ox} \frac{W}{L}(V_{in} - V_{TH})$	$A_v = \frac{\partial V_{out}}{\partial V_{in}}$ $\frac{-\mu_n C_{ox}(W/L)R_D V_{out}}{1 + \mu_n C_{ox}(W/L)R_D(V_{in} - V_{TH} - V_{out})}$

Common-Source stage with Resistive load

P 1. Sketch the drain current and transconductance of M1in below Fig. as a function of the input voltage

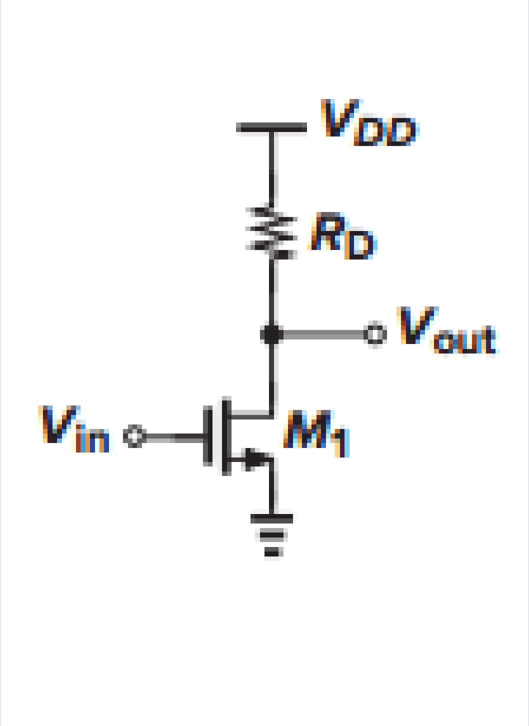


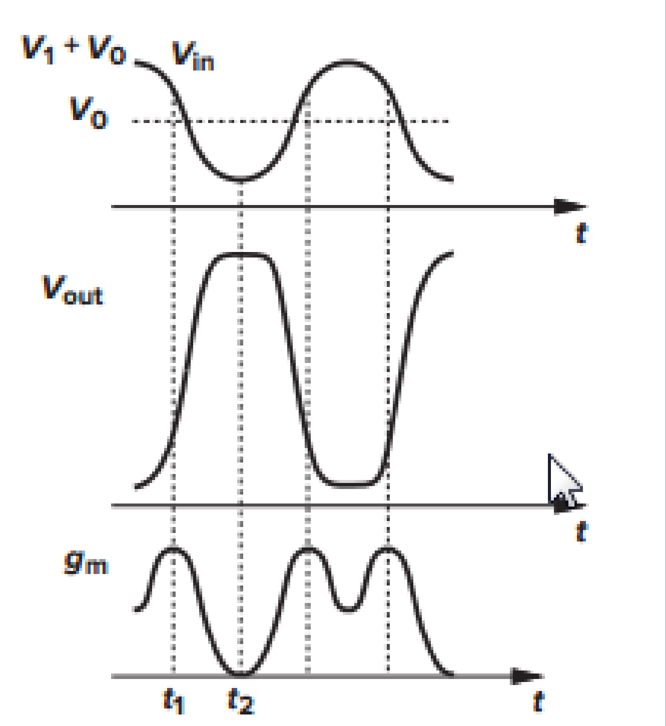




Common-Source stage with Resistive load

P 2. A CS stage is driven by a sinusoid, Vin =V1cosω1t+V0, whereV0is the bias value andV1is large enough to drive the transistor into the off and triode regions. Sketch the gm of the transistor as a function of time.





Common-Source stage with Resistive load

- For large values of R_D, the effect of channel-length modulation in M1 becomes significant

$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2(1 + \lambda V_{out})$$

$$\frac{\partial V_{out}}{\partial V_{in}} = -R_D \mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})(1 + \lambda V_{out}) \; -R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2 \lambda \frac{\partial V_{out}}{\partial V_{in}}$$

Let $(1/2)\mu_n C_{ox}(W/L)(V_{in} - V_{TH})^2\lambda = 1/r_O$

ro is output resistance

$$A_v = -R_D g_m - \frac{R_D}{r_O} A_v$$

Thus $A_v = -g_m \dfrac{r_O R_D}{r_O + R_D}$

$$A_v = -g_m \, (r_O || R_D)$$

Common-Source stage with Resistive load

- **For large values of RD, the effect of channel-length modulation in M1becomes significant**

$$V_{out} = V_{DD} - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2(1 + \lambda V_{out})$$

$$\frac{\partial V_{out}}{\partial V_{in}} = -R_D \mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})(1 + \lambda V_{out}) \; - R_D \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2 \lambda \frac{\partial V_{out}}{\partial V_{in}}$$

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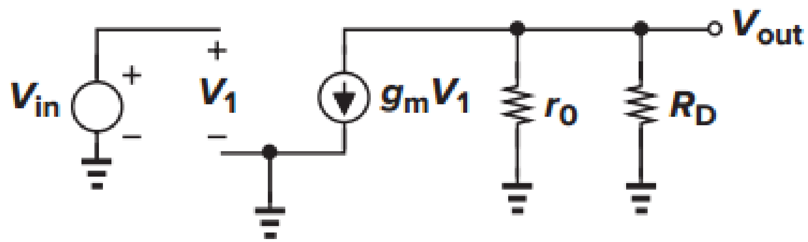
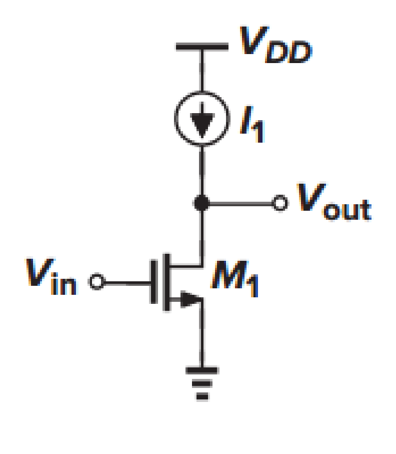


Small-signal model of CS stage including the transistor output resistance.

Common-Source stage with Resistive load

P3. Assuming thatM1in Fig. is biased in saturation, calculate the small-signal voltage gain of the circuit.



 # Since I1 introduces an infinite impedance (RD=∞),

 # the gain is limited by the output resistance of M1

$$A_v = -g_m r_O$$

Called the "intrinsic gain" of a transistor,

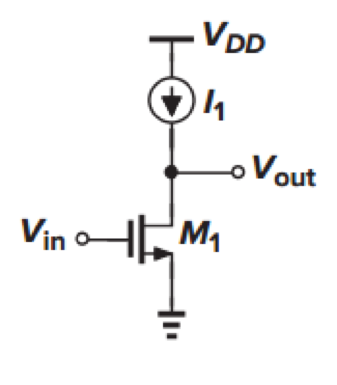
this quantity represents the maximum voltage gain

that can be achieved using a single device

- **In today's CMOS technology, gm r_O of short-channel devices is between roughly 5 and 10. We usually assume (1/gm)<< r*o***

Common-Source stage with Resistive load

P3. Assuming thatM1in Fig. is biased in saturation, calculate the small-signal voltage gain of the circuit.



By applying KCL @ Vout node

$$I_{D1} = I_1$$

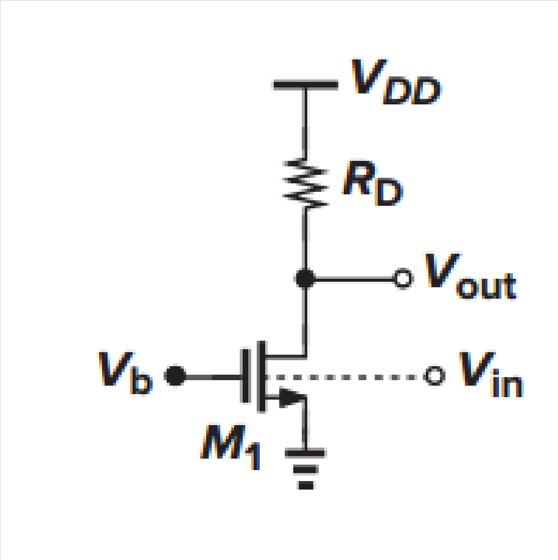
$$\begin{aligned} I_{D1} &= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{TH})^2(1 + \lambda V_{out}) \\ &= I_1 \end{aligned}$$

Vin appears in the square term and Vout in the linear term.

As Vin increases, Vout must decrease such that the product remains constant

Common-Source stage with Resistive load

P4. It is possible to use the bulk (back gate) of a MOSFET as the terminal controlling the channel. Shown in Fig. Determine the voltage gain if λ=0.



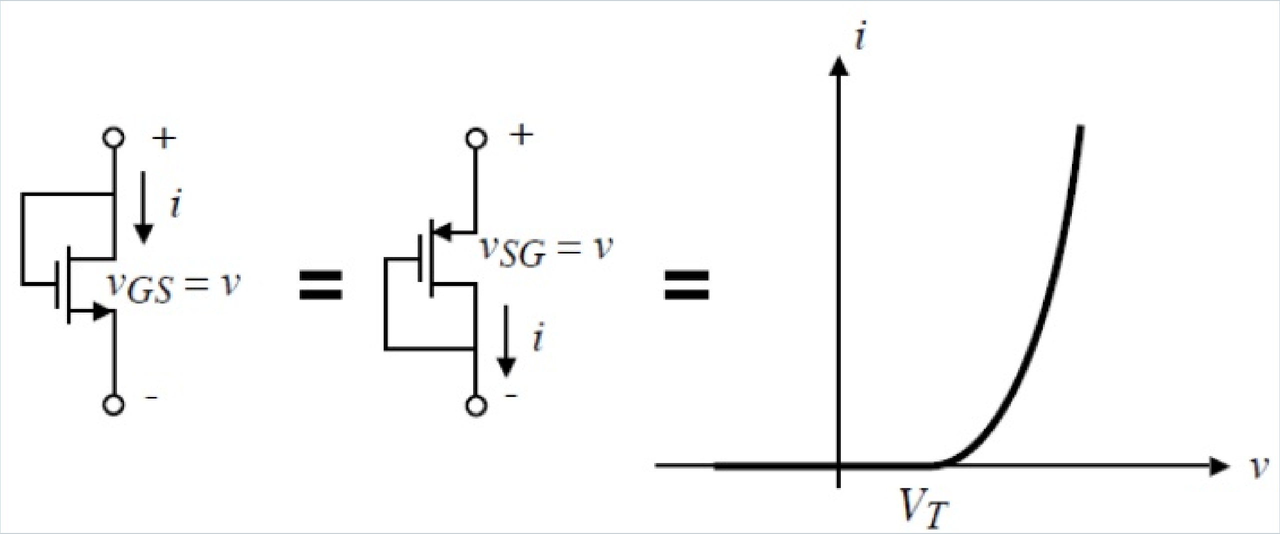
The drain current is given by $g_{mb}V_{in}$

Thus, $A_v = -g_{mb} R_D$.

Common-Source stage with Diode Connected Load

MOS as Diode

- **When a gate of MOSFET is connected to the drain, it acts like a diode with characteristics similar to a pn-junction diode.**



Common-Source stage with Diode Connected Load

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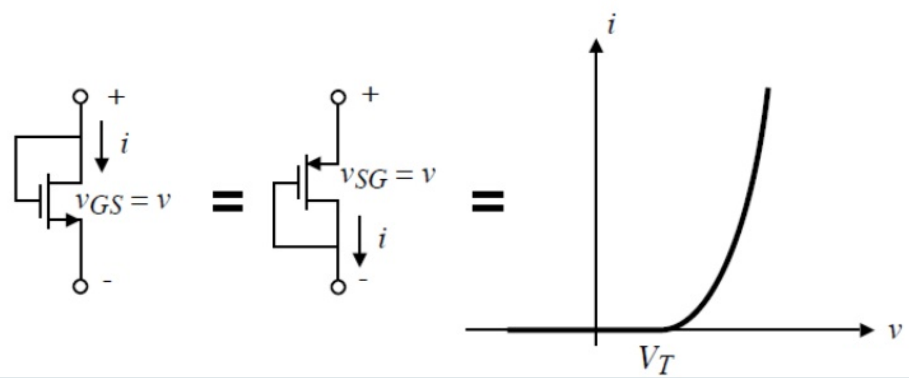
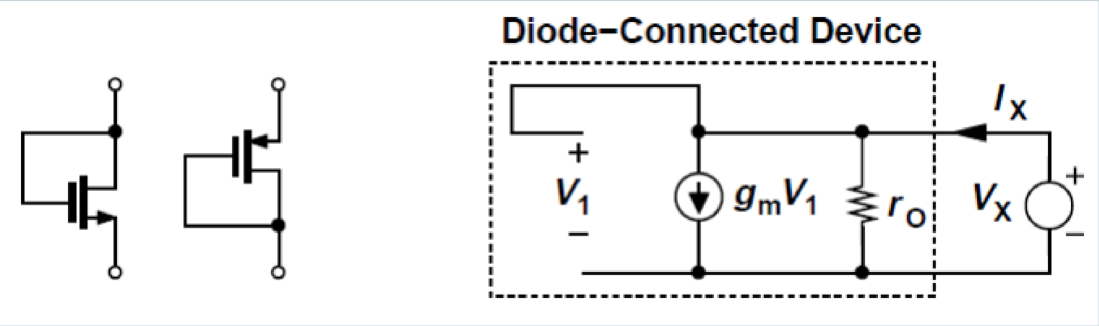


- **When the gate is connected to the drain of an enhancement MOSFET, the MOSFET is always in the saturation region.**

$$v_{DS} \geq v_{GS} - V_T$$
$$\Rightarrow \quad v_D - v_S \geq v_G - v_S - V_T$$
$$\Rightarrow \quad v_D - v_G \geq -V_T$$
$$\Rightarrow \quad v_{DG} \geq -V_T$$

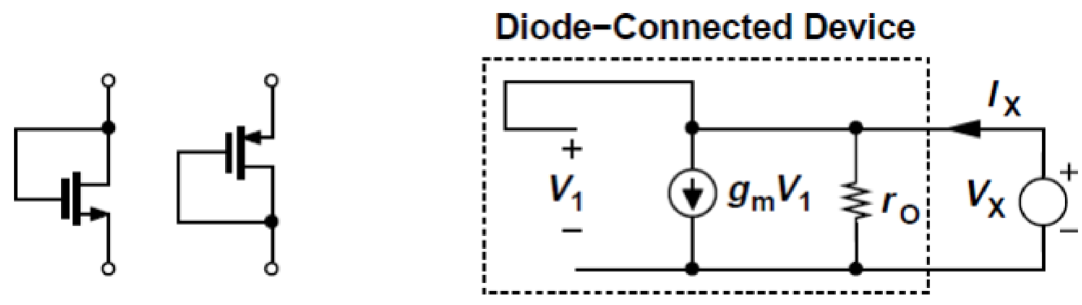
Common-Source stage with Diode Connected Load

- In many CMOS technologies, it is difficult to fabricate resistors because it requires large area on a silicon wafer.
- A MOSFET can operate as a small-signal resistor if its gate and drain are shorted as shown in fig below
- Called a "Diode connected " device in analogy with its bipolar counterpart, this configuration exhibits a small-signal behavior to a two-terminal resistor.



- Transistor always operates in saturation because the drain and the gate have the same potential.

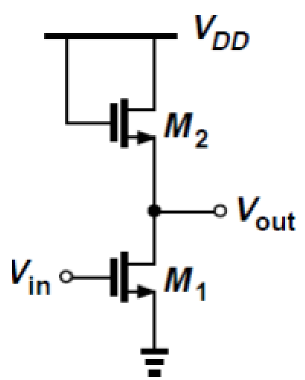
Common-Source stage with Diode Connected Load



$$V_1 = V_X \qquad I_X = V_X/r_O + g_m V_X$$

$$V_X/I_X = (1/g_m)\|r_O \approx 1/g_m$$

- **The voltage gain of CS stage with diode connected (without body effect) load is**



$$A_v = -\frac{g_{m1}}{g_{m2}} \qquad A_v = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$