GENERAL GUIDELINES

- Maintain absolute discipline and decorum inside the Campus.
- 85% attendance is a mandatory requirement.
- Mobile phones are strictly prohibited and not to be carried to college.
- Bring this Course Information Booklet to the class, daily.
- Be well on time.
- Keep the classrooms, laboratories, workshop, amenities and the surroundings always clean.
- Show due respect to all staff.
- Clarify your doubts in the respective subjects with faculty by taking prior appointment.
- Inform your parents to follow up your progress at regular intervals with the college authorities.
- Avail the facility of Suggestions box to convey your suggestions.

NOTE

- If you secure less than 60% in the ESA examination and / or in the internal test you have to go through Student Academic Support Program compulsorily
- The questions indicated in the question bank have appeared in the previous examination question papers / model papers
- T – Text Book
- R – Reference Book

STUDENT SELF APPRAISAL
SESSION: Aug – Dec 2019

Course Name	Marks		Attendance	
	Test 1	Test 2	Report 1	Report 2
Engineering Mathematics III				
Network Analysis and Synthesis				
Signals and Systems				
CMOS Analog Circuit Design				
Digital Circuit Design using HDL				
CMOS Analog Circuit Design LAB				
Digital Circuit Design LAB using HDL				

INDEX SHEET

#	Subject code	Subject	Faculty Handling
1	UE18MA201	Engineering Mathematics III	Dr.Leela V /Dr.Anitha N
2	UE18EC201	Network Analysis and Synthesis	Dr. Koshy George K/Dr. Anuradha M/ Dr. R G Kulkarni /Prof. Karpagavalli S/ Prof.Thippeswamy E
3	UE18EC202	Signals and Systems	Dr.Chandar T S/Dr. Manikandan J/Prof. Rajini M/Prof.R Swetha/Prof. Sarita U/
4	UE18EC203	CMOS Analog Circuit Design	Prof. S.S Rekha/Prof.K R Savithri/ Prof. Annapurna K.Y.
5	UE18EC204	Digital Circuit Design using HDL	Prof.Nagaraj L J/ Prof. Vanishree P/ Prof. Ravikant G. Biradar/ Prof. S Veena/
6	UE18EC205	CMOS Analog Circuit Design LAB	Prof. S.S Rekha/Prof.M S Sunitha/Dr.Chethan K S/ Prof. Annapurna K.Y./Prof.Shruthi M L J/ Prof.K R Savithri/Prof.ShwethaG/Prof.Thippeswamy/Prof.R Swetha/Prof.M G Purvidatta/Prof.Ranjan Chaudhuri/Prof.Lavanya /Prof.Hema N
7	UE18EC206	Digital Circuit Design LAB using HDL	Prof.Nagaraj L J/ Prof. Vanishree P/ Prof. Ravikant G. Biradar/ Prof. S Veena/Prof.Suganthi J, Prof.M Rajasekar/Prof.Sahana Srikanth,Prof.Melisa, Dr.Purushotham/Prof.Kedar/Prof. Sumanth/Prof.M Pavithra/Prof.Santha Meena/Prof.Rajini M/ Prof.Sudeendra K/Prof.Y J Pavithra/Prof.Bharathi / Prof.Shilpa/Prof.Nishitha/Prof.Karpagavalli/ Prof.Ashwini

UE18MA202-Engineering Mathematics-III (3-1-1-0-4)

Credits: 04 No. of Periods: 52

Class Number	Portion to be covered	Percentage covered/ Marks allotted
1	Unit-I. Complex Function Theory: Introduction to Complex Functions, Limit , Continuity and Derivative of complex functions	20% 20 marks
2-3	Cauchy-Riemann equations in Cartesian form, Analytic Functions,	
4	Cauchy-Riemann equations in Polar form.	
5	Harmonic functions &Orthogonal Trajectories with applications to flow problems	
6	Milne Thompson method	
7	Lab-1 Introduction to finite differences & Scilab.	
8	Geometrical representation of *w=f(z),*Conformal Transformation $w = z^{2.}$	
9	Conformal Mapping: $w = e^z$	
10	Conformal Mapping: $w = z+a^2/z$ ($z \neq 0$)	
11	Application problems.	
12	Lab-2. Newtons Forward and Backward Interpolation Formulae.	
13	Unit-II Complex Integration: Line integral of a complex function.	40% 20 marks
14-15	Cauchy's theorem and consequences of Cauchy theorem.	
16-17	Cauchy's integral formula & its generalization	
18	Series of complex terms-Taylor's series and Laurent's series	
19	Lab-3. Lagrange's Interpolation Formlae.	
20	Singularities and Poles	
21-22	Residues, Cauchy's residue Theorem.	
23	Lab-4. Trapezoidal Rule.	
24	Unit-III . Probability and Discrete Random Variable:Probability review, Basic Terminology.	60% 20 marks
25-26	Independent events, combined events, axioms of probability, compound law of probability, Bernoulli trials.	
27-28	Baye's Theorem and formula.	
29	Lab-5. Simpson's one third and three eighth rule.	
30	Random variable, Discrete random variable, discrete probability distribution.	
31-32	Binomial distribution.	
33	Poisson distribution.	
34	Uniform distribution.	
35	Lab-5. Modified Euler's method.	
36-37	Unit- 4. Concept (Continuous random variable) , continuous probability distribution and cumulative distribution function.	80% 20 marks

38	Gaussian random variable and distribution.	
39	Expectation, expected value of a random variable and function of a random variable, conditional expected value.	
40-41	Transformation of a random variable, conditional density and distribution function.	
42	Rayleigh random variable.	
43	Lab-5. Runge-kutta fourth order method.	
44	Unit-IV. Formation of PDEs by the method of separation of variables .	100% 20 Marks
45-46	Linear PDE's of first order- Lagrange's linear equation	
47	solution of PDE by direct method	
48-49	Solution of homogeneous linear PDE with constant co-efficients	
50-51	Non homogeneous linear PDE.	
52	Lab Test Evaluation.	

UE18EC201 NETWORK ANALYSIS AND SYNTHESIS (3-0-0-3)

Faculty: Dr. Koshy George K/Dr. Anuradha M/ Dr. R G Kulkarni /Prof. Karpagavalli S/ Prof.Thippeswamy E

Credits: 03 **No. of Periods: 42**

Class #	Chapter Title/ Reference Literature	Topics to be Covered	% Portions Covered	
			Individual	Cumulative
Basic Analysis				
1-2	**R1: Chap 1, 2, 3 R2: Chap 2, 3, 4, 5, 7**	Reference directions, conventions and notations. Passive components. Dot conventions.	19.0	19.0
3-4		Active components. Physical devices and approximations: linearity; time-invariance; lumped parameters		
5-6		Kirchhoff's laws; independent network equations. Node and mesh analysis with dc excitation. Duality.		
7		Source transformations. Star-delta transformations.		
8		More examples of network analysis with dc excitation.		
Transient Behaviour				
9-10	**R1: Chap 4, 5, 6, parts of 7, 8, 9, 10 R2: Chap 8, 9, 10, 11, 13, 14, 15**	First order circuits; time constants. Initial conditions and their evaluation.	26.0	45.0
11-12		Second order circuits; damping.		
13		Laplace transforms; properties; the Dirac delta		
14-16		s-domain analysis of first and second order circuits.		
17		Waveform synthesis		
18		Evaluation of initial and final values; Impedance, admittance and immittance functions. Network functions.		
19		More examples of network analysis with dc and ac excitations.		
Network Theorems				
20	**R1: Chap 9, 14**	Superposition theorem.	19.0	64.0

21-22	**R2: Chap 5**	Thevenin's and Norton's theorems		
23-24		Maximum power transfer and reciprocity theorems.		
25-26		Millmann's and Tellegen's theorems.		
27		More examples of network analysis with dc and ac excitations.		
Two-ports				
28	**R1: Chap 11 R2: Chap 17 R3: Chap 9**	One-ports: review	17.0	81.0
29		z-parameters: open circuit analysis		
30		y-parameters: short circuit analysis		
31		h- and t-parameters		
32		Relations between parameter sets		
33		Interconnections of two-port networks		
34		More examples		
Network Synthesis				
35	**R3: Chap 10, 11**	Causality and stability	19.0	100
36		Hurwitz polynomials; positive-real functions.		
37-38		Elementary synthesis procedures.		
39		Properties of RC impedance, RL admittance and LC immitance functions.		
40-42		Foster forms I and II; Cauer forms I and II		

Note: A maximum of 14 additional hours can be considered as tutorials which have been factored into the time-table.

Reference Books:

1. M.E Van Valkenburg, Network Analysis, Third Edition, PHI, 2006.
2. W.H. Hayt, J.E. Kemmerly, S.M. Durbin, Engineering Circuit Analysis, Seventh Edition, TMH, 2007.
3. F. F Kuo, Network Analysis and Synthesis, Second Edition, Wiley India, 2006.
4. C. K Alexander, M. N. Sadiku, Fundamentals of Electric Circuits, Third Edition, McGraw Hill, 2010.
5. R. L. Boylestad, Introductory Circuit Analysis, Tenth Edition, Prentice Hall, 2002.
6. J. O'Malley, Theory and Problems of Basic Circuit Analysis, Second Edition, McGraw Hill, 1992.

UE18EC202 - SIGNALS AND SYSTEMS

Credits: 3 **No. of Hours: 42**

Faculty : **Dr. T. S. Chandar (TSC), Dr. J. Manikandan (JMK), Mrs. Rajini M. (RMM), Mrs. R. Swetha (RS), Ms. Saritha U (SU), Ms. Lavanya K (LK), Dr. Sanjoy Mondal, Prof. Shreyus**

LESSON PLAN

Class #	Chapter Title / Reference Literature	Topics to be covered	% of Portion covered	
			Reference Unit	*Cumulative*
1-8 (8 hrs)	**UNIT-1 Signals and Systems (R1 – Sec. 1.1 – 1.6)**	Classification of signals, Continuous-time and discrete-time signals, Transformations of the independent variable, Exponential and sinusoidal signals, The unit impulse and unit step functions, Sa (x) / Sinc functions, Importance of Sinc function, Continuous-time and discrete-time systems, Basic system properties.	**19%**	**19%**
9-16 (8 hrs)	**UNIT-II LTI Systems (R1 – Sec. 2.1 – 2.4)**	Discrete-time LTI systems: The convolution sum, Continuous-time LTI systems: The convolution integral, Properties of LTI systems, Causal LTI systems described by difference and differential equations (Natural, Forced, and Complete Response).	**19%**	**38%**
17-24 (8 hrs)	**UNIT-III Representation of Periodic (Continuous-time & Discrete-time) signals using Fourier series. (R1 – Sec. 3.1 – 3.7)**	Explanation of Complex Exponentials, Response of LTI systems to complex exponentials, Trigonometric Fourier Series, Fourier series representation of continuous-time periodic signals, Convergence of the Fourier series (brief discussion only), Properties of continuous-time Fourier series (CTFS), Introduction to Fourier series representation of discrete-	**19%**	**57%**

		time periodic signals, Properties of Discrete-time Fourier Series (DTFS).		
25-34 (10 hrs)	**UNIT-IV** **Continuous-time / Discret-time Fourier Transform.** **(R1 – Sec. 4.1 – 4.5, 5.1 – 5.3)**	Representation of aperiodic signals: **Continuous-time Fourier transform (CTFT)**, The Fourier transform for periodic signals, Properties of continuous-time Fourier transform, Fourier transform pairs. **Discrete-time Fourier transform:** Representation of aperiodic signals: the discrete-time Fourier transform (DTFT), The Fourier transform for discrete periodic signals, Properties of discrete-time Fourier transform, Fourier transform pairs, Duality. Introduction to Sampling : Sampling theorem, Nyquist Criterion.	**23%**	**80%**
35-42 (8 hrs)	**UNIT-V** **Z-Transforms** **(R1 – 10.1 – 10.3, 10.5 – 10.7, 10.9)**	The Z-transform, The region of convergence (ROC) for the Z-transform, The inverse Z-transform, Properties of the Z-transform, Z-transform pairs, Analysis and characterization of LTI systems using Z-transforms. The unilateral Z-transform and solution of difference equations.	**20%**	**100%**

Note: A total of 14 hours need to be earmarked over above the allotted 42 hours, for Tutorials. The same needs to be distributed evenly across the 5 Units.

References:

Book Type	Code	Title & Author	Publication Info		
			Edition	**Publisher**	**Year**
Text Book - 1	R1	Signals and Systems by Alan V Oppenheim, Alan S. Willsky	2nd	Pearson Education Asia	2013
Reference Book - 1	R2	Signals & Systems Simon Haykin & Barry Van Veen	2nd	John Wiley & Sons	2002
Reference Book - 2	R3	Signals Processing and Linear Systems. B.P. Lathi	1st	Ind Press	2006
Reference Book - 3	R4	"Analog and Digital Signal Processing"Ashok Ambardar	2nd	--	1999

ISA Evaluation Pattern:

ISA – 1 – weightage 15 Marks
ISA – 2 – weightage 15 Marks
Assignment – 10 Marks

Total – 40 Marks

UE18EC203 CMOS ANALOG CIRCUIT DESIGN (4-0-0-4)

Faculty: Dr.ST, Prof.MAS, Prof.SSR, Prof.KRS ,Prof. AKY

Credits: 04 No. of Classes: 56

Class #	Chapter Title/ Reference Literature	Topics to be Covered	% Portions Covered	
			Individual	Cumulative
PHYSICS OF MOS TRANSISTORS				
1-2	**R1: Chapter 6**	Introduction to Analog Design, **Structure of MOSFET**	19%	19%
3-7		**Operation of MOSFET**: Qualitative Analysis, Derivation of I-V Characteristics , **Channel-Length** Modulation, MOS Traconductance, Body effect		
8-10		**MOS device Models**: Large Signal Model, Small Signal Model,		
11		**PMOS transistor,** **CMOS technology**		
SINGLE STAGE AMPLIFIER				
12-17	**R2: Chapter 3**	**Basic Concepts**, **Common Source stage**: 1. Resistive Load: Av 2. Diode Connected Load: Av 3. Source Degeneration: Av, Rout (Till Page 64)	21%	40%
18-19		**Source follower:** Av and Rout (Till Page 71)		
20-21		**Common gate stage**: Av (Till Page 77)		

22-23		**Cascode stage:** Input & Output Characteristics, Small Signal and Rout (Till Page 85)		
DIFFERENTIAL AMPLIFIER				
24	**R2: Chapter 4**	**Single Ended and Differential operation**	18%	58%
25-29		**Basic differential pair:** **1.** Qualitative Analysis(Till Page 106) **2.** Small Signal behaviour of differential pairs-Half Circuit Analysis only		
30-32		**Common Mode response:** Av,cm (Till Page 119)		
33		Differential Pair with MOS loads		
PASSIVE AND ACTIVE CURRENT MIRRORS				
34-35	**R2: Chapter 5**	**Basic current mirror**	20%	78%
36-37		**Cascode current mirrors** (Till Page 142)		
38-40		**Active Current Mirror**: Av of Differential Pair with Current Source Load (Till Page 147)		
41-42		**Large signal analysis of active current mirror**		
43-44		**Small signal analysis of active current mirror:** Av with First Approach only (Till page 152)		
FREQUENCY RESPONSE				
45	**R2: Chapter 6** **Chapter 8**	**Miller Effect,**	22%	100%
46-47		**Common source stage**		

48-50		**Feedback** **General Consideration Properties of negative feedback** (Till Page 255)		
51-54		**Feedback Topologies-** Different Types of Feedback Topologies with effect of feedback on input and output impedance		
55-56		**Effect of Loading** 1. Two Port Network Model 2. Loading in Voltage –Voltage feedback		

DIGITAL DESIGN USING HDL

Subject Code: UE18EC204 **No of Hours: 56**

LESSON PLAN

Class #	Chapter Title	Topics to be covered	% of Portions covered	
			Reference Chapter	Cumulative
1-16	**Unit-1** **Gate-level minimization and Introduction to Verilog HDL**	Introduction to Boolean Functions, K Map-Method: 2-Variable, 3-Variable, 4-Variable, Five Variable map, POS Simplification, Don't Care Conditions, NAND NOR Implementation, Other Two Level Implementations, Quine-McCluskey Minimization Methods; HDL Flow, Module Declaration, Gate Delays, Boolean Expression Assignment, User Defined Primitives	**28%**	**28%**
17-29	**Unit-2** **Combinational Logic Circuit**	Design Procedure, Binary Adder-Subtractor, Decimal Adder, Binary Multiplier, Magnitude Comparator, Decoders and Encoders, Multiplexers and Demultiplexers; Verilog Models of CLC: Gate Level Modeling, Three State Gates, Data Flow modeling, Behavioral Modeling, Test Bench	**23%**	**51%**

Class #	Chapter Title	Topics to be covered	% of Portions covered	
			Reference Chapter	Cumulative
1-16	**Unit-1** **Gate-level minimization and Introduction to Verilog HDL**	Introduction to Boolean Functions, K Map-Method: 2-Variable, 3-Variable, 4-Variable, Five Variable map, POS Simplification, Don't Care Conditions, NAND NOR Implementation, Other Two Level Implementations, Quine-McCluskey Minimization Methods; HDL Flow, Module Declaration, Gate Delays, Boolean Expression Assignment, User Defined Primitives	**28%**	**28%**
30-40	**Unit-3** **Sequential Logic Circuits**	Introduction to Sequential Circuits, Storage Elements-Latches, Storage Elements- Flip-Flop, Analysis of Clocked Sequential Circuits; Verilog Models of SLC: Verilog Models of Flipflops and Latches, State Diagram Based HDL Models, Structural Description of Clocked Sequential Circuits	**20%**	**71%**
41-49	**Unit-4** **Registers and Counters**	Registers, Shift Registers, Ripple Counters, Synchronous Counters, Ring and Johnson Counters; Verilog Models of Registers and Counters: Shift Register, Synchronous counters, Ripple Counter	**16%**	**87%**

Class #	Chapter Title	Topics to be covered	% of Portions covered	
			Reference Chapter	Cumulative
1-16	**Unit-1** **Gate-level minimization and Introduction to Verilog HDL**	Introduction to Boolean Functions, K Map-Method: 2-Variable, 3-Variable, 4-Variable, Five Variable map, POS Simplification, Don't Care Conditions, NAND NOR Implementation, Other Two Level Implementations, Quine-McCluskey Minimization Methods; HDL Flow, Module Declaration, Gate Delays, Boolean Expression Assignment, User Defined Primitives	**28%**	**28%**
50-56	**Unit-5** **Memories and Programmable Logic**	Random Access Memory, Memory Decoding, Error Detection and Correction, Read Only Memory, PLA, PAL, Sequential Programmable Device	**13%**	**100%**

Literature:

Book Type	Title & Author	Publication Info		
		Edition	Publisher	Year
Reference Book	M. Morris Mano Michael D. Ciletti, "Digital Design with an Introduction to the Verilog HDL"	5th Edition	Pearson	2013
Reference Book	Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design",	2nd Edition	McGraw Hil	2003
Reference Book	Ronalad J Tocci, Neal S Widmer, Gregory L Moss, "Digital Systems Principles and Applications",	10th Edition	Prentice Hall	2006
Reference Book	J. Bhasker, "Verilog HDL Synthesis A Practical Primer",	------	BSP	2001
Reference Book	Joseph Cavanagh, "Verilog HDL: Digital Design and Modeling" ,	----	CRC press	2007
Reference Book	Michael D Ciletti, "Advanced digital design with Verilog HDL",,,.	2nd Edition	Pearson	2003

Evaluation criterion:

ISA-I : 20 M
ISA-II: 20 M
ESA: 60 M