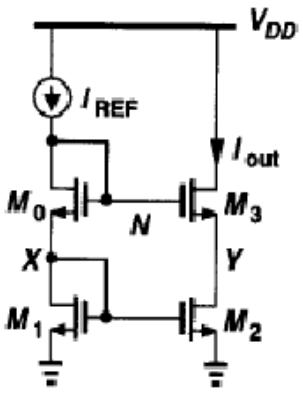
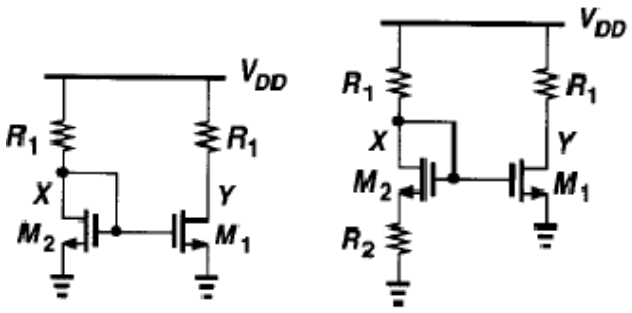
Assignment-2 (CMOS Analog Circuit Design)

Q1.	Suppose the total capacitance between adjacent lines in Fig. 4.2 is 10 fF and the capacitance from the drains of M_1 and M_2 to ground is 100 fF. (a) What is the amplitude of the glitches in the analog output in Fig. 4.2(a) for a clock swing of 3 V? (b) If in Fig. 4.2(b), the capacitance between L_1 and L_2 is 10% less than that between L_1 and L_3, what is the amplitude of the glitches in the differential analog output for a clock swing of 3 V?
Q2.	In the circuit of Fig. 4.10, $(W/L)_{1,2} = 50/0.5$ and $I_{SS} = 0.5$ mA. (a) What is the maximum allowable output voltage swing if $V_{in,CM} = 1.2$ V? (b) What is the voltage gain under this condition?
Q3	A differential pair uses input NMOS devices with $W/L = 50/0.5$ and a tail current of 1 mA. (a) What is the equilibrium overdrive voltage of each transistor? (b) How is the tail current shared between the two sides if $V_{in1} - V_{in2} = 50$ mA? (c) What is the equivalent G_m under this condition?
Q4	For the differential pairs of Fig. 4.32(a) calculate the differential voltage gain if $I_{SS} = 1$ mA, $(W/L)_{1,2} = 50/0.5$, and $(W/L)_{3,4} = 50/1$. What is the minimum allowable input CM level if I_{SS} requires at least 0.4 V across it? Using this value for $V_{in,CM}$, calculate the maximum output voltage swing
Q5	In the circuit shown below, sketch V_X and V_Y as a function of I_{REF}. If I_{REF} requires 0.5 V to operate as a current source, what is its maximum value?

Q6.	In Fig. 5.2, assume $(W/L)_1 = 50/0.5$, $\lambda = 0$, $I_{out} = 0.5$ mA, and M_1 is saturated. **(a)** Determine R_2/R_1. **(b)** Calculate the sensitivity of I_{out} to V_{DD}, defined as $\partial I_{out}/\partial V_{DD}$ and normalized to I_{out}. **(c)** How much does I_{out} change if V_{TH} changes by 50 mV?
Q7.	Consider the circuit of Fig. 5.9(a), assuming $(W/L)_{1-3} = 40/0.5$, $I_{REF} = 0.3$ mA, and $\gamma = 0$. **(a)** Determine V_b such that $V_X = V_Y$. **(b)** If V_b deviates from the value calculated in part (a) by 100 mV, what is the mismatch between I_{out} and I_{REF}? **(c)** If the circuit fed by the cascode current source changes V_P by 1 V, how much does V_Y change?
Q8.	Consider the circuit of Fig. 5.22(a) with $(W/L)_{1-5} = 50/0.5$ and $I_{D5} = 0.5$ mA. **(a)** Calculate the deviation of V_{out} from V_F if $\lvert V_{TH3}\rvert$ is 1 mV less than $\lvert V_{TH4}\rvert$.
Q9.	Sketch V_X and V_Y as a function of V_{DD} for each circuit Assume the transistors in each circuit are identical.

	
Q10.	Derive an expression for small signal voltage gain of active current mirror assuming ideal tail current source.

Note : Please refer Text Book (Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill Edition, 2002)for the Figure Numbers indicated in the Questions.