

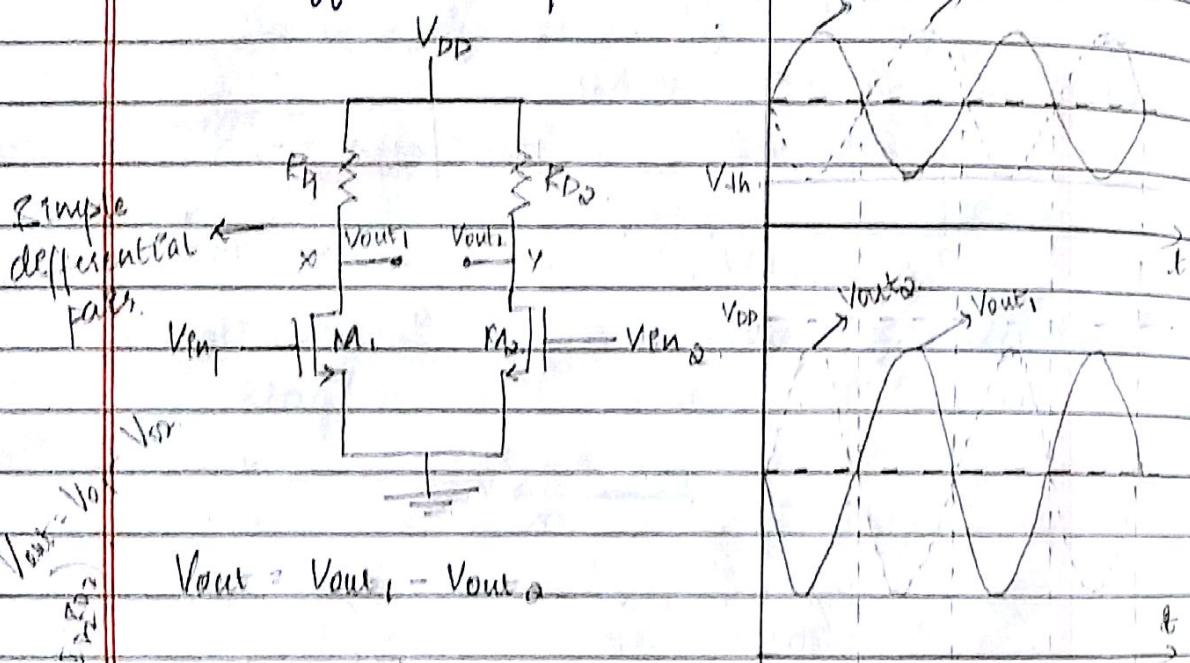
UNIT 3: DIFFERENTIAL AMPLIFIERS

Single-ended \rightarrow Unbalanced

Differential \rightarrow Balanced \rightarrow Has pqr.

[Power Supply Rejection Ratio]

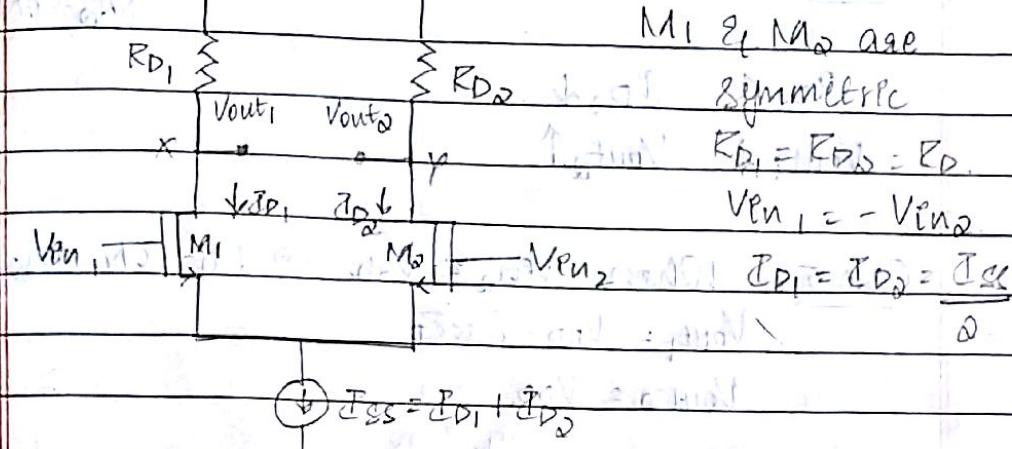
Basic differential para:



When there is a change in V_{ctrl} or level, then the threshold voltage affects the input waveform. Due to this the off waveform is clipped off.

In order to overcome this, make θ a weak function of V_{can} level, a current source $I_{SC} = I_{D1} + I_{D2}$ is introduced near the source terminal.

The higher peak should be less than edge of saturation and the lower peak should be greater than equal to Km.

V_{DD} 

Basic differential pair.

When $V_{in_1} = V_{in_2}$, $V_{out_{\text{differential}}} = V_{DD} - \frac{I_{SS} \cdot R_D}{2}$

Qualitative Analysis of Differential pair.

① Differential mode behaviour:-

Let us assume that $(V_{in_1} - V_{in_2})$ will vary from $-\infty$ to ∞ .

Case 1: If V_{in_1} is more negative than V_{in_2} , then $M_1 \rightarrow \text{OFF}$. $\Rightarrow V_{out_1} = V_{DD}$.

$$M_2 \rightarrow \text{ON} \Rightarrow V_{out_2} = V_{DD} - I_{D_2} R_D.$$

$$\text{Case 2: } V_{in_1} < V_{DD}; V_{in_1} < V_{in_2}; I_{D_2} = I_{SS}$$

$$V_{out_2} = V_{DD} - I_{SS} R_D.$$

Case 3: When V_{in_1} is brought closer to V_{in_2} .

$$[V_{in_1} < V_{in_2} \text{ and } V_{in_1} \geq V_{th}]$$

$$M_1 \rightarrow \text{ON}, M_2 \rightarrow \text{ON}, I_{SS} = I_{D_1} + I_{D_2}$$

$$V_{out_1} \downarrow \quad V_{out_2} \uparrow$$

Case 4: When $V_{in_1} = V_{in_2}$, $M_1 \rightarrow \text{ON}, M_2 \rightarrow \text{ON}$

$$I_{D_1} = I_{D_2} \quad V_{out_1} = V_{out_2} = V_{DD} - I_{SS} \times R_D$$

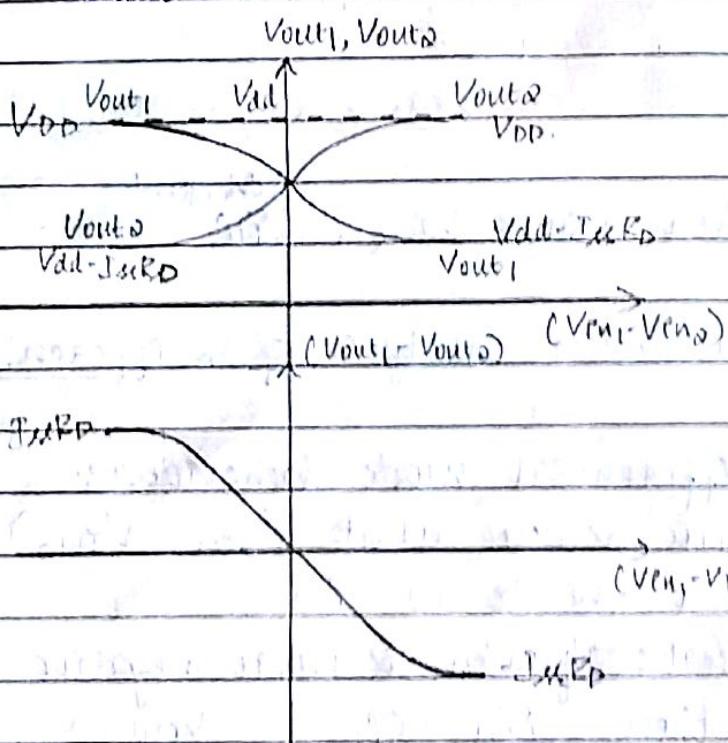
Case 4: When $V_{in_1} > V_{in_2}$ then $M_1 \rightarrow ON$
 $M_2 \rightarrow ON$.

$I_{D1} \uparrow I_{D2} \downarrow$
 $V_{out_1} \downarrow V_{out_2} \uparrow$

Case 5: When $V_{in_2} < V_{in_1} \Rightarrow M_1 \rightarrow ON$ $M_2 \rightarrow OFF$

$$V_{out_1} = V_{DD} - I_{S2} R_D$$

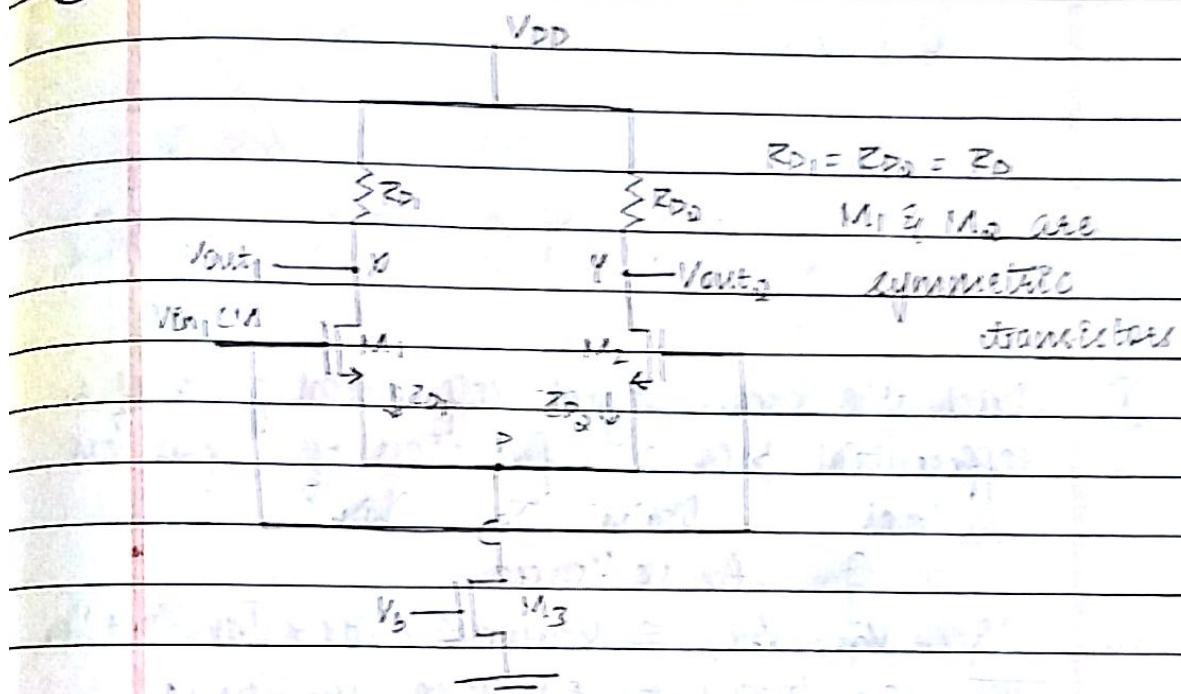
$$V_{out_2} = V_{DD}$$



Max voltage $\rightarrow V_{DD}$ Min voltage $\rightarrow V_{DD} - I_{S2} R_D$
 Whenever $V_{in_1} = V_{in_2}$ then gain is more
 in that region.

Gain is maximum when both the inputs are equal.

② Common Mode Behaviour:



$$V_{INCM} = 0 \quad M_1, M_2 \rightarrow OFF \quad V_p = 0 \quad I_{DS} = 0$$

$V_{OUT1} = V_{OUT2} = 0 \quad M_3 \rightarrow$ Deep triode region

If V_{INCM} is slightly greater than V_{TH} ,
 $M_1, M_2 \rightarrow$ Saturation.
 $M_3 \rightarrow$ Triode

For all 3 transistors to be in saturation,

$$V_p > V_{GS3} - V_{TH3}$$

$$V_p + V_{GS1} = V_{INCM}$$

$$V_p = V_{INCM} - V_{GS1}$$

$$V_{INCM} - V_{GS1} > V_{GS3} - V_{TH3}$$

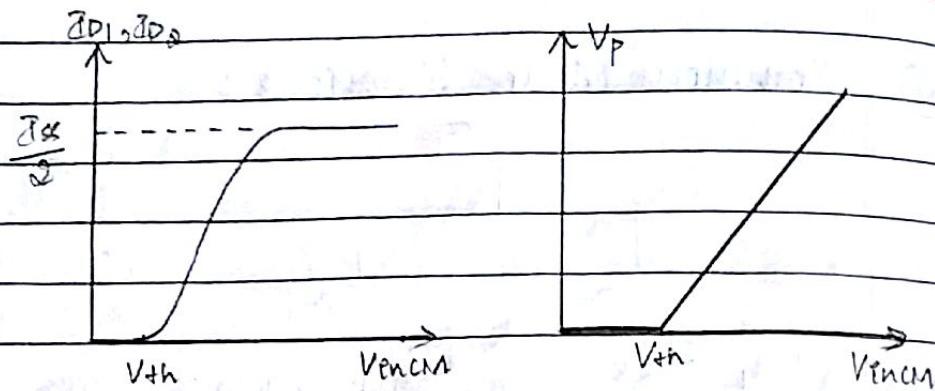
$$V_{INCM} > V_{GS3} - V_{TH3} + V_{GS1} \rightarrow \text{Min } V_{INCM}$$

$$V_{DS} > V_{GS} - V_{TH}$$

$$V_{DD} - \frac{I_{DS}}{\Omega} R_D > V_{IN} - V_{TH}$$

$$V_{IN} < V_{OUT} - \frac{I_{DS} R_D}{\Omega} + V_{TH}$$

$$V_{GS3} + V_{GS1} - V_{TH3} > V_{INCM} > V_{OUT} - \frac{I_{DS} R_D}{\Omega} + V_{TH}$$



- ① Sketch the small signal differential gain of a differential pair as a function of input CM level.

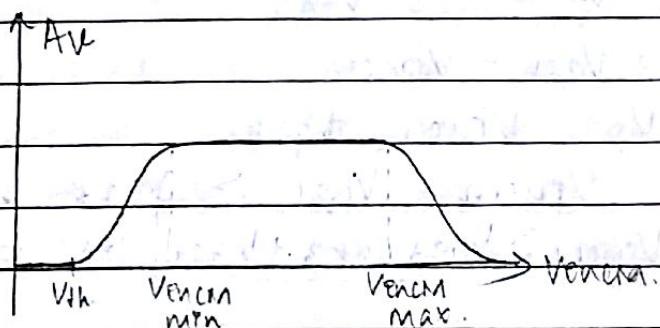
$\text{From } Av \propto V_{inCM}$

$$V_{gs1} + V_{gs3} - V_{th3} \leq V_{inCM} \leq V_{dd} - P_{ssy, RD} + V_{th}$$

The gain begins to increase as V_{inCM} exceeds threshold voltage.

After the tail current source enters saturation the gain remains relatively constant.

Finally if V_{inCM} is greater than $V_{max}(cm)$ the input transistors M_1 & M_2 enter diode region, hence gain falls.



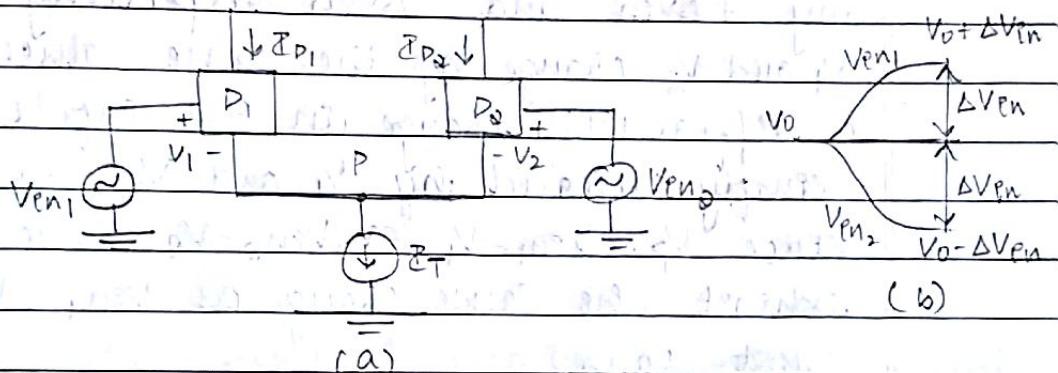
- ② How large can the op voltage swings in the differential pair.

$$\text{Maximum voltage} = V_{dd}$$

$$\text{Minimum voltage} = V_{inCM} - V_{th}.$$

Differential mode gain using small-signal analysis:

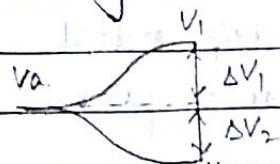
Method II: Half circuit method.



Lemma: Consider the symmetric circuit as shown in figure (a) where P_1 & P_2 represent any 3-terminal active device. Suppose V_{EN_1} changes from V_0 to $V_0 + \Delta V_{EN}$ and V_{EN_2} changes from V_0 to $V_0 - \Delta V_{EN}$ as shown in figure (b) then, if the circuit remains linear (all 3 transistors are in saturation) then V_P is constant.

Proof:

Assume that V_1 & V_2 have an equilibrium value of V_A and change by ΔV_1 & ΔV_2 respectively as shown in figure (c).



The output current therefore changes by $g_m \Delta V_1 + g_m \Delta V_2$. $g_m \Delta V_1 + g_m \Delta V_2 = 0$

$$\Delta V_1 = -\Delta V_2$$

$$V_{EN_1} - V_1 = V_{P12} - V_2$$

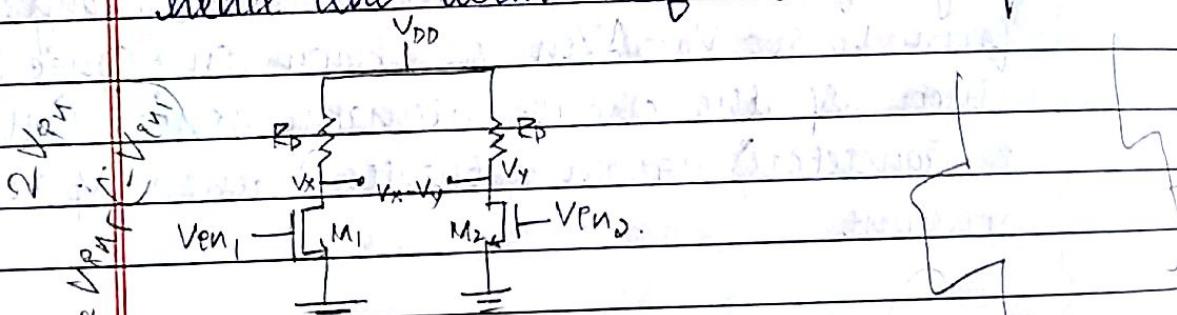
$$V_o + \Delta V_{en} - (V_a + \Delta V_1) = V_o - \Delta V_{en} - (V_a - \Delta V_2)$$

$$\Delta V_{en} - \Delta V_1 = -\Delta V_{en} + \Delta V_2$$

$$\Delta \Delta V_{en} = \Delta \Delta V_1 - \Delta \Delta V_2$$

In other words if V_{en1} and V_{en2} change by $+\Delta V_{en}$ and $-\Delta V_{en}$ respectively then V_1 and V_2 change by the same values i.e. a differential change in the inputs is simply observed by V_1 and V_2 , in fact since $V_p = V_{en1} - V_1$ or $V_{en2} - V_2$ hence V_p exhibits the same change as V_{en1} , V_p does not change.

Since V_p experiences no changes, node P can be considered as AC ground & circuit can be decomposed into 2 separate halves and hence the term half circuit concept.



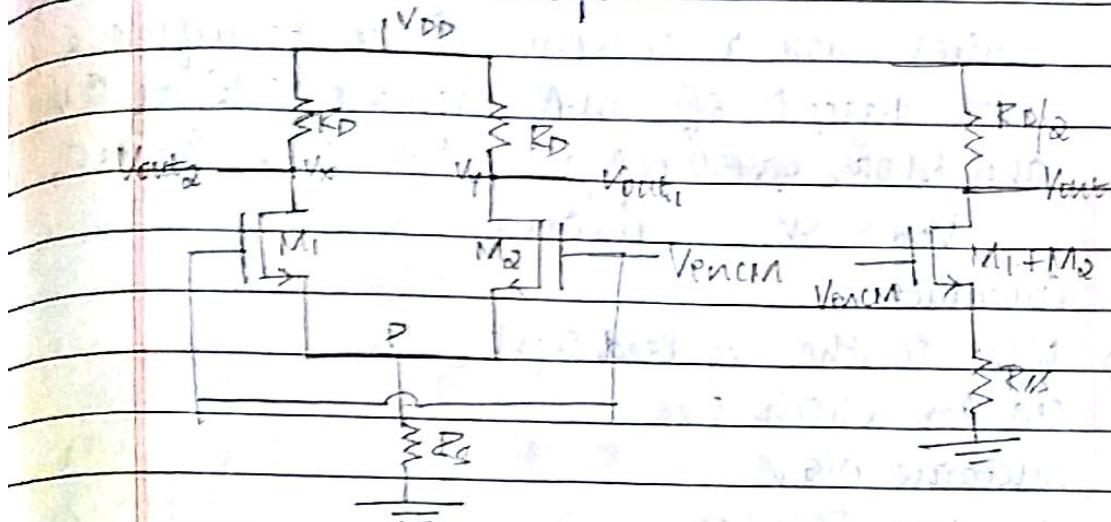
$$\frac{V_x}{V_{en1}} = -g_m R_D \quad \frac{V_y}{V_{en2}} = -g_m R_D$$

$$V_x - V_y = -g_m R_D V_{en1} - g_m R_D V_{en2} \quad V_{en} = V_{en1}$$

$$V_x - V_y = -2 g_m R_D V_{en}$$

$$\frac{V_x - V_y}{2 V_{en}} = -g_m R_D \rightarrow \text{differential mode gain.}$$

Common mode response:



Assume now the circuit is symmetric but the current source at finite output impedance R_{os} .

As V_{os} changes, so does V_D thereby increasing the drain currents of M_1 & M_2 and lowering the V_x and V_y .

Because of the symmetry V_x remains equal to V_y and it is depicted as shown in the figure. The nodes V_x and V_y can be shorted as shown in the figure.

Since M_1 and M_2 are now connected in parallel (they shall all their respective terminals) the circuit can be reduced to as shown in figure.

The compound device $M_1 + M_2$ has twice the width and the biasing current of each of M_1 and M_2 therefore twice their transconductance.

The common-mode gain of the circuit is given by, $A_V = \frac{V_{out}}{V_{os}} = \frac{R_D/2}{\frac{1}{g_m} + R_{os}}$

$V_{AS} = V_{IN} \cdot \frac{R_D}{R_S}$
 $V_{AS} = V_{IN} \cdot \frac{I_D}{I_{AS}}$

- Q) The circuit shown in figure uses a resistor rather than a current source to define a tail current of $I_{m,A}$. Assume (W/L) of M_{AS} and $M_{D/A}$ as $\mu A/V^2$. $V_{DH} = 0.6 V$, $\lambda = 0.2$,

$$V_{DD} = 5V \quad \text{pinCon} \quad V_{DD}$$

Calculate :-

- i) What is the required input CM for which R_{SS} sustains $0.5 V$

- ii) Calculate R_D for differential gain of 5.

- iii) What happens at the output of the input CM level as $50 mV$ higher than the value calculated in i).

Sol. i) $I_{D1} = I_{D2} = I_{AS}/2 = 0.5 mA$.

$$I_D = \frac{1}{2} \mu n C_o v \left(\frac{W}{L} \right) (V_{GS} - V_{TH})^2$$

$$(V_{GS} - V_{TH})^2 = \frac{2 I_D}{\mu n C_o \left(\frac{W}{L} \right)}$$

$$(V_{GS} - V_{TH})^2 = 0.4$$

$$V_{GS} - V_{TH} = 0.623 V$$

$$V_{GS} = 0.623 + 0.6 \quad V_{IN} = V_P$$

$$V_{GS} = 1.23 V$$

$$V_{IN,CM} = V_{GS} + I_P$$

$$V_{IN,CM} = 1.23 + 0.5 = 1.73 V$$

$$R_{SS} = \frac{V_P}{I_{AS}} = \frac{0.5 V}{1 m} = 500 \Omega$$

ii) $G_{in} = -g_m R_D$

$$g_m = \sqrt{\mu n C_o \left(\frac{W}{L} \right) I_D}$$

$$V_{ds} = V_d \cdot V_o$$

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$$10^{-9} \times 200 \times 10^{-9} = V_{in}$$

$$10^{-5} \times 10^{-6}$$

$$g_m = \sqrt{2 \times 50 \times 10^6 \times 0.05 \times 10^{-3} \times 0.5}$$

$$g_m^2 = 10^{-5} \text{ A/V}$$

$$R_D = \frac{V_o}{I_D} = 10^5 \times 0.32 = 3.16 \times 10^5 \Omega$$

$$g_m = \frac{V_o}{I_D} =$$

iii)	Vout	$V_{gs} - V_{th}$	
	1.42	1.23 - 0.6	$= 1.17 \text{ V}$
	1.42	0.7	290mV away from threshold region.

$$\text{Output static level} = V_{dd} - I_d R_d = 1.42 \text{ V}$$

Since $V_{envelope} = 1.73 \text{ V}$ and $V_{th} = 0.6 \text{ V}$, the transistors are now 290mV away from the threshold region. If the $V_{envelope}$ is increased by 50mV

$$A_v = \frac{\Delta V_o}{\Delta V_{en}} = \frac{R_D / 2}{Y_{Ogm} + R_{es}}$$

$$\frac{\Delta V_o}{\Delta V_{en}} = \frac{R_D / 2}{Y_{Ogm} + R_{es}}$$

$$\Delta V_o = (50 \times 10^{-3}) \times \frac{1980}{316 + 500}$$

$$\Delta V_o = 50 \times 10^{-3} \times 1.936$$

$$\Delta V_o = 96.81 \text{ mV}$$

$$V_{out} = 1.42 - 97 \text{ mV}$$

- (1) It is required to design common source amplifier with resistive load for following specification: Gain = -5, Power $\leq 1\text{mW}$
 Bandwidth = $f_{-3\text{dB}} = 100\text{MHz}$; $C_L = 1\text{pF}$ at 0°^{ideal capacitor condition},
 output swing $\geq 400\text{mV}$. Also calculate the maximum input swing [p-p] which can be tolerated by the circuit without getting into non-linear distortion.

$$GBW = \frac{g_m}{2\pi C_L} = \text{Calculate } R_D \text{ using } g_m$$

$P = I^2 R_D - \text{calc } Z$

Calculate $\mu_{n\text{Cox}}$ using I_d V_{gs} graph

$$g_m = \sqrt{2D\mu_{n\text{Cox}}(\omega/L)}, \quad (\omega/L)_1 = 0/1$$

$$g_m = \sqrt{2D\mu_{n\text{Cox}}(\omega/L)}, \quad (\omega/L)_2 = 0(\omega/L),$$

$\mu_{n\text{Cox}}$ should be approx same.

- (2) It is required to design common source amplifier with following specification:

Gain = -3, Power $\leq 0.8\text{mW}$, $f_{-3\text{dB}} = 100\text{MHz}$,
 $C_L = 1.5\text{pF}$, Output swing $\geq 500\text{mV}$. Also calculate max p-p swing which can be tolerated by the circuit without getting into non-linear distortion.

$$\mu_{n\text{Cox}} = 30 \times 10^{-10}$$

$$g_m = 3.1415 \times 10^{-3}$$

$$g_m = \sqrt{2D\mu_{n\text{Cox}}(\omega/L)}$$

$$(3.1415 \times 10^{-3})^2$$

$$2 \times 0.79 \times 10^{-3} \times 30 \times 10^{-6}$$

89.23

Differential pair with pMOS diode-connected load:

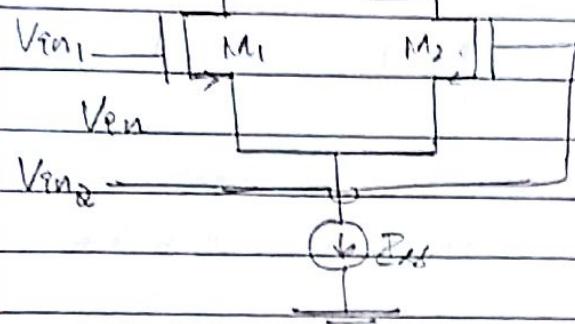
In pMOS decade the

body effect will be zero.

The body terminal & source are connected to VDD

Hence no body effect.

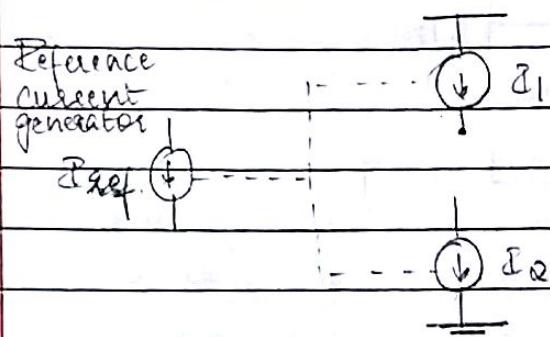
So p-n-p diode is used.



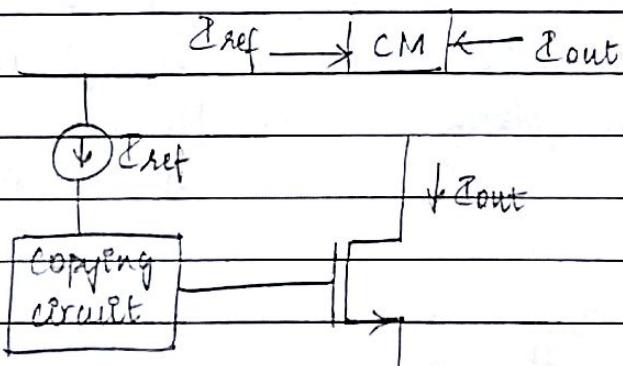
UNIT 4 : PASSIVE AND ACTIVE CURRENT

RODRIKE MIRRORE

The motivation behind the current mirror is to scale the current from the golden current source and duplicate this golden current to other locations.

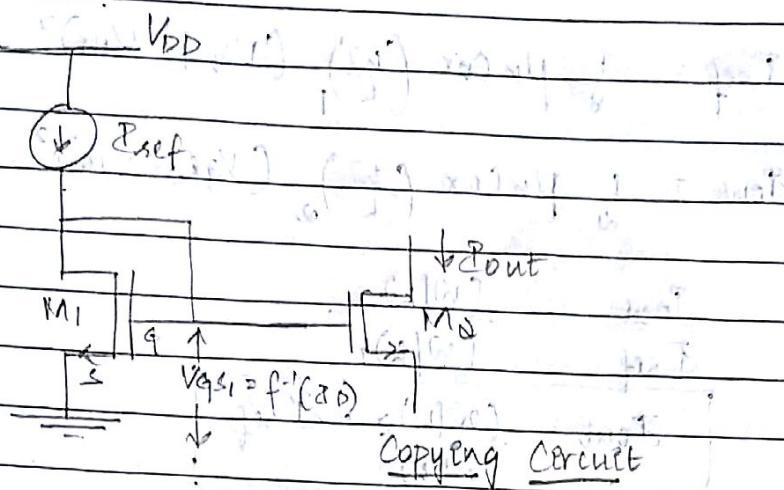


From this figure, a relatively complex circuit sometimes requiring external adjustment is used to generate a stable reference current I_{ref} which is then copied to many current sources in the system.



Conceptual means of
copying circuits

Basic current mirror



For the mosfet, $I_D = f(V_{GS})$

$$V_{GS} = f^{-1}(I_D)$$

If a transistor is biased at V_{ref} , then it produces $V_{GS2} = f^{-1}(I_D)$ as shown in the figure.

Thus if this voltage is applied to the gate and source terminal of second MOSFET, the resulting current will be,

$$I_{out} = f(V_{GS2})$$

$$V_{GS2} = V_{ref}$$

$$I_{out} = f(f^{-1}(V_{ref}))$$

$$\boxed{I_{out} = V_{ref}}$$

Two identical NMOSFETs that have equal gate source voltage and operate in saturation carry equal currents.

From the figure, the current mirror structure consists of M_1 and M_2 . In general case, the devices need not be identical. [Device dimensions need not be identical].

Neglecting channel-length modulation, we can write,

$$P_{ref} = \frac{1}{\alpha} \mu m \cos\left(\frac{\omega}{L}\right) (V_{ref} - V_{in})^2$$

$$P_{out} = \frac{1}{2} \mu n C_{ox} \left(\frac{W}{L} \right)_2 \left(V_{gs2} - V_{th} \right)^2$$

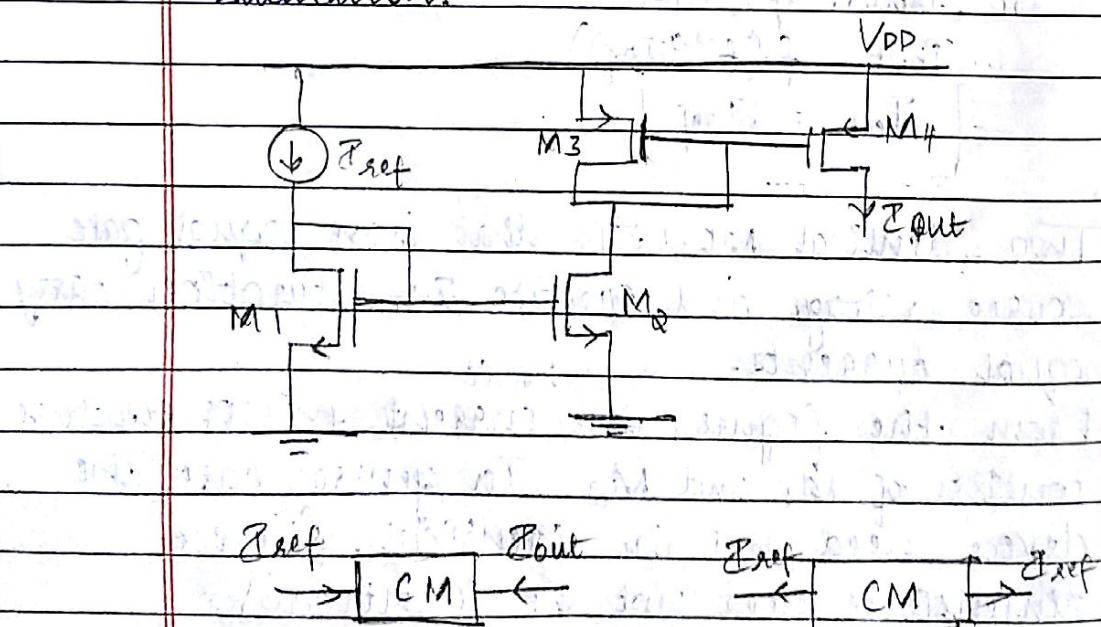
$$\underline{\text{Pout}} = \underline{(W/L)_2}$$

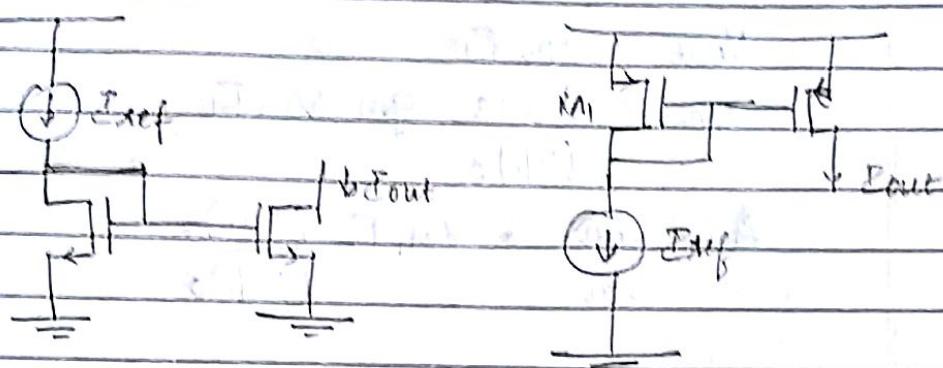
Reef (ω/h)₁

$$\text{Effout} = \frac{(\text{W(L)})_2}{(\text{W(L)})_1} \cdot \text{Effref}$$

The key property of this topology is that it allows copying of the current with no dependency on process and temperature. The ratio of I_{out} & I_{ref} is given by the ratio of device dimensions (a quantity that can be controlled with reasonable accuracy).

- ① Find the drain current of M4 of the figure given below if all the transistors are in saturation.





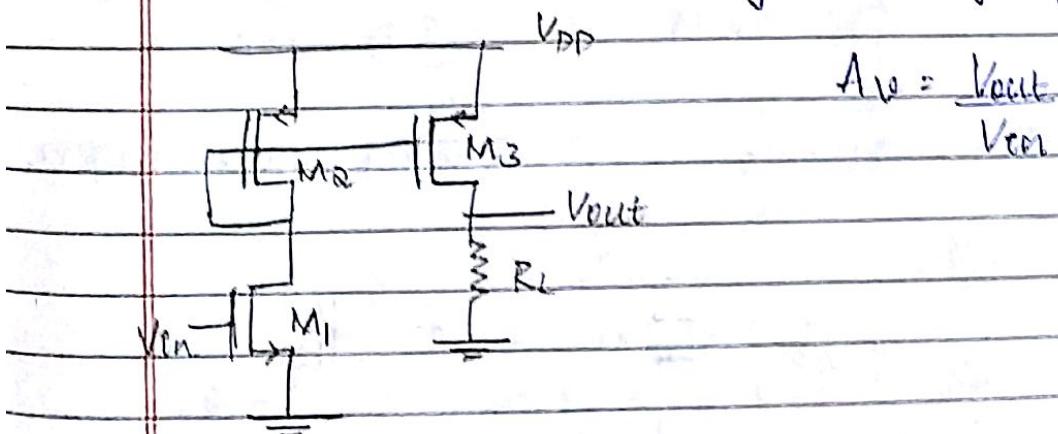
$$I_{D3} = \frac{(W/L)_2}{(W/L)_1} I_{ref}$$

$$I_{D4} = I_{D3}$$

$$I_{D4} = \frac{(W/L)_4}{(W/L)_3} I_{D3}$$

$$I_{D4} = \frac{(W/L)_4}{(W/L)_3} \times \frac{(W/L)_2}{(W/L)_1} I_{ref}$$

Q) Calculate the small signal voltage gain



$$g_{m1} = \frac{I_D}{V_{gs}} = \frac{I_{D1}}{V_{gs1}}$$

$$I_{D1} = g_{m1} V_{gs1} = g_{m1} V_{in}$$

$$I_{D2} = I_{D1}$$

$$I_{D3} = \frac{(W/L)_3}{(W/L)_2} \cdot I_{D2} = \frac{(W/L)_3}{(W/L)_2} \cdot I_{D1}$$

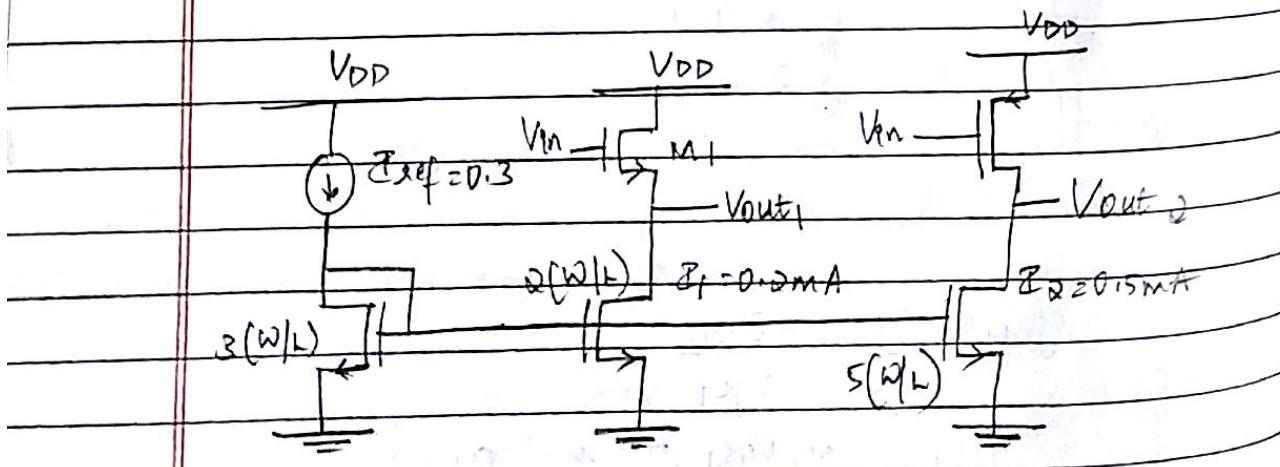
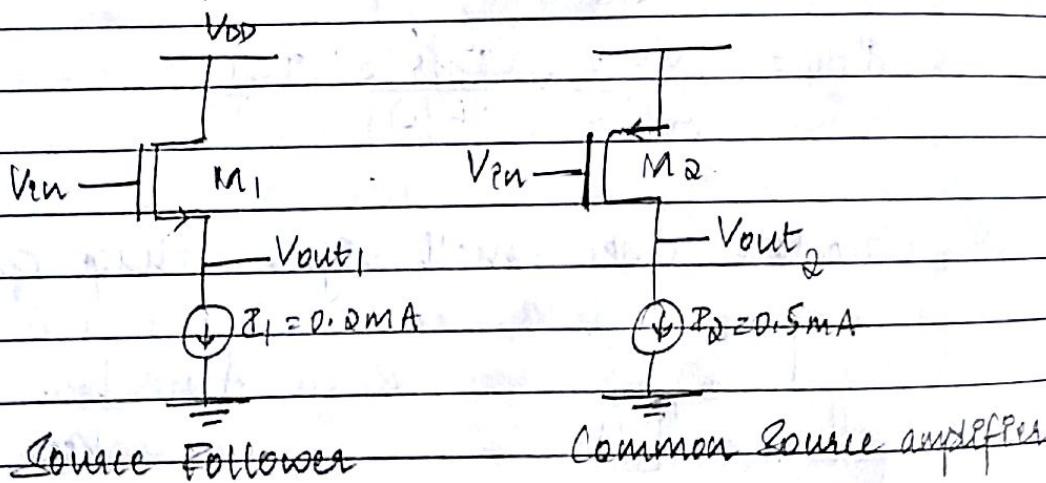
$$V_{out} = I_D R_L$$

$$V_{out} = \frac{W}{L} g_m V_{in} R_L$$

$$\frac{C}{(W/L)}_0$$

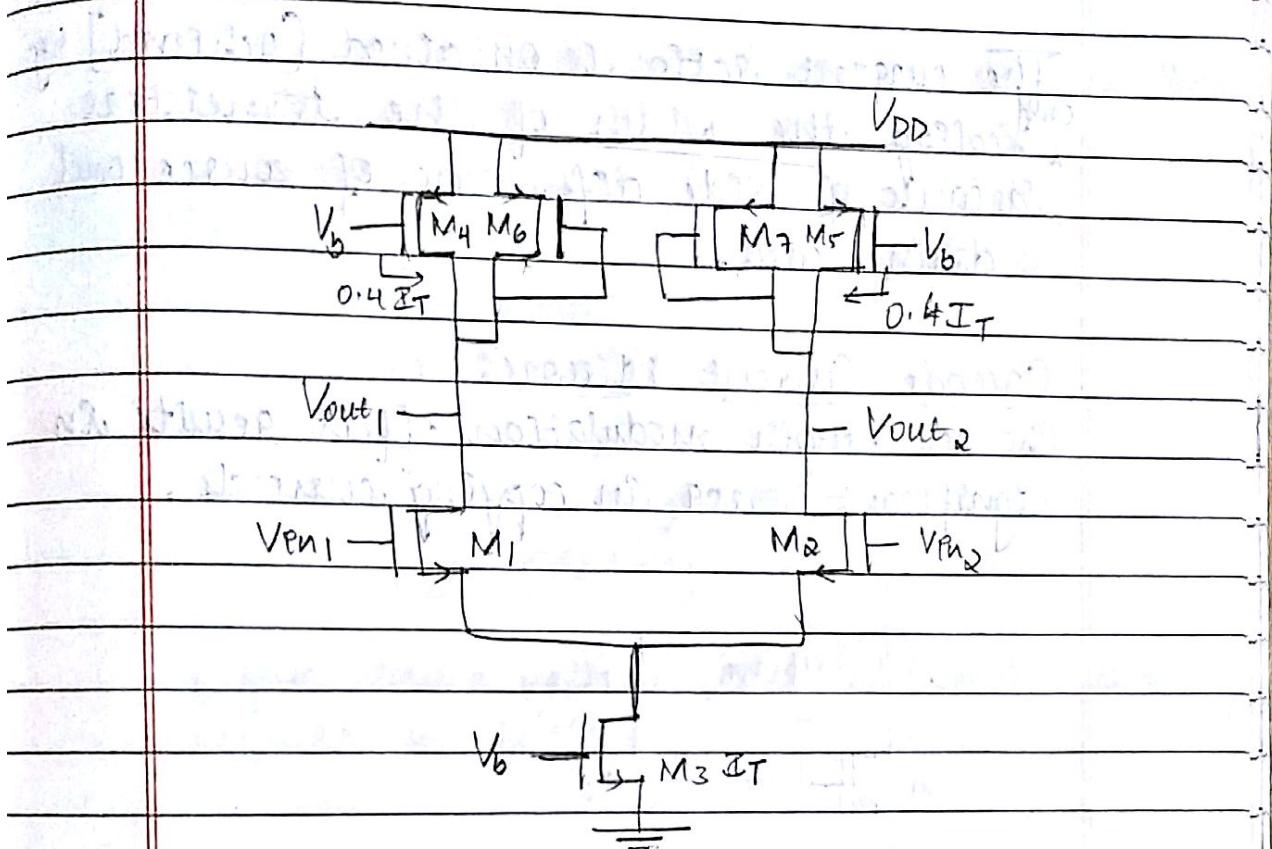
$$A_v = \frac{V_{out}}{V_{in}} = g_m R_L \frac{C}{(W/L)}_0$$

(3) An integrated circuit consist of source follower and common source amplifier as shown in the figure. Design a current mirror to provide/generate I_1 and I_2 with 0.3mA as the reference current.



$$\frac{I_1}{I_{ref}} = \frac{2}{3}$$

$$\frac{I_2}{I_{ref}} = \frac{5}{3}$$



$$(2N+1)^2 \left(\text{arctan} \frac{1}{2N+1} \right)^2 = \frac{\pi^2}{4} \cdot \frac{1}{(2N+1)^2}$$

$$(68\sqrt{6} + 15)^{\circ} \text{ (approx. } 97.5^{\circ} \text{ approx.) with } \frac{1}{\sqrt{6}} = 0.2887$$

$$(\overline{a_1}a_2a_3) \cdot a_4(a_5a_6) = \overline{a_1}a_2a_3a_4a_5a_6$$

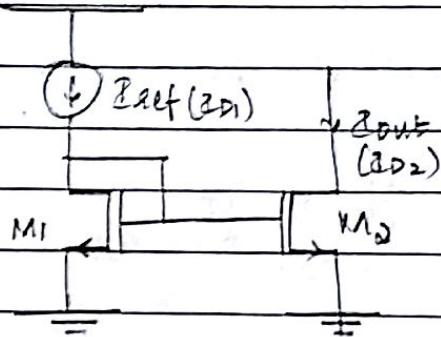
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Leptochilus *lanceolatus* (L.) Steyermark

The current ratio is obtained [acheived] by
only scaling the width of the transistors
because of side diffusions of source and
drain area.

Cascade Current Mirror:

Channel length modulation effect results in significant error in copying currents.

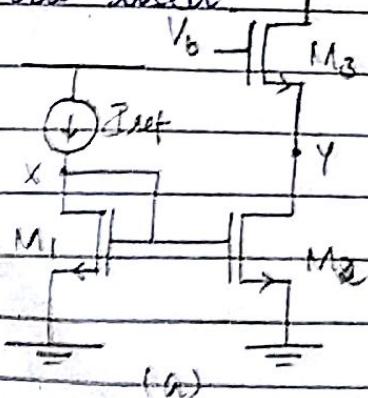


$$Z_{out} = \frac{1}{2} \mu n C_{ox} \left(\frac{W}{L} \right)_2 (V_{GS2} - V_{th})^2 (1 + \lambda V_{DS2})$$

$$Z_{ref} = \frac{1}{2} \mu n C_{ox} \left(\frac{W}{L} \right)_1 (V_{GS1} - V_{th})^2 (1 + \lambda V_{DS1})$$

$$\frac{Z_{out}}{Z_{ref}} = \frac{Z_{D2}}{Z_{D1}} = \frac{(W/L)_2}{(W/L)_1} \frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})}$$

In order to suppress the effect of channel length modulation, cascade current source can be used.



(a)

$$V_b = V_{q50} + V_{n2}$$

As shown in figure 'a' V_b is chosen such that
 $(V_x = V_y) V_a$ is close to V_y .

$P_{D_1} = P_{D_2}$ with high accuracy.

The objective is to ensure $V_1 \leq V_2$ so,

$$V_{GS3} = V_G - V_C$$

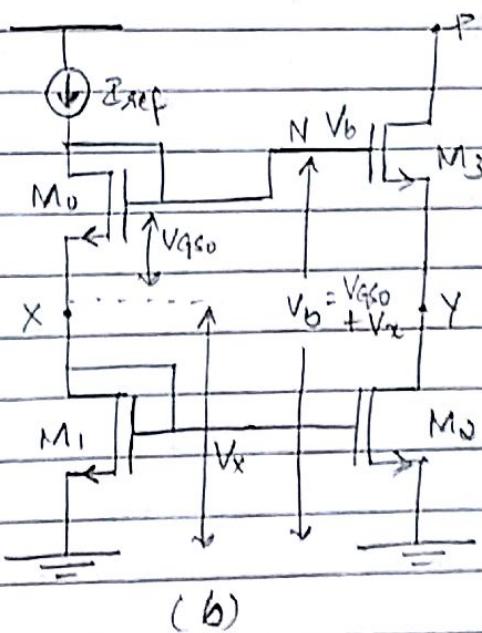
$$\frac{V_{GS3}}{2} = V_b - V_y$$

$$V_b = V_{QS3} + V_y$$

$$V_b - V_{GSS} = V_y = V_x$$

$$V_b = Vg_{\ell_3} + V_N$$

If gate-source voltage is added to V_x , the required V_b is generated.



As shown in figure 'b', diode connected M₀ device is connected in series with M₁ thereby generating $V_b = V_{GS0} + V_x = V_N$. If M₀ and M₃ are with identical dimension, then $V_{GS0} = V_{GS3}$. Now, connect this V_N to a gate of

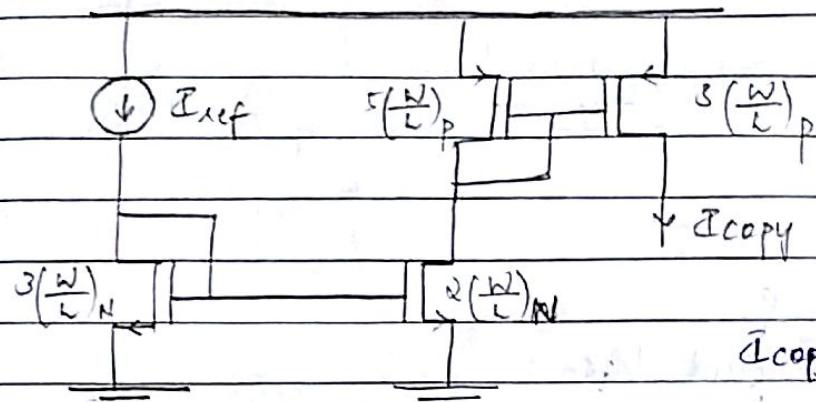
$$V_{GS3} + V_y = V_{GS0} + V_x$$

$$VN = V_{GSS} + Vy$$

$$V_N = V_{qs0} + V_\alpha$$

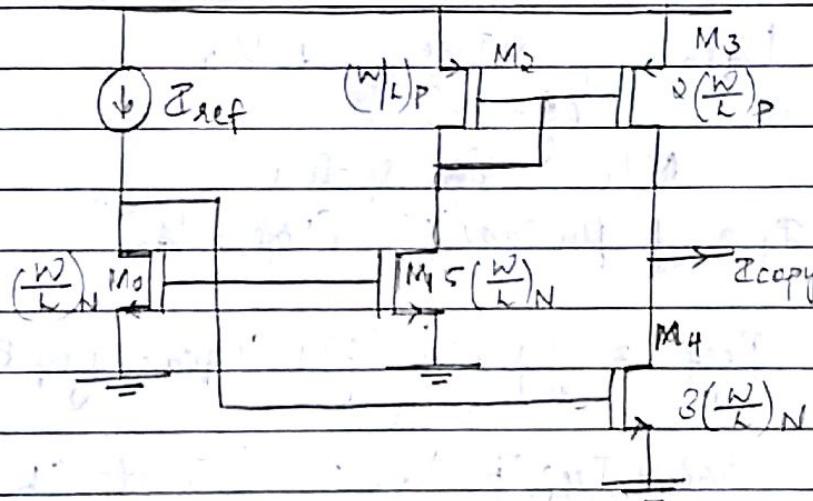
① Calculate I_{copy} from each of the circuits.
assume all the transistors operate in saturation.

i)



$$I_{\text{copy}} = \frac{2}{5} I_{\text{ref}}$$

ii)



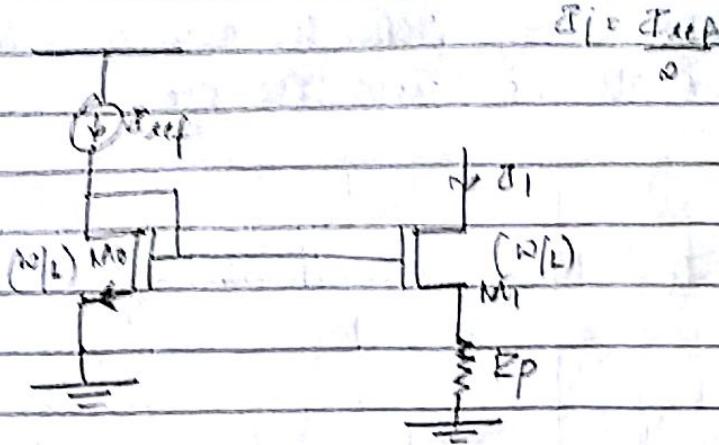
$$I_{\text{through } M_3} = 10 I_{\text{ref}}$$

$$I_{\text{through } M_4} = 3 I_{\text{ref}}$$

$$I_{\text{copy}} = 10 I_{\text{ref}} - 3 I_{\text{ref}}$$

$$I_{\text{copy}} = 7 I_{\text{ref}}$$

② Determine the value of R_p in the circuit such that $I_i = I_{\text{eff}}/2$, With the choice of R_p , does I_i change if the threshold voltage of both transistors is increased by ΔV_0 .



To find V_{gs0} :

$$I_{ref} = \frac{1}{2} \mu n C_{ox} \left(\frac{W}{L} \right) (V_{gs0} - V_{th})^2$$

$$V_{gs0} = \sqrt{\frac{I_{ref}}{\mu n C_{ox} \left(\frac{W}{L} \right)}} + V_{th}$$

N.B. \rightarrow Saturation.

$$I_1 = \frac{1}{2} \mu n C_{ox} \left(\frac{W}{L} \right) (V_{ds} - V_{th})^2$$

$$I_{ref} = \frac{1}{2} \mu n C_{ox} \left(\frac{W}{L} \right) (V_{gs0} - \frac{I_{ref} R_p}{2} - V_{th})^2$$

$$V_{gs0} - \frac{I_{ref} R_p}{2} - V_{th} = \sqrt{\frac{I_{ref}}{\mu n C_{ox} \left(\frac{W}{L} \right)}}$$

$$\frac{I_{ref} R_p}{2} = V_{gs0} - V_{th} - \sqrt{\frac{I_{ref} \left(\frac{W}{L} \right)}{\mu n C_{ox}}}$$

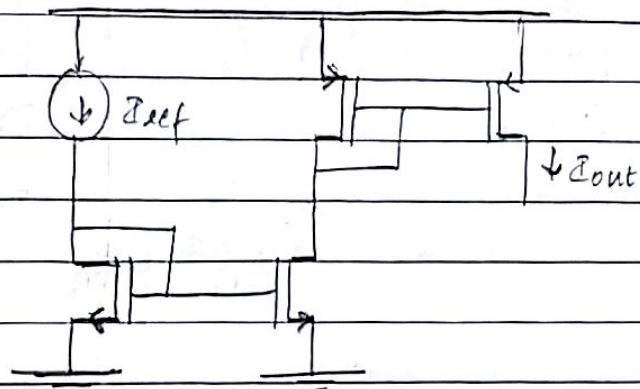
$$R_p = \frac{2}{I_{ref}} \left[V_{gs0} - V_{th} - \sqrt{\frac{I_{ref} \left(\frac{W}{L} \right)}{\mu n C_{ox}}} \right]$$

$$R_p = \frac{2}{I_{ref}} \left[\sqrt{\frac{2 I_{ref}}{\mu n C_{ox} \left(\frac{W}{L} \right)}} - \sqrt{\frac{I_{ref}}{\mu n C_{ox} \left(\frac{W}{L} \right)}} \right]$$

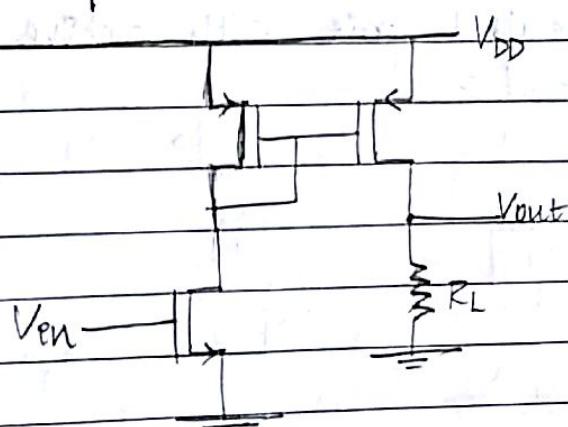
$$R_p = \frac{2 (\sqrt{2} - 1)}{\sqrt{I_{ref} \mu n C_{ox} \left(\frac{W}{L} \right)}}$$

ii) $R_p = ? \quad P_1 = 0.8 \text{ mW}$

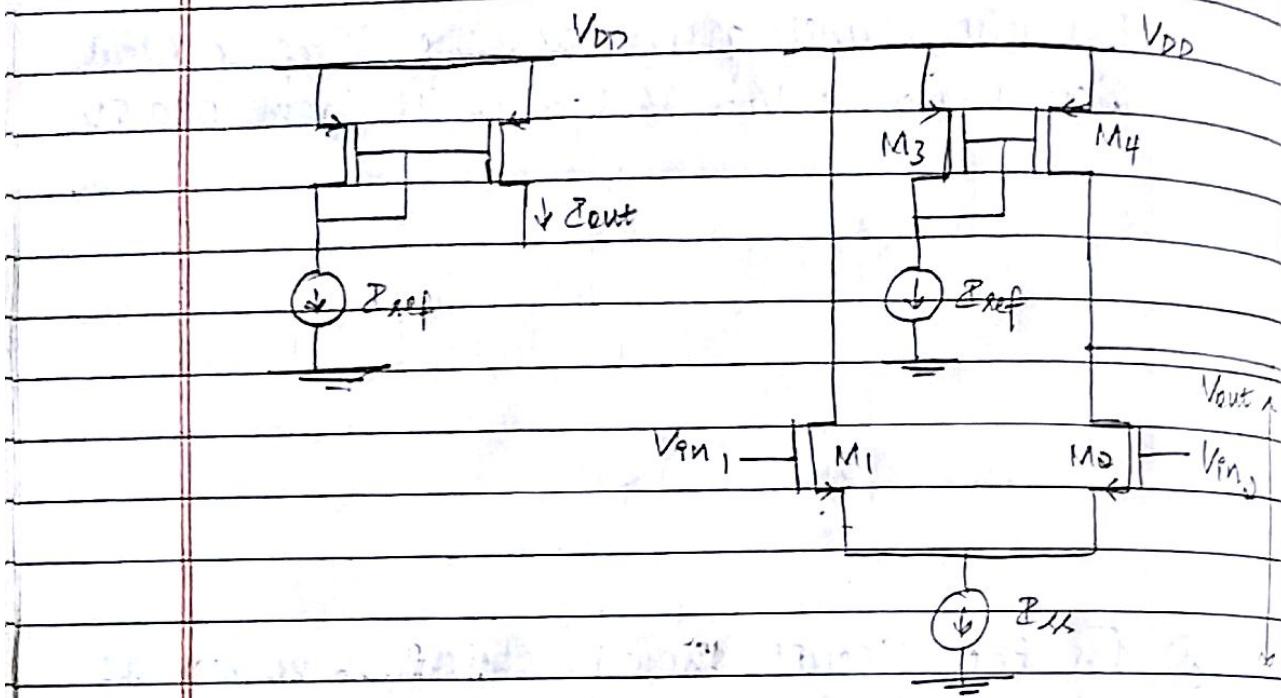
- (b) For the circuit given, assume β_{ref} is ideal
Sketch I_o vs V_{DD} as V_{DD} varies from 0 to 5V.



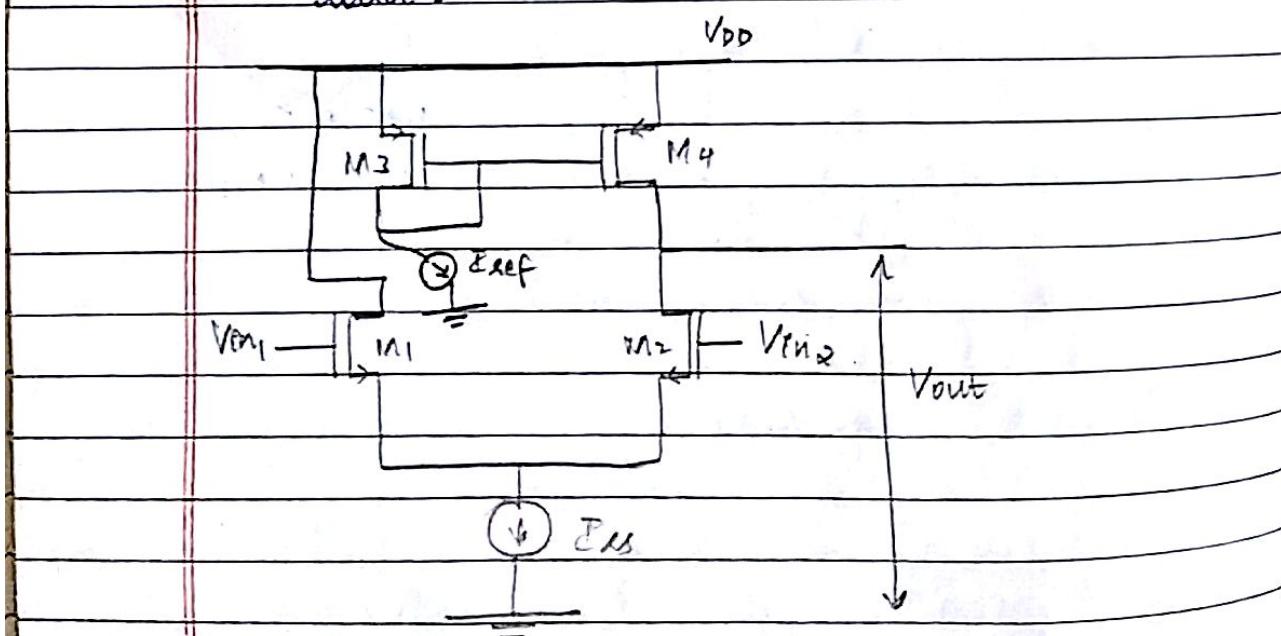
- (a) For the circuit shown, sketch V_o vs V_{DD} as V_{DD} varies from 0 to 5V



Active Current Mirror :-



Differential pair with active current mirror load :



Voltage Gain (using small signal analysis)

$$A_V = \frac{V_{out}}{V_{in}}$$

$$A_V = G_m R_{out}$$

$$G_m = \frac{V_o}{V_{in}}$$

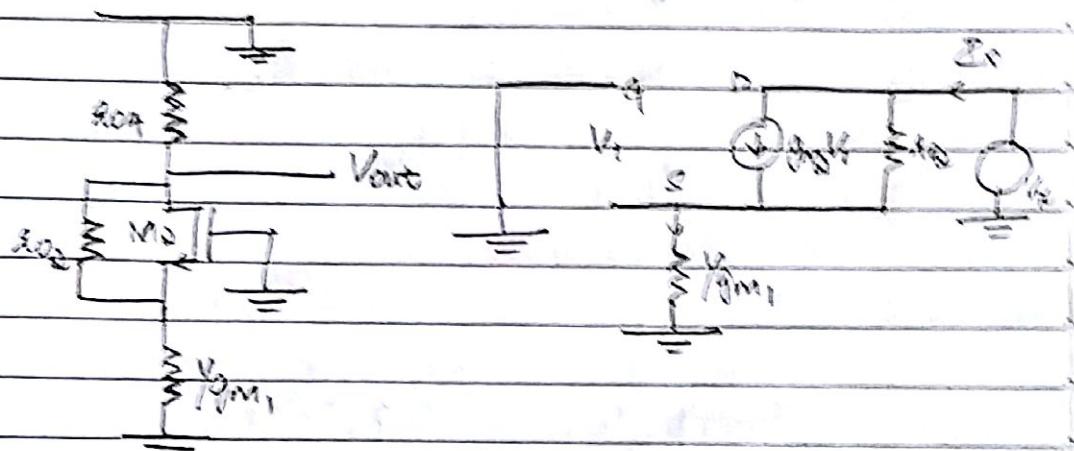
$M_1 \in M_2$

$$g_{m1} = g_{m2}$$

$$I_{out} = \frac{g_{m1} V_{in}}{2}$$

$$G_m = \frac{g_{m1} V_{in}/2}{V_{in}} = \frac{g_{m1}}{2}$$

To calculate I_{out} :



$$V_i = -V_c = -\frac{I_x}{g_{m1}}$$

$$I_x = g_{m1} \frac{V_i}{g_{m1}}$$

$$\text{Current through } R_{O2} = I_x - g_{m1} V_i = I_x + \frac{I_x g_{m1}}{g_{m1}}$$

$$V_x = V_{in} + V_i$$

$$V_i = g_{m2} \left[I_x + \frac{I_x g_{m1}}{g_{m1}} \right] + \frac{I_x}{g_{m1}}$$

$$V_x = \left[(1 + g_{m1} g_{m2}) \frac{1}{g_{m1}} + g_{m2} \right] I_x$$

$$R_{out} = \frac{V_x}{I_x} = (1 + g_{m1} g_{m2}) \frac{1}{g_{m1}} + g_{m2}$$

$$R_{out} = \frac{1}{g_{m1}} + g_{m2}$$

$$\frac{1}{g_m} \ll 2R_o$$

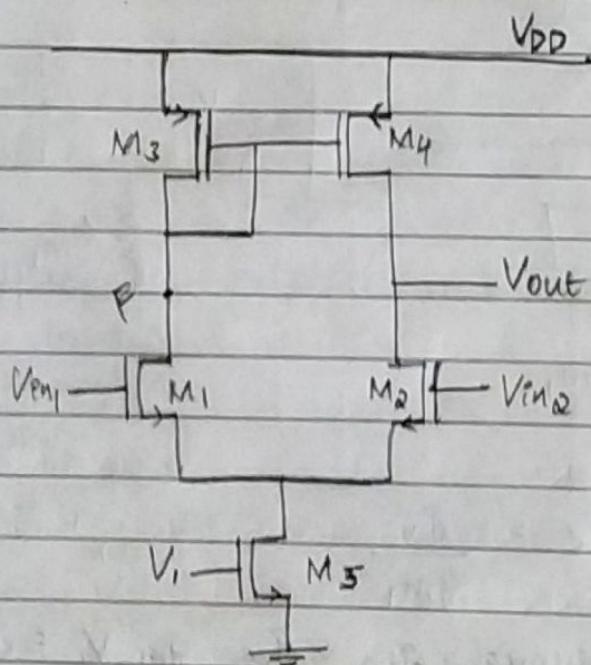
$$R_{out} \approx 2R_o$$

$$R_{out} = R_{in} \parallel R_{out} = R_{in} \parallel 2R_o$$

$$A_v = g_m R_{out}$$

$$A_v = \frac{g_m}{2} (R_{in} \parallel 2R_o)$$

Large Signal Analysis:



Case 1: V_{in_1} is more negative than V_{in_2}

$$\text{i.e. } V_{in_1} > V_{in_2} < V_{in_2}$$

0.7 -1 3

$$(V_{in_1} - V_{in_2}) = -V_e$$

$M_1 \rightarrow \text{OFF}$

$M_3 \& M_4 \rightarrow \text{OFF}$

$M_2 - \text{ON}$ [Deep Triode Region $\delta_{D2}=0$]

$M_5 - \text{ON}$ [Deep Triode Region $\delta_{D5}=0$]

$$\boxed{V_{out} = 0V}$$

Case 2: V_{in_1} is greater than V_{th} & less than V_{in_2} .

$$(V_{in_1} - V_{in_2}) = -v.$$

This V_{in_1} turns on M_1 , M_3 and M_4 .

V_{out} depends on the difference between i_{D_4} and i_{D_2} .

If V_{in_1} is more negative than V_{in_2} , i_{D_1} , i_{D_3} , i_{D_4} increases and i_{D_2} decreases.

Eventually driving M_2 into triode region.

⇒ If $V_{in_1} - V_{in_2}$ is significantly large (i.e. $V_{in_2} < V_{th}$) then M_2 turns off. M_4 operates in deep triode region with zero current. $V_{out} \approx V_{DD}$.

The choice of input commonmode voltage of the circuit is also important. M_2 to be in saturation, the output voltage cannot be less than $V_{in_2} - V_{th}$. Thus to allow maximum output swing, V_{in_2} must be as low as possible with the minimum given by $V_{GS2} + V_{DS2}$.

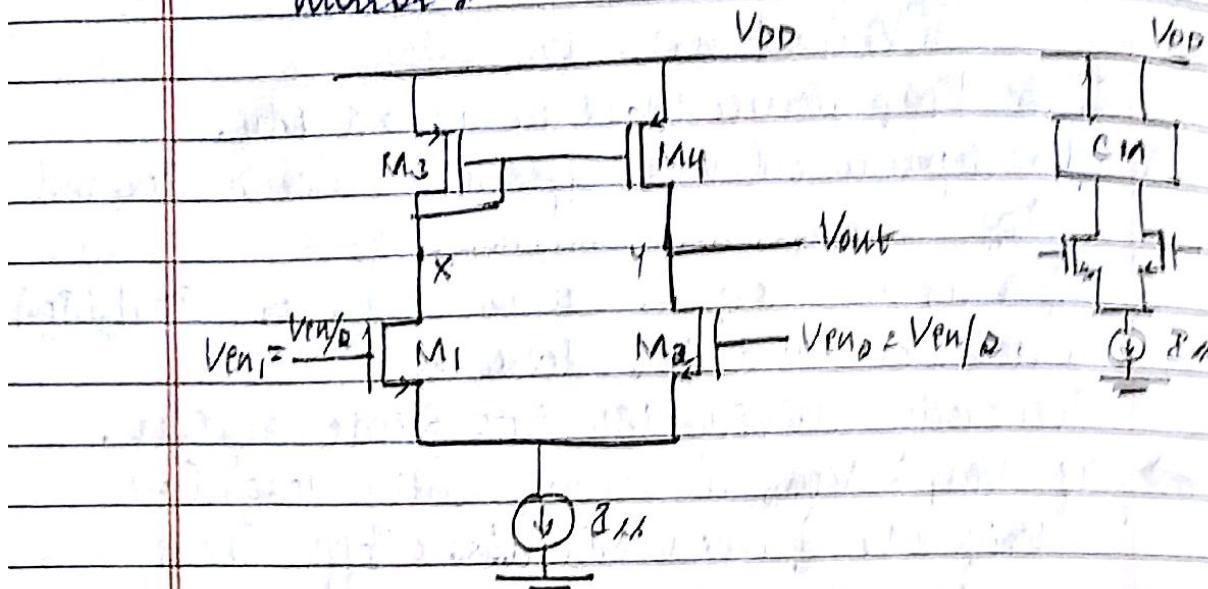
The direct relationship between the V_{in_2} and output swing in this circuit is critical drawback.

When $V_{out} < V_F$

- M_1 carries more current than M_2 .
- This means i_{D_1} is greater than i_{D_2} .
- i.e. total current through M_3 also exceeds i_{D_2} .
- Violating assumption that M_4 carries more current than M_3 .

Small-signal Analysis with Active Current Mirror

mirror :-



method

Half circuit is used to calculate differential gain.

With small differential inputs, the voltage swing at node X and node Y are different.

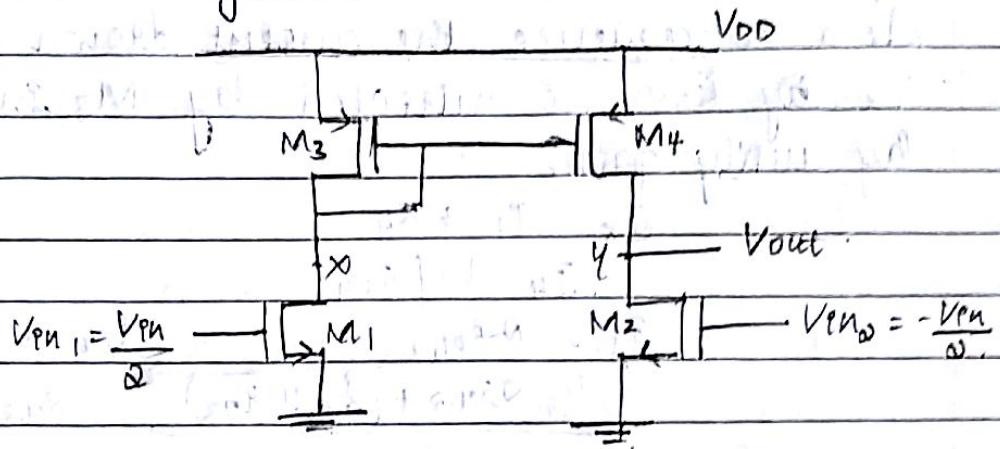
An asymmetric op-amp using in a differential pair with active current mirror. This is because, the diode connected device M3 yields a much smaller voltage gain from input to node X than that from input to node Y. So the effect of V_{in1} and V_{in2} at node 'P' through R_{o1} and R_{o2} respectively do not cancel each other.

The node cannot be considered as a virtual ground (AC ground).

1st Approach for gain calculation :-

The circuit is not quite symmetric but because the impedance seen at node X is

relatively low and the swing at this node is small. The current returning from node X to P through node Y is negligibly small and now P can be viewed as a neutral ground or AC ground.



$$A_v = G_m R_{out}$$

$$G_m = \frac{I_{out}}{V_{in}} = \frac{g_{m1} V_{in}}{V_{in}} = g_{m1,0}$$

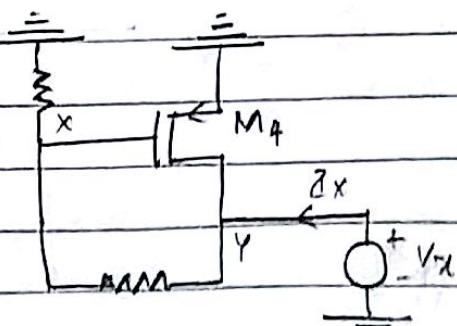
$$I_{D1} = |I_{D3}| = |I_{D4}| = g_{m1,0} \frac{V_{in}}{2}$$

$$I_{D2} = -g_{m1,0} V_{in} / 2$$

$$I_{out} = I_{D4} - I_{D2} = g_{m1,0} V_{in}$$

To calculate R_{out} :

When the voltage is applied to the output to measure R_{out} , the gate voltage of M4 does not remain constant, the respective equivalent circuit is as shown in figure.



For small signal, current source is open, hence any current flowing into M₁ must flow out of M₂ and the role of 2 resistors R_{O1} & R_{O2} can be represented by a resistor R_{ox} = R_{O1,2}.

As a consequence, the current drawn from V_x by R_{ox} is mirrored by M₃ into M₄ by unity gain.

$$I_x = I_1 + I_4$$

$$I_H = V_x / R_{O4}$$

$$I_1 = \alpha R_{O1,2}$$

$$V_x = V_x$$

$$\frac{2R_{O1,2} + (\frac{1}{gm_3} || R_{O3})}{R_{O1,2}}$$

$$I_x = \frac{\alpha V_x}{2R_{O1,2} + (\frac{1}{gm_3} || R_{O3})} + \frac{V_x}{R_{O4}}$$

where factor 'α' accounts for current copying action of M₃ and M₄.

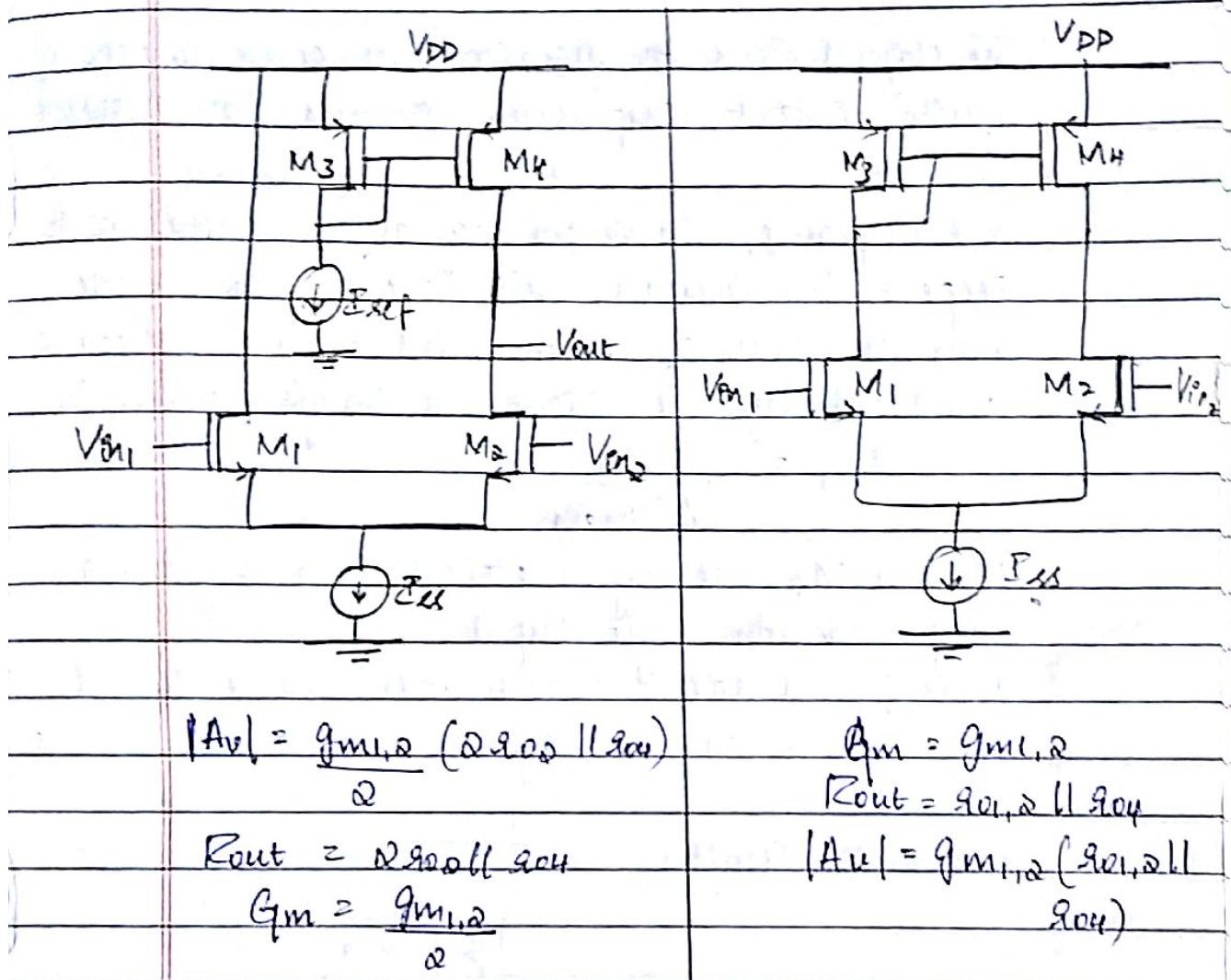
$$\left(\frac{R_{O3} || 1}{gm_3} \right) \ll \alpha R_{O1,2} \text{ neglect } \left(\frac{1}{gm_3} || R_{O3} \right)$$

$$I_x = V_x \left(\frac{1}{R_{O1,2}} + \frac{1}{R_{O4}} \right)$$

$$R_{out} = \frac{V_x}{I_x} = R_{O1,2} || R_{O4}$$

$$\text{Gain, } A_v = gm_{out}$$

$$A_v = \underline{gm_{H,D}} (R_{O1,2} || R_{O4})$$



$$|A_V| = \frac{g_{m1,2}}{2} (2g_{o2} || g_{o1})$$

$$G_m = g_{m1,2}$$

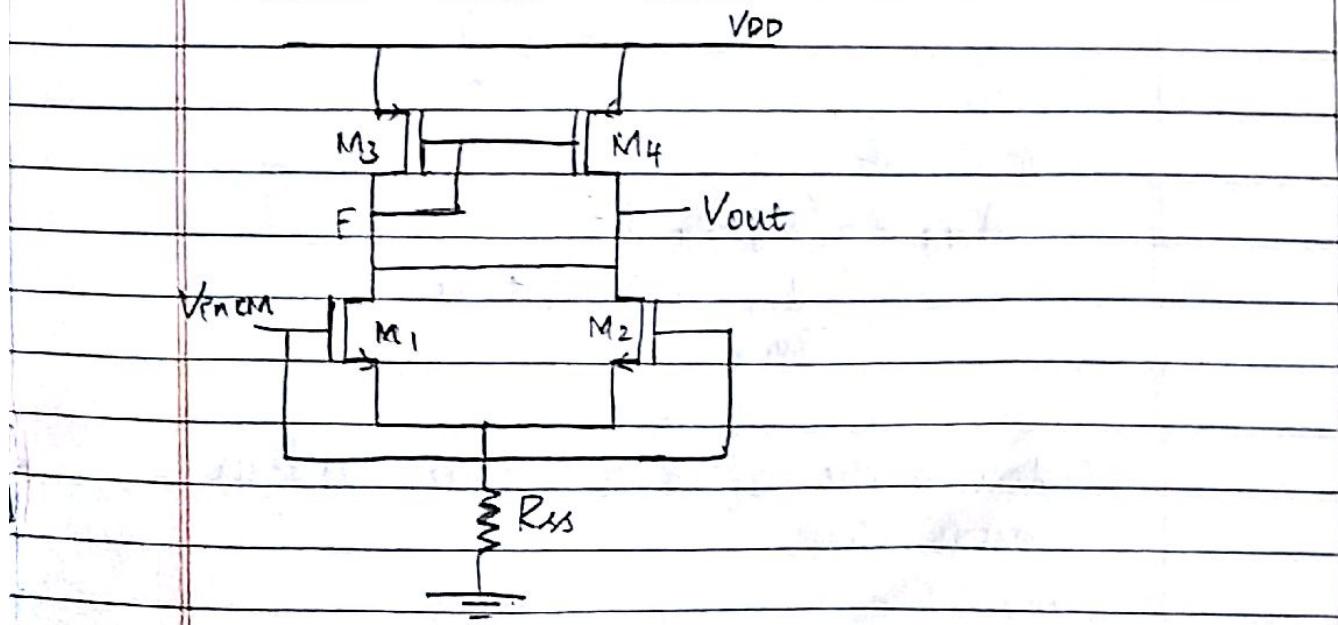
$$R_{out} = g_{o1,2} || g_{o4}$$

$$R_{out} = 2g_{o2} || g_{o4}$$

$$G_m = \frac{g_{m1,2}}{2}$$

$$|A_V| = g_{m1,2} (g_{o1,2} || g_{o4})$$

Common-mode properties of differential pair with Active current mirror:-



The objective is to predict the consequences of finite output impedance in the ideal current source.

In the figure, the output signal is sensed with respect to ground. Thus the common mode gain in terms of single ended output component produced by the input change is given by,

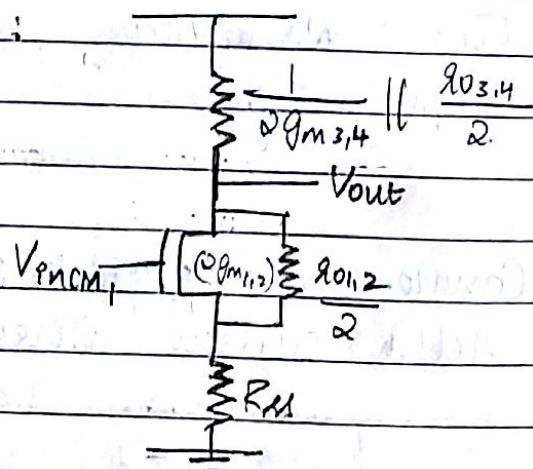
$$A_{CM} = \frac{\Delta V_{out}}{\Delta V_{inCM}}$$

Assuming

M_1 and M_2 are symmetrical, $V_{out} = V_F$ for any common mode input.

Node F and node M output node can be shorted as shown in the figure.

Equivalent circuit:



$$V_F = V_{out}$$

$$A_{CM} = - \frac{1}{\alpha g_{m_{3,4}}} \parallel \frac{R_{0,4}}{\alpha} \cdot \left(\frac{1}{\alpha g_{m_{1,2}}} \parallel \frac{R_{0,1,2}}{\alpha} \right) + R_{in}$$

Neglecting the effect of channel-length modulation,

$$A_{CM} = - \frac{1}{(1 + \alpha g_{m_{1,2}} R_{in})} \cdot \frac{g_{m_{1,2}}}{g_{m_{3,4}}}$$

$$Q_2 X \quad V_{D2} = -0.1V \quad R_{DS2} = 35\Omega \quad I_D = 1A$$

Common Mode Rejection Ratio,

$$CMRR = \frac{A_{diff}}{A_{common}}$$

$$CMRR = \frac{(1 + 2g_m L_s R_s) g_m}{g_m^2 / 2 g_m L_s}$$

$$CMRR = \frac{(1 + 2g_m L_s R_s) g_m}{g_m^2 / 2 g_m L_s} (g_m \parallel g_m)$$

ASSIGNMENT PROBLEMS:

- ① The total capacitance between adjacent lines is 10PF. The resistance from drain of M₁ to ground is 100Ω.

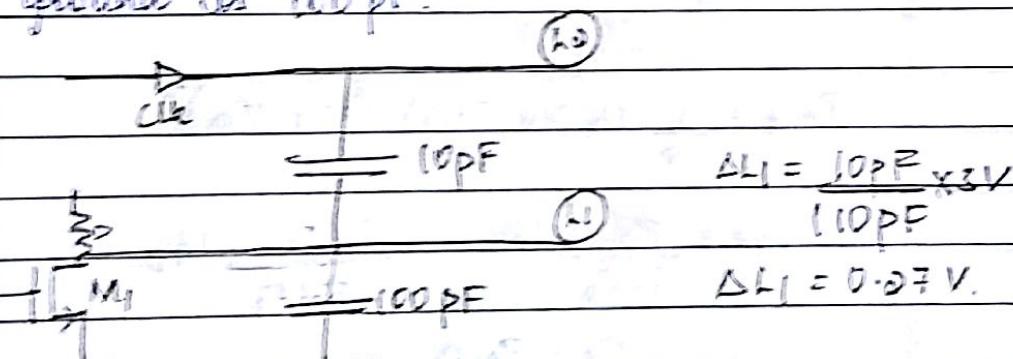
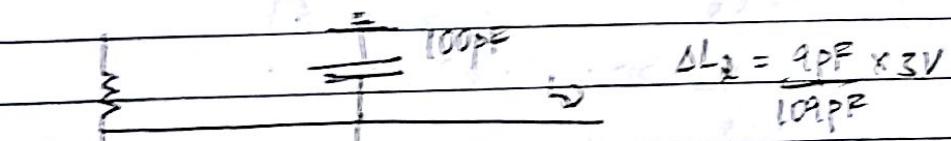


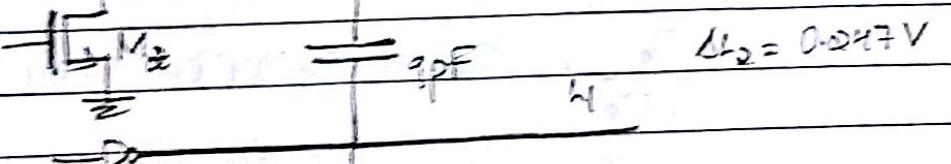
fig 4.2 (a)

$$\Delta L_1 = \frac{10PF \times 3V}{110PF}$$

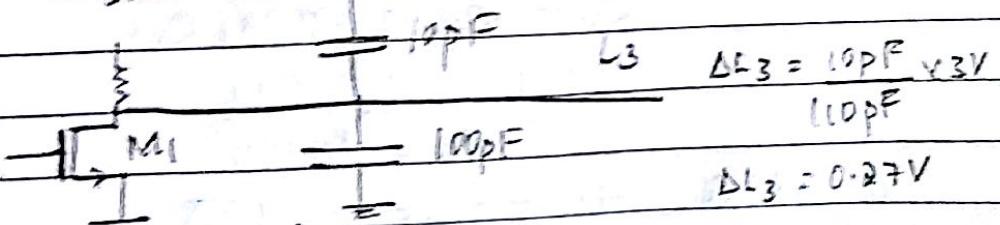
$$\Delta L_1 = 0.07V.$$



$$\Delta L_2 = 0.07V$$



$$\Delta L_2 = 0.07V$$



$$\Delta L_3 = \frac{10PF \times 3V}{110PF}$$

$$\Delta L_3 = 0.07V$$

fig 4.2 (b)

$$\Delta V = \Delta L_3 - \Delta L_2$$

$$\Delta V = 0.27 - 0.047$$

NOTE :- $V_{DD} = 3V$

nMOS

pMOS

$$V_{TH} = 0.4V$$

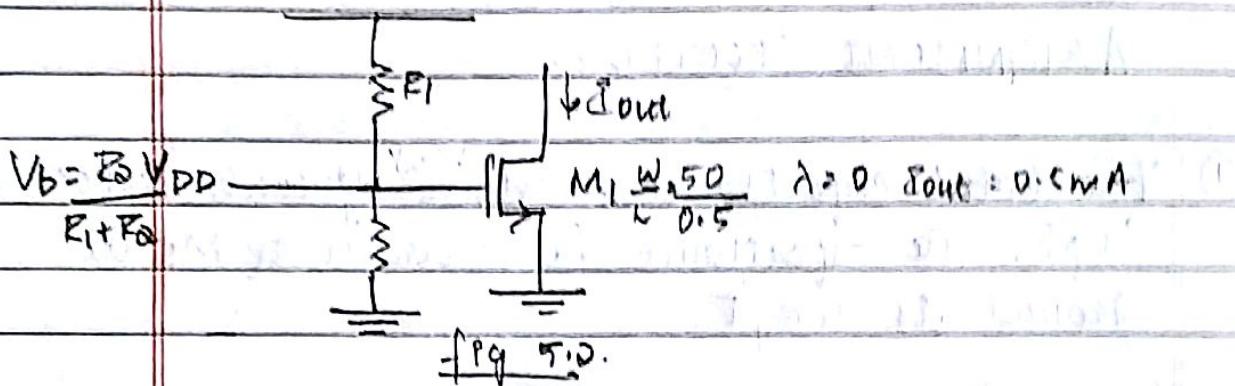
$$V_{TP} = 0.8V$$

$$\mu_n C_{ox} = 13.4 \mu A/V^2 \quad \mu_p C_{ox} = 34.3 \mu A/V^2$$

$$\lambda = 0.1$$

$$\lambda = 0.12$$

⇒ Find E_0/E_1



$$P_{out} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{TH})^2$$

$$V_{GS} = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{R_2 / R_1}{1 + R_2 / R_1} V_{DD}$$

$$R_x = R_2 / R_1$$

$$\frac{R_x}{1 + R_x} V_{DD} = \sqrt{\frac{2 I_{Dout}}{\mu_n C_{ox} (W/L)}} + V_{TH}$$

$$\frac{R_x}{1 + R_x} V_{DD} = 0.073 + 0.7$$

$$\frac{R_x}{1 + R_x} = 0.091 \quad 0.091 \cdot R_x = 0.3043$$

$$R_x = 0.091 + 0.091 R_x$$

$$0.091 R_x = 0.091$$

$$R_x = 0.100$$

$$0.6757 R_x \rightarrow 0.007 R_x \rightarrow 0.973$$

$$R_x = \frac{0.3043}{0.6757} \rightarrow 0.458$$

b) Calculate the sensitivity of I_{out} to V_{DD} and
normalize to I_{out} .

$$\text{Sensitivity normalize to } I_{out} = \frac{dI_{out}}{dV_{DD}}$$

$$I_{out} = \frac{1}{2} \mu n C_o \left(\frac{W}{L} \right) \left(\frac{R_o}{1+R_o} V_{DD} - V_{th} \right)^2$$

$$\frac{dI_{out}}{dV_{DD}} = \frac{\mu n C_o \left(\frac{W}{L} \right)}{1+R_o} \left(\frac{R_o}{1+R_o} V_{DD} - V_{th} \right) \left(\frac{R_o}{1+R_o} \right)$$

$$\begin{aligned} \frac{dI_{out}}{dV_{DD}} &= \frac{1}{2} \mu n C_o \left(\frac{W}{L} \right) \left(\frac{R_o}{1+R_o} V_{DD} - V_{th} \right)^2 \\ &= \frac{0.5 \left(R_o / 1+R_o \right)}{\frac{V_{DD} R_o - V_{th}}{1+R_o}} \end{aligned}$$

$$= \frac{0}{V_{DD} - V_{th} (1 + 1/R_o)}$$

$$= \frac{0}{3 - 0.7 (3.0833)}$$

$$= \frac{0}{3 - 0.1583}$$

$$= \frac{0}{0.8416}$$

$$= \underline{0.37}$$

c) How much does I_{out} change if V_{th} changes by 50 mV.

$$\frac{dI_{out}}{dV_{th}} = \Delta I_{out}$$