Chapter 5: Current Mirrors and Biasing Techniques

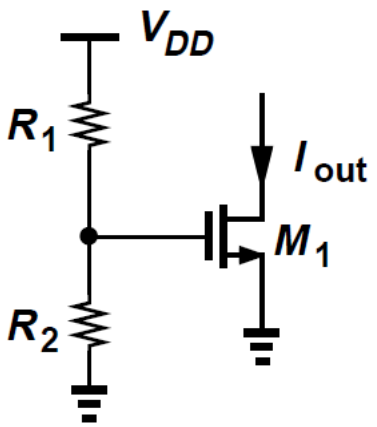
5.1 Basic Current Mirrors

5.2 Cascode Current Mirrors

5.3 Active Current Mirrors

5.4 Biasing Techniques

Basic Current Mirrors

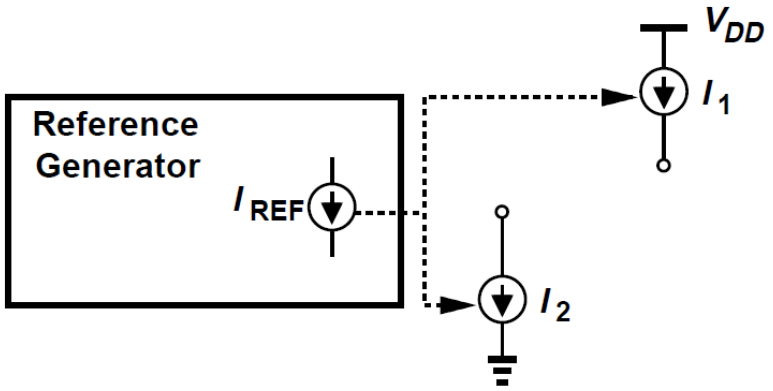


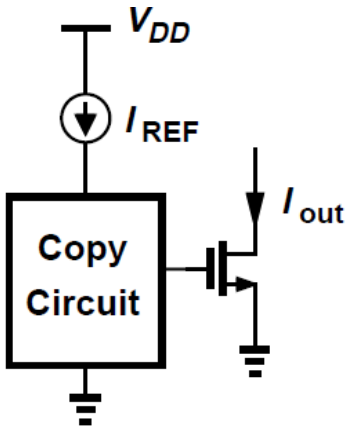
- **AssumingM1 is in saturation, we can write**

$$I_{out} \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1+R_2}V_{DD}-V_{TH}\right)^2.$$

- **The threshold voltage may vary by 50 to 100 mV from wafer to wafer**
- **Both μn and V_{TH} exhibit temperature dependence**
- **We must seek other methods of biasingMOS current sources.**

Conceptual means of copying currents



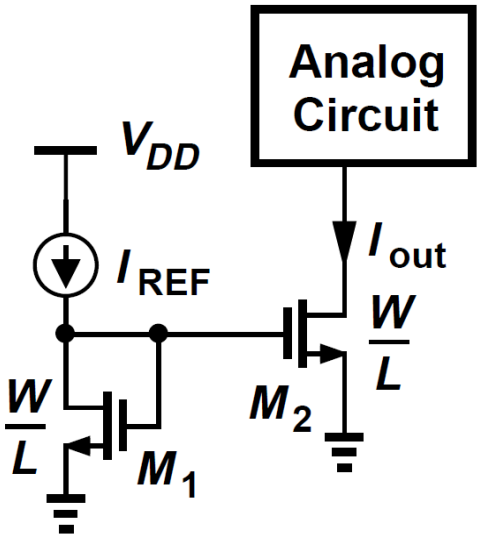


- **Use of a reference to generate various currents.**

$$I_{out} = f[f^{-1}(I_{REF})] = I_{REF}$$

- **Two identical MOS devices that have equal gate-source voltages and operate in saturation carry equal currents**

Effect of Channel-Length Modulation



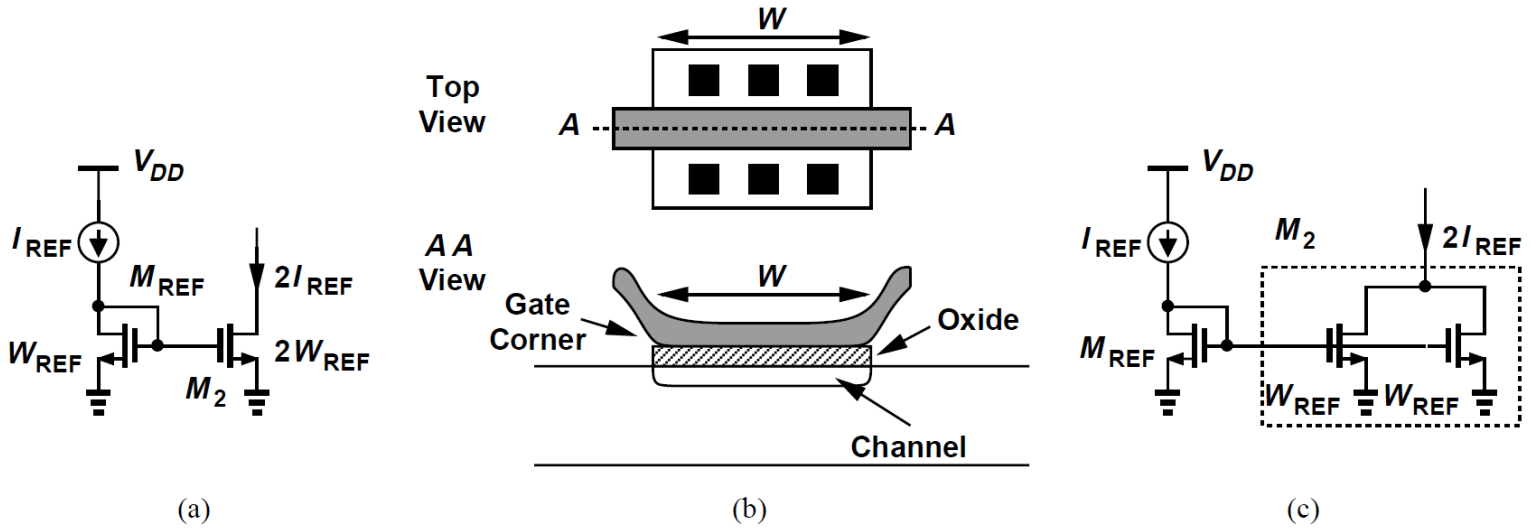
- **Neglecting channel-length modulation, we can write**

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$$
$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2,$$

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}.$$

- **Allows precise copying of the current with no dependence on process and temperature**

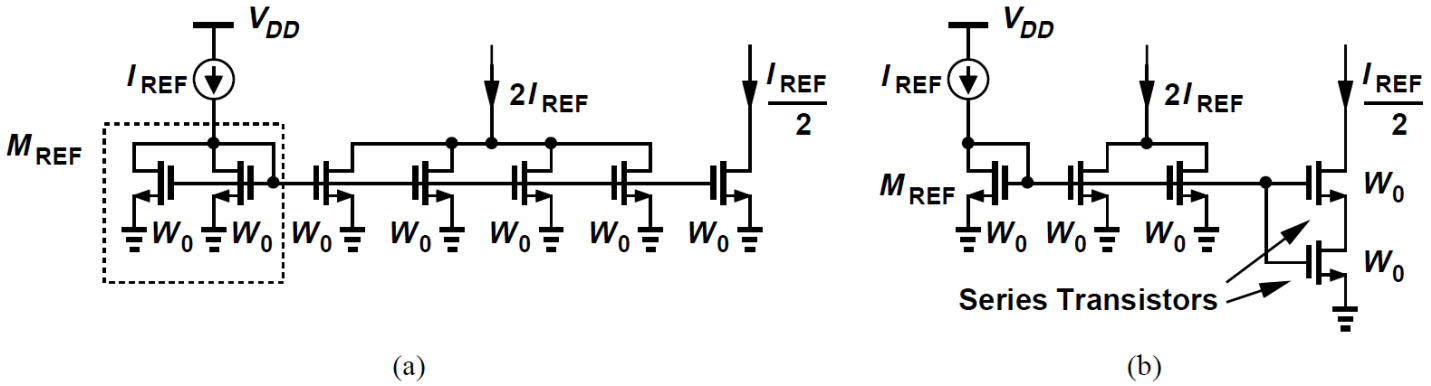
Sizing issues



- Current mirrors usually employ the same length for all of the transistors.
- Current ratioing is achieved by only scaling the width of transistors.
- Direct scaling of the width also faces difficulties.
- We thus prefer to employ a “unit” transistor and create copies by repeating such a device.

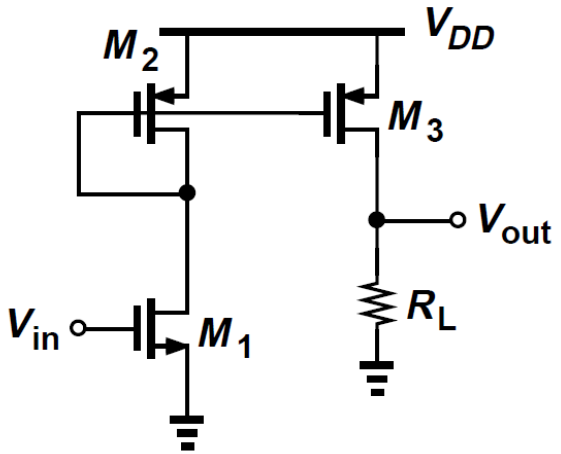
Sizing Issues

- How do we generate a current equal to $I_{REF}/2=2$ from I_{REF} ?



- (a) half-width device, and (b) series transistors
- Approach (b) preserves an effective length of (L_{drawn}-2L_D) for each unit, yielding an equivalent length of 2(L_{drawn} - 2L_D)
- Current mirrors can process signals as well, example next slide.

Example



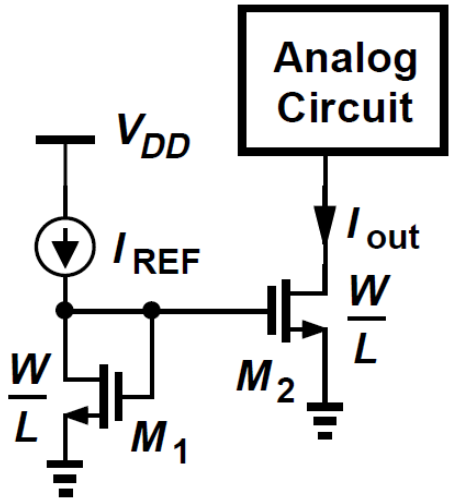
- **Calculate the small-signal voltage gain of the circuit shown in Figure.**

$$I_{D2} = I_{D1}$$

$$I_{D3} = I_{D2}(W/L)_3/(W/L)_2$$

- **Gain=** $g_{m1}R_L(W/L)_3/(W/L)_2$

Cascode Current Mirrors



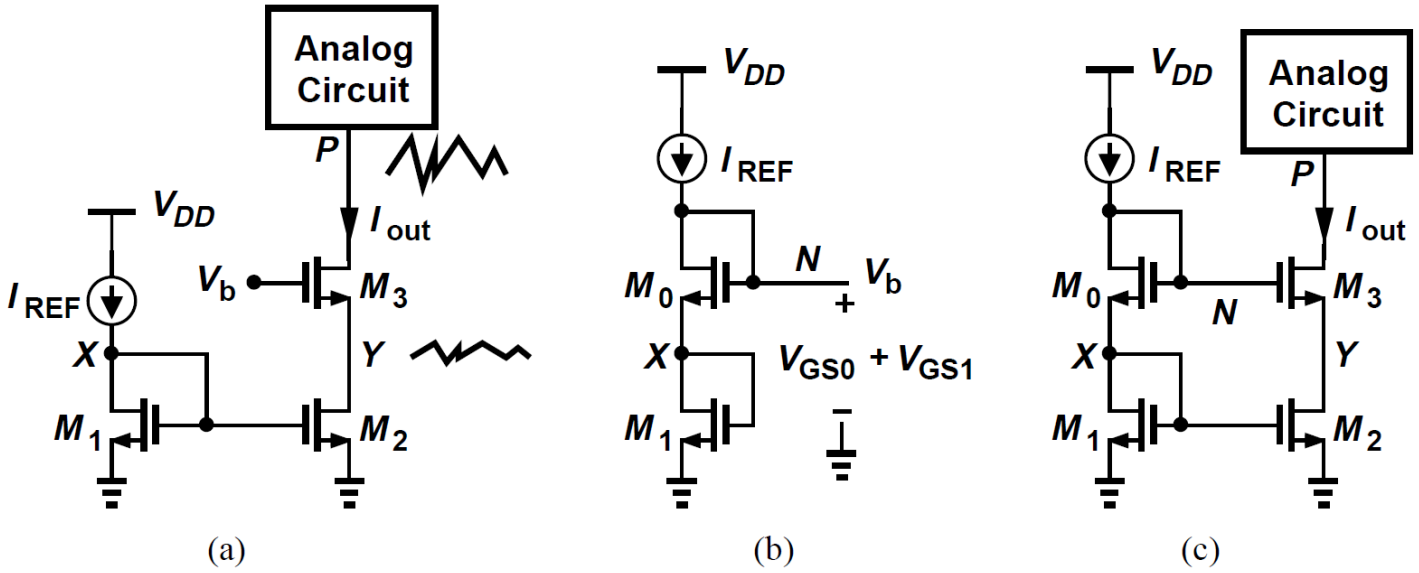
$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS1})$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS2})$$

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}.$$

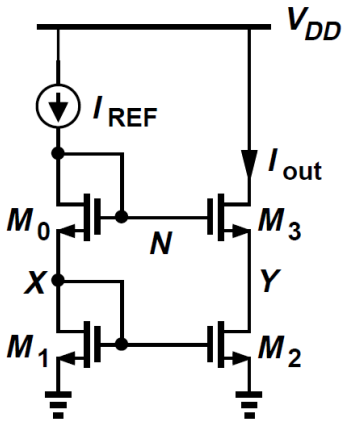
- **While $V_{DS1} = V_{GS1} = V_{GS2}$, V_{DS2} may not equal V_{GS2}**
- **We can (a) force V_{DS2} to be equal to V_{DS1}, or (b) force VDS1 to be equal to V_{DS2}.**

First Approach

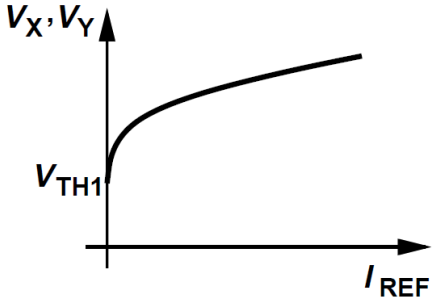


- **A cascode device can shield a current source, thereby reducing the voltage variations across it.**
- **But, how do we ensure that $V_{DS2} = V_{DS1}$?**
- **We must generate V_b such that $V_b - V_{GS3} = V_{DS1} (= V_{GS1})$**

Example



(a)



(b)

- **sketch VX and VY as a function of IREF. If IREF requires 0.5 V to operate as a current source, what is its maximum value?**

$$V_Y = V_X \approx \sqrt{2I_{REF}/[\mu_n C_{ox}(W/L)_1]} + V_{TH1}$$

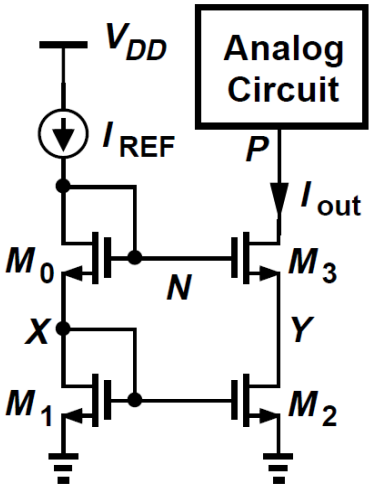
$$V_N = V_{GS0} + V_{GS1}$$

$$= \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}}}\left[\sqrt{\left(\frac{L}{W}\right)_0} + \sqrt{\left(\frac{L}{W}\right)_1}\right] + V_{TH0} + V_{TH1}$$

$$V_{DD} - \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}}}\left[\sqrt{\left(\frac{L}{W}\right)_0} + \sqrt{\left(\frac{L}{W}\right)_1}\right] - V_{TH0} - V_{TH1} = 0.5\ \text{V}$$

$$I_{REF,max} = \frac{\mu_n C_{ox}}{2}\frac{(V_{DD} - 0.5\ \text{V} - V_{TH0} - V_{TH1})^2}{(\sqrt{(L/W)_0} + \sqrt{(L/W)_1})^2}.$$

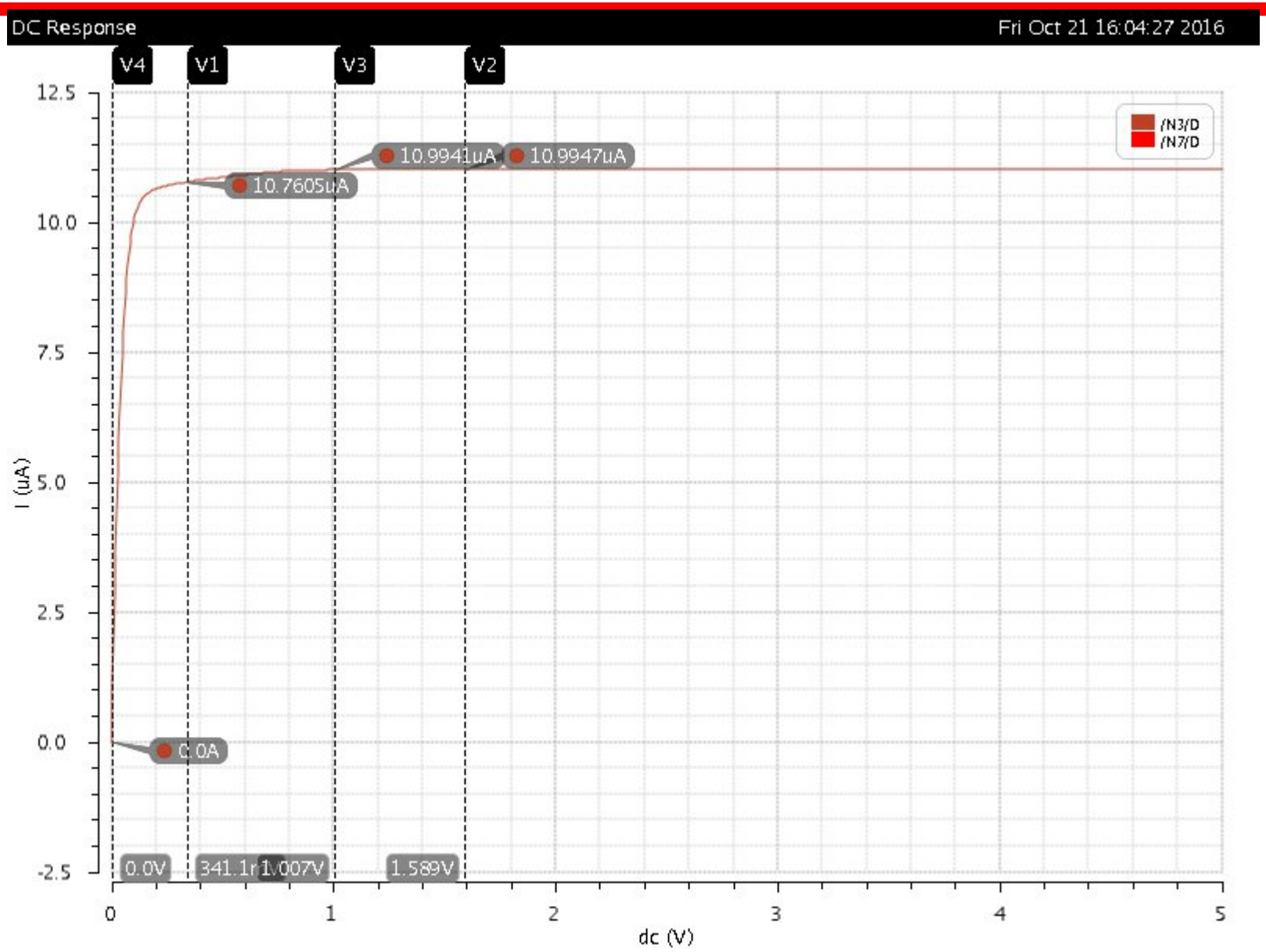
Example



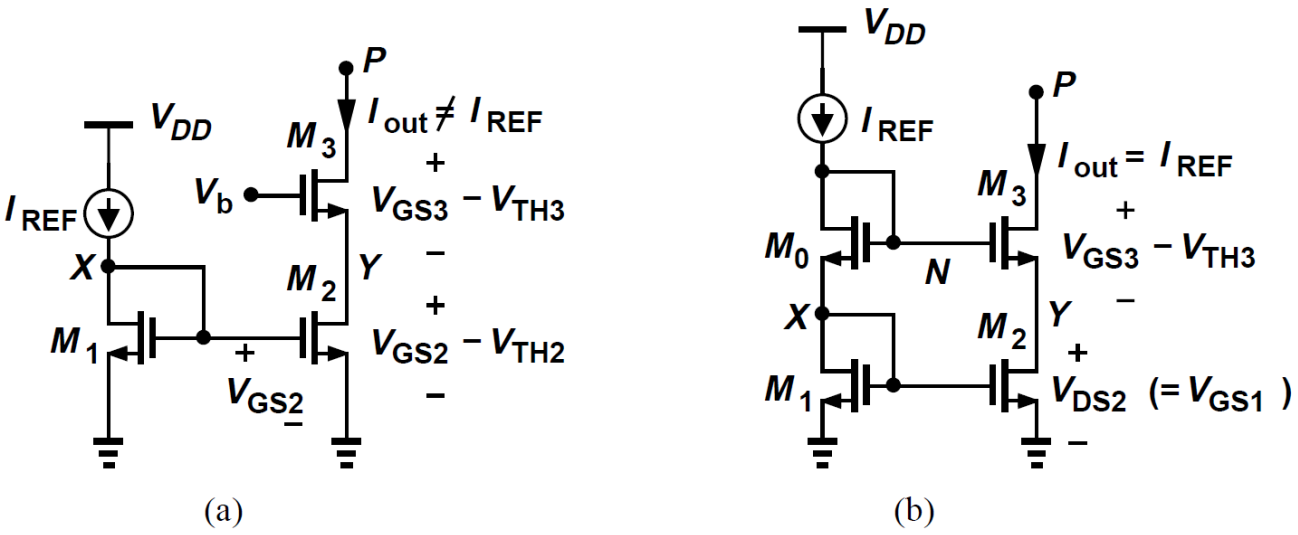
- **the minimum allowable voltage at node P is equal to**

$$\begin{aligned} V_N - V_{TH} &= V_{GS0} + V_{GS1} - V_{TH} \\ &= (V_{GS0} - V_{TH}) + (V_{GS1} - V_{TH}) + V_{TH} \end{aligned}$$

- **The cascode mirror "wastes" one threshold voltage in the headroom.**
- **Because $V_{DS2} = V_{GS2}$, whereas V_{DS2} could be as low as $V_{GS2} - V_{TH}$ while maintaining M2 in saturation.**

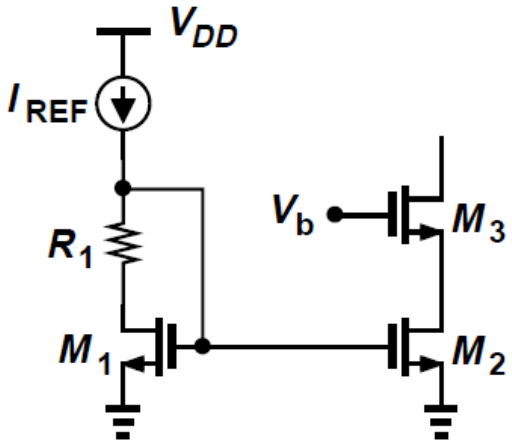


Approach summary



- In Fig(a), V_b is chosen to allow the lowest possible value of V_P but the output current does not accurately track I_{REF}.
- In Fig(b), a higher accuracy is achieved, but the minimum level at P is higher by one threshold voltage.

Second Approach

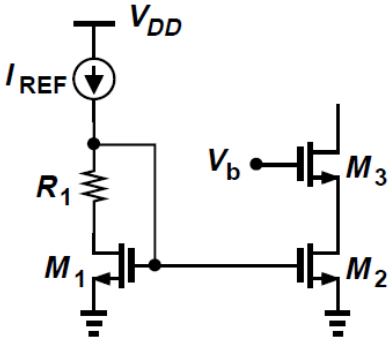


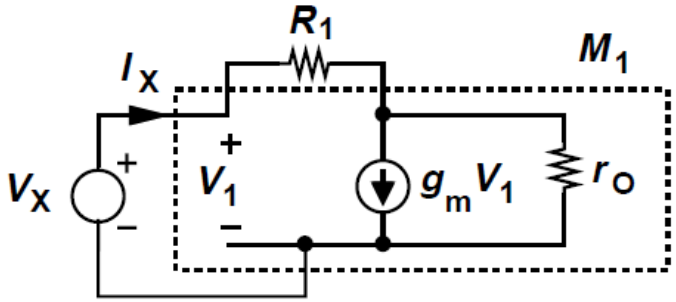
- Consider the branch shown in Fig. 5.16(b)
- As a candidate and write $V_b = V_{GS5} + R_6 I_6$.

$$R_1 I_{REF} \approx V_{TH1}$$

$$V_b = V_{GS3} + (V_{GS1} - V_{TH1})$$

Small signal Model





$$\frac{V_X - I_X R_1}{r_O} + g_m V_X = I_X.$$

$$\frac{V_X}{I_X} = \frac{R_1 + r_O}{1 + g_m r_O},$$

- **Reduces to 1/gm in the absence of channel-length modulation.**
- **Thus, from a small-signal point of view, the combination is close to a diode-connected device.**
- **But**

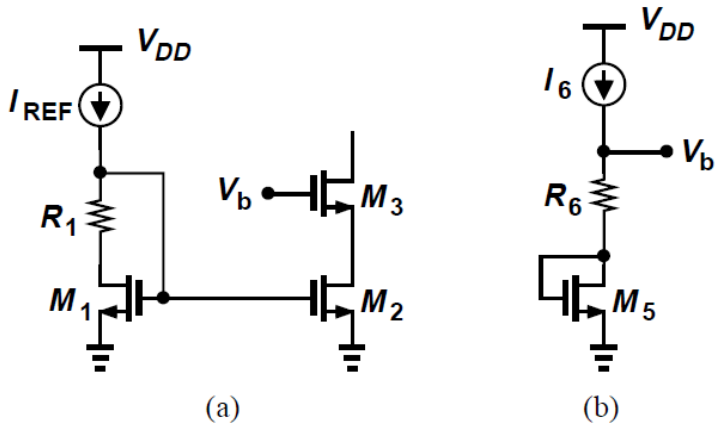
(1) It may be difficult to guarantee that $R_1 I_{REF} \approx V_{TH1}$

(2) The generation of

$$V_b = V_{GS3} + (V_{GS1} - V_{TH1})$$

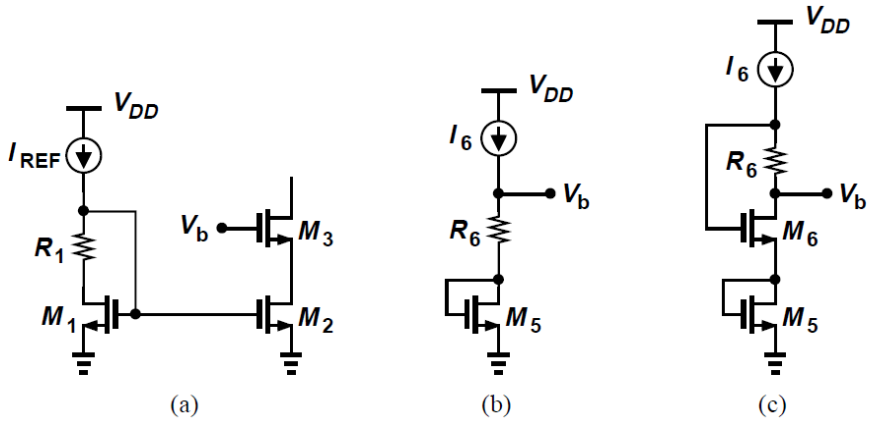
is not straightforward.

Generate Vb



- **Consider the branch shown in Fig(b) as a candidate and write $V_b = V_{GS5} + R_6 I_6$.**
- **$V_{GS5} = V_{GS3}$**
- **However, the condition $R_6 I_6 = V_{GS1} - V_{TH1} = V_{GS1} - R_1 I_{REF}$ is hard to meet.**

Generate Vb



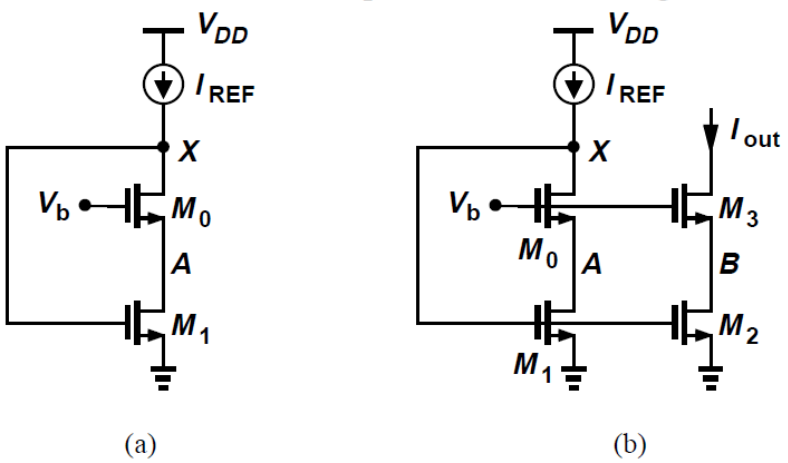
$$V_{GS5} = V_{GS3}$$

$$V_{GS6} - R_6 I_6 = V_{GS1} - V_{TH1}$$

$$= V_{GS1} - R_1 I_{REF}$$

- **It is now possible to ensure that V_{GS6} and V_{GS1} track each other.**
- **For example, we may simply choose $I_6 = I_{REF}$, $R_6 = R_1$, and (W/L)6 = (W=/L)1**

Another circuit topology

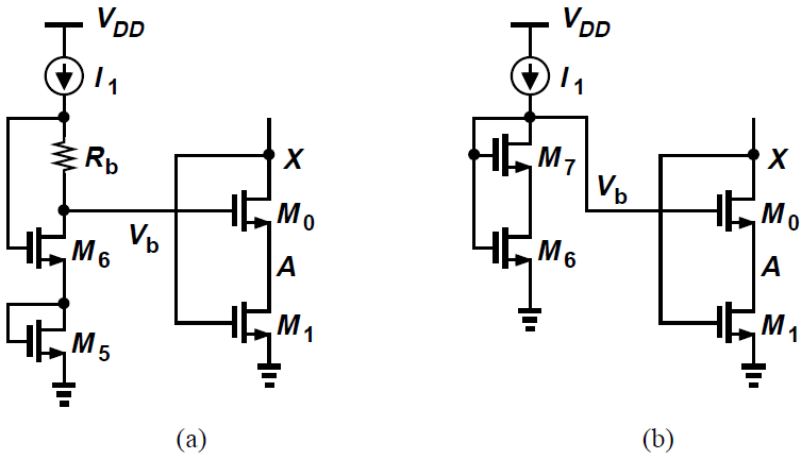


- **In this case**

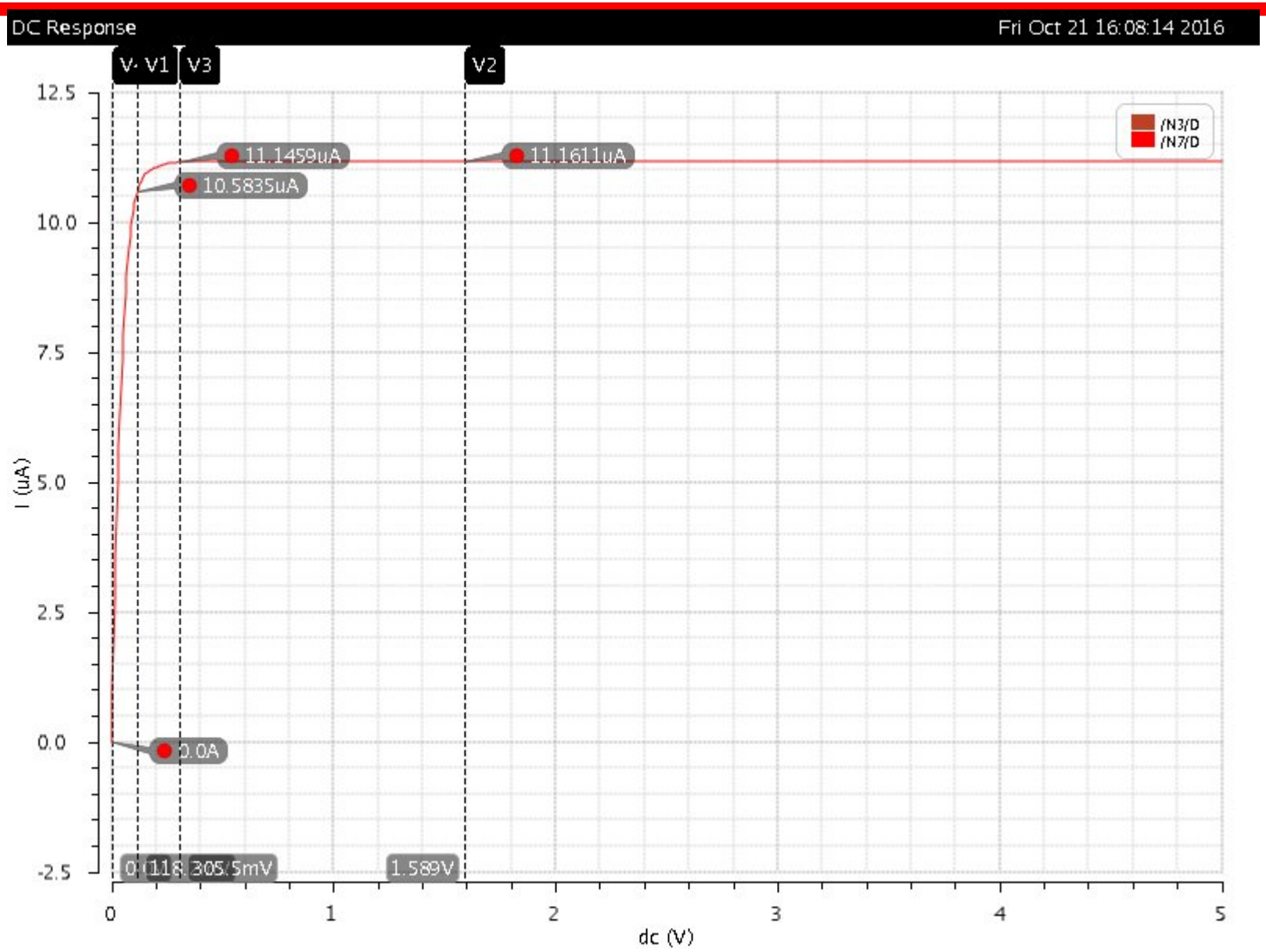
$$V_{DS1} = V_b - V_{GS0}$$

- **Must have** $V_b - V_{TH0} \leq V_X\ (= V_{GS1})$ **for M0 to be saturated and** $V_{GS1} - V_{TH1} \leq V_A\ (= V_b - V_{GS0})$ **for M1 to be saturated.**
- **A solution exists if** $V_{GS0} + (V_{GS1} - V_{TH1}) < V_{GS1} + V_{TH0}$
- **We must therefore sizeM0 to ensure its overdrive is well below VTH1.**

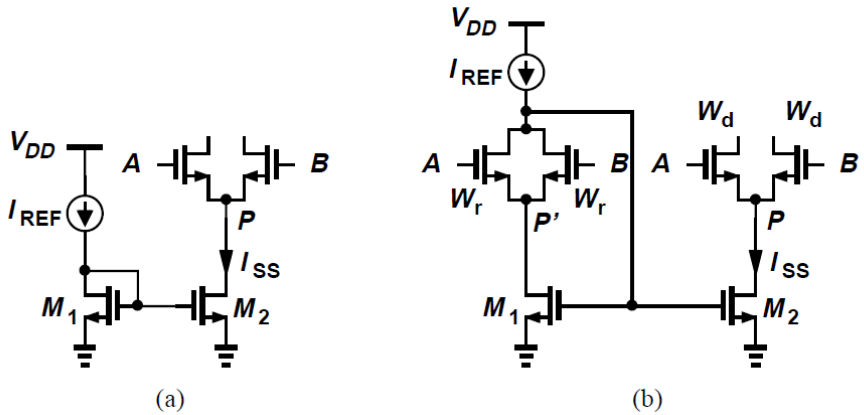
How to generate Vb



- **In figure (a)** $V_{DS6} = V_{GS6} - R_b I_1 \approx V_{GS1} - V_{TH1}$
- **Some inaccuracy nevertheless arises because M5 does not suffer from body effect whereas M0 does.**
- **Also, the magnitude of R6*I1 is not well-controlled.**
- **A simpler alternative is shown in Fig(b)**

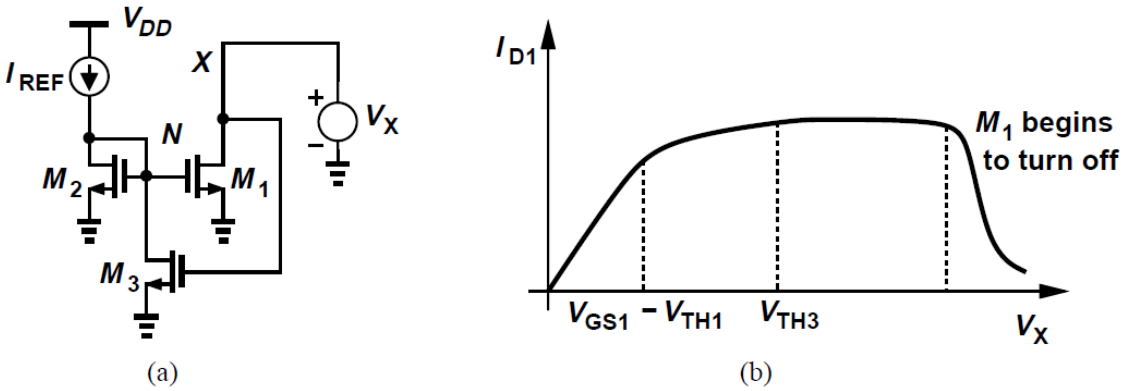


Example



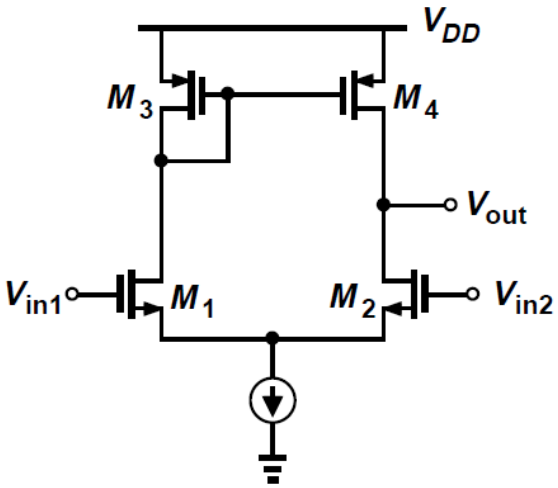
- **Voltage headroom is too small to allow the use of a cascode current source. Devise a method to reduce the current mirror error due to channel-length modulation.**
- **The voltages at P0 and P track even if the CM level at A and B varies.**
- **The two differential pairs must incorporate the same lengths and scale their widths according to Wr/Wd = I_{REF}/I_{SS}.**

Example



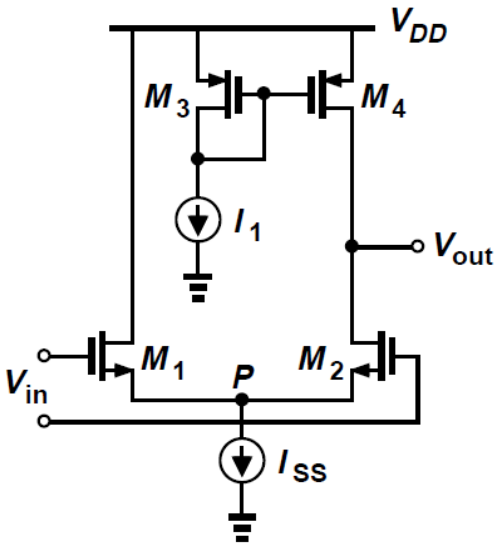
- **An alternative current mirror exhibiting a high output impedance.**
- **Small signal: If we choose $g_{m3}g_{m1}/g_{m2} \approx r_{O1}^{-1}$ the net change in ID1 is small.**
- **Figure b for large signal.**
- **The above circuit does pose its own voltage headroom limitation: V_X must exceed V_{TH3}.**

Active Current Mirrors



- A five-transistor “operational transconductance amplifier” (OTA).
- Note that the output is single-ended, hence the circuit is sometimes used to convert differential signals to a single-ended output.

Quick Calculation

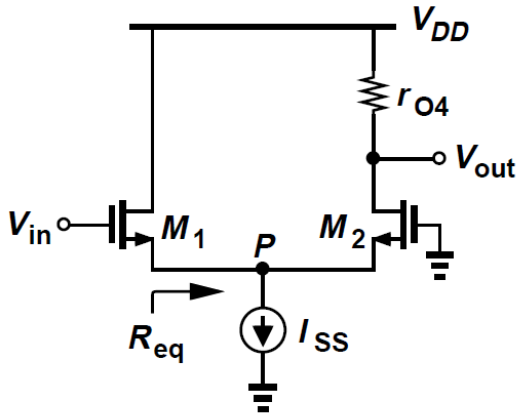


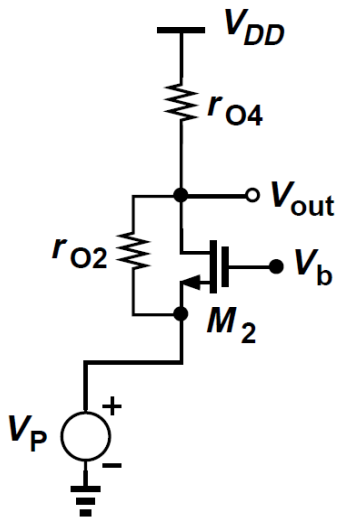
- **We may simply discard one output of a differential pair as shown in Fig.**
- **What is the small-signal gain?**

$$|A_v| = G_m R_{out}$$

$$|A_v| = \frac{g_{m1}}{2}[(2r_{O2})||r_{O4}].$$

Second Approach





- **We calculate V_p /V_{in} and V_{out}/V_p**

$$\frac{V_P}{V_{in}} = \frac{R_{eq}||r_{O1}}{R_{eq}||r_{O1} + \dfrac{1}{g_{m1}}}$$

$$R_{eq} = \frac{r_{O2} + r_{O4}}{1 + g_{m2}r_{O2}}$$

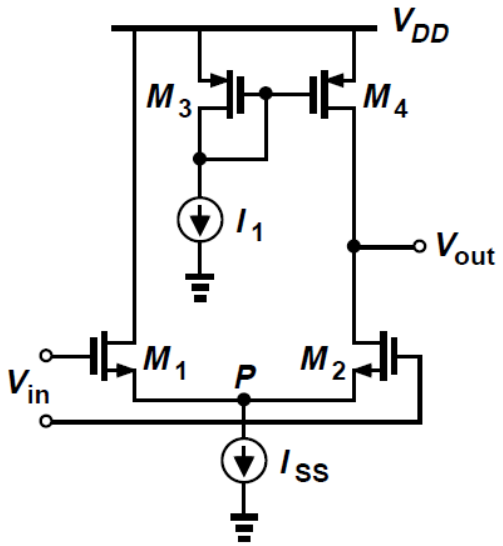
$$\frac{V_P}{V_{in}} = \frac{g_{m1}r_{O1}(r_{O2} + r_{O4})}{(1 + g_{m1}r_{O1})(r_{O2} + r_{O4}) + (1 + g_{m2}r_{O2})r_{O1}}$$

- **Caculate V_{out}/V_p**

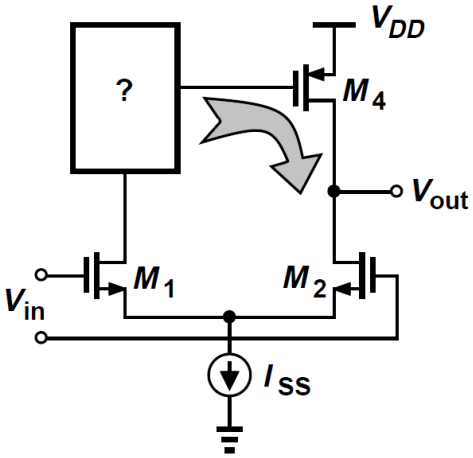
$$\frac{V_{out}}{V_P} = \frac{(1 + g_{m2}r_{O2})r_{O4}}{r_{O2} + r_{O4}}.$$

$$\frac{V_{out}}{V_{in}} = \frac{g_{m2}r_{O2}r_{O4}}{2r_{O2} + r_{O4}} = \frac{g_{m2}}{2}[(2r_{O2})||r_{O4}]$$

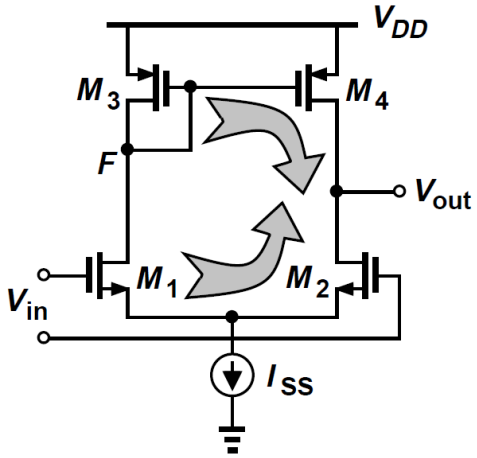
Differential Pair with Active Load



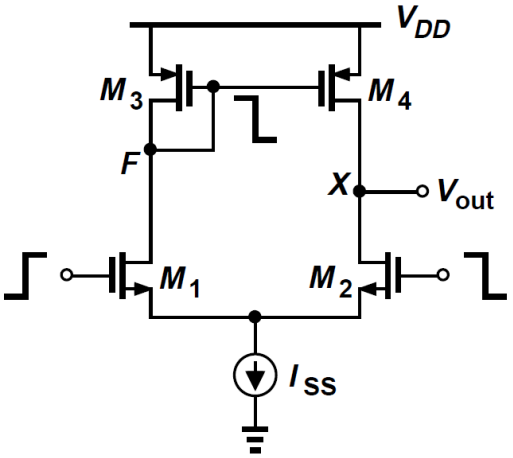
- The small-signal draincurrent of M1 is “wasted.”
- It is desirable to utilize this current with proper polarity at the output.
- This can be accomplished by the five-transistor OTA.
- M3 enhances the gain.
- The five-transistor OTA is also called a differential pair with active load.



(a)

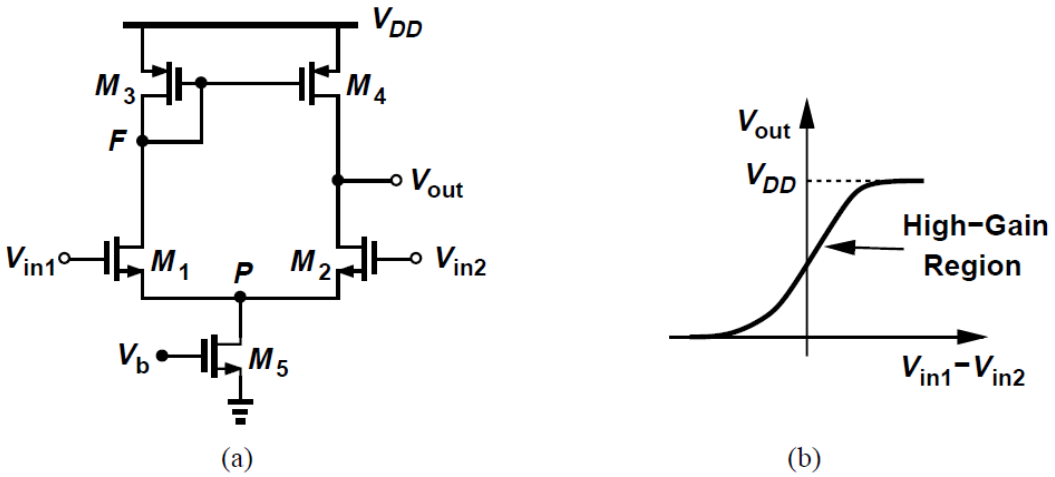


(b)



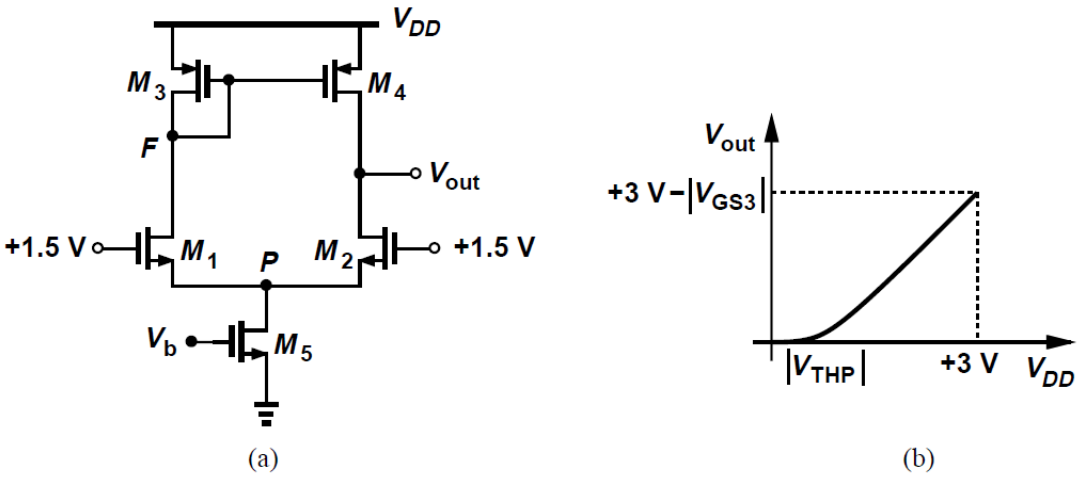
(c)

Large-Signal Analysis



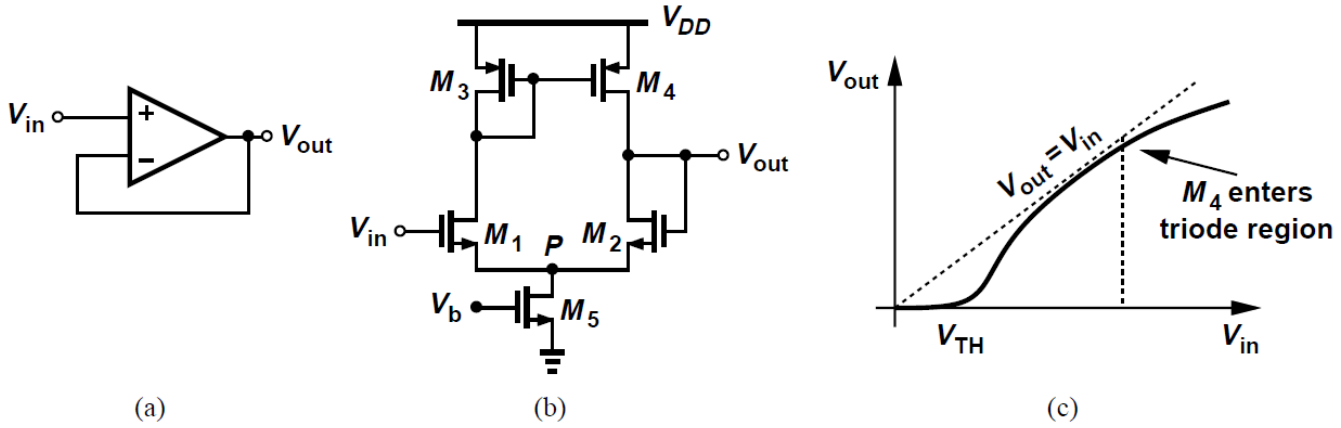
- If Vin1 is much more negative than Vin2, Vout = 0.
- As Vin1 approaches Vin2, The output voltage then depends on the difference between I_{D4} and I_{D2}. For a small difference between V_{in1} and V_{in2}, both M2 and M4 are saturated, providing a high gain.
- As Vin1 becomes more positive than V_{in2}, allowing Vout to rise and eventually driving M4 into the triode region .

Example



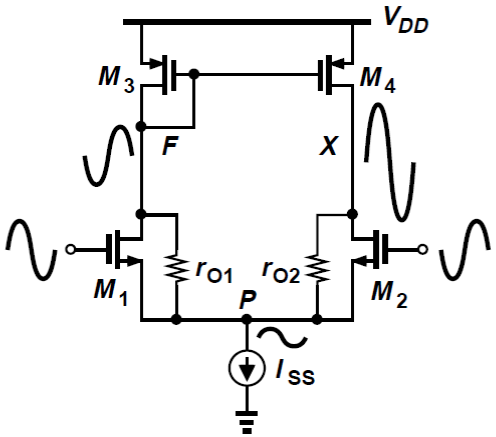
- **For VDD = 3 V, symmetry requires that $V_{out} = V_F$.**
- **As VF and Vout fall below +1:5 V -V_{TH}, M1 and M2 enter the triode region, but their drain currents are constant if M5 is saturated.**
- **Eventually M5 into the triode region. Thereafter, the bias current of all of the transistors drops, lowering the rate at which V_{out} decreases.**

Example



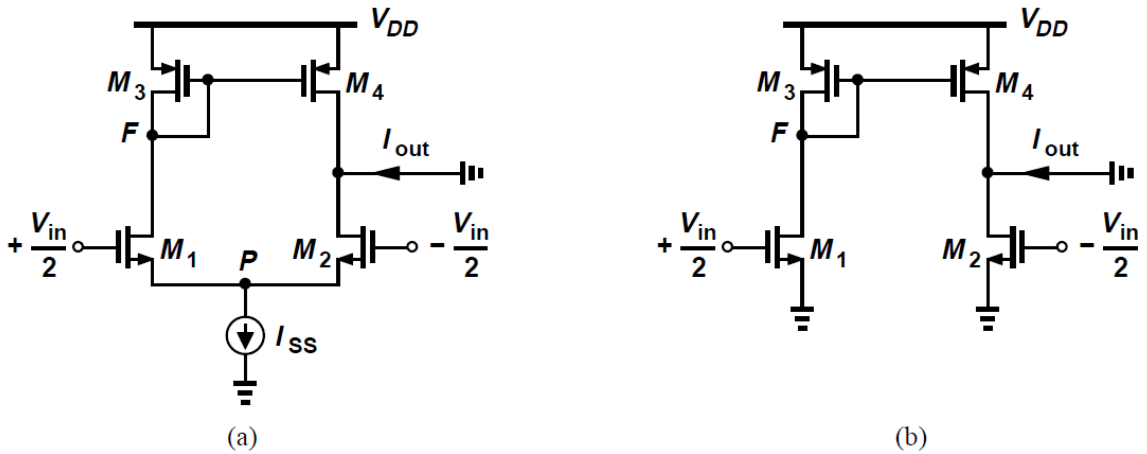
- **Sketch the large-signal input-output characteristic of the unity-gain buffer shown in Fig if the op amp is realized as a five-transistor OTA.**
- **We begin with $V_{in} = 0$ and note that M1,M3, and M4 are off.**
- **As Vin rises, $V_{out} \approx V_{in}$. This unity-gain action continues as V_{in} increases.**
- **For a sufficiently high Vin: M1 and M4 went to triode region.**

Small-Signal Analysis



- **With small differential inputs, the voltage swings at nodes F and X are vastly different.**
- **The effects of V_F and V_X at node P (through r_{O1} and r_{O2}, respectively) do not cancel each other and this node cannot be considered a virtual ground.**

Approximate Analysis



- **Node P can be approximated by a virtual ground.**

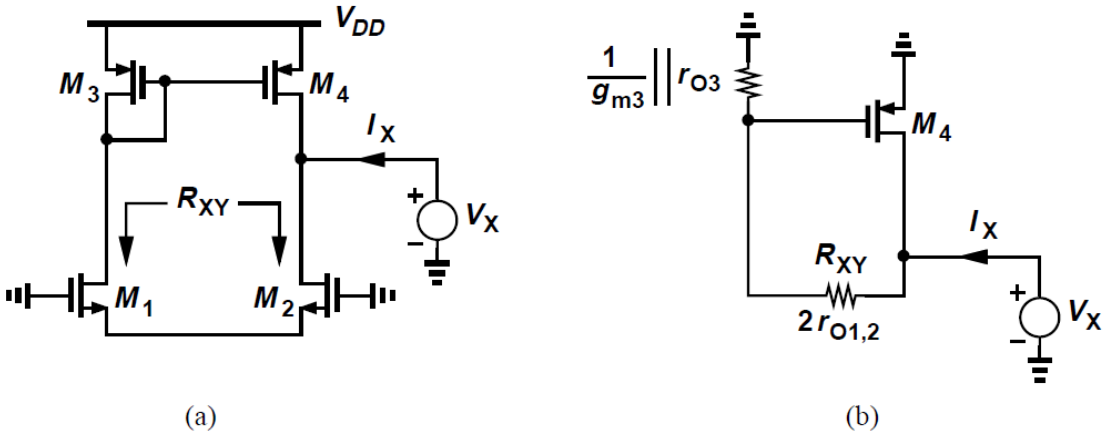
$$I_{D1} = |I_{D3}| = |I_{D4}| = g_{m1,2}V_{in}/2$$

$$I_{D2} = -g_{m1,2}V_{in}/2$$

$$I_{out} = -g_{m1,2}V_{in}$$

$$|G_m| = g_{m1,2}$$

Calculation of Rout



- **Any current flowing intoM1 must flow out of M2, and the role of the two transistors can be represented by a resistor** $R_{XY} = 2r_{O1,2}$
- **The current drawn from V_X by R_{XY} is mirrored byM3 ontoM4 with unity gain.**

$$I_X = \frac{V_X}{2r_{O1,2} + \frac{1}{g_{m3}} || r_{O3}} \left[1 + \left(\frac{1}{g_{m3}} || r_{O3}\right) g_{m4}\right] + \frac{V_X}{r_{O4}}$$

- **For** $2r_{O1,2} \gg (1/g_{m3}) || r_{O3}$

$$R_{out} \approx r_{O2} || r_{O4}$$

Exact Analysis

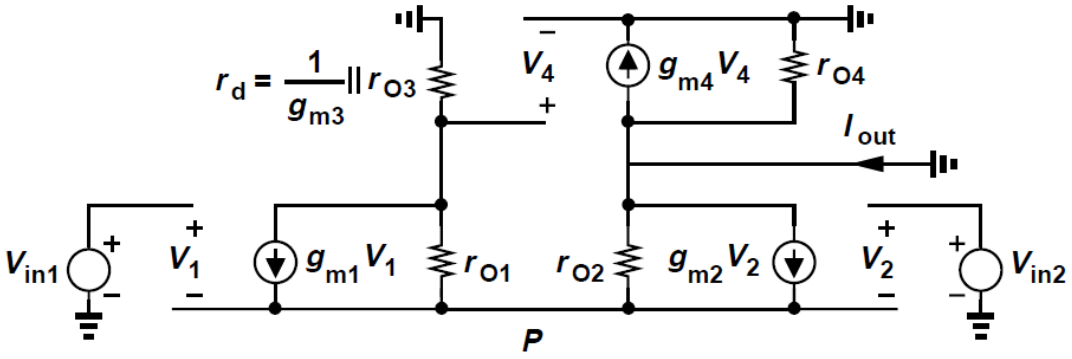


Figure 5.34. Equivalent circuit of five-transistor OTA

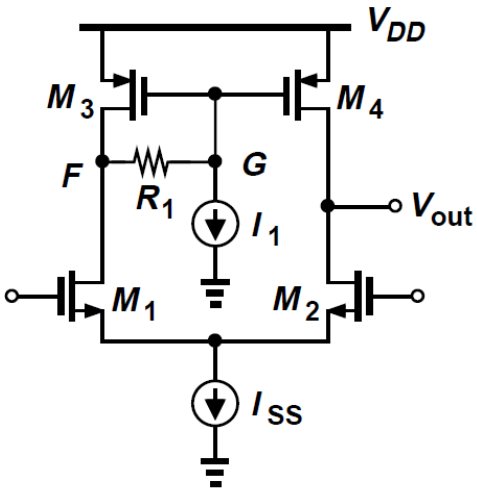
$$G_m R_{out} = -g_{m1} r_{O1} r_{O4} \frac{2g_{m3} r_{O3} + 1}{(2g_{m3} r_{O3} + 1) r_{O4} + 2r_{O1}(1 + g_{m3} r_{O3}) + r_{O3}}$$

$$= -\frac{g_{m1} r_{O1} r_{O4}}{r_{O1} + r_{O3}} \cdot \frac{2g_{m3} r_{O3} + 1}{2(g_{m3} r_{O3} + 1)}.$$

$$|A_v| = g_{m1}(r_{O1} || r_{O4}) \frac{2g_{m4} r_{O4} + 1}{2(g_{m4} r_{O4} + 1)}$$

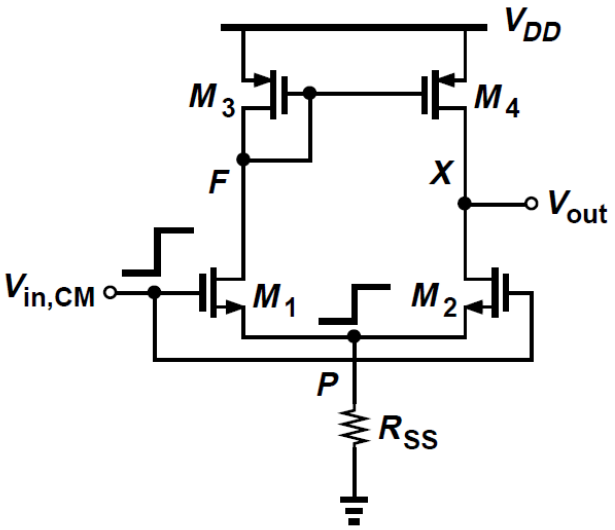
- **We can viewthis result as our approximate solution, $g_{m1}(r_{O1} || r_{O4})$. multiplied by a "correction" factor that is less than unity.**

Headroom Issues



- The five-transistor OTA does not easily lend itself to low-voltage operation.
- The value of I1 must be much less than Iss/2.
- Insert a resistor in series with the gate and draw a constant current from it.

Common-Mode Properties

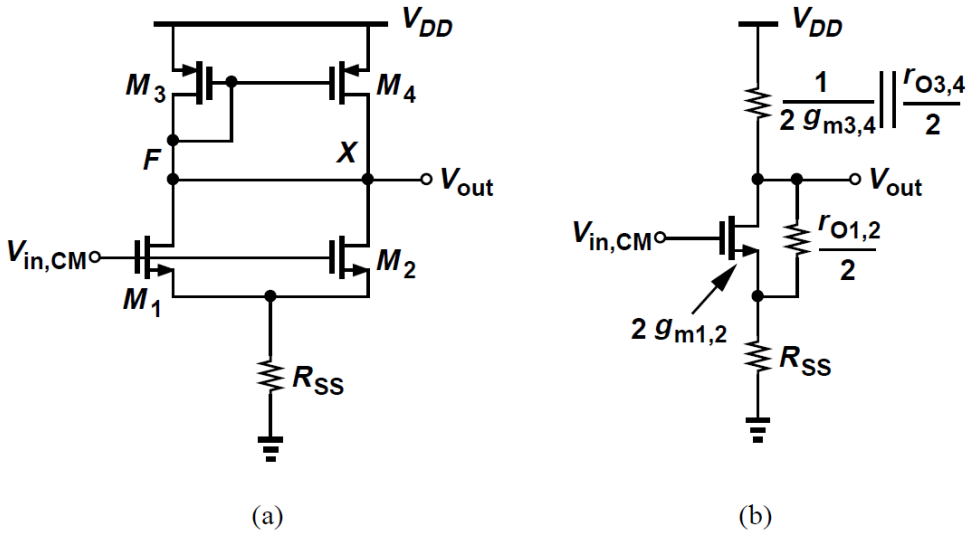


$$A_{CM} = \frac{\Delta V_{out}}{\Delta V_{in,CM}}.$$

$$A_{CM} \approx \frac{-\dfrac{1}{2g_{m3,4}} \Big\| \dfrac{r_{O3,4}}{2}}{\dfrac{1}{2g_{m1,2}} + R_{SS}}$$

$$= \frac{-1}{1 + 2g_{m1,2}R_{SS}} \frac{g_{m1,2}}{g_{m3,4}}$$

CMRR



(a) Simplified circuit of Fig. 5.37, (b) equivalent circuit of (a).

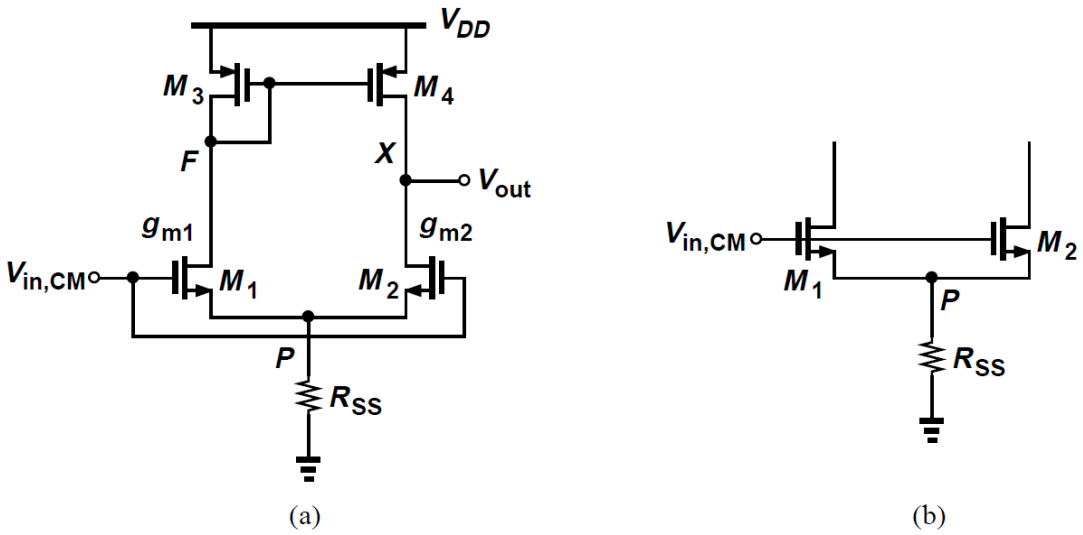
$$CMRR = \left|\frac{A_{DM}}{A_{CM}}\right|$$

$$= g_{m1,2}(r_{O1,2}\|r_{O3,4})\frac{g_{m3,4}(1+2g_{m1,2}R_{SS})}{g_{m1,2}}$$

$$= (1+2g_{m1,2}R_{SS})g_{m3,4}(r_{O1,2}\|r_{O3,4}).$$

- **Even with perfect symmetry, the output signal is corrupted by input CM variations.**

Effect of Mismatches

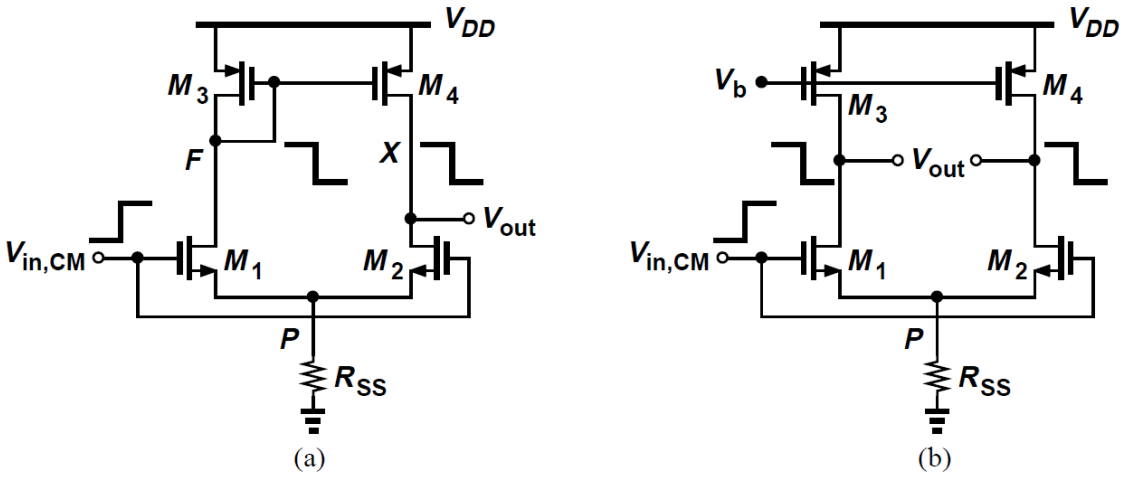


- we consider the case where the input transistors exhibit slightly different transconductances 。
- How does Vout depend on Vincm?

$$\frac{\Delta V_{out}}{\Delta V_{in,CM}} \approx \frac{(g_{m1} - g_{m2})r_{O3} - g_{m2}/g_{m3}}{1 + (g_{m1} + g_{m2})R_{SS}}.$$

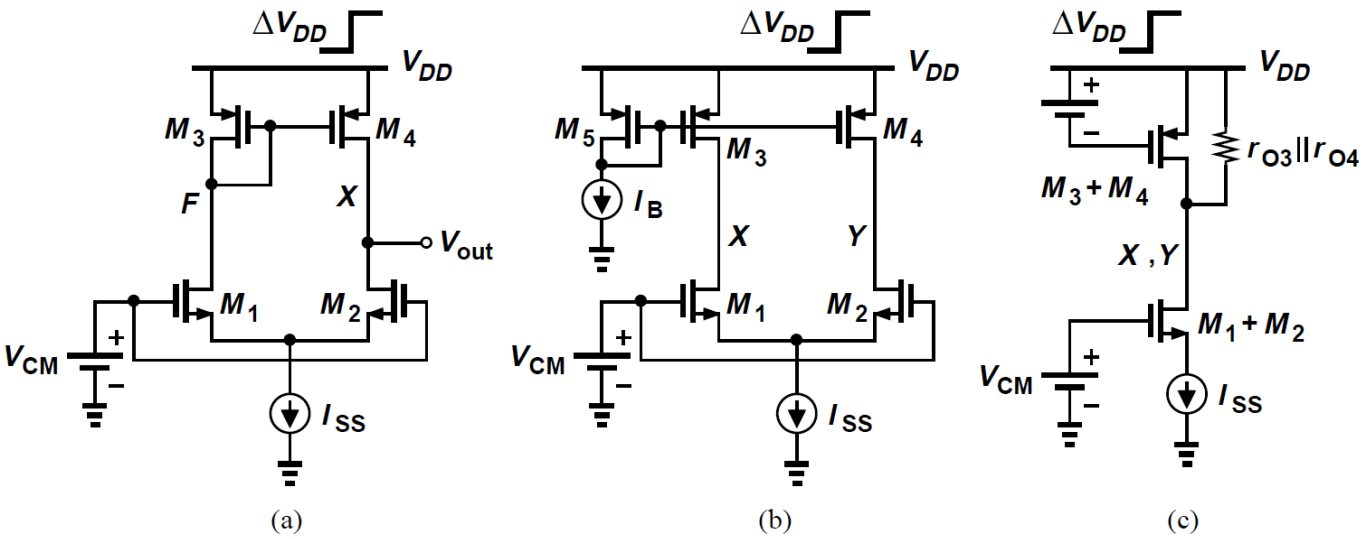
- This result contains the additional term $(g_{m1} - g_{m2})r_{O3}$

Other Properties



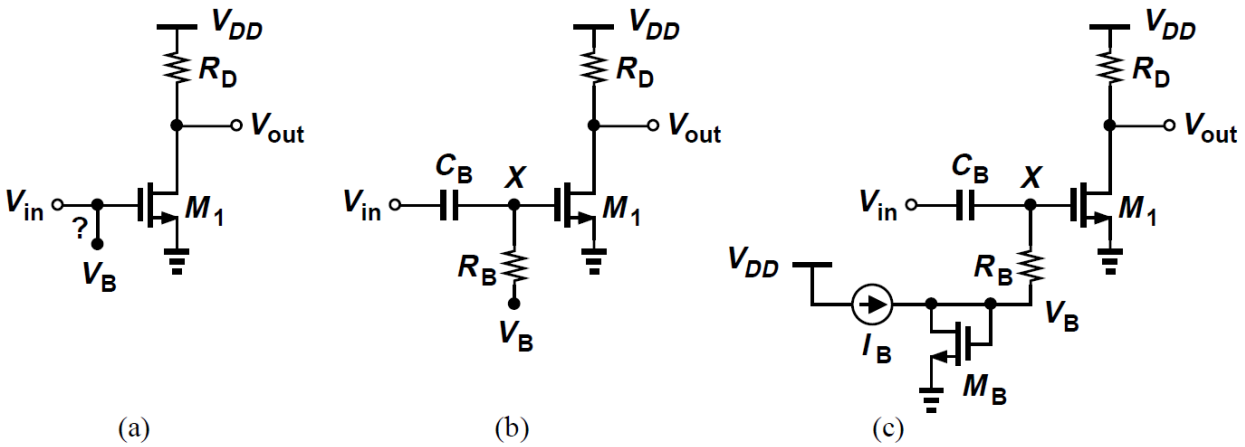
- **A finite CMRR even with perfectly matched transistors.**
- **The supply rejection of this OTA is inferior.**
- **Change V_{DD} by a small amount, how much does V_F change?**

Other Properties



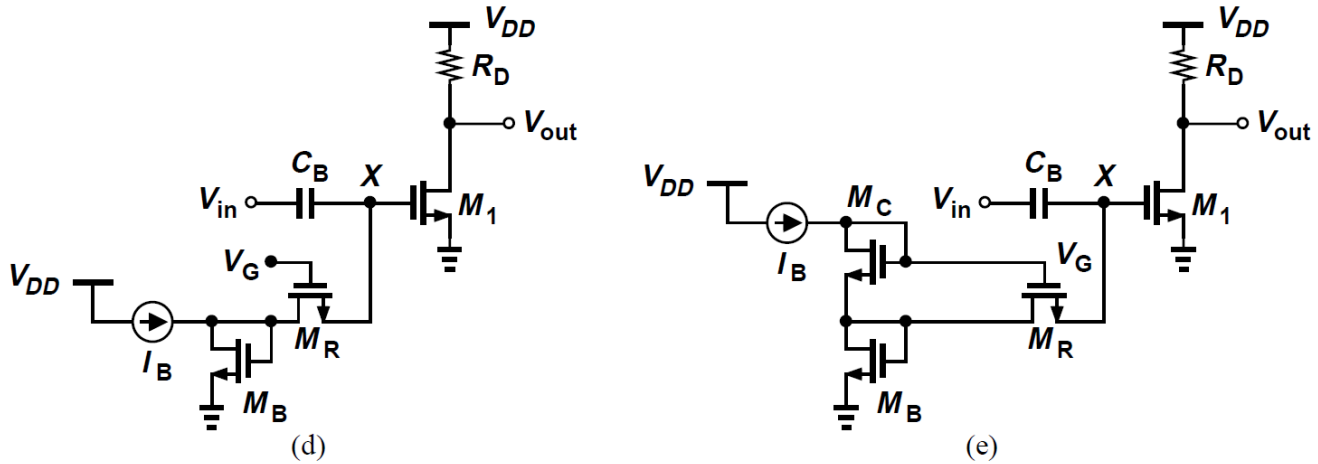
- For (a), The gain from V_{DD} to Vout is about unity.
- Now consider the fully-differential topology in Fig(b).
- In this case, too, the output voltages change by ΔV_{DD} but their difference remains intact.
- This circuit requires common-mode feedback.

Biasing Techniques



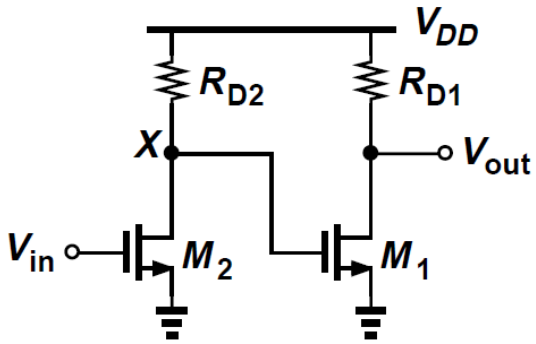
- **Simple CS Stage**
- **How do we ensure that V_B does not "fight" Vin?**
- **Couple V_{in} capacitively and establish a high impedance for V_B.**
- **Node X in Fig (b) must have a dc path to a voltage.**
- **The bias voltage must be generated by a diode-connected device**
- **Typically select I_B about one-tenth to one-fifth of I_{D1} so as to minimize the power.**

Biasing Using a MOSFET



- The capacitor and the resistor may occupy a large chip area.
- The capacitor introduces its own parasitics.
- In applications requiring a large RC product, one can replace R_B with a long, narrow MOSFET.
- But how do we guarantee that MR does not turn off?
- The overdrive of M_R must be well controlled. This difference can be created by means of a diode-connected device.

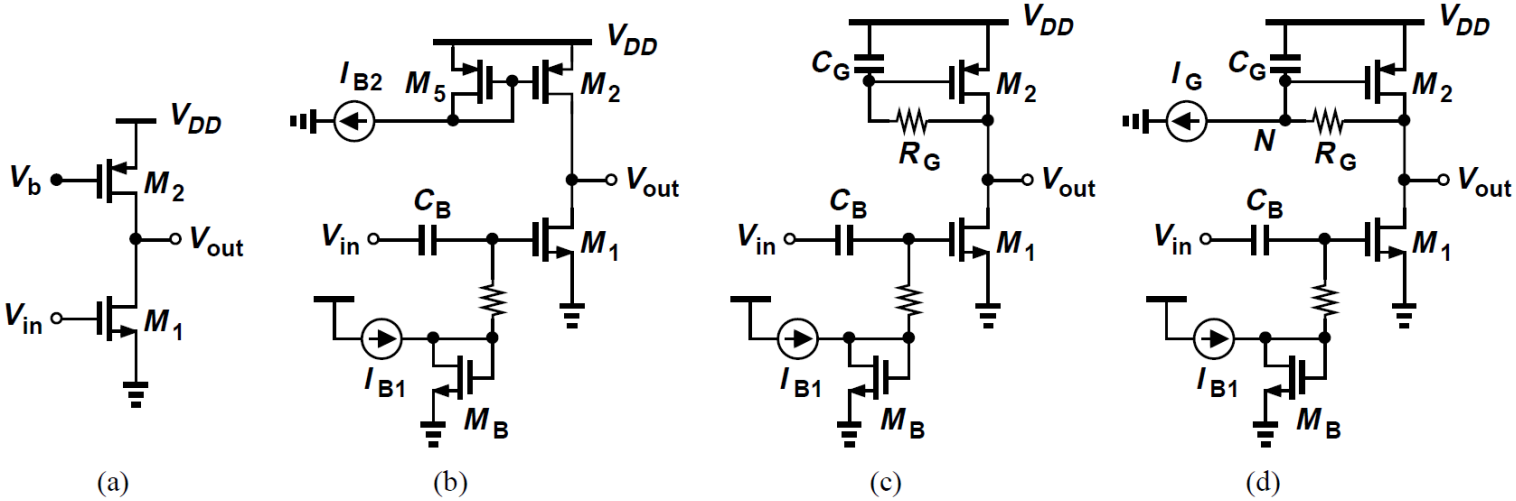
Direct Coupling



Direct coupling between two stages.

- **Possible to remove the input coupling capacitor and provide the bias voltage from the preceding stage?**
- **The bias conditions of M1 are influenced by those of M2.**
- **The PVT variations are amplified.**
- **One can employ direct coupling between two stages if each has a low gain.**

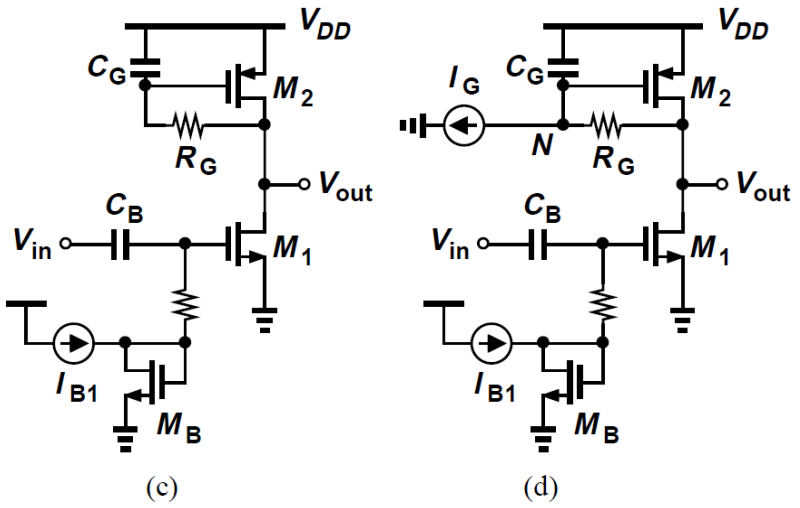
CS Stage with Current-Source Load



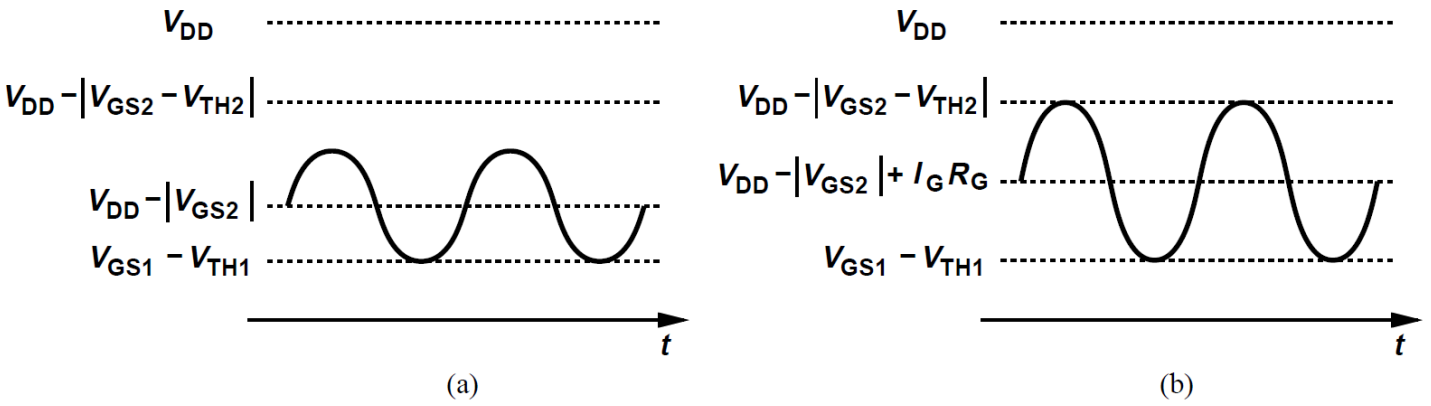
- **If the copied currents in Fig (b) are not exactly equal, each transistor wants to impose its own current.**
- **To resolve this issue, we modify the circuit as shown in Fig (c).**

- **Select** $A_v = -g_{m1}(r_{O1}||r_{O2}||R_G)$
- **We can** $R_G \gg r_{O1}||r_{O2}$ **stant current of I_G from R_G, so that Vout is higher.**

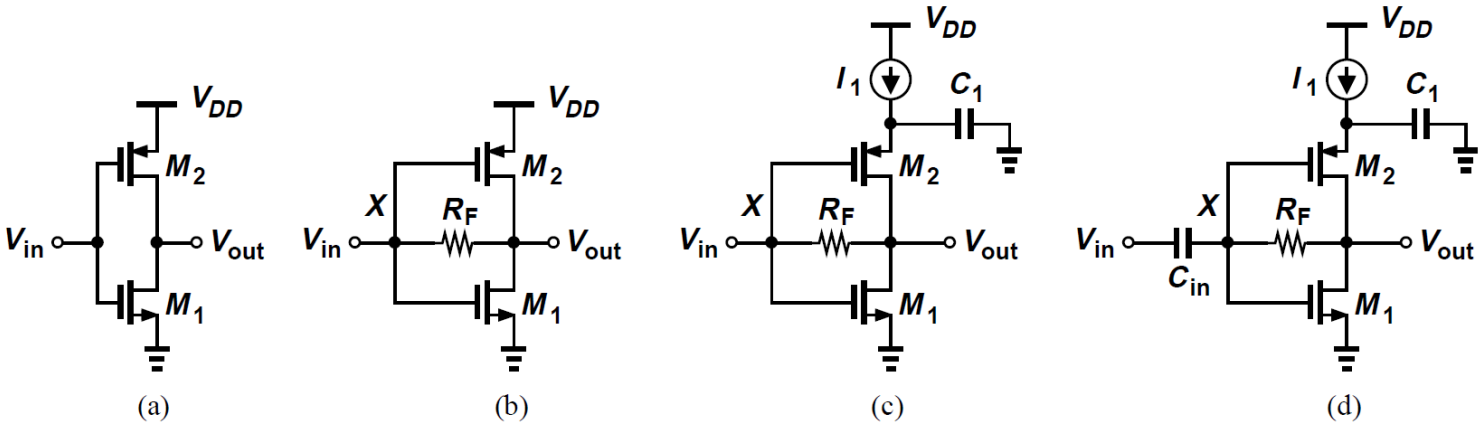
Example



- **Compare the maximum allowable voltage swings.**
- **In Fig (c), the up-swing cannot reach its maximum.**
- **In Fig. 5.45(d), on the other hand, $I_G R_G$ can shift the operating point such that the down-swing and the up-swing are approximately equal.**

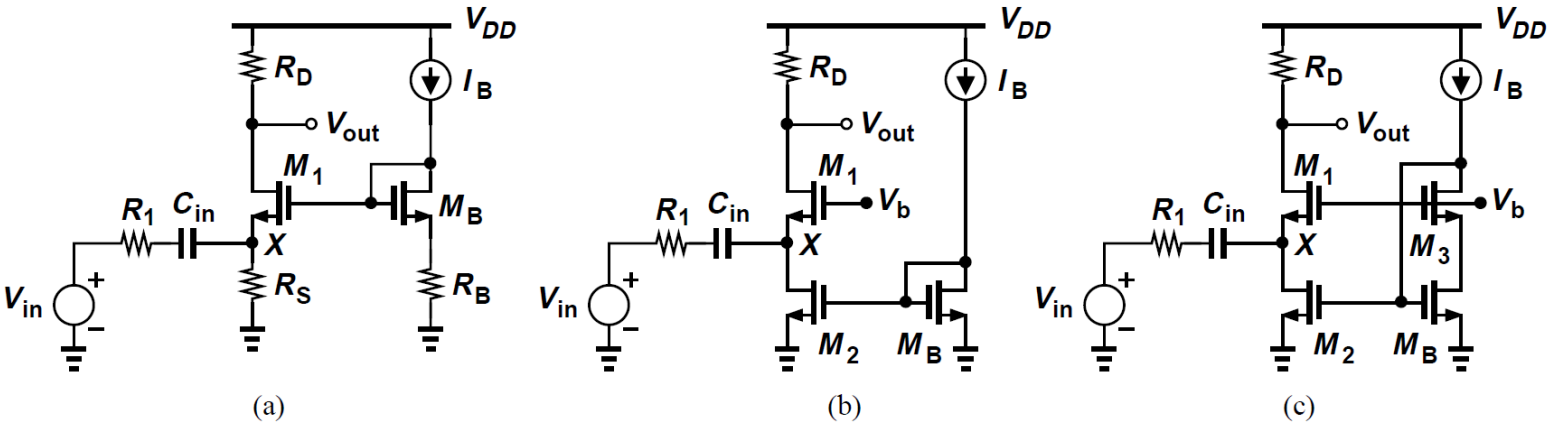


Complementary CS Stage



- **Shown in Fig. (b), each transistor is configured as a diode-connect device and guaranteed to operate in saturation.**
- **Self-biased topology.**
- **To define the bias current accurately, we modify the circuit as shown in Fig. (c).**
- **Since the bias voltage at node X must track Vout, the input must be capacitively coupled.**

CG Biasing

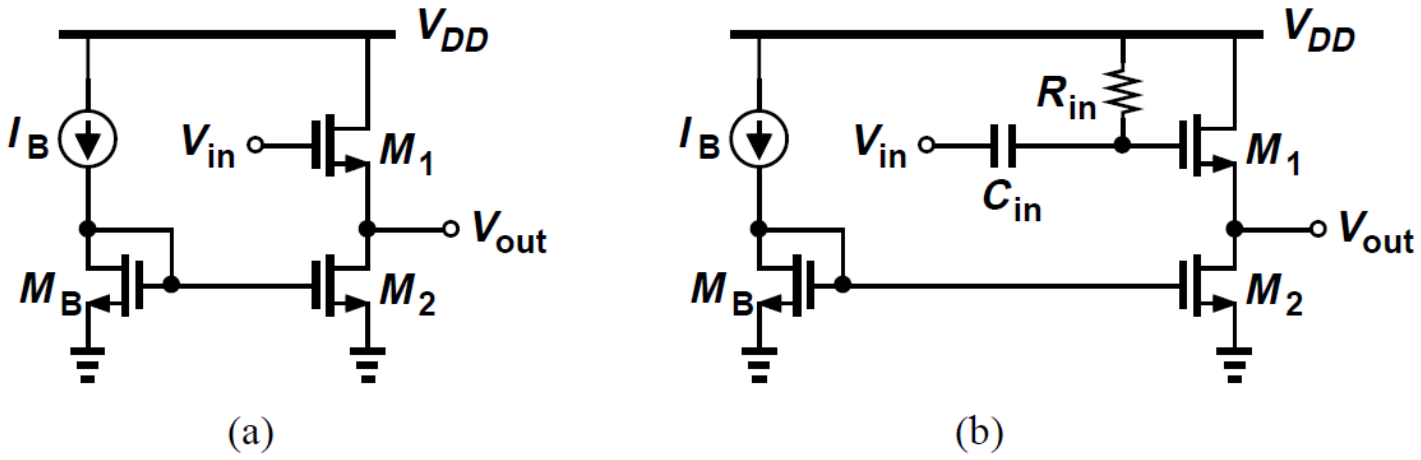


- **The circuit of Fig. (a) faces difficulties in low-voltage design.**

$$\frac{V_X}{V_{in}} = \frac{\dfrac{1}{g_{m1}+g_{mb1}} || R_S}{\dfrac{1}{g_{m1}+g_{mb1}} || R_S + R_1}$$

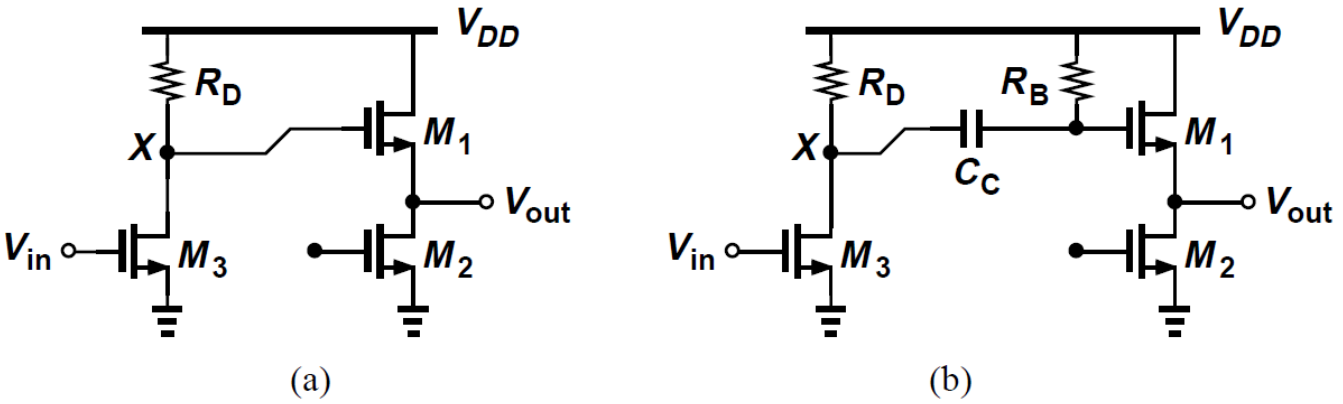
- **RS may reach or even exceed RD.**
- **Replace RS with a current source.**

Source Follower Biasing



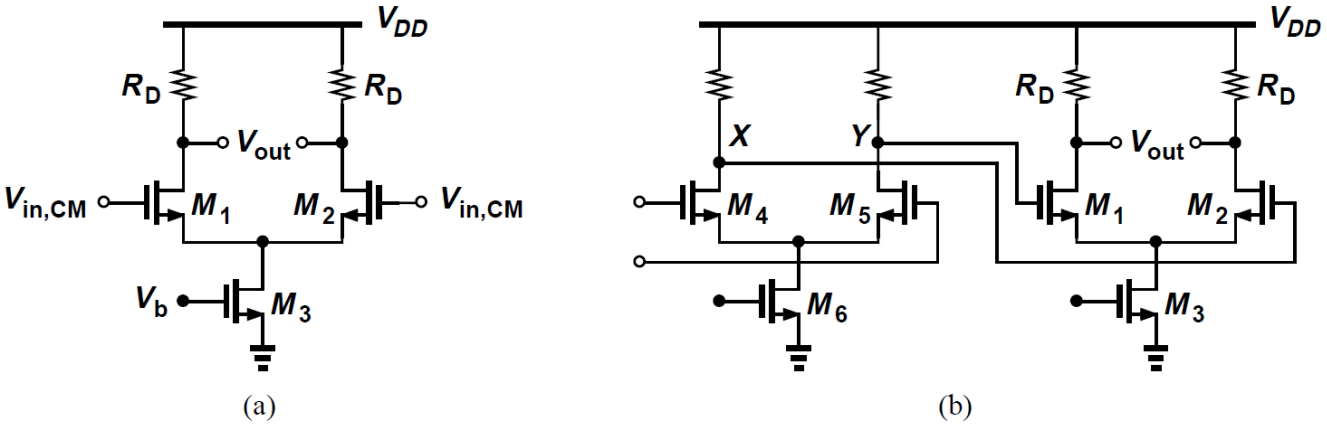
- **In applications where the input dc voltage may vary considerably, capacitive coupling can be used.**
- **Study the performance with and without capacitive coupling between the two stages.**

Use of SF



- **In Fig (a), the minimum drain voltage of M3 is given by $V_{GS1} + V_{DS2min}$, leaving little for the allowable voltage drop across R_D.**
- **Fig (b), on the other hand, the first stage's gain can be independently maximized.**

Differential Pair Biasing



- **Since the bias currents of M1 and M2 in Fig. (a) are relatively insensitive to their gate voltages, we can directly connect their gates to the preceding stage.**
- **If the bias value of VX and VY is chosen equal to two overdrives above ground, then it is an excessively low common-mode level for the second stage.**
- **May resort to capacitive coupling in some cases.**