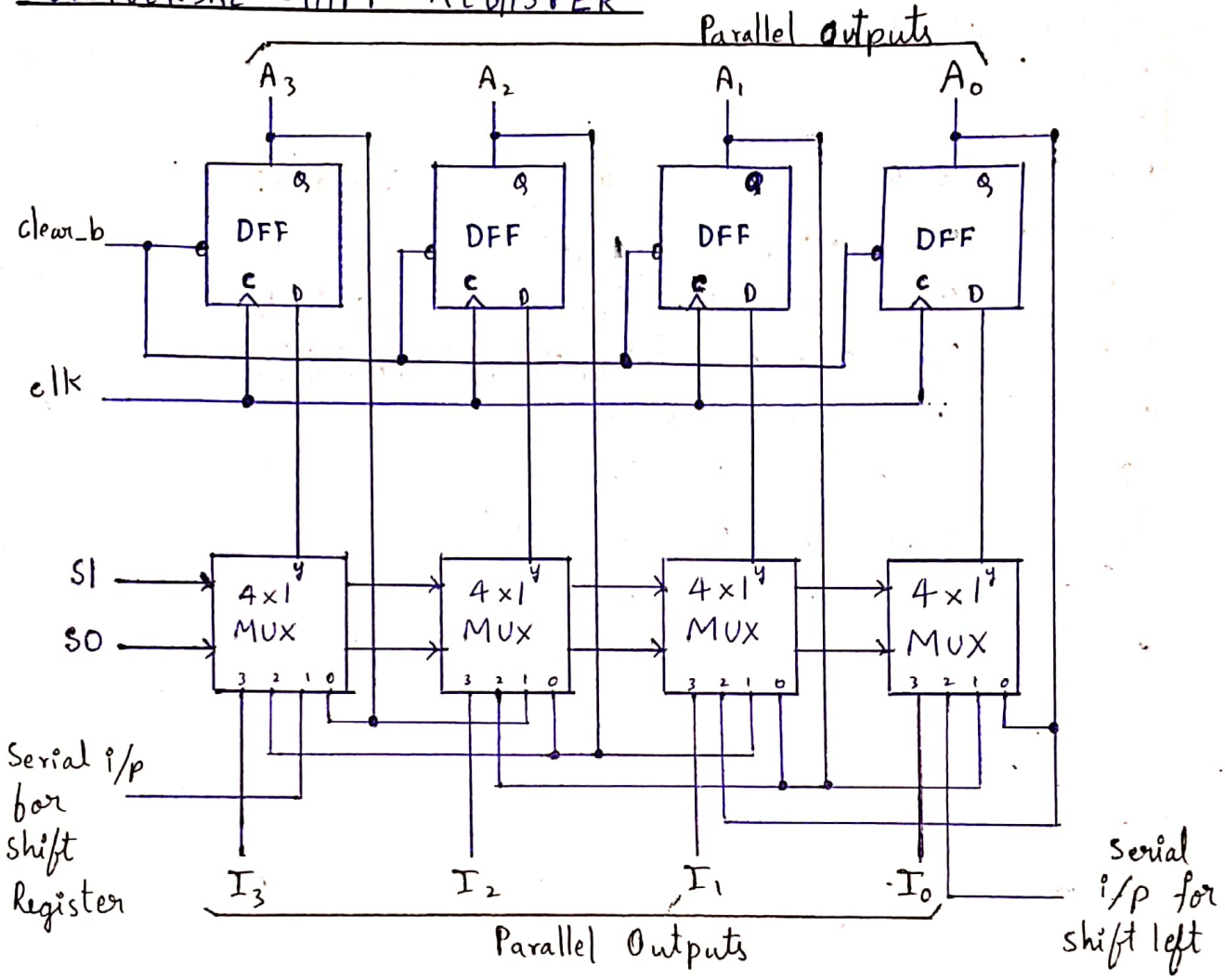
BHARADWAJ. D
PES2201800626
ECE-B
3rd SEM

HDL-ASSIGNMENT

UNIVERSAL SHIFT REGISTER



Design Code [D-Flip Flop]

dff.v

```
module dff (d, clk, rst, q);
input d, clk, rst;
output q; reg q;
always@ (posedge clk)
  if (rst == 1'b1)
     q <= 1'b0;
  else
     q <= d;
endmodule.
```

4:1 MUX Design Code.

mux41.v

```
module mux41(i0, i1, i2, i3, s0, s1, y)
input i0, i1, i2, i3, s0, s1;
output y; reg y;
always@ (s0, s1, i0, i1, i2 i3)
begin
   if (s0 == 0 & s1 == 0)
        y = i0;
   else if (s0 == 0 & s1 == 1)
        y = i1;
   else if (s0 == 1 & s1 == 0)
        y = i2;
   else if (s0 == 1 & s1 == 1)
        y = i3;
end
endmodule.
```

(2)

Universal Shift Register Design Code :-

```
module USR(rst,clk, i,o, sinsr, sinsl);
input [3:0]i;
input [1:0]s;
input rst, clk, sinsr, sinsl;
output [3:0]o;
wire [3:0]w;
mux41 m1(o[0], o[1], sinsl, i[0], s[0], s[1], w[0]);
mux41 m2(o[1], o[2], o[0], i[1], s[0], s[1], w[1]);
mux41 m3(o[2], o[3], o[1], i[2], s[0], s[1], w[2]);
mux41 m4(o[3], sinsr, o[2], i[3], s[0], s[1], w[3]);
dff d1(w[0], clk, rst, o[0]);
dff d2(w[1], clk, rst, o[1]);
dff d3(w[2], clk, rst, o[2]);
dff d4(w[3], clk, rst, o[3]);
endmodule.
```