CHAPTER

5

Current Mirrors and Biasing Techniques

Our study of single-stage and differential amplifiers in Chapters 3 and 4 points to the wide usage of current sources. In these circuits, current sources act as a large resistor without consuming excessive voltage headroom. We also noted that MOS devices operating in saturation can act as a current source.

Current sources find other applications in analog design as well. For example, some digital-to-analog (D/A) converters employ an array of current sources to produce an analog output proportional to the digital input. Also, current sources, in conjunction with "current mirrors," can perform useful functions on analog signals.

This chapter deals with the design of current mirrors and bias circuits. Following a review of basic current mirrors, we study the cascode mirror. Next, we analyze active current mirrors and describe the properties of differential pairs using such circuits as loads. Finally, we introduce various biasing techniques for amplifier stages.

5.1 ■ Basic Current Mirrors

Figure 5.1 illustrates two examples in which a current source proves useful. From our study in Chapter 2, recall that the output resistance and capacitance and the voltage headroom of a current source trade with the magnitude of the output current. In addition to these issues, several other aspects of current sources are important: supply, process, and temperature dependence; output noise current; and matching with other current sources. We defer the noise and matching considerations to Chapters 7 and 14, respectively.

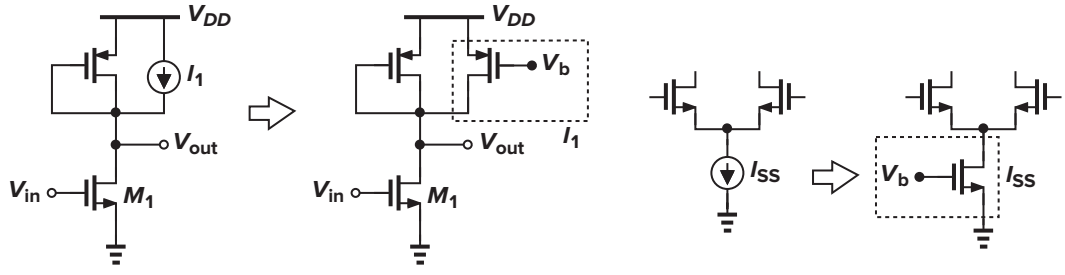


Figure 5.1 Applications of current sources.

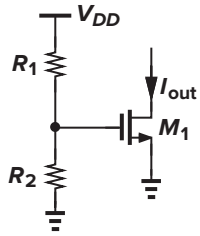


Figure 5.2 Definition of current by resistive divider.

How should a MOSFET be biased so as to operate as a stable current source? To gain a better view of the issues, let us consider the simple resistive biasing shown in Fig. 5.2. Assuming M_1 is in saturation, we can write

$$I_{out} \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1+R_2}V_{DD} - V_{TH}\right)^2 \tag{5.1}$$

This expression reveals various PVT dependencies of I_{out}. The overdrive voltage is a function of V_{DD} and V_{TH}; the threshold voltage may vary by 50 to 100 mV from wafer to wafer. Furthermore, both μ_n and V_{TH} exhibit temperature dependence. Thus, I_{out} is poorly defined. The issue becomes more severe as the device is biased with a smaller overdrive voltage, e.g., to consume less headroom and support greater voltage swings at the drain. With a nominal overdrive of, say, 200 mV, a 50-mV error in V_{TH} results in a 44% error in the output current.

It is important to note that process and temperature dependencies exist even if the gate voltage is not a function of the supply voltage. In other words, if the gate-source *voltage* of a MOSFET is precisely defined, then its drain *current* is not! For this reason, we must seek other methods of biasing MOS current sources.

The design of current sources in analog circuits is based on "copying" currents from a reference, with the assumption that *one* precisely-defined current source is already available. While this method may appear to entail an endless loop, it is carried out as illustrated in Fig. 5.3. A relatively complex circuit—sometimes requiring external adjustments—is used to generate a stable reference current, I_{REF}, which is then "cloned" to create many current sources in the system. We study the copying operation here and the reference generator (which is based on "bandgap" techniques) in Chapter 12.

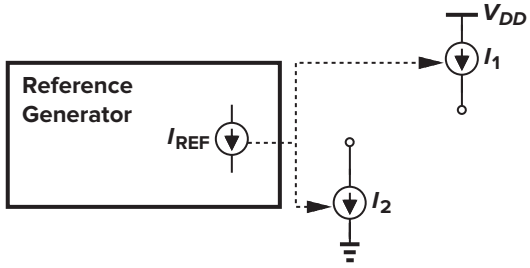


Figure 5.3 Use of a reference to generate various currents.

How do we generate copies of a reference current? For example, in Fig. 5.4, how do we guarantee that $I_{out} = I_{REF}$? For a MOSFET, if $I_D = f(V_{GS})$, where $f(\cdot)$ denotes the dependence of I_D upon V_{GS}, then $V_{GS} = f^{-1}(I_D)$. That is, if a transistor is biased at I_{REF}, then it produces $V_{GS} = f^{-1}(I_{REF})$ [Fig. 5.5(a)]. Thus, if this voltage is applied to the gate and source terminals of a second MOSFET, the resulting current is $I_{out} = f[f^{-1}(I_{REF})] = I_{REF}$ [Fig. 5.5(b)]. From another point of view, two identical MOS devices that have equal gate-source voltages and operate in saturation carry equal currents (if $\lambda = 0$).

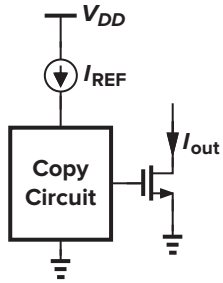


Figure 5.4 Conceptual means of copying currents.

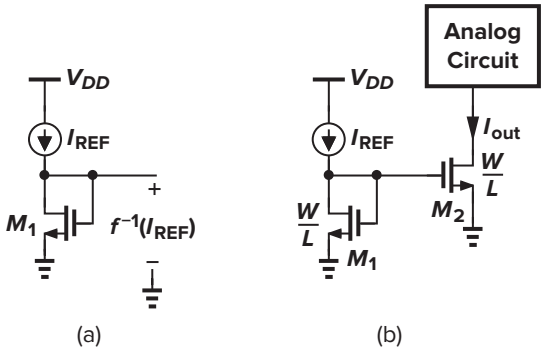


Figure 5.5 (a) Diode-connected device providing inverse function; (b) basic current mirror.

The structure consisting of M_1 and M_2 in Fig. 5.5(b) is called a "current mirror." In the general case, the transistors need not be identical. Neglecting channel-length modulation, we can write

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2 \tag{5.2}$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2 \tag{5.3}$$

obtaining

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF} \tag{5.4}$$

The key property of this topology is that it allows precise copying of the current with no dependence on process and temperature. The translation from I_{REF} to I_{out} merely involves the *ratio* of device dimensions, a quantity that can be controlled with reasonable accuracy.

It is important to appreciate the cause-and-effect relationships stipulated by $V_{GS} = f^{-1}(I_{REF})$ and $f[f^{-1}(I_{REF})] = I_{REF}$. The former suggests that we must *generate* a V_{GS} *from* I_{REF}; i.e., I_{REF} is the cause and V_{GS} is the effect. A MOSFET can perform this function only if it is configured as a diode while carrying a current of I_{REF} [M_1 in Fig. 5.5(b)]. Similarly, the latter equation indicates that a transistor must sense $f^{-1}(I_{REF})$ ($= V_{GS}$) and generate $f[f^{-1}(I_{REF})]$. In this case, the cause is V_{GS} and the effect is the output current, $f[f^{-1}(I_{REF})]$ [as provided by M_2 in Fig. 5.5(b)].

With the aid of these observations, we can understand why a circuit such as that in Fig. 5.6 does not perform current *copying*. Here, V_b is *not* caused by I_{REF}, and hence I_{out} does not track I_{REF}.

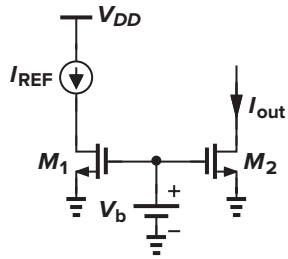


Figure 5.6 Circuit incapable of copying current.

▶ **Example 5.1**

In Fig. 5.7, find the drain current of M_4 if all of the transistors are in saturation.

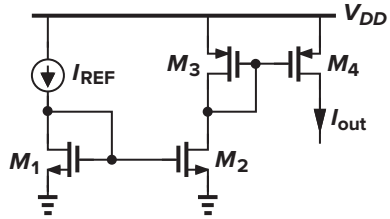


Figure 5.7

Solution

We have $I_{D2} = I_{REF}[(W/L)_2/(W/L)_1]$. Also, $|I_{D3}| = |I_{D2}|$ and $I_{D4} = I_{D3} \times [(W/L)_4/(W/L)_3]$. Thus, $|I_{D4}| = \alpha\beta I_{REF}$, where $\alpha = (W/L)_2/(W/L)_1$ and $\beta = (W/L)_4/(W/L)_3$. Proper choice of α and β can establish large or small ratios between I_{D4} and I_{REF}. For example, $\alpha = \beta = 5$ yields a magnification factor of 25. Similarly, $\alpha = \beta = 0.2$ can be utilized to generate a small, well-defined current.

◀

We should also remark that the copy of a copy may not be as "clear" as the original. Owing to random "mismatches" between M_1 and M_2 in the above example, I_{D2} slightly deviates from its nominal value. Similarly, as I_{D2} is copied onto I_{D4}, additional errors accumulate. We must therefore avoid long current mirror chains.

Current mirrors find wide application in analog circuits. Figure 5.8 illustrates a typical case, where a differential pair is biased by means of an NMOS mirror for the tail current source and a PMOS mirror

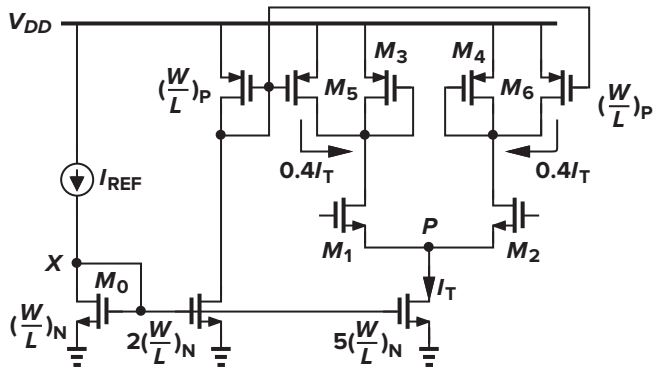


Figure 5.8 Current mirrors used to bias a differential amplifier.

for the load current sources. The device dimensions shown establish a drain current of $0.4I_T$ in M_5 and M_6, reducing the drain current of M_3 and M_4 and hence increasing the amplifier's gain.

Sizing Issues Current mirrors usually employ the same *length* for all of the transistors so as to minimize errors due to the side-diffusion of the source and drain areas (L_D). For example, in Fig. 5.8, the NMOS current sources must have the same channel length as M_0. This is because if L_{drawn} is, say, doubled, then $L_{eff} = L_{drawn} - 2L_D$ is not. Furthermore, the threshold voltage of short-channel devices exhibits some dependence on the channel length (Chapter 17). Thus, current ratioing is achieved by scaling only the width of the transistors.

Suppose we wish to copy a reference current, I_{REF}, and generate $2I_{REF}$. We begin with a width of W_{REF} for the diode-connected reference transistor and hence choose $2W_{REF}$ for the current source [Fig. 5.9(a)]. Unfortunately, direct scaling of the width also faces difficulties. As illustrated in Fig. 5.9(b), since the "corners" of the gate are poorly defined, if the drawn W is doubled, the actual width does not exactly double. We thus prefer to employ a "unit" transistor and create copies by *repeating* such a device [Fig. 5.9(c)].

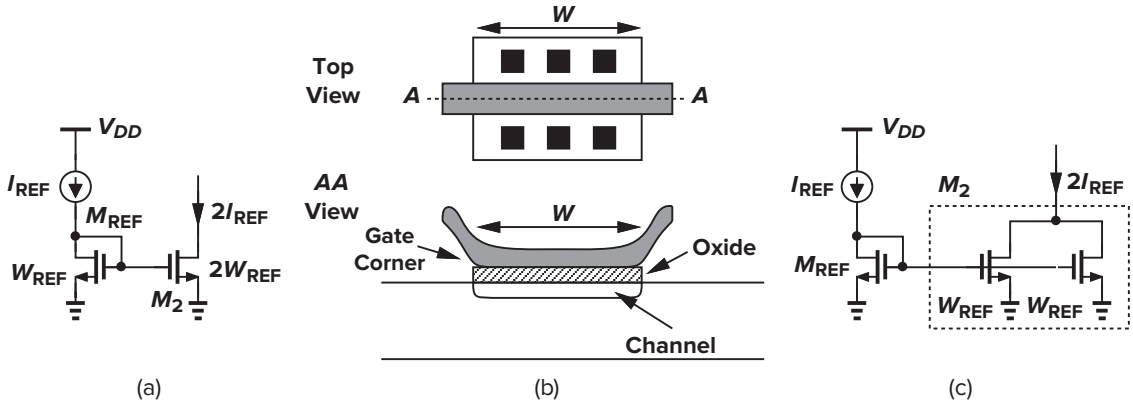


Figure 5.9 (a) Current mirror multiplying I_{REF} by 2, (b) effect of gate corner on current accuracy, and (c) more accurate current multiplication.

But how do we generate a current equal to $I_{REF}/2$ from I_{REF}? In this case, the diode-connected device itself must consist of *two* units, each carrying $I_{REF}/2$. Figure 5.10(a) depicts an example for the generation of both $2I_{REF}$ and $I_{REF}/2$; each unit has a width of W_0 (and the same length).

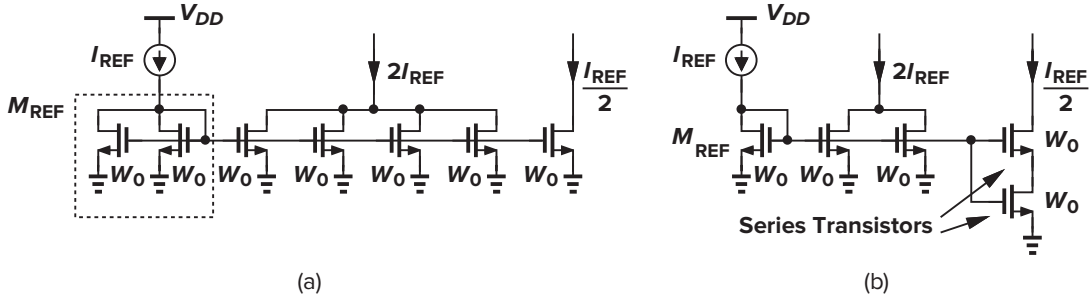


Figure 5.10 Current mirrors providing $I_{REF}/2$ from I_{REF} by (a) half-width device and (b) series transistors.

The above approach requires a large number of unit transistors if many different currents must be generated. It is possible to reduce the complexity by scaling the *lengths*, but not directly. In order to avoid the errors due to L_D, we can, for example, double the equivalent length by placing two unit

transistors *in series*. Illustrated in Fig. 5.10(b), this approach preserves an effective length of $L_{drawn}-2L_D$ for each unit, yielding an equivalent length of $2(L_{drawn}-2L_D)$ for the composite device and hence halving the current. Note that this structure is *not* a cascode because the bottom device is in the triode region (why?).

We should also mention that current mirrors can process *signals* as well. In Fig. 5.5(b), for example, if I_{REF} increases by ΔI, then I_{out} increases by $\Delta I(W/L)_2/(W/L)_1$. That is, the circuit *amplifies* the small-signal current if $(W/L)_2/(W/L)_1 > 1$ (but at the cost of proportional multiplication of the bias current).

▶ **Example 5.2**

Calculate the small-signal voltage gain of the circuit shown in Fig. 5.11.

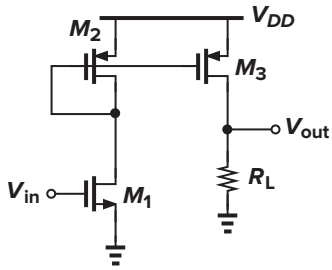


Figure 5.11

Solution

The small-signal drain current of M_1 is equal to $g_{m1}V_{in}$. Since $I_{D2} = I_{D1}$ and $I_{D3} = I_{D2}(W/L)_3/(W/L)_2$, the small-signal drain current of M_3 is equal to $g_{m1}V_{in}(W/L)_3/(W/L)_2$, yielding a voltage gain of $g_{m1}R_L(W/L)_3/(W/L)_2$.

◀

5.2 ■ Cascode Current Mirrors

In our discussion of current mirrors thus far, we have neglected channel-length modulation. In practice, this effect produces significant error in copying currents, especially if minimum-length transistors are used so as to minimize the width and hence the output capacitance of the current source. For the simple mirror of Fig. 5.5(b), we can write

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS}-V_{TH})^2(1+\lambda V_{DS1}) \tag{5.5}$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS}-V_{TH})^2(1+\lambda V_{DS2}) \tag{5.6}$$

and hence

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1}\cdot\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \tag{5.7}$$

While $V_{DS1} = V_{GS1} = V_{GS2}$, V_{DS2} may not equal V_{GS2} because of the circuitry fed by M_2. For example, in Fig. 5.8, the potential at node P is determined by the input common-mode level and the gate-source voltage of M_1 and M_2, and it may not equal V_X.

In order to suppress the effect of channel-length modulation in Fig. 5.5(b), we can (1) force V_{DS2} to be equal to V_{DS1}, or (2) force V_{DS1} to be equal to V_{DS2}. These two principles lead to two different topologies.

First Approach We begin with the first principle and wish to ensure that V_{DS2} in Fig. 5.5(b) is both *constant* and equal to V_{DS1}. Recall from Chapter 3 that a cascode device can shield a current source, thereby reducing the voltage variations across it. As shown in Fig. 5.12(a), even though the analog circuit may allow V_P to vary substantially, V_Y remains relatively constant. But how do we ensure that $V_{DS2} = V_{DS1}$? We must generate V_b such that $V_b - V_{GS3} = V_{DS1}$ $(= V_{GS1})$, i.e., $V_b = V_{GS3} + V_{GS1}$. In other words, V_b can be established by two diode-connected devices in series [Fig. 5.12(b)], provided that $V_{GS0} + V_{GS1} = V_{GS3} + V_{GS1}$, and hence $V_{GS0} = V_{GS3}$. We now attach the V_b generator of Fig. 5.12(b) to the cascode current source as shown in Fig. 5.12(c). The result allows accurate copying of the current even in the presence of body effect (why?).

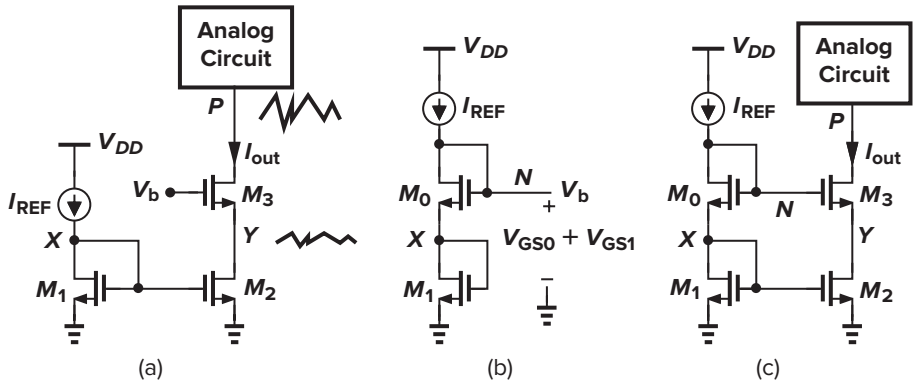


Figure 5.12 (a) Cascode current source, (b) modification of mirror circuit to generate the cascode bias voltage, and (c) cascode current mirror.

A few notes on the sizing of the transistors in Fig. 5.12(c) are warranted. As explained earlier, we typically select $L_2 = L_1$ and scale W_2 (in integer units) with respect to W_1 to obtain the desired multiple of I_{REF}. Similarly, for V_{GS3} to be equal to V_{GS0}, we choose $L_3 = L_0$ and scale W_3 with respect to W_0 by the same factor, i.e., $W_3/W_0 = W_2/W_1$. In practice, L_3 and L_0 are equal to the minimum allowable value so as to minimize their width, while L_1 and L_2 may be longer in some cases.[1]

▶ Example 5.3

In Fig. 5.13, sketch V_X and V_Y as a function of I_{REF}. If I_{REF} requires 0.5 V to operate as a current source, what is its maximum value?

Solution

Since M_2 and M_3 are properly ratioed with respect to M_1 and M_0, we have $V_Y = V_X \approx \sqrt{2I_{REF}/[\mu_n C_{ox}(W/L)_1]} + V_{TH1}$. The behavior is plotted in Fig. 5.13(b).

To find the maximum value of I_{REF}, we note that

$$V_N = V_{GS0} + V_{GS1} \tag{5.8}$$

$$= \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}}}\left[\sqrt{\left(\frac{L}{W}\right)_0} + \sqrt{\left(\frac{L}{W}\right)_1}\right] + V_{TH0} + V_{TH1} \tag{5.9}$$

[1] To reduce channel-length modulation, mismatches, or flicker noise.

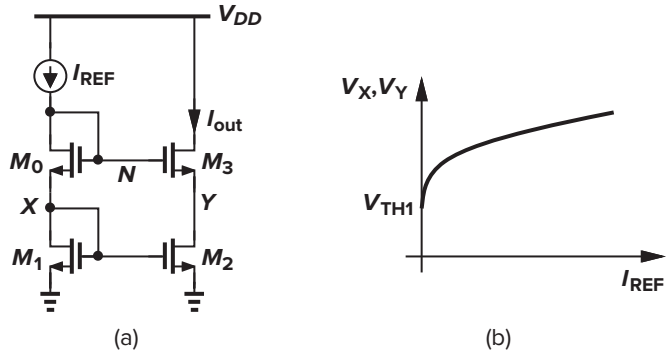


Figure 5.13

Thus,

$$V_{DD} - \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}}}\left[\sqrt{\left(\frac{L}{W}\right)_0} + \sqrt{\left(\frac{L}{W}\right)_1}\right] - V_{TH0} - V_{TH1} = 0.5\ \text{V} \tag{5.10}$$

and hence

$$I_{REF,max} = \frac{\mu_n C_{ox}}{2}\frac{(V_{DD} - 0.5\ \text{V} - V_{TH0} - V_{TH1})^2}{(\sqrt{(L/W)_0} + \sqrt{(L/W)_1})^2} \tag{5.11}$$

While operating as a current source with a high output impedance and accurate value, the topology of Fig. 5.12(c) nonetheless consumes substantial voltage headroom. For simplicity, let us neglect the body effect and assume that all of the transistors are identical. Then, the minimum allowable voltage at node P is equal to

$$V_N - V_{TH} = V_{GS0} + V_{GS1} - V_{TH} \tag{5.12}$$

$$= (V_{GS0} - V_{TH}) + (V_{GS1} - V_{TH}) + V_{TH} \tag{5.13}$$

i.e., two overdrive voltages plus one threshold voltage. How does this value compare with that in Fig. 5.12(a) if V_b could be chosen more arbitrarily? As shown in Fig. 5.14(a), V_b could be so low

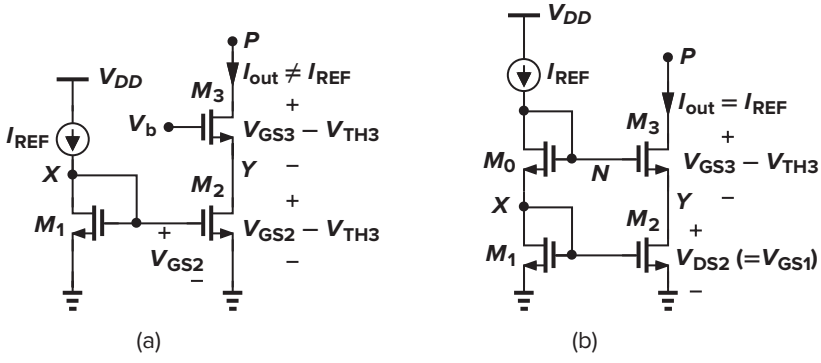


Figure 5.14 (a) Cascode current source with minimum headroom voltage; (b) headroom consumed by a cascode mirror.

$(= V_{GS3} + V_{GS2} - V_{TH2})$ that the minimum allowable voltage at P is merely two overdrive voltages. Thus, the cascode mirror of Fig. 5.12(c) "wastes" one threshold voltage in the headroom. This is because $V_{DS2} = V_{GS2}$, whereas V_{DS2} *could* be as low as $V_{GS2} - V_{TH}$ while maintaining M_2 in saturation.

Figure 5.14 summarizes our discussion. In Fig. 5.14(a), V_b is chosen to allow the lowest possible value of V_P, but the output current does not accurately track I_{REF} because M_1 and M_2 sustain unequal drain-source voltages. In Fig. 5.14(b), a higher accuracy is achieved, but the minimum level at P is higher by one threshold voltage.

Before resolving this issue, it is instructive to examine the large-signal behavior of a cascode current source.

▶ Example 5.4

In Fig. 5.15(a), assume that all of the transistors are identical and sketch I_X and V_B as V_X drops from a large positive value.

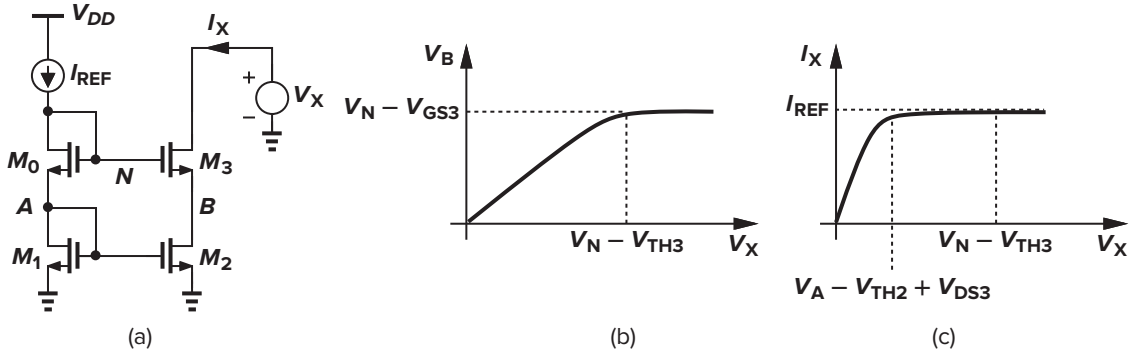


Figure 5.15

Solution

For $V_X \geq V_N - V_{TH}$, both M_2 and M_3 are in saturation, $I_X = I_{REF}$ and $V_B = V_A$. As V_X drops, which transistor enters the triode region first, M_3 or M_2? Suppose M_2 enters the triode region before M_3 does. For this to occur, V_{DS2} must drop and, since V_{GS2} is constant, so must I_{D2}. This means that V_{GS3} increases while I_{D3} decreases, which is not possible if M_3 is still in saturation. Thus, M_3 enters the triode region first.

As V_X falls below $V_N - V_{TH}$, M_3 enters the triode region, requiring a greater gate-source overdrive to carry the same current. Thus, as shown in Fig. 5.15(b), V_B begins to drop, causing I_{D2} and hence I_X to decrease slightly. As V_X and V_B decrease further, eventually we have $V_B < V_A - V_{TH}$, and M_2 enters the triode region. At this point, I_{D2} begins to drop sharply. For $V_X = 0$, $I_X = 0$, and M_2 and M_3 operate in the deep triode region. Note that as V_X drops below $V_N - V_{TH3}$, the output impedance of the cascode falls rapidly because g_{m3} degrades in the triode region. ◀

Second Approach In order to avoid the V_{TH} penalty in the voltage headroom of the above cascode current source, we force V_{DS1} to be equal to V_{DS2} instead. To understand this principle, we return to Fig. 5.14(a) and recognize that the V_{TH} headroom consumption is eliminated *only* if $V_b = V_{GS3} + (V_{GS2} - V_{TH2})$, i.e., only if V_{DS2} is around one overdrive voltage. How can we then ensure that $V_{DS1} = V_{DS2}$ $(= V_{GS2} - V_{TH2})$? Since M_1 is a diode-connected device, it appears impossible to expect a V_{DS1} less than one threshold.

A simple escape from the foregoing quandary is to create a deliberate voltage difference between the gate and drain of M_1 by a means of a resistor. Illustrated in Fig. 5.16(a), the idea is to choose $R_1 I_{REF} \approx V_{TH1}$ and $V_b = V_{GS3} + (V_{GS1} - V_{TH1})$. Now, $V_{DS1} = V_{GS1} - R_1 I_{REF} \approx V_{GS1} - V_{TH1}$, which is equal to $V_b - V_{GS3}$ and hence to V_{DS2}.

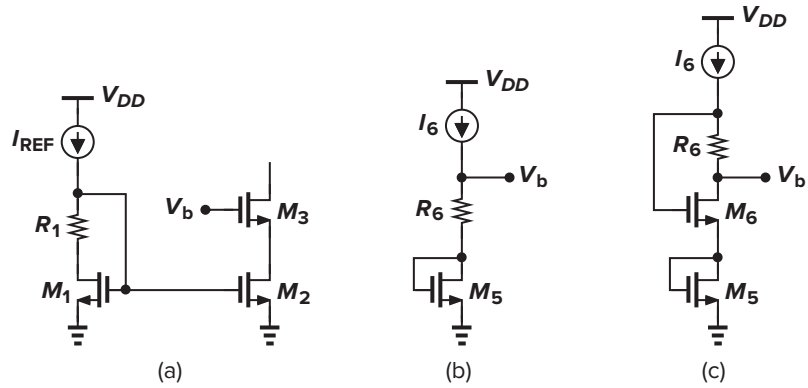


Figure 5.16 (a) Use of IR drop to improve accuracy of current mirror, (b) generation of V_b, and (c) alternative generation of V_b.

▶ Example 5.5

Is the M_1-R_1 combination in Fig. 5.16(a) a diode-connected device? Assume $\lambda > 0$.

Solution

From the small-signal equivalent shown in Fig. 5.17, we express the voltage drop across R_1 as $I_X R_1$ and write a KCL at the drain node:

$$\frac{V_X - I_X R_1}{r_O} + g_m V_X = I_X \tag{5.14}$$

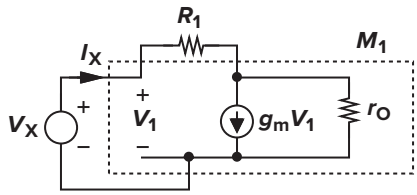


Figure 5.17

It follows that

$$\frac{V_X}{I_X} = \frac{R_1 + r_O}{1 + g_m r_O} \tag{5.15}$$

which reduces to $1/g_m$ in the absence of channel-length modulation. (Is it a coincidence that this impedance is the same as that seen at the source of a common-gate stage with $\gamma = 0$?!) Thus, from a small-signal point of view, the combination is close to a diode-connected device. From a large-signal point of view, $V_{GS1} \approx \sqrt{2I_D/[\mu_n C_{ox}(W/L)]} + V_{TH}$ if λ is small, suggesting diode-connected operation as well. ◀

The circuit of Fig. 5.16(a) entails two issues. First, in the presence of PVT variations, it may be difficult to guarantee that $R_1 I_{REF} \approx V_{TH1}$ as R_1 and V_{TH} may vary differently. Second, the generation of $V_b = V_{GS3} + (V_{GS1} - V_{TH1})$ is not straightforward. Let us address the latter issue first. We seek an arrangement that adds one gate-source voltage to an overdrive, surmising that we must begin with a diode-connected device. We consider the branch shown in Fig. 5.16(b) as a candidate and write $V_b = V_{GS5} + R_6 I_6$. We can readily choose I_6 and the dimensions of M_5 to ensure that $V_{GS5} = V_{GS3}$. However, the condition $R_6 I_6 = V_{GS1} - V_{TH1} = V_{GS1} - R_1 I_{REF}$ translates to $R_6 I_6 + R_1 I_{REF} = V_{GS1}$, which is difficult to meet

▶ **Example 5.7**

Figure 5.21(a) shows an alternative current mirror exhibiting a high output impedance. Study the small-signal and large-signal properties of the circuit.

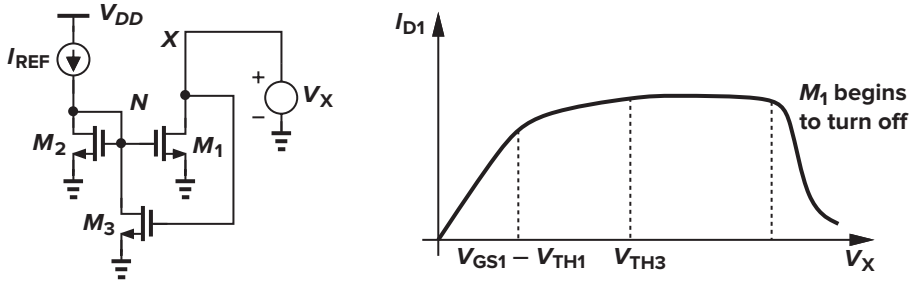


Figure 5.21

Solution

In this circuit, M_3 raises the output impedance by sensing the voltage change at node X and adjusting the voltage at node N. For example, suppose V_X rises by ΔV and tends to increase I_{D1} by $\Delta V/r_{O1}$. Transistor M_3 then draws a current change of $g_{m3}\Delta V$ from node N, causing V_N to fall by approximately $g_{m3}\Delta V/g_{m2}$ and I_{D1} to decrease by $(g_{m3}\Delta V/g_{m2})g_{m1}$. In other words, if we choose $g_{m3}g_{m1}/g_{m2} \approx r_{O1}^{-1}$, the net change in I_{D1} is small.

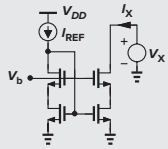
The circuit displays interesting large-signal properties. Let us sweep V_X from 0 to a high value and examine I_{D1}. At $V_X = 0$, M_1 operates in the deep triode region, carrying a zero current, and M_3 is off. As V_X rises, so does I_{D1} proportionally, up to $V_X = V_{GS1} - V_{TH1}$. Beyond this point, I_{D1} varies more gradually [Fig. 5.21(b)]. If V_X exceeds V_{TH3}, M_3 turns on and begins to "regulate" I_{D1}, creating a higher output impedance. However, for a sufficiently large V_X, M_3 absorbs all of I_{REF} and turns M_1 off.

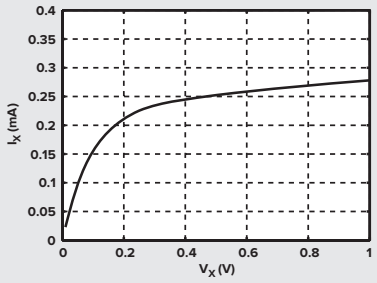
While providing a high output impedance without a cascode device, the above circuit does pose its own voltage headroom limitation, i.e., V_X must exceed $V_{TH3}(> V_{DS,sat})$.

◀

Nanometer Design Notes

Owing to severe channel-length modulation in nanometer devices, even the cascode current mirror may exhibit substantial mismatches. We choose $W/L = 5\ \mu$m/40 nm for the devices in the circuit shown below and $I_{REF} = 0.25$ mA. As V_X is swept from low to high values, we observe that I_X still varies noticeably even though all transistors are in saturation for 0.4 V $< V_X$.





5.3 ■ Active Current Mirrors

As mentioned earlier and exemplified by the circuit of Fig. 5.11, current mirrors can also process signals, i.e., operate as "active" elements. Particularly useful is a type of mirror topology used in conjunction with differential pairs. In this section, we study this circuit and its properties. Shown in Fig. 5.22 and sometimes called a five-transistor "operational transconductance amplifier" (OTA), this topology finds application in many analog and digital systems and merits a detailed study here. Note that the output is single-ended; hence the circuit is sometimes used to convert differential signals to a single-ended output. We analyze a simpler topology with passive load before studying the OTA.

Differential Pair with Passive Load To generate a single-ended output, we may simply discard one output of a differential pair as shown in Fig. 5.23(a). Here, a current source in a "passive " mirror arrangement serves as the load. What is the small-signal gain, $A_v = V_{out}/V_{in}$, of this circuit? We

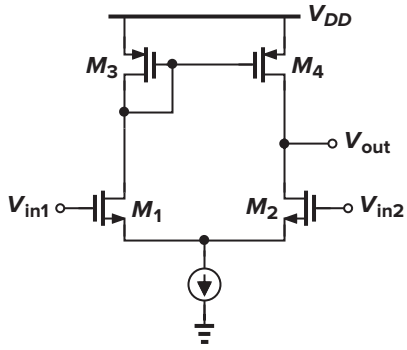


Figure 5.22 Five-transistor OTA.

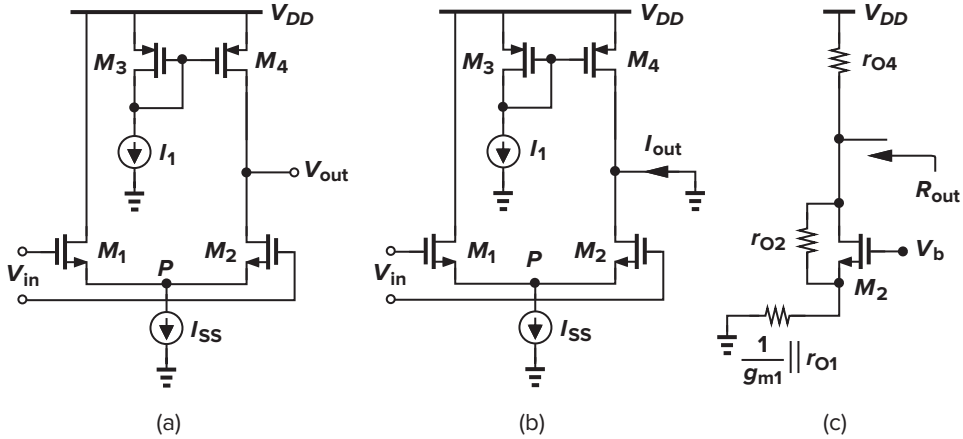


Figure 5.23 (a) Differential pair with current-source load; (b) circuit for calculation of G_m; (c) circuit for calculation of R_{out}.

calculate A_v using two different approaches, assuming $\gamma = 0$ for simplicity. Owing to the asymmetry, the half-circuit concept cannot be applied directly here.

Writing $|A_v| = G_m R_{out}$, we must compute the short-circuit transconductance, G_m, and the output resistance, R_{out}. We recognize from Fig. 5.23(b) that M_1 and M_2 become symmetric when the output is shorted to ac ground. Thus, $G_m = I_{out}/V_{in} = (g_{m1}V_{in}/2)/V_{in} = g_{m1}/2$. As illustrated in Fig. 5.23(c), for the R_{out} calculation, M_2 is degenerated by the source output impedance of M_1, $R_{deg} = (1/g_{m1})||r_{O1}$, thereby exhibiting an output impedance equal to $(1 + g_{m2}r_{O2})R_{deg} + r_{O2}a \approx 2r_{O2}$. It follows that $R_{out} = (2r_{O2})\|r_{O4}$, and

$$|A_v| = \frac{g_{m1}}{2}[(2r_{O2})\|r_{O4}] \tag{5.20}$$

Interestingly, if $r_{O4} \to \infty$, then $A_v \to -g_{m1}r_{O2}$.

In our second approach, we calculate V_P/V_{in} and V_{out}/V_P in Fig. 5.23(a) and multiply the results to obtain V_{out}/V_{in}. With the aid of Fig. 5.24 and viewing M_1 as a source follower, we write

$$\frac{V_P}{V_{in}} = \frac{R_{eq}||r_{O1}}{R_{eq}||r_{O1} + \dfrac{1}{g_{m1}}} \tag{5.21}$$

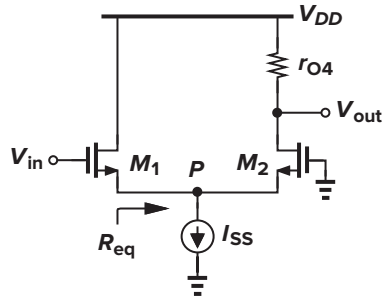


Figure 5.24 Circuit for calculation of V_P/V_{in}.

where R_{eq} denotes the resistance seen looking into the source of M_2. Since the drain of M_2 is terminated by a relatively large resistance, r_{O4}, the value of R_{eq} must be obtained from Eq. (3.117):

$$R_{eq} = \frac{r_{O2} + r_{O4}}{1 + g_{m2}r_{O2}} \tag{5.22}$$

It follows that

$$\frac{V_P}{V_{in}} = \frac{g_{m1}r_{O1}(r_{O2} + r_{O4})}{(1 + g_{m1}r_{O1})(r_{O2} + r_{O4}) + (1 + g_{m2}r_{O2})r_{O1}} \tag{5.23}$$

We now calculate V_{out}/V_P. From Fig. 5.25,

$$\frac{V_{out}}{V_P} = \frac{(1 + g_{m2}r_{O2})r_{O4}}{r_{O2} + r_{O4}} \tag{5.24}$$

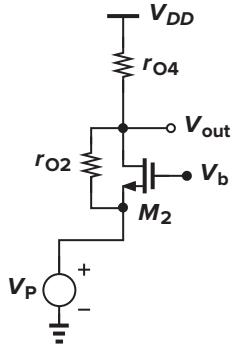


Figure 5.25 Circuit for calculation of V_{out}/V_P.

From (5.23) and (5.24), we have

$$\frac{V_{out}}{V_{in}} = \frac{g_{m2}r_{O2}r_{O4}}{2r_{O2} + r_{O4}} \tag{5.25}$$

$$= \frac{g_{m2}}{2}[(2r_{O2}) \| r_{O4}] \tag{5.26}$$

Differential Pair with Active Load In the circuit of Fig. 5.23(a), the small-signal drain current of M_1 is "wasted." As conceptually shown in Fig. 5.26(a), it is desirable to utilize this current with proper polarity at the output. This can be accomplished by the five-transistor OTA shown in Fig. 5.26(b), where M_3 and M_4 are identical and operate as an active current mirror.

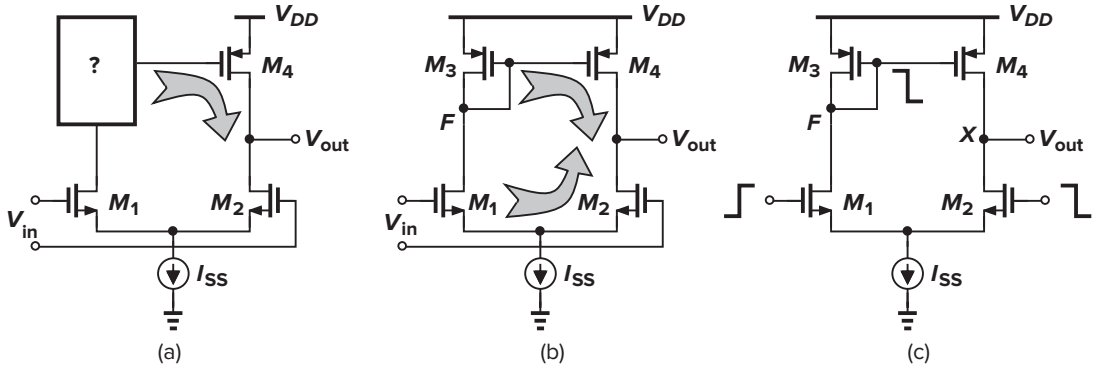


Figure 5.26 (a) Concept of combining the drain currents of M_1 and M_2, (b) realization of (a), and (c) response of the circuit to differential inputs.

To see how M_3 enhances the gain, suppose the gate voltages of M_1 and M_2 change by equal and opposite amounts [Fig. 5.26(c)]. Consequently, I_{D1} increases, V_F falls, and I_{D2} decreases. Thus, the output voltage rises by means of *two* mechanisms: M_2 draws less current from X to ground *and* M_4 pushes a greater current from V_{DD} to X. By contrast, in the circuit of Fig. 5.23(a), M_4 plays no active role in changing V_{out} because its gate voltage is constant. The five-transistor OTA is also called a differential pair with active load.

5.3.1 Large-Signal Analysis

Let us study the large-signal behavior of the five-transistor OTA. To this end, we replace the ideal tail current source by a MOSFET as shown in Fig. 5.27(a). If V_{in1} is much more negative than V_{in2}, M_1 is off, and so are M_3 and M_4. Since no current can flow from V_{DD}, both M_2 and M_5 operate in the deep triode region, carrying zero current. Thus, $V_{out} = 0$.[3] As V_{in1} approaches V_{in2}, M_1 turns on, drawing a fraction of I_{D5} from M_3 and turning M_4 on. The output voltage then depends on the difference between I_{D4} and I_{D2}. For a small difference between V_{in1} and V_{in2}, both M_2 and M_4 are saturated, providing a high gain [Fig. 5.27(b)]. As V_{in1} becomes more positive than V_{in2}, I_{D1}, $|I_{D3}|$, and $|I_{D4}|$ increase and I_{D2} decreases, allowing V_{out} to rise and eventually driving M_4 into the triode region. If $V_{in1} - V_{in2}$ is sufficiently large, M_2 turns off, M_4 operates in the deep triode region with zero current, and $V_{out} = V_{DD}$.

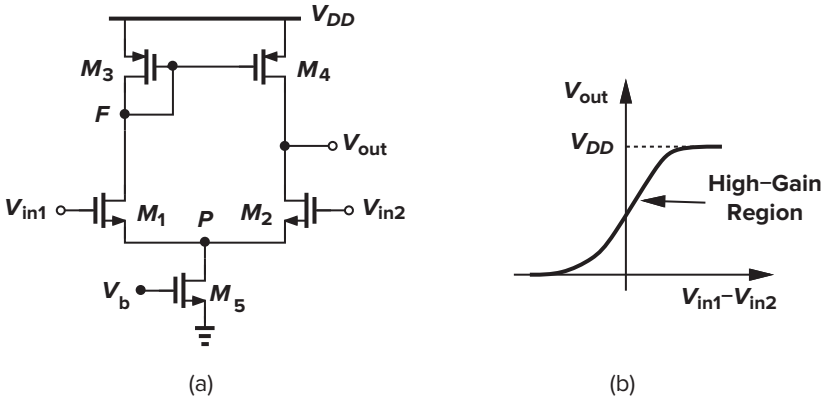


Figure 5.27 (a) Differential pair with active current mirror and realistic current source; (b) large-signal input-output characteristic.

[3] If V_{in1} is greater than one threshold voltage with respect to ground, M_5 may draw a small current from M_1, raising V_{out} slightly.

Note that if $V_{in1} > V_F + V_{TH}$, then M_1 enters the triode region. Also, V_{out} is in-phase with respect to V_{in1} but 180° out of phase with respect to V_{in2}.

The choice of the input common-mode voltage of the circuit is also important. For M_2 to be saturated, the output voltage cannot be less than $V_{in,CM} - V_{TH}$. Thus, to allow maximum output swings, the input CM level must be as low as possible, with the minimum given by $V_{GS1,2} + V_{DS5,min}$. The constraint imposed by the input CM level upon the output swing in this circuit is a critical drawback.

What is the output voltage of the circuit when $V_{in1} = V_{in2}$? With perfect symmetry, $V_{out} = V_F = V_{DD} - |V_{GS3}|$. This can be proved by contradiction as well. Suppose, for example, that $V_{out} < V_F$. Then, due to channel-length modulation, M_1 must carry a greater current than M_2 (and M_4 a greater current than M_3). In other words, the total current through M_1 is greater than half of I_{SS}. But this means that the total current through M_3 also exceeds $I_{SS}/2$, violating the assumption that M_4 carries more current than M_3. In reality, however, asymmetries in the circuit may result in a large deviation in V_{out}, possibly driving M_2 or M_4 into the triode region. For example, if the threshold voltage of M_2 is slightly smaller than that of M_1, the former carries a greater current than the latter even with $V_{in1} = V_{in2}$, causing V_{out} to drop significantly. For this reason, the circuit is rarely used in an open-loop configuration to amplify small signals. Nonetheless, the open-loop OTA proves useful as a differential to a single-ended converter for large swings, as illustrated by the following example.

▶ Example 5.8

Some digital circuits operate with differential (complementary) signals having voltage swings less than V_{DD}. For example, the single-ended swing can be 300 mV_{pp}. Explain how a five-transistor OTA can convert the moderate-swing differential signals to a single-ended rail-to-rail signal.

Solution

Consider the OTA shown in Fig. 5.28, where M_1 and M_2 sense swings equal to $V_2 - V_1 = 300$ mV. With proper choice of $(W/L)_{1,2}$ and I_{SS}, we can guarantee that such a swing turns off one side. For example, if M_1 carries all of I_{SS}, then M_2 remains off, allowing M_4 to pull V_{out} to V_{DD}. Conversely, when M_2 hogs I_{SS}, M_1, M_2, and M_4 turn off, M_2 and M_5 remain on with zero current, and $V_{out} = 0$. The "push-pull" action between M_2 and M_4 thus produces rail-to-rail swings at the output.

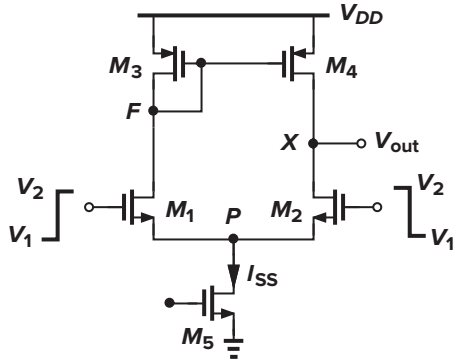


Figure 5.28

In practice, V_{out} does not reach exactly V_{DD} or zero if $V_1 > V_{TH1,2}$. The proof is left as an exercise for the reader. (Hint: if M_2 and M_5 are in the deep triode region, then V_P approaches zero, possibly turning on M_1.) For this reason, the OTA is typically followed by a CMOS inverter to obtain rail-to-rail swings. ◀

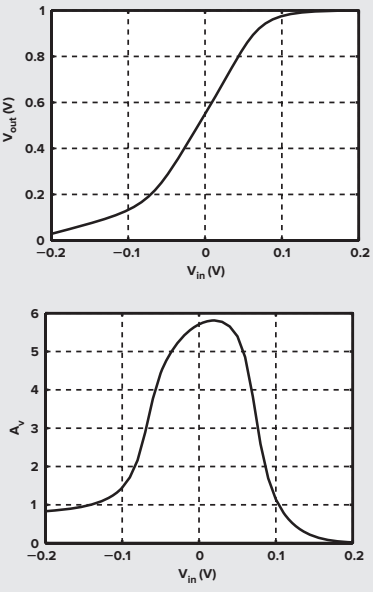
▶ Example 5.9

Assuming perfect symmetry, sketch the output voltage of the circuit in Fig. 5.29(a) as V_{DD} varies from 3 V to zero. Assume that for $V_{DD} = 3$ V, all of the devices are saturated.

turning M_4 and hence M_2 on. Note that, since $I_{D3} \approx I_{D4}$, we have $I_{D1} \approx I_{D2}$ and $V_{GS1} \approx V_{GS2}$. That is, $V_{out} \approx V_{in}$. This unity-gain action continues as V_{in} increases. For a sufficiently high V_{in}, two phenomena occur: (a) M_1 enters the triode region if $V_{in} > V_{DD} - |V_{GS3}| + V_{TH1}$, and (b) M_4 enters the triode region if $V_{out} > V_{DD} - |V_{GS4} - V_{TH4}|$, and hence $V_{in} > V_{DD} - |V_{GS4} - V_{TH4}|$. These two values are roughly equal if V_{TH1} and $|V_{TH4}|$ are comparable. Beyond this point, $|I_{D4}| < |I_{D3}|$ (why?), and hence $V_{GS1} > V_{GS2}$, yielding $V_{out} < V_{in}$. If $V_{in} = V_{DD}$, then M_4 carries little current and V_{out} incurs substantial error.

Nanometer Design Notes

The five-transistor OTA provides a limited gain in nanometer technologies and across a limited output range. With $V_{DD} = 1$ V, $W/L = 5\ \mu/40$ nm, a tail current of 0.25 mA, and input CM level of 0.5 V, we obtain the characteristic shown below. The slope plot also shows the steep drop in the gain as the NMOS or PMOS device tied to the output enters the triode region.



5.3.2 Small-Signal Analysis

We now analyze the small-signal properties of the circuit shown in Fig. 5.27(a), assuming $\gamma = 0$ for simplicity. Can we apply the half-circuit concept to calculate the differential gain here? As illustrated in Fig. 5.31, with small differential inputs, the voltage swings at nodes F and X are vastly different. This is because the diode-connected device M_3 yields a much lower voltage gain from the input to node F than that from the input to node X. As a result, the effects of V_F and V_X at node P (through r_{O1} and r_{O2}, respectively) do not cancel each other, and this node cannot be considered a virtual ground. Using the lemma $|A_v| = G_m R_{out}$, we first perform an approximate analysis so as to develop insight and then carry out an exact calculation of the gain.

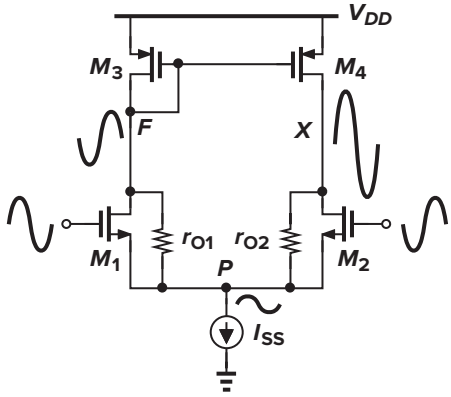


Figure 5.31 Asymmetric swings in a differential pair with active current mirror.

Approximate Analysis For the calculation of G_m, consider Fig. 5.32(a). The circuit is not quite symmetric, but because the impedance seen at node F is relatively low and the swing at this node small, the current returning from F to P through r_{O1} is negligible, and node P can be approximated by a virtual ground [Fig. 5.32(b)]. Thus, $I_{D1} = |I_{D3}| = |I_{D4}| = g_{m1,2}V_{in}/2$ and $I_{D2} = -g_{m1,2}V_{in}/2$, yielding $I_{out} = -g_{m1,2}V_{in}$, and hence $|G_m| = g_{m1,2}$. Note that, by virtue of active current mirror operation, this value is twice the transconductance of the circuit of Fig. 5.23(b).

Calculation of R_{out} is less straightforward. We may surmise that the output resistance of this circuit is equal to that of the circuit in Fig. 5.23(c), namely, $(2r_{O2})\|r_{O4}$. In reality, however, the active mirror operation yields a different value because when a voltage is applied to the output to measure R_{out}, the gate voltage of M_4 does not remain constant. Rather than draw the entire equivalent circuit, we observe that for small signals, I_{SS} is open [Fig. 5.33(a)], any current flowing into M_1 must flow out of M_2, and the role of the two transistors can be represented by a resistor $R_{XY} = 2r_{O1,2}$ [Fig. 5.33(b)]. As a result, the current drawn from V_X by R_{XY} is mirrored by M_3 onto M_4 with unity gain. This current is equal to

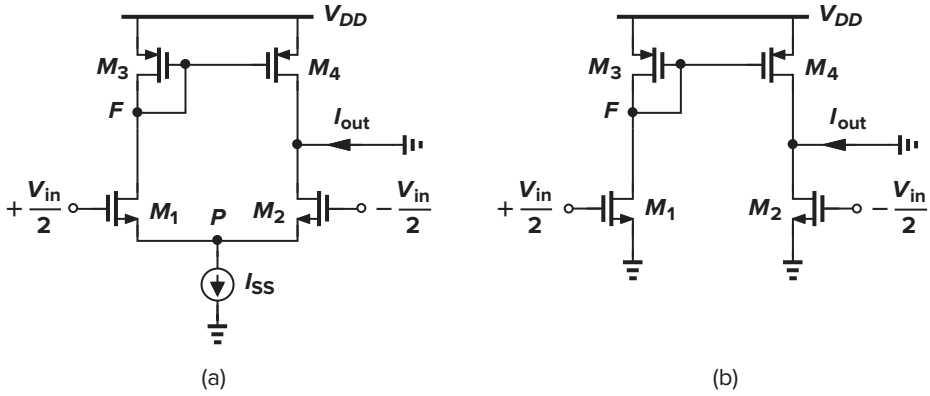


Figure 5.32 (a) Circuit for calculation of G_m; (b) circuit of (a) with node P grounded.

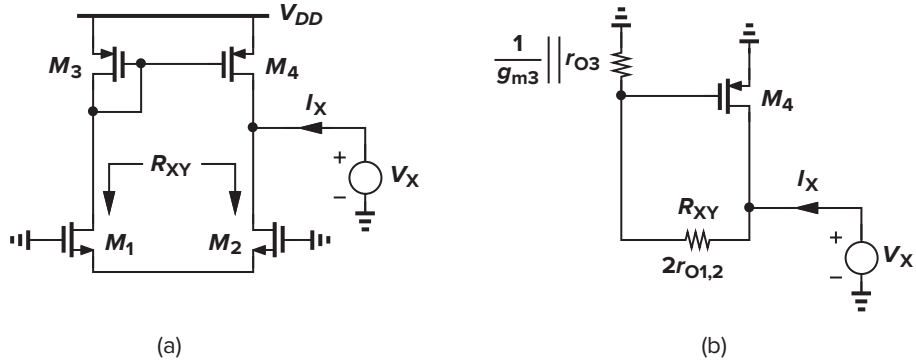


Figure 5.33 (a) Circuit for calculating R_{out}; (b) substitution of a resistor for M_1 and M_2.

$V_X/[2r_{O1,2} + (1/g_{m3})||r_{O3}]$. We multiply this current by $(1/g_{m3})||r_{O3}$ to obtain the gate-source voltage of M_4 and then multiply the result by g_{m4}. It follows that

$$I_X = \frac{V_X}{2r_{O1,2} + \dfrac{1}{g_{m3}}||r_{O3}} \left[1 + \left(\frac{1}{g_{m3}}||r_{O3}\right) g_{m4}\right] + \frac{V_X}{r_{O4}} \tag{5.27}$$

For $2r_{O1,2} \gg (1/g_{m3})\|r_{O3}$, we have

$$R_{out} \approx r_{O2}\|r_{O4} \tag{5.28}$$

The overall voltage gain is approximately equal to $|A_v| = G_m R_{out} = g_{m1,2}(r_{O2}\|r_{O4})$, somewhat higher than that of the circuit in Fig. 5.23(a).

Exact Analysis We must compute both the G_m and R_{out} of the OTA. Let us determine the G_m, without grounding node P, by solving the equivalent circuit shown in Fig. 5.34. For the sake of brevity, we use the subscript 1 to denote both M_1 and M_2. Since the current flowing downward through $(1/g_{m3})||r_{O3}$ (denoted by r_d hereafter) is $-V_4/r_d$, r_{O1} sustains a voltage equal to $(-V_4/r_d - g_{m1}V_1)r_{O1}$. Adding this voltage to $V_P = V_{in1} - V_1$, we have

$$\left(-\frac{V_4}{r_d} - g_{m1}V_1\right) r_{O1} + V_{in1} - V_1 = V_4 \tag{5.29}$$

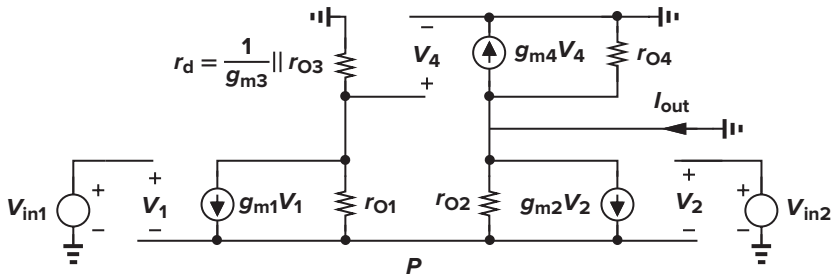


Figure 5.34 Equivalent circuit of five-transistor OTA

We also recognize that the sum of $g_{m2}V_2$ and the current flowing through r_{O2} is equal to V_4/r_d (why?). That is

$$g_{m2}V_2 - \frac{V_{in2} - V_2}{r_{O2}} = \frac{V_4}{r_D} \tag{5.30}$$

Obtaining V_1 and V_2 from these equations in terms of V_4 and noting that $V_1 - V_2 = V_{in1} - V_{in2}$ and $I_{out} = g_{m4}V_4 + V_4/r_d$, we arrive at

$$I_{out} = -g_{m1}r_{O1}\frac{g_{m4}r_d + 1}{r_d + 2r_{O1}}(V_{in1} - V_{in2}) \tag{5.31}$$

It follows that

$$G_m = -g_{m1}r_{O1}\frac{g_{m4}r_d + 1}{r_d + 2r_{O1}} \tag{5.32}$$

In the next step, we calculate R_{out}. Let us express the output admittance from Eq. (5.27) as

$$\frac{I_X}{V_X} = \frac{1 + g_{m4}r_d}{2r_{O1} + r_d} + \frac{1}{r_{O4}} \tag{5.33}$$

$$= \frac{(1 + g_{m4}r_d)r_{O4} + 2r_{O1} + r_d}{(2r_{O1} + r_d)r_{O4}} \tag{5.34}$$

and hence

$$G_m R_{out} = -g_{m1}r_{O1}\frac{(g_{m4}r_d + 1)r_{O4}}{(g_{m4}r_d + 1)r_{O4} + 2r_{O1} + r_d} \tag{5.35}$$

Since $r_d = r_{O3}/(1 + g_{m3}r_{O3})$, this expression reduces to

$$G_m R_{out} = -g_{m1}r_{O1}r_{O4}\frac{2g_{m3}r_{O3} + 1}{(2g_{m3}r_{O3} + 1)r_{O4} + 2r_{O1}(1 + g_{m3}r_{O3}) + r_{O3}} \tag{5.36}$$

$$= -\frac{g_{m1}r_{O1}r_{O4}}{r_{O1} + r_{O3}} \cdot \frac{2g_{m3}r_{O3} + 1}{2(g_{m3}r_{O3} + 1)} \tag{5.37}$$

We thus obtain a simple but exact expression for the gain:

$$|A_v| = g_{m1}(r_{O1}||r_{O4})\frac{2g_{m4}r_{O4} + 1}{2(g_{m4}r_{O4} + 1)} \tag{5.38}$$

We can view this result as our approximate solution, $g_{m1}(r_{O1}||r_{O4})$, multiplied by a "correction" factor that is *less* than unity. For example, if $g_{m4}r_{O4} = 5$, then $|A_v| = 0.92g_{m1}(r_{O1}||r_{O4})$.

▶ Example 5.11

With the aid of the above results, determine the output response to an input CM change if mismatches are neglected.

Solution

To represent an input CM change, we choose $V_{in1} = V_{in2}$ in Fig. 5.34, obtaining from Eq. (5.31) $I_{out} = 0$. The single-ended output voltage is therefore free from the input CM change. ◀

▶ Example 5.12

Calculate the small-signal voltage gain of the circuit shown in Fig. 5.35. How does the performance of this circuit compare with that of a differential pair with active mirror?

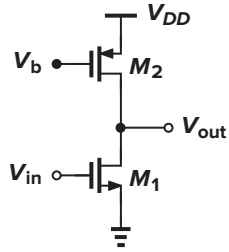


Figure 5.35

Solution

We have $A_v = g_{m1}(r_{O1}\|r_{O2})$, similar to the value derived above. For given device dimensions, this circuit requires half of the bias current to achieve the same gain as a differential pair. However, advantages of differential operation (less sensitivity to CM noise and less distortion) often outweigh the power penalty. ◀

The above calculations of the gain have assumed an ideal tail current source. In reality, the output impedance of this source affects the gain, but the error is relatively small.

Headroom Issues The five-transistor OTA does not easily lend itself to low-voltage operation as the diode-connected PMOS device tends to consume a substantial voltage headroom. To arrive at a modification, we observe that the gate voltage of this device need not be equal to its drain voltage. As shown in Fig. 5.36, we insert a resistor in series with the gate and draw a constant current from it, thereby

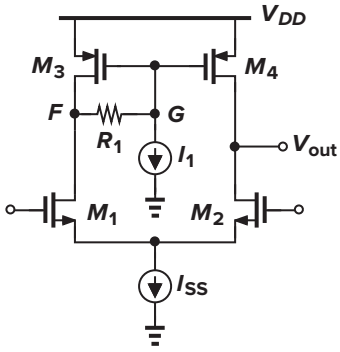


Figure 5.36 OTA headroom improvement by level shift.

allowing V_G to be below V_F by $R_1 I_1 \leq V_{TH3}$. With this level shift, the input CM level can be higher, easing the design of the preceding stage and the tail current source. The value of I_1 must be much less than $I_{SS}/2$ so as to introduce negligible asymmetry between the two sides of the circuit. The reader is encouraged to compute the input-referred offset voltage arising from I_1.

5.3.3 Common-Mode Properties

Let us now study the common-mode properties of the differential pair with active current mirror. We assume $\gamma = 0$ for simplicity and leave a more general analysis including body effect for the reader. Our objective is to predict the consequences of a finite output impedance in the tail current source. As depicted in Fig. 5.37, a change in the input CM level leads to a change in the bias current of all of the transistors. How do we define the common-mode gain here? Recall from Chapter 4 that the CM gain represents the *corruption* of the output signal of interest due to variations in the input CM level. In the circuits of Chapter 3, the output signal was sensed differentially, and hence the CM gain was defined in terms of the output differential component generated by the input CM change. In the circuit of Fig. 5.37, on the other hand, the output signal of interest is sensed with respect to ground. Thus, we define the CM gain in terms of the single-ended output component produced by the input CM change:

$$A_{CM} = \frac{\Delta V_{out}}{\Delta V_{in,CM}} \tag{5.39}$$

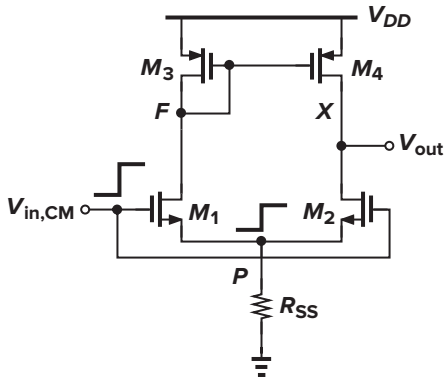


Figure 5.37 Differential pair with active current mirror sensing a common-mode change.

To determine A_{CM}, we observe that if the transistors are symmetric, $V_{out} = V_F$ for any input CM level (Section 5.3.1). For example, as $V_{in,CM}$ increases, V_F drops and so does V_{out}. In other words, nodes F and X can be shorted [Fig. 5.38(a)], resulting in the equivalent circuit shown in Fig. 5.38(b). Here, M_1 and M_2 appear in parallel and so do M_3 and M_4. It follows that

$$A_{CM} \approx \frac{-\dfrac{1}{2g_{m3,4}} \Big\| \dfrac{r_{O3,4}}{2}}{\dfrac{1}{2g_{m1,2}} + R_{SS}} \tag{5.40}$$

$$= \frac{-1}{1 + 2g_{m1,2}R_{SS}} \frac{g_{m1,2}}{g_{m3,4}} \tag{5.41}$$

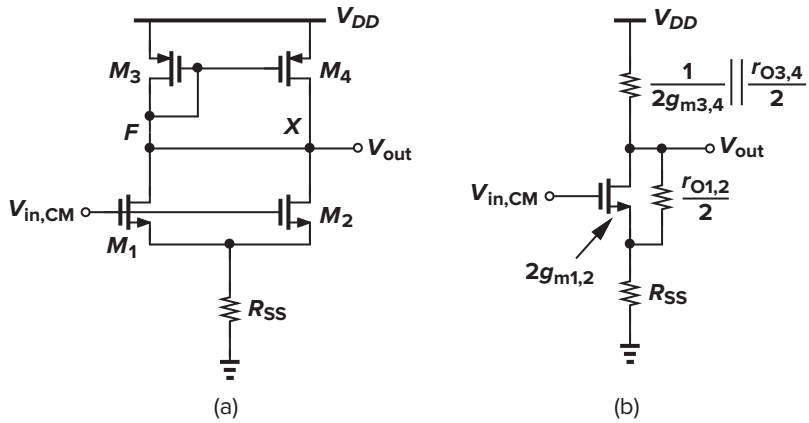


Figure 5.38 (a) Simplified circuit of Fig. 5.37; (b) equivalent circuit of (a).

where we have assumed that $1/(2g_{m3,4}) \ll r_{O3,4}$ and neglected the effect of $r_{O1,2}/2$. The CMRR is then given by

$$\text{CMRR} = \left| \frac{A_{DM}}{A_{CM}} \right| \tag{5.42}$$

$$= g_{m1,2}(r_{O1,2} \| r_{O3,4}) \frac{g_{m3,4}(1 + 2g_{m1,2}R_{SS})}{g_{m1,2}} \tag{5.43}$$

$$= (1 + 2g_{m1,2}R_{SS}) g_{m3,4}(r_{O1,2} \| r_{O3,4}) \tag{5.44}$$

For example, if $R_{SS} = r_O$ and $2g_{m1,2}r_O \gg 1$, then CMRR is on the order of $(g_m r_O)^2$.

Equation (5.41) indicates that, even with perfect symmetry, the output signal is corrupted by input CM variations. High-frequency common-mode noise therefore degrades the performance considerably as the capacitance shunting the tail current source exhibits a lower impedance.

▶ Example 5.13

The CM gain of the circuit of Fig. 5.37 can be shown to be *zero* by a (flawed) argument. As shown in Fig. 5.39(a), if $V_{in,CM}$ introduces a change of ΔI in the drain current of each input transistor, then I_{D3} also experiences the same change, and so does I_{D4}. Thus, M_4 seemingly provides the additional current required by M_2, and the output voltage need not change, i.e., $A_{CM} = 0$. Explain the flaw in this proof.

Solution

The assumption that ΔI_{D4} completely cancels the effect of ΔI_{D2} is incorrect. Consider the equivalent circuit shown in Fig. 5.39(b). Since

$$\Delta V_F = \Delta I_1 \left(\frac{1}{g_{m3}} \middle\| r_{O3} \right) \tag{5.45}$$

we have

$$|\Delta I_{D4}| = g_{m4} \Delta V_F \tag{5.46}$$

$$= g_{m4} \Delta I_1 \frac{r_{O3}}{1 + g_{m3} r_{O3}} \tag{5.47}$$

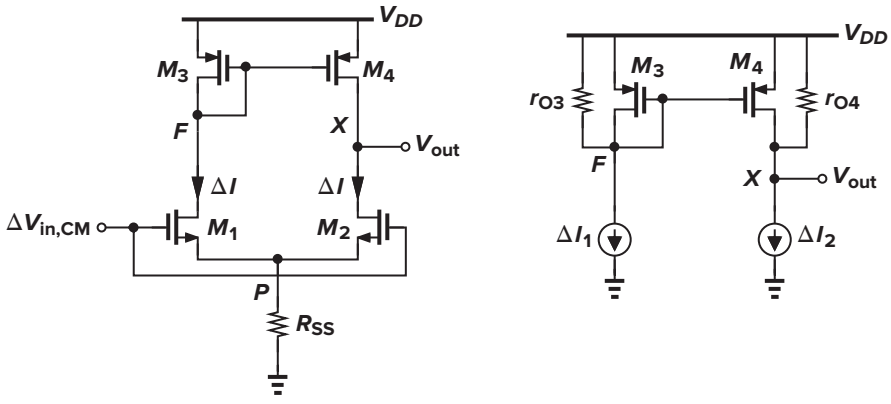


Figure 5.39

This current and ΔI_2 ($= \Delta I_1 = \Delta I$) give a net voltage change equal to

$$\Delta V_{out} = (\Delta I_1 g_{m4} \frac{r_{O3}}{1 + g_{m3} r_{O3}} - \Delta I_2) r_{O4} \tag{5.48}$$

$$= -\Delta I \frac{1}{g_{m3} r_{O3} + 1} r_{O4} \tag{5.49}$$

which is equal to the voltage change at node F. ◀

Effect of Mismatches It is also instructive to calculate the common-mode gain in the presence of mismatches. As an example, we consider the case where the input transistors exhibit slightly different transconductances [Fig. 5.40(a)]. How does V_{out} depend on $V_{in,CM}$? Since the change at nodes F and X is relatively small, we can compute the change in I_{D1} and I_{D2} while neglecting the effect of r_{O1} and r_{O2}. As shown in Fig. 5.40(b), the voltage change at P can be obtained by considering M_1 and M_2 as a single transistor (in a source follower configuration) with a transconductance equal to $g_{m1} + g_{m2}$, i.e.,

$$\Delta V_P = \Delta V_{in,CM} \frac{R_{SS}}{R_{SS} + \dfrac{1}{g_{m1} + g_{m2}}} \tag{5.50}$$

where body effect is neglected. The changes in the drain currents of M_1 and M_2 are therefore given by

$$\Delta I_{D1} = g_{m1}(\Delta V_{in,CM} - \Delta V_P) \tag{5.51}$$

$$= \frac{\Delta V_{in,CM}}{R_{SS} + \dfrac{1}{g_{m1} + g_{m2}}} \frac{g_{m1}}{g_{m1} + g_{m2}} \tag{5.52}$$

$$\Delta I_{D2} = g_{m2}(\Delta V_{in,CM} - \Delta V_P) \tag{5.53}$$

$$= \frac{\Delta V_{in,CM}}{R_{SS} + \dfrac{1}{g_{m1} + g_{m2}}} \frac{g_{m2}}{g_{m1} + g_{m2}} \tag{5.54}$$

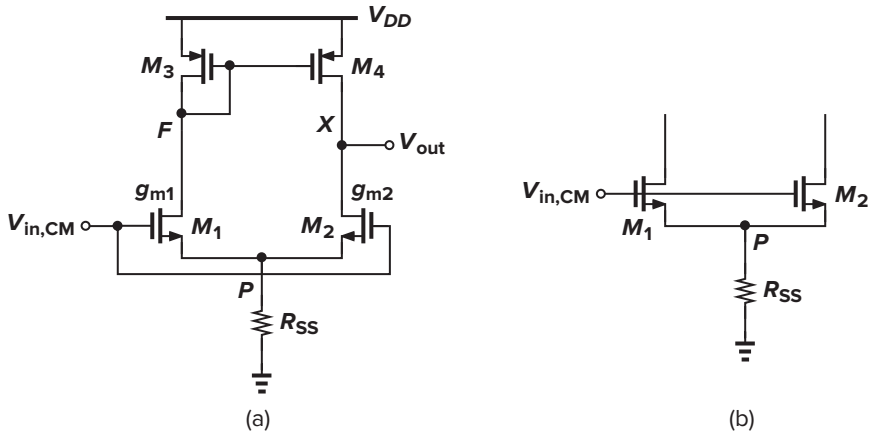


Figure 5.40 Differential pair with g_m mismatch.

The change ΔI_{D1} multiplied by $(1/g_{m3})\|r_{O3}$ yields $|\Delta I_{D4}| = g_{m4}[(1/g_{m3})\|r_{O3}]\Delta I_{D1}$. The difference between this current and ΔI_{D2} flows through the output impedance of the circuit, which is equal to r_{O4} because we have neglected the effect of r_{O1} and r_{O2}:

$$\Delta V_{out} = \left[\frac{g_{m1}\Delta V_{in,CM}}{1+(g_{m1}+g_{m2})R_{SS}} \frac{r_{O3}}{r_{O3}+\dfrac{1}{g_{m3}}} - \frac{g_{m2}\Delta V_{in,CM}}{1+(g_{m1}+g_{m2})R_{SS}} \right] r_{O4} \tag{5.55}$$

$$= \frac{\Delta V_{in,CM}}{1+(g_{m1}+g_{m2})R_{SS}} \frac{(g_{m1}-g_{m2})r_{O3}-g_{m2}/g_{m3}}{r_{O3}+\dfrac{1}{g_{m3}}} r_{O4} \tag{5.56}$$

If $r_{O3} \gg 1/g_{m3}$, we have

$$\frac{\Delta V_{out}}{\Delta V_{in,CM}} \approx \frac{(g_{m1}-g_{m2})r_{O3}-g_{m2}/g_{m3}}{1+(g_{m1}+g_{m2})R_{SS}} \tag{5.57}$$

Compared to Eq. (5.41), this result contains the additional term $(g_{m1}-g_{m2})r_{O3}$ in the numerator, revealing the effect of transconductance mismatch on the common-mode gain.

5.3.4 Other Properties of Five-Transistor OTA

The five-transistor OTA suffers from two drawbacks with respect to the fully-differential topologies studied in Chapter 4. First, the circuit exhibits a finite CMRR even with perfectly-matched transistors. As depicted in Fig. 5.41(a), an input CM change directly corrupts V_{out} in this OTA, but not the *differential* output in the fully-differential version [Fig. 5.41(b)].

Second, the supply rejection of this OTA is inferior. To understand this point, let us tie the inputs to a constant voltage and change V_{DD} by a small amount, ΔV_{DD} [Fig. 5.42(a)]. How much does V_F change? Viewing M_1 as a constant current source with a high output impedance, we recognize that V_{GS3} must remain relatively constant. That is, $\Delta V_F \approx \Delta V_{DD}$. With symmetric transistors, V_{out} must also change by ΔV_{DD}. In other words, the gain from V_{DD} to V_{out} is about unity.

Now consider the fully-differential topology in Fig. 5.42(b), where the PMOS current sources are biased by a current mirror arrangement. How do V_X and V_Y change here in response to a supply change

Problems

Unless otherwise stated, in the following problems, use the device data shown in Table 2.1 and assume that $V_{DD} = 3$ V where necessary. All device dimensions are effective values and in microns.

5.1. In Fig. 5.2, assume that $(W/L)_1 = 50/0.5$, $\lambda = 0$, $I_{out} = 0.5$ mA, and M_1 is saturated.
(a) Determine R_2/R_1.
(b) Calculate the sensitivity of I_{out} to V_{DD}, defined as $\partial I_{out}/\partial V_{DD}$ and normalized to I_{out}.
(c) How much does I_{out} change if V_{TH} changes by 50 mV?
(d) If the temperature dependence of μ_n is expressed as $\mu_n \propto T^{-3/2}$ but V_{TH} is independent of temperature, how much does I_{out} vary if T changes from 300 °K to 370 °K?
(e) What is the worst-case change in I_{out} if V_{DD} changes by 10%, V_{TH} changes by 50 mV, and T changes from 300 °K to 370 °K?

5.2. Consider the circuit of Fig. 5.7. Assuming I_{REF} is *ideal*, sketch I_{out} versus V_{DD} as V_{DD} varies from 0 to 3 V.

5.3. In the circuit of Fig. 5.8, $(W/L)_N = 10/0.5$, $(W/L)_P = 10/0.5$, and $I_{REF} = 100\ \mu$A. The input CM level applied to the gates of M_1 and M_2 is equal to 1.3 V.
(a) Assuming $\lambda = 0$, calculate V_P and the drain voltage of the PMOS diode-connected transistors.
(b) Now take channel-length modulation into account to determine I_T and the drain current of the PMOS diode-connected transistors more accurately.

5.4. In the circuit of Fig. 5.11, sketch V_{out} versus V_{DD} as V_{DD} varies from 0 to 3 V.

5.5. Consider the circuit of Fig. 5.12(a), assuming $(W/L)_{1-3} = 40/0.5$, $I_{REF} = 0.3$ mA, and $\gamma = 0$.
(a) Determine V_b such that $V_X = V_Y$.
(b) If V_b deviates from the value calculated in part (a) by 100 mV, what is the mismatch between I_{out} and I_{REF}?
(c) If the circuit fed by the cascode current source changes V_P by 1 V, how much does V_Y change?

5.6. The circuit of Fig. 5.18(b) is designed with $(W/L)_{1,2} = 20/0.5$, $(W/L)_{3,0} = 60/0.5$, and $I_{REF} = 100\ \mu$A.
(a) Determine V_X and the acceptable range of V_b.
(b) Estimate the deviation of I_{out} from 300 μA if the drain voltage of M_3 is higher than V_X by 1 V.

5.7. The circuit of Fig. 5.23(a) is designed with $(W/L)_{1-4} = 50/0.5$ and $I_{SS} = 2I_1 = 0.5$ mA.
(a) Calculate the small-signal voltage gain.
(b) Determine the maximum output voltage swing if the input CM level is 1.3 V.

5.8. Consider the circuit of Fig. 5.29(a) with $(W/L)_{1-5} = 50/0.5$ and $I_{D5} = 0.5$ mA.
(a) Calculate the deviation of V_{out} from V_F if $|V_{TH3}|$ is 1 mV less than $|V_{TH4}|$.
(b) Determine the CMRR of the amplifier.

5.9. Sketch V_X and V_Y as a function of V_{DD} for each circuit in Fig. 5.52. Assume the transistors in each circuit are identical.

5.10. Sketch V_X and V_Y as a function of V_{DD} for each circuit in Fig. 5.53. Assume the transistors in each circuit are identical.

5.11. For each circuit in Fig. 5.54, sketch V_X and V_Y as a function of V_1 for $0 < V_1 < V_{DD}$. Assume the transistors in each circuit are identical.

5.12. For each circuit in Fig. 5.55, sketch V_X and V_Y as a function of V_1 for $0 < V_1 < V_{DD}$. Assume the transistors in each circuit are identical.

5.13. For each circuit in Fig. 5.56, sketch V_X and V_Y as a function of I_{REF}.

5.14. For the circuit of Fig. 5.57, sketch I_{out}, V_X, V_A, and V_B as a function of **(a)** I_{REF}, **(b)** V_b.

5.15. In the circuit shown in Fig. 5.58, a source follower using a wide transistor and a small bias current is inserted in series with the gate of M_3 so as to bias M_2 at the edge of saturation. Assuming M_0–M_3 are identical and $\lambda \neq 0$, estimate the mismatch between I_{out} and I_{REF} if **(a)** $\gamma = 0$, **(b)** $\gamma \neq 0$.

5.16. Sketch V_X and V_Y as a function of time for each circuit in Fig. 5.59. Assume the transistors in each circuit are identical.

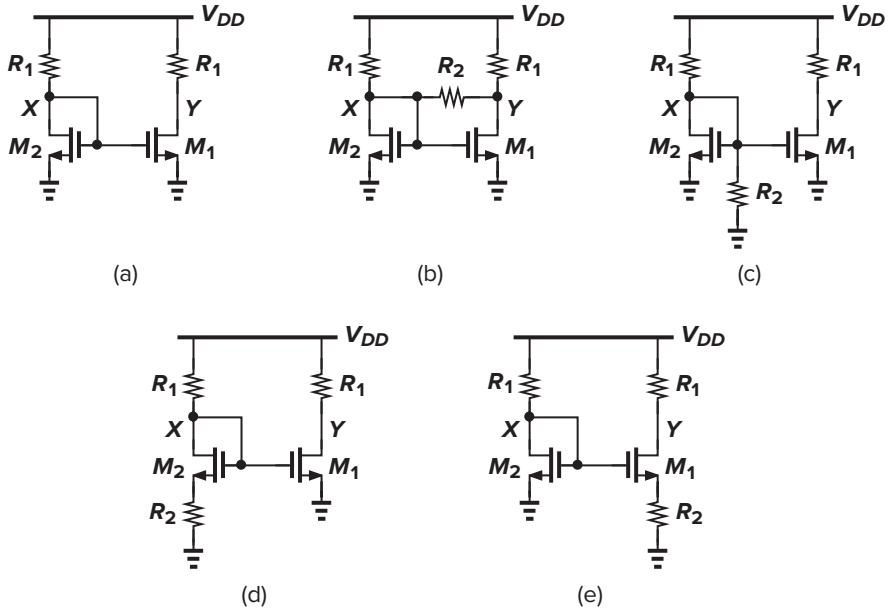


Figure 5.52

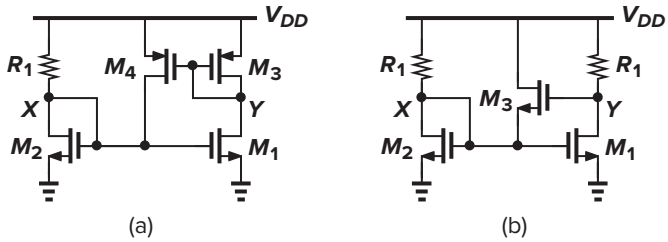


Figure 5.53

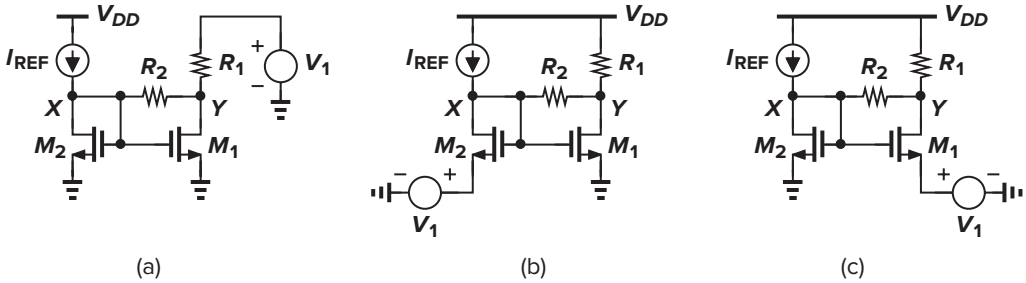


Figure 5.54

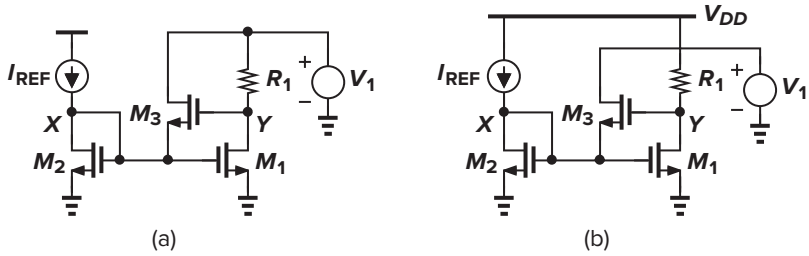


Figure 5.55

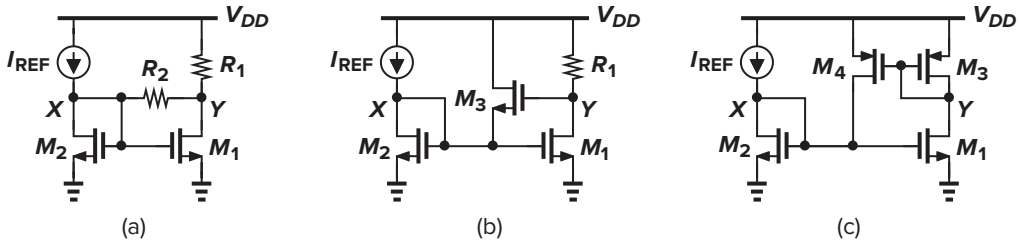


Figure 5.56

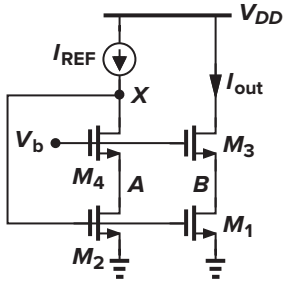


Figure 5.57

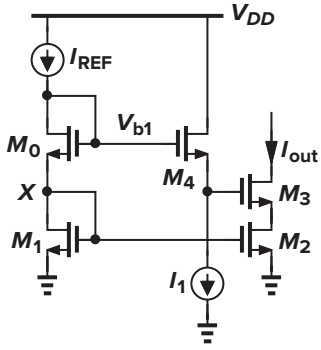


Figure 5.58

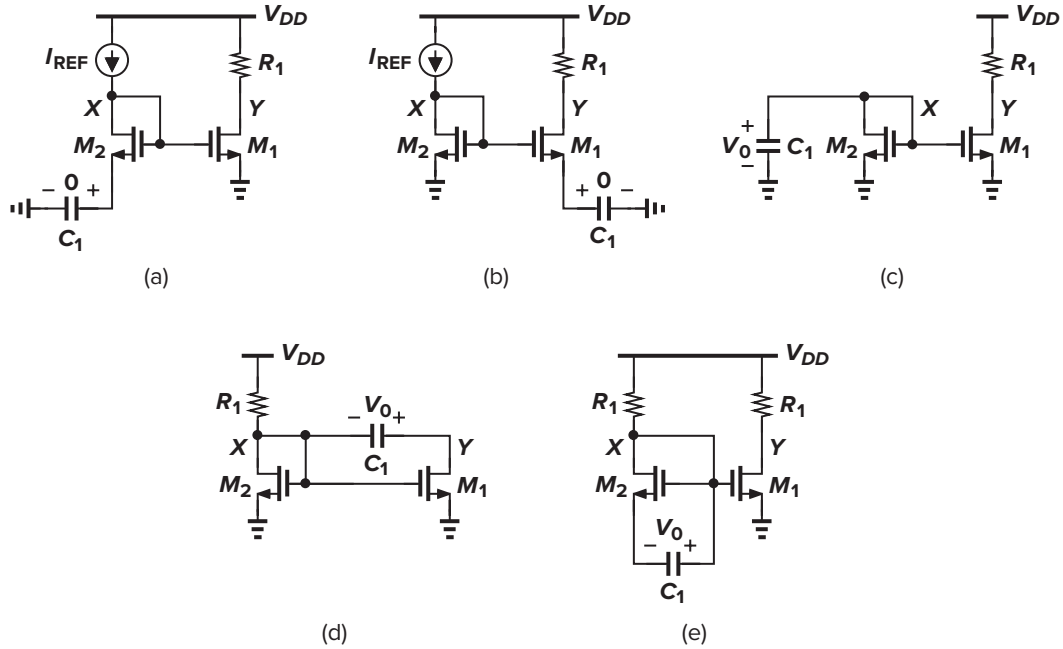


Figure 5.59

5.17. Sketch V_X and V_Y as a function of time for each circuit in Fig. 5.60. Assume the transistors in each circuit are identical.

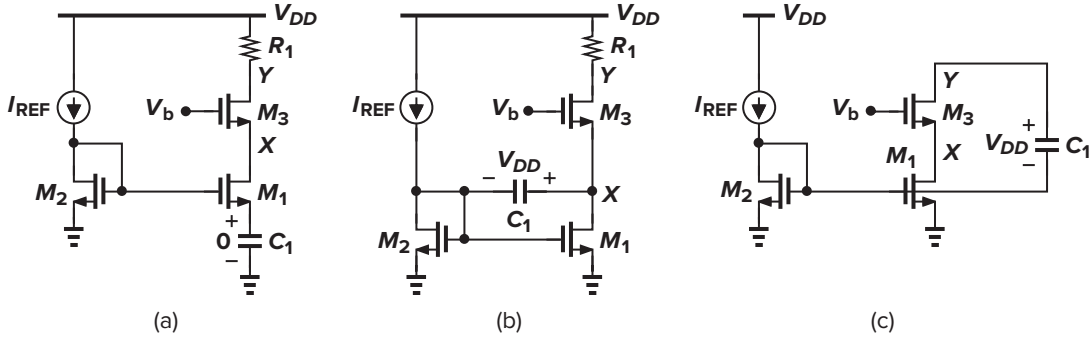


Figure 5.60

5.18. Sketch V_X and V_Y as a function of time for each circuit in Fig. 5.61. Assume the transistors in each circuit are identical.

5.19. The circuit shown in Fig. 5.62 exhibits a *negative* input inductance. Calculate the input impedance of the circuit and identify the inductive component.

5.20. Due to a manufacturing defect, a large parasitic resistance, R_1, has appeared in the circuits of Fig. 5.63. Calculate the gain of each circuit if $\lambda > 0$.

5.21. In digital circuits such as memories, a differential pair with an active current mirror is used to convert a small differential signal to a large single-ended swing (Fig. 5.64). In such applications, it is desirable that the output levels be as close to the supply rails as possible. Assuming moderate differential input swings (e.g., $\Delta V = 0.1$ V) around a common-mode level $V_{in,CM}$ and a high gain in the circuit, explain why V_{min} depends on $V_{in,CM}$.

5.22. Sketch V_X and V_Y for each circuit in Fig. 5.65 as a function of time. The initial voltage across C_1 is shown.

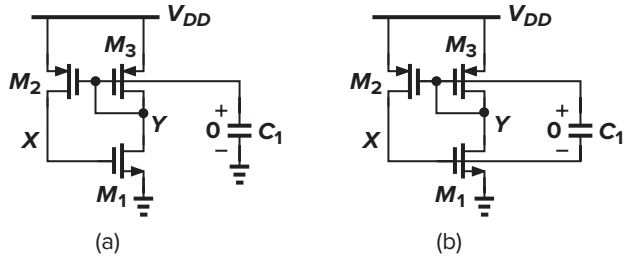


Figure 5.61

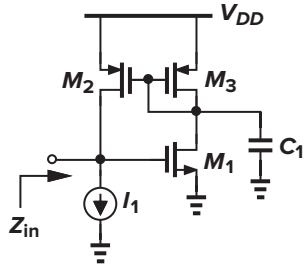


Figure 5.62

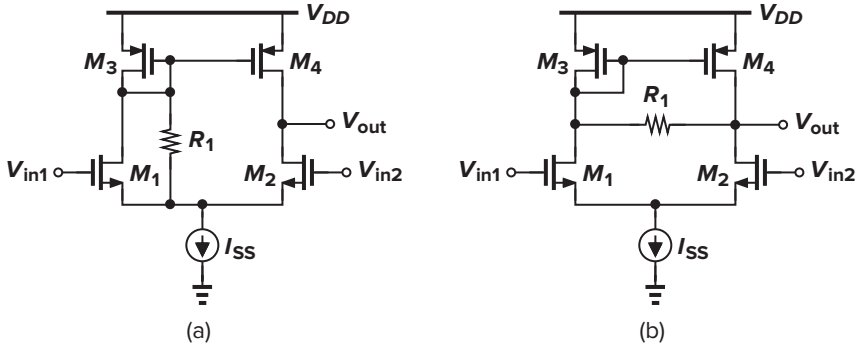


Figure 5.63

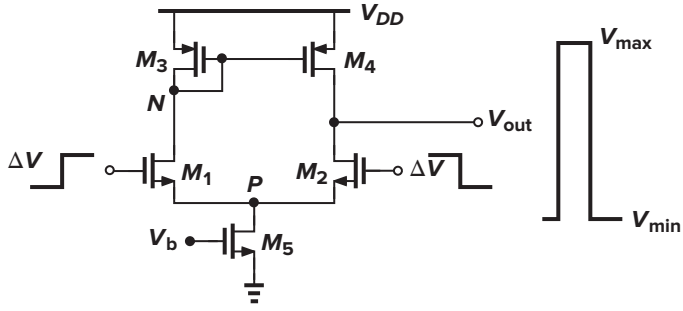


Figure 5.64

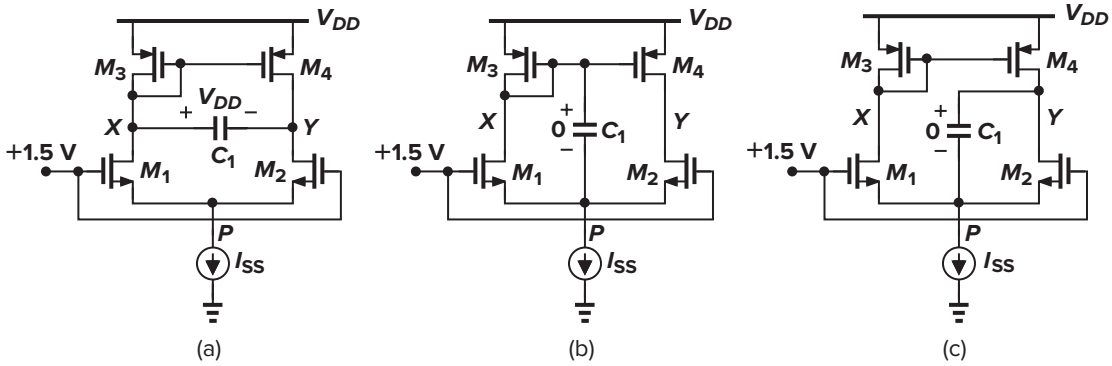


Figure 5.65

5.23. If in Fig. 5.66, ΔV is small enough that all of the transistors remain in saturation, determine the time constant and the initial and final values of V_{out}.

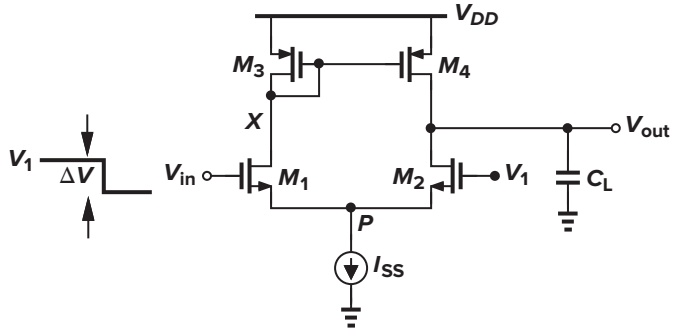


Figure 5.66

5.24. For a device operating in the subthreshold region, we have

$$I_D = \mu C_d \frac{W}{L} V_T^2 \left(\exp \frac{V_{GS} - V_{TH}}{V_T} \right) \left(1 - \exp \frac{-V_{DS}}{V_T} \right) \tag{5.64}$$

(a) If the device is in the deep triode region, $V_{DS} \ll V_T$. Using $\exp(-\epsilon) \approx 1 - \epsilon$, determine the on-resistance.
(b) If the device is in saturation, $V_{DS} \gg V_T$. Compute the transconductance.
(c) Find the relation between $g_{m,B}$ and $R_{on,R}$ in Fig. 5.43(d) using the above results.

5.25. Determine the corner frequency resulting from C_{in} in Fig. 5.47(d). For simplicity, assume C_1 is a short circuit.

5.26. Determine the supply rejection of the circuit shown in Fig. 5.67.

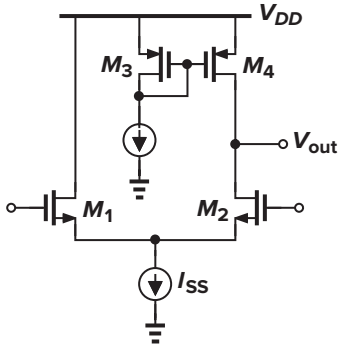


Figure 5.67