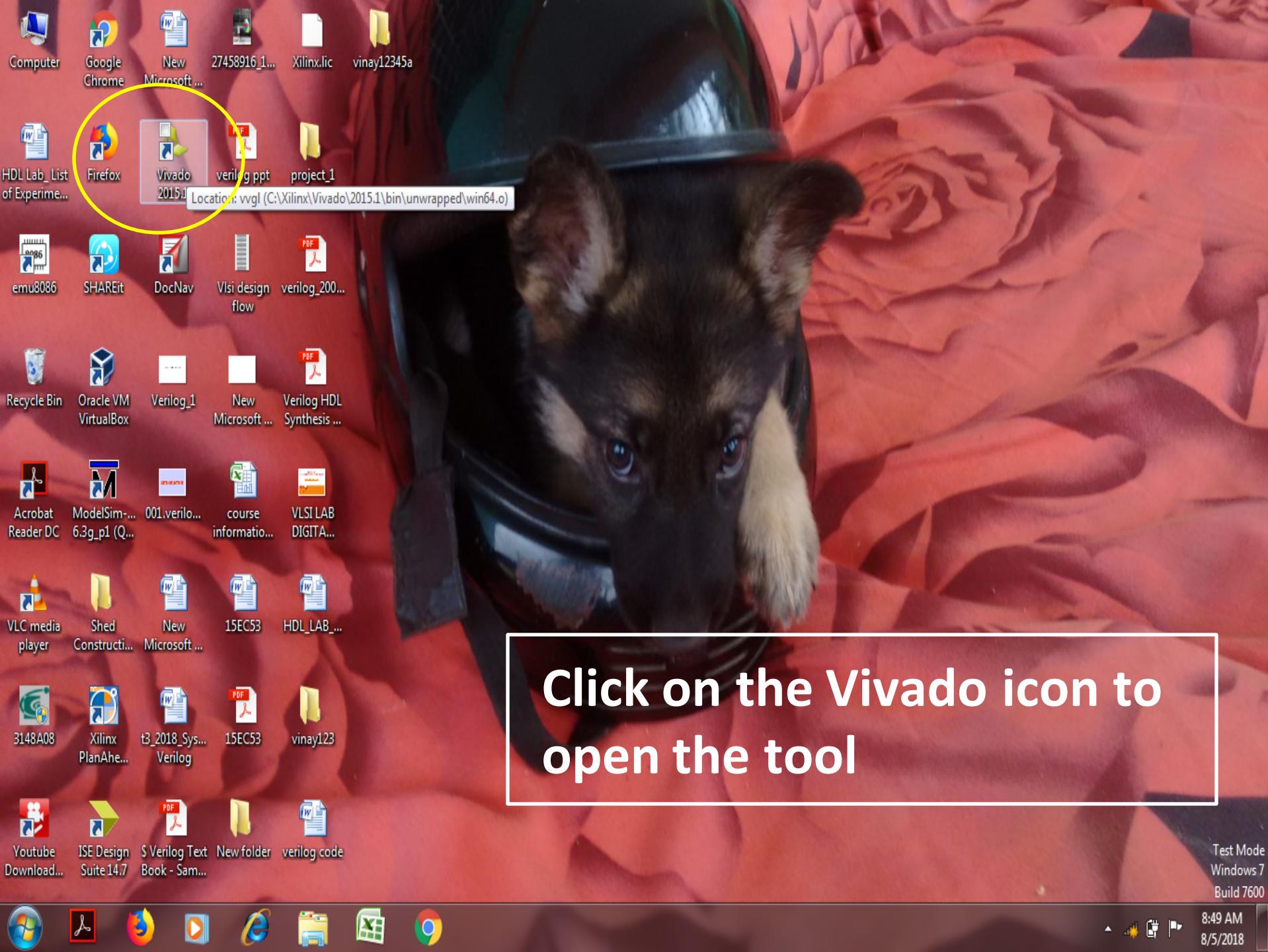


XILINX VIVADO SIMULATION PROCEDURE



Prepared
by
Vinay Reddy
Dept of ECE



Click on the Vivado icon to
open the tool

Computer Google Chrome New Microsoft ...
27458916_1... Xilinx.lic vinay12345a

HDL Lab_List of Experime...
Firefox

emu8086 SHAREit DocNav Vlsi design flow
verilog_200...
Location: vgl (C:\Xilinx\Vivado\2015.1\bin\unwrapped\win64.o)

Recycle Bin Oracle VM VirtualBox Verilog_1 New Microsoft ... Verilog HDL Synthesis ...
Location: C:\Users\vinay\OneDrive\Desktop\Verilog\Verilog_1

Acrobat Reader DC ModelSim... 001.verilo... course informatio... VLSI LAB DIGITA...
6.3g_p1 (Q...) Location: C:\Users\vinay\OneDrive\Desktop\Verilog\001.verilog

VLC media player Shed Construct... New Microsoft ... 15EC53 HDL_LAB_...
Location: C:\Users\vinay\OneDrive\Desktop\Verilog\Shed\15EC53

3148A08 Xilinx PlanAhe... t3_2018_Sys... 15EC53 vinay123
Location: C:\Users\vinay\OneDrive\Desktop\Verilog\t3_2018_Sys...

Youtube Download... ISE Design Suite 14.7 S Verilog Text Book - Sam... New folder verilog code
Location: C:\Users\vinay\OneDrive\Desktop\Verilog\ISE Design Suite 14.7

Test Mode
Windows 7
Build 7600

8:49 AM

8/5/2018





Productivity. Multiplied.

XILINX
ALL PROGRAMMABLE.**Quick Start**

Create New Project



Open Project



Open Example Project

Tasks

Manage IP



Open Hardware Manager



Xilinx Td Store

Information Center

Documentation and Tutorials



Quick Take Videos



Release Notes Guide

Recent Projects

vinay12345a

C:/Users/user/Desktop/vinay12345a

vinay123

C:/Users/user/Desktop/vinay123

project_1

C:/Users/user/Desktop/project_1

vinay

C:/Users/user/vinay

project_1

C:/Users/user/project_1

Create a new project

- Inside your project your verilog file and the other related simulated files, netlist etc will be stored



Productivity

XILINX
ALL PROGRAMMABLE.

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Create a New Vivado Project

This wizard will guide you through the creation of a new project.

To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.

To continue, click Next.

< Back **Next >** Finish Cancel



Tcl Console

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.





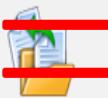
Productivity

XILINX
ALL PROGRAMMABLE.

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

Create project subdirectory

Project will be created at: C:/Users/user/Desktop/project_2

< Back Finish Cancel

Give a name for your project and also set the location where the project folder has to be created



Productivity

XILINX
ALL PROGRAMMABLE.

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

Create project subdirectory

Project will be created at: C:/Users/user/Desktop/vinayreddy

Tcl Console

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.



Productivity

 XILINX
ALL PROGRAMMABLE.

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Project Type
Specify the type of project to create.

RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
 Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
 Do not specify sources at this time

I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.

Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project
Create a new Vivado project from a predefined template.

< Back **Next >** **Finish** **Cancel**

Tcl Console

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.





Productivity

XILINX
ALL PROGRAMMABLE.

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Add Sources

Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Press the + button to Add Files, Add Directories or Create File

+
 ↑ ↓

Scan and add RTL include files into project
 Copy sources into project
 Add sources from subdirectories

Target language: Verilog Simulator language: Verilog

< Back Next > Finish Cancel

Tcl Console

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.



Productivity

XILINX
ALL PROGRAMMABLE.

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Add Sources

Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Press the button to Add Files, Add Directories or Create File

Add
Add or create source file.

Scan and add RTL include files into project
 Copy sources into project
 Add sources from subdirectories

Target language: Verilog Simulator language: Verilog

< Back Next > Finish Cancel

Tcl Console

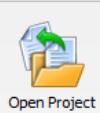
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.



Productivity

XILINX
ALL PROGRAMMABLE.**Quick Start**

Create New Project



Open Project

Tasks

Manage IP



Open Hardware Manager

Information Center

Documentation and Tutorials



Quick Take Videos

New Project**Add Sources**

Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

- [Add Files...](#)
- [Add Directories...](#)
- [Create File...](#)

Press the button to Add Files, Add Directories or Create File

 Scan and add RTL include files into project Copy sources into project Add sources from subdirectoriesTarget language: VerilogSimulator language: Verilog

< Back

Next >

Finish

Cancel

Tcl Console





Productivity

XILINX
ALL PROGRAMMABLE.

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Add Sources

Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Press the button to Add Files, Add Directories or Create File

Add Files...
 Add Directories...
Create File...

Scan and add RTL include files into project
 Copy sources into project
 Add sources from subdirectories

Target language: Verilog Simulator language: Verilog

< Back Next > Finish Cancel

Tcl Console

Create a new source file on disk and add it to your project



Productivity

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Add Sources

Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Create Source File

Create a new source file and add it to your project.

File type: Verilog

File name:

File location: <Local to Project>

OK Cancel

Scan and add RTL include files into project

Copy sources into project

Add sources from subdirectories

Target language: Verilog Simulator language: Verilog

< Back Next > Finish Cancel

XILINX
ALL PROGRAMMABLE.

ay12345a

ay123

ject_1



Productivity

XILINX
ALL PROGRAMMABLE.

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Add Sources

Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Create Source File

Create a new source file and add it to your project.

File type: Verilog

File name: inverter

File location: <Local to Project>

OK Cancel

Scan and add RTL include files into project

Copy sources into project

Add sources from subdirectories

Target language: Verilog Simulator language: Verilog

< Back Next > Finish Cancel

ay12345a

ay123

ject_1



Productivity

XILINX
ALL PROGRAMMABLE.

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Add Sources

Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

	Index	Name	Library	HDL Source For	Location
	1	inverter.v	xil_defaultlib	Synthesis & Simulation	<Local to Project>

Scan and add RTL include files into project
 Copy sources into project
 Add sources from subdirectories

Target language: Verilog Simulator language: Verilog

[< Back](#) [Next >](#) [Finish](#) [Cancel](#)

Tcl Console

Create a new source file on disk and add it to your project





Productivity

XILINX
ALL PROGRAMMABLE.

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Add Existing IP (optional)

Specify existing configurable IP, DSP composite, and Embedded sub-design files to add to your project.

Press the button to Add Files or Add Directories

Copy sources into project

< Back Next > Finish Cancel

Tcl Console

Create a new source file on disk and add it to your project



9:01 AM

8/5/2018



Productivity

XILINX
ALL PROGRAMMABLE.

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Add Constraints (optional)

Specify or create constraint files for physical and timing constraints.

Press the button to Add Files or Create File

Copy constraints files into project

< Back Next > Finish Cancel

Tcl Console

Create a new source file on disk and add it to your project



9:02 AM

8/5/2018



Productivity

XILINX
ALL PROGRAMMABLE.

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: **Parts** Boards

Filter

Product category: All Package: All
Family: All Speed grade: All
Sub-Family: All Temp grade: All
Revision: All

Reset All Filters

Search: Q

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	DSPs	Gb Transceivers	Clock Cells
xc7vx485ffg1157-2L	1,157	600	303600	607200	1030	2800	20	2
xc7vx485ffg1157-1	1,157	600	303600	607200	1030	2800	20	2
xc7vx485ffg1158-3	1,158	350	303600	607200	1030	2800	48	4
xc7vx485ffg1158-2	1,158	350	303600	607200	1030	2800	48	4
xc7vx485ffg1158-2L	1,158	350	303600	607200	1030	2800	48	4
xc7vx485ffg1158-1	1,158	350	303600	607200	1030	2800	48	4
xc7vx485ffg1761-3	1,761	700	303600	607200	1030	2800	28	2

< Back Next > Finish Cancel

Tcl Console

Create a new source file on disk and add it to your project





Productivity

XILINX
ALL PROGRAMMABLE.

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: Parts Boards

Filter

Vendor: All

Display Name: All

Board Rev: Latest

Reset All Filters

Search:

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Available IOBs
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1	484	1.3	200
Artix-7 AC701 Evaluation Platform	xilinx.com	1.1	xc7a200tfg676-2	676	1.2	400
Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	xc7k325tffg900-2	900	1.2	500
Kintex-Ultrascale KCU105 Evaluation Platform	xilinx.com	1.0	xcu040-ffva1156-2-e	1,156	1.0	520
Virtex-7 VC707 Evaluation Platform	xilinx.com	1.1	xc7vx48tffg1761-2	1,761	1.2	700
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2	1,761	1.6	850
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.2	200
ZYNQ-7 ZC706 Evaluation Board	xilinx.com	1.1	xc7z045ffg900-2	900	1.2	362

< Back Next > Finish Cancel

Tcl Console

Create a new source file on disk and add it to your project



Productivity

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: Parts Boards

Filter

Vendor: All

Display Name: All

Board Rev: Latest

Reset All Filters

Search: Q

Display Name	Vendor	Board Rev	Part	I/O Pins	Cloud	File Version	Train	Jobs
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	1.0	xc7z020clg484-1	484	1.3	200		
Artix-7 AC201 Evaluation Platform	xilinx.com	1.1	xc7a200tfgb676-2	676	1.2	400		
Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	xc7k325tffg900-2	900	1.2	500		
Kintex-Ultrascale KCU105 Evaluation Platform	xilinx.com	1.0	xcu040-ffva1156-2-e	1,156	1.0	520		
Virtex-7 VC707 Evaluation Platform	xilinx.com	1.1	xc7vx485tffg1761-2	1,761	1.2	700		
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2	1,761	1.6	850		
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.2	200		
ZYNQ-7 ZC706 Evaluation Board	xilinx.com	1.1	xc7z045ffg900-2	900	1.2	362		

< Back Next > Finish Cancel

Next Page

I am supposed to select the basys 3 board, since the board file is not installed in my laptop. I have randomly chosen Zedboard



Productivity

Quick Start



Create New Project



Open Project

Tasks



Manage IP



Open Hardware Manager

Information Center



Documentation and Tutorials



Quick Take Videos

New Project

New Project Summary

A new RTL project named 'vinayreddy' will be created.

1 source file will be added.

No Configurable IP files will be added. Use Add Sources to add them later.

No constraints files will be added. Use Add Sources to add them later.

The default part and product family for the new project:
Default Board: ZedBoard Zynq Evaluation and Development Kit
Default Part: xc7z020clg484-1
Product: Zynq-7000
Family: Zynq-7000
Package: clg484
Speed Grade: -1

To create the project, click Finish

< Back Next > Finish Cancel

 XILINX
ALL PROGRAMMABLE.

ay12345a

ay123

ject_1



Productivity. Multiplied.

XILINX
ALL PROGRAMMABLE.**Quick Start**

Create New Project



Open Project



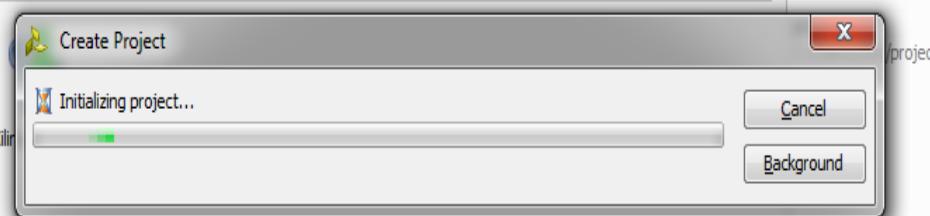
Open Example Project

Tasks

Manage IP



Open Hardware Manager

**Information Center**

Documentation and Tutorials



Quick Take Videos



Release Notes Guide

Project Manager - vinayreddy

Sources Project Summary X

Project part: ZedBoard Zyng Evaluation and Development Kit (xc7z020clq484-1)

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name: inverter

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
input	input		0	0

OK Cancel

Updating Hierarchy... Constraints

Hierarchy Libraries | Compil Sources Templates

Properties

Select an item

Design Runs

Name

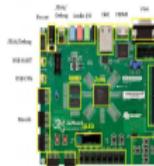
synth_1
impl_1

Tcl Console Messages Log Reports Design Runs

Implementation

Status: Not started
Messages: No errors or warnings

LUT % LUTs FF % FFs BRAM % BRAMs DSP %



* All memory and IP blocks are not visible on board.

Project Manager - vinayreddy

Sources Project Summary X

Project part: ZedBoard Zyng Evaluation and Development Kit (xc7z020clq484-1)

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name: inverter

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
a	input	<input type="checkbox"/>	0	0
b	output	<input type="checkbox"/>	0	0

OK Cancel

Updating Hierarchy... Constraints

Hierarchy Libraries | Compil Sources Templates

Properties

Select an item

Design Runs

Name

synth_1
impl_1

Tcl Console Messages Log Reports Design Runs

Implementation

Status: Not started
Messages: No errors or warnings

LUT % LUTs FF % FFs BRAM % BRAMs DSP %



Project Manager - vinayreddy

Sources

- Design Sources (1)
 - inverter (inverter.v)
- Constraints
- Simulation Sources (1)

Hierarchy Libraries Compile Order

Sources Templates

Properties

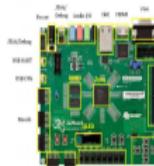
Select an object to see properties

Project Summary

Project part: ZedBoard Zynq Evaluation and Development Kit (xc7z020clg484-1)
 Top module name: inverter

Board Part

Display name: ZedBoard Zynq Evaluation and Development Kit
 Board part name: em.avnet.com:zed:part0:1.3
 Repository path: C:/Xilinx/Vivado/2015.1/data/boards/board_files
 URL: <http://www.zedboard.org>
 Board overview: ZedBoard Zynq Evaluation and Development Kit



* MicroSD and WiFi module not included on board.

Synthesis

Status: Not started
 Messages: No errors or warnings

Implementation

Status: Not started
 Messages: No errors or warnings

Design Runs

Name	Constraints	Status	Progress	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT %	LUTs	FF %	FFs	BRAM %	BRAMs	DSP %
synth_1	constrs_1	Not started	0%													
impl_1	constrs_1	Not started	0%													

Tcl Console Messages Log Reports Design Runs





Flow Navigator

Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

IP Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

Run Simulation

RTL Analysis

Elaboration Settings

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Des

Implementation

Implementation Setting

Run Implementation

Open Implemented Des

Project Manager - vinayreddy

Sources

- Design Sources (1)
 - inverter (inverter.v)
- Constraints
- Simulation Sources (1)

Project Summary X inverter.v X

```
C:/Users/user/Desktop/vinayreddy/vinayreddy.srcts/sources_1/new/inverter.v
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////
21 //
22 //
23 module inverter(
24     input a,
25     output b
26 );
27 endmodule
28
```

Hierarchy Libraries Cor

Sources Templates

Design Runs

Name	Constraints	Status	Progress	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT %	LUTs	FF %	FFs	BRAM %	BRAMs	DSP %
synth_1	constrs_1	Not started	0%													
	impl_1	constrs_1	Not started													

Tcl Console Messages Log Reports Design Runs

23:0

Insert

Verilog





Flow Navigator

Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

IP Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

Run Simulation

RTL Analysis

Elaboration Settings

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Des

Implementation

Implementation Setting

Run Implementation

Open Implemented Des

Project Manager - vinayreddy

Sources

- Design Sources (1)
 - inverter (inverter.v)
- Constraints
- Simulation Sources (1)

Project Summary X inverter.v *

C:/Users/user/Desktop/vinayreddy/vinayreddy.srcc/sources_1/new/inverter.v

```
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////
21 //
22 //
23 module inverter(
24     input a,
25     output b
26 );
27     assign b = ~a;
28 endmodule
29
```

Sources Libraries Templates

Design Runs

Name	Constraints	Status	Progress	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT %	LUTs	FF %	FFs	BRAM %	BRAMs	DSP %
synth_1	constrs_1	Not started	<div style="width: 0%;">0%</div>													
	impl_1	constrs_1	Not started	<div style="width: 0%;">0%</div>												

Tcl Console Messages Log Reports Design Runs





Flow Navigator

Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

IP Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

Run Simulation

RTL Analysis

Elaboration Settings

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Des

Implementation

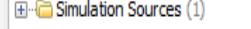
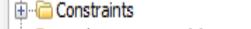
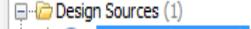
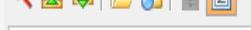
Implementation Setting

Run Implementation

Open Implemented Des

Project Manager - vinayreddy

Sources



Default Layout

Project Summary X inverter.v *

C:/Users/user/Desktop/vinayreddy/vinayreddy.srcc/sources_1/new/inverter.v

13 //

Save File (Ctrl+S)
Save changes to the current file.

16 // Revision:

17 // Revision 0.01 - File Created

18 // Additional Comments:

19 //

20 ////////////////////////////////

21 //

22 //

23 module inverter(

24 input a,

25 output b

26);

27 assign b = ~a;

28 endmodule

29 //

Hierarchy Libraries Cor

Sources Templates

Design Runs

Name	Constraints	Status	Progress	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT %	LUTs	FF %	FFs	BRAM %	BRAMs	DSP %
synth_1	constrs_1	Not started	0%													
	impl_1	constrs_1	Not started													

Tcl Console Messages Log Reports Design Runs

Save changes to the current file

27:13

Insert

Verilog



Flow Navigator

Project Manager - vinayreddy

Sources

Project Summary X inverter.v X

C:/Users/user/Desktop/vinayreddy/vinayreddy.srcc/sources_1/new/inverter.v

```
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////
21 //
22 //
23 module inverter(
24     input a,
25     output b
26 );
27     assign b = ~a;
28 endmodule
29
```

Hierarchy Libraries Cor > Sources Templates

Run Simulation Vivado Simulator. on Runs

Name	Constraints	Status	Progress	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT %	LUTs	FF %	FFs	BRAM %	BRAMs	DSP %
synth_1	constrs_1	Not started	0%													
	impl_1	constrs_1	Not started													

Tcl Console Messages Log Reports Design Runs

Flow Navigator

Project Manager - vinayreddy

Sources

Project Summary X inverter.v X

C:/Users/user/Desktop/vinayreddy/vinayreddy.srcc/sources_1/new/inverter.v

```
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////
21
22
23 module inverter(
24     input a,
25     output b
26 );
27     assign b = ~a;
28 endmodule
29
```

Run Behavioral Simulation

Run Post-Synthesis Functional Simulation

Run Post-Synthesis Timing Simulation

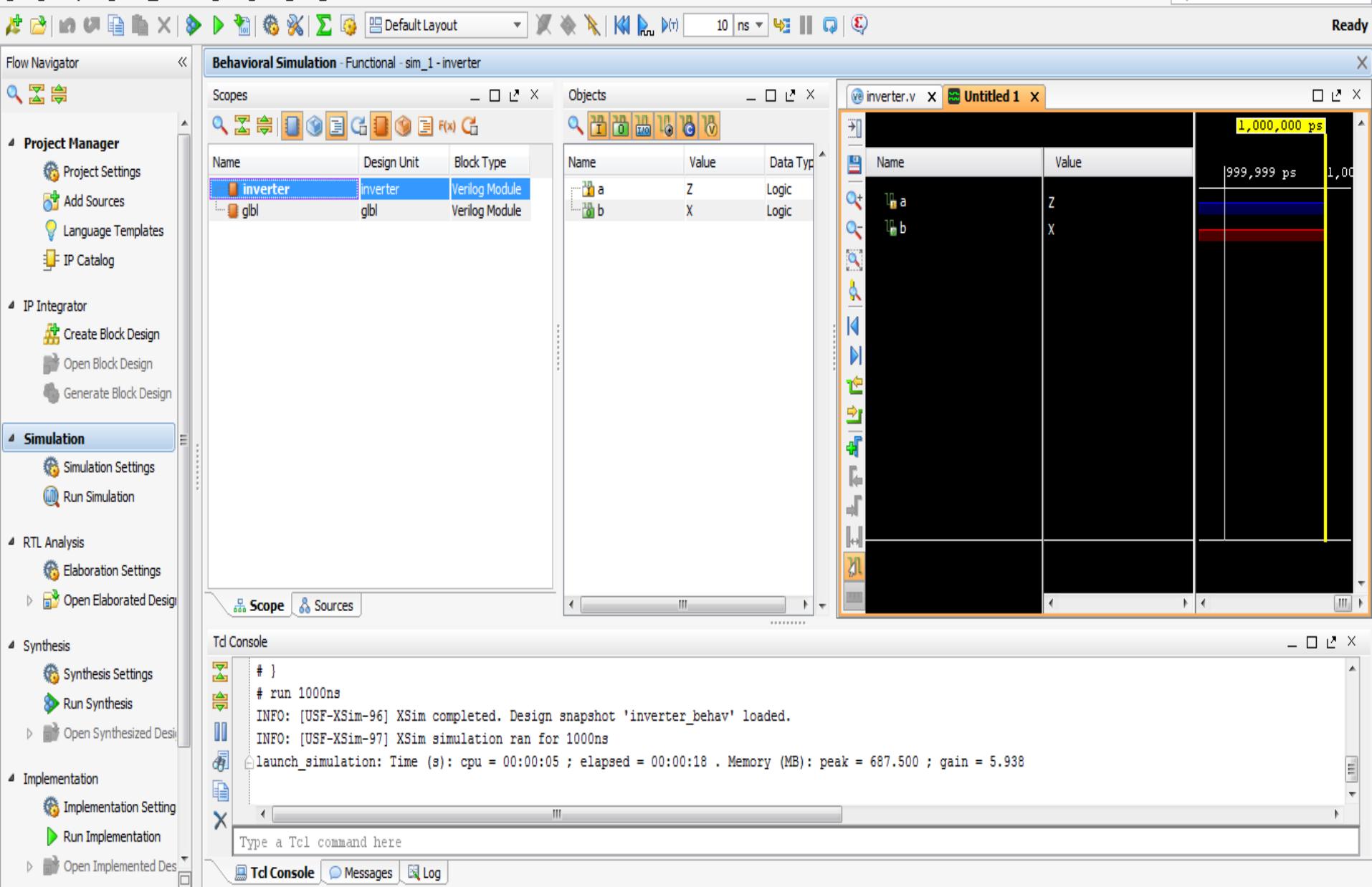
Run Post-Implementation Functional Simulation

Run Post-Implementation Timing Simulation

Constraints Status Progress WNS TNS WHS THS TPWS Failed Routes LUT % LUTs FF % FFs BRAM % BRAMs DSP %

constrs_1	Not started	0%													
constrs_1	Not started	0%													

Tcl Console Messages Log Reports Design Runs



Flow Navigator

Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

IP Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

RTL Analysis

- Elaboration Settings
- Open Elaborated Design

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Setting
- Run Implementation
- Open Implemented Design

Behavioral Simulation - Functional - sim_1 - inverter

Scopes Objects

inverter.v Untitled 1

inverter.v

Name	Value	Data Type
a	Z	Logic
b	X	Logic

inverter.v

Name	Value
a	Z
b	X

Scope Sources

Tcl Console

```
# }
# run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'inverter_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:18 . Memory (MB): peak = 687.500 ; gain = 5.938
```

Type a Tcl command here

Tcl Console Messages Log

Sim Time: 1 us

Flow Navigator

Project Manager - vinayreddy

Sources

- Design Sources (1) **inverter (inverter.v)**
- Constraints
- Simulation Sources (1)

Project Summary X inverter.v X

C:/Users/user/Desktop/vinayreddy/vinayreddy.srsc/sources_1/new/inverter.v

```
14 // Dependencies:  
15 //  
16 // Revision:  
17 // Revision 0.01 - File Created  
18 // Additional Comments:  
19 //  
20 ///////////////////////////////////////////////////////////////////  
21  
22//  
23 module inverter(  
24     input a,  
25     output b  
26 );  
27     assign b = ~a;  
28 endmodule  
29
```

Hierarchy Libraries Cor > Sources Templates

Log

```
Starting static elaboration  
Completed static elaboration  
Starting simulation data flow analysis  
Completed simulation data flow analysis  
Time Resolution for simulation is 1ps  
Compiling module xil_defaultlib.inverter  
Compiling module xil_defaultlib.glbl  
Waiting for 3 sub-compilation(s) to finish...  
Built simulation snapshot inverter_behav
```

Synthesis | Implementation | **Simulation**

Tcl Console Messages Log Reports Design Runs

Flow Navigator

Project Manager - vinayreddy

Sources Default Layout

Project Summary X inverter.v X

C:/Users/user/Desktop/vinayreddy/vinayreddy.srsc/sources_1/new/inverter.v

14 // Dependencies:
15 //
16 // Revision:
17 // File Created
18 // Additional Comments:
19 module inverter(
20 input a,
21 output b
22);
23
24 assign b = ~a;
25 endmodule
26
27
28
29

Properties... Ctrl+E
Hierarchy Update
Refresh Hierarchy
IP Hierarchy
Edit Constraints Sets...
Edit Simulation Sets...
Add Sources... Alt+A

Hierarchy Libraries Cor

Sources Templates

Log

Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.inverter
Compiling module xil_defaultlib.glbl
Waiting for 3 sub-compilation(s) to finish...
Built simulation snapshot inverter_behav

Synthesis Implementation Simulation

Tcl Console Messages Log Reports Design Runs

Specify and/or create source files to add to the project





Flow Navigator

Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

IP Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

Run Simulation

RTL Analysis

Elaboration Settings

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Design

Implementation

Implementation Setting

Run Implementation

Open Implemented Design

Project Manager - vinayreddy

Sources

Add Sources



Add Sources

This guides you through the process of adding and creating sources for your project

- Add or create constraints
- Add or create design sources
- Add or create simulation sources
- Add or create DSP sources
- Add existing block design sources
- Add existing IP

To continue, click Next

< Back

Next >

Finish

Cancel

Synthesis | Implementation | **Simulation**

Tcl Console | Messages | Log | Reports | Design Runs

Specify and/or create source files to add to the project



Project Manager - vinayreddy

Sources

Add Sources

Design Constraints Simulation

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set: sim_1

Press the + button to Add Files, Add Directories or Create File

Hierarchy

Sources

Log

Starting... Completed Starting... Completed Time Remaining Compiling Compiling Waiting Built

Scan and add RTL include files into project
 Copy sources into project
 Add sources from subdirectories
 Include all design sources for simulation

< Back Next > Finish Cancel

Synthesis | Implementation | **Simulation**

Tcl Console Messages Log Reports Design Runs

Specify and/or create source files to add to the project



Flow Navigator

Project Manager - vinayreddy

Sources

Add Sources

Design Constraints Simulation

Specify simulation set: sim_1

Add Files... Add Directories... Create File...

Hierarchy

Log

Starting Completed Starting Completed Time Remaining Compiling Compiling Waiting Built

Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation

< Back Next > Finish Cancel

Synthesis | Implementation | **Simulation**

Tcl Console Messages Log Reports Design Runs

Create a new source file on disk and add it to your project

Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

IP Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

RTL Analysis

- Elaboration Settings
- Open Elaborated Design

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Setting
- Run Implementation
- Open Implemented Design

Default Layout

Ready



Flow Navigator

Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

IP Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

RTL Analysis

- Elaboration Settings
- Open Elaborated Design

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Setting
- Run Implementation
- Open Implemented Design

Project Manager - vinayreddy

Sources

Add Sources

Design Sources

Constraints

Simulations

Hierarchy

Sources

Log

Starting

Completed

Starting

Completed

Time Re

Compili

Compili

Waiting

Built

Scan and add RTL include files into project

Copy sources into project

Add sources from subdirectories

Include all design sources for simulation

Create Source File

Create a new source file and add it to your project.

File type: Verilog

File name: inverter_tb

File location: <Local to Project>

OK Cancel

< Back Next > Finish Cancel

Synthesis | Implementation | **Simulation**

Tcl Console Messages Log Reports Design Runs

Create a new source file on disk and add it to your project



Flow Navigator

Project Manager - vinayreddy

Sources

Add Sources

Design Sources

Constraints

Simulation Sources

Add or Create Simulation Sources

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set: sim_1

	Index	Name	Library	Location
	1	inverter_tb.v	xil_defaultlib	<Local to Project>

Hierarchy

Sources

Log

Starting

Completed

Starting

Completed

Time Re

Compili

Compili

Waiting

Built

Scan and add RTL include files into project

Copy sources into project

Add sources from subdirectories

Include all design sources for simulation

< Back Next > Finish Cancel

Synthesis | Implementation | **Simulation**

Tcl Console Messages Log Reports Design Runs

Create a new source file on disk and add it to your project



Flow Navigator

Project Manager - vinayreddy

Sources Project Summary inverter.v C:/Users/user/Desktop/vinayreddy/vinayreddy.srcts/sources_1/new/inverter.v

Updating Hierarchy... Design Sources (1) inverter Constraints Simulation Sources (1)

Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

IP Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

RTL Analysis

- Elaboration Settings
- Open Elaborated Design

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Setting
- Run Implementation
- Open Implemented Design

Default Layout

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name: inverter_tb

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
input	input		0	0

Hierarchy Libraries Coriolis Sources Templates

Log

- Starting static elaboration
- Completed static elaboration
- Starting simulation
- Completed simulation
- Time Resolution for
- Compiling module xil...
- Compiling module xil...
- Waiting for 3 sub-compilation(s) to finish...
- Built simulation snapshot inverter_behav

OK Cancel

Synthesis | Implementation | **Simulation**

Tcl Console Messages Log Reports Design Runs

Flow Navigator

Project Manager - vinayreddy

Sources Project Summary inverter.v C:/Users/user/Desktop/vinayreddy/vinayreddy.srcts/sources_1/new/inverter.v

Updating Hierarchy... Design Sources (1) inverter Constraints Simulation Sources (1)

Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

IP Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

RTL Analysis

- Elaboration Settings
- Open Elaborated Design

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Setting
- Run Implementation
- Open Implemented Design

Default Layout

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name: inverter_tb

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
a	input	<input type="checkbox"/>	0	0
b	output	<input type="checkbox"/>	0	0

OK Cancel

Log

- Starting static elaboration
- Completed static elaboration
- Starting simulation
- Completed simulation
- Time Resolution for
- Compiling module xil...
- Compiling module xil...
- Waiting for 3 sub-compilation(s) to finish...
- Built simulation snapshot inverter_behav

Simulation

Tcl Console Messages Log Reports Design Runs

9:12 AM 8/5/2018



Flow Navigator

Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

IP Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

Run Simulation

RTL Analysis

Elaboration Settings

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Des

Implementation

Implementation Setting

Run Implementation

Open Implemented Des

Project Manager - vinayreddy

Sources

- Design Sources (1)
 - inverter (inverter.v)
- Constraints
- Simulation Sources (2)
 - sim_1 (2)
 - inverter (inverter.v)
 - inverter_tb (inverter_tb)

Project Summary X inverter.v X

C:/Users/user/Desktop/vinayreddy/vinayreddy.srsc/sources_1/new/inverter.v

```
14 // Dependencies:  
15 //  
16 // Revision:  
17 // Revision 0.01 - File Created  
18 // Additional Comments:  
19 //  
20 ///////////////////////////////  
21  
22 //  
23 module inverter(  
24     input a,  
25     output b  
26 );  
27     assign b = ~a;  
28 endmodule  
29
```

Hierarchy Libraries Cor Sources Templates

Log

```
Starting static elaboration  
Completed static elaboration  
Starting simulation data flow analysis  
Completed simulation data flow analysis  
Time Resolution for simulation is 1ps  
Compiling module xil_defaultlib.inverter  
Compiling module xil_defaultlib.glbl  
Waiting for 3 sub-compilation(s) to finish...  
Built simulation snapshot inverter_behav
```

Synthesis | Implementation | **Simulation**

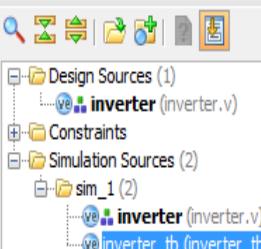
Tcl Console Messages Log Reports Design Runs





Project Manager - vinayreddy

Sources



Project Summary | inverter.v | inverter_tb.v

```
8 // Module Name: inverter_tb
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
```

```
23 module inverter_tb(
```

```
[I] Starting static elaboration
[!] Completed static elaboration
[!] Starting simulation data flow analysis
[!] Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.inverter
Compiling module xil_defaultlib.glbl
Waiting for 3 sub-compilation(s) to finish...
Built simulation snapshot inverter behav
```



23:

Insert

Insert | Verilog



Flow Navigator

Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

IP Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

Run Simulation

RTL Analysis

Elaboration Settings

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Design

Implementation

Implementation Setting

Run Implementation

Open Implemented Design

Project Manager - vinayreddy

Sources

- Design Sources (1)
 - inverter (inverter.v)
- Constraints
- Simulation Sources (2)
 - sim_1 (2)
 - inverter (inverter.v)
 - inverter_tb (inverter_tb)

Project Summary X inverter.v X inverter_tb.v *

C:/Users/user/Desktop/vinayreddy/vinayreddy.srscs/sim_1/new/inverter_tb.v

```
21
22
23 module inverter_tb;
24   wire b;
25   reg a;
26   inverter i1(b,a);
27   initial
28   begin
29     a=1'b0;
// 30   #10 a=1'b1;
31   #10 a=1'bX;
32   #10 a= 1'bZ;
33   end
34
35 endmodule
36
```

- Hierarchy
- Libraries
- Cor
-

- Sources
- Templates

Log

```
Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.inverter
Compiling module xil_defaultlib.glbl
Waiting for 3 sub-compilation(s) to finish...
Built simulation snapshot inverter_behav
```

- Synthesis
- Implementation
- Simulation

- Tcl Console
- Messages
- Log
- Reports
- Design Runs

36:0

Insert

Verilog

9:14 AM

8/5/2018



Flow Navigator

Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

IP Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

Run Simulation

RTL Analysis

Elaboration Settings

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Des

Implementation

Implementation Setting

Run Implementation

Open Implemented Des

Project Manager - vinayreddy

Sources

- Design Sources (1)
 - inverter (inverter.v)
- Constraints
- Simulation Sources (2)
 - sim_1 (2)
 - inverter (inverter.v)
 - inverter_tb (inverter_tb)

Project Summary X inverter.v X inverter_tb.v *

C:/Users/user/Desktop/vinayreddy/vinayreddy.srscs/sim_1/new/inverter_tb.v

21

Save File (Ctrl+S)
Save changes to the current file.

```
24    wire b;
25    reg a;
26    inverter i1(b,a);
27    initial
28    begin
29      a=1'b0;
// 30      #10 a=1'b1;
31      #10 a=1'bx;
32      #10 a= 1'bz;
33    end
34
35 endmodule
36
```

Hierarchy Libraries Cor**Sources** Templates

Log

```
Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.inverter
Compiling module xil_defaultlib.glbl
Waiting for 3 sub-compilation(s) to finish...
Built simulation snapshot inverter_behav
```

Simulation

Tcl Console Messages Log Reports Design Runs

Save changes to the current file

36:0

Insert

Verilog

9:18 AM

8/5/2018



Flow Navigator

Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

IP Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

Run Simulation

RTL Analysis

Elaboration Settings

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Des

Implementation

Implementation Setting

Run Implementation

Open Implemented Des

Project Manager - vinayreddy

Sources

- Design Sources (1)
 - inverter (inverter.v)
- Constraints
- Simulation Sources (1)
 - sim_1 (1)
 - inverter_tb (inverter_tb.v)
 - i1 - inverter (inverte

Project Summary

C:/Users/user/Desktop/vinayreddy/vinayreddy.srscs/sim_1/new/inverter_tb.v

```
21
22
23 module inverter_tb;
24   wire b;
25   reg a;
26   inverter i1(b,a);
27   initial
28   begin
29     a=1'b0;
// 30   #10  a=1'b1;
31   #10  a=1'bX;
32   #10  a= 1'bZ;
33   end
34
35 endmodule
36
```

Sources**Templates**

Log

```
Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.inverter
Compiling module xil_defaultlib.glbl
Waiting for 3 sub-compilation(s) to finish...
Built simulation snapshot inverter_behav
```

Simulation**Tcl Console****Messages****Log****Reports****Design Runs**



Flow Navigator

Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

IP Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

Run Simulation

Simulation Settings
Open simulation settings to change options.

RTL Analysis

Elaboration Settings

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Design

Implementation

Implementation Setting

Run Implementation

Open Implemented Design

Project Manager - vinayreddy

Sources

- Design Sources (1)
 - inverter (inverter.v)
- Constraints
- Simulation Sources (1)
 - sim_1 (1)
 - inverter_tb (inverter_tb.v)
 - i1 - inverter (inverte

Project Summary

C:/Users/user/Desktop/vinayreddy/vinayreddy.srscs/sim_1/new/inverter_tb.v

```
21
22
23 module inverter_tb;
24   wire b;
25   reg a;
26   inverter i1(b,a);
27   initial
28   begin
29     a=1'b0;
// 30   #10  a=1'b1;
31   #10  a=1'bX;
32   #10  a= 1'bZ;
33   end
34
35 endmodule
36
```

Log

```
Starting static elaboration
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.inverter
Compiling module xil_defaultlib.glbl
Waiting for 3 sub-compilation(s) to finish...
Built simulation snapshot inverter_behav
```

Synthesis | Implementation | **Simulation**

Tcl Console | Messages | Log | Reports | Design Runs

Open simulation settings to change options

Project Manager - vinayreddy

Sources

- Design Sources (1)
 - inverter (inverter)
- Constraints
- Simulation Sources (1)
 - sim_1 (1)
 - inverter_tb (inverter_tb)
 - i1 - inverter (i1 - inverter)

Simulation

Target simulator: Vivado Simulator

Simulator language: Verilog

Simulation set: sim_1

Simulation top module name: inverter_tb

Clean up simulation files

Generate scripts only

Verilog options:

Generics/Parameters options:

xsim.compile.xvhdl.nosort

xsim.compile.xvlog.relax

xsim.compile.xvhdl.relax

xsim.compile.xvlog.more_options

xsim.compile.xvhdl.more_options

Select an option above to see a description of it

OK Cancel Apply

Flow Navigator

Project Manager - vinayreddy

Sources

Design Sources (1) inverter (inverter.v)

Constraints

Simulation Sources (1) sim_1 (1) inverter_tb (inverter_tb.v)

Project Summary inverter.v inverter_tb.v

C:/Users/user/Desktop/vinayreddy/vinayreddy.srscs/sim_1/new/inverter_tb.v

```
21
22
23 module inverter_tb;
24   wire b;
25   reg a;
26   inverter i1(b,a);
27   initial
28   begin
29     a=1'b0;
30     #10 a=1'b1;
31     #10 a=1'bx;
32     #10 a= 1'bz;
33   end
34
35 endmodule
36
```

Run Behavioral Simulation

Run Post-Synthesis Functional Simulation

Run Post-Synthesis Timing Simulation

Run Post-Implementation Functional Simulation

Run Post-Implementation Timing Simulation

Completed simulation data flow analysis

Time Resolution for simulation is 1ps

Compiling module xil_defaultlib.inverter

Compiling module xil_defaultlib.glbl

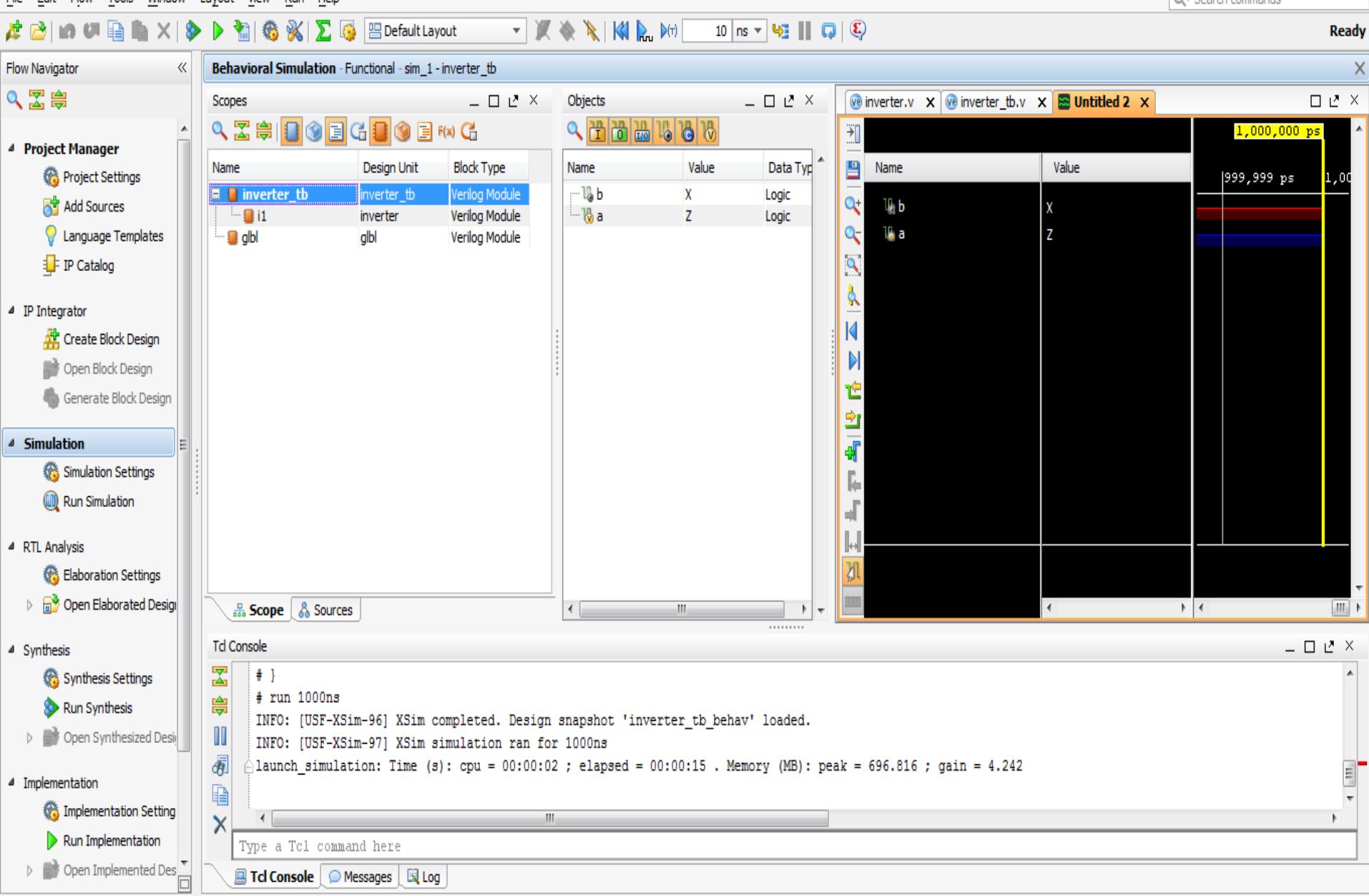
Waiting for 3 sub-compilation(s) to finish...

Built simulation snapshot inverter_behav

Synthesis | Implementation | **Simulation**

Tcl Console Messages Log Reports Design Runs





Flow Navigator

Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

IP Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

RTL Analysis

- Elaboration Settings
- Open Elaborated Design

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Setting
- Run Implementation
- Open Implemented Design

Behavioral Simulation - Functional - sim_1 - inverter_tb

Scopes Objects

Name Design Unit

Name	Design Unit
inverter_tb	inverter_tb
i1	inverter
gbl	gbl

Name Value

Name	Value
b	X
a	Z

Run for 10ns (Shift+F2)
Runs the simulation for the amount of time previously set with the 'Run For...' dialog.

1,000,000 ps

1,000,000 ps

1,000,001 ps

1,000,002 ps

Td Console

```
# }
# run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'inverter_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:15 . Memory (MB): peak = 696.816 ; gain = 4.242
```

Type a Tcl command here

Tcl Console Messages Log

Runs the simulation for the amount of time previously set with the 'Run For...' dialog

Sim Time: 1 us

Flow Navigator

Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

IP Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

RTL Analysis

- Elaboration Settings
- Open Elaborated Design

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Setting
- Run Implementation
- Open Implemented Design

Behavioral Simulation - Functional - sim_1 - inverter_tb

Scopes Objects

inverter.v x inverter_tb.v x Untitled 2 x

Name Design Unit

Name	Design Unit
inverter_tb	inverter_tb
i1	inverter
gbl	gbl

Name Value

Name	Value
b	X
a	Z

Zoom Fit

Scope Sources

Td Console

```
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:15 . Memory (MB): peak = 696.816 ; gain = 4.242
run 10 ns
run 10 ns
run all
```

Type a Tcl command here

Tcl Console Messages Log

Zoom Fit

Sim Time: 1020 ns

9:23 AM
8/5/2018

Flow Navigator

Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

IP Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

RTL Analysis

- Elaboration Settings
- Open Elaborated Design

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Setting
- Run Implementation
- Open Implemented Design

Behavioral Simulation - Functional - sim_1 - inverter_tb

Scopes Objects

inverter.v x inverter_tb.v x Untitled 2 x

inverter_tb

Name	Design Unit
inverter_tb	inverter_tb
i1	inverter
gbl	gbl

inverter_tb

Name	Value
b	X
a	Z

inverter_tb

Name	Value
b	0
a	1

10.000 ns

Scope Sources

Td Console

```
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:15 . Memory (MB): peak = 696.816 ; gain = 4.242
run 10 ns
run 10 ns
run all
```

Type a Tcl command here

Tcl Console Messages Log

Sim Time: 1020 ns



Flow Navigator

Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

IP Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

Run Simulation

RTL Analysis

Elaboration Settings

RTL Analysis

Show/Hide RTL Analysis actions

Switch to RTL Analysis environment (when enabled/bold).

Synthesis

Synthesis Settings

Run Synthesis

Implementation

Implementation Setting

Run Implementation

Open Implemented Des

Project Manager - vinayreddy

Sources

Design Sources (1)

inverter (inverter.v)

Constraints

Simulation Sources (1)

sim_1 (1)

inverter_tb (inverte
r_tb.v)

Project Summary X inverter.v X inverter_tb.v X

C:/Users/user/Desktop/vinayreddy/vinayreddy.srscs/sim_1/new/inverter_tb.v

```
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////
21
22
23 module inverter_tb;
24     wire b;
25     reg a;
26     inverter i1(a,b);
27     initial
28     begin
29         a=1'b0;
30         #10 a=1'b1;
31         #10 a=1'bx;
32         #10 a= 1'bz;
33     end
34 
```

Hierarchy Libraries Cor Sources Templates

Log

Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.inverter
Compiling module xil_defaultlib.inverter_tb
Compiling module xil_defaultlib.glbl
Waiting for 2 sub-compilation(s) to finish...
Built simulation snapshot inverter_tb_behav

Synthesis | Implementation | **Simulation**

Tcl Console Messages Log Reports Design Runs

Show/Hide RTL Analysis actions Switch to RTL Analysis environment (when enabled/bold)



Flow Navigator

Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

IP Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

Run Simulation

RTL Analysis

Elaboration Settings

Open Elaborated Design

Open Elaborated Design

Analyze and constrain an elaborated netlist.

data flow analysis

simulation is ips

Compiling module xil_defaultlib.inverter

Compiling module xil_defaultlib.inverter_tb

Compiling module xil_defaultlib.glbl

Waiting for 2 sub-compilation(s) to finish...

Built simulation snapshot inverter_tb_behav

Implementation

Implementation Setting

Run Implementation

Open Implemented Des

Project Manager - vinayreddy

Sources

Design Sources (1)

inverter (inverter.v)

Constraints

Simulation Sources (1)

sim_1 (1)

inverter_tb (inverte

r_tb (inverte

Project Summary X inverter.v X inverter_tb.v X

C:/Users/user/Desktop/vinayreddy/vinayreddy.srscs/sim_1/new/inverter_tb.v

17 // Revision 0.01 - File Created

18 // Additional Comments:

19 //

20 //

21

22

23 module inverter_tb;

24 wire b;

25 reg a;

26 //

27 initial

28 begin

29 a=1'b0;

30 #10 a=1'b1;

31 #10 a=1'bx;

32 #10 a= 1'bz;

33 //

Hierarchy Libraries Cor

Sources Templates

Log

Completed static elaboration

Starting simulation data flow analysis

data flow analysis simulation is ips

Compiling module xil_defaultlib.inverter

Compiling module xil_defaultlib.inverter_tb

Compiling module xil_defaultlib.glbl

Waiting for 2 sub-compilation(s) to finish...

Built simulation snapshot inverter_tb_behav

Synthesis | Implementation | Simulation

Tcl Console

Messages

Log

Reports

Design Runs

Analyze and constrain an elaborated netlist



Flow Navigator

Project Manager

Project Settings

Add Sources

Language Templates

IP Catalog

IP Integrator

Create Block Design

Open Block Design

Generate Block Design

Simulation

Simulation Settings

Run Simulation

RTL Analysis

Elaboration Settings

Open Elaborated Design

Synthesis

Synthesis Settings

Run Synthesis

Open Synthesized Des

Implementation

Implementation Setting

Run Implementation

Open Implemented Des

Project Manager - vinayreddy

Sources

Default Layout

Design Sources (1)

.../ve/inverter (inverter.v)

Constraints

Simulation Sources (1)

sim_1 (1)

.../ve/inverter_tb (inverte

.../ve/i1-inverter (inverte

Project Summary

C:/Users/user/Desktop/vinayreddy/vinayreddy.srscs/sim_1/new/inverter_tb.v

17 // Revision 0.01 - File Created

18 // Additional Comments:

19 //

20 ////////////////////////////////

21

22

23 module inverter_tb;

Elaborate Design



The current Elaboration settings allow you to perform I/O planning and constraint-related work with the elaborated netlist, but these settings slow down netlist elaboration. If you are not performing I/O pin planning you can change these settings from the Elaboration page of the Project Settings dialog box.

 Don't show this dialog again

OK

Cancel

Log

Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.inverter
Compiling module xil_defaultlib.inverter_tb
Compiling module xil_defaultlib.glbl
Waiting for 2 sub-compilation(s) to finish...
Built simulation snapshot inverter_tb_behav

Synthesis | Implementation | **Simulation**

Tcl Console | Messages | Log | Reports | Design Runs

Analyze and constrain an elaborated netlist



Flow Navigator

Project Manager - vinayreddy

Sources

Design Sources (1) *inverter (inverter.v)*

Constraints

Simulation Sources (1) *sim_1 (1)*

inverter_tb (inverte

i1 - inverter (inverte

Project Summary *inverter.v* *inverter_tb.v*

C:/Users/user/Desktop/vinayreddy/vinayreddy.srscs/sim_1/new/inverter_tb.v

```
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21
22
23 module inverter_tb;
24   wire b;
25   reg a;
26   inverter i1(a,b);
```

Open Elaborated Design

Elaborating design...

Hierarchy Libraries Cor

Sources Templates

Log

```
Completed static elaboration
Starting simulation data flow analysis
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.inverter
Compiling module xil_defaultlib.inverter_tb
Compiling module xil_defaultlib.glbl
Waiting for 2 sub-compilation(s) to finish...
Built simulation snapshot inverter_tb_behav
```

Synthesis | Implementation | **Simulation**

Tcl Console Messages Log Reports Design Runs

Elaborating design...

Flow Navigator

Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

IP Integrator

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

RTL Analysis

- Elaboration Settings
- Elaborated Design

 - Report DRC
 - Report Noise
 - Schematic

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

Elaborated Design xc7z020dg484-1 (active)

RTL Netlist

inverter

- Nets (3)
- Leaf Cells (2)

Sources RTL Netlist

Properties

Select an object to see properties

Project Summary Schematic inverter.v inverter_tb.v

2 Cells 2 I/O Ports 3 Nets

Diagram:

```
graph LR; a((a)) -- IO --> b_i[RTL_INV]; b_i -- 0 --> I[OBUF]; I -- 0 --> b((b));
```

Design Runs

Name	Constraints	Status	Progress	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT %	LUTs	FF %	FFs	BRAM %	BRAMs	DSP %
synth_1	constrs_1	Not started	0%													
impl_1	constrs_1	Not started	0%													

Tcl Console Messages Log Reports Design Runs



