CBT-1 (portions)

Subject: Digital Design Using HDL

Code : UE18EC20H.

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Module 1

1. Introduction to Boolean Functions * (Basic Theorems and properties of Boolean Algebra)

* Operator precedence

* Boolean Functions

* Canonical and Standard Forms

-> Minterms
-> Mancterms

-> Conversion between Canonical forms

* Logic Gates.

2. SK- Maps

2-Variable 15-Maps

* 3 - Variable K- Map

* H- Variable K-Map

* 5 - Variable K-Map

3. Prime Implicants

* PI -> Prime Implicants

* FPI -> Essential Prime Implicants

* RPI -> Redundant Prime Implicanto

H. SOP & POS Simplification

5. Don't care Conditions.

6. Quine - McCluskey Minimization Method.

7. NAND - NOR Implementation

* Two - level Implementation.

* Multi- level Emplementation.

8. Other Two-Level Implementation

* AND -OR - INVERT (ADI)

* OR - AND - INVERT (OAI)

* Wined logic

* Nondegenerate forms

9. HOL Flow

* Design entily

* Logic Simulation

* Logic Synthesis

* Timing Verification

* Faut Simulation.

10. Module Declaration

* How to declare a module in verilog

* Venlog - Posts

* Post - deceleration

* Verilog Primitives

* Verilog løde using primitives

* Delays > Yate Delays

* user defined primitives

* Verilog Test bench

* Verilog code using data flow style

L> Logical operators

Li Bit-Wise operators

Module - 2

1. Design procedure

2. Binary Adder - Subtractor

* Hay adder

* Full adder

* Parallel adder

* Limitations of Parallel adder

* carry Lookahead adder

* Signed q censigned numbers

* Binary Subtractor

Ly with overflow detection.

* Decimal / BCD Adder

\$. Binary Multiplier

L) abit by abit Multiplier

L. Four bit by 3 bit Muliplier

A. Magnitude Comparator

Lab

SOP and POS Simplification using K-Map

- Hay adder 2.
- 3. Hay Subtractor
- Ful adder
- 5. Full Subtractor
- 6. Parallel Adder (7483)/subtractor.
- BCD to Excess 3 and Vice Verson using (7483)
- Gray to Binary and Vice Versa
- a: 1 mux 9.
- H; 1 mux 10
 - 1; 4 Demux
 - Deal 4:1 mux IC74153
 - Dual ato 4 line decodes IC 74139
 - Full adder Half adder using \$4153
 - Full addu/ Half adder using 74139

** All the Best **