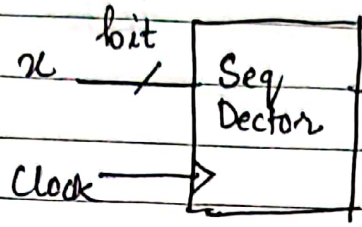
DATE

SEQUENCE DETECTORS

Vinay Reddy Narayana (Pg 1)

Sequence Detector

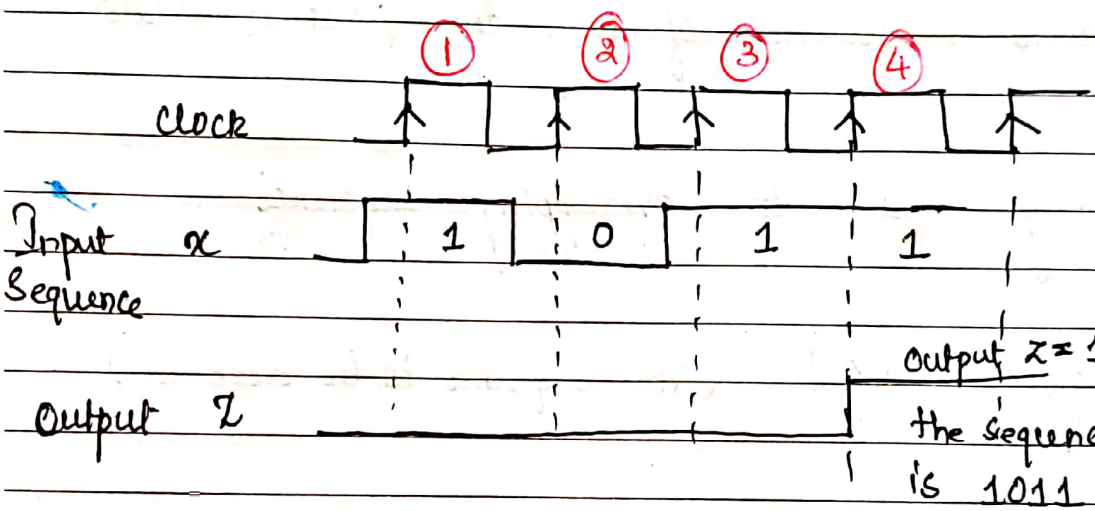


When the required sequence is detected, the output becomes 1 else the output is 0.

Example

To detect the sequence 1011

Take x = 1011.



Applications : In Digital Communication where we have to recognize a specific pattern or message.

Types of Sequence detectors

- Sequence detector to detect Overlapping sequence
- Sequence detector to detect Non-overlapping sequence

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Sequence detector

- Mealy sequence detector machine
- Moore sequence tector machine

Mealy

o/p is a function of both the present state and the present inputs

Moore

o/p is a function of only the present state

Overlapping and Non-overlapping sequence

Eg: 1101 (The sequence to be detected)

Input x = 1 1 0 1 1 0 1 1 0 1

Non overlapping output Z = 0 0 0 1 0 0 0 0 0 1

Input x = 1 1 0 1 1 0 1 1 0 1 (Overlapping, Overlapping)

Overlapping o/p Z = 0 0 0 1 0 0 1 0 0 1

Eg: 1-bit overlap sequence

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Important Note :

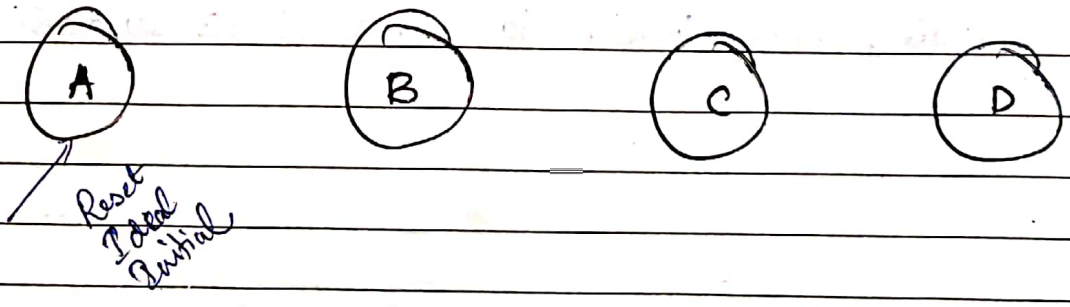
For n-bit sequence

Mealy Model ⇒ n states are required to detect the sequence
Moore Model ⇒ n+1 states are required to detect the sequence
(Extra 1 state is required to represent the output)

Eg 1101 is the sequence to be detected.

Sequence = 1101
Type of Machine = Mealy.

Hence the no of states = n = 4



Considering the 4 states.

Sequence : 1101

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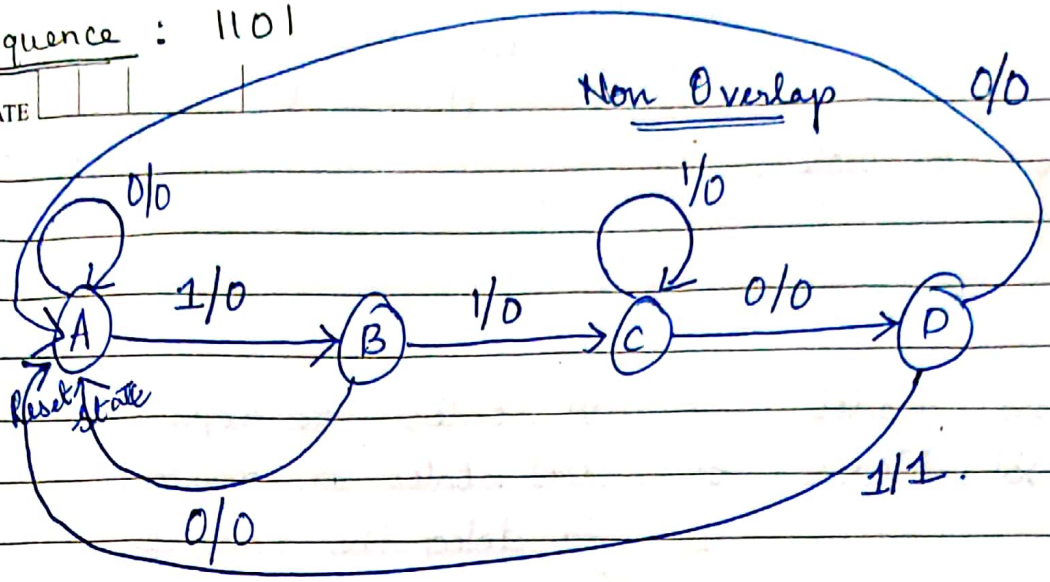

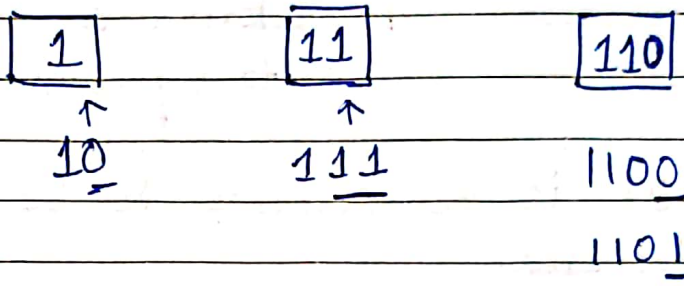

For Mealy Model

* For Non-OL (overlap), Move the last bit to reset state
* For 1-bit OL, compare the last bit to 1-bit state
* For 2-bit OL, compare the last 2 bits to 2-bit state, then 1-bit to 1-bit state and so on.

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Mealy Model 1-bit Overlap

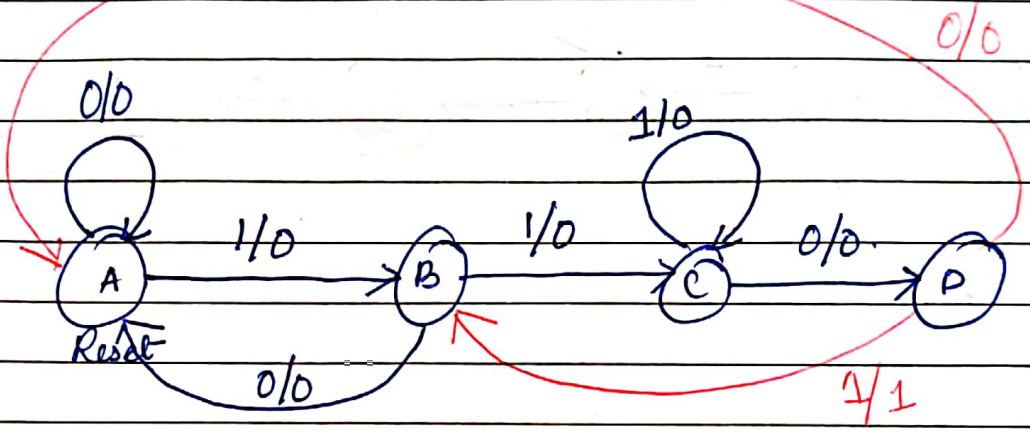
1101

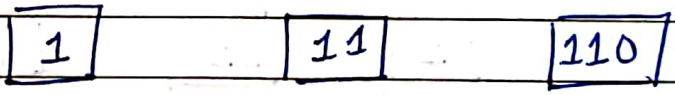
↳ this bit is reused

1101011

↳ 1'st bit for the second sequence

n=4, in mealy model we require 4 states





10

~~110~~

111

1100

1101

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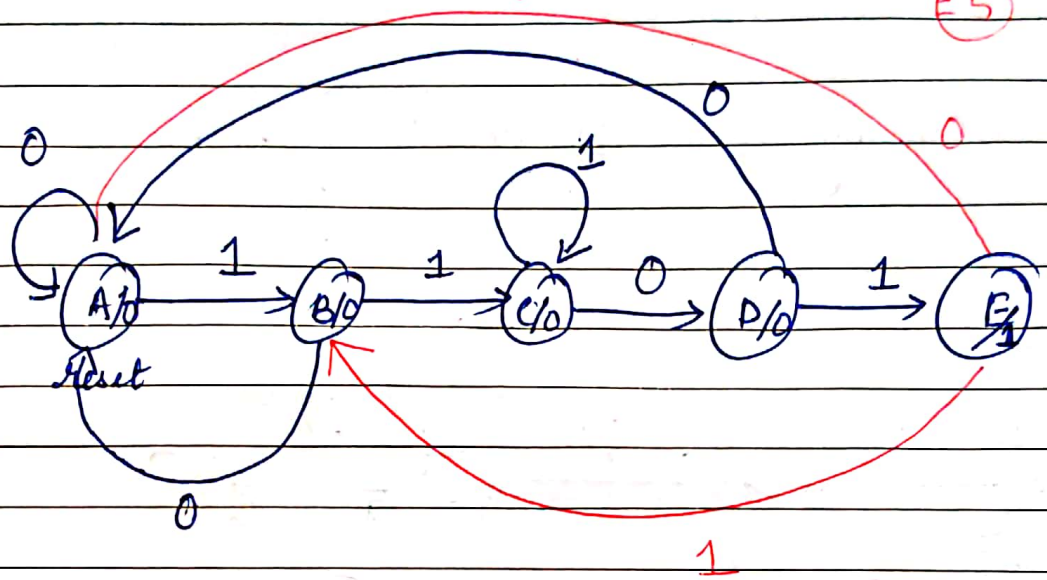
MOORE (Non - OL)

Eg = 1101

n = 4, no of states required = n + 1 = 5



1	11	110	1101
10	111	1100	11010
			11011

For Moore Model

* For Non-OL, compare the last bit to 1-bit state.

* For 1-bit OL, compare the last 2-bits to 2-bit state, then 1-bit to 1-bit state and so on.

* For 2-bit OL, compare the last 3 bits to 3-bit states, then 2-bits to 2-bit state and so on.

Eg For 2-bit overlap Moore Model

Eg 11011 → These 2 bits are reused

11011011

↳ These two bits are reused.

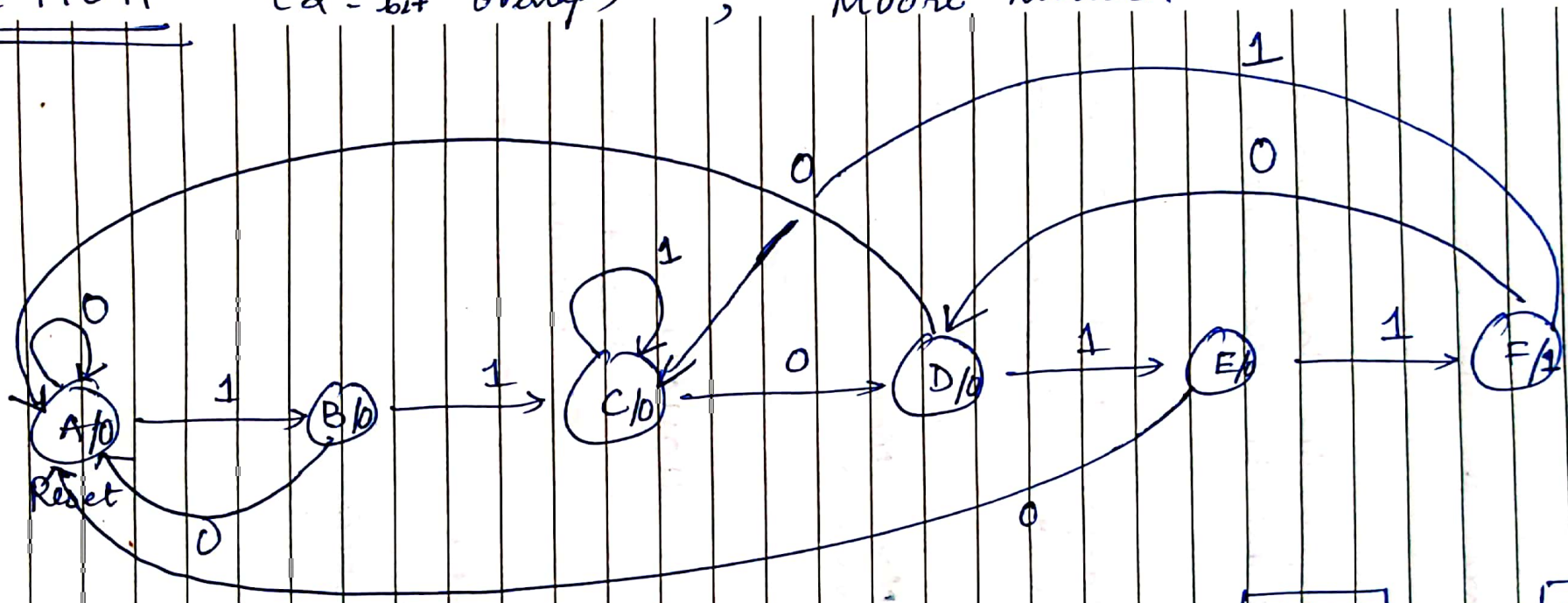
Sequence = 11011

no of states = n+1

= 5+1

= 6 states

Sequence 11011 (2-bit overlap), Moore Model.



1 → 10

11 → 111

110 → 1100

1101 → 11010

11011 → 110110 → 110111

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Experiment NO : 11

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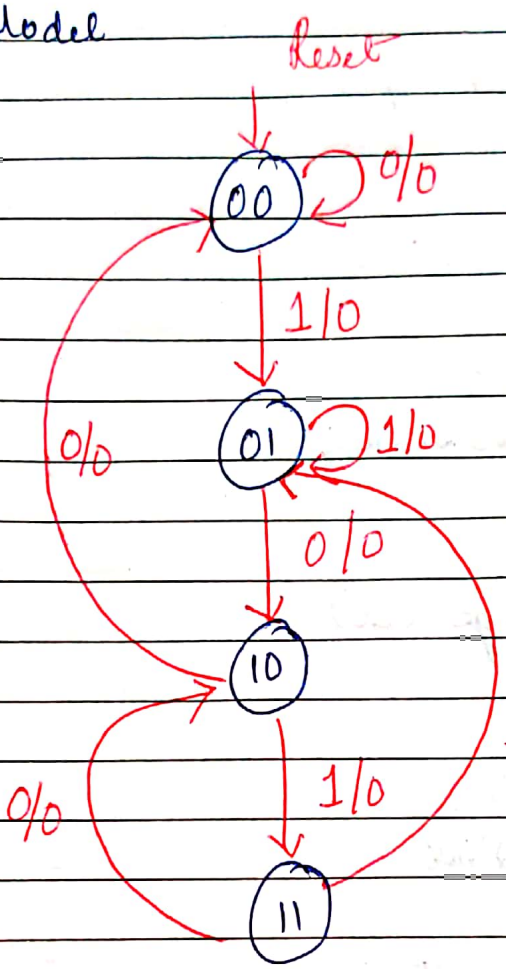
PG-5

Write a Verilog Code to Simulate Mealy and Moore Sequence detectors for the given sequence 1011.

Mealy Model



Taking two bit overlap

1

1

10

100

101

1010

1011

Since it is a 2 bit overlap we have to compare the last two bits to the 2-bit state and so on.

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Verilog Code

```
Module Mealy (clk, reset, inp, oltp);

input clk, reset, inp;
Output oltp;
reg oltp;

reg [1:0] state;
reg [1:0] next_state;

always@ (posedge clk)

  begin
     if (reset)
      state = 2'b00;
     else
      state = next_state;
  end
```

State transition logic.

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```
always @ ( state, inp, reset)

case (state)

2'b00 : begin
          if (inp) begin
            next_state <= 2'b01;
            Outp       <= 0;
          end
          else begin
            next_state <= 2'b00;
            Outp       <= 0;
          end

2'b01 : begin
          if (inp) begin
            next_state <= 2'b01;
            Outp       <= 0;
          end
          else begin
            next_state <= 2'b10;
            Outp       <= 0;
          end

2'b10 : begin
          if (inp) begin
            next_state <= 2'b11;
            Outp       <= 0;
          end
          else begin
            next_state <= 2'b00;
            Outp       <= 0;
          end
```

for state 00

for state 01

for state 10

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```
2'b11 : begin
        if (inp) begin
          next_state <= 2'b10;
          Outp       <= 1;
        else end begin
          next_state <= 2'b10;
          Outp       <= 0;
        end end
endcase
endmodule
```

for state 11

Moore Model (n+1 states)

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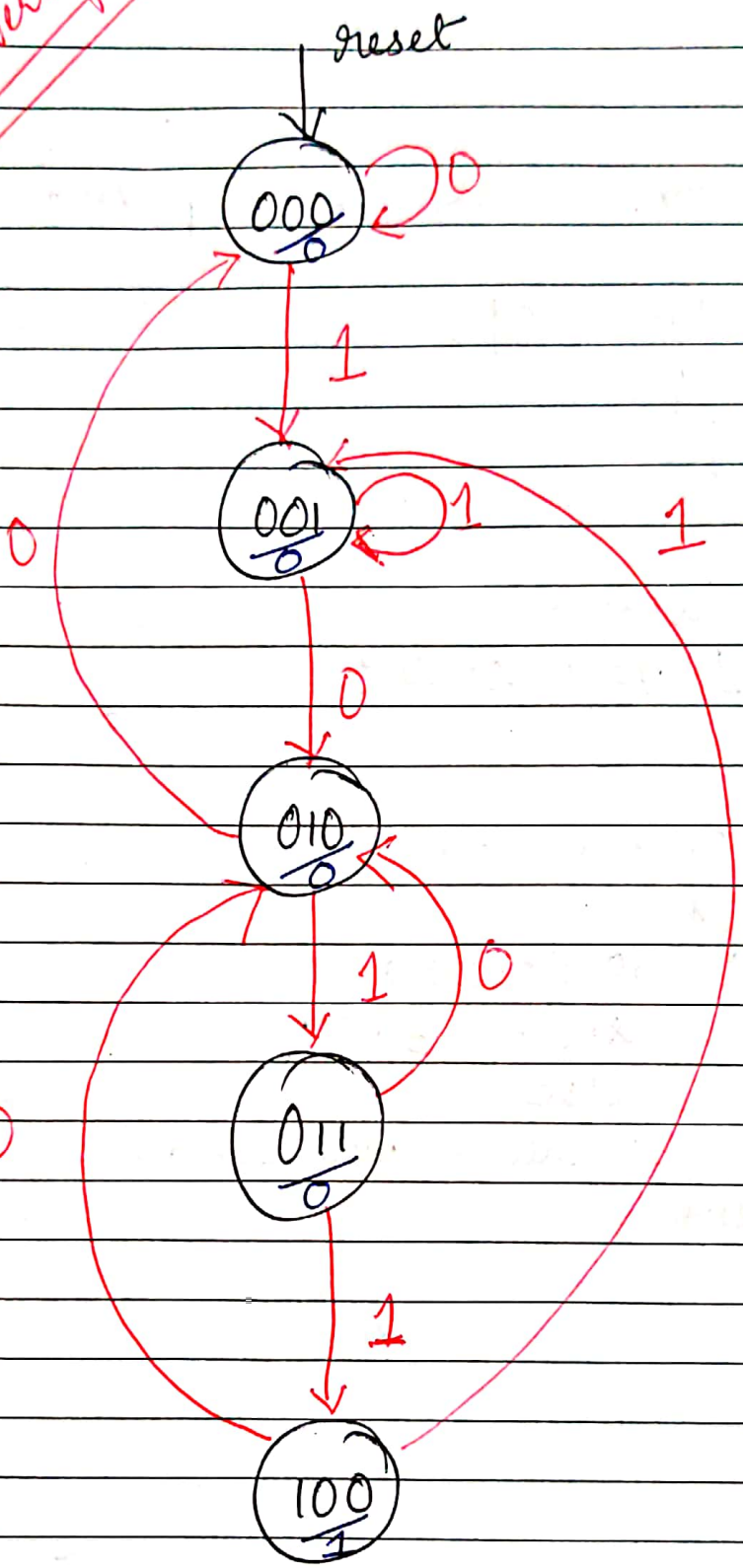
2 bit overlapping



1

11

10

100

101

1010

1011

1011

or

1010

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Verilog code

```
module moore (clk, reset, inp, outp);

input clk, reset, inp;
output outp;
reg outp;

reg [2:0] state;
reg [2:0] next_state;

always @ (posedge clk)
    begin
        if (reset)
        state = 3'b000;
        else
        state = next_state;
    end
```

State Transition.

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```
always@ (state, inp, reset)

case (state)

3'b000: begin
        if (inp)
        next_state <= 3'b001;
        else
        next_state <= 3'b000;
        end

3'b001 : begin
        if (inp)
        next_state <= 3'b001;
        else
        next_state <= 3'b010;
        end

3'b010 : begin
        if (inp)
        next_state <= 3'b011;
        else
        next_state <= 3'b000;
        end

3'b011 : begin
        if (inp)
        next_state <= 3'b100;
        else
        next_state <= 3'b010;
        end
```

For state 000

For state 001

For state 010

For state 011

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```
3'b100 : begin
            if (inp)
              next_state <= 3'b001;
            else
              next_state <= 3'b010;
         end
endcase
```

For state 100

```
always @ (state or reset)
begin
   if (reset)
   outp = 0;
   else

   case (state)

   3'b000 : outp = 0;
   3'b001 : outp = 0;
   3'b010 : outp = 0;
   3'b011 : outp = 0;
   3'b100 : outp = 1;

   endcase
end

endmodule
```

Outputs for all the states