Unit 4 : Differential Amplifiers

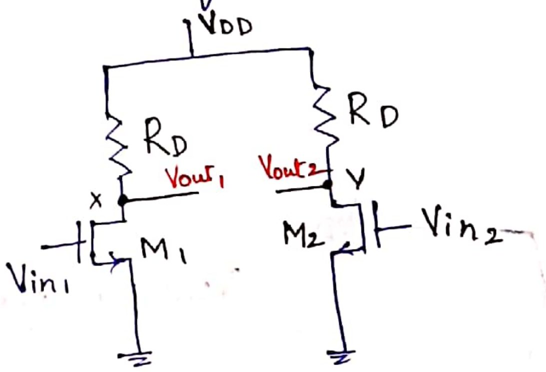
Basic Differential pair [How do we amplify a differential signal?]

→ Two identical ~~sig~~ single-ended signal paths to process the two phases.

→ Such a circuit indeed offers some of the advantages of differential signaling such as.

① high rejection supply voltage noise.

② higher output swings etc.

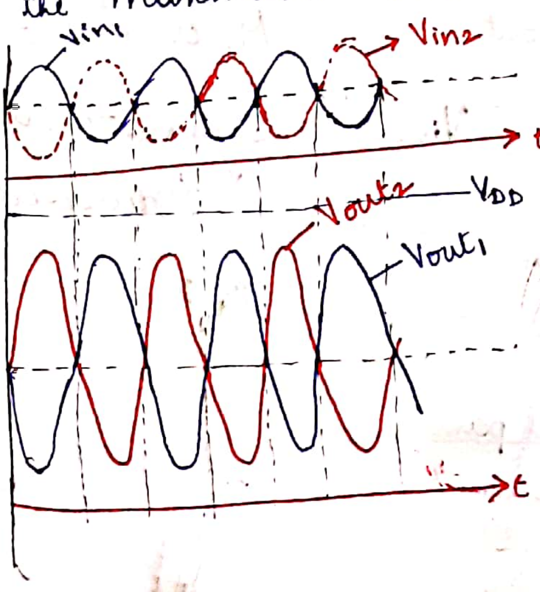


Simple differential circuit

→ If the input CM level, VincM, changes.

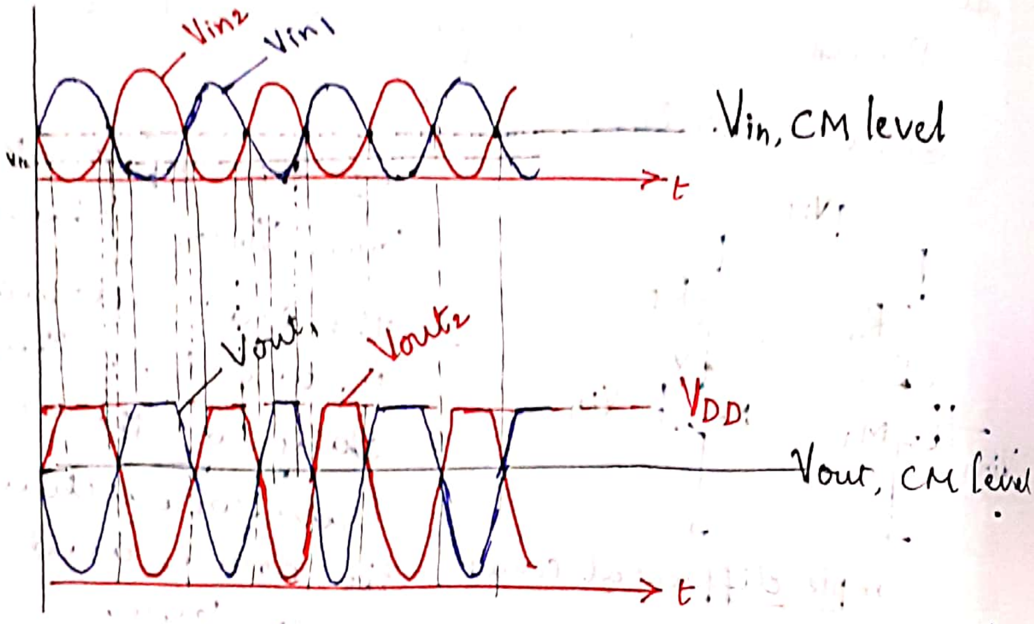
→ The bias currents of M_1 and M_2, thus varying the both transconductance of the devices and the o/p CM level.

→ The variation of the transconductance in turn leads to a change in the small-signal gain while the departure of the output CM level from its ideal value lowers the maximum allowable o/p swings.

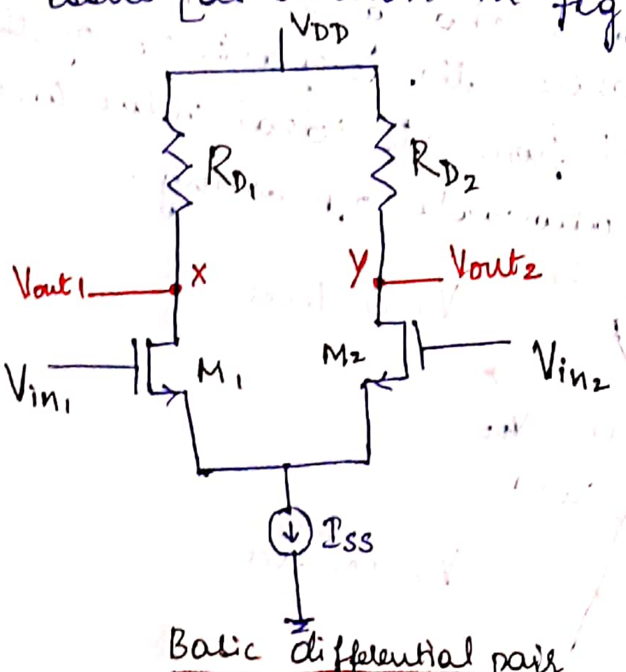


→ If input CM level is excessively low, the minimum values of V_{in1} and V_{in2} may in fact turn off M_1 and M_2, leading to severe clipping at the output.

→ Thus, it is important that the bias of the devices have minimal dependence on the input CM level



→ A simple modification can resolve the above issue [as shown in fig below]



$R_{D1} = R_{D2} = R_D$

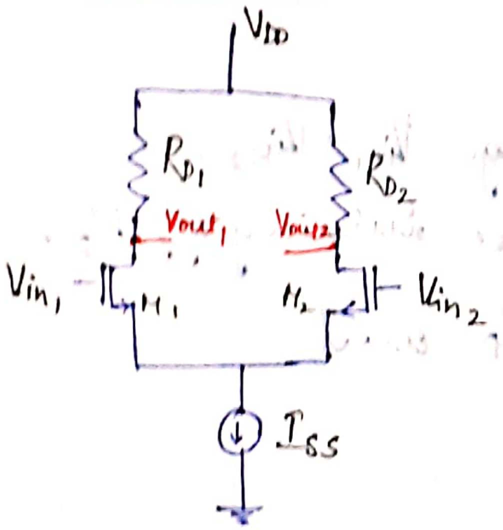
M_1 and M_2 are Symmetrical transistors.

Basic differential pair

→ The differential pair employs a current source I_{SS} to make I_{D_1} (drain current of M_1) + I_{D_2} (drain current of M_2) independence of $V_{in,CM}$

→ If $V_{in_1} = V_{in_2}$, the bias current of each transistor is equal to $\frac{I_{SS}}{2}$ and the output common-mode level is $V_{DD} - \frac{I_{SS}R_D}{2}$.

Qualitative Analysis [Difference mode behaviour]



$\boxed{R_{D_1} = R_{D_2} = R_D}$

→ Let us assume that in fig. $V_{in_1} - V_{in_2}$ varies from $-\infty$ to ∞

→ If V_{in_1} is more negative than V_{in_2}.

M_1 is off, M_2 is ON

$I_{D_2} = I_{SS}$

$V_{out_1} = V_{DD}$, $V_{out_2} = V_{DD} - I_{SS}R_{D_2}$

→ when V_{in_1} is brought closer to V_{in_2}

M_1 turns ON, drawing fraction of I_{SS} from R_{D_1}

Since $I_{SS} = I_{D_1}\uparrow + I_{D_2}\downarrow$

hence lowering V_{out_1} and V_{out_2} rises.

$V_{out_1} = V_{DD} - I_{D_1}R_D$

$V_{out_2} = V_{DD} - I_{D_2}R_D$

$V_{out_2} - V_{out_1} = (I_{D_1} - I_{D_2})R_D$

$$\boxed{\frac{\Delta V_{out}}{\Delta I_D} = R_D}$$

→ for $V_{in_1} = V_{in_2}$

$$I_{D_1} = I_{D_2} = \frac{I_{SS}}{2}$$

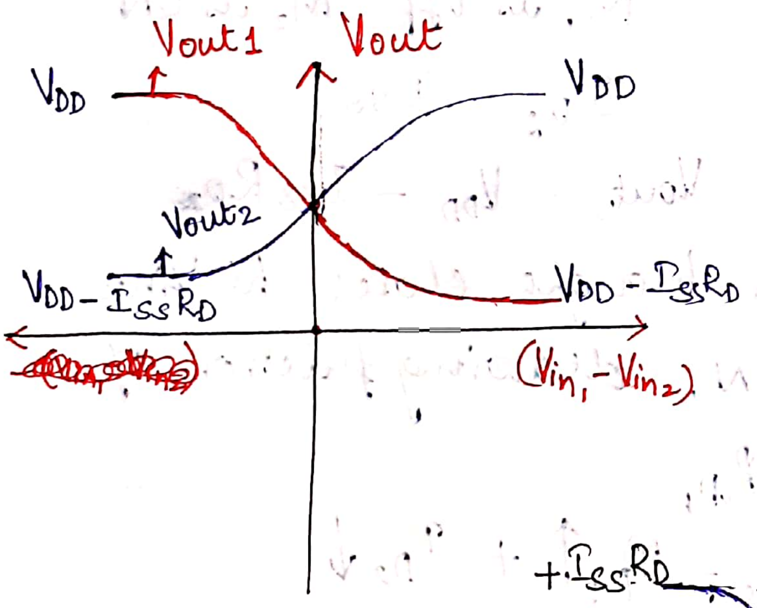
$$V_{out_1} = V_{out_2} = V_{DD} - \frac{I_{SS}R_D}{2}$$

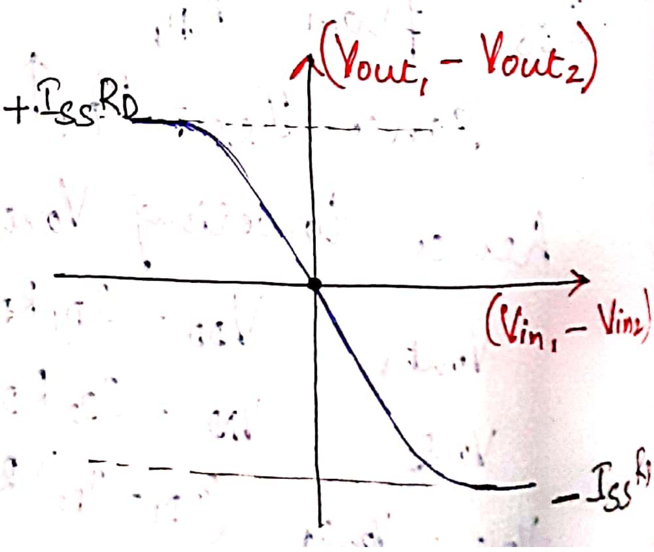
→ As V_{in_1} becomes more +ve than V_{in_2} M_1 carries a greater current than M_2 and V_{out_1} drops below V_{out_2}

→ For sufficiently large $V_{in_1} - V_{in_2}$, M_1 hogs all the I_{SS} turning off M_2.

$$V_{out_1} = V_{DD} - I_{SS}R_D \text{ and}$$

$$V_{out_2} = V_{DD}$$





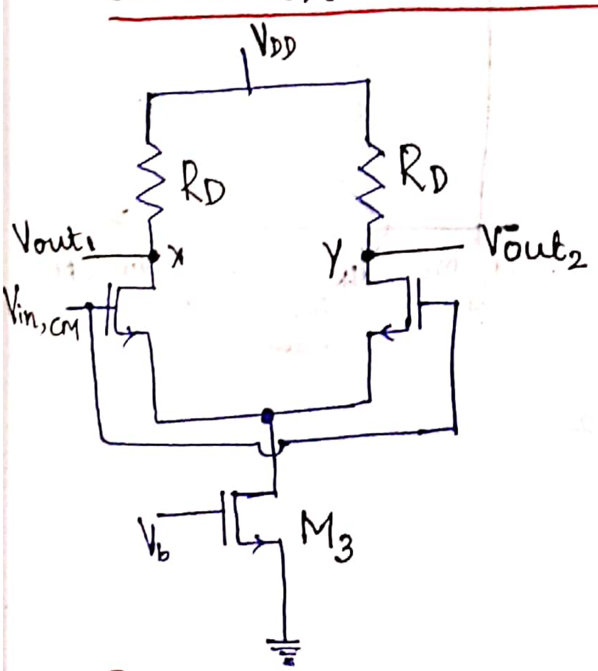
Input - output characteristics of a differential pair

→ From the differential mode behaviour analysis, reveals two important attributes of the differential pair.

1. The maximum and minimum level at the output are well defined V_{DD} and $V_{DD} - I_{SS}R_D$ respectively.

2. The small-signal gain [the slope of $(V_{out_1} - V_{out_2})$ versus $(V_{in_1} - V_{in_2})$] is maximum for $V_{in_1} = V_{in_2}$, gradually falling to zero as $|V_{in_1} - V_{in_2}|$ increases (or) The circuit becomes more nonlinear as the input voltage swing increases. For $V_{in_1} = V_{in_2}$ the circuit is in equilibrium.

Common Mode behaviour



→ The role of the tail current source is to suppress the effect of input CM level variations on the operations of M_1 and M_2 and the output level.

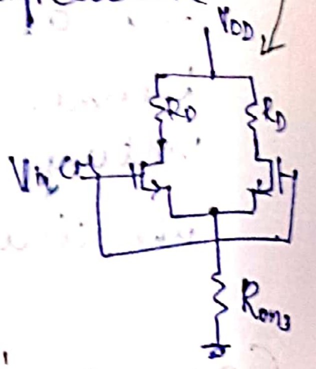
Does this means that $V_{in,CM}$ can assumed arbitrarily low or high values? [Does this enable us to set any arbitrary level of input CM]

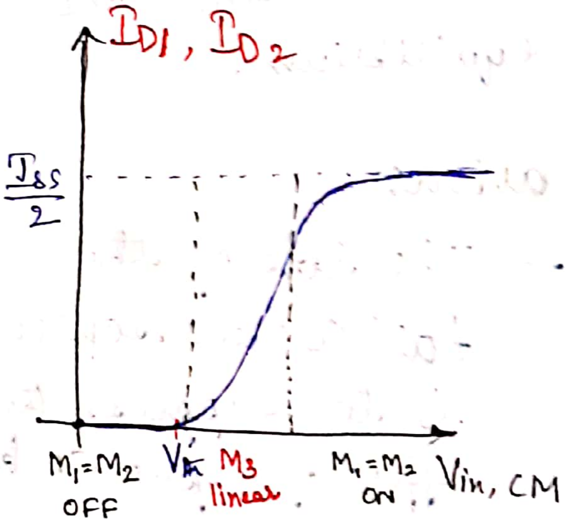
→ Set $V_{in_1} = V_{in_2} = V_{in,CM}$ and vary $V_{in,CM}$ from 0 to V_{DD}

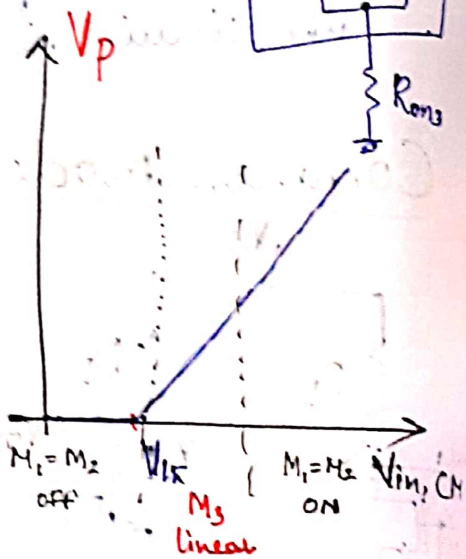
→ If $V_{in,CM} = 0$, since the gate potential of M_1 and M_2 is not more positive than their source potential, both devices are off, yielding $I_{D_3} = 0$

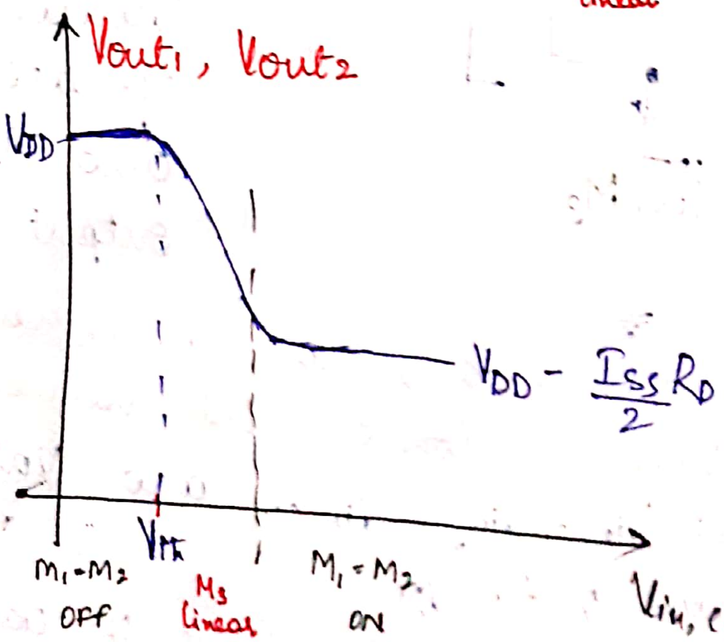
→ This indicates that M_3 is in deep triode region because V_b is high enough to create an inversion layer in the transistor [modeling M_3 by a resistor as shown in fig below]

→ with $I_{D_1} = I_{D_2} = 0$, the circuit is incapable of signal amplification and $V_{out_1} = V_{out_2} = V_{DD}$.









→ Now suppose $V_{in,CM}$ becomes more positive. the M_1 and M_2 turn on if $V_{in,CM} \geq V_{th}$

→ Beyond this point, I_{D1} and I_{D2} continue to increase and V_P also rises.

→ In a sense, M_1 and M_2 constitute a source follower, forcing V_P to track $V_{in,CM}$.

→ For a sufficiently high $V_{in,CM}$, the drain-source voltage of M_3 exceeds $V_{GS3} - V_{TH3}$, allowing the device to operate in saturation.

→ The total current through M_1 and M_2 then remains constant.

→ The conclusion, is that for proper operation, $V_{in,CM} \geq V_{GS1} + (V_{GS3} - V_{TH3})$.

What happens if $V_{in,CM}$ rises further?

→ Since V_{out1} and V_{out2} are relatively constant., and ~~if~~ ~~M~~

→ Since M_1 and M_2 enter the triode ~~linear~~ region if $V_{in,CM} > V_{out1} + V_{th}$

$$= V_{DD} - \frac{R_D I_{SS}}{2} + V_{th}.$$

M_1 and M_2 will remain in saturation if. $V_{in,CM} \leq V_{DD} - \frac{I_{SS}}{2} R_D + V_{th}$

This sets an upper limit on the input CM level. The allowable value of $V_{in,CM}$ is

$$V_{GS1} + (V_{GS3} - V_{TH3}) \leq V_{in,CM} \leq \min\left[V_{DD} - \frac{I_{SS} R_D}{2} + V_{TH},\ V_{DD}\right]$$

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$$\boxed{V_{GS_1} + (V_{GS_3} - V_{TH_3}) \leq V_{in,CM} \leq \text{Min}\left[V_{DD} - \frac{I_{SS}R_D}{2} + V_{TH},\ V_{DD}\right]}$$

Sketch the small-signal differential gain of a differential pair as a function of the input CM level.

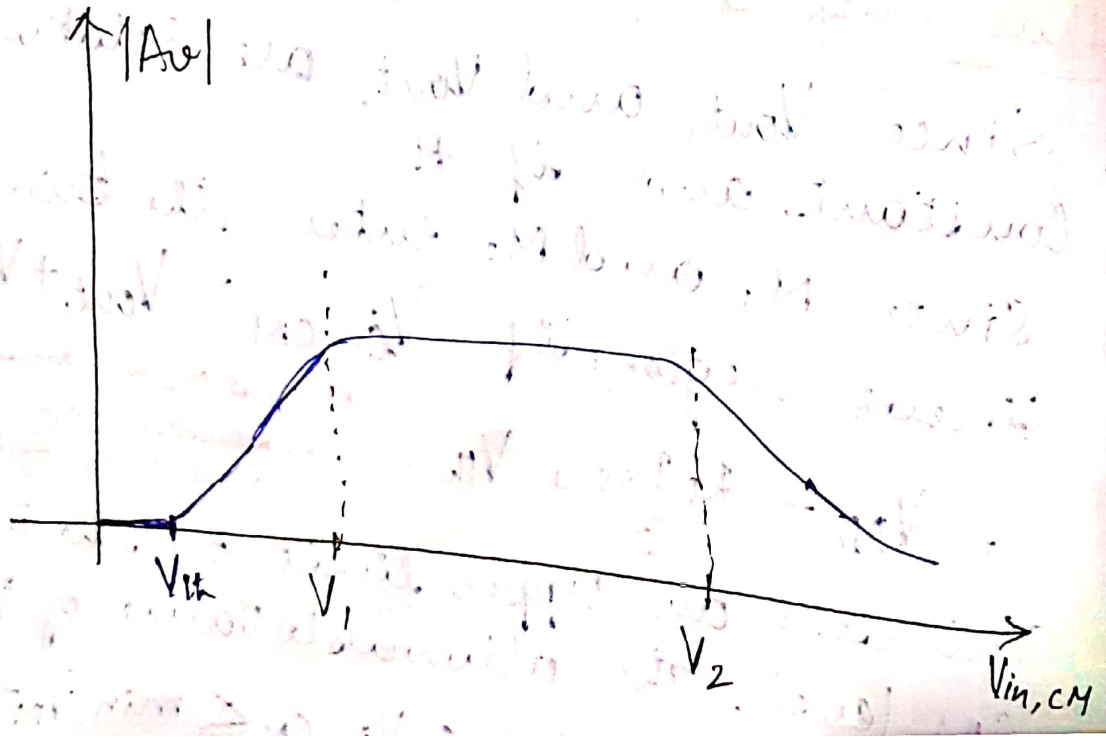
→ The gain begins to increases as $V_{in,CM}$ exceeds V_{TH}

→ After the tail current source enters saturation $(V_{in,CM} = V_1)$

i.e $V_{in,CM} \geq V_{GS_1} + (V_{GS_3} - V_{TH_3})$

the gain remains relatively constant

→ Finally, if $V_{in,CM}$ is greater, ~~than~~ that the input transistors enter the triode region $(V_{in,CM} = V_2)$, the gain begins to fall



How large can the output voltage swings of a differential pair.

M_1 and M_2 to be saturated, each output can go as high as V_{DD} but as low as approximately $V_{in,CM} - V_{TH}$.

$$\boxed{\begin{aligned} V_{out,max} &= V_{DD} \\ V_{out,min} &= V_{in,CM} - V_T \end{aligned}}$$

The higher the input CM level, the smaller the allowable output swings.

MOS Differential pair - Small Signal Analysis

Method 1 : Superposition technique - The idea is to see the effect of V_{in_1} and V_{in_2} on the output and then combine to get the differential small signal voltage gain.

Method II : If a fully-symmetric differential pair senses differential inputs (i.e the two inputs change by equal and opposite amounts from the equilibrium condition), then the concept of "half circuit" can be applied.

First prove a lemma

Lemma: Consider the symmetric circuit shown in fig(a) below, where D_1 and D_2 represent any three-terminal active device.

Suppose V_{in_1} changes from V_0 to $V_0 + \Delta V_{in}$

and V_{in_2} from V_0 to $V_0 - \Delta V_{in}$ as shown in fig(b). Then, if the circuit remains linear, V_P does not change.

Assume $\lambda = 0$

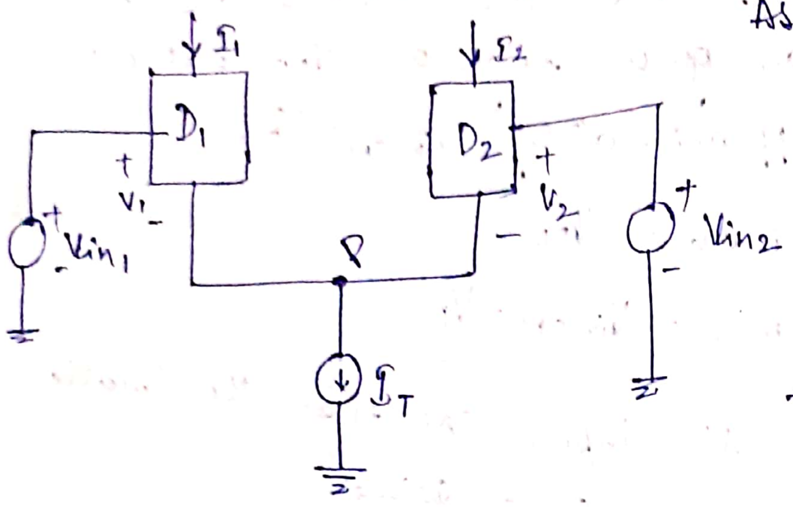
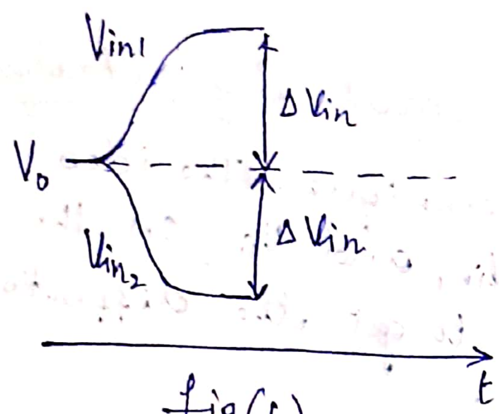
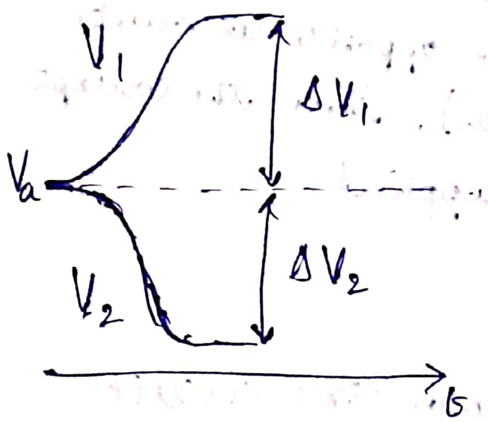


fig (a)



fig(b)



Proof: Let us assume that V_1 and V_2 have an equilibrium value of V_a and change by ΔV_1 and ΔV_2 respectively as shown in fig. (c). The output currents therefore change by ~~$g_m \Delta V_{in}$~~ $g_m \Delta V_1$ and $g_m \Delta V_2$.

→ Since $I_1 + I_2 = I_T$

we have $g_m \Delta V_1 + g_m \Delta V_2 = 0$.

i,e $\Delta V_1 = -\Delta V_2$,

→ $V_{in_1} - V_1 = V_{in_2} - V_2$ and hence

$$V_0 + \Delta V_{in} - (V_a + \Delta V_1) = V_0 - \Delta V_{in} - (V_a + \Delta V_2)$$

$$2\Delta V_{in} = \Delta V_1 - \Delta V_2 = 2\Delta V_1$$

$$2\Delta V_{in} = 2\Delta V_1$$

→ In other words, if V_{in1} and V_{in2} change by $+\Delta V_{in}$ and $-\Delta V_{in}$ respectively then V_1 and V_2 change by the same values; i.e.

→ a differential change in the inputs is simply "absorbed" by V_1 and V_2.

→ In fact, since $V_P = V_{in1} - V_1$ and since V_1 exhibits the same change as V_{in1}, V_P does not change.

→ As long as the operation remains linear so that the difference between the bias currents of D_1 and D_2 is negligible, the circuit is symmetric.

→ Thus, V_P cannot "favor" the change at one input and "ignore" the other.

→ The above lemma greatly simplifies the small-signal analysis of differential amplifiers.

→ Since V_P experiences no change, node P can be considered "ac ground" and the circuit can be decomposed into two separate halves. hence the term "half-circuit concept"

$$\frac{V_x}{V_{in_1}} = -g_m R_D$$

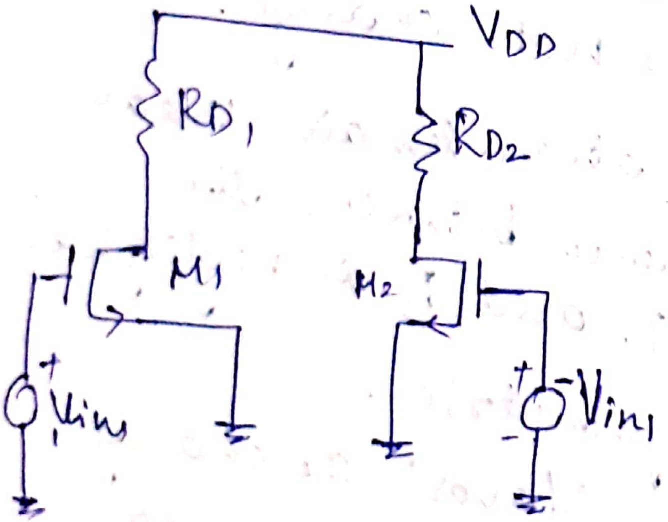
$$\frac{V_y}{-V_{in_1}} = -g_m R_D$$

$$V_x - V_y = -g_m R_D V_{in_1} - (g_m R_D) V_{in_1}$$

$$V_x - V_y = -g_m R_D (2 V_{in_1})$$

$$\boxed{\frac{V_x - V_y}{2 V_{in_1}} = -g_m R_D}$$

Differential mode gain



Application of the half-circuit concept.

Differential pair with MOS loads

→ The load of a differential pair need not be implemented by linear resistors.

→ differential pairs can employ diode-connected or current-source loads.

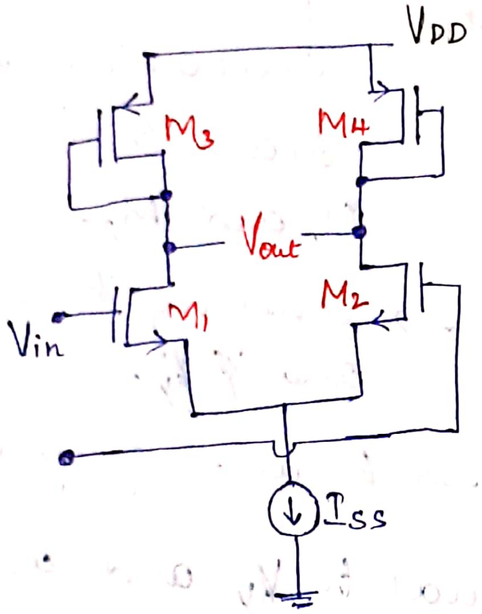
→ 

fig: Differential pair diode-connected load

→ The small signal differential gain can be derived using the half-circuit concept

$$A_v = -\frac{g_{mN}(r_{ON} \parallel r_{OP})}{g_{mp}}$$

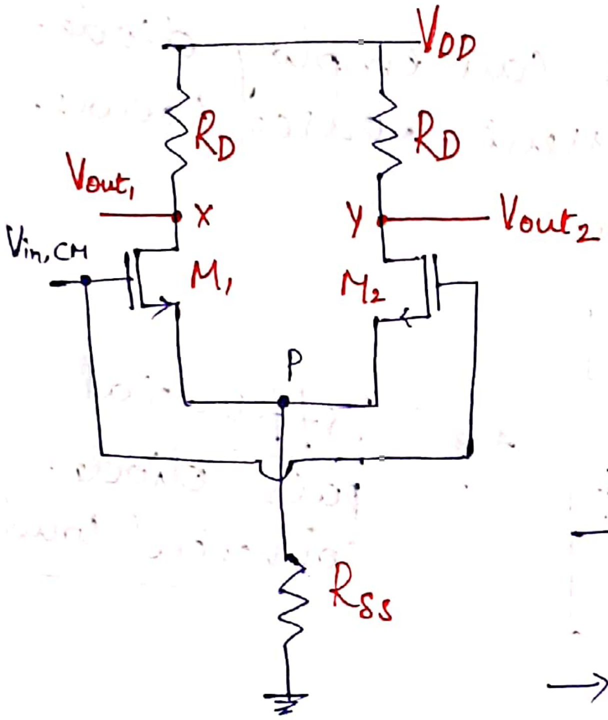
If $\lambda = 0$.

$$A_v \simeq -\frac{g_{mN}}{g_{mp}}$$

$$\boxed{A_v \simeq -\sqrt{\frac{\mu_n \left(\frac{W}{L}\right)_N}{\mu_p \left(\frac{W}{L}\right)_p}}}$$

Common-Mode Response

→ Assume the circuit is symmetric but the current source has a finite output impedance, R_{SS}

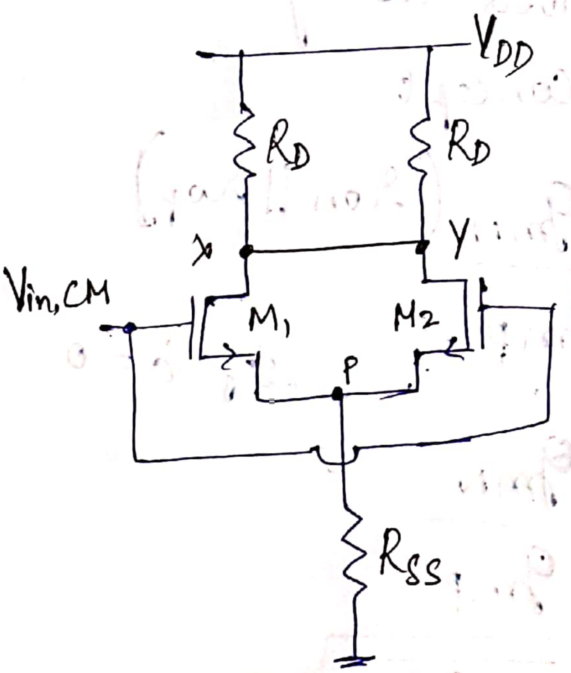


→ As $V_{in,CM}$ changes, so does V_P, thereby increasing the drain currents of M_1 and M_2.

→ lowering both V_X and V_Y.

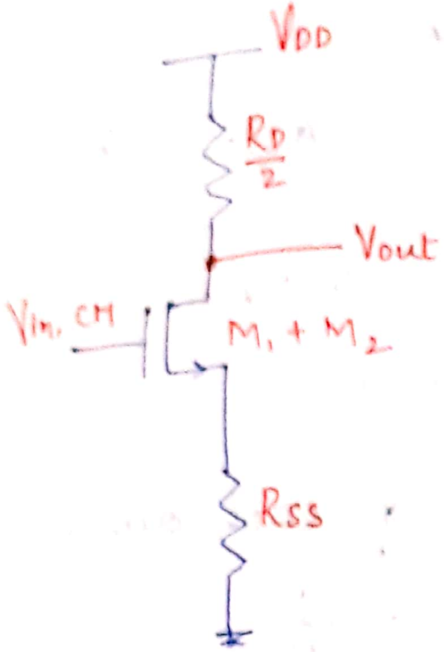
→ Because of symmetry,

→ V_X remains equal to V_Y and as depicted in fig below, the two nodes can be shorted together.



→ Since M_1 and M_2 are now in parallel i.e. They share all of their respective terminals,

→ The circuit can be reduced to that as shown in fig next



→ The compound device, $M_1 + M_2$ has twice the width and the ~~bias~~ bias current of each of M_1 and M_2

→ Therefore, twice their transconductance.

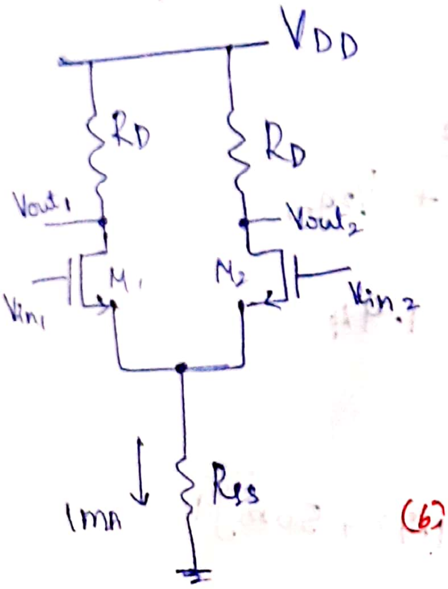
→ The CM gain of the circuit is thus equal to.

Common mode gain

$$\boxed{A_{v,CM} = \frac{V_{out}}{V_{in,CM}} = \frac{R_D/2}{(1/2g_m) + R_{SS}}}$$

where g_m denotes the transconductance of each of M_1 and M_2 & $\lambda = 0$

The circuit shown in fig uses a resistor rather than a current source to define a tail current of 1mA. Assume



$(W/L)_{1,2} = \frac{25}{0.5}$

$\mu_n C_{ox} = 50 \mu A/V^2$

$V_{th} = 0.6V$

$\lambda = \gamma = 0$ and $V_{DD} = 3V$

(a) what is the required input CM for which Rss sustains 0.5V?

(b) Calculate R_D for a differential gain of 5

(c) what happens at the output if the input CM level is 50mV higher than the value calculated in (a)?

(a) Since $I_{D_1} = I_{D_2} = 0.5mA$,

$$V_{GS_1} = V_{GS_2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}\frac{W}{L}}} + V_{th} = 1.23V$$

Thus $V_{in,CM} = V_{GS_1} + 0.5V = 1.73V$ ..

$R_{ss} = 0.5 \times 1mA = 500\Omega$

(b) The Transconductance of each device is $g_m = \sqrt{2\mu_n C_{ox}(W/L) I_{D_1}} = \frac{1}{632\Omega}$

$A_v = -g_m R_D$

$$\boxed{R_D = 3.16k\Omega}$$

Output bias level is equal to $V_{DD} - I_{D_1}R_D = 1.42V$

Since $V_{in,CM} = 1.73V$ and $V_{th} = 0.6V$, the transistors are 290mV away from the triode region.

(c) If $V_{in,CM}$ increases by 50mV, ~~the equivalent circuit of~~

$$\frac{\Delta V_{xy}}{\Delta V_{in,CM}} = \frac{R_D/2}{R_{ss} + 1/2g_m}$$

$\Delta V_{xy} = \Delta V_{in,CM} \times 1.94$

$\rightarrow = 96.8mV$

Now $V_{in,CM} = 1.78V = [1.73 + 50m]V$

$V_{in,CM} - V_{th} = 1.18V$

$V_{out} = 1.42V \mp 96.8mV = \cancel{1.516V}$ $1.32V$

Now, M_1 and M_2 are only 143mV away from the triode region because the input CM level has increased by 50mV and o/p CM level decreased by 96.8mV.