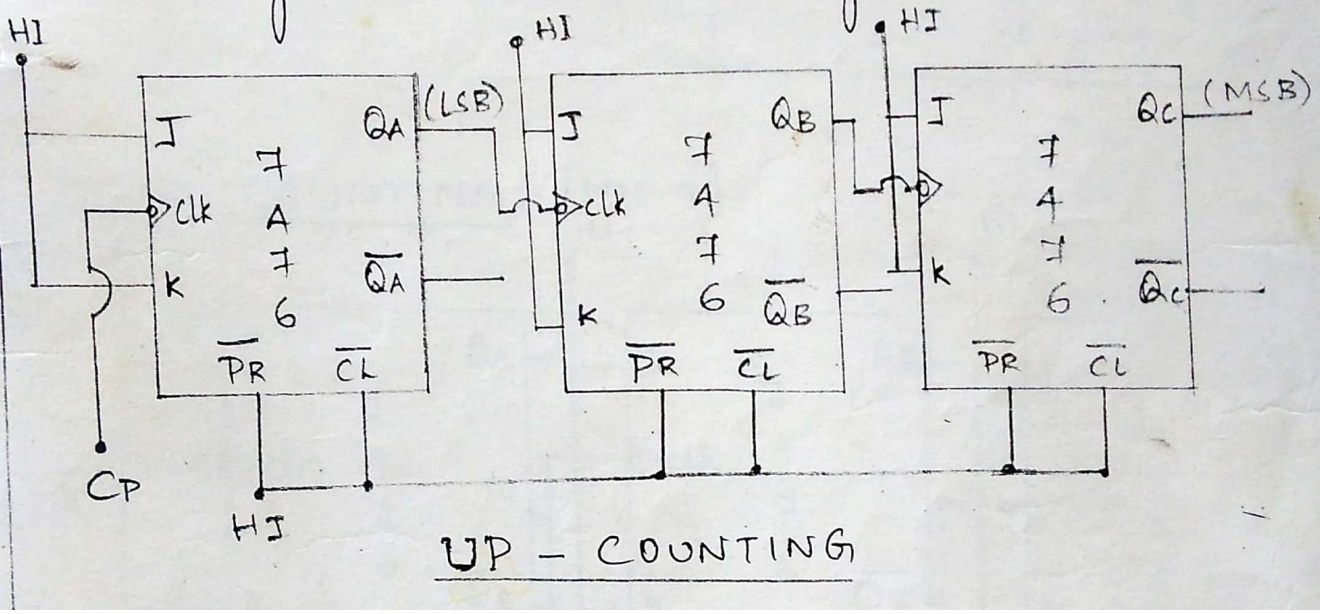
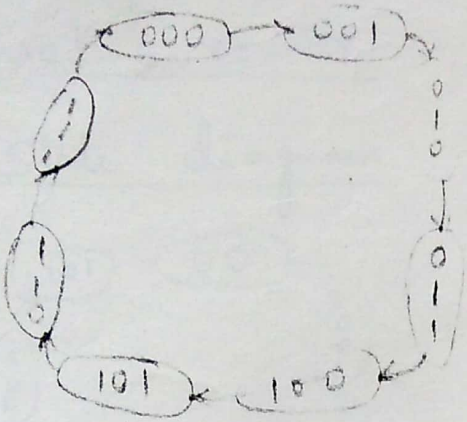
3- bit asynchronous counter using IC 7476 :- [MOD-8]



UP - COUNTING

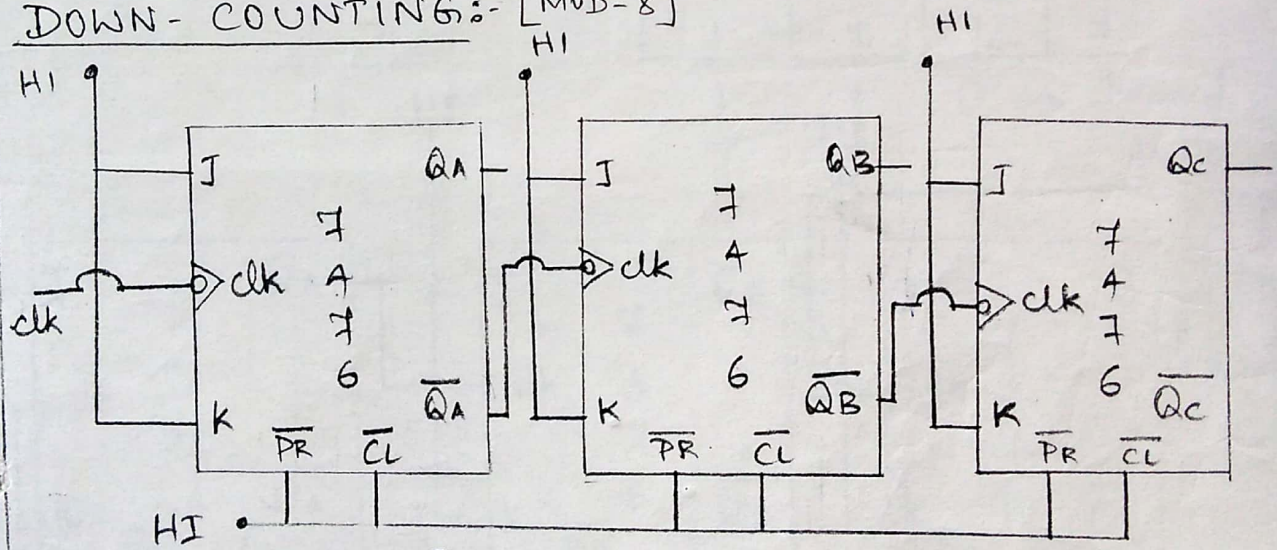
State diagrams

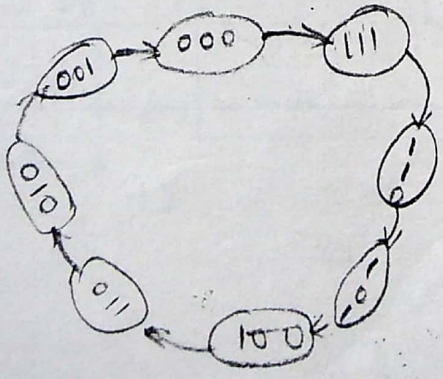


Truth-table :-

C_P	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	ø1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

DOWN-COUNTING :- [MOD-8]





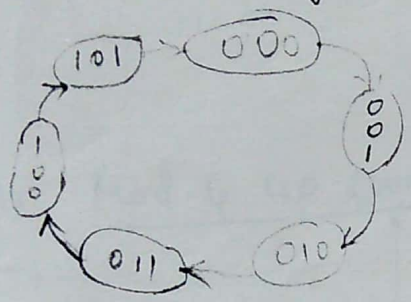
Truth-table

C_P	Q_C	Q_B	Q_A
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0

mod-n counters :- [UP- counting]

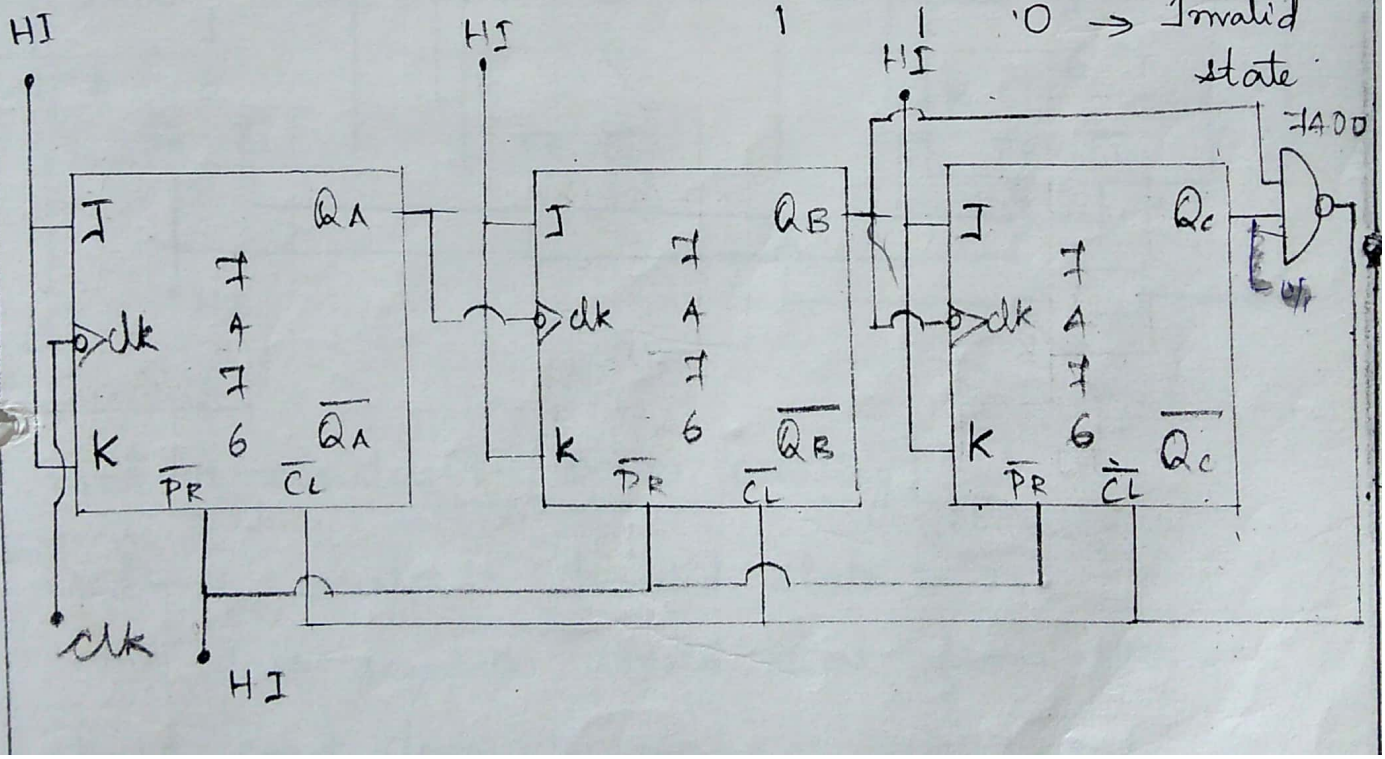
(1) mod-6 counter

State diagram

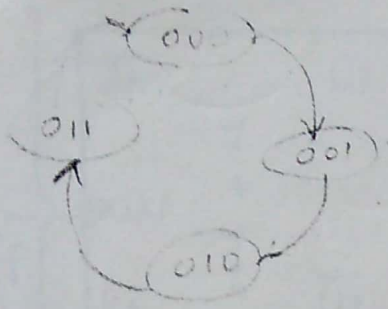


Truth- table

Q_C	Q_B	Q_A	C_P
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	→ Invalid state



mod-4 counter :-



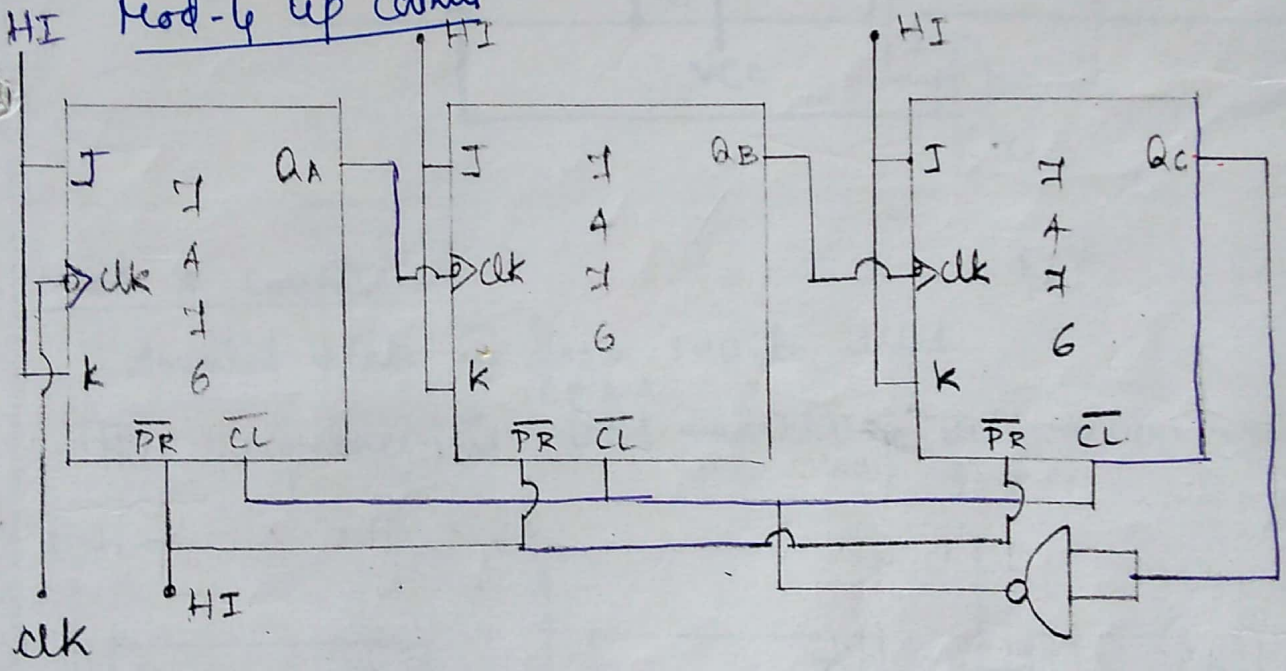
Truth-table

Q_C	Q_B	Q_A	C_P
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

Q_C Q_B Q_A

1 0 0 → invalid state

Mod-4 up counter



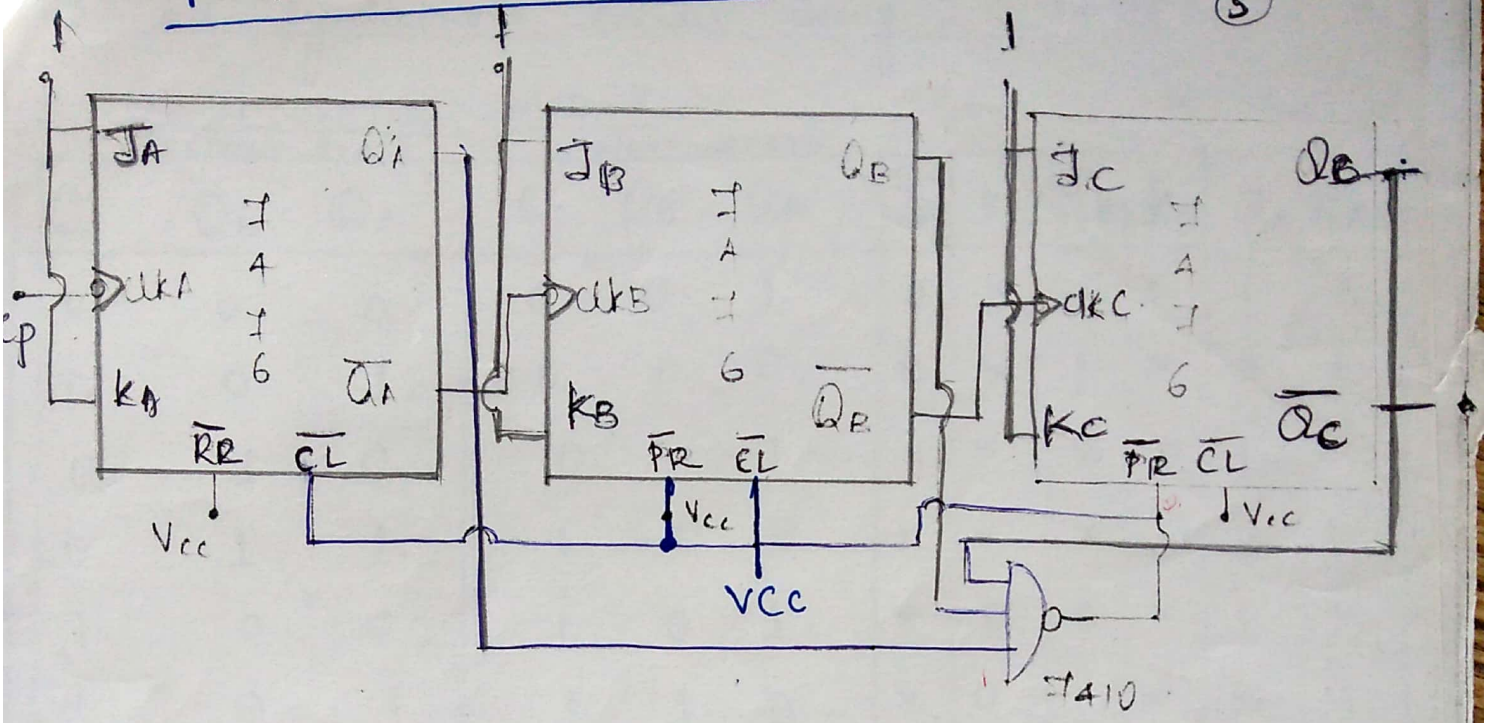
mod-n counters :- [DOWN-counting]

(i) mod-7 counter :- Invalid state :- 111

The data sequence should start from 110 & should count down to 000.

110 → 101 → 100 → 011 → 010 → 001 → 000 → 110

Mod-7 down counter



mod-4 counter :-

Invalid state is from 100 to 111.

Then sequence is $011 \rightarrow 010 \rightarrow 001 \rightarrow 000 \rightarrow 011$ (C B A)