CHAPTER

6

Frequency Response of Amplifiers

Our analysis of simple amplifiers has thus far focused on low-frequency characteristics, neglecting the effect of device and load capacitances. In most analog circuits, however, the speed trades with many other parameters such as gain, power dissipation, and noise. It is therefore necessary to understand the frequency-response limitations of each circuit.

In this chapter, we study the behavior of single-stage and differential amplifiers in the frequency domain. Following a review of basic concepts, we analyze the high-frequency response of common-source and common-gate stages and source followers. Next, we deal with cascode and differential amplifiers. Finally, we consider the effect of active current mirrors on the frequency response of differential pairs.

6.1 ■ General Considerations

Recall that a MOS device exhibits four capacitances: C_{GS}, C_{GD}, C_{DB}, and C_{SB}. For this reason, the transfer function of CMOS circuits can rapidly become complicated, calling for approximations that simplify the circuit. In this section, we introduce two such approximations, namely, Miller's theorem and association of poles with nodes. We remind the reader that a two-terminal impedance, Z, is defined as $Z = V/I$, where V and I denote the voltage across and the current flowing through the device. For example, $Z = 1/(Cs)$ for a capacitor. Also, the transfer function of a circuit yields the frequency response if we replace s with $j\omega$, i.e., if we assume a sinusoidal input such as $A\cos\omega t$. For example, $H(j\omega) = (RCj\omega + 1)^{-1}$ provides the magnitude and phase of a simple low-pass filter.

In this chapter, we are primarily interested in the *magnitude* of the transfer function (with $s = j\omega$). Figure 6.1 shows examples of magnitude response. We should also remark that, even if computed exactly, some transfer functions do not offer much insight. We therefore study numerous special cases by considering extreme conditions, e.g., if the load capacitance is very small or very large.

A few basic concepts are used extensively throughout this chapter and merit a brief review. (1) The magnitude of a complex number $a + jb$ is given by $\sqrt{a^2 + b^2}$. (2) Zeros and poles are respectively defined as the roots of the numerator and denominator of the transfer function. (3) According to Bode's approximations, the slope of the magnitude of a transfer function increases by 20 dB/decade as ω passes a pole frequency and decreases by 20 dB/decade as ω passes a zero frequency.

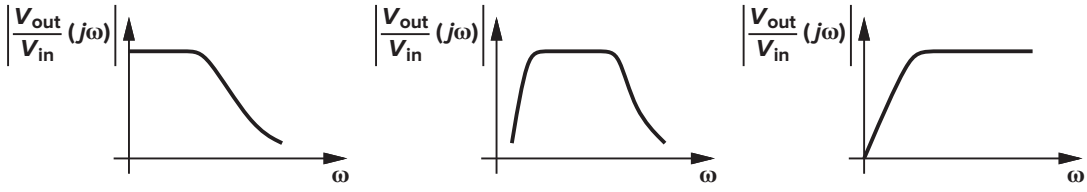


Figure 6.1 (a) Low-pass, (b) band-pass, and (c) high-pass frequency-response examples.

6.1.1 Miller Effect

An important phenomenon that occurs in many analog (and digital) circuits is related to the "Miller effect," as described by Miller in a theorem.

Miller's Theorem If the circuit of Fig. 6.2(a) can be converted to that of Fig. 6.2(b), then $Z_1 = Z/(1 - A_v)$ and $Z_2 = Z/(1 - A_v^{-1})$, where $A_v = V_Y/V_X$.

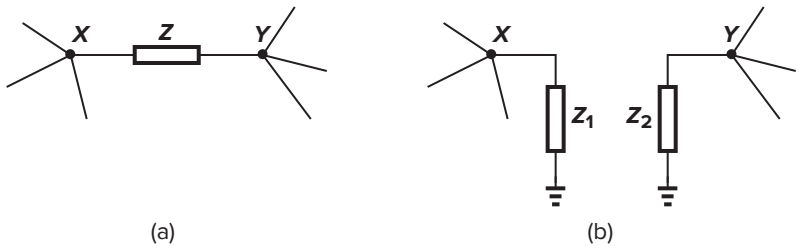


Figure 6.2 Application of Miller effect to a floating impedance.

Proof The current flowing through Z from X to Y is equal to $(V_X - V_Y)/Z$. For the two circuits to be equivalent, the same current must flow through Z_1. Thus,

$$\frac{V_X - V_Y}{Z} = \frac{V_X}{Z_1} \tag{6.1}$$

that is

$$Z_1 = \frac{Z}{1 - \dfrac{V_Y}{V_X}} \tag{6.2}$$

Similarly,

$$Z_2 = \frac{Z}{1 - \dfrac{V_X}{V_Y}} \tag{6.3}$$

This decomposition of a "floating" impedance, Z, into two "grounded" impedances proves useful in analysis and design.

▶ **Example 6.1**

Consider the circuit shown in Fig. 6.3(a), where the voltage amplifier has a negative gain equal to $-A$ and is otherwise ideal. Calculate the input capacitance of the circuit.

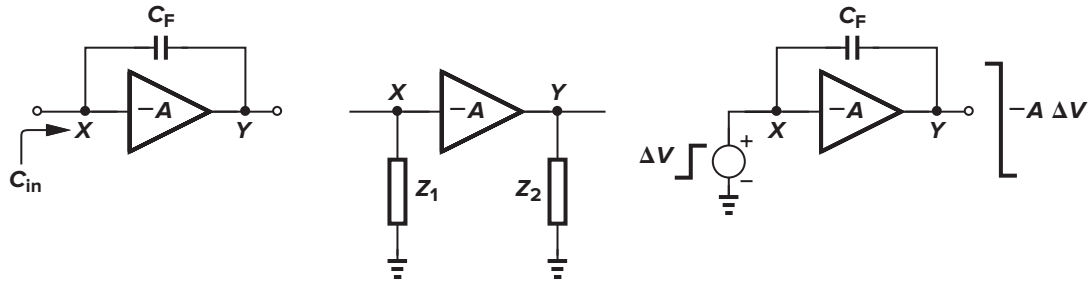


Figure 6.3

Solution

Using Miller's theorem to convert the circuit to that shown in Fig. 6.3(b), we have $Z = 1/(C_F s)$ and $Z_1 = [1/(C_F s)]/(1 + A)$. That is, the input capacitance is equal to $C_F(1 + A)$. We call this effect "Miller multiplication" of the capacitor.

Why is C_F multiplied by $1 + A$? Suppose, as depicted in Fig. 6.3(c), we measure the input capacitance by applying a voltage step at the input and calculating the charge supplied by the voltage source. A step equal to ΔV at X results in a change of $-A\Delta V$ at Y, yielding a total change of $(1 + A)\Delta V$ in the voltage across C_F. Thus, the charge drawn by C_F from V_{in} is equal to $(1 + A)C_F\Delta V$ and the equivalent input capacitance equal to $(1 + A)C_F$. ◀

▶ **Example 6.2**

A student needs a large capacitor for a filter and decides to utilize the Miller multiplication of [Fig. 6.4(a)]. Explain the issues in this approach.

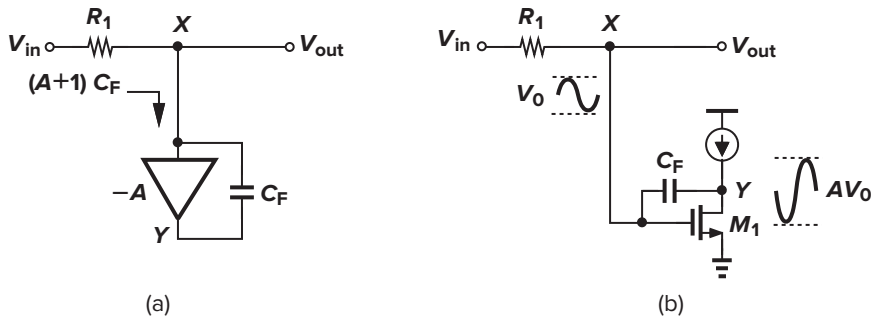


Figure 6.4

Solution

The issues relate to the amplifier, particularly to its output swing. As exemplified by the implementation in Fig. 6.4(b), if the voltage at X swings by V_0, then Y must accommodate a swing of AV_0 without saturating the amplifier. In addition, the dc level in V_{in} must be compatible with the input of the amplifier. ◀

It is important to understand that (6.2) and (6.3) hold *if* we know a priori that the circuit of Fig. 6.2(a) can be converted to that of Fig. 6.2(b). That is, Miller's theorem does not stipulate the conditions under which this conversion is valid. If the impedance Z forms the only signal path between X and Y, then the conversion is often invalid. Illustrated in Fig. 6.5 for a simple resistive divider, the theorem gives a correct

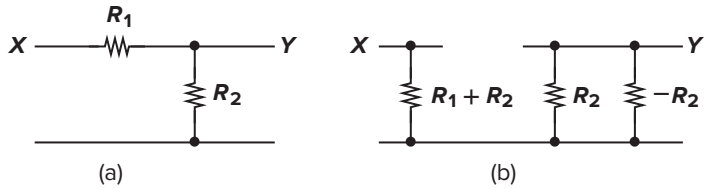


Figure 6.5 Improper application of Miller's theorem.

input impedance but an incorrect gain. Nevertheless, Miller's theorem proves useful in cases where the impedance Z appears in parallel with the main signal (Fig. 6.6).

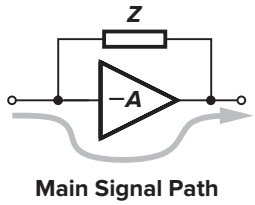


Figure 6.6 Typical case for valid application of Miller's theorem.

▶ Example 6.3

Calculate the input resistance of the circuit shown in Fig. 6.7(a).

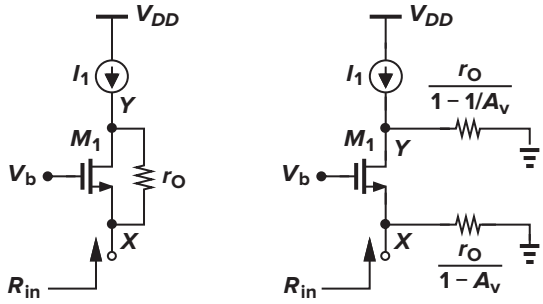


Figure 6.7

Solution

The reader can prove that the voltage gain from X to Y is equal to $1 + (g_m + g_{mb})r_O$. As shown in Fig. 6.7(b), the input resistance is given by the parallel combination of $r_O/(1 - A_v)$ and $1/(g_m + g_{mb})$. Since A_v is usually greater than unity, $r_O/(1 - A_v)$ is a *negative* resistance. We therefore have

$$R_{in} = \frac{r_O}{1 - [1 + (g_m + g_{mb})r_O]} \Big\| \frac{1}{g_m + g_{mb}} \tag{6.4}$$

$$= \frac{-1}{g_m + g_{mb}} \Big\| \frac{1}{g_m + g_{mb}} \tag{6.5}$$

$$= \infty \tag{6.6}$$

This is the same result as obtained in Chapter 3 (Fig. 3.54) by direct calculation.

◀

We should also mention that, strictly speaking, the value of $A_v = V_Y/V_X$ in (6.2) and (6.3) must be calculated at the frequency of interest, complicating the algebra significantly. To understand this point, let us return to Example 6.1 and assume an amplifier with a finite output resistance. Depicted in Fig. 6.8, the equivalent circuit reveals that $V_Y \neq -AV_X$ at high frequencies, and hence C_F cannot be simply multiplied by $1+A$ to yield the input capacitance. However, in many cases we use the low-frequency value of V_Y/V_X to gain insight into the behavior of the circuit. We call this approach "Miller's approximation."

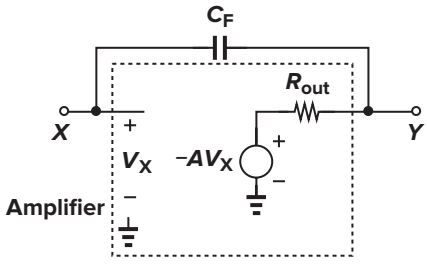


Figure 6.8 Equivalent circuit showing gain change at high frequencies.

▶ Example 6.4

Determine the transfer function of the circuit shown in Fig. 6.9(a) using (a) direct analysis and (b) Miller's approximation.

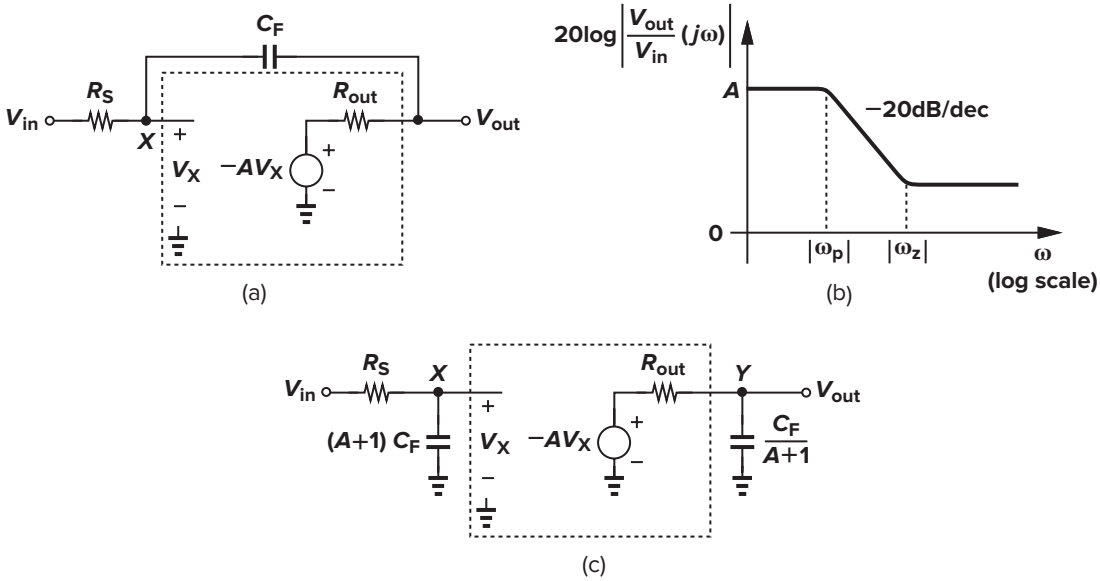


Figure 6.9

Solution

(a) We note that the current flowing through R_S is given by $(V_{in} - V_X)/R_S$, yielding a voltage drop across R_{out} equal to $(V_{in} - V_X)R_{out}/R_S$. It follows that

$$\frac{V_{in} - V_X}{R_S} R_{out} - AV_X = V_{out} \tag{6.7}$$

We also equate the currents flowing through R_S and C_F:

$$\frac{V_{in} - V_X}{R_S} = (V_X - V_{out})C_F s \tag{6.8}$$

The reader can find V_X from the first equation and substitute the result in the second, thereby obtaining

$$\frac{V_{out}}{V_{in}}(s) = \frac{R_{out}C_F s - A}{[(A+1)R_S + R_{out}]C_F s + 1} \tag{6.9}$$

The circuit thus exhibits a zero at $\omega_z = A/(R_{out}C_F)$ and a pole at $\omega_p = -1/[(A+1)R_S C_F + R_{out}C_F]$. Figure 6.9(b) plots the response for the case of $|\omega_p| < |\omega_z|$.

(b) Applying Miller's approximation, we decompose C_F into $(1+A)C_F$ at the input and $C_F/(1+A^{-1})$ at the output [Fig. 6.9(c)]. Since $V_{out}/V_{in} = (V_X/V_{in})(V_{out}/V_X)$, we first write V_X/V_{in} by considering R_S and $(1+A)C_F$ as a voltage divider:

$$\frac{V_X}{V_{in}} = \frac{\dfrac{1}{(1+A)C_F s}}{\dfrac{1}{(1+A)C_F s} + R_S} \tag{6.10}$$

$$= \frac{1}{(1+A)R_S C_F s + 1} \tag{6.11}$$

As for V_{out}/V_X, we first amplify V_X by $-A$ and subject the result to the output voltage divider,

$$\frac{V_{out}}{V_X} = \frac{-A}{\dfrac{1}{1+A^{-1}}C_F R_{out} s + 1} \tag{6.12}$$

That is

$$\frac{V_{out}}{V_{in}}(s) = \frac{-A}{[(1+A)R_S C_F s + 1]\left(\dfrac{1}{1+A^{-1}}C_F R_{out} s + 1\right)} \tag{6.13}$$

Sadly, Miller's approximation has eliminated the zero and predicted *two* poles for the circuit! Despite these shortcomings, Miller's approximation can provide intuition in many cases.[1] ◀

If applied to obtain the input-output transfer function, Miller's theorem cannot be used simultaneously to calculate the output impedance. To derive the transfer function, we apply a voltage source to the *input* of the circuit, obtaining a value for V_Y/V_X in Fig. 6.2(a). On the other hand, to determine the output impedance, we must apply a voltage source to the *output* of the circuit, obtaining a value for V_X/V_Y that may not be equal to the inverse of the V_Y/V_X measured in the first test. For example, the circuit of Fig. 6.7(b) may suggest that the output impedance is equal to

$$R_{out} = \frac{r_O}{1 - 1/A_v} \tag{6.14}$$

$$= \frac{r_O}{1 - [1 + (g_m + g_{mb})r_O]^{-1}} \tag{6.15}$$

$$= \frac{1}{g_m + g_{mb}} + r_O \tag{6.16}$$

[1] Both of these artifacts can be avoided if we multiply C_F by $1 + A(s)$, where $A(s)$ is the actual transfer function from V_X to V_{out}, but the algebra is as lengthy as that in part (a).

whereas the actual value is equal to r_O (if X is grounded). Other subtleties of Miller's theorem are described in the Appendix C.

In summary, Miller's approximation divides a floating impedance by the low-frequency gain and faces the following limitations: (1) it may eliminate zeros, (2) it may predict additional poles, and (3) it does not correctly compute the "output" impedance.

6.1.2 Association of Poles with Nodes

Consider the simple cascade of amplifiers depicted in Fig. 6.10. Here, A_1 and A_2 are ideal voltage amplifiers, R_1 and R_2 model the output resistance of each stage, C_{in} and C_N represent the input capacitance of each stage, and C_P denotes the load capacitance. The overall transfer function can be written as

$$\frac{V_{out}}{V_{in}}(s) = \frac{A_1}{1 + R_S C_{in} s} \cdot \frac{A_2}{1 + R_1 C_N s} \cdot \frac{1}{1 + R_2 C_P s} \tag{6.17}$$

The circuit exhibits three poles, each of which is determined by the total capacitance seen from each node to ground multiplied by the total resistance seen at the node to ground. We can therefore associate each pole with one node of the circuit, i.e., $\omega_j = \tau_j^{-1}$, where τ_j is the product of the capacitance and resistance seen at node j to ground. From this perspective, we may say that "each node in the circuit contributes one pole to the transfer function."

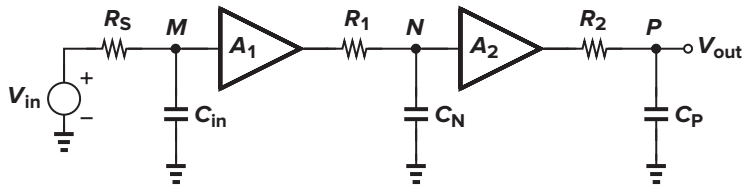


Figure 6.10 Cascade of amplifiers.

The above statement is not valid in general. For example, in the circuit of Fig. 6.11, the location of the poles is difficult to calculate because R_3 and C_3 create interaction between X and Y. Nevertheless, in many circuits, association of one pole with each node provides an intuitive approach to estimating the transfer function: we simply multiply the total equivalent capacitance by the total incremental (small-signal) resistance (both from the node of interest to ground), thus obtaining an equivalent time constant and hence a pole frequency.

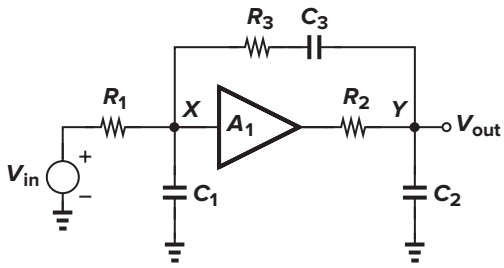


Figure 6.11 Example of interaction between nodes.

▶ **Example 6.5**

Neglecting channel-length modulation, compute the transfer function of the common-gate stage shown in Fig. 6.12(a).

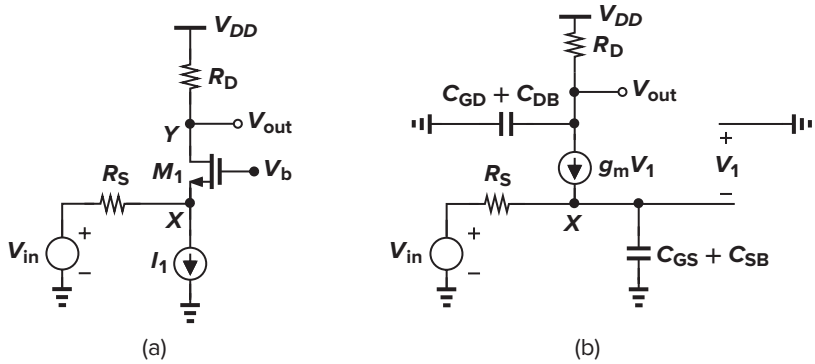


Figure 6.12 Common-gate stage with parasitic capacitances.

Solution

In this circuit, the capacitances contributed by M_1 are connected from the input and output nodes to ground [Fig. 6.12(b)]. At node X, $C_S = C_{GS} + C_{SB}$, giving a pole frequency

$$\omega_{in} = \left[(C_{GS} + C_{SB}) \left(R_S \left\| \frac{1}{g_m + g_{mb}} \right. \right) \right]^{-1} \tag{6.18}$$

Similarly, at node Y, $C_D = C_{DG} + C_{DB}$, yielding a pole frequency

$$\omega_{out} = [(C_{DG} + C_{DB}) R_D]^{-1} \tag{6.19}$$

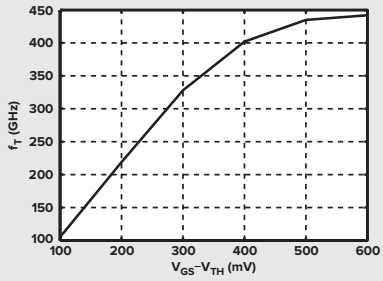
The overall transfer function is thus given by

$$\frac{V_{out}}{V_{in}}(s) = \frac{(g_m + g_{mb}) R_D}{1 + (g_m + g_{mb}) R_S} \cdot \frac{1}{\left(1 + \dfrac{s}{\omega_{in}}\right)\left(1 + \dfrac{s}{\omega_{out}}\right)} \tag{6.20}$$

where the first fraction represents the low-frequency gain of the circuit. Note that if we do not neglect r_{O1}, the input and output nodes interact, making it difficult to calculate the poles. ◀

Nanometer Design Notes

Defined as the frequency at which the small-signal current gain of a device is unity, the transit frequency, f_T, of MOSFETs increases with the overdrive, but flattens out as the vertical electric field reduces the mobility. Plotted below is the f_T for an NMOS device with $W/L = 5\ \mu$m/40 nm and $V_{DS} = 0.8$ V.



As observed in Example 6.4, Miller's approximation converts a floating impedance to two grounded impedances, allowing us to associate one pole with each node. We apply this technique to various amplifier topologies in this chapter—but cautiously and retrospectively to avoid its pitfalls. It is also helpful to bear in mind that the f_T of a MOS transistor is roughly equal to $g_m/(2\pi C_{GS})$ and can exceed 300 GHz in today's technologies. (However, since $f_T \propto V_{GS} - V_{TH}$, as we push the devices for low-voltage operation, we tend to reduce their f_T's.)

6.2 ■ Common-Source Stage

The common-source topology exhibits a relatively high input impedance while providing voltage gain and requiring a minimal voltage headroom. As such, it finds wide application in analog circuits and its frequency response is of interest.

Shown in Fig. 6.13(a) is a common-source stage driven by a finite source resistance, R_S.[2] We identify all of the capacitances in the circuit, noting that C_{GS} and C_{DB} are "grounded" capacitances while C_{GD} appears between the input and the output. In reality, the circuit also drives a load capacitance, which can be merged with C_{DB}.

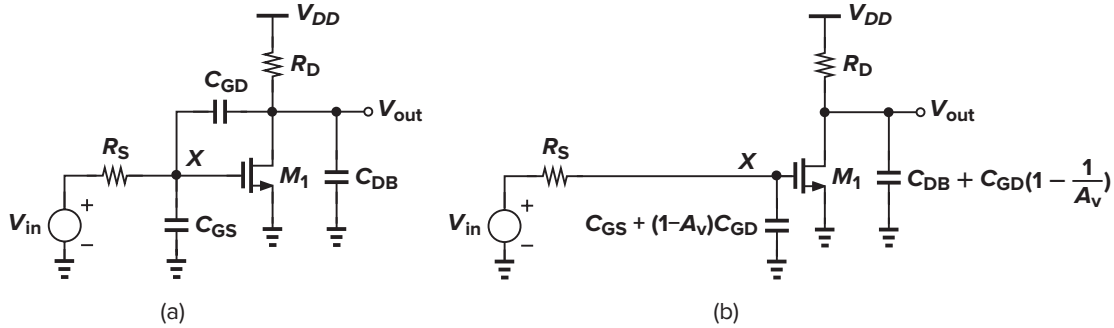


Figure 6.13 (a) High-frequency model of a common-source stage, and (b) simplified circuit using Miller's approximation.

Miller's Approximation Assuming that $\lambda = 0$ and M_1 operates in saturation, let us first estimate the transfer function by associating one pole with each node. The total capacitance seen from X to ground is equal to C_{GS} plus the Miller multiplication of C_{GD}, namely, $C_{GS} + (1 - A_v)C_{GD}$, where $A_v = -g_m R_D$ [Fig. 6.13(b)]. The magnitude of the "input" pole is therefore given by

$$\omega_{in} = \frac{1}{R_S[C_{GS} + (1 + g_m R_D)C_{GD}]} \tag{6.21}$$

At the output node, the total capacitance seen to ground is equal to C_{DB} plus the Miller effect of C_{GD}, i.e., $C_{DB} + (1 - A_v^{-1})C_{GD} \approx C_{DB} + C_{GD}$ (if $A_v \gg 1$). Thus,

$$\omega_{out} = \frac{1}{R_D(C_{DB} + C_{GD})} \tag{6.22}$$

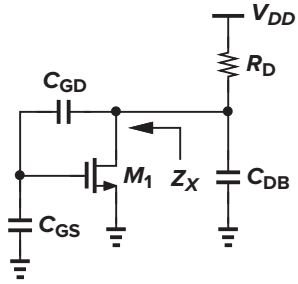


Figure 6.14 Model for calculation of output impedance.

Another approximation of the output pole can be obtained if R_S is relatively large. Simplifying the circuit as shown in Fig. 6.14, where the effect of R_S is neglected, the reader can prove that

$$Z_X = \frac{1}{C_{eq}s} \left\| \left(\frac{C_{GD} + C_{GS}}{C_{GD}} \cdot \frac{1}{g_{m1}} \right) \right. \tag{6.23}$$

[2]Note that R_S is not deliberately added to the circuit. Rather, it models the output resistance of the preceding stage.

where $C_{eq} = C_{GD}C_{GS}/(C_{GD} + C_{GS})$. Thus, the output pole is roughly equal to

$$\omega_{out} = \frac{1}{\left[R_D \left\| \left(\frac{C_{GD} + C_{GS}}{C_{GD}} \cdot \frac{1}{g_{m1}} \right) \right.\right] (C_{eq} + C_{DB})} \tag{6.24}$$

We should point out that the sign of ω_{in} and ω_{out} in the above equations is positive because we eventually write the denominator of the transfer function in the form of $(1 + s/\omega_{in})(1 + s/\omega_{out})$; i.e., the denominator vanishes at $s = -\omega_{in}$ and $s = -\omega_{out}$. Alternatively, we could express the values of ω_{in} and ω_{out} with a negative sign and hence write the denominator as $(1 - s/\omega_{in})(1 - s/\omega_{out})$. We adopt the former notation in this book. We then surmise that the transfer function is

$$\frac{V_{out}}{V_{in}}(s) = \frac{-g_m R_D}{\left(1 + \frac{s}{\omega_{in}}\right)\left(1 + \frac{s}{\omega_{out}}\right)} \tag{6.25}$$

Note that r_{O1} and any load capacitance can easily be included here.

The primary error in this estimation is that we have not considered the existence of zeros in the circuit. Another concern stems from approximating the gain of the amplifier by $-g_m R_D$ whereas in reality the gain varies with frequency (for example, due to the capacitance at the output node).

Direct Analysis We now obtain the exact transfer function, investigating the validity of the above approach. Using the equivalent circuit depicted in Fig. 6.15, we can sum the currents at each node:

$$\frac{V_X - V_{in}}{R_S} + V_X C_{GS} s + (V_X - V_{out}) C_{GD} s = 0 \tag{6.26}$$

$$(V_{out} - V_X) C_{GD} s + g_m V_X + V_{out}\left(\frac{1}{R_D} + C_{DB} s\right) = 0 \tag{6.27}$$

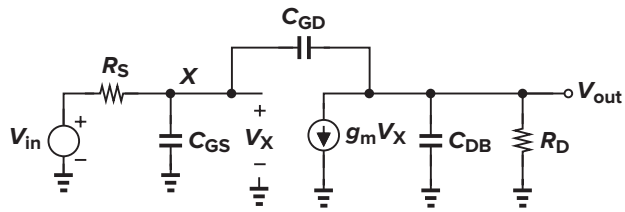


Figure 6.15 Equivalent circuit of Fig. 6.13.

From (6.27), V_X is obtained as

$$V_X = -\frac{V_{out}\left(C_{GD} s + \frac{1}{R_D} + C_{DB} s\right)}{g_m - C_{GD} s} \tag{6.28}$$

which, upon substitution in (6.26), yields

$$-V_{out}\frac{[R_S^{-1} + (C_{GS} + C_{GD})s][R_D^{-1} + (C_{GD} + C_{DB})s]}{g_m - C_{GD} s} - V_{out} C_{GD} s = \frac{V_{in}}{R_S} \tag{6.29}$$

That is

$$\frac{V_{out}}{V_{in}}(s) = \frac{(C_{GD}s - g_m)R_D}{R_S R_D \xi s^2 + [R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})]s + 1} \tag{6.30}$$

where $\xi = C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB}$. Note that the transfer function is of second order even though the circuit contains three capacitors. This is because the capacitors form a "loop," allowing only *two* independent initial conditions in the circuit and hence yielding a second-order differential equation for the time response.

▶ **Example 6.6**

A student considers only C_{GD} in Fig. 6.13(a) so as to obtain a one-pole response, reasons that the voltage gain drops by 3 dB (by a factor of $= \sqrt{2}$) at the pole frequency, and concludes that a better approximation of the Miller effect should multiply C_{GD} by $1 + g_m R_D\sqrt{2}$. Explain the flaw in this reasoning.

Solution

Setting C_{GS} and C_{DB} to zero, we obtain

$$\frac{V_{out}}{V_{in}}(s) = \frac{(C_{GD}s - g_m)R_D}{\dfrac{s}{\omega_0} + 1} \tag{6.31}$$

where $\omega_0 = R_S(1 + g_m R_D)C_{GD} + R_D C_{GD}$. We note that C_{GD} is multiplied by $1 + g_m R_D$ in this exact analysis. So where is the flaw in the student's argument? It is true that the voltage gain in Fig. 6.13(a) falls by $\sqrt{2}$ at ω_0, but this gain would be from V_{in} to V_{out} and *not* the gain seen by C_{GD}. The reader can readily express the transfer function from node X to V_{out} as

$$\frac{V_{out}}{V_X}(s) = \frac{(C_{GD}s - g_m)R_D}{R_D C_{GD} + 1} \tag{6.32}$$

observing that this gain begins to roll off at a *higher* frequency, namely, at $1/(R_D C_{GD})$. Thus, the multiplication of C_{GD} by $1 + g_m R_D$ is still justified. ◀

Special Cases If manipulated judiciously, Eq. (6.30) reveals several interesting points about the circuit. While the denominator appears rather complicated, it can yield intuitive expressions for the two poles, ω_{p1} and ω_{p2}, if we assume that $|\omega_{p1}| \ll |\omega_{p2}|$. This is called the "dominant pole" approximation. Writing the denominator as

$$D = \left(\frac{s}{\omega_{p1}} + 1\right)\left(\frac{s}{\omega_{p2}} + 1\right) \tag{6.33}$$

$$= \frac{s^2}{\omega_{p1}\omega_{p2}} + \left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}}\right)s + 1 \tag{6.34}$$

we recognize that the coefficient of s is approximately equal to $1/\omega_{p1}$ if ω_{p2} is much farther from the origin. It follows from (6.30) that the dominant pole is given by

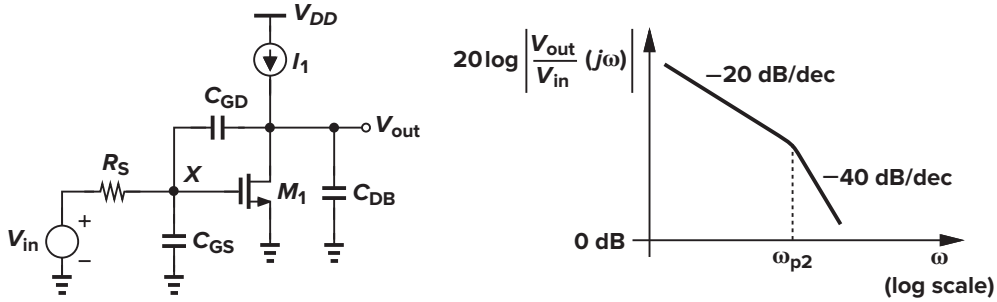
$$\omega_{p1} = \frac{1}{R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})} \tag{6.35}$$

How does this compare with the "input" pole given by (6.21)? The only difference results from the term $R_D(C_{GD}+C_{DB})$, which may be negligible in some cases. The key point here is that the intuitive approach of associating a pole with the input node provides a rough estimate with much less effort. We also note that the Miller multiplication of C_{GD} by the low-frequency gain of the amplifier is relatively accurate in this case. Of course, for a given set of values, we must check to ensure that $\omega_{p1} \ll \omega_{p2}$.

Other special cases are also of interest. We consider the case of $C_{GD} = 0$ in Problem 6.26 and the case of $R_D = \infty$ below.

▶ Example 6.7

The circuit shown in Fig. 6.16(a) is a special case where $R_D \to \infty$. Calculate the transfer function (with $\lambda = 0$) and explain why the Miller effect vanishes as C_{DB} (or the load capacitance) increases.



(a) (b)

Figure 6.16

Solution

Using (6.30) and letting R_D approach infinity, we have

$$\frac{V_{out}}{V_{in}}(s) = \frac{C_{GD}s - g_m}{R_S\xi s^2 + [g_m R_S C_{GD} + (C_{GD} + C_{DB})]s} \tag{6.36}$$

$$= \frac{C_{GD}s - g_m}{s[R_S(C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB})s + (g_m R_S + 1)C_{GD} + C_{DB}]}$$

As expected, the circuit exhibits two poles—one at the origin because the dc gain is infinity [Fig. 6.16(b)]. The magnitude of the other pole is given by

$$\omega_{p2} \approx \frac{(1 + g_m R_S)C_{GD} + C_{DB}}{R_S(C_{GD}C_{GS} + C_{GS}C_{DB} + C_{GD}C_{DB})} \tag{6.37}$$

For a large C_{DB} or load capacitance, this expression reduces to

$$\omega_{p2} \approx \frac{1}{R_S(C_{GS} + C_{GD})} \tag{6.38}$$

indicating that C_{GD} experiences no Miller multiplication. This can be explained by noting that, for a large C_{DB}, the voltage gain from node X to the output begins to drop even at low frequencies. As a result, for frequencies close to $[R_S(C_{GS} + C_{GD})]^{-1}$, the effective gain is quite small and $C_{GD}(1 - A_v) \approx C_{GD}$. Such a case is an example where the application of the Miller effect using low-frequency gain does not provide a reasonable estimate. ◀

From (6.30) and applying the dominant pole approximation, we can also estimate the second pole of the CS stage of Fig. 6.13(a). Since the coefficient of s^2 is equal to $(\omega_{p1}\omega_{p2})^{-1}$, we have

$$\omega_{p2} = \frac{1}{\omega_{p1}} \cdot \frac{1}{R_S R_D (C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB})} \tag{6.39}$$

$$= \frac{R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})}{R_S R_D (C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB})} \tag{6.40}$$

We emphasize that these results hold only if $\omega_{p1} \ll \omega_{p2}$.

As a special case, if $C_{GS} \gg (1 + g_m R_D)C_{GD} + R_D(C_{GD} + C_{DB})/R_S$, then

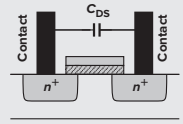
$$\omega_{p2} \approx \frac{R_S C_{GS}}{R_S R_D (C_{GS}C_{GD} + C_{GS}C_{DB})} \tag{6.41}$$

$$= \frac{1}{R_D(C_{GD} + C_{DB})} \tag{6.42}$$

the same as (6.22). Thus, the "output" pole approach is valid only if C_{GS} dominates the response.

Nanometer Design Notes

The high-frequency MOS model developed in Chapter 2 does not contain a drain-source capacitance. In reality, however, the metal contact stacks touching the source and drain areas form two "columns" that create a capacitance between the drain and the source. This effect has become more pronounced in modern CMOS technologies because of the shorter channel length, i.e., less spacing between the columns, and the ability to stack many contacts, i.e., taller columns. The reader is encouraged to analyze a C_G stage while including C_{DS}.



The transfer function of (6.30) exhibits a zero given by $\omega_z = +g_m/C_{GD}$, an effect not predicted by Miller's approximation and (6.25). Located in the *right* half plane, the zero arises from direct coupling of the input to the output through C_{GD}. As illustrated in Fig. 6.17, C_{GD} provides a feedthrough path that conducts the input signal to the output at very high frequencies, resulting in a slope in the frequency response that is less negative than −40 dB/dec. Note that $g_m/C_{GD} > g_m/C_{GS}$ because $C_{GD} < C_{GS}$, implying that the zero lies beyond the transistor's f_T. However, as explained in Chapter 10, this zero falls to lower frequencies in cases where we deliberately add a capacitor between the gate and the drain, introducing other difficulties.

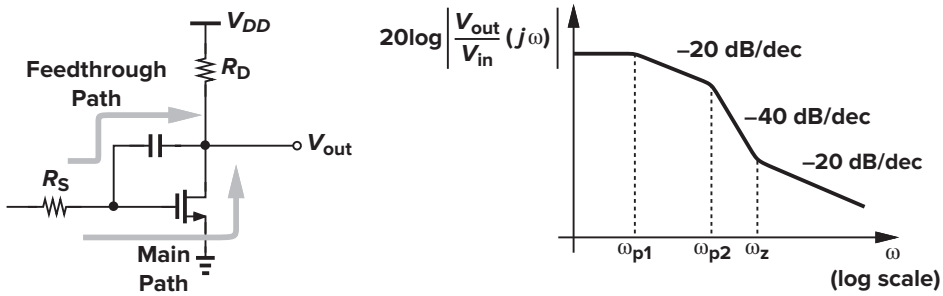


Figure 6.17 Feedforward path through C_{GD} (log-log scale).

The zero, s_z, can also be computed by noting that the transfer function $V_{out}(s)/V_{in}(s)$ must drop to zero for $s = s_z$. For a finite V_{in}, this means that $V_{out}(s_z) = 0$, and hence the output can be *shorted* to ground at this (possibly complex) frequency with no current flowing through R_D or the short (Fig. 6.18). Therefore, the currents through C_{GD} and M_1 are equal and opposite:

$$V_1 C_{GD} s_z = g_m V_1 \tag{6.43}$$

That is, $s_z = +g_m/C_{GD}$.[3]

[3]This approach is similar to expressing the transfer function as $G_m Z_{out}$ and finding the zeros of G_m and Z_{out}.

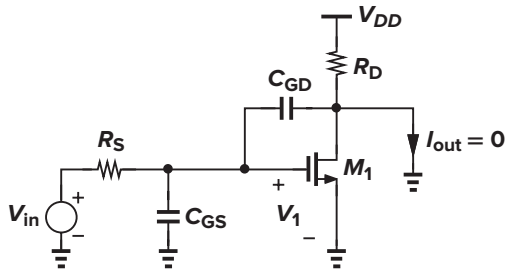


Figure 6.18 Calculation of the zero in a CS stage.

▶ Example 6.8

We have seen that the signals traveling through two paths within an amplifier may cancel each other at one frequency, creating a zero in the transfer function (Fig. 6.19). Can this occur if $H_1(s)$ and $H_2(s)$ are first-order low-pass circuits?

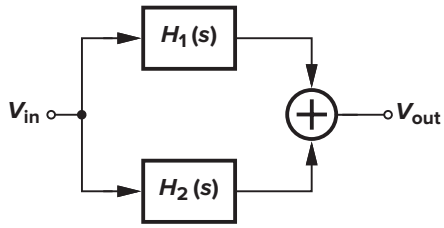


Figure 6.19

Solution

Modeling $H_1(s)$ by $A_1/(1 + s/\omega_{p1})$ and $H_2(s)$ by $A_2/(1 + s/\omega_{p2})$, we have

$$\frac{V_{out}}{V_{in}}(s) = \frac{\left(\dfrac{A_1}{\omega_{p2}} + \dfrac{A_2}{\omega_{p1}}\right) s + A_1 + A_2}{\left(1 + \dfrac{s}{\omega_{p1}}\right)\left(1 + \dfrac{s}{\omega_{p2}}\right)} \tag{6.44}$$

Indeed, the overall transfer function contains a zero. ◀

▶ Example 6.9

Determine the transfer function of the complementary CS stage shown in Fig. 6.20(a).

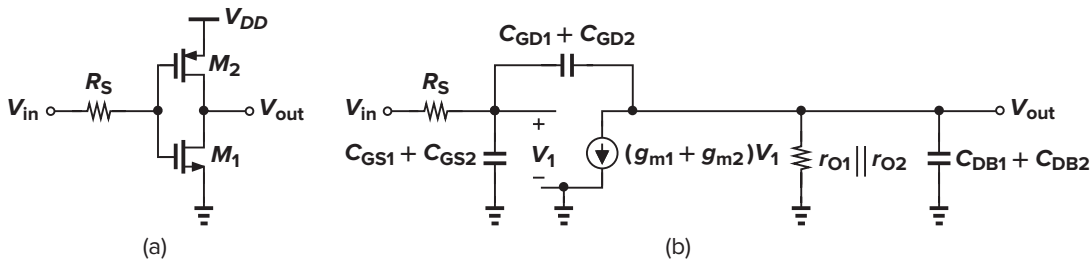


Figure 6.20

Solution

Since the corresponding terminals of M_1 and M_2 are shorted to one another in the small-signal model, we merge the two transistors, drawing the equivalent circuit as shown in Fig. 6.20(b). The circuit thus has the same transfer function as the simple CS stage studied above. ◀

In high-speed applications, the input impedance of the common-source stage is also important. With the aid of Miller's approximation, we have from Fig. 6.21(a)

$$Z_{in} = \frac{1}{[C_{GS} + (1 + g_m R_D)C_{GD}]s} \tag{6.45}$$

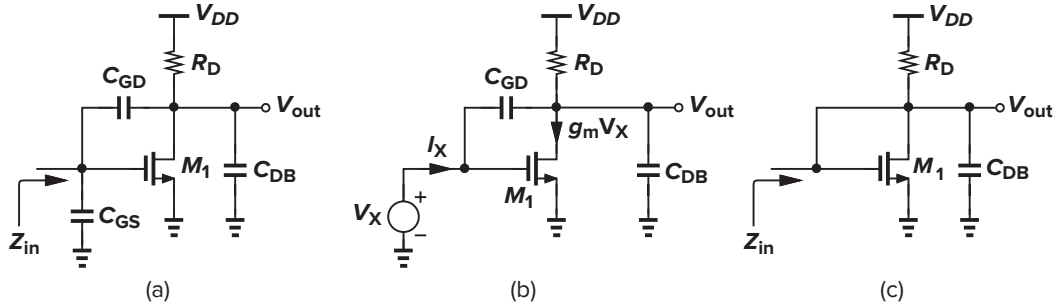


Figure 6.21 Calculation of input impedance of a CS stage.

But at high frequencies, the effect of the output node capacitance must be taken into account. Ignoring C_{GS} for the moment and using the circuit of Fig. 6.21(b), we add the voltage drops across $R_D||(C_{DB}s)^{-1}$ and C_{GD}, equating the result to V_X:

$$(I_X - g_m V_X)\frac{R_D}{1 + R_D C_{DB} s} + \frac{I_X}{C_{GD} s} = V_X \tag{6.46}$$

and hence

$$\frac{V_X}{I_X} = \frac{1 + R_D(C_{GD} + C_{DB})s}{C_{GD}s(1 + g_m R_D + R_D C_{DB} s)} \tag{6.47}$$

The actual input impedance consists of the parallel combination of (6.47) and $1/(C_{GS}s)$.

As a special case, suppose that at the frequency of interest, $|R_D(C_{GD}+C_{DB})s| \ll 1$ and $|R_D C_{DB} s| \ll 1+g_m R_D$. Then, (6.47) reduces to $[(1+g_m R_D)C_{GD}s]^{-1}$ (as expected), indicating that the input impedance is primarily capacitive. At higher frequencies, however, (6.47) contains both real and imaginary parts. In fact, if C_{GD} is large, it provides a low-impedance path between the gate and the drain of M_1, yielding the equivalent circuit of Fig. 6.21(c) and suggesting that $1/g_{m1}$ and R_D appear in parallel with the input.

▶ **Example 6.10**

Explain what happens to Eq. (6.47) if the circuit drives a large load capacitance.

Solution

Merged with C_{DB}, the large load capacitance reduces the numerator to $R_D C_{DB} s$ and the denominator to $C_{GD}s(R_D C_{DB} s)$, yielding $V_X/I_X \approx 1/(C_{GD}s)$. In a manner similar to that in Example 6.7, the large load capacitance lowers the gain at high frequencies, suppressing Miller multiplication of C_{GD}. ◀

CHAPTER

8

Feedback

On a mild August morning in 1927, Harold Black was riding the ferry from New York to New Jersey, where he worked at Bell Laboratories. Black and many other researchers had been investigating the problem of nonlinearity in amplifiers used in long-distance telephone networks, seeking a practical solution. While reading the newspaper on the ferry, Black was suddenly struck by an idea and began to draw a diagram on the newspaper, which would later be used as the evidence in his patent application. The idea is known to us as the negative-feedback amplifier.

Feedback is a powerful technique that finds wide application in analog circuits. For example, negative feedback allows high-precision signal processing, and positive feedback makes it possible to build oscillators. In this chapter, we consider only negative feedback and use the term feedback to mean that.

We begin with a general view of feedback circuits, describing important benefits that result from feedback. Next, we study four feedback topologies and their properties. We then deal with difficulties in feedback circuit analysis and introduce the two-port technique, Bode's technique, and Blackman's theorem as possible solutions.

8.1 ■ General Considerations

Figure 8.1 shows a negative-feedback system, where $H(s)$ and $G(s)$ are called the feedforward and the feedback networks, respectively. Since the output of $G(s)$ is equal to $G(s)Y(s)$, the input to $H(s)$, called the feedback error, is given by $X(s) - G(s)Y(s)$. That is

$$Y(s) = H(s)[X(s) - G(s)Y(s)] \tag{8.1}$$

Thus,

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 + G(s)H(s)} \tag{8.2}$$

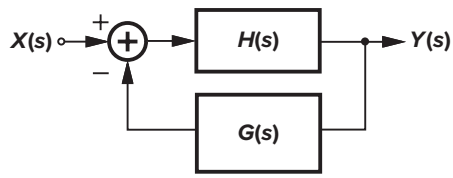


Figure 8.1 General feedback system.

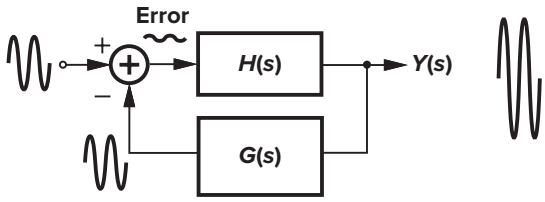


Figure 8.2 Similarity between output of feedback network and input signal.

We call $H(s)$ the "open-loop" transfer function and $Y(s)/X(s)$ the "closed-loop" transfer function. In most cases of interest in this book, $H(s)$ represents an amplifier and $G(s)$ is a frequency-independent quantity. In other words, a fraction of the output signal is sensed and compared with the input, generating an error term. In a well-designed negative-feedback system, the error term is minimized, thereby making the output of $G(s)$ an accurate "copy" of the input and hence the output of the system a faithful (scaled) replica of the input (Fig. 8.2). We also say that the input of $H(s)$ is a "virtual ground" because the signal amplitude at this point is small. In subsequent developments, we replace $G(s)$ by a frequency-independent quantity β and call it the "feedback factor."

It is instructive to identify four elements in the feedback system of Fig. 8.1: (1) the feedforward amplifier, (2) a means of sensing the output, (3) the feedback network, and (4) a means of generating the feedback error, i.e., a subtractor (or an adder). These elements exist in every feedback system, even though they may not be obvious in cases such as a simple common-source stage with resistive degeneration.

8.1.1 Properties of Feedback Circuits

Before proceeding to the analysis of feedback circuits, we study some simple examples to describe the benefits of negative feedback.

Gain Desensitization Consider the common-source stage shown in Fig. 8.3(a), where the voltage gain is equal to $g_{m1}r_{O1}$. A critical drawback of this circuit is the poor definition of the gain: both g_{m1} and r_{O1} vary with process and temperature. Now suppose the circuit is configured as in Fig. 8.3(b), where the gate bias of M_1 is set by means not shown here (Chapter 13). Let us calculate the overall voltage gain of the circuit at relatively low frequencies such that C_2 draws a negligible (small-signal) current from the output node, i.e., $V_{out}/V_X = -g_{m1}r_{O1}$ because the entire drain current flows through r_{O1}. Since $(V_{out} - V_X)C_2 s = (V_X - V_{in})C_1 s$, we have

$$\frac{V_{out}}{V_{in}} = -\frac{1}{\left(1 + \dfrac{1}{g_{m1}r_{O1}}\right)\dfrac{C_2}{C_1} + \dfrac{1}{g_{m1}r_{O1}}} \tag{8.3}$$

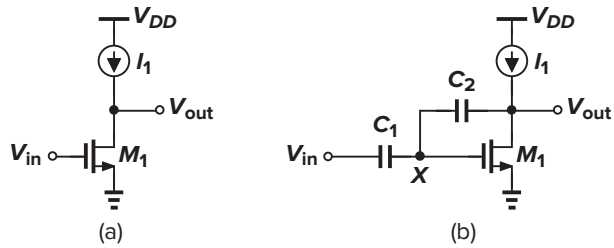


Figure 8.3 (a) Simple common-source stage; (b) circuit of (a) with feedback.

If $g_{m1}r_{O1}$ is sufficiently large, the $1/(g_{m1}r_{O1})$ terms in the denominator can be neglected, yielding

$$\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2} \tag{8.4}$$

Compared to $g_{m1}r_{O1}$, this gain can be controlled with much higher accuracy because it is given by the *ratio* of two capacitors. If C_1 and C_2 are made of the same material, then process and temperature variations do not change C_1/C_2.

The above example reveals that negative feedback provides gain "desensitization," i.e., the closed-loop gain is less sensitive to device parameters than the open-loop gain is. One may also say that negative feedback "stabilizes" the gain and hence "improves the stability." But this nomenclature may be confused with frequency stability (Chapter 10), which typically *worsens* as a result of negative feedback. Illustrated for a more general case in Fig. 8.4, gain desensitization can be quantified by writing

$$\frac{Y}{X} = \frac{A}{1+\beta A} \tag{8.5}$$

$$\approx \frac{1}{\beta}\left(1 - \frac{1}{\beta A}\right) \tag{8.6}$$

where we have assumed that $\beta A \gg 1$. We note that the closed-loop gain is determined, to the first order by the feedback factor, β. More important, even if the open-loop gain, A, varies by a factor of, say, 2, Y/X varies by a small percentage because $1/(\beta A) \ll 1$.

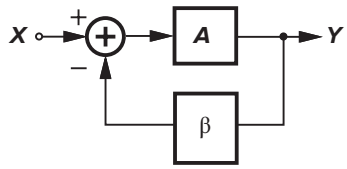


Figure 8.4 Simple feedback system.

Called the "loop gain," the quantity βA plays an important role in feedback systems.[1] We see from (8.6) that the higher βA is, the less sensitive Y/X will be to variations in A. From another perspective, the accuracy of the closed-loop gain improves by maximizing βA. Note that as β increases, the closed-loop gain, $Y/X \approx 1/\beta$, decreases, suggesting a trade-off between precision and the closed-loop gain. In other words, we begin with a high-gain amplifier and apply feedback to obtain a low, but less sensitive, closed-loop gain. Another conclusion here is that the output of the feedback network is equal to $\beta Y = X \cdot \beta A/(1+\beta A)$, approaching X as βA becomes much greater than unity. This result agrees with the illustration in Fig. 8.2.

The calculation of the loop gain can proceed as follows. As illustrated in Fig. 8.5, we set the main input to (ac) zero, break the loop at some point, inject a test signal in the "right direction," follow the signal around the loop, and obtain the value that returns to the break point. The negative of the transfer function thus derived is the loop gain. Note that the loop gain is a dimensionless quantity. In Fig. 8.5, we have $V_t\beta(-1)A = V_F$ and hence $V_F/V_t = -\beta A$. Similarly, as depicted in Fig. 8.6, for the simple feedback circuit, we can write $V_X = V_t C_2/(C_1+C_2)$ and[2]

$$V_t \frac{C_2}{C_1+C_2}(-g_{m1}r_{O1}) = V_F \tag{8.7}$$

[1] The loop gain, βA, and the open-loop gain, A, must not be confused with each other.

[2] A common mistake here is to say that C_2 does not pass signals at very low frequencies, and hence $V_X = 0$. This is not true because C_1 also has a high impedance at very low frequencies.

We should emphasize that the desensitization of gain by feedback leads to many other properties of feedback systems. Our examination of Eq. (8.6) indicates that large variations in A affect Y/X negligibly if βA is large. Such variations can arise from different sources: process, temperature, frequency, and loading. For example, if A drops at high frequencies, Y/X varies to a lesser extent, and the bandwidth is increased. Similarly, if A decreases because the amplifier drives a heavy load, Y/X is not affected much. These concepts become clearer below.

Terminal Impedance Modification As a second example, let us study the circuit shown in Fig. 8.8(a), where a capacitive voltage divider senses the output voltage of a common-gate stage, applying the result to the gate of current source M_2 and hence returning a signal to the input.[3] Our objective is to compute the input resistance at relatively low frequencies with and without feedback. Neglecting channel-length modulation and the current drawn by C_1, we break the feedback loop as shown in Fig. 8.8(b) and write

$$R_{in,open} = \frac{1}{g_{m1} + g_{mb1}} \tag{8.9}$$

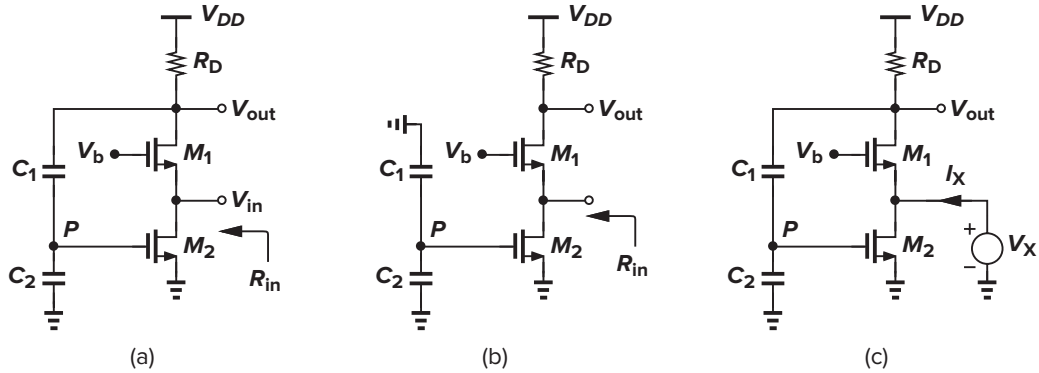


Figure 8.8 (a) Common-gate circuit with feedback; (b) open-loop circuit; (c) calculation of input resistance.

For the closed-loop circuit, as depicted in Fig. 8.8(c), we write $V_{out} = (g_{m1} + g_{mb1})V_X R_D$ and

$$V_P = V_{out}\frac{C_1}{C_1 + C_2} \tag{8.10}$$

$$= (g_{m1} + g_{mb1})V_X R_D \frac{C_1}{C_1 + C_2} \tag{8.11}$$

Thus, the small-signal drain current of M_2 equals $g_{m2}(g_{m1} + g_{mb1})V_X R_D C_1/(C_1 + C_2)$. Adding this current to the drain current of M_1 with proper polarity yields I_X:

$$I_X = (g_{m1} + g_{mb1})V_X + g_{m2}(g_{m1} + g_{mb1})\frac{C_1}{C_1 + C_2} R_D V_X \tag{8.12}$$

$$= (g_{m1} + g_{mb1})\left(1 + g_{m2}R_D\frac{C_1}{C_1 + C_2}\right)V_X \tag{8.13}$$

[3]The bias network for M_2 is not shown.

It follows that

$$R_{in,closed} = V_X/I_X \tag{8.14}$$

$$= \frac{1}{g_{m1}+g_{mb1}} \frac{1}{1+g_{m2}R_D\dfrac{C_1}{C_1+C_2}} \tag{8.15}$$

We therefore conclude that this type of feedback reduces the input resistance by a factor of $1 + g_{m2}R_DC_1/(C_1 + C_2)$. The reader can prove that the quantity $g_{m2}R_DC_1/(C_1 + C_2)$ is the loop gain.

Let us now consider the circuit of Fig. 8.9(a) as an example of output impedance modification by feedback. Here M_1, R_S, and R_D constitute a common-source stage and C_1, C_2, and M_2 sense the output voltage,[4] returning a current equal to $[C_1/(C_1 + C_2)]V_{out}g_{m2}$ to the source of M_1. The reader can prove that the feedback is indeed negative. To compute the output resistance at relatively low frequencies, we set the input to zero [Fig. 8.9(b)] and write

$$I_{D1} = V_X\frac{C_1}{C_1+C_2}g_{m2}\frac{R_S}{R_S+\dfrac{1}{g_{m1}+g_{mb1}}} \tag{8.16}$$

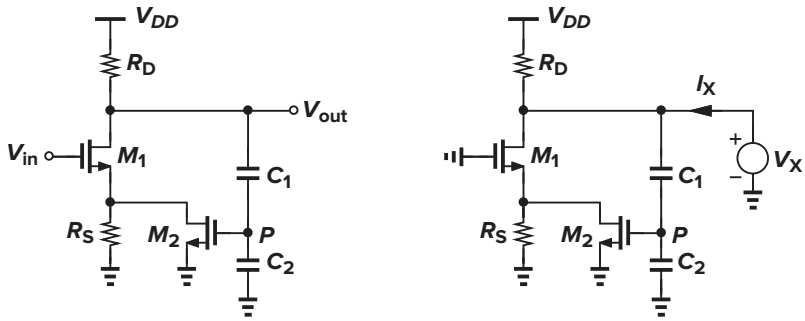


Figure 8.9 (a) CS stage with feedback; (b) calculation of output resistance.

Since $I_X = V_X/R_D + I_{D1}$, we have

$$\frac{V_X}{I_X} = \frac{R_D}{1+\dfrac{g_{m2}R_S(g_{m1}+g_{mb1})R_D}{(g_{m1}+g_{mb1})R_S+1}\dfrac{C_1}{C_1+C_2}} \tag{8.17}$$

Equation (8.17) implies that this type of feedback decreases the output resistance. The denominator of (8.17) is indeed equal to one plus the loop gain.

Bandwidth Modification. The next example illustrates the effect of negative feedback on the bandwidth. Suppose the feedforward amplifier has a one-pole transfer function:

$$A(s) = \frac{A_0}{1+\dfrac{s}{\omega_0}} \tag{8.18}$$

[4]Biasing of M_2 is not shown.

where A_0 denotes the low-frequency gain and ω_0 is the 3-dB bandwidth. What is the transfer function of the closed-loop system? From (8.5), we have

$$\frac{Y}{X}(s) = \frac{\dfrac{A_0}{1+\dfrac{s}{\omega_0}}}{1+\beta\dfrac{A_0}{1+\dfrac{s}{\omega_0}}} \tag{8.19}$$

$$= \frac{A_0}{1+\beta A_0+\dfrac{s}{\omega_0}} \tag{8.20}$$

$$= \frac{\dfrac{A_0}{1+\beta A_0}}{1+\dfrac{s}{(1+\beta A_0)\omega_0}} \tag{8.21}$$

The numerator of (8.21) is simply the closed-loop gain at low frequencies—as predicted by (8.5)—and the denominator reveals a pole at $(1+\beta A_0)\omega_0$. Thus, the 3-dB bandwidth has increased by a factor of $1+\beta A_0$, albeit at the cost of a proportional reduction in the gain (Fig. 8.10).

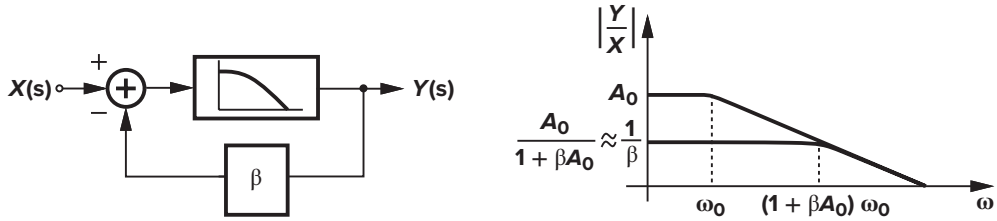


Figure 8.10 Bandwidth modification as a result of feedback.

The increase in the bandwidth fundamentally originates from the gain desensitization property of feedback. Recall from (8.6) that, if A is large enough, the closed-loop gain remains approximately equal to $1/\beta$ even if A experiences substantial variations. In the example of Fig. 8.10, A varies with frequency rather than process or temperature, but negative feedback still suppresses the effect of this variation. Of course, at high frequencies, A drops to such low levels that βA becomes comparable with unity and the closed-loop gain falls below $1/\beta$.

Equation (8.21) suggests that the "gain-bandwidth product" of a one-pole system is equal to $A_0\omega_0$ and does not change much with feedback, making the reader wonder how feedback improves the speed if a high gain is required. Suppose we need to amplify a 20-MHz square wave by a factor of 100 and maximum bandwidth, but we have only a single-pole amplifier with an open-loop gain of 100 and 3-dB bandwidth of 10 MHz. If the input is applied to the open-loop amplifier, the response appears as shown in Fig. 8.11(a), exhibiting a long risetime and falltime because the time constant is equal to $1/(2\pi f_{3\text{-dB}}) \approx 16$ ns.

Now suppose we apply feedback to the amplifier such that the gain and bandwidth are modified to 10 and 100 MHz, respectively. Placing two of these amplifiers in a cascade [Fig. 8.11(b)], we obtain a much faster response with an overall gain of 100. Of course, the cascade consumes twice as much power, but it would be quite difficult to achieve this performance with the original amplifier even if its power dissipation were doubled.

Nonlinearity Reduction An important property of negative feedback is the reduction of nonlinearity in analog circuits. A nonlinear characteristic is one that departs from a straight line, i.e., one whose *slope* varies (Fig. 8.12). A familiar example is the input-output characteristic of differential pairs. Note that

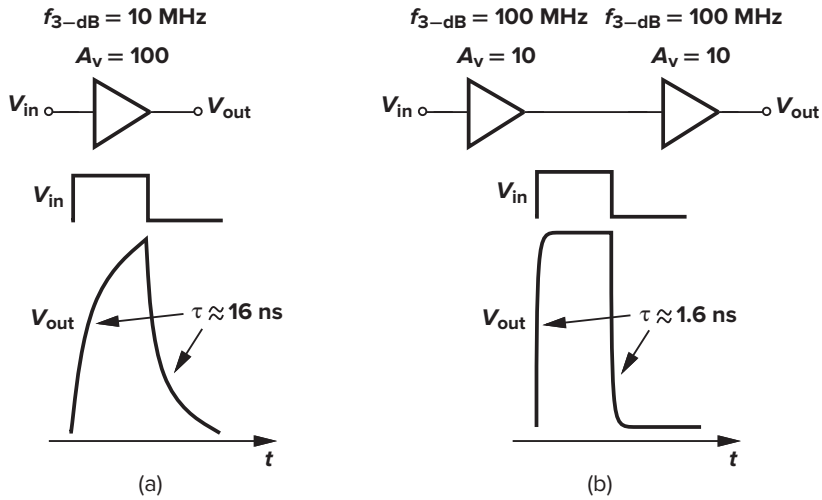


Figure 8.11 Amplification of a 20-MHz square wave by (a) a 10-MHz amplifier and (b) a cascade of two 100-MHz feedback amplifiers.

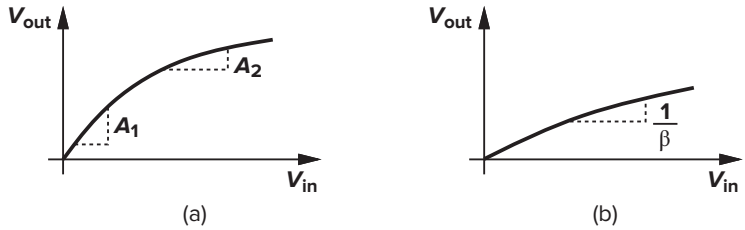


Figure 8.12 Input-output characteristic of a nonlinear amplifier (a) before and (b) after applying feedback.

the slope can be viewed as the small-signal gain. We predict that, even though the gain of an open-loop amplifier varies from A_1 to A_2 in Fig. 8.12, a closed-loop feedback system incorporating such an amplifier exhibits less gain variation and hence a higher linearity. To quantify this effect, we note that the open-loop gain ratio between regions 1 and 2 in Fig. 8.12 is equal to

$$r_{open} = \frac{A_2}{A_1} \tag{8.22}$$

For example, $r_{open} = 0.9$ means that the gain falls by 10% from region 1 to region 2. Assuming $A_2 = A_1 - \Delta A$, we can write

$$r_{open} = 1 - \frac{\Delta A}{A_1} \tag{8.23}$$

Let us place this amplifier in a negative-feedback loop. For the closed-loop gain ratio, we have

$$r_{closed} = \frac{\dfrac{A_2}{1+\beta A_2}}{\dfrac{A_1}{1+\beta A_1}} \tag{8.24}$$

$$= \frac{1+\dfrac{1}{\beta A_1}}{1+\dfrac{1}{\beta A_2}} \tag{8.25}$$

It follows that

$$r_{closed} \approx 1 - \frac{\dfrac{1}{\beta A_2} - \dfrac{1}{\beta A_1}}{1 + \dfrac{1}{\beta A_2}} \tag{8.26}$$

$$\approx 1 - \frac{A_1 - A_2}{1 + \beta A_2} \frac{1}{A_1} \tag{8.27}$$

$$\approx 1 - \frac{\Delta A}{1 + \beta A_2} \frac{1}{A_1} \tag{8.28}$$

Comparison of (8.23) and (8.28) suggests that the gain ratio is much closer to 1 in the latter if the loop gain, $1 + \beta A_2$, is large.

We study nonlinearity and its behavior in feedback systems more extensively in Chapter 14.

8.1.2 Types of Amplifiers

Most of the circuits studied thus far can be considered "voltage amplifiers" because they sense a voltage at the input and produce a voltage at the output. However, three other types of amplifiers can also be constructed such that they sense or produce currents. Shown in Fig. 8.13, the four configurations have quite different properties: (1) circuits sensing a voltage must exhibit a high input impedance (a voltmeter measures a voltage with minimal loading) whereas those sensing a current must provide a low input impedance (a current meter inserted in a wire must negligibly disturb the current); (2) circuits generating a voltage must exhibit a low output impedance (as a voltage source) while those generating a current must provide a high output impedance (as a current source). Note that the gains of transimpedance and transconductance[5] amplifiers have a dimension of resistance and conductance, respectively. For example, a transimpedance amplifier may have a gain of 2 kΩ, which means that it produces a 2-V output in response to a 1-mA input. Also, we use the sign conventions depicted in Fig. 8.13; for example, the transimpedance $R_0 = V_{out}/I_{in}$ if I_{in} flows *into* the amplifier.

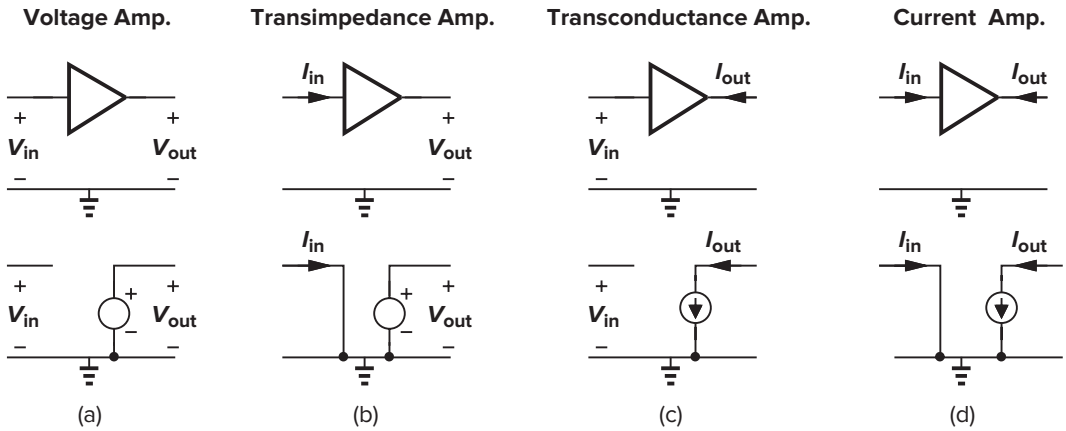


Figure 8.13 Types of amplifiers along with their idealized models.

[5]This terminology is standard but not consistent. One should use either transimpedance and transadmittance or transresistance and transconductance.

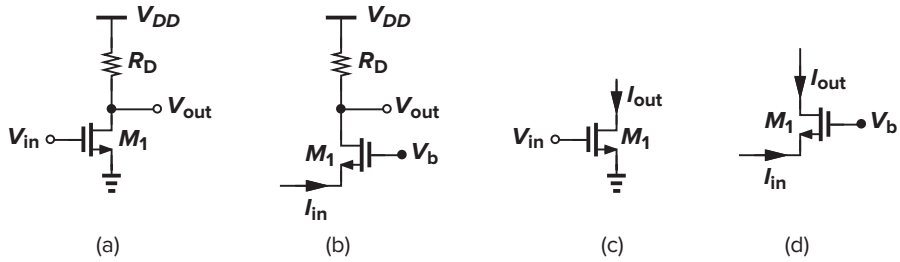


Figure 8.14 Simple implementations of four types of amplifiers.

Figure 8.14 illustrates simple implementations of each amplifier. In Fig. 8.14(a), a common-source stage senses and produces Voltages, and in Fig. 8.14(b), a common-gate circuit serves as a transimpedance amplifier, converting the source current to a voltage at the drain. In Fig. 8.14(c), a common-source transistor operates as a transconductance amplifier (also called a V/I converter), generating an output current in response to an input voltage, and in Fig. 8.14(d), a common-gate device senses and produces currents.

The circuits of Fig. 8.14 may not provide adequate performance in many applications. For example, the circuits of Figs. 8.14(a) and (b) suffer from a relatively high output impedance. Figure 8.15 depicts modifications that alter the output impedance or increase the gain.

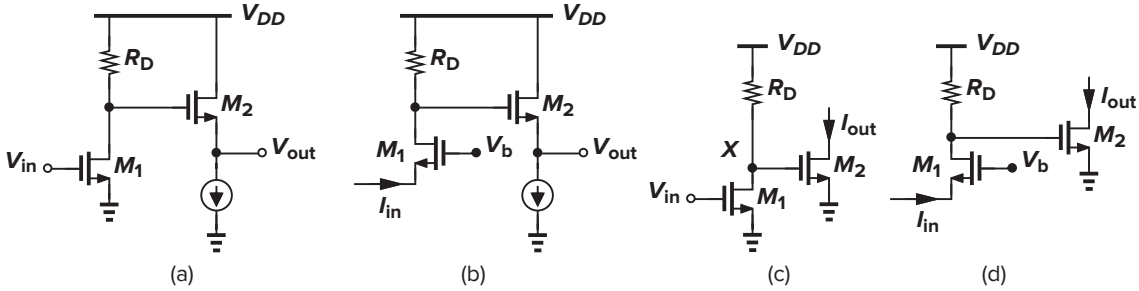


Figure 8.15 Four types of amplifiers with improved performance.

▶ Example 8.2

Calculate the gain of the transconductance amplifier shown in Fig. 8.15(c).

Solution

The gain in this case is defined as $G_m = I_{out}/V_{in}$. That is

$$G_m = \frac{V_X}{V_{in}} \cdot \frac{I_{out}}{V_X} \tag{8.29}$$

$$= -g_{m1}(r_{O1} \| R_D) \cdot g_{m2} \tag{8.30}$$

◀

While most familiar amplifiers are of the voltage-voltage type, the other three configurations do find usage. For example, transimpedance amplifiers are an integral part of optical fiber receivers because they must sense the current produced by a photodiode, eventually generating a voltage that can be processed by subsequent circuits.

current by placing a small resistor in series with the wire and sensing the voltage across it [Figs. 8.19(b) and (c)]. To subtract two voltages, a differential pair can be used [Fig. 8.19(d)]. Alternatively, a single transistor can perform voltage subtraction as shown in Figs. 8.19(e) and (f) because I_{D1} is a function of $V_{in} - V_F$. Subtraction of currents can be accomplished as depicted in Fig. 8.19(g) or (h). Note that for voltage subtraction, the input and feedback signals are applied to *two* distinct nodes, whereas for current subtraction, they are applied to a single node. This observation proves helpful in identifying the type of feedback.

While ideally having no influence on the operation of the open-loop amplifier itself, the feedback network in reality introduces loading effects that must be taken into account. This issue is discussed in Sec. 8.5.

8.2 ■ Feedback Topologies

In this section, we study four "canonical" topologies resulting from placing each of the four amplifier types in a negative-feedback loop. As depicted in Fig. 8.20, X and Y can be a current or a voltage quantity. The main amplifier is called the "feedforward" or simply the "forward" amplifier, around which we apply feedback to improve the performance.

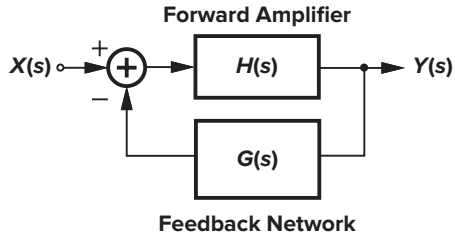


Figure 8.20 Canonical feedback system.

We should remark that some feedback circuits do not conform to the four canonical topologies. We return to this point later in the chapter, but the intuition gained from the analysis of these topologies proves essential to analog design. For example, we greatly benefit from the knowledge that one type of feedback lowers the output impedance while another raises it.

8.2.1 Voltage-Voltage Feedback

This topology senses the output voltage and returns the feedback signal as a voltage.[7] Following the conceptual illustrations of Figs. 8.17 and 8.18, we note that the feedback network is connected in *parallel* with the output and in *series* with the input port (Fig. 8.21). An ideal feedback network in this case exhibits infinite input impedance and zero output impedance because it senses a voltage and generates a voltage. We can therefore write $V_F = \beta V_{out}$, $V_e = V_{in} - V_F$, $V_{out} = A_0(V_{in} - \beta V_{out})$, and hence

$$\frac{V_{out}}{V_{in}} = \frac{A_0}{1 + \beta A_0} \tag{8.31}$$

We recognize that βA_0 is the loop gain and that the overall gain has dropped by $1 + \beta A_0$. Note that here both A_0 and β are dimensionless quantities.

As a simple example of voltage-voltage feedback, suppose we employ a differential voltage amplifier with single-ended output as the feedforward amplifier and a resistive divider as the feedback network

[7] This configuration is also called "series-shunt" feedback, where the first term refers to the *input* connection and the second to the *output* connection.

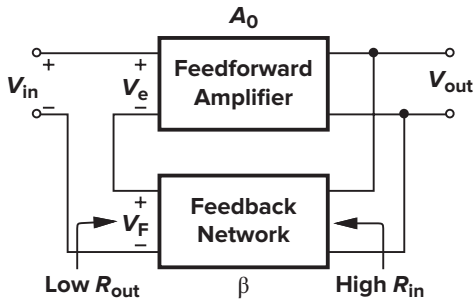


Figure 8.21 Voltage-voltage feedback.

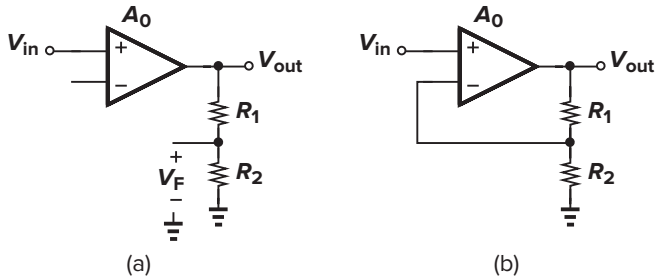


Figure 8.22 (a) Amplifier with output sensed by a resistive divider; (b) voltage-voltage feedback amplifier.

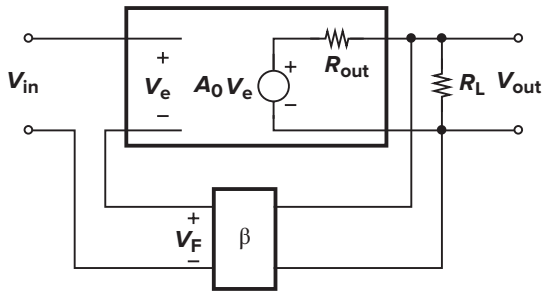


Figure 8.23 Effect of voltage-voltage feedback on output resistance.

[Fig. 8.22(a)]. The divider senses the output voltage, producing a fraction thereof as the feedback signal V_F. Following the block diagram of Fig. 8.21, we place V_F in series with the input of the amplifier to perform subtraction of voltages [Fig. 8.22(b)].

How does voltage-voltage feedback modify the input and output impedances? Let us first consider the output impedance. Recall that a negative-feedback system attempts to make the output an accurate (scaled) replica of the input. Now suppose, as shown in Fig. 8.23, we load the output by a resistor R_L, gradually decreasing its value. While in the open-loop configuration, the output would simply drop in proportion to $R_L/(R_L + R_{out})$, in the feedback system, V_{out} is maintained as a reasonable replica of V_{in} even though R_L decreases. That is, so long as the loop gain remains much greater than unity, $V_{out}/V_{in} \approx 1/\beta$, regardless of the value of R_L. From another point of view, since the circuit stabilizes ("regulates") the output voltage amplitude despite load variations, it behaves as a *voltage* source, thus exhibiting a low output impedance. This property fundamentally originates from the gain desensitization provided by feedback.

In order to formally prove that voltage feedback lowers the output impedance, we consider the simple model in Fig. 8.24, where R_{out} represents the output impedance of the feedforward amplifier. Setting the input to zero and applying a voltage at the output, we write $V_F = \beta V_X$, $V_e = -\beta V_X$, $V_M = -\beta A_0 V_X$,

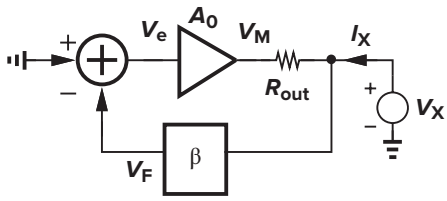


Figure 8.24 Calculation of output resistance of a voltage-voltage feedback circuit.

and hence $I_X = [V_X - (-\beta A_0 V_X)]/R_{out}$ (if the current drawn by the feedback network is neglected). It follows that

$$\frac{V_X}{I_X} = \frac{R_{out}}{1 + \beta A_0} \tag{8.32}$$

Thus, the output impedance and the gain are lowered by the same factor. In the circuit of Fig. 8.22(b), for example, the output impedance is lowered by $1 + A_0 R_2/(R_1 + R_2)$.

▶ Example 8.4

The circuit shown in Fig. 8.25(a) is an implementation of the feedback configuration depicted in Fig. 8.22(b), but with the resistors replaced by capacitors. (The bias network of M_2 is not shown.) Calculate the closed-loop gain and output resistance of the amplifier at relatively low frequencies.

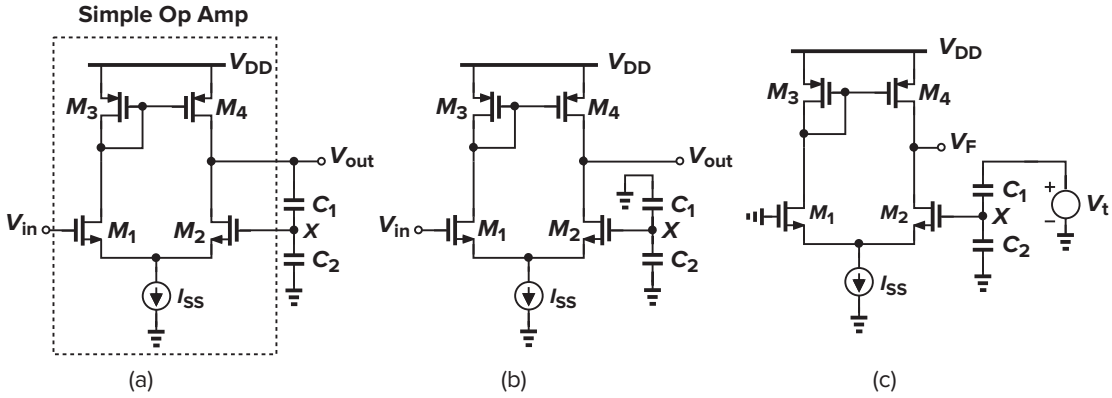


Figure 8.25

Solution

At low frequencies, C_1 and C_2 draw a negligible current from the output node. To find the open-loop voltage gain, we break the feedback loop as shown in Fig. 8.25(b), grounding the top plate of C_1 to ensure zero voltage feedback. The open-loop gain is thus equal to $g_{m1}(r_{O2} \| r_{O4})$.

We must also compute the loop gain, βA_0. With the aid of Fig. 8.25(c), we have

$$V_F = -V_t \frac{C_1}{C_1 + C_2} g_{m1}(r_{O2} \| r_{O4}) \tag{8.33}$$

That is

$$\beta A_0 = \frac{C_1}{C_1 + C_2} g_{m1}(r_{O2} \| r_{O4}) \tag{8.34}$$

and hence

$$A_{closed} = \frac{g_{m1}(r_{O2} \| r_{O4})}{1 + \dfrac{C_1}{C_1 + C_2} g_{m1}(r_{O2} \| r_{O4})} \tag{8.35}$$

As expected, if $\beta A_0 \gg 1$, then $A_{closed} \approx 1 + C_2/C_1$.

The open-loop output resistance of the circuit is equal to $r_{O2} \| r_{O4}$ (Chapter 5). It follows that

$$R_{out,closed} = \frac{r_{O2} \| r_{O4}}{1 + \dfrac{C_1}{C_1 + C_2} g_{m1}(r_{O2} \| r_{O4})} \tag{8.36}$$

It is interesting to note that if $\beta A_0 \gg 1$, then

$$R_{out,closed} \approx \left(1 + \frac{C_2}{C_1}\right) \frac{1}{g_{m1}} \tag{8.37}$$

In other words, even if the open-loop amplifier suffers from a *high* output resistance, the closed-loop output resistance is independent of $r_{O2} \| r_{O4}$, simply because the open-loop *gain* scales with $r_{O2} \| r_{O4}$ as well.

◀

▶ Example 8.5

Figure 8.26(a) shows an inverting amplifier using an op amp, and Fig. 8.26(b) illustrates a circuit implementation incorporating capacitors rather than resistors for the feedback network. Determine the loop gain and output impedance of the latter at low frequencies.

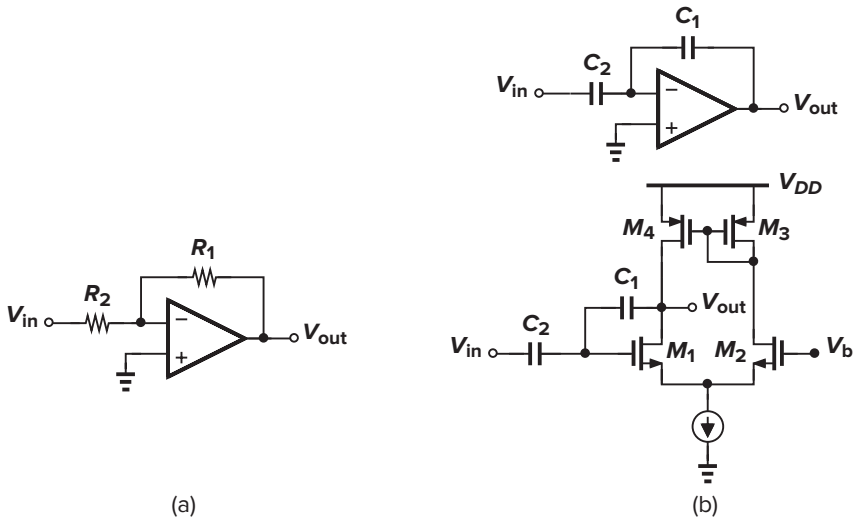


Figure 8.26

Solution

With V_{in} set to zero, this circuit becomes indistinguishable from that in Fig. 8.25(a). Thus, the loop gain is given by (8.34) and the output impedance by (8.36).

The circuits in Figs. 8.25(a) and 8.26(b) appear similar, but provide different closed-loop gains, approximately $1 + C_2/C_1$ and $-C_2/C_1$, respectively. Thus, for a gain of, say, 4, $C_2/C_1 \approx 3$ in the former and $C_2/C_1 \approx 4$ in the latter. Which topology exhibits a higher loop gain in this case?

◀

Voltage-voltage feedback also modifies the input impedance. Comparing the configurations in Fig. 8.27, we note that the input impedance of the feedforward amplifier sustains the entire input voltage in Fig. 8.27(a), but only a fraction of V_{in} in Fig. 8.27(b). As a result, the current drawn by R_{in} in the feedback topology is *less* than that in the open-loop system, suggesting that returning a voltage quantity to the input *increases* the input impedance.

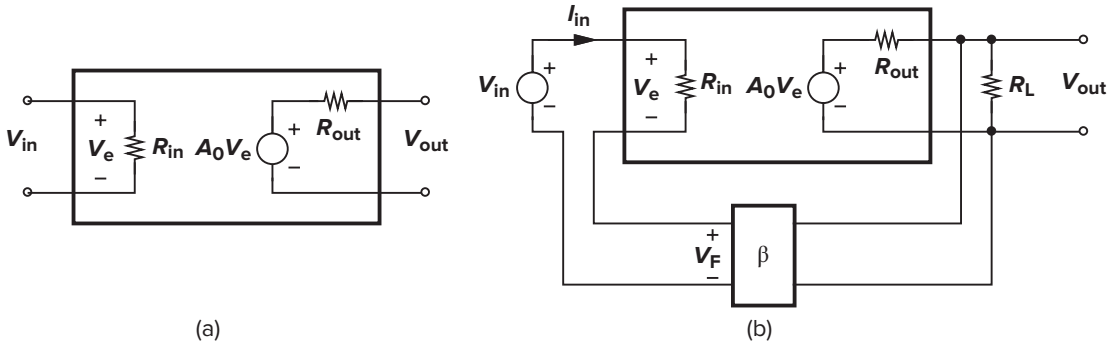


Figure 8.27 Effect of voltage-voltage feedback on input resistance.

The foregoing observation can be confirmed analytically with the aid of Fig. 8.28. Since $V_e = I_X R_{in}$ and $V_F = \beta A_0 I_X R_{in}$, we have $V_e = V_X - V_F = V_X - \beta A_0 I_X R_{in}$. Thus, $I_X R_{in} = V_X - \beta A_0 I_X R_{in}$, and

$$\frac{V_X}{I_X} = R_{in}(1 + \beta A_0) \tag{8.38}$$

The input impedance therefore increases by the ubiquitous factor $1 + \beta A_0$, bringing the circuit closer to an ideal voltage amplifier.

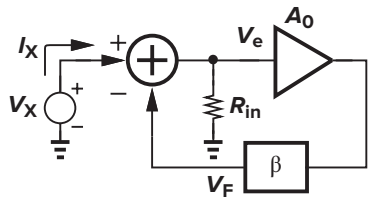


Figure 8.28 Calculation of input impedance of a voltage-voltage feedback circuit.

▶ Example 8.6

Figure 8.29(a) shows a common-gate topology placed in a voltage-voltage feedback configuration. Note that the summation of the feedback voltage and the input voltage is accomplished by applying the former to the gate and the latter to the source.[8] Calculate the input resistance at low frequencies if channel-length modulation is negligible.

Solution

Breaking the loop as depicted in Fig. 8.29(b), we recognize that the open-loop input resistance is equal to $(g_{m1} + g_{mb1})^{-1}$. To find the loop gain, we set the input to zero and inject a test signal in to the loop [Fig. 8.29(c)], obtaining $V_F/V_t = -g_{m1}R_D C_1/(C_1 + C_2)$. The closed-loop input impedance is then equal to

$$R_{in,closed} = \frac{1}{g_{m1} + g_{mb1}} \left(1 + \frac{C_1}{C_1 + C_2} g_{m1} R_D\right) \tag{8.39}$$

[8]This circuit is similar to the right half of the topology shown in Fig. 8.25(a).

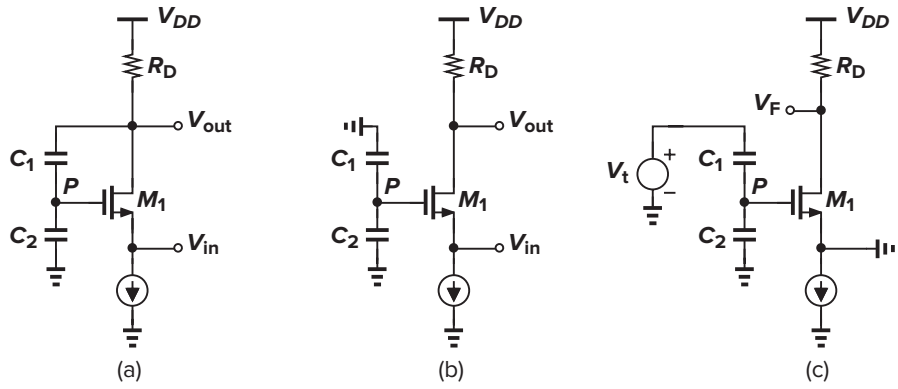


Figure 8.29

The increase in the input impedance can be explained as follows. Suppose the input voltage decreases by ΔV, causing the output voltage to fall. As a result, the gate voltage of M_1 *decreases*, thereby lowering the gate-source voltage of M_1 and yielding a change in V_{GS1} that is *less* than ΔV. This means that the drain current changes by an amount less than $(g_m + g_{mb})\Delta V$. By contrast, if the gate of M_1 were connected to a constant potential, the gate-source voltage would change by ΔV, resulting in a larger current change.

In summary, voltage-voltage feedback decreases the output impedance and increases the input impedance, thereby proving useful as a "buffer" stage that can be interposed between a high-impedance source and a low-impedance load.

8.2.2 Current-Voltage Feedback

In some circuits, it is desirable or simpler to sense the output current to perform feedback. The current is actually sensed by placing a (preferably small) resistor in series with the output and using the voltage drop across the resistor as the feedback information. This voltage may even serve as the return signal that is directly subtracted from the input.

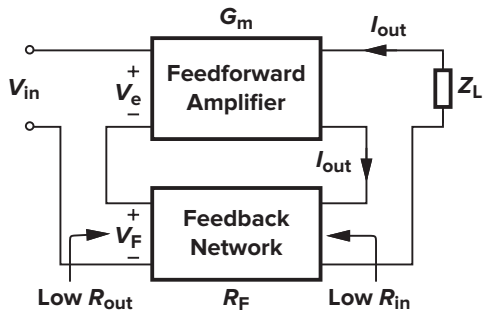


Figure 8.30 Current-voltage feedback.

Let us consider the general current-voltage feedback system illustrated in Fig. 8.30.[9] Since the feedback network senses the output current and returns a voltage, its feedback factor, β, has the dimension of resistance and is denoted by R_F. It is important to note that a G_m stage must be loaded ("terminated") by a finite impedance, Z_L, to ensure that it can deliver its output current. If $Z_L = \infty$, then an ideal G_m

[9]This topology is also called "series-series" feedback.

This method proves more efficient than direct analysis of the circuit (with no knowledge of feedback) if the loop is assumed unilateral, i.e., the forward propagation of the input signal through the feedback network is neglected, and so is the backward propagation of the signal through the forward amplifier. The other two methods do not attempt to break the loop and yield the closed-loop quantities exactly but with lengthier algebra.

8.5 ■ Effect of Loading

The problem of loading manifests itself when we need to break the feedback loop so as to identify the open-loop system, e.g., calculate the open-loop gain and the input and output impedances. To arrive at the proper procedure for including the feedback network terminal impedances, we first review models of two-port networks.

8.5.1 Two-Port Network Models

The simplified amplifier and feedback network models employed in the previous sections may not suffice in general. We must therefore resort to accurate two-port models. For example, the feedback network placed around the feedforward amplifier can be considered a two-port circuit sensing and producing voltages or currents. Recall from basic circuit theory that a two-port linear (and time-invariant) network can be represented by any of the four models shown in Fig. 8.50. The "Z model" in Fig. 8.50(a) consists of input and output impedances in series with current-dependent voltage sources, whereas the "Y model" in Fig. 8.50(b) comprises input and output admittances in parallel with voltage-dependent current sources. The "hybrid models" of Figs. 8.50(c) and (d) incorporate a combination of impedances and admittances and voltage sources and current sources. Each model is described by two equations. For the Z model, we have

$$V_1 = Z_{11} I_1 + Z_{12} I_2 \tag{8.57}$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2 \tag{8.58}$$

Each Z parameter has a dimension of impedance and is obtained by leaving one port open, e.g., $Z_{11} = V_1/I_1$ when $I_2 = 0$. Similarly, for the Y model,

$$I_1 = Y_{11} V_1 + Y_{12} V_2 \tag{8.59}$$

$$I_2 = Y_{21} V_1 + Y_{22} V_2 \tag{8.60}$$

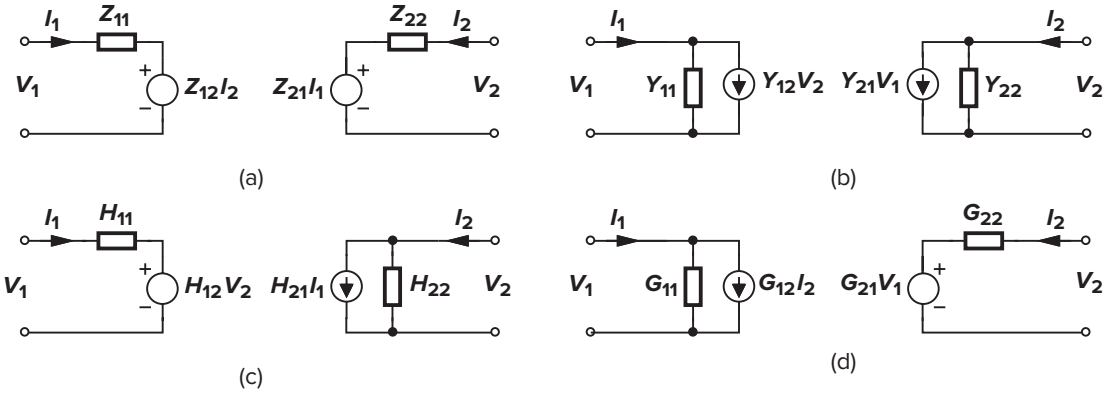


Figure 8.50 Linear two-port network models.

where each Y parameter is calculated by shorting one port, e.g., $Y_{11} = I_1/V_1$ when $V_2 = 0$. For the H model,

$$V_1 = H_{11}I_1 + H_{12}V_2 \tag{8.61}$$

$$I_2 = H_{21}I_1 + H_{22}V_2 \tag{8.62}$$

and for the G model,

$$I_1 = G_{11}V_1 + G_{12}I_2 \tag{8.63}$$

$$V_2 = G_{21}V_1 + G_{22}I_2 \tag{8.64}$$

Note that, for example, Y_{11} may not be equal to the inverse of Z_{11} because the two are obtained under different conditions: the output is shorted for the former but left open for the latter.

It is instructive to compare the general two-port models with the simplified amplifier representations that we have used in the previous sections. For example, let us consider the voltage amplifier model in Example 8.3 vis-à-vis the Z model. We observe that (1) absent in the former, $Z_{12}I_2$ represents the amplifier's *internal* feedback, e.g., due to C_{GD}; (2) if Z_{12} is zero, then Z_{11} is equal to Z_{in}, the input impedance calculated with the output left open; and (3) Z_{22} is not necessarily equal to Z_{out}: the former is computed with the input port left open and the latter with the input *shorted*.

The most important drawback of the Z model for our purposes is that its output generator, $Z_{21}I_1$, is controlled by the input *current* rather than the input voltage. For a MOS circuit with the input applied to the gate, this model becomes meaningless if the input capacitance is neglected. The H model entails the same difficulty.

Do any of the two-port models agree with our intuitive picture of voltage amplifiers? Yes, the G model is close. If the internal feedback, $G_{12}I_2$, is neglected, then G_{11} ($= I_1/V_1$ with $I_2 = 0$) represents the inverse of the input impedance, and G_{22} ($= V_2/I_2$ with $V_1 = 0$) the output impedance. The reader can try this exercise for the other three types of amplifiers.

8.5.2 Loading in Voltage-Voltage Feedback

As mentioned before, the Z and H models fail to represent voltage amplifiers if the input current is very small—as in a simple CS stage. We therefore choose the G model here.[13] The complete equivalent circuit is shown in Fig. 8.51(a), where the forward and feedback network parameters are denoted by upper-case and lower-case letters, respectively. Since the *input* port of the feedback network is connected to the *output* port of the forward amplifier, g_{11} and $g_{12}I_{in}$ are tied to V_{out}.

It is possible to solve this circuit exactly, but we simplify the analysis by neglecting two quantities: the amplifier's internal feedback, $G_{12}V_{out}$, and the "forward" propagation of the input signal through the feedback network, $g_{12}I_{in}$. In other words, the loop is "unilateralized." Figure 8.51(b) depicts the resulting circuit with our intuitive amplifier notations (Z_{in}, Z_{out}, A_0) added to indicate equivalencies. Let us first directly compute the closed-loop voltage gain. Recognizing that g_{11} is an admittance and g_{22} an impedance, we write a KVL around the input network and a KCL at the output node:

$$V_{in} = V_e + g_{22}\frac{V_e}{Z_{in}} + g_{21}V_{out} \tag{8.65}$$

$$g_{11}V_{out} + \frac{V_{out} - A_0V_e}{Z_{out}} = 0 \tag{8.66}$$

[13] Though allowing simpler algebra, the Y model does not provide intuitive results.

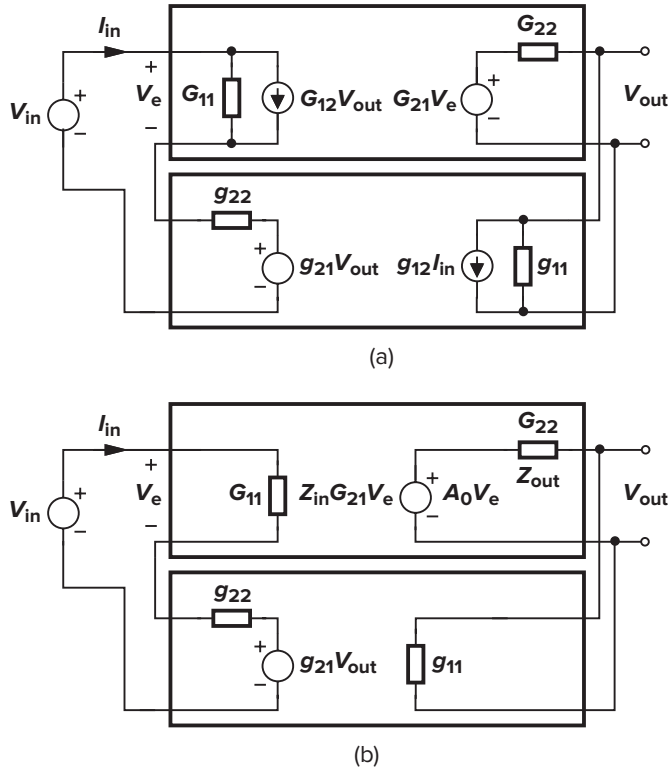


Figure 8.51 Voltage-voltage feedback circuit with (a) feedback network represented by a G model and (b) a simplified G model.

Finding V_e from the latter equation and substituting the result in the former, we have

$$\frac{V_{out}}{V_{in}} = \frac{A_0}{(1 + \frac{g_{22}}{Z_{in}})(1 + g_{11}Z_{out}) + g_{21}A_0} \tag{8.67}$$

It is desirable to express the closed-loop gain in the familiar form, $A_{v,open}/(1 + \beta A_{v,open})$. To this end, we divide the numerator and the denominator by $(1 + g_{22}/Z_{in})(1 + g_{11}Z_{out})$:

$$\frac{V_{out}}{V_{in}} = \frac{\dfrac{A_0}{(1 + \frac{g_{22}}{Z_{in}})(1 + g_{11}Z_{out})}}{1 + g_{21}\dfrac{A_0}{(1 + \frac{g_{22}}{Z_{in}})(1 + g_{11}Z_{out})}} \tag{8.68}$$

We can thus write

$$A_{v,open} = \frac{A_0}{(1 + \frac{g_{22}}{Z_{in}})(1 + g_{11}Z_{out})} \tag{8.69}$$

$$\beta = g_{21} \tag{8.70}$$

Let us now interpret these results. The equivalent open-loop gain contains a factor A_0, i.e., the original amplifier's voltage gain (before immersion in feedback). But this gain is attenuated by two factors, namely, $1 + g_{22}/Z_{in}$ and $1 + g_{11}Z_{out}$. Interestingly, we can write $1 + g_{22}/Z_{in} = (Z_{in} + g_{22})/Z_{in}$, concluding that A_0 is multiplied by $Z_{in}/(Z_{in} + g_{22})$, which reminds us of a voltage divider. Similarly, $1 + g_{11}Z_{out} = (g_{11}^{-1} + Z_{out})/g_{11}^{-1}$, whose inverse points to another voltage divider. The loaded forward amplifier now emerges as shown in Fig. 8.52. Note that this model excludes the two generators $G_{12}V_{out}$ and $g_{12}I_{in}$, which are generally not negligible.

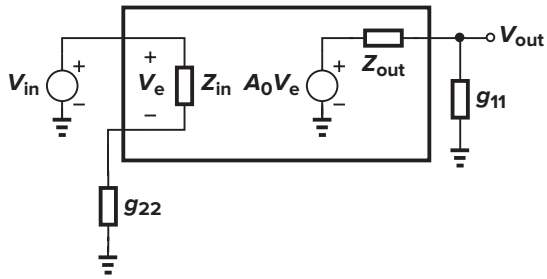


Figure 8.52 Proper method of including loading in a voltage-voltage feedback circuit.

The reader may wonder why we go to the trouble of finding the open-loop parameters while the closed-loop circuit in Fig. 8.51(a) can be solved exactly. The key principle here is that the rules depicted in Fig. 8.52 afford us a quick and intuitive understanding of the circuit that would not be possible from the direct analysis of Fig. 8.51(a). Specifically, we recognize that the finite input and output impedances of the feedback network reduce the output voltage and the voltage seen by the input of the main amplifier, respectively.

It is important to note that g_{11} and g_{22} in Fig. 8.50 are computed as follows:

$$g_{11} = \left.\frac{I_1}{V_1}\right|_{I2=0} \tag{8.71}$$

$$g_{22} = \left.\frac{V_2}{I_2}\right|_{V1=0} \tag{8.72}$$

Thus, as illustrated in Fig. 8.53, g_{11} is obtained by leaving the output of the feedback network open whereas g_{22} is calculated by *shorting* the input of the feedback network.

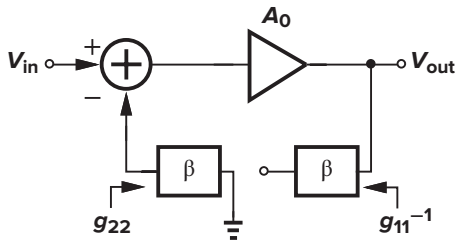


Figure 8.53 Conceptual view of opening a voltage-voltage feedback loop with proper loading.

Another important result of the foregoing analysis is that the loop gain, i.e., the second term in the denominator of (8.68), is simply equal to the loaded open-loop gain multiplied by g_{21}. Thus, a separate calculation of the loop gain is not necessary. Also, the open-loop input and output impedances obtained from Fig. 8.52 are scaled by $1 + g_{21}A_{v,open}$ to yield the closed-loop values. Again, we must bear in mind that this loop gain neglects the effect of $G_{12}V_{out}$ and $g_{12}I_{in}$.

▶ Example 8.12

For the circuit shown in Fig. 8.54(a), calculate the open-loop and closed-loop gains assuming $\lambda = \gamma = 0$.

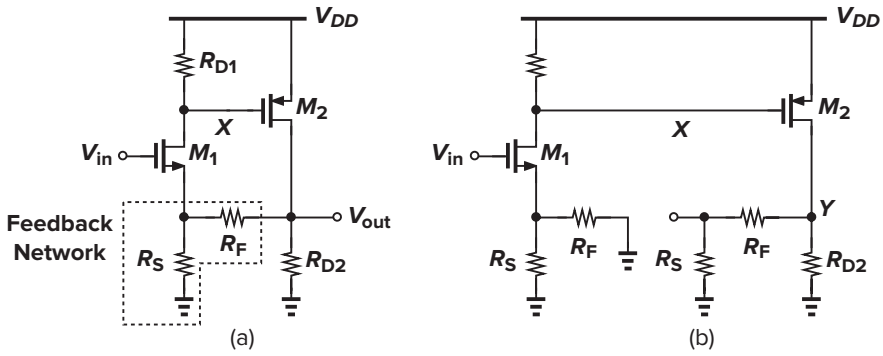


Figure 8.54

Solution

The circuit consists of two common-source stages, with R_F and R_S sensing the output voltage and returning a fraction thereof to the source of M_1. This transistor subtracts the returned voltage from V_{in}. The reader can prove that the feedback is indeed negative. Following the procedure illustrated in Fig. 8.53, we identify R_F and R_S as the feedback network and construct the open-loop circuit as shown in Fig. 8.54(b). Note that the loading effect in the input network is obtained by shorting the right terminal of R_F to ground and that in the output by leaving the left terminal of R_F open. Neglecting channel-length modulation and body effect for simplicity, we observe that M_1 is degenerated by the feedback network and

$$A_{v,open} = \frac{V_Y}{V_{in}} = \frac{-R_{D1}}{R_F \| R_S + 1/g_{m1}} \{-g_{m2}[R_{D2} \| (R_F + R_S)]\} \tag{8.73}$$

To compute the closed-loop gain, we first find the loop gain as $g_{21}A_{v,open}$. Recall from (8.64) that $g_{21} = V_2/V_1$ with $I_2 = 0$. For the voltage divider consisting of R_F and R_S, $g_{21} = R_S/(R_F + R_S)$. The closed-loop gain is simply equal to $A_{v,closed} = A_{v,open}/(1 + g_{21}A_{v,open})$.

Can we include R_{D2} in the feedback network rather than in the forward amplifier? Yes, we can ascribe a finite r_O to M_2 and proceed while considering R_{D2}, R_F, and R_S as the feedback network. The result is slightly different from that obtained above.

The above analysis neglects the forward amplifier's internal feedback (e.g., due to C_{GD2}) and the propagation of the input signal from the source of M_1 and through R_F to the output. (Transistor M_1 also operates as a source follower in this case.)

◀

▶ Example 8.13

A student eager to understand the approximations leading to the circuit in Fig. 8.51(b) decides to use an H model for the forward amplifier and obtain an exact solution. Perform this analysis and explain the results.

Solution

Illustrated in Fig. 8.55, this representation is attractive as it allows a simple series connection of voltages and impedances at the input and a parallel connection at the output. Writing a KVL and a KCL gives

$$V_{in} = I_{in}H_{11} + H_{12}V_{out} + I_{in}g_{22} + g_{21}V_{out} \tag{8.74}$$

$$H_{22}V_{out} + H_{21}I_{in} + g_{11}V_{out} + g_{12}I_{in} = 0 \tag{8.75}$$

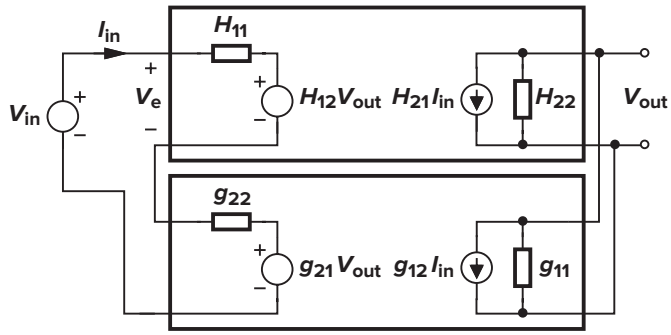


Figure 8.55

Finding I_{in} from the latter and replacing it in the former, we have

$$\frac{V_{out}}{V_{in}} = \frac{-\dfrac{H_{21}+g_{12}}{(H_{22}+g_{11})(H_{11}+g_{22})}}{1-(H_{12}+g_{21})\dfrac{H_{21}+g_{12}}{(H_{22}+g_{11})(H_{11}+g_{22})}} \tag{8.76}$$

We can thus define

$$A_{v,open} = -\frac{H_{21}+g_{12}}{(H_{22}+g_{11})(H_{11}+g_{22})} \tag{8.77}$$

$$\beta = H_{12}+g_{21} \tag{8.78}$$

If we assume that $g_{12} \ll H_{21}$ and $H_{12} \ll g_{21}$, then

$$A_{v,open} = \frac{-H_{21}}{(H_{22}+g_{11})(H_{11}+g_{22})} \tag{8.79}$$

$$\beta = g_{21} \tag{8.80}$$

and the attenuation factors $H_{22}+g_{11}$ and $H_{11}+g_{22}$ can be interpreted in the same manner as those in Eq. (8.69). This approach therefore explicitly reveals the simplifying approximations, namely, $g_{12} \ll H_{21}$ and $H_{12} \ll g_{21}$. Unfortunately, however, for a MOS gate input, H_{21} (the "current gain") approaches infinity, making the model difficult to use.

◀

8.5.3 Loading in Current-Voltage Feedback

In this case, the feedback network appears in series with the output so as to sense the current. We represent the forward amplifier and the feedback network by Y and Z models, respectively (Fig. 8.56), neglecting the generators $Y_{12}V_{out}$ and $z_{12}I_{in}$. We wish to compute the closed-loop gain, I_{out}/V_{in}, and therefrom determine how the open-loop parameters can be obtained in the presence of loading. Noting that $I_{in} = Y_{11}V_e$ and $I_2 = I_{in}$, we write two KVLs:

$$V_{in} = V_e + Y_{11}V_e z_{22} + z_{21}I_{out} \tag{8.81}$$

$$-I_{out}z_{11} = \frac{I_{out} - Y_{21}V_e}{Y_{22}} \tag{8.82}$$