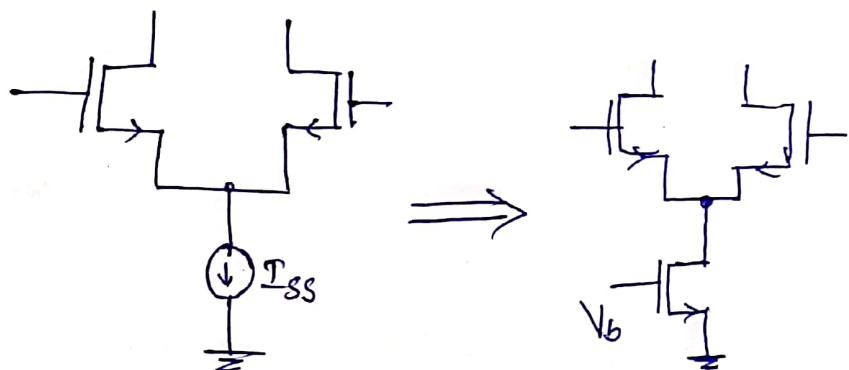
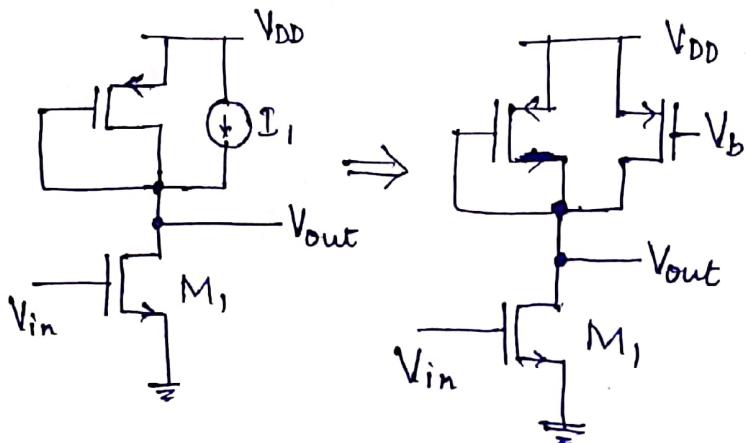


## Unit 4

### Passive and Active Current Mirror

In analog circuits current sources act as a large resistor without consuming excessive voltage headroom.

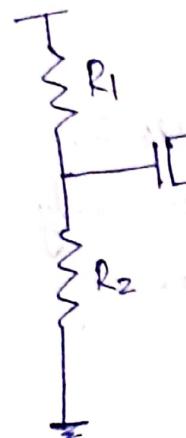
#### Basic Current Sources Application.



- The output resistance and capacitance and the voltage headroom of a current source trade with the magnitude of the output current.
- In addition to these issues, several other aspects of current sources are important: it depends on supply, process and temperature.

How should a MOSFET be biased so as to operate as a stable current source?

Consider the simple resistive biasing as shown in fig.



$$\rightarrow \text{Assuming } M_1 \text{ is in saturation, we have}$$

$$I_{out} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left( \frac{V_{DD} - V_{th}}{R_1 + R_2} \right)$$

$\rightarrow$  This expression reveals various dependencies of  $I_{out}$  upon the supply, process and temperature.

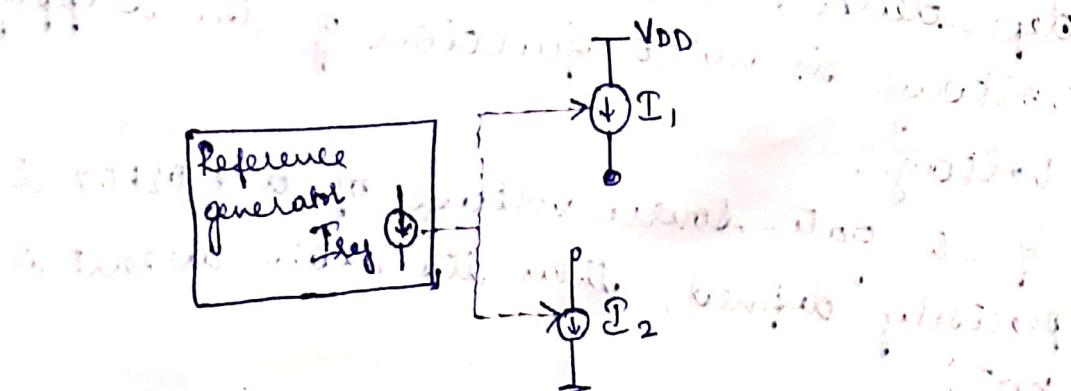
- $\rightarrow$  The overdrive voltage ( $V_{GS} - V_{th}$ ) is a function of  $V_{DD}$  and  $V_{th}$ .
- $\rightarrow$  The threshold voltage may vary by 100mV from wafer to wafer.
- $\rightarrow$  Furthermore, both  $\mu_n$  and  $V_{th}$  exhibit temperature dependence. Thus,  $I_{out}$  is poorly defined.
- $\rightarrow$  It is important to note that the above expression process and temperature dependencies exist even if the gate voltage is not a function of the supply voltage.
- $\rightarrow$  If the gate-source voltage of a MOSFET is precisely defined, then its drain current is not!

For these reasons, we must seek other methods of biasing the current sources.

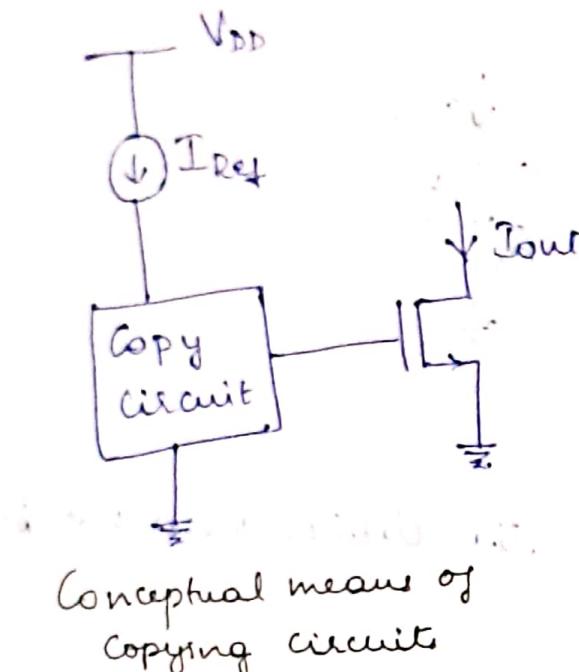
- The design of current sources in analog circuits is based on "Copying" currents from a reference, with the assumption that one precisely defined current source is already available.

## Concept of Current Miller

- The motivation behind a current mirror is to sense the current from a "golden current source" and duplicate this "golden current" to other locations.
  - Illustrated in fig, A relatively complex circuit - sometimes requiring external adjustments - is used to generate a stable reference current  $I_{ref}$ .
  - Which is then copied to many current sources into the system



How do we generate copies of a reference current? How do we guarantee  $I_{out} = I_{Ref}$ ?



for MOSFET

$$I_D = f(V_{GS})$$

where  $f(\cdot)$  denotes the functionality of  $I_D$  versus  $V_{GS}$   
then  $V_{GS} = f^{-1}(I_D)$

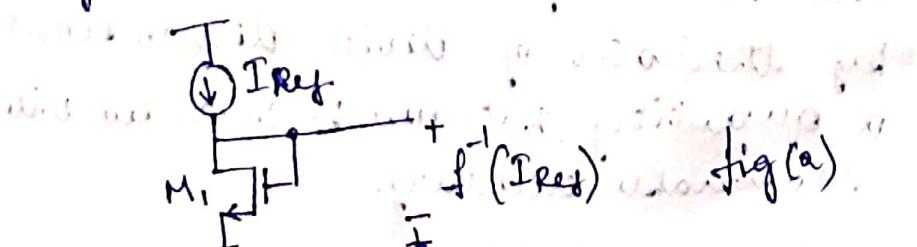
→ Thus, if this voltage that is, if a transistor is biased at  $I_{Ref}$ , then it produces:  $V_{GS} = f^{-1}(I_{Ref})$  as shown in fig(a)

→ Thus, if this voltage is applied to the gate and source terminal of a second MOSFET, the resulting current

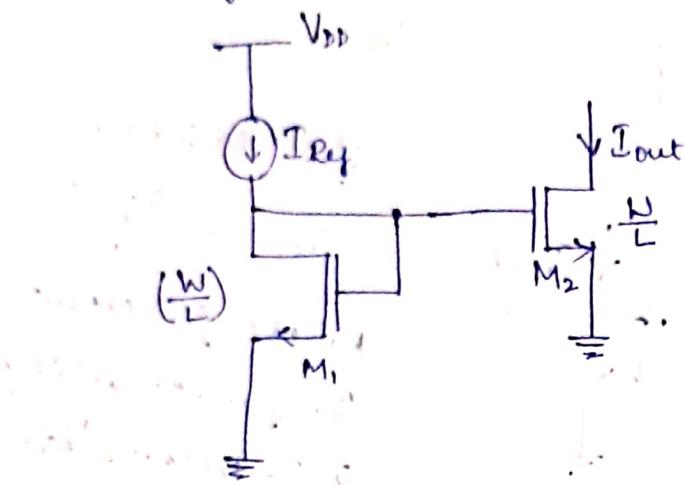
$$I_{out} = f \circ f^{-1}(I_{Ref}) = I_{Ref}$$

$$\boxed{[I_{out} = f(V_{GS})] \\ = f(f^{-1}(I_{Ref}))}$$

→ From another point of view, two identical MOS devices that have equal gate-source voltage and operate in saturation carry equal currents (if  $\lambda=0$ ).



The structure consisting of  $M_1$  and  $M_2$  in fig below is called a "current mirror".



- In general case, the devices need not be identical.
- Neglecting channel-length modulation, we can write,

$$P_{\text{ref}} = \frac{1}{2} M_2 \cos\left(\frac{w}{L}\right)_2 (V_{GS} - V_{TH})^2$$

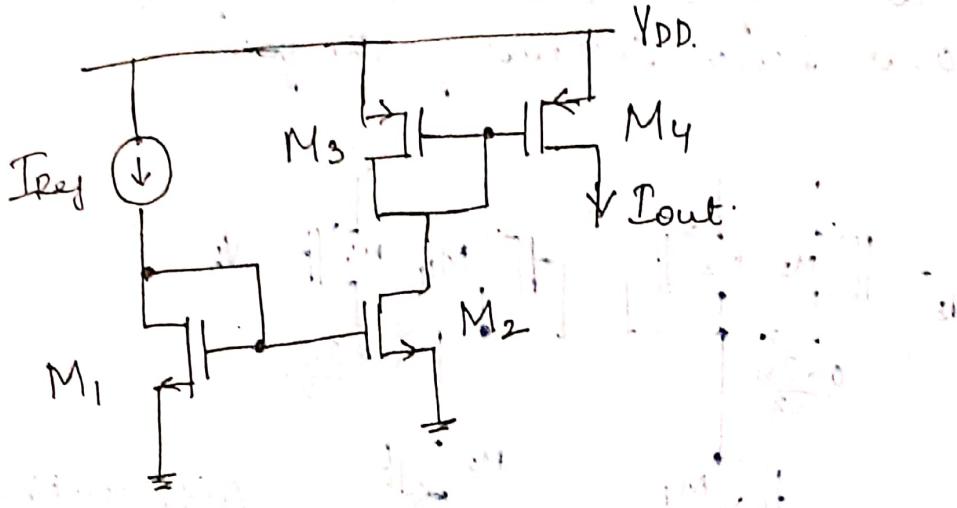
$$P_{\text{out}} = \frac{1}{2} M_2 \cos\left(\frac{w}{L}\right)_2 (V_{GS} - V_{TH})^2$$

$$P_{\text{out}} = \frac{(w/c)_2}{(w/c)_1} P_{\text{ref}}$$

- The key property of this topology is that it allows copying of the current with no dependence on process and temperature.

- The ratio of  $I_{\text{out}}$  and  $P_{\text{ref}}$  is given by the ratio of device dimensions, a quantity that can be controlled with reasonable accuracy.

find the drain current of  $M_4$  if all of the transistors are in saturation.



$$I_{D2} = \frac{(w/l)_2}{(w/l)_1} \cdot I_{ref}$$

$$|I_{D3}| = |I_{D2}|$$

$$I_{D4} = \frac{(w/l)_4}{(w/l)_3} \cdot I_{D3}$$

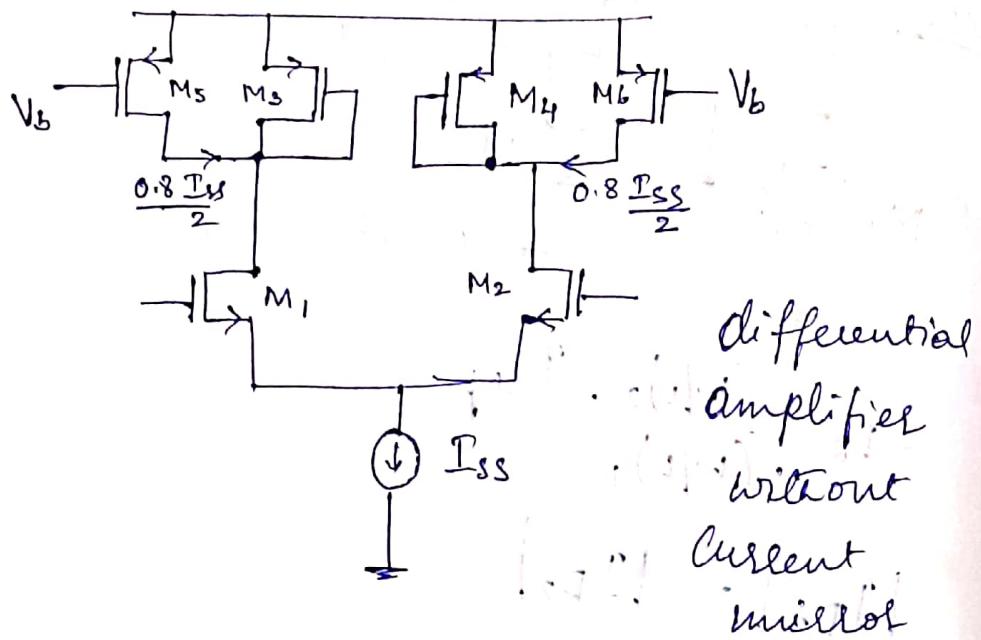
if  $\frac{(w/l)_2}{(w/l)_1} = \alpha$ , and  $\frac{(w/l)_4}{(w/l)_3} = \beta$ .

$I_{D4} = \alpha \cdot \beta \cdot I_{ref}$

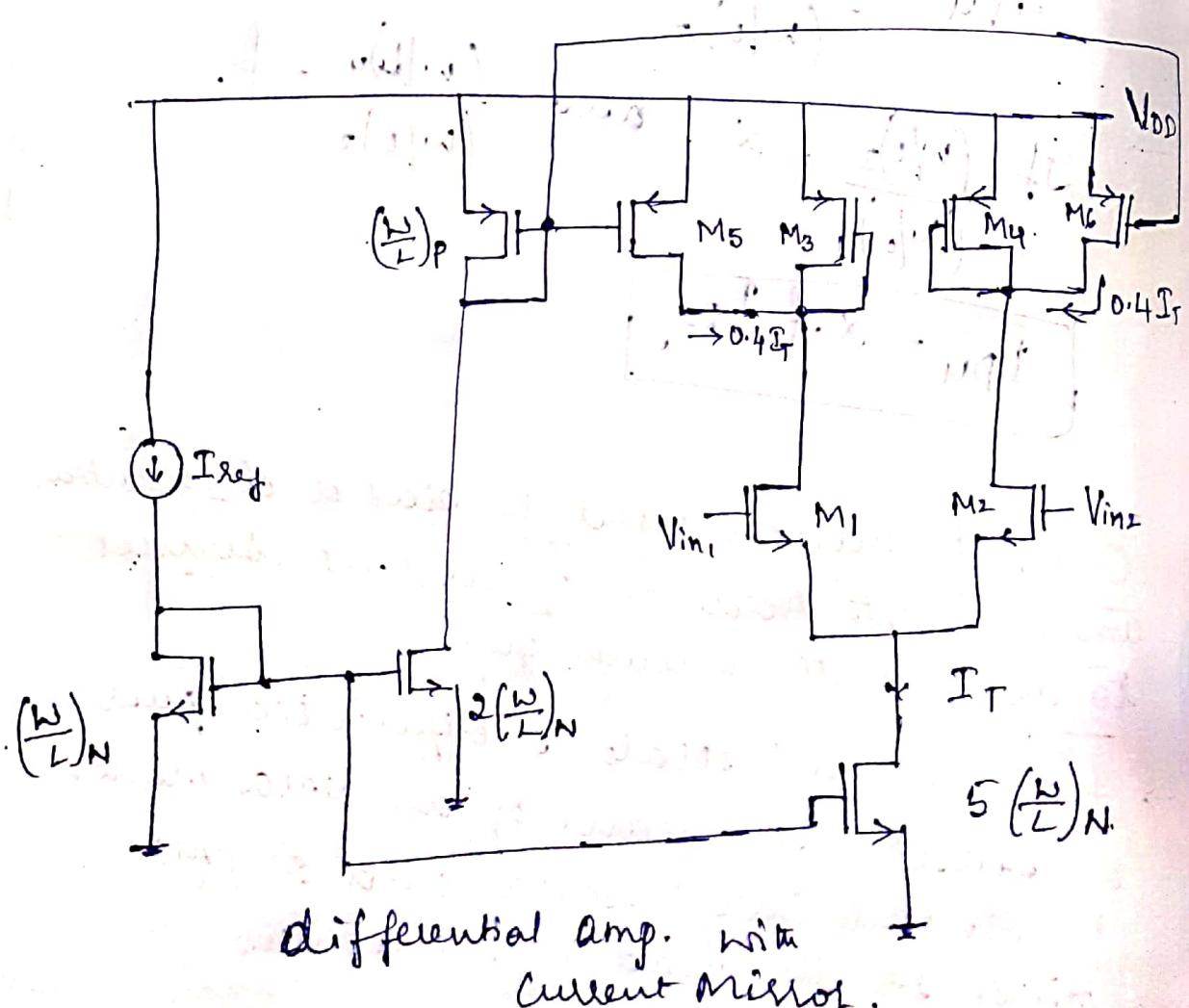
Current mirrors used to bias a differential amplifier with addition of current sources to increase the voltage gain.

→ fig below illustrates a differential pair is biased by means of an NMOS mirror for the tail current source and a PMOS mirror for the load current sources.

→ The device dimensions shown establish a drain current of  $0.4 I_T$  in  $M_5$  and  $M_6$ , reducing the drain current of  $M_3$  and  $M_4$ , and hence increasing the gain.



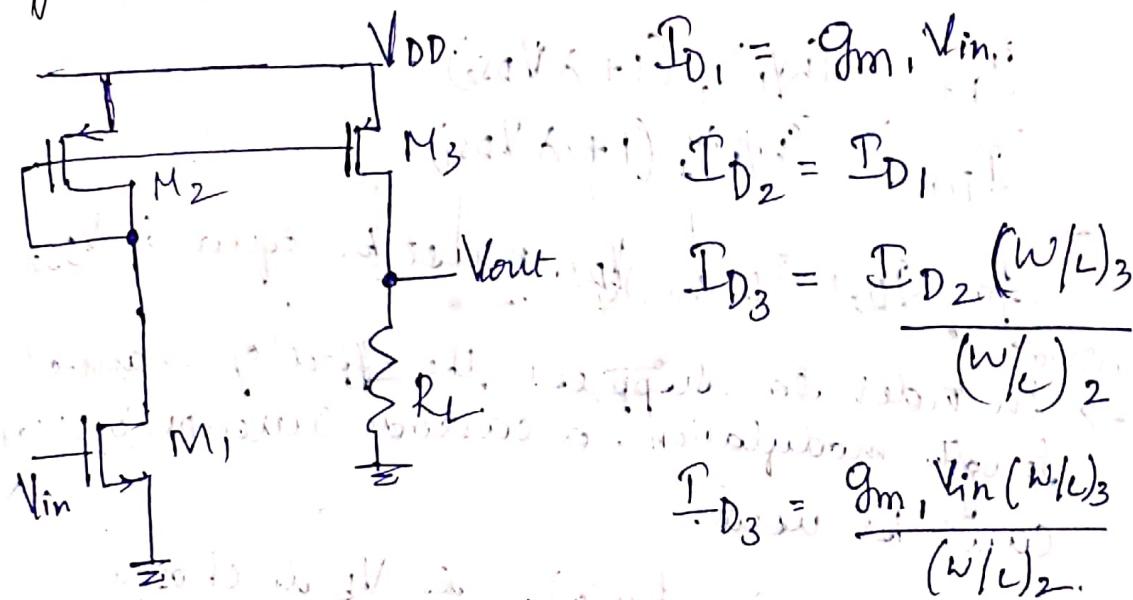
differential  
amplifier  
without  
current  
mirror



differential amp. with  
current mirror.

- Current mirrors usually employ the same length for all of the transistors so as to minimize errors due to the side-diffusion of the source and drain areas ( $L_d$ ).
  - Thus, current rationing is achieved by only scaling the width of transistors.

Calculate the small-signal voltage gain of the circuit shown in fig:



$$H_{\text{out}} = \frac{g_m V_{\text{in}} (w/c)}{R_e}$$

$$Ave = \frac{\text{Total}}{\text{Linen}} = \text{Avg. } (\frac{w/c}{c_2}) R$$

## Cascode Current Mirror

Channel length modulation effect results in significant error in copying currents.

$$I_{D_1} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS_1})$$

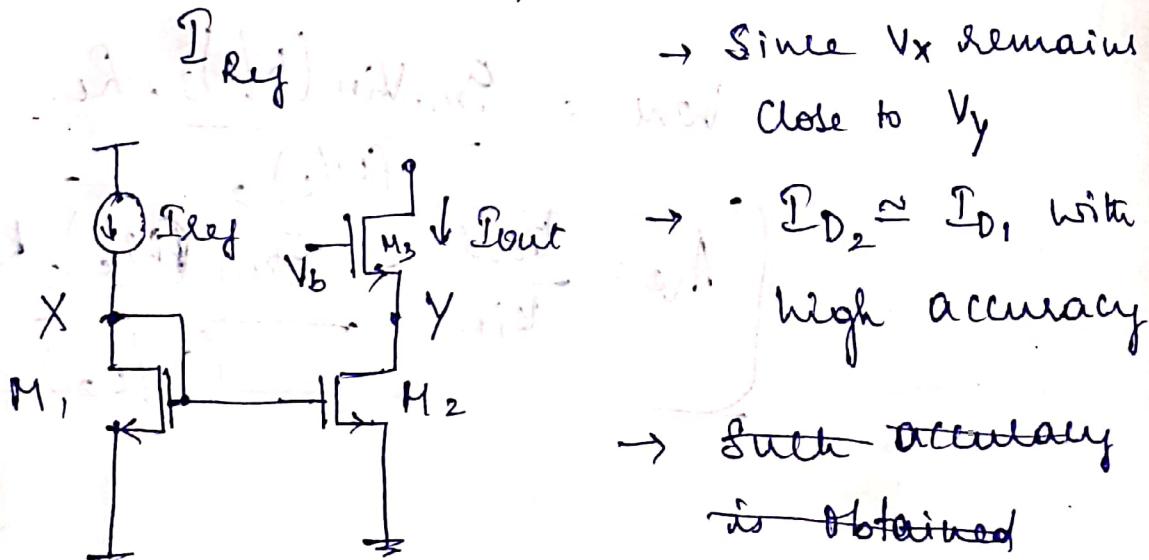
$$I_{D_2} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS_2})$$

$$\frac{I_{D_2}}{I_{D_1}} = \frac{\left(\frac{W}{L}\right)_2 (1 + \lambda V_{DS_2})}{\left(\frac{W}{L}\right)_1 (1 + \lambda V_{DS_1})}$$

for  $I_{D_2} = I_{D_1}$ ,  $V_{DS_1}$  must be equal to  $V_{DS_2}$ .

→ In order to suppress the effect of channel length modulation, a cascode current source can be used.

→ As shown in fig(a), if  $V_b$  is chosen such that  $V_y = V_x$ , then  $I_{out}$  tracks



fig(a)

$$L_3 = L_2$$

L<sub>3</sub> need not be equal to L<sub>1</sub> and L<sub>2</sub>

How do we generate  $V_b$ ?

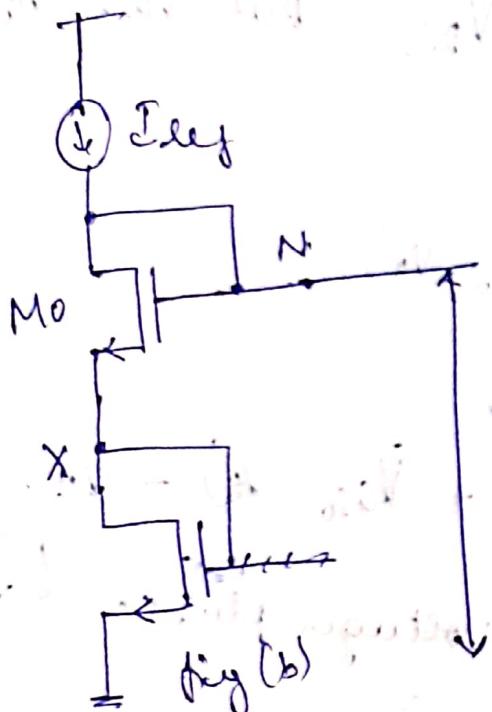
→ Objective is to ensure  $V_y = V_x$

$$\text{So } V_b - V_{GS3} = V_x$$

$$\therefore V_b = V_{GS3} + V_x$$

→ If gate-source voltage is added to  $V_x$ , the required  $V_b$  is generated. Since, as shown in fig(b)

→  $M_0 \rightarrow$  diode connected device is connected in series with  $M_1$ ,



thereby generating

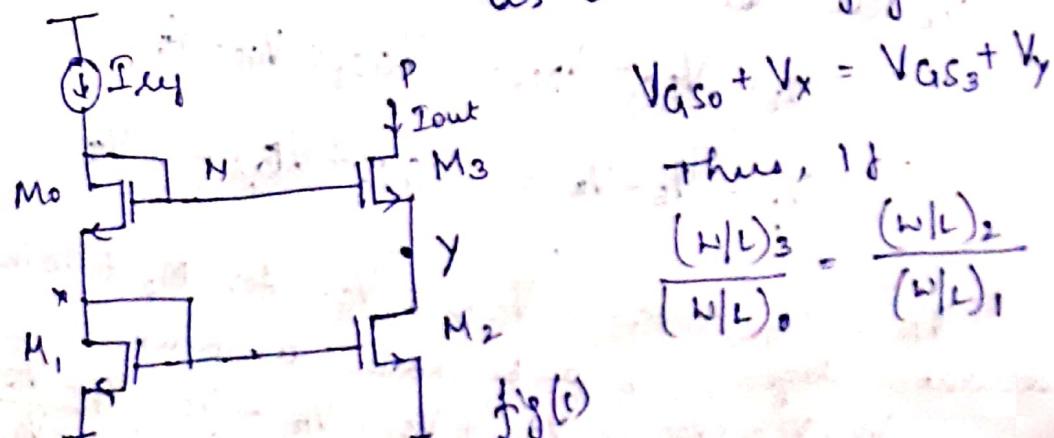
$$V_N = V_{GS0} + V_x$$

$$V_{GS0} + V_x = V_N$$

→ If  $M_0$  and  $M_3$  are identical devices,

$$\text{then } V_{GS0} = V_{GS3}$$

→ Connecting  $N$  to the gate of  $M_3$  as shown in fig(c):



$$V_{GS0} + V_x = V_{GS3} + V_y$$

Thus, if

$$\frac{(W/L)_3}{(W/L)_0} = \frac{(W/L)_2}{(W/L)_1}$$

then  $V_{GS_2} = V_{GSO}$  and  $V_x = V_y$

→ This result holds even if  $M_2$  and  $M_3$  suffer from body effect.

$$V_{GSO} = V_{GS_3} \Rightarrow V_{GD_2} = 0 \Rightarrow V_{DS_2} = V_{GS_2} = V_{GS}$$

→ The minimum allowable voltage at node P is equal to

$$V_N = V_{TH} =$$

$$V_p = V_{DS_3} + V_{DS_2} \quad \text{But } V_{DS_2} = V_{GS_2} = V_{GS}$$

$$\therefore V_p = V_{GS_3} + V_{GS_2}$$

$$V_p = V_{GS} + (V_{GSO} - V_{TH})$$

$$V_p = V_N = V_{TH}$$

$$\boxed{V_p = (V_{GS} - V_{TH}) + (V_{GSO} - V_{TH}) + V_{TH}}$$

i.e two overdrive voltages plus one threshold voltage.

→ for  $M_2$  to be in saturation region,  $V_b$  can be chosen as low as

$$V_b = V_{GS_3} + V_{DS_2} = V_{GS_3} + V_{GS} - V_{TH}$$

$$V_p = V_b - V_{TH} = V_{GS_3} + V_{GS} - 2V_{TH}$$

$V_N = V_{GS_2} + V_{GS_3} = V_{GSO} + V_{GS}$  for  $M_2$  to be in saturation region,  $V_b$  can be chosen as low as

$$V_b - V_{GS_3} + V_{DS_2} = V_{GS_3} + V_{GS} - V_{TH} \Rightarrow \boxed{V_p = V_b - V_{TH}}$$

$$\boxed{V_p = V_{GS_2} + V_{GS} - 2V_{TH}}$$

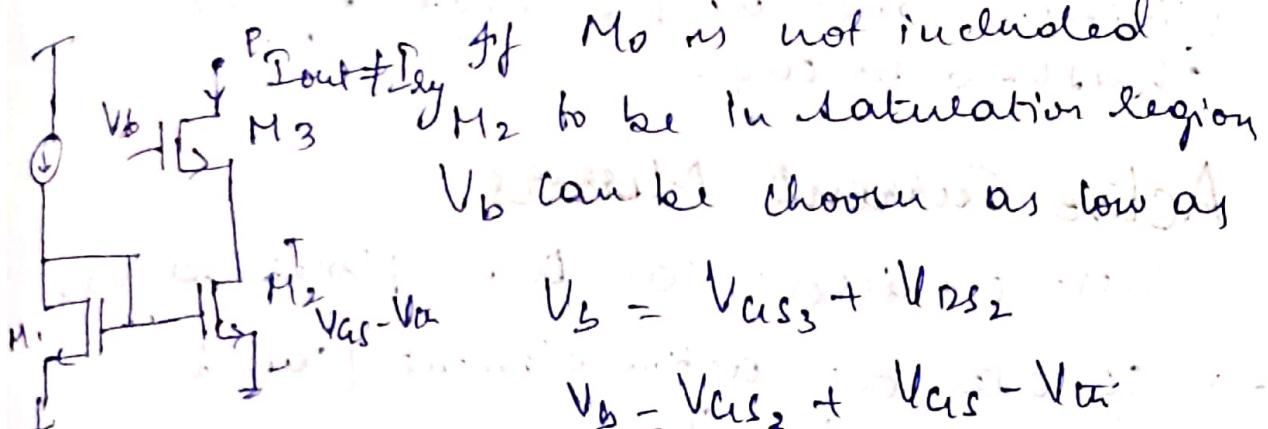
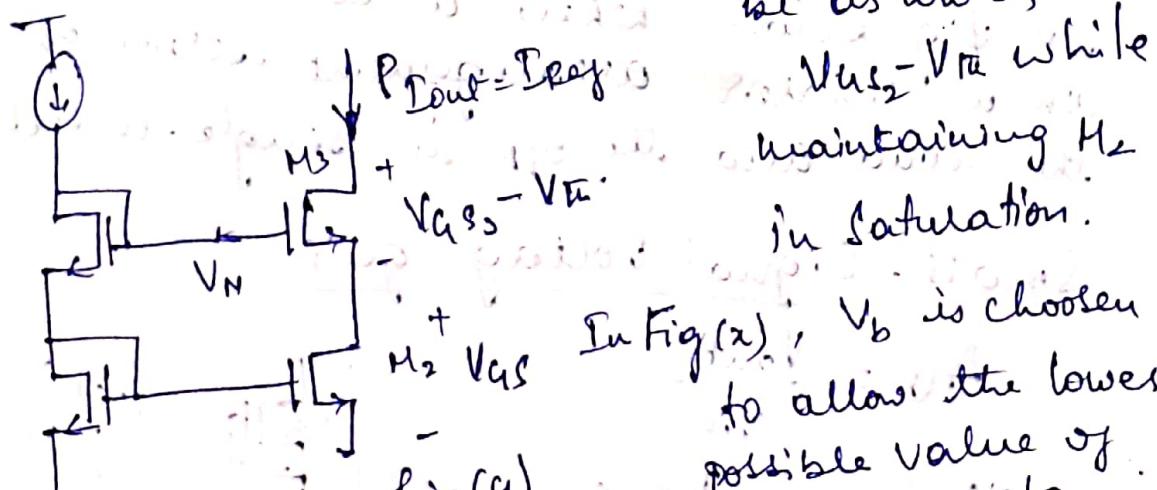


fig (x)

Cascode current:  $V_p = V_b - V_{TH}$   
 Source with minimum headroom voltage  $V_p = V_{AS3} + V_{AS} - 2V_{TH}$

from eq's & fig (x).  
 is merely two overdrive voltages. This cascode mirror "waits" one threshold voltage in the headroom as shown in fig (y). This is because  $V_{DS2} = V_{AS2}$ . Whereas  $V_{DS2}$  could



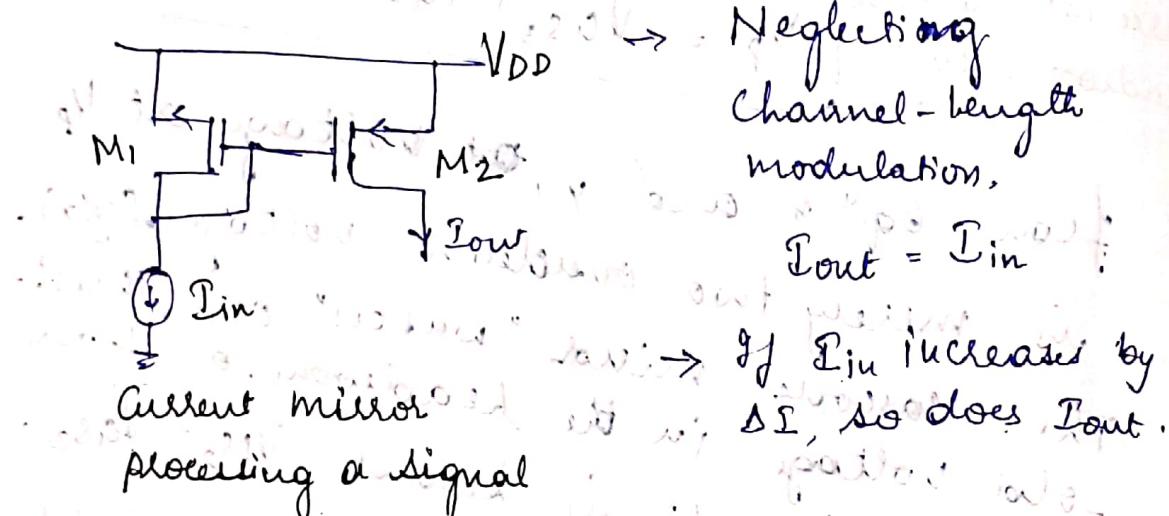
Cascode current:  $V_b$  is chosen to allow the lowest possible value of  $V_p$  but the IOP current does not accurately track  $I_{P_{ref}}$  because  $M_1$  and  $M_2$  sustain unequal  $V_{DS}$ .

fig (y) higher accuracy is achieved, but the

minimum level at P is higher by one threshold voltage.

## Active Current Mirrors

- Current Mirrors can also process signals
- Operates as active elements [can be used as load]
- As shown in fig M<sub>1</sub> and M<sub>2</sub> are identical



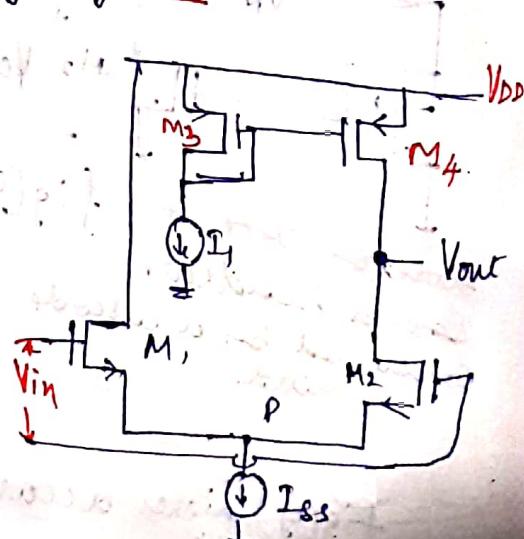
- Consider Differential Amp as shown in fig below, where a current source in a mirror arrangement serves as the load and the op-amp is single-ended.

## Small-Signal Voltage gain

$$\text{Av} = \frac{V_{out}}{V_{in}}$$

$$|\text{Av}| = G_m R_{out}$$

$$G_m = \frac{I_{out}}{V_{in}}$$



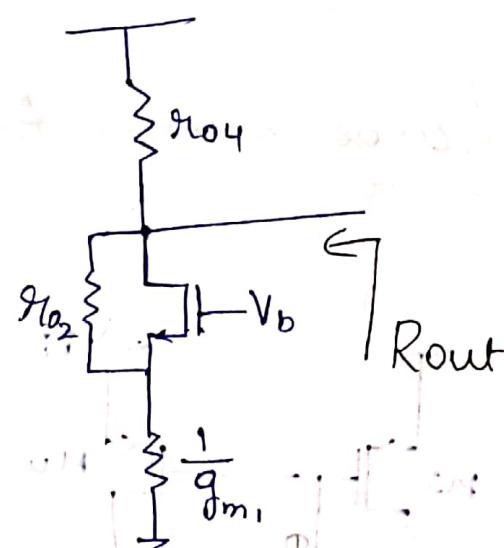
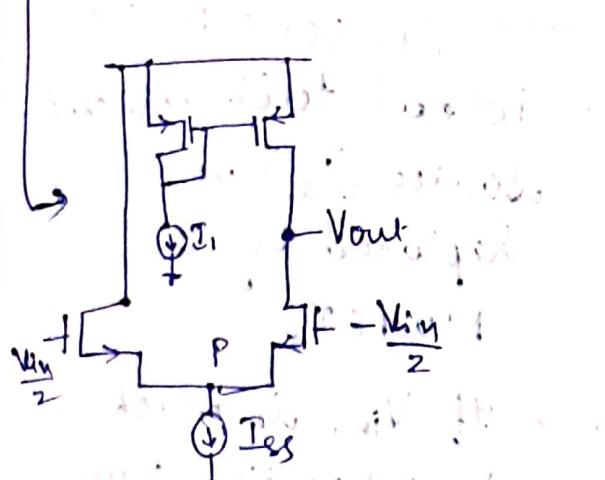
$M_1 \equiv M_2$ , the signal voltage across gate and source  $M_1$  or  $M_2$  is  $\frac{V_{in}}{2}$ .

$$g_{m1} = g_{m2}, |A_{vo}| = G_m R_{out}$$

$$G_m = \frac{P_{out}}{V_{in}} = \frac{g_{m1} \frac{V_{in}}{2}}{V_{in}} = \frac{g_{m1}}{2}$$

$\gamma = 0$  (no body effect)

The output Impedance looking into the drain of  $M_2$  is .



$$V_1 = -\frac{I_x}{g_{m1}}$$

$$I_{DQ2} = I_x - (g_{m2} V_1)$$

$$I_{DQ2} = I_x \left( 1 + \frac{g_{m2}}{g_{m1}} \right)$$

$$V_x = g_{m2} [I_x + \frac{g_{m2}}{g_{m1}} I_x] + \frac{I_x}{g_{m1}}$$

$$V_x = \left[ \left( 1 + g_{m2} \frac{g_{m2}}{g_{m1}} \right) \frac{1}{g_{m1}} + g_{m2} \right] I_x$$

$$R_{out} = \frac{V_x}{I_x} = \frac{\left( 1 + g_{m2} \frac{g_{m2}}{g_{m1}} \right) \frac{1}{g_{m1}} + g_{m2}}{g_{m1}}$$

$$R_{out} = \frac{1}{g_m} + \frac{g_{m2}r_{o2}}{g_{m1}} + r_{o2}$$

$\hookrightarrow \approx \frac{1}{g_m} + 2r_{o2} \approx 2r_{o2}$

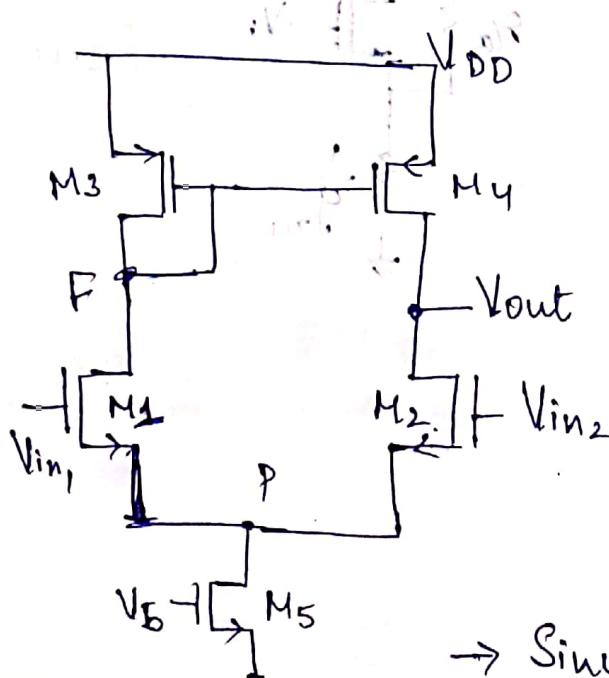
Thus  $R_{out} = R'_{out} \parallel r_{o4}$

$$|A_v| \approx \frac{g_{m1}}{2} (2r_{o2} \parallel r_{o4})$$

### Large Signal Analysis with Active Current Mirror

→ ideal tail current source ( $I_{ss}$ ) is replaced by a MOSFET.

→ If  $V_{in_1}$  is more negative than  $V_{in_2}$ ,  $M_1$  is off and so  $M_3$  and  $M_4$ .



→ Since no current can flow from  $V_{DD}$ , both  $M_2$  and  $M_5$  operates in deep triode region, carrying zero current.  $V_{out} = 0$ .

→ As  $V_{in_1}$  approaches  $V_{in_2}$  (for a small difference between  $V_{in_1}$  and  $V_{in_2}$ )  $M_1$  turns on, drawing part of

$I_{D3}$  from  $M_3$  and turning  $M_4$  ON.  
→  $V_{out}$  depends on the difference between  $I_{D4}$  and  $I_{D2}$ .

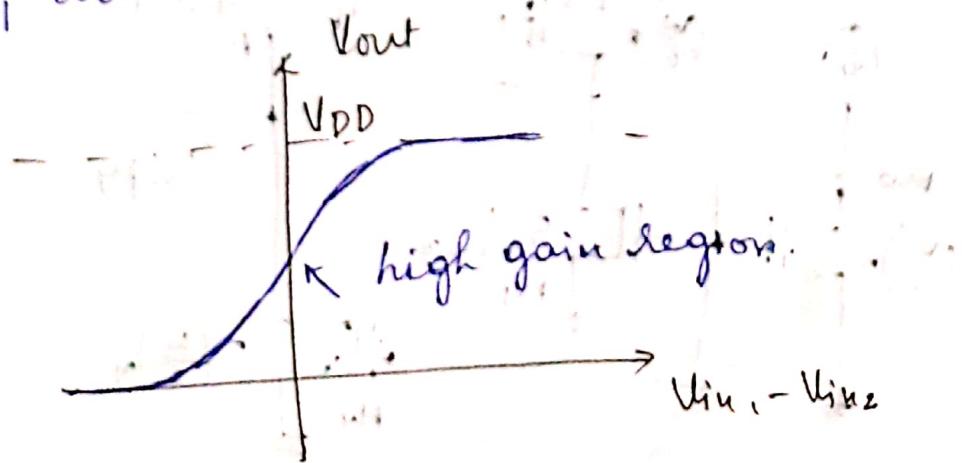
→ for a small difference bet<sup>n</sup>  $V_{in_1}$  &  $V_{in_2}$ , both  $M_2$  and  $M_3$  are saturated, providing high gain.

→ As  $V_{in_1}$  becomes more positive than  $V_{in_2}$ ,  $I_{D1}$ ,  $|I_{D3}|$  and  $|I_{D2}|$  increase

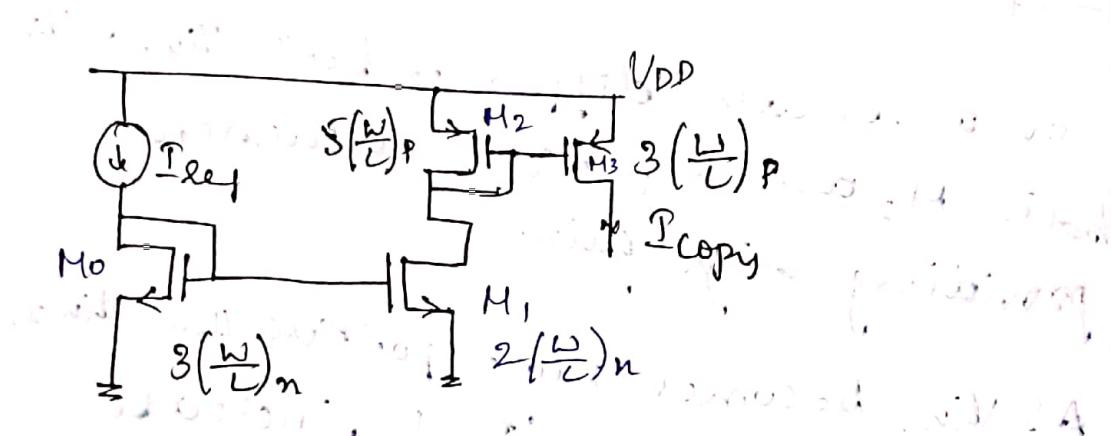
and  $I_{D2}$  decreases, eventually driving  $M_4$  into the triode region.

→ If  $V_{in_1} - V_{in_2}$  is sufficiently large,  $M_2$  turns off,  $M_4$  operates in deep triode region with no current and  $V_{out} = V_{DD}$ .

→ If  $V_F > V_{in_1} - V_{in_2}$ ,  $V_{in_1} > V_F + V_{th}$ ,  $M_1$  enters the triode region.



Calculate  $I_{\text{copy}}$  in each of the circuit.  
 Assume all of the transistors operate in saturation.

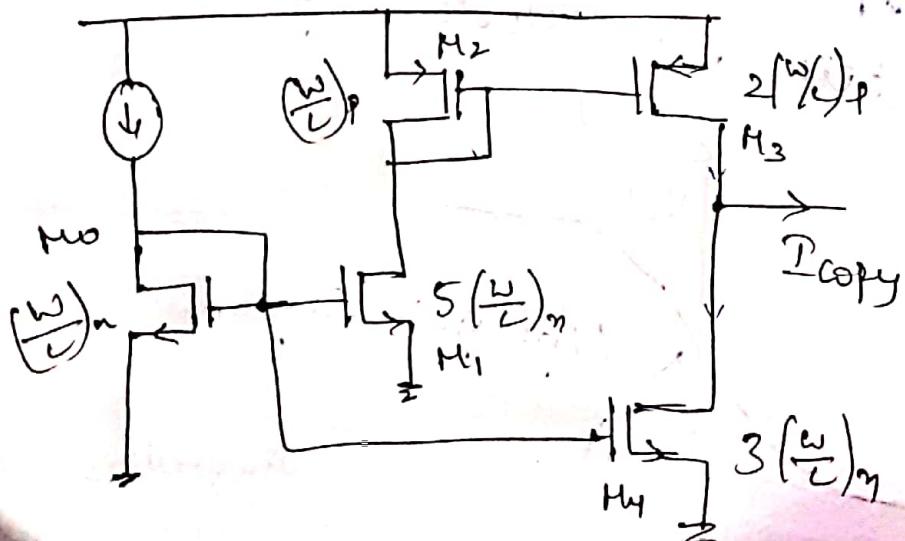


$$I_{D1} = \frac{2(w/c)n}{3(w/c)n} \cdot I_{\text{ref}} = \frac{2}{3} I_{\text{ref}}$$

$$I_{D2} = I_{D1} = \frac{2}{3} I_{\text{ref}}$$

$$I_{\text{copy}} = \frac{3(w/c)p}{5(w/c)p} \cdot \frac{2}{3} I_{\text{ref}} = \frac{2}{5} I_{\text{ref}}$$

$$\Rightarrow \frac{2}{5} I_{\text{ref}}$$



$$I_{D1} = 5 I_{Ref}$$

$$I_{D3} = \frac{2}{3} \times 5 I_{Ref} = 10 I_{Ref}$$

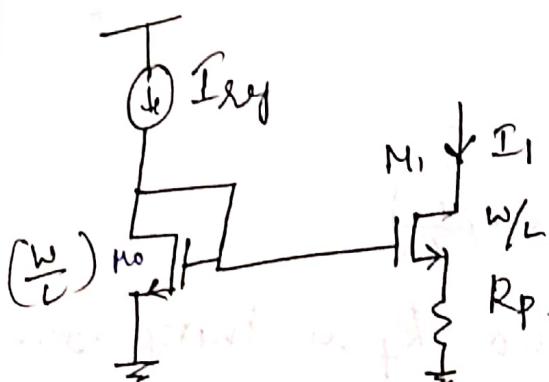
$$I_{D4} = 3 I_{Ref}$$

$$I_{Copy} = I_{D3} - I_{D4}$$

$$= (10 - 3) I_{Ref}$$

$$\rightarrow = 7 I_{Ref}$$

Determine the value of  $R_p$  in the circuit such that  $I_1 = I_{Ref}/2$ . With this choice of  $R_p$ , does  $I_1$  change if the threshold voltage of both transistors



$$V_{GS0}$$

$$V_{GS0} = \sqrt{\frac{2 I_{Ref}}{M_n C_o \frac{w}{L}}} + V_{th}$$

Assuming  $M_1$  in saturation.

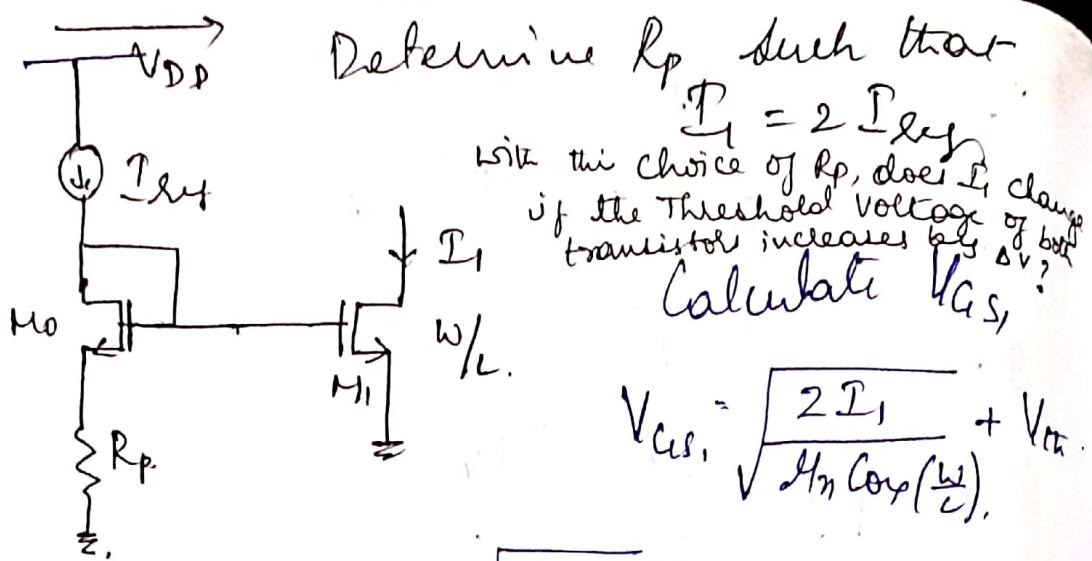
$$I_1 = \frac{1}{2} M_n C_o \left(\frac{w}{L}\right) \left[V_{GS1} - V_{Tg}\right]^2$$

$$I_1 = \frac{I_{Ref}}{2}$$

$$I_{Ref} = \frac{1}{2} M_n C_o \left(\frac{w}{L}\right) \left[V_{GS0} - \frac{I_{Ref}}{2} R_p - V_{th}\right]$$

Rearrange, substitute (1) into equation above and solve for  $R_p$ .

$$R_p = \frac{2(\sqrt{2} - 1)}{\sqrt{I_{Ref} M_n C_o \left(\frac{w}{L}\right)}}$$



$$V_{GS1} = \sqrt{\frac{2I_1}{M_n C_{ox}(\frac{W}{L})}} + V_{th}.$$

$$V_{GS1} = 2 \sqrt{\frac{I_1}{M_n C_{ox}(\frac{W}{L})}} + V_{th} \rightarrow ①$$

$$I_{ref} = \frac{1}{2} M_n C_{ox} \left( \frac{W}{L} \right) (V_{GS0} - V_{th})^2$$

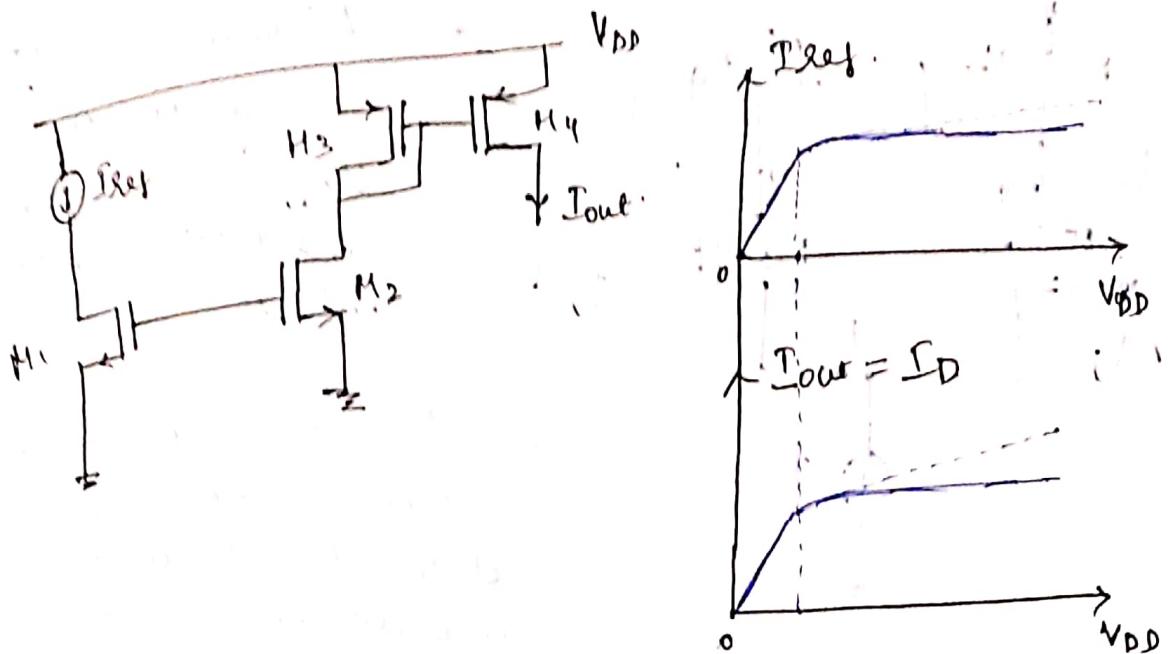
$$\rightarrow = \frac{1}{2} M_n C_{ox} \left( \frac{W}{L} \right) (V_{GS1} - I_{ref} R_p - V_{th})^2$$

$$I_{ref} = \frac{1}{2} M_n C_{ox} \left( \frac{W}{L} \right) \left[ 2 \sqrt{\frac{I_{ref}}{M_n C_{ox} \left( \frac{W}{L} \right)}} - I_{ref} R_p \right]^2$$

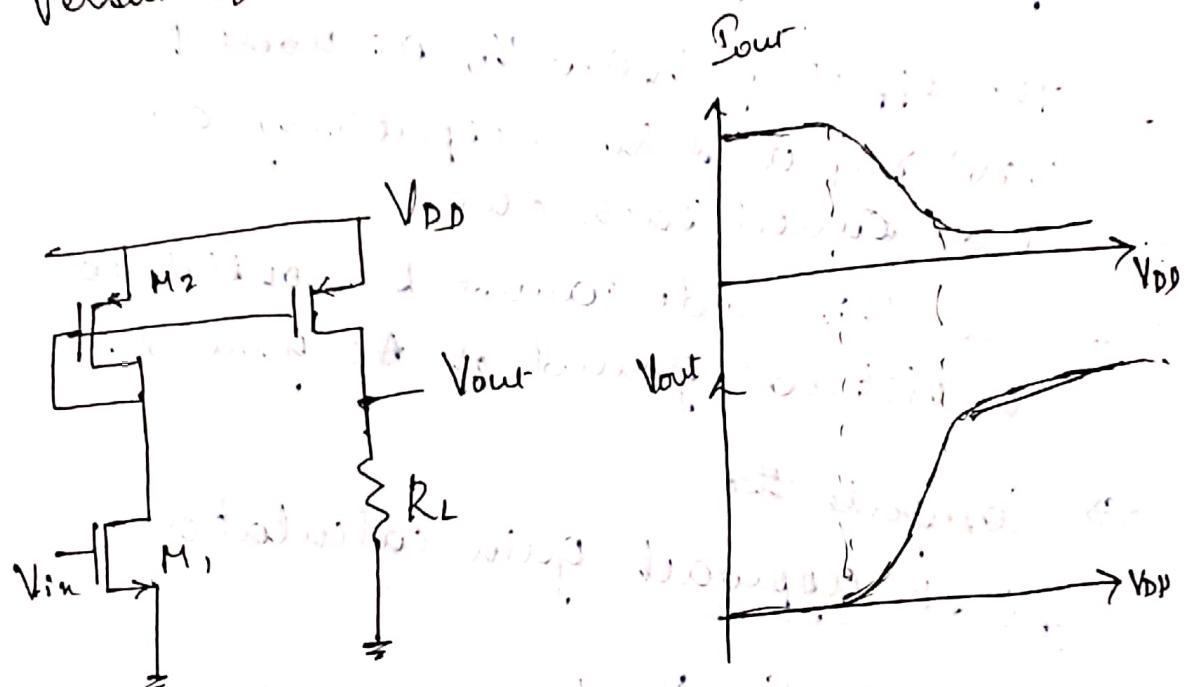
$$R_p = \frac{(2 - \sqrt{2})}{\sqrt{I_{ref} M_n C_{ox} \left( \frac{W}{L} \right)}}$$

from ①, we find that  $R_p$  is independent of any change in  $V_{th}$ ,  $\Delta V$ .

for the circuit given, Assuming  $I_{ref}$  is ideal, sketch  $I_{out}$  versus  $V_{DD}$  as  $V_{DD}$

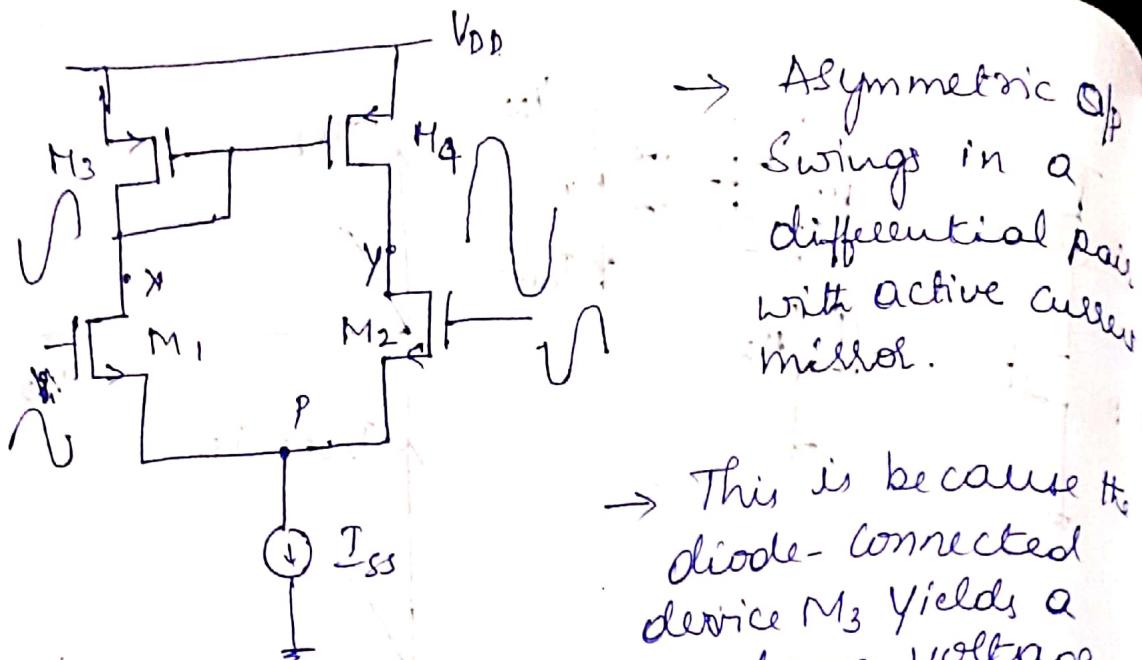


for the circuit given, sketch  $V_{out}$  versus  $V_{DD}$  as  $V_{DD}$  varies from 0 to 3V.



## Small-Signal Analysis with Current Active Current mirror.

- Half-circuit concept to calculate the differential gain.
- With small differential inputs, the voltage swings at nodes x and y are vastly different.



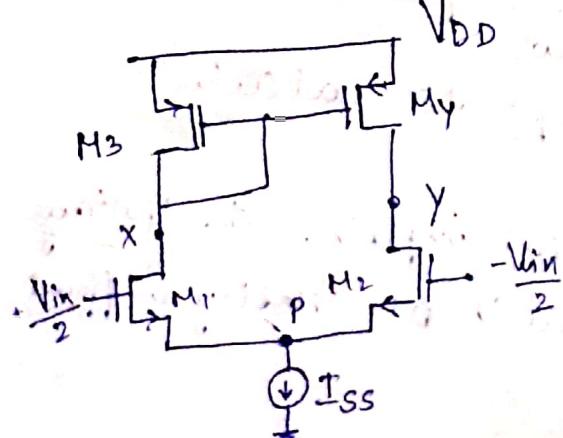
→ Asymmetric Op  
Swings in a differential pair  
with active cascode mirror.

→ This is because the  
diode-connected  
device M<sub>3</sub> yields a  
much lower voltage  
gain from input to  
node X, than that  
from the input to node Y.

- The effect of  $V_x$  and  $V_y$  at node P  
through  $r_{o1}$  and  $r_{o2}$  respectively do  
not cancel each other.
- So this node cannot be considered  
a virtual ground or AC ground.

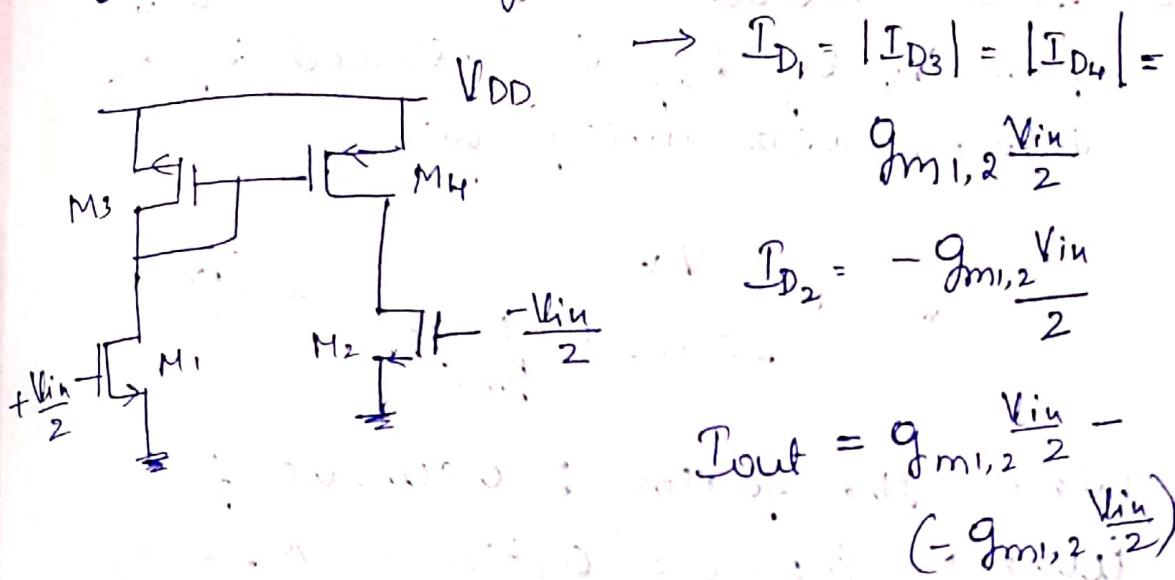
→ Complete the  
first approach gain calculation

$$|A_V| = G_m R_{out}$$



→ The circuit is  
not quite symmetric  
but because the  
impedance seen at  
node X is relatively  
low and the swing  
at this node small,

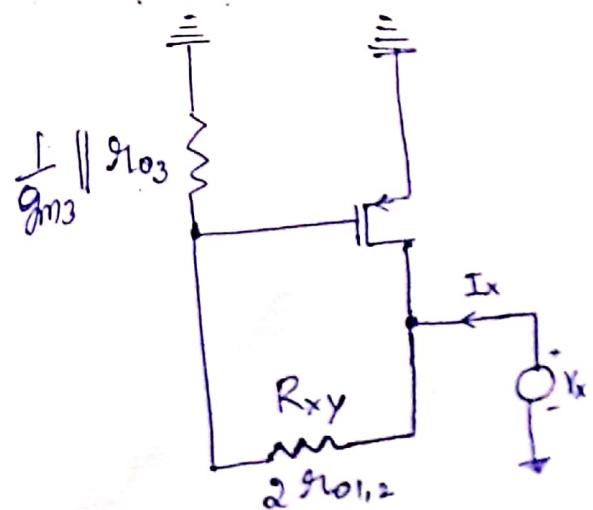
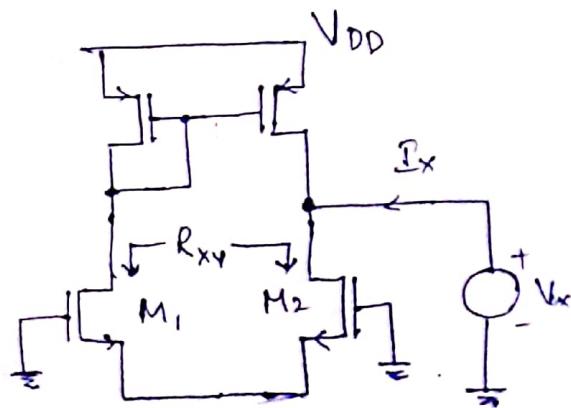
the current returning from  $x$  to path 2,  $i_{D_2}$ , is negligible and  $p$  can be viewed as a virtual ground.



$$|G_m| = g_{m1,2} \frac{V_{in}}{2}$$

$$|G_m| = \frac{I_{out}}{V_{in}} = g_{m1,2}$$

- When a voltage is applied to the output to measure  $R_{out}$ , the gate-to-source voltage of  $M_4$  does not remain constant.
- The respective equivalent circuit is as shown below.



- for small signals,  $I_{ss}$  is open, any current flowing into  $M_1$  must flow out of  $M_2$  and role of the

two transistors can be represented by a resistor  $R_{xy} = 2g_{o1,2}$

→ As a consequence, the current drawn from  $V_x$  by  $R_{xy}$  is mirrored by  $M_3$  into  $M_4$  with unity gain.

$$I_x = 2 \frac{V_x}{2g_{o1,2} + \frac{1}{g_{m3}} \| g_{o3}} + \frac{V_x}{g_{o4}}$$

Where the factor 2 accounts for current copying action of  $M_3$  &  $M_4$

$$\text{for } 2g_{o1,2} \gg \left( \frac{1}{g_{m3}} \| g_{o3} \right)$$

$$R_{out} = \frac{V_x}{I_x} = \left( \frac{1}{g_{o1,2}} + \frac{1}{g_{o4}} \right)$$

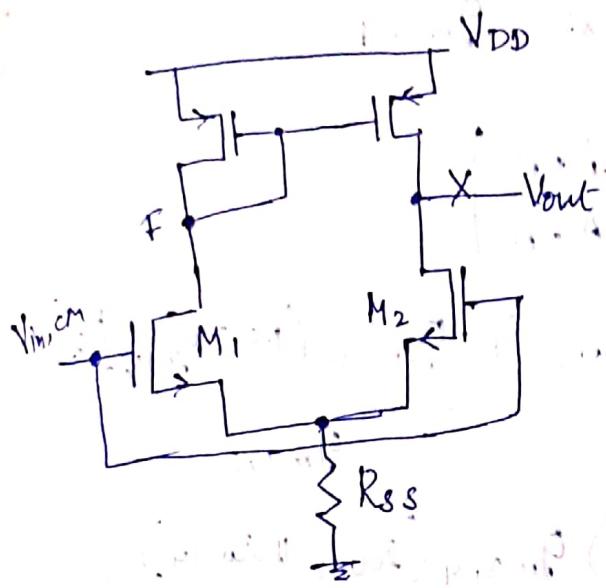
$$R_{out} \approx g_{o1,2} \| g_{o4}$$

The overall voltage gain is

$$|Av| = G_m R_{out} = g_{m1,2} (g_{o1,2} \| g_{o4})$$

## Common-Mode Properties

- Common-mode properties of the differential pair with active current mirror.
- Objective is to predict the consequences of a finite output impedance in the tail current source.

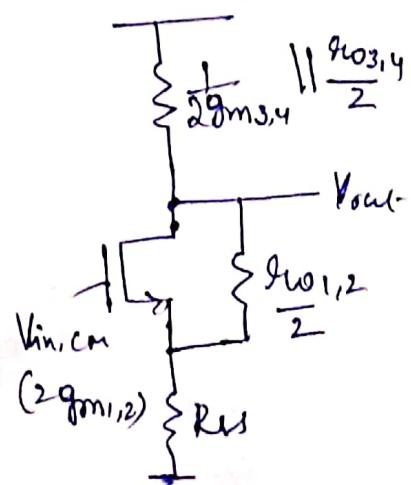
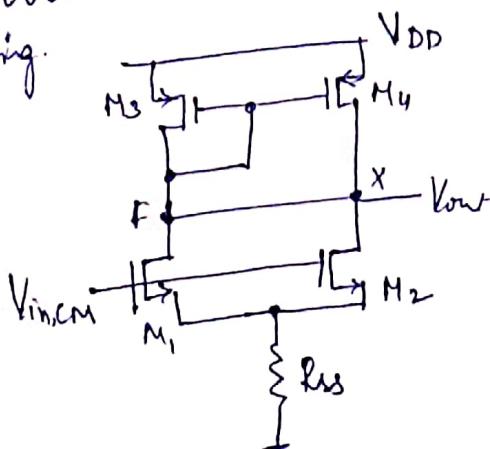


→ In the fig., the output signal of interest is denoted with respect to ground.

→ Thus, the CM gain in terms of the single-ended output component produced by the input CM change

$$A_{CM} = \frac{\Delta V_{out}}{\Delta V_{in,CM}}$$

- To determine  $A_{CM}$ , Assume Circuit is symmetric,  $V_{out} = V_F$  for any input level
- for example, as  $V_{in,CM}$  increases,  $V_F$  drops and  $V_{out}$
- nodes F and X can be shorted as shown in fig.



in above equivalent circuit,  $M_1$  and  $M_2$  appear in parallel &  $M_3$  and  $M_4$  in parallel.

$$A_{CM} \approx \frac{-\frac{1}{2g_{m3,4}} \parallel \frac{r_{o3,4}}{2}}{\frac{1}{2g_{m1,2}} + R_{SS}} \rightarrow \text{the effect of } \frac{r_{o1,2}}{2} \text{ is neglected}$$

$$A_{CM} \approx \frac{-1}{1 + 2g_{m1,2}R_{SS}} \cdot \frac{g_{m1,2}}{g_{m3,4}}$$

$$CMRR = \left| \frac{A_{DM}}{A_{CM}} \right|$$

$$= g_{m1,2} (r_{o1,2} \parallel r_{o3,4}) \cdot g_{m3,4} (1 + 2g_{m1,2}R_{SS})$$

$$\boxed{CMRR = (1 + 2g_{m1,2}R_{SS}) g_{m3,4} (r_{o1,2} \parallel r_{o3,4})}$$

## Large Signal Analysis of Diff. pair with Active Miller Curren

→ If  $V_{in} > V_{in_1} < V_{in_2}$  [  $V_{in_1}$  is more negative

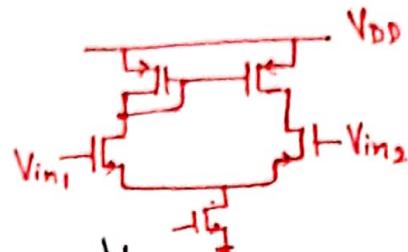
$M_1$  is off.

$M_3$  &  $M_4$  off.

no current flows from  $V_{DD}$ ,

$M_2$  and  $M_5$  operate in deep triode region, carrying zero current.

Thus  $V_{out} = 0$ .



→  $V_{in} < V_{in_1} < V_{in_2}$

$M_1$  turns ON.

$M_3$  and  $M_4$  ON.

$V_{out}$  depends on the difference bet<sup>n</sup>  $I_{D4}$  and  $I_{D2}$ .

→  $V_{in_1}$  is more positive than  $V_{in_2}$ ,  $|I_{D1}|$  and  $|I_{D4}|$  increases

and  $|I_{D2}|$  decreases.

eventually driving  $M_4$  into triode region.

$V_{out} \uparrow$   $M_Q \downarrow$  hence  
 $M_Q \rightarrow$  Triode region

$$P_{MOS} \\ V_{DS} > V_{GS} - V_t \\ \underbrace{V_{out} - V_{DD}}_{\downarrow V_Q} \quad \downarrow V_{DD} - V_t$$

- If  $V_{in_1} - V_{in_2}$  is sufficiently large,  $M_2$  turns off,  $M_4$  operates in deep triode region with zero current and  $V_{out} = V_{DD}$ .
- If  $V_{in_1} > V_F + V_{th}$ , then  $M_1$  enters the triode region.
- The choice of the input common mode voltage of the circuit is also important.
- $M_2$  to be in saturation, the output voltage cannot be less than  $V_{in_1} - V_{th}$ .  
Thus, to allow max. output swings, the  $V_{in_1}$  less must be as low as possible, with the min. given by  $V_{as1,2} + V_{DS, min}$ .
- The direct relationship between the input CM level and the output swing in this circuit is a critical drawback.

$V_{in_1} = V_{in_2}$  what is the op voltage  
with perfect symmetry.

$$V_{out} = V_f = V_{DD} - |V_{GS3}|.$$

This proved by contradiction as well

$V_{out} < V_f$ . Then, due to CLM,  $M_1$  must carry a greater current than  $M_2$

$[M_4$  is greater current than  $M_3]$ .

→ The total current thro'  $M_1$  is greater than  $\frac{I_{SS}}{2}$

→ But this means that the total current thro'  $M_3$  also exceeds  $\frac{I_{SS}}{2}$

→ Violating the assumption that  $M_4$  carries more current than  $M_3$ .

→ In reality, asymmetries in the circuit may result in a large deviation in  $V_{out}$ , possibly driving  $M_2$  or  $M_4$  into the triode region.

→ if  $V_{in_2} < V_{in_1}$ ,  $V_{in_1} = V_{in_2}$  causing  $V_{out}$  to drop significantly.

→ For this reason, the circuit is rarely used in an open loop configuration to amplify small signals.