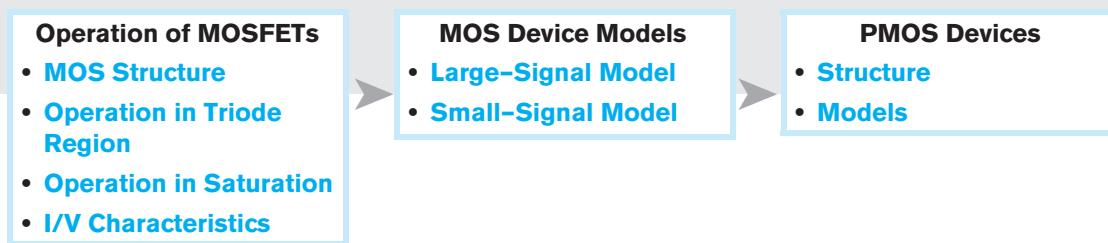


Physics of MOS Transistors

Today's field of microelectronics is dominated by a type of device called the metal-oxide-semiconductor field-effect transistor (MOSFET). Conceived in the 1930s but first realized in the 1960s, MOSFETs (also called MOS devices) offer unique properties that have led to the revolution of the semiconductor industry. This revolution has culminated in microprocessors having 100 million transistors, memory chips containing billions of transistors, and sophisticated communication circuits providing tremendous signal processing capability.

Our treatment of MOS devices and circuits follows the same procedure as that taken in Chapters 2 and 3 for *pn* junctions. In this chapter, we analyze the structure and operation of MOSFETs, seeking models that prove useful in circuit design. In Chapter 7, we utilize the models to study MOS amplifier topologies. The outline below illustrates the sequence of concepts covered in this chapter.



6.1

STRUCTURE OF MOSFET

Recall from Chapter 5 that any voltage-controlled current source can provide signal amplification. MOSFETs also behave as such controlled sources but their characteristics are different from those of bipolar transistors.

In order to arrive at the structure of the MOSFET, we begin with a simple geometry consisting of a conductive (e.g., metal) plate, an insulator ("dielectric"), and a doped

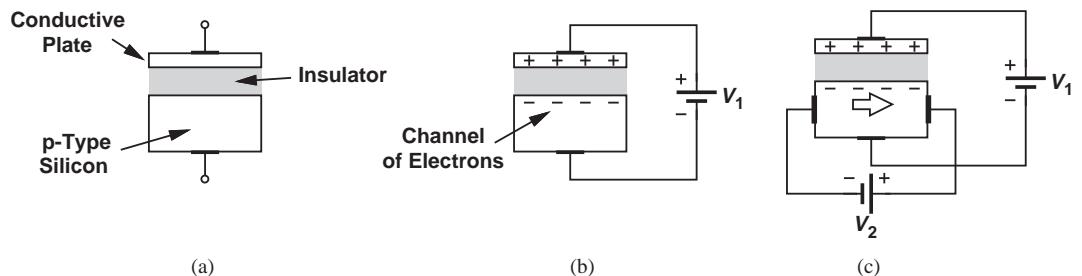


Figure 6.1 (a) Hypothetical semiconductor device, (b) operation as a capacitor, (c) current flow as a result of potential difference.

piece of silicon. Illustrated in Fig. 6.1(a), such a structure operates as a capacitor because the *p*-type silicon is somewhat conductive, “mirroring” any charge deposited on the top plate.

What happens if a potential difference is applied as shown in Fig. 6.1(b)? As positive charge is placed on the top plate, it attracts negative charge, e.g., electrons, from the piece of silicon. (Even though doped with acceptors, the *p*-type silicon does contain a small number of electrons.) We therefore observe that a “channel” of *free* electrons may be created at the interface between the insulator and the piece of silicon, potentially serving as a good conductive path if the electron density is sufficiently high. The key point here is that the density of electrons in the channel *varies* with V_1 , as evident from $Q = CV$, where C denotes the capacitance between the two plates.

The dependence of the electron density upon V_1 leads to an interesting property: if, as depicted in Fig. 6.1(c), we allow a current to flow from left to right through the silicon material, V_1 can *control* the current by adjusting the resistivity of the channel. (Note that the current prefers to take the path of least resistance, thus flowing primarily through the channel rather than through the entire body of silicon.) This will serve our objective of building a voltage-controlled current source.

Equation $Q = CV$ suggests that, to achieve a strong control of Q by V , the value of C must be maximized, for example, by *reducing* the thickness of the dielectric layer separating the two plates.¹ The ability of silicon fabrication technology to produce extremely thin but uniform dielectric layers (with thicknesses below 20 Å today) has proven essential to the rapid advancement of microelectronic devices.

The foregoing thoughts lead to the MOSFET structure shown in Fig. 6.2(a) as a candidate for an amplifying device. Called the “gate” (G), the top conductive plate resides on a thin dielectric (insulator) layer, which itself is deposited on the underlying *p*-type silicon “substrate.” To allow current flow through the silicon material, two contacts are attached to the substrate through two heavily-doped *n*-type regions because direct connection of metal to the substrate would not produce a good “ohmic” contact.² These two terminals are called “source” (S) and “drain” (D) to indicate that the former can *provide* charge carriers and the latter can *absorb* them. Figure 6.2(a) reveals that the device is symmetric with respect to S and D; i.e., depending on the voltages applied to the device, either of

¹The capacitance between two plates is given by $\epsilon A/t$, where ϵ is the “dielectric constant” (also called the “permittivity”), A is the area of each plate, and t is the dielectric thickness.

²Used to distinguish it from other types of contacts such as diodes, the term “ohmic” contact emphasizes bi-directional current flow—as in a resistor.

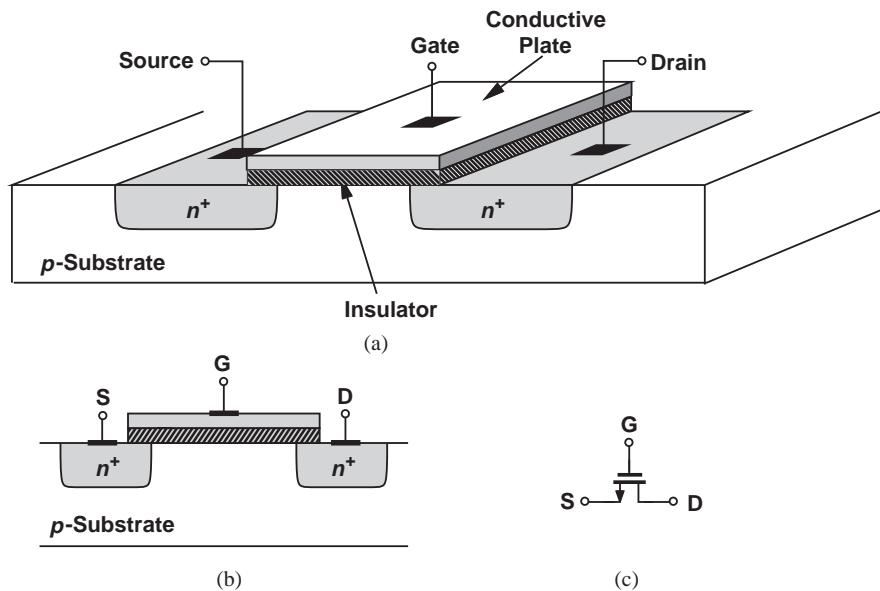


Figure 6.2 (a) Structure of MOSFET, (b) side view, (c) circuit symbol.

these two terminals can drain the charge carriers from the other. As explained in Section 6.2, with *n*-type source/drain and *p*-type substrate, this transistor operates with electrons rather than holes and is therefore called an *n*-type MOS (NMOS) device. (The *p*-type counterpart is studied in Section 6.4.) We draw the device as shown in Fig. 6.2(b) for simplicity. Figure 6.2(c) depicts the circuit symbol for an NMOS transistor, wherein the arrow signifies the source terminal.

Before delving into the operation of the MOSFET, let us consider the types of materials used in the device. The gate plate must serve as a good conductor and was in fact realized by metal (aluminum) in the early generations of MOS technology. However, it was discovered that noncrystalline silicon (“polysilicon” or simply “poly”) with heavy doping (for low resistivity) exhibits better fabrication and physical properties. Thus, today’s MOSFETs employ polysilicon gates.

The dielectric layer sandwiched between the gate and the substrate plays a critical role in the performance of transistors and is created by growing silicon dioxide (or simply

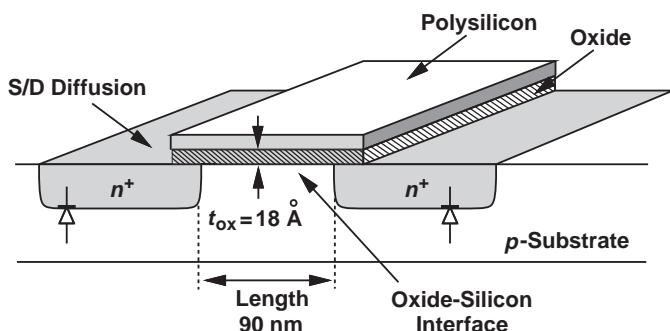


Figure 6.3 Typical dimensions of today’s MOSFETs.

“oxide”) on top of the silicon area. The n^+ regions are sometimes called source/drain “diffusion,” referring to a fabrication method used in early days of microelectronics. We should also remark that these regions in fact form *diodes* with the *p*-type substrate (Fig. 6.3). As explained later, proper operation of the transistor requires that these junctions remain reverse-biased. Thus, only the depletion region capacitance associated with the two diodes must be taken into account. Figure 6.3 shows some of the device dimensions in today’s state-of-the-art MOS technologies. The oxide thickness is denoted by t_{ox} .

6.2

OPERATION OF MOSFET

This section deals with a multitude of concepts related to MOSFETs. The outline is shown in Fig. 6.4.



Figure 6.4 Outline of concepts to be studied.

6.2.1 Qualitative Analysis

Our study of the simple structures shown in Figs. 6.1 and 6.2 suggests that the MOSFET may conduct current between the source and drain if a channel of electrons is created by making the gate voltage sufficiently positive. Moreover, we expect that the magnitude of the current can be controlled by the gate voltage. Our analysis will indeed confirm these conjectures while revealing other subtle effects in the device. Note that the gate terminal draws no (low-frequency) current as it is insulated from the channel by the oxide.

Since the MOSFET contains three terminals,³ we may face many combinations of terminal voltages and currents. Fortunately, with the (low-frequency) gate current being zero, the only current of interest is that flowing between the source and the drain. We must study the dependence of this current upon the gate voltage (e.g., for a constant drain voltage) and upon the drain voltage (e.g., for a constant gate voltage). These concepts become clearer below.

Let us first consider the arrangement shown in Fig. 6.5(a), where the source and drain are grounded and the gate voltage is varied. This circuit does not appear particularly useful but it gives us a great deal of insight. Recall from Fig. 6.1(b) that, as V_G rises, the positive charge on the gate must be mirrored by negative charge in the substrate. While we stated in Section 6.1 that electrons are attracted to the interface, in reality, another phenomenon precedes the formation of the channel. As V_G increases from zero, the positive charge on the gate *repels* the holes in the substrate, thereby exposing negative ions and creating a depletion region [Fig. 6.5(b)].⁴

Did you know?

The concept of MOSFET was proposed by Julius Edgar Lilienfeld in 1925, decades before the invention of the bipolar transistor. But why did it take until the 1960s for the MOS transistor to be successfully fabricated? The critical issue was the oxide-silicon interface. In initial attempts, this interface contained many “surface states,” trapping the charge carriers and leading to poor conduction. As semiconductor technology advanced and “clean rooms” were invented for fabrication, the oxide could be grown on silicon with almost no surface states, yielding a high transconductance.

³The substrate acts as a fourth terminal, but we ignore that for now.

⁴Note that this depletion region contains only one immobile charge polarity, whereas the depletion region in a *pn* junction consists of two areas of negative and positive ions on the two sides of the junction.

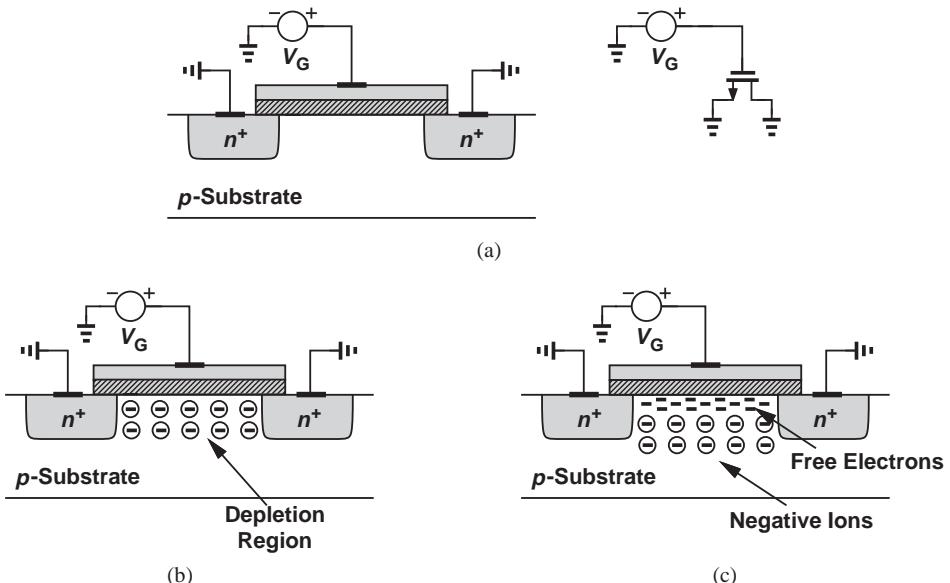


Figure 6.5 (a) MOSFET with gate voltage, (b) formation of depletion region, (c) formation of channel.

Note that the device still acts as a capacitor—positive charge on the gate is mirrored by negative charge in the substrate—but no channel of *mobile* charge is created yet. Thus, no current can flow from the source to the drain. We say the MOSFET is off.

Can the source-substrate and drain-substrate junctions carry current in this mode? To avoid this effect, the substrate itself is also tied to zero, ensuring that these diodes are not forward-biased. For simplicity, we do not show this connection in the diagrams.

What happens as V_G increases? To mirror the charge on the gate, more negative ions are exposed and the depletion region under the oxide becomes deeper. Does this mean the transistor never turns on?! Fortunately, if V_G becomes sufficiently positive, free electrons are attracted to the oxide-silicon interface, forming a conductive channel [Fig. 6.5(c)]. We say the MOSFET is on. The gate potential at which the channel begins to appear is called the “threshold voltage,” V_{TH} , and falls in the range of 300 mV to 500 mV. Note that the electrons are readily provided by the n⁺ source and drain regions, and need not be supplied by the substrate.

It is interesting to recognize that the gate terminal of the MOSFET draws no (low-frequency) current. Resting on top of the oxide, the gate remains insulated from other terminals and simply operates as a plate of a capacitor.

MOSFET as a Variable Resistor The conductive channel between S and D can be viewed as a resistor. Furthermore, since the density of electrons in the channel must increase as V_G becomes more positive (why?), the value of this resistor *changes* with the gate voltage. Conceptually illustrated in Fig. 6.6, such a voltage-dependent resistor proves extremely useful in analog and digital circuits.

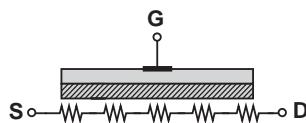


Figure 6.6 MOSFET viewed as a voltage-dependent resistor.

**Example
6.1**

In the vicinity of a wireless base station, the signal received by a cellphone may become very strong, possibly “saturating” the circuits and prohibiting proper operation. Devise a variable-gain circuit that lowers the signal level as the cellphone approaches the base station.

Solution A MOSFET can form a voltage-controlled attenuator along with a resistor as shown in Fig. 6.7.

Since

$$\frac{v_{out}}{v_{in}} = \frac{R_1}{R_M + R_1}, \quad (6.1)$$

the output signal becomes smaller as V_{cont} falls because the density of electrons in the channel decreases and R_M rises. MOSFETs are commonly utilized as voltage-dependent resistors in “variable-gain amplifiers.”

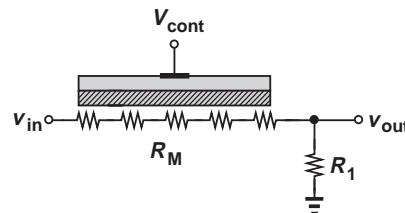


Figure 6.7 Use of MOSFET to adjust signal levels.

Exercise What happens to R_M if the channel length is doubled?

In the arrangement of Fig. 6.5(c), no current flows between S and D because the two terminals are at the same potential. We now raise the drain voltage as shown in Fig. 6.8(a) and examine the drain current (= source current). If $V_G < V_{TH}$, no channel exists, the device is off, and $I_D = 0$ regardless of the value of V_D . On the other hand, if $V_G > V_{TH}$, then $I_D > 0$ [Fig. 6.8(b)]. In fact, the source-drain path may act as a simple resistor, yielding the I_D - V_D characteristic shown in Fig. 6.8(c). The slope of the characteristic is equal to $1/R_{on}$, where R_{on} denotes the “on-resistance” of the transistor.⁵

Our brief treatment of the MOS I-V characteristics thus far points to two different views of the operation: in Fig. 6.8(b), V_G is varied while V_D remains constant whereas in Fig. 6.8(c), V_D is varied while V_G remains constant. Each view provides valuable insight into the operation of the transistor.

How does the characteristic of Fig. 6.8(b) change if V_G increases? The higher density of electrons in the channel lowers the on-resistance, yielding a *greater* slope. Depicted in Fig. 6.8(d), the resulting characteristics strengthen the notion of voltage-dependent resistance.

⁵The term “on-resistance” always refers to that between the source and drain, as no resistance exists between the gate and other terminals.

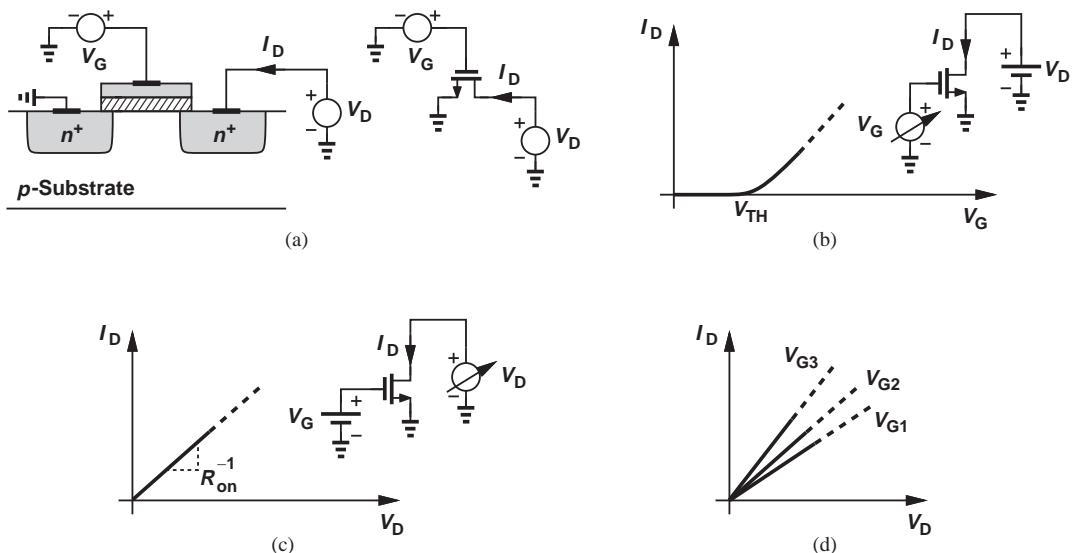


Figure 6.8 (a) MOSFET with gate and drain voltages, (b) I_D - V_G characteristic, (c) I_D - V_D characteristic, (d) I_D - V_D characteristics for various gate voltages.

Recall from Chapter 2 that charge flow in semiconductors occurs by diffusion or drift. How about the transport mechanism in a MOSFET? Since the voltage source tied to the drain creates an electric field along the channel, the current results from the *drift* of charge.

The I_D - V_G and I_D - V_D characteristics shown in Figs. 6.8(b) and (c), respectively, play a central role in our understanding of MOS devices. The following example reinforces the concepts studied thus far.

Example 6.2

Sketch the I_D - V_G and I_D - V_D characteristics for (a) different channel lengths, and (b) different oxide thicknesses.

Solution

As the channel length increases, so does the on-resistance.⁶ Thus, for $V_G > V_{TH}$, the drain current begins with lesser values as the channel length increases [Fig. 6.9(a)]. Similarly, I_D exhibits a smaller slope as a function of V_D [Fig. 6.9(b)]. It is therefore desirable to *minimize* the channel length so as to achieve large drain currents—an important trend in the MOS technology development.

How does the oxide thickness, t_{ox} , affect the I-V characteristics? As t_{ox} increases, the capacitance between the gate and the silicon substrate *decreases*. Thus, from $Q = CV$, we note that a given voltage results in *less* charge on the gate and hence a lower electron density in the channel. Consequently, the device suffers from a *higher* on-resistance, producing less drain current for a given gate voltage [Fig. 6.9(c)] or drain voltage [Fig. 6.9(d)]. For this reason, the semiconductor industry has continued to reduce the gate oxide thickness.

⁶Recall that the resistance of a conductor is proportional to the length.

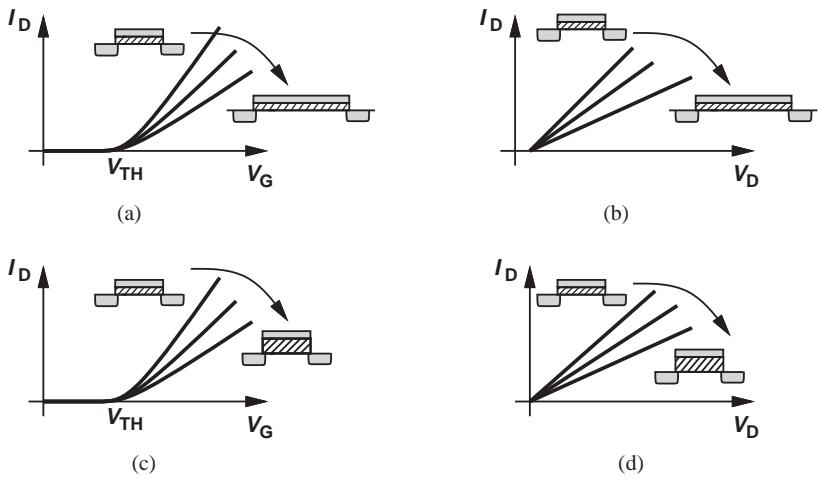


Figure 6.9 (a) I_D - V_G characteristics for different channel lengths, (b) I_D - V_D characteristics for different channel lengths, (c) I_D - V_G characteristics for different oxide thicknesses, (d) I_D - V_D characteristics for different oxide thicknesses.

Exercise The current conduction in the channel is in the form of drift. If the mobility falls at high temperatures, what can we say about the on-resistance as the temperature goes up?

While both the length and the oxide thickness affect the performance of MOSFETs, only the former is under the circuit designer's control, i.e., it can be specified in the "layout" of the transistor. The latter, on the other hand, is defined during fabrication and remains constant for all transistors in a given generation of the technology.

Another MOS parameter controlled by circuit designers is the *width* of the transistor, the dimension perpendicular to the length [Fig. 6.10(a)]. We therefore observe that

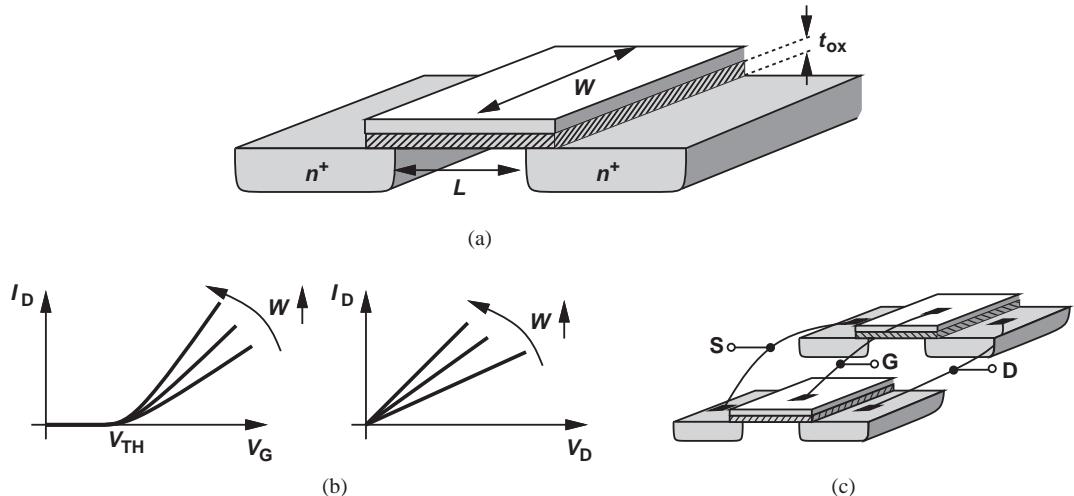


Figure 6.10 (a) Dimensions of a MOSFET (W and L are under circuit designer's control), (b) I_D characteristics for different values of W , (c) equivalence to devices in parallel.

“lateral” dimensions such as L and W can be chosen by circuit designers whereas “vertical” dimensions such as t_{ox} cannot.

How does the gate width impact the I-V characteristics? As W increases, so does the width of the channel, thus *lowering* the resistance between the source and the drain⁷ and yielding the trends depicted in Fig. 6.10(b). From another perspective, a wider device can be viewed as two narrower transistors *in parallel*, producing a high drain current [Fig. 6.10(c)]. We may then surmise that W must be maximized, but we must also note that the total gate capacitance increases with W , possibly limiting the speed of the circuit. Thus, the width of each device in the circuit must be chosen carefully.

Channel Pinch-Off Our qualitative study of the MOSFET thus far implies that the device acts as a voltage-dependent resistor if the gate voltage exceeds V_{TH} . In reality, however, the transistor operates as a *current source* if the drain voltage is sufficiently positive. To understand this effect, we make two observations: (1) to form a channel, the potential difference between the gate and the oxide-silicon interface must exceed V_{TH} ; (2) if the drain voltage remains higher than the source voltage, then the voltage at each point along the channel with respect to ground increases as we go from the source towards the drain. Illustrated in Fig. 6.11(a), this effect arises from the gradual voltage drop along the channel resistance. Since the gate voltage is constant (because the gate is conductive but carries no current in any direction), and since the potential at the oxide-silicon interface rises from the source to the drain, the potential difference *between* the gate and the oxide-silicon interface *decreases* along the x -axis [Fig. 6.11(b)]. The density of electrons in the channel follows the same trend, falling to a minimum at $x = L$.

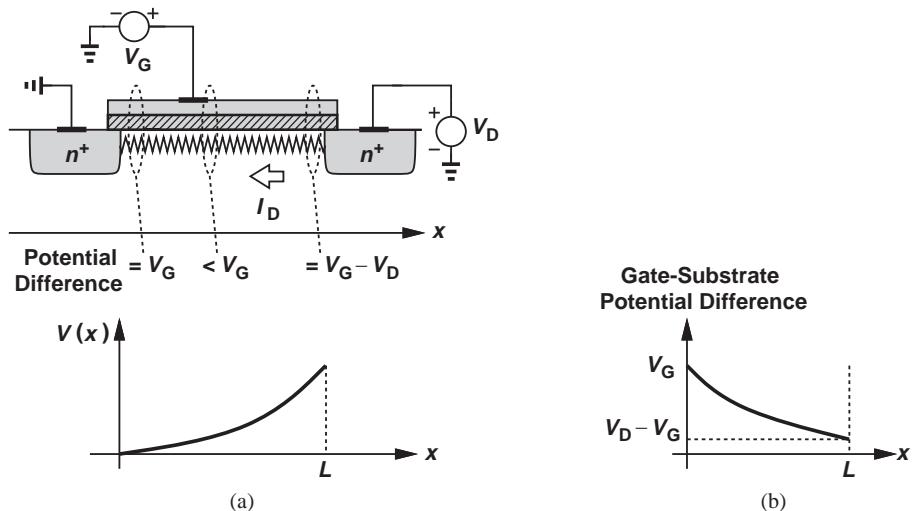
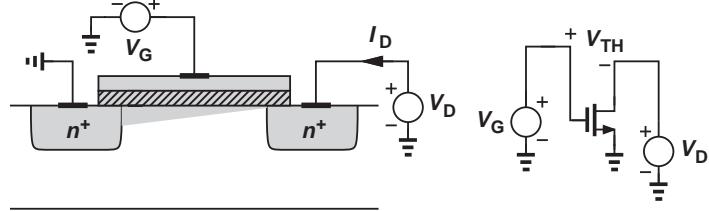
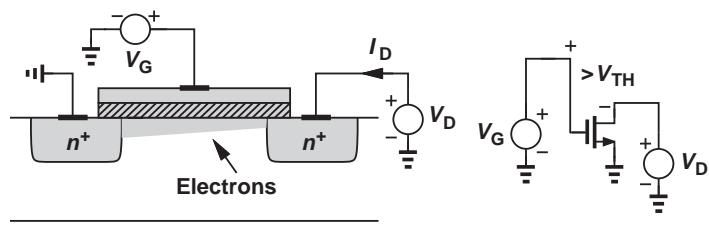
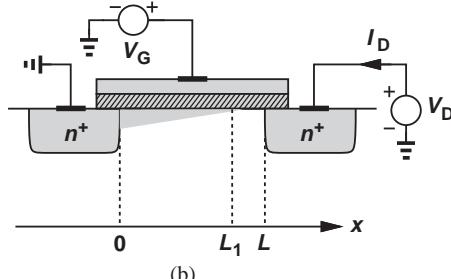


Figure 6.11 (a) Channel potential variation, (b) gate-substrate voltage difference along the channel.

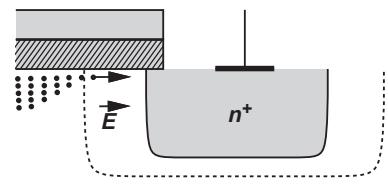
⁷Recall that the resistance of a conductor is inversely proportional to the cross section area, which itself is equal to the product of the width and thickness of the conductor.



(a)



(b)



(c)

Figure 6.12 (a) Pinchoff, (b) variation of length with drain voltage, (c) detailed operation near the drain.

From these observations, we conclude that, if the drain voltage is high enough to produce $V_G - V_D \leq V_{TH}$, then the channel ceases to exist near the drain. We say the gate-substrate potential difference is not sufficient at $x = L$ to attract electrons and the channel is “pinched off” [Fig. 6.12(a)].

What happens if V_D rises even higher than $V_G - V_{TH}$? Since $V(x)$ now goes from 0 at $x = 0$ to $V_D > V_G - V_{TH}$ at $x = L$, the voltage difference between the gate and the substrate falls to V_{TH} at some point $L_1 < L$ [Fig. 6.12(b)]. The device therefore contains no channel between L_1 and L . Does this mean the transistor cannot conduct current? No, the device still conducts: as illustrated in Fig. 6.12(c), once the electrons reach the end of the channel, they experience the high electric field in the depletion region surrounding the drain junction and are rapidly swept to the drain terminal. Nonetheless, as shown in the next section, the drain voltage no longer affects the current significantly, and the MOSFET acts as a constant current source—similar to a bipolar transistor in the forward active region. Note that the source-substrate and drain-substrate junctions carry no current.

6.2.2 Derivation of I-V Characteristics

With the foregoing qualitative study, we can now formulate the behavior of MOSFETs in terms of their terminal voltages.

Channel Charge Density Our derivations require an expression for the channel charge (i.e., free electrons) per unit *length*, also called the “charge density.” From $Q = CV$, we note

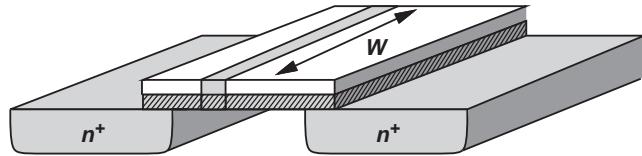


Figure 6.13 Illustration of capacitance per unit length.

that if C is the gate capacitance per unit length and V the voltage difference between the gate and the channel, then Q is the desired charge density. Denoting the gate capacitance per unit *area* by C_{ox} (expressed in F/m^2 or $\text{fF}/\mu\text{m}^2$), we write $C = WC_{ox}$ to account for the width of the transistor (Fig. 6.13). Moreover, we have $V = V_{GS} - V_{TH}$ because no mobile charge exists for $V_{GS} < V_{TH}$. (Hereafter, we denote both the gate and drain voltages with respect to the source.) It follows that

$$Q = WC_{ox}(V_{GS} - V_{TH}). \quad (6.2)$$

Note that Q is expressed in coulomb/meter. Now recall from Fig. 6.11(a) that the channel voltage varies along the length of the transistor, and the charge density falls as we go from the source to the drain. Thus, Eq. (6.2) is valid only near the source terminal, where the channel potential remains close to zero. As shown in Fig. 6.14, we denote the channel potential at x by $V(x)$ and write

$$Q(x) = WC_{ox}[V_{GS} - V(x) - V_{TH}], \quad (6.3)$$

noting that $V(x)$ goes from zero to V_D if the channel is not pinched off.

Drain Current What is the relationship between the mobile charge density and the current? Consider a bar of semiconductor having a uniform charge density (per unit length) equal to Q and carrying a current I (Fig. 6.15). Note from Chapter 2 that (1) I is given by the total charge that passes through the cross section of the bar in one second, and (2) if the carriers move with a velocity of v m/s, then the charge enclosed in v meters along the bar passes through the cross section in one second. Since the charge enclosed in v meters is equal to $Q \cdot v$, we have

$$I = Q \cdot v. \quad (6.4)$$

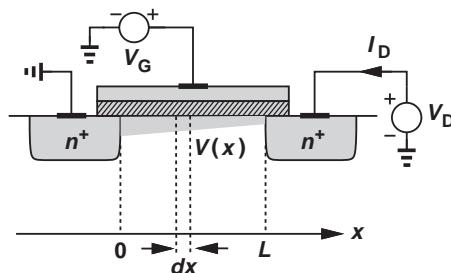


Figure 6.14 Device illustration for calculation of drain current.

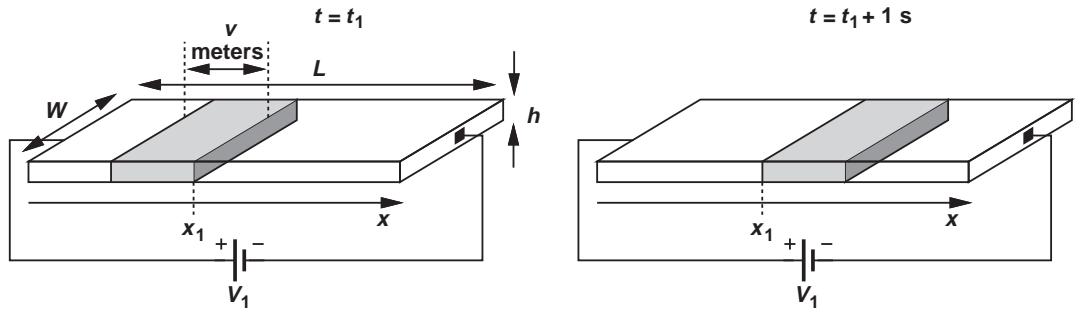


Figure 6.15 Relationship between charge velocity and current.

As explained in Chapter 2,

$$v = -\mu_n E, \quad (6.5)$$

$$= +\mu_n \frac{dV}{dx}, \quad (6.6)$$

where dV/dx denotes the derivative of the voltage at a given point. Combining Eqs. (6.3), (6.4), and (6.6), we obtain

$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}] \mu_n \frac{dV(x)}{dx}. \quad (6.7)$$

Interestingly, since I_D must remain constant along the channel (why?), $V(x)$ and dV/dx must vary such that the product of $V_{GS} - V(x) - V_{TH}$ and dV/dx is independent of x .

While it is possible to solve the above differential equation to obtain $V(x)$ in terms of I_D (and the reader is encouraged to do that), our immediate need is to find an expression for I_D in terms of the terminal voltages. To this end, we write

$$\int_{x=0}^{x=L} I_D dx = \int_{V(x)=0}^{V(x)=V_{DS}} \mu_n C_{ox} W [V_{GS} - V(x) - V_{TH}] dV. \quad (6.8)$$

That is,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2]. \quad (6.9)$$

We now examine this important equation from different perspectives to gain more insight. First, the linear dependence of I_D upon μ_n , C_{ox} , and W/L is to be expected: a higher mobility yields a greater current for a given drain-source voltage; a higher gate oxide capacitance leads to a larger electron density in the channel for a given gate-source voltage; and a larger W/L (called the device “aspect ratio”) is equivalent to placing more transistors in parallel [Fig. 6.10(c)]. Second, for a constant V_{GS} , I_D varies *parabolically* with V_{DS} (Fig. 6.16), reaching a maximum of

$$I_{D,max} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (6.10)$$

at $V_{DS} = V_{GS} - V_{TH}$. It is common to write W/L as the ratio of two values e.g., $5 \mu\text{m}/0.18 \mu\text{m}$ (rather than 27.8) to emphasize the choice of W and L . While only the

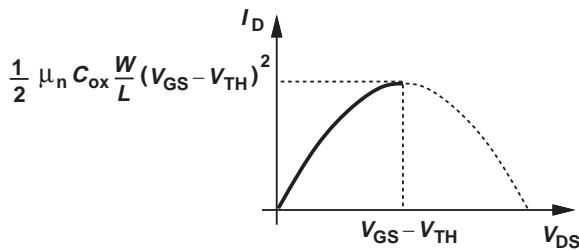


Figure 6.16 Parabolic I_D - V_{DS} characteristic.

ratio appears in many MOS equations, the individual values of W and L also become critical in most cases. For example, if both W and L are doubled, the ratio remains unchanged but the gate capacitance increases.

**Example
6.3**

Plot the I_D - V_{DS} characteristics for different values of V_{GS} .

Solution As V_{GS} increases, so do $I_{D,max}$ and $V_{GS} - V_{TH}$. Illustrated in Fig. 6.17, the characteristics exhibit maxima that follow a parabolic shape themselves because $I_{D,max} \propto (V_{GS} - V_{TH})^2$.

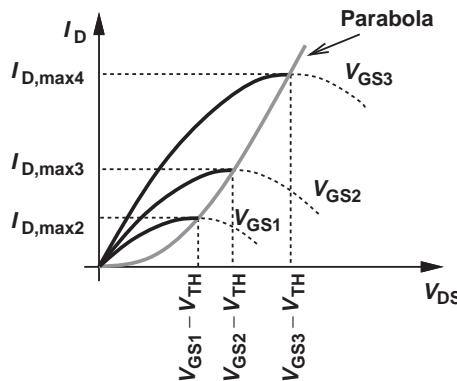


Figure 6.17 MOS characteristics for different gate-source voltages.

Exercise What happens to the above plots if t_{ox} is halved?

The nonlinear relationship between I_D and V_{DS} reveals that the transistor *cannot* generally be modeled as a simple linear resistor. However, if $V_{DS} \ll 2(V_{GS} - V_{TH})$, Eq. (6.9) reduces to:

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}, \quad (6.11)$$

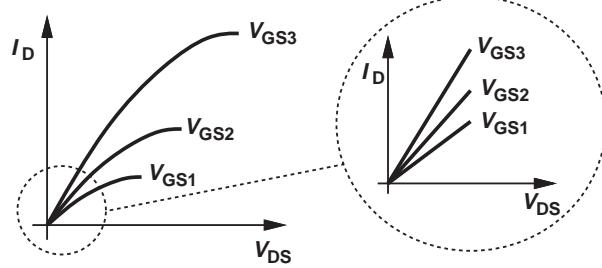


Figure 6.18 Detailed characteristics for small V_{DS} .

exhibiting a linear I_D - V_{DS} behavior for a given V_{GS} . In fact, the equivalent on-resistance is given by V_{DS}/I_D :

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}. \quad (6.12)$$

From another perspective, at small V_{DS} (near the origin), the parabolas in Fig. 6.17 can be approximated by straight lines having different slopes (Fig. 6.18).

As predicted in Section 6.2.1, Eq. (6.12) suggests that the on-resistance can be controlled by the gate-source voltage. In particular, for $V_{GS} = V_{TH}$, $R_{on} = \infty$, i.e., the device can operate as an electronic switch.

**Example
6.4**

A cordless telephone incorporates a single antenna for reception and transmission. Explain how the system must be configured.

Solution

The system is designed so that the phone receives for half of the time and transmits for the other half. Thus, the antenna is alternately connected to the receiver and the transmitter in regular intervals, e.g., every 20 ms (Fig. 6.19). An electronic antenna switch is therefore necessary here.⁸

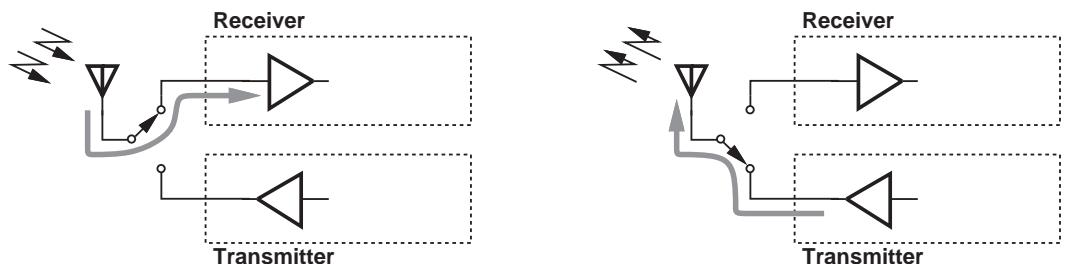


Figure 6.19 Role of antenna switch in a cordless phone.

Exercise

Some systems employ two antennas, each of which receives and transmits signals. How many switches are needed?

⁸Some cellphones operate in the same manner.

In most applications, it is desirable to achieve a low on-resistance for MOS switches. The circuit designer must therefore maximize W/L and V_{GS} . The following example illustrates this point.

**Example
6.5**

In the cordless phone of Example 6.4, the switch connecting the transmitter to the antenna must negligibly attenuate the signal, e.g., by no more than 10%. If $V_{DD} = 1.8$ V, $\mu_n C_{ox} = 100 \mu\text{A}/\text{V}^2$, and $V_{TH} = 0.4$ V, determine the minimum required aspect ratio of the switch. Assume the antenna can be modeled as a 50Ω resistor.

Solution As depicted in Fig. 6.20, we wish to ensure

$$\frac{V_{out}}{V_{in}} \geq 0.9 \quad (6.13)$$

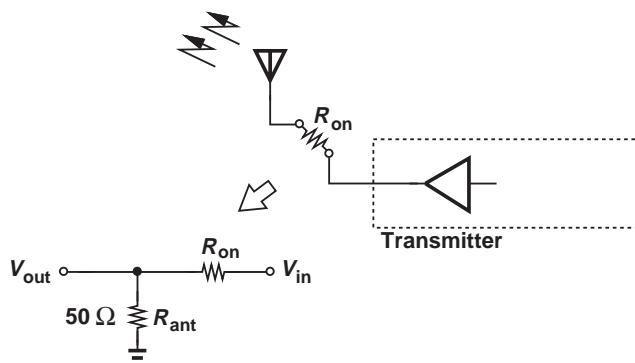


Figure 6.20 Signal degradation due to on-resistance of antenna switch.

and hence

$$R_{on} \leq 5.6 \Omega. \quad (6.14)$$

Setting V_{GS} to the maximum value, V_{DD} , we obtain from Eq. (6.12),

$$\frac{W}{L} \geq 1276. \quad (6.15)$$

(Since wide transistors introduce substantial capacitance in the signal path, this choice of W/L may still attenuate high-frequency signals.)

Exercise What W/L is necessary if V_{DD} drops to 1.2 V?

Triode and Saturation Regions Equation (6.9) expresses the drain current in terms of the device terminal voltages, implying that the current begins to fall for $V_{DS} > V_{GS} - V_{TH}$. We say the device operates in the “triode region” (also called the “linear region”) if $V_{DS} < V_{GS} - V_{TH}$ (the rising section of the parabola). We also use the term “deep triode region” for $V_{DS} \ll 2(V_{GS} - V_{TH})$, where the transistor operates as a resistor.

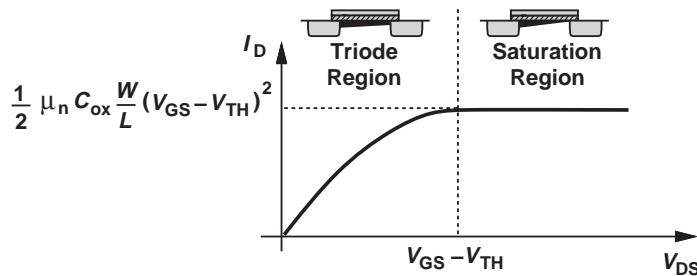


Figure 6.21 Overall MOS characteristic.

In reality, the drain current reaches “saturation,” that is, becomes *constant* for $V_{DS} > V_{GS} - V_{TH}$ (Fig. 6.21). To understand why, recall from Fig. 6.12 that the channel experiences pinch-off if $V_{DS} = V_{GS} - V_{TH}$. Thus, further increase in V_{DS} simply shifts the pinch-off point slightly toward the drain. Also, recall that Eqs. (6.7) and (6.8) are valid only where channel charge exists. It follows that the integration in Eq. (6.8) must encompass only the channel, i.e., from $x = 0$ to $x = L_1$ in Fig. 6.12(b), and be modified to

$$\int_{x=0}^{x=L_1} I_D dx = \int_{V(x)=0}^{V(x)=V_{GS}-V_{TH}} \mu_n C_{ox} W [V_{GS} - V(x) - V_{TH}] dV. \quad (6.16)$$

Note that the upper limits correspond to the channel pinch-off point. In particular, the integral on the right-hand side is evaluated up to $V_{GS} - V_{TH}$ rather than V_{DS} . Consequently,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L_1} (V_{GS} - V_{TH})^2, \quad (6.17)$$

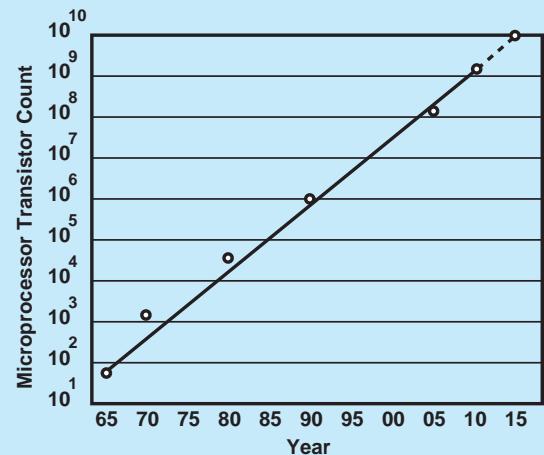
a result independent of V_{DS} and identical to $I_{D,max}$ in Eq. (6.10) if we assume $L_1 \approx L$. Called the “overdrive voltage,” the quantity $V_{GS} - V_{TH}$ plays a key role in MOS circuits. MOSFETs are sometimes called “square-law” devices to emphasize the relationship between I_D and the overdrive. For the sake of brevity, we hereafter denote L_1 with L .

The I-V characteristic of Fig. 6.21 resembles that of bipolar devices, with the triode and saturation regions in MOSFETs appearing similar to saturation and forward active regions in bipolar transistors, respectively. It is unfortunate that the term “saturation” refers to completely different regions in MOS and bipolar I-V characteristics.

We employ the conceptual illustration in Fig. 6.22 to determine the region of operation. Note that the gate-drain potential difference suits this purpose and we need not compute the gate-source and gate-drain voltages separately.

Did you know?

The explosive growth of MOS technology is attributed to two factors: the ability to shrink the dimensions of the MOS device (W , L , t_{ox} , etc.) and the ability to integrate a greater number of MOS devices on a chip each year. The latter trend was predicted by one of Intel’s founders, Gordon Moore, in 1965. He observed that the number of transistors per chip doubled every two years. Indeed, starting with 50 devices per chip in 1965, we now have reached tens of billions on memory chips and several billion on microprocessor chips. Can you think of any other product in human history that has grown so much so fast (except for Bill Gates’ wealth)?



Moore’s Law: transistor count per chip throughout the years.

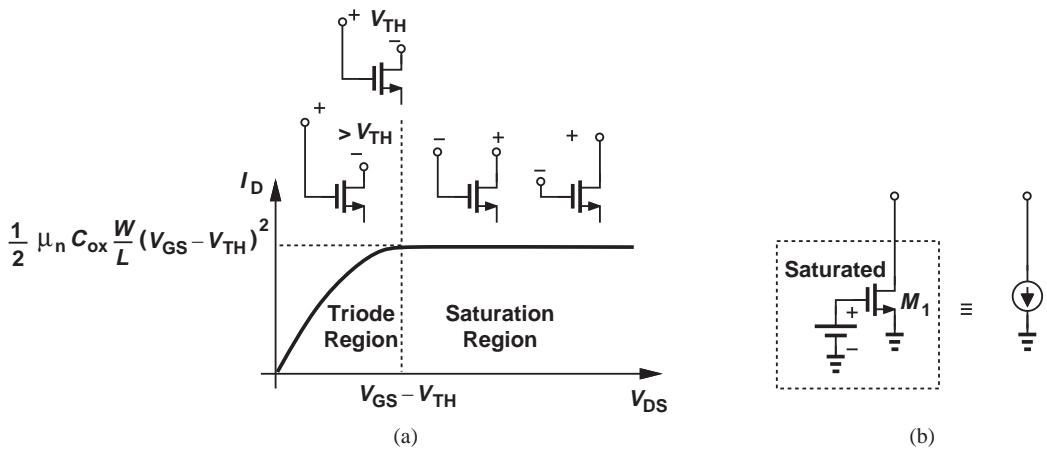


Figure 6.22 Illustration of triode and saturation regions based on the gate and drain voltages.

Exhibiting a “flat” current in the saturation region, a MOSFET can operate as a current source having a value given by Eq. (6.17). Furthermore, the square-law dependence of I_D upon $V_{GS} - V_{TH}$ suggests that the device can act as a voltage-controlled current source.

**Example
6.6**

Calculate the bias current of M_1 in Fig. 6.23. Assume $\mu_n C_{ox} = 100 \mu\text{A/V}^2$ and $V_{TH} = 0.4 \text{ V}$. If the gate voltage increases by 10 mV, what is the change in the drain voltage?

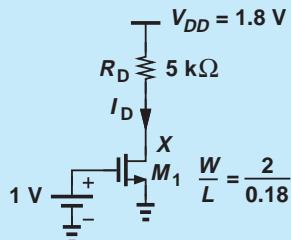


Figure 6.23 Simple MOS circuit.

Solution It is unclear a priori in which region M_1 operates. Let us assume M_1 is saturated and proceed. Since $V_{GS} = 1 \text{ V}$,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (6.18)$$

$$= 200 \mu\text{A}. \quad (6.19)$$

We must check our assumption by calculating the drain potential:

$$V_X = V_{DD} - R_D I_D \quad (6.20)$$

$$= 0.8 \text{ V}. \quad (6.21)$$

The drain voltage is lower than the gate voltage, but by less than V_{TH} . The illustration in Fig. 6.22 therefore indicates that M_1 indeed operates in saturation.

If the gate voltage increases to 1.01 V, then

$$I_D = 206.7 \mu\text{A}, \quad (6.22)$$

lowering V_X to

$$V_X = 0.766 \text{ V.} \quad (6.23)$$

Fortunately, M_1 is still saturated. The 34-mV change in V_X reveals that the circuit can *amplify* the input.

Exercise What choice of R_D places the transistor at the edge of the triode region?

It is instructive to identify several points of contrast between bipolar and MOS devices. (1) A bipolar transistor with $V_{BE} = V_{CE}$ resides at the edge of the active region whereas a MOSFET approaches the edge of saturation if its drain voltage falls below its gate voltage by V_{TH} . (2) Bipolar devices exhibit an exponential I_C - V_{BE} characteristic while MOSFETs display a square-law dependence. That is, the former provide a greater transconductance than the latter (for a given bias current). (3) In bipolar circuits, most transistors have the same dimensions and hence the same I_S , whereas in MOS circuits, the aspect ratio of each device may be chosen differently to satisfy the design requirements. (4) The gate of MOSFETs draws no bias current.⁹

**Example
6.7**

Determine the value of W/L in Fig. 6.23 that places M_1 at the edge of saturation and calculate the drain voltage change for a 1-mV change at the gate. Assume $V_{TH} = 0.4 \text{ V}$.

Solution With $V_{GS} = +1 \text{ V}$, the drain voltage must fall to $V_{GS} - V_{TH} = 0.6 \text{ V}$ for M_1 to enter the triode region. That is,

$$I_D = \frac{V_{DD} - V_{DS}}{R_D} \quad (6.24)$$

$$= 240 \mu\text{A}. \quad (6.25)$$

Since I_D scales linearly with W/L ,

$$\left. \frac{W}{L} \right|_{max} = \frac{240 \mu\text{A}}{200 \mu\text{A}} \cdot \frac{2}{0.18} \quad (6.26)$$

$$= \frac{2.4}{0.18}. \quad (6.27)$$

If V_{GS} increases by 1 mV,

$$I_D = 248.04 \mu\text{A}, \quad (6.28)$$

changing V_X by

$$\Delta V_X = \Delta I_D \cdot R_D \quad (6.29)$$

$$= 4.02 \text{ mV}. \quad (6.30)$$

The voltage gain is thus equal to 4.02 in this case.

Exercise Repeat the above example if R_D is doubled.

⁹New generations of MOSFETs suffer from gate “leakage” current, but we neglect this effect here.

**Example
6.8**

Calculate the maximum allowable gate voltage in Fig. 6.24 if M_1 must remain saturated.

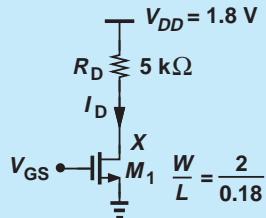


Figure 6.24 Simple MOS circuit.

Solution At the edge of saturation, $V_{GS} - V_{TH} = V_{DS} = V_{DD} - R_D I_D$. Substituting for I_D from Eq. (6.17) gives

$$V_{GS} - V_{TH} = V_{DD} - \frac{R_D}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2, \quad (6.31)$$

and hence

$$V_{GS} - V_{TH} = \frac{-1 + \sqrt{1 + 2R_D V_{DD} \mu_n C_{ox} \frac{W}{L}}}{R_D \mu_n C_{ox} \frac{W}{L}}. \quad (6.32)$$

Thus,

$$V_{GS} = \frac{-1 + \sqrt{1 + 2R_D V_{DD} \mu_n C_{ox} \frac{W}{L}}}{R_D \mu_n C_{ox} \frac{W}{L}} + V_{TH}. \quad (6.33)$$

Exercise Calculate the value of V_{GS} if $\mu_n C_{ox} = 100 \mu\text{A/V}^2$ and $V_{TH} = 0.4$.

6.2.3 Channel-Length Modulation

In our study of the pinch-off effect, we observed that the point at which the channel vanishes in fact moves toward the source as the drain voltage increases. In other words, the value of L_1 in Fig. 6.12(b) varies with V_{DS} to some extent. Called “channel-length modulation” and illustrated in Fig. 6.25, this phenomenon yields a larger drain current as V_{DS} increases because $I_D \propto 1/L_1$ in Eq. (6.17). Similar to the Early effect in bipolar devices,

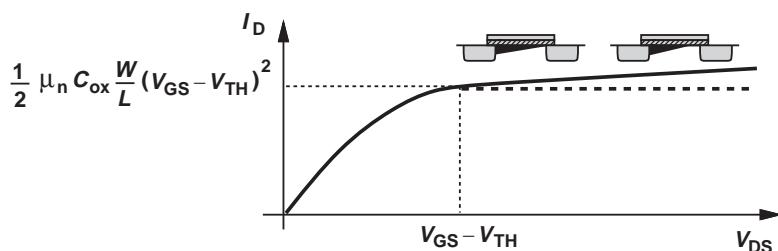


Figure 6.25 Variation of I_D in saturation region.

channel-length modulation results in a finite output impedance given by the inverse of the I_D - V_{DS} slope in Fig. 6.25.

To account for channel-length modulation, we assume L is constant, but multiply the right-hand side of Eq. (6.17) by a corrective term:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}), \quad (6.34)$$

where λ is called the “channel-length modulation coefficient.” While only an approximation, this linear dependence of I_D upon V_{DS} still provides a great deal of insight into the circuit design implications of channel-length modulation.

Unlike the Early effect in bipolar devices (Chapter 4), the amount of channel-length modulation is under the circuit designer’s control. This is because λ is inversely proportional to L : for a longer channel, the *relative* change in L (and hence in I_D) for a given change in V_{DS} is smaller (Fig. 6.26).¹⁰ (By contrast, the base width of bipolar devices cannot be adjusted by the circuit designer, yielding a constant Early voltage for all transistors in a given technology.)

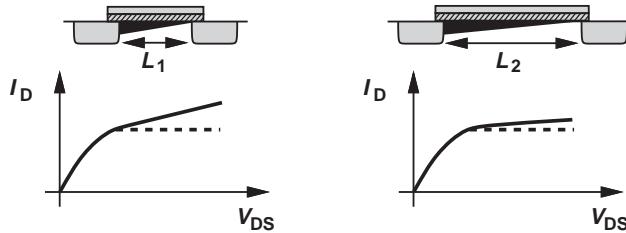


Figure 6.26 Channel-length modulation.

**Example
6.9**

A MOSFET carries a drain current of 1 mA with $V_{DS} = 0.5$ V in saturation. Determine the change in I_D if V_{DS} rises to 1 V and $\lambda = 0.1$ V $^{-1}$. What is the device output impedance?

Solution We write

$$I_{D1} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS1}) \quad (6.35)$$

$$I_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS2}) \quad (6.36)$$

and hence

$$I_{D2} = I_{D1} \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}. \quad (6.37)$$

With $I_{D1} = 1$ mA, $V_{DS1} = 0.5$ V, $V_{DS2} = 1$ V, and $\lambda = 0.1$ V $^{-1}$,

$$I_{D2} = 1.048 \text{ mA}. \quad (6.38)$$

¹⁰Since different MOSFETs in a circuit may be sized for different λ ’s, we do not define a quantity similar to the Early voltage here.

The change in I_D is therefore equal to $48 \mu\text{A}$, yielding an output impedance of

$$r_O = \frac{\Delta V_{DS}}{\Delta I_D} \quad (6.39)$$

$$= 10.42 \text{ k}\Omega. \quad (6.40)$$

Exercise Does W affect the above results?

The above example reveals that channel-length modulation limits the output impedance of MOS current sources. The same effect was observed for bipolar current sources in Chapters 4 and 5.

**Example
6.10**

Assuming $\lambda \propto 1/L$, calculate ΔI_D and r_O in Example 6.9 if both W and L are doubled.

Solution In Eqs. (6.35) and (6.36), W/L remains unchanged but λ drops to 0.05 V^{-1} . Thus,

$$I_{D2} = I_{D1} \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} \quad (6.41)$$

$$= 1.024 \text{ mA}. \quad (6.42)$$

That is, $\Delta I_D = 24 \mu\text{A}$ and

$$r_O = 20.84 \text{ k}\Omega. \quad (6.43)$$

Exercise What output impedance is achieved if W and L are quadrupled and I_D is halved?

6.2.4 MOS Transconductance

As a voltage-controlled current source, a MOS transistor can be characterized by its transconductance:

$$g_m = \frac{\partial I_D}{\partial V_{GS}}. \quad (6.44)$$

This quantity serves as a measure of the “strength” of the device: a higher value corresponds to a greater change in the drain current for a given change in V_{GS} . Using Eq. (6.17) for the saturation region, we have

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}), \quad (6.45)$$

concluding that (1) g_m is linearly proportional to W/L for a given $V_{GS} - V_{TH}$, and (2) g_m is linearly proportional to $V_{GS} - V_{TH}$ for a given W/L . Also, substituting for $V_{GS} - V_{TH}$ from Eq. (6.17), we obtain

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}. \quad (6.46)$$

TABLE 6.1 Various dependencies of g_m .

$\frac{W}{L}$ Constant $V_{GS} - V_{TH}$ Variable	$\frac{W}{L}$ Variable $V_{GS} - V_{TH}$ Constant	$\frac{W}{L}$ Variable $V_{GS} - V_{TH}$ Constant
$g_m \propto \sqrt{I_D}$	$g_m \propto I_D$	$g_m \propto \sqrt{\frac{W}{L}}$
$g_m \propto V_{GS} - V_{TH}$	$g_m \propto \frac{W}{L}$	$g_m \propto \frac{1}{V_{GS} - V_{TH}}$

That is, (1) g_m is proportional to $\sqrt{W/L}$ for a given I_D , and (2) g_m is proportional to $\sqrt{I_D}$ for a given W/L . Moreover, dividing Eq. (6.45) by (6.17) gives

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}}, \quad (6.47)$$

revealing that (1) g_m is linearly proportional to I_D for a given $V_{GS} - V_{TH}$, and (2) g_m is inversely proportional to $V_{GS} - V_{TH}$ for a given I_D . Summarized in Table 6.1, these dependencies prove critical in understanding performance trends of MOS devices and have no counterpart in bipolar transistors.¹¹ Among these three expressions for g_m , Eq. (6.46) is more frequently used because I_D may be predetermined by power dissipation requirements.

Example 6.11

For a MOSFET operating in saturation, how do g_m and $V_{GS} - V_{TH}$ change if both W/L and I_D are doubled?

Solution

Equation (6.46) indicates that g_m is also doubled. Moreover, Eq. (6.17) suggests that the overdrive remains constant. These results can be understood intuitively if we view the doubling of W/L and I_D as shown in Fig. 6.27. Indeed, if V_{GS} remains constant and the width of the device is doubled, it is as if two transistors carrying equal currents are placed in parallel, thereby doubling the transconductance. The reader can show that this trend applies to any type of transistor.

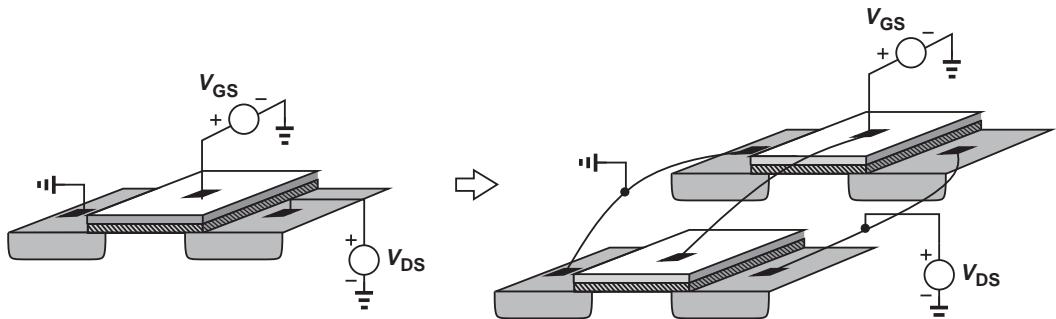


Figure 6.27 Equivalence of a wide MOSFET to two in parallel.

Exercise

How do g_m and $V_{GS} - V_{TH}$ change if only W and I_D are doubled?

¹¹There is some resemblance between the second column and the behavior of $g_m = I_C/V_T$. If the bipolar transistor width is increased while V_{BE} remains constant, then both I_C and g_m increase linearly.

6.2.5 Velocity Saturation*

Recall from Section 2.1.3 that at high electric fields, carrier mobility degrades, eventually leading to a *constant* velocity. Owing to their very short channels (e.g., $0.1\ \mu\text{m}$), modern MOS devices experience velocity saturation even with drain-source voltages as low as 1 V. As a result, the I/V characteristics no longer follow the square-law behavior.

Let us examine the derivations in Section 6.2.2 under velocity saturation conditions. Denoting the saturated velocity by v_{sat} , we have

$$I_D = v_{sat} \cdot Q \quad (6.48)$$

$$= v_{sat} \cdot WC_{ox}(V_{GS} - V_{TH}). \quad (6.49)$$

Interestingly, I_D now exhibits a *linear* dependence on $V_{GS} - V_{TH}$ and no dependence on L .¹² We also recognize that

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad (6.50)$$

$$= v_{sat} WC_{ox}, \quad (6.51)$$

a quantity independent of L and I_D .

6.2.6 Other Second-Order Effects

Body Effect In our study of MOSFETs, we have assumed that both the source and the substrate (also called the “bulk” or the “body”) are tied to ground. However, this condition need not hold in all circuits. For example, if the source terminal rises to a positive voltage while the substrate is at zero, then the source-substrate junction remains reverse-biased and the device still operates properly.

Figure 6.28 illustrates this case. The source terminal is tied to a potential V_S with respect to ground while the substrate is grounded through a p^+ contact.¹³ The dashed line added to the transistor symbol indicates the substrate terminal. We denote the voltage difference between the source and the substrate (the bulk) by V_{SB} .

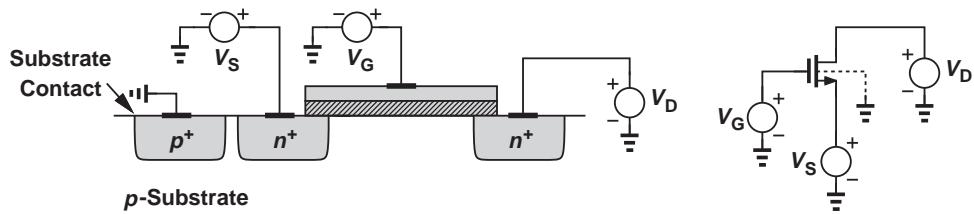


Figure 6.28 Body effect.

*This section can be skipped in a first reading.

¹²Of course, if L is increased substantially, while V_{DS} remains constant, then the device experiences less velocity saturation and Eq. (6.49) is not accurate.

¹³The p^+ island is necessary to achieve an “ohmic” contact with low resistance.

An interesting phenomenon occurs as the source-substrate potential difference departs from zero: the threshold voltage of the device *changes*. In particular, as the source becomes more positive with respect to the substrate, V_{TH} *increases*. Called “body effect,” this phenomenon is formulated as

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}), \quad (6.52)$$

where V_{TH0} denotes the threshold voltage with $V_{SB} = 0$ (as studied earlier), and γ and ϕ_F are technology-dependent parameters having typical values of $0.4\sqrt{V}$ and 0.4 V, respectively.

**Example
6.12**

In the circuit of Fig. 6.28, assume $V_S = 0.5$ V, $V_G = V_D = 1.4$ V, $\mu_nC_{ox} = 100 \mu\text{A/V}^2$, $W/L = 50$, and $V_{TH0} = 0.6$ V. Determine the drain current if $\lambda = 0$.

Solution

Since the source-body voltage, $V_{SB} = 0.5$ V, Eq. (6.52) and the typical values for γ and ϕ_F yield

$$V_{TH} = 0.698 \text{ V}. \quad (6.53)$$

Also, with $V_G = V_D$, the device operates in saturation (why?) and hence

$$I_D = \frac{1}{2}\mu_nC_{ox}\frac{W}{L}(V_G - V_S - V_{TH})^2 \quad (6.54)$$

$$= 102 \mu\text{A}. \quad (6.55)$$

Exercise Sketch the drain current as a function of V_S as V_S goes from zero to 1 V.

Body effect manifests itself in some analog and digital circuits and is studied in more advanced texts. We neglect body effect in this book.

Subthreshold Conduction The derivation of the MOS I-V characteristic has assumed that the transistor abruptly turns on as V_{GS} reaches V_{TH} . In reality, formation of the channel is a gradual effect, and the device conducts a small current even for $V_{GS} < V_{TH}$. Called “subthreshold conduction,” this effect has become a critical issue in modern MOS devices and is studied in more advanced texts.

6.3

MOS DEVICE MODELS

With our study of MOS I-V characteristics in the previous section, we now develop models that can be used in circuit analysis and design.

6.3.1 Large-Signal Model

For arbitrary voltage and current levels, we must resort to Eqs. (6.9) and (6.34) to express the device behavior:

$$I_D = \frac{1}{2}\mu_nC_{ox}\frac{W}{L}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] \quad \text{Triode Region} \quad (6.56)$$

$$I_D = \frac{1}{2}\mu_nC_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad \text{Saturation Region} \quad (6.57)$$

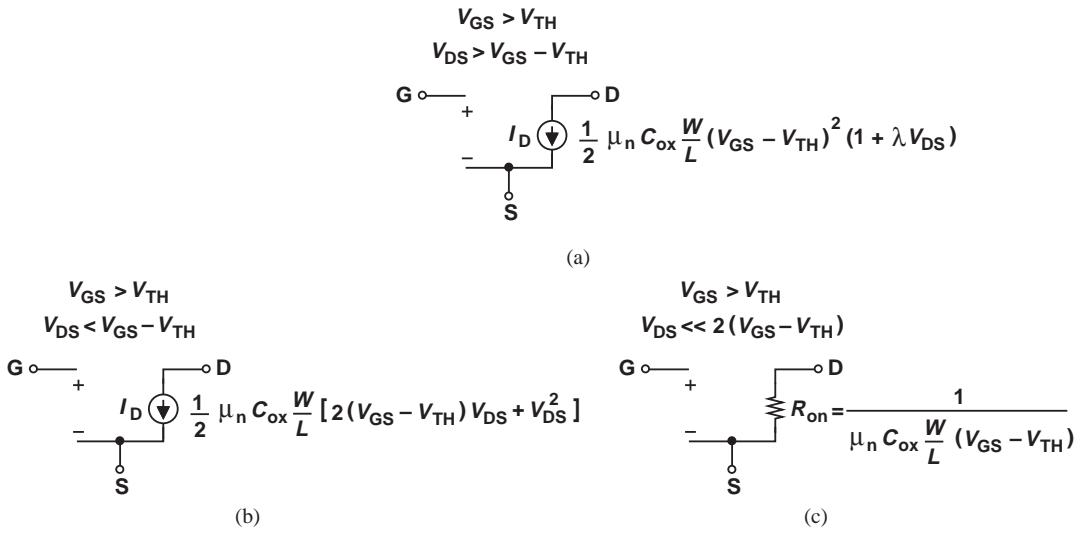


Figure 6.29 MOS models for (a) saturation region, (b) triode region, (c) deep triode region.

In the saturation region, the transistor acts as a voltage-controlled current source, lending itself to the model shown in Fig. 6.29(a). Note that I_D does depend on V_{DS} and is therefore not an ideal current source. For $V_{DS} < V_{GS} - V_{TH}$, the model must reflect the triode region, but it can still incorporate a voltage-controlled current source, as depicted in Fig. 6.29(b). Finally, if $V_{DS} \ll 2(V_{GS} - V_{TH})$, the transistor can be viewed as a voltage-controlled resistor [Fig. 6.29(c)]. In all three cases, the gate remains an open circuit to represent the zero gate current.

**Example
6.13**

Sketch the drain current of M_1 in Fig. 6.30(a) versus V_1 as V_1 varies from zero to V_{DD} . Assume $\lambda = 0$.

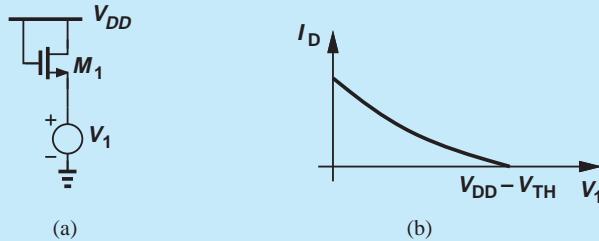


Figure 6.30 (a) Simple MOS circuit, (b) variation of I_D with V_1 .

Solution Noting that the device operates in saturation (why?), we write

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (6.58)$$

$$= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{DD} - V_1 - V_{TH})^2. \quad (6.59)$$

At $V_1 = 0$, $V_{GS} = V_{DD}$ and the device carries maximum current. As V_1 rises, V_{GS} falls and so does I_D . If V_1 reaches $V_{DD} - V_{TH}$, V_{GS} drops to V_{TH} , turning the transistor off. The drain current thus varies as illustrated in Fig. 6.30(b). Note that, owing to body effect, V_{TH} varies with V_1 if the substrate is tied to ground.

Exercise Repeat the above example if the gate of M_1 is tied to a voltage equal to 1.5 V and $V_{DD} = 2$ V.

6.3.2 Small-Signal Model

If the bias currents and voltages of a MOSFET are only slightly disturbed by signals, the nonlinear, large-signal models can be reduced to linear, small-signal representations. The development of the model proceeds in a manner similar to that in Chapter 4 for bipolar devices. Of particular interest to us in this book is the small-signal model for the saturation region.

Viewing the transistor as a voltage-controlled current source, we draw the basic model as in Fig. 6.31(a), where $i_D = g_m v_{GS}$ and the gate remains open. To represent channel-length modulation, i.e., variation of i_D with v_{DS} , we add a resistor as in Fig. 6.31(b):

$$r_O = \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1} \quad (6.60)$$

$$= \frac{1}{\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \cdot \lambda}. \quad (6.61)$$

Since channel-length modulation is relatively small, the denominator of Eq. (6.61) can be approximated as $I_D \cdot \lambda$, yielding

$$r_O \approx \frac{1}{\lambda I_D}. \quad (6.62)$$

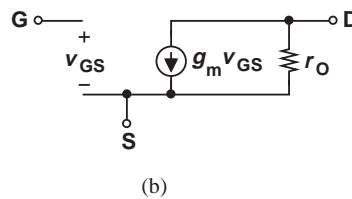
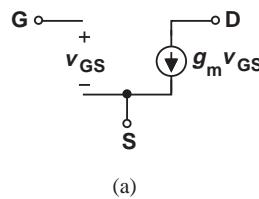
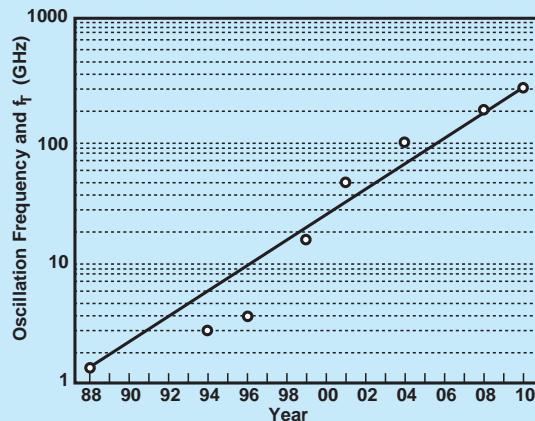


Figure 6.31 (a) Small-signal model of MOSFET, (b) inclusion of channel-length modulation.

Did you know?

In addition to integrating a larger number of transistors per chip, MOS technology has also benefited tremendously from “scaling,” i.e., the reduction of the transistors’ dimensions. The minimum channel length has fallen from about 10 μm to about 25 nm today and the speed of MOSFETs has improved by more than 4 orders of magnitude. For example, the clock frequency of Intel’s microprocessors has risen from 100 kHz to 4 GHz. But have analog circuits taken advantage of the scaling as well? Yes, indeed. Plotted below is the frequency of MOS oscillators as a function of time over the past three decades.



MOS oscillator frequency as a function of time.

**Example
6.14**

A MOSFET is biased at a drain current of 0.5 mA. If $\mu_n C_{ox} = 100 \mu\text{A/V}^2$, $W/L = 10$, and $\lambda = 0.1 \text{ V}^{-1}$, calculate its small-signal parameters.

Solution We have

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \quad (6.63)$$

$$= \frac{1}{1 \text{ k}\Omega}. \quad (6.64)$$

Also,

$$r_O = \frac{1}{\lambda I_D} \quad (6.65)$$

$$= 20 \text{ k}\Omega. \quad (6.66)$$

This means that the intrinsic gain, $g_m r_O$ (Chapter 4), is equal to 20 for this choice of device dimensions and bias current.

Exercise Repeat the above example if W/L is doubled.

6.4

PMOS TRANSISTOR

Having seen both *npn* and *pnp* bipolar transistors, the reader may wonder if a *p*-type counterpart exists for MOSFETs. Indeed, as illustrated in Fig. 6.32(a), changing the doping polarities of the substrate and the S/D areas results in a “PMOS” device. The channel now consists of *holes* and is formed if the gate voltage is *below* the source potential by one threshold voltage. That is, to turn the device on, $V_{GS} < V_{TH}$, where V_{TH} itself is negative. Following the conventions used for bipolar devices, we draw the PMOS device as in Fig. 6.32(b), with the source terminal identified by the arrow and placed

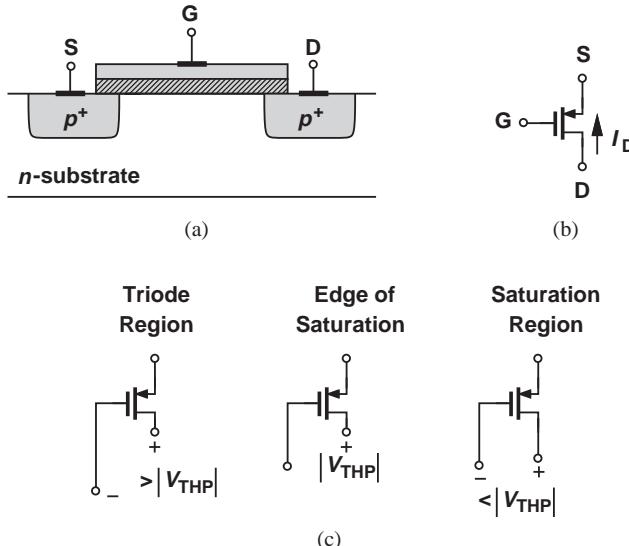


Figure 6.32 (a) Structure of PMOS device, (b) PMOS circuit symbol, (c) illustration of triode and saturation regions based on gate voltages.

on top to emphasize its higher potential. The transistor operates in the triode region if the drain voltage is near the source potential, approaching saturation as V_D falls to $V_G - V_{TH} = V_G + |V_{TH}|$. Figure 6.32(c) conceptually illustrates the gate-drain voltages required for each region of operation. We say that if V_{DS} of a PMOS (NMOS) device is sufficiently negative (positive), then it is in saturation.

**Example
6.15**

In the circuit of Fig. 6.33, determine the region of operation of M_1 as V_1 goes from V_{DD} to zero. Assume $V_{DD} = 2.5$ V and $|V_{TH}| = 0.5$ V.

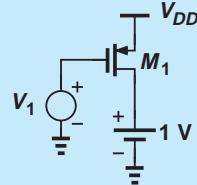


Figure 6.33 Simple PMOS circuit.

Solution For $V_1 = V_{DD}$, $V_{GS} = 0$ and M_1 is off. As V_1 falls and approaches $V_{DD} - |V_{TH}|$, the gate-source potential is negative enough to form a channel of holes, turning the device on. At this point, $V_G = V_{DD} - |V_{TH}| = +2$ V while $V_D = +1$ V; i.e., M_1 is saturated [Fig. 6.32(c)]. As V_1 falls further, V_{GS} becomes more negative and the transistor current rises. For $V_1 = +1$ V $- |V_{TH}| = 0.5$ V, M_1 is at the edge of the triode region. As V_1 goes below 0.5 V, the transistor enters the triode region further.

The voltage and current polarities in PMOS devices can prove confusing. Using the current direction shown in Fig. 6.32(b), we express I_D in the saturation region as

$$I_{D,sat} = -\frac{1}{2}\mu_p C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 - \lambda V_{DS}), \quad (6.67)$$

where λ is multiplied by a negative sign.¹⁴ In the triode region,

$$I_{D,tri} = -\frac{1}{2}\mu_p C_{ox} \frac{W}{L} [2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2]. \quad (6.68)$$

Alternatively, both equations can be expressed in terms of absolute values:

$$|I_{D,sat}| = \frac{1}{2}\mu_p C_{ox} \frac{W}{L} (|V_{GS}| - |V_{TH}|)^2 (1 + \lambda |V_{DS}|) \quad (6.69)$$

$$|I_{D,tri}| = \frac{1}{2}\mu_p C_{ox} \frac{W}{L} [2(|V_{GS}| - |V_{TH}|)|V_{DS}| - V_{DS}^2]. \quad (6.70)$$

The small-signal model of PMOS transistor is identical to that of NMOS devices (Fig. 6.31). The following example illustrates this point.

¹⁴To make this equation more consistent with that of NMOS devices [Eq. (6.34)], we can define λ itself to be negative and express I_D as $(1/2)\mu_p C_{ox}(W/L)(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$. But a negative λ carries little physical meaning.

**Example
6.16**

For the configurations shown in Fig. 6.34(a), determine the small-signal resistances R_X and R_Y . Assume $\lambda \neq 0$.

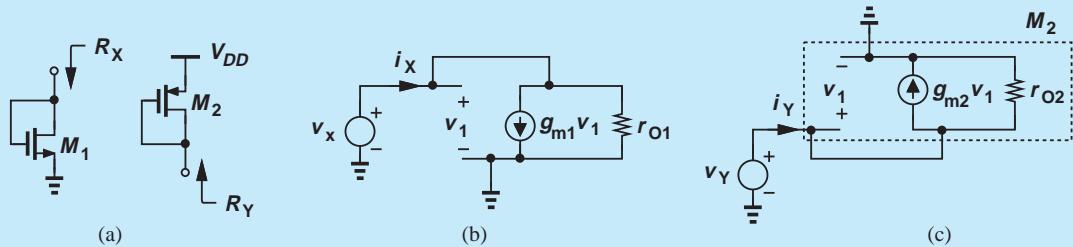


Figure 6.34 (a) Diode-connected NMOS and PMOS devices, (b) small-signal model of (a), (c) small-signal model of (b).

Solution For the NMOS version, the small-signal equivalent appears as depicted in Fig. 6.34(b), yielding

$$R_X = \frac{v_X}{i_X} \quad (6.71)$$

$$= \left(g_{m1}v_X + \frac{v_X}{r_{O1}} \right) \frac{1}{i_X} \quad (6.72)$$

$$= \frac{1}{g_{m1}} || r_{O1}. \quad (6.73)$$

For the PMOS version, we draw the equivalent as shown in Fig. 6.34(c) and write

$$R_Y = \frac{v_Y}{i_Y} \quad (6.74)$$

$$= \left(g_{m2}v_Y + \frac{v_Y}{r_{O1}} \right) \frac{1}{i_Y} \quad (6.75)$$

$$= \frac{1}{g_{m2}} || r_{O2}. \quad (6.76)$$

In both cases, the small-signal resistance is equal to $1/g_m$ if $\lambda \rightarrow 0$.

In analogy with their bipolar counterparts [Fig. 4.44(a)], the structures shown in Fig. 6.34(a) are called “diode-connected” devices and act as two-terminal components: we will encounter many applications of diode-connected devices in Chapters 9 and 10.

Owing to the lower mobility of holes (Chapter 2), PMOS devices exhibit a poorer performance than NMOS transistors. For example, Eq. (6.46) indicates that the transconductance of a PMOS device is lower for a given drain current. We therefore prefer to use NMOS transistors wherever possible.

6.5

CMOS TECHNOLOGY

Is it possible to build both NMOS and PMOS devices on the same wafer? Figures 6.2(a) and 6.32(a) reveal that the two require *different* types of substrate. Fortunately, a *local n*-type substrate can be created in a *p*-type substrate, thereby accommodating PMOS transistors.

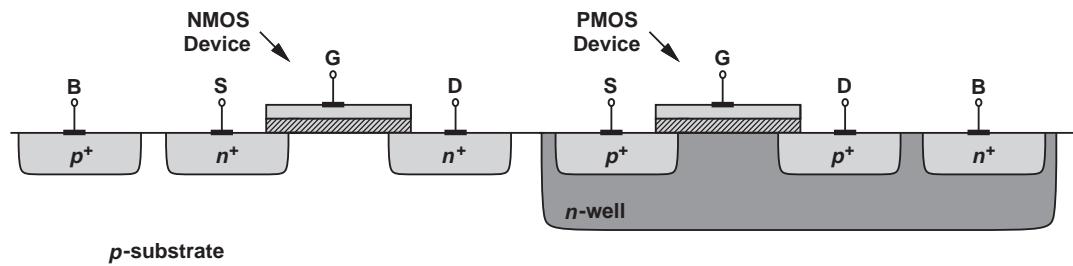


Figure 6.35 CMOS technology.

As illustrated in Fig. 6.35, an “*n*-well” encloses a PMOS device while the NMOS transistor resides in the *p*-substrate.

Called “complementary MOS” (CMOS) technology, the above structure requires more complex processing than simple NMOS or PMOS devices. In fact, the first few generations of MOS technology contained only NMOS transistors,¹⁵ and the higher cost of CMOS processes seemed prohibitive. However, many significant advantages of complementary devices eventually made CMOS technology dominant and NMOS technology obsolete.

6.6

COMPARISON OF BIPOLEAR AND MOS DEVICES

Having studied the physics and operation of bipolar and MOS transistors, we can now compare their properties. Table 6.2 shows some of the important aspects of each device. Note that the exponential $I_C - V_{BE}$ dependence of bipolar devices accords them a higher transconductance for a given bias current.

TABLE 6.2 Comparison of bipolar and MOS transistors.

Bipolar Transistor	MOSFET
Exponential Characteristic	Quadratic Characteristic
Active: $V_{CB} > 0$	Saturation: $V_{DS} > V_{GS} - V_{TH}$ (NMOS)
Saturation: $V_{CB} < 0$	Triode: $V_{DS} < V_{GS} - V_{TH}$ (NMOS)
Finite Base Current	Zero Gate Current
Early Effect	Channel-Length Modulation
Diffusion Current	Drift Current
—	Voltage-Dependent Resistor

6.7

CHAPTER SUMMARY

- A voltage-dependent current source can form an amplifier along with a load resistor. MOSFETs are electronic devices that can operate as voltage-dependent current sources.
- A MOSFET consists of a conductive plate (the “gate”) atop a semiconductor substrate and two junctions (“source” and “drain”) in the substrate. The gate controls the current flow from the source to the drain. The gate draws nearly zero current because an insulating layer separates it from the substrate.

¹⁵The first Intel microprocessor, the 4004, was realized in NMOS technology.

- As the gate voltage rises, a depletion region is formed in the substrate under the gate area. Beyond a certain gate-source voltage (the “threshold voltage”), mobile carriers are attracted to the oxide-silicon interface and a channel is formed.
- If the drain-source voltage is small, the device operates a voltage-dependent resistor.
- As the drain voltage rises, the charge density near the drain falls. If the drain voltage reaches one threshold below the gate voltage, the channel ceases to exist near the drain, leading to “pinch-off.”
- MOSFETs operate in the “triode” region if the drain voltage is more than one threshold below the gate voltage. In this region, the drain current is a function of V_{GS} and V_{DS} . The current is also proportional to the device aspect ratio, W/L .
- MOSFETs enter the “saturation region” if channel pinch-off occurs, i.e., the drain voltage is less than one threshold below the gate voltage. In this region, the drain current is proportional to $(V_{GS} - V_{TH})^2$.
- MOSFETs operating in the saturation region behave as current sources and find wide application in microelectronic circuits.
- As the drain voltage exceeds $V_{GS} - V_{TH}$ and pinch-off occurs, the drain end of the channel begins to move toward the source, reducing the effective length of the device. Called “channel-length modulation,” this effect leads to variation of drain current in the saturation region. That is, the device is not an ideal current source.
- A measure of the small-signal performance of voltage-dependent current sources is the “transconductance,” defined as the change in the output current divided by the change in the input voltage. The transconductance of MOSFETs can be expressed by one of three equations in terms of the bias voltages and currents.
- Operation across different regions and/or with large swings exemplifies “large-signal behavior.” If the signal swings are sufficiently small, the MOSFET can be represented by a small-signal model consisting of a *linear* voltage-dependent current source and an output resistance.
- The small-signal model is derived by making a small change in the voltage difference between two terminals while the other voltages remain constant.
- The small-signal models of NMOS and PMOS devices are identical.
- NMOS and PMOS transistors are fabricated on the same substrate to create CMOS technology.

PROBLEMS

In the following problems, unless otherwise stated, assume $\mu_n C_{ox} = 200 \mu\text{A}/\text{V}^2$, $\mu_p C_{ox} = 100 \mu\text{A}/\text{V}^2$, and $V_{TH} = 0.4 \text{ V}$ for NMOS devices and -0.4 V for PMOS devices.

Sec. 6.2 Operation of MOSFET

*6.1. Two identical MOSFETs are placed in series as shown in Fig. 6.36. If both devices operate as resistors, explain intuitively why

this combination is equivalent to a single transistor, M_{eq} . What are the width and length of M_{eq} ?

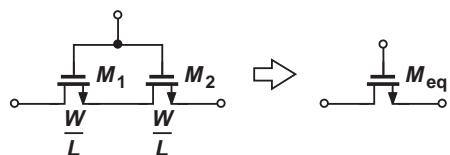


Figure 6.36

6.2. Referring to Fig. 6.11 and assuming that $V_D > 0$,

- (a) Sketch the electron density in the channel as a function of x .
- (b) Sketch the local resistance of the channel (per unit length) as a function of x .

6.3. Calculate the total charge stored in the channel of an NMOS device if $C_{ox} = 10 \text{ fF}/\mu\text{m}^2$, $W = 5 \mu\text{m}$, $L = 0.1 \mu\text{m}$, and $V_{GS} - V_{TH} = 1 \text{ V}$. Assume $V_{DS} = 0$.

***6.4.** Consider a MOSFET experiencing pinch-off near the drain. Equation (6.4) indicates that the charge density and carrier velocity must change in opposite directions if the current remains constant. How can this relationship be interpreted at the pinch-off point, where the charge density approaches zero?

6.5. Assuming I_D is constant, solve Eq. (6.7) to obtain an expression for $V(x)$. Plot both $V(x)$ and dV/dx as a function of x for different values of W or V_{TH} .

***6.6.** The drain current of a MOSFET in the triode region is expressed as

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]. \quad (6.77)$$

Suppose the values of $\mu_n C_{ox}$ and W/L are unknown. Is it possible to determine these quantities by applying different values of $V_{GS} - V_{TH}$ and V_{DS} and measuring I_D ?

6.7. An NMOS device carries 1 mA with $V_{GS} - V_{TH} = 0.6 \text{ V}$ and 1.6 mA with $V_{GS} - V_{TH} = 0.8 \text{ V}$. If the device operates in the triode region, calculate V_{DS} and W/L .

***6.8.** Compute the transconductance of a MOSFET operating in the triode region. Define $g_m = \partial I_D / \partial V_{GS}$ for a constant V_{DS} . Explain why $g_m = 0$ for $V_{DS} = 0$.

6.9. For a MOS transistor biased in the triode region, we can define an incremental drain-source resistance as

$$r_{DS,tri} = \left(\frac{\partial I_D}{\partial V_{DS}} \right)^{-1}. \quad (6.78)$$

Derive an expression for this quantity.

6.10. We wish to use an NMOS transistor as a variable resistor with $R_{on} = 500 \Omega$ at

$V_{GS} = 1 \text{ V}$ and $R_{on} = 400 \Omega$ at $V_{GS} = 1.5 \text{ V}$. Explain why this is not possible.

6.11. An NMOS device operating with a small drain-source voltage serves as a resistor. If the supply voltage is 1.8 V, what is the minimum on-resistance that can be achieved with $W/L = 20$?

6.12. It is possible to define an “intrinsic time constant” for a MOSFET operating as a resistor:

$$\tau = R_{on} C_{GS}, \quad (6.79)$$

where $C_{GS} = WLC_{ox}$. Obtain an expression for τ and explain what the circuit designer must do to minimize the time constant.

6.13. In the circuit of Fig. 6.37, M_1 serves as an electronic switch. If $V_{in} \approx 0$, determine W/L such that the circuit attenuates the signal by only 5%. Assume $V_G = 1.8 \text{ V}$ and $R_L = 100 \Omega$.

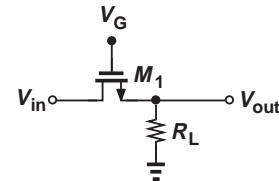


Figure 6.37

6.14. In the circuit of Fig. 6.37, the input is a small sinusoid superimposed on a dc level: $V_{in} = V_0 \cos \omega t + V_1$, where V_0 is on the order of a few millivolts.

- (a) For $V_1 = 0$, obtain W/L in terms of R_L and other parameters so that $V_{out} = 0.95 V_{in}$.
- (b) Repeat part (a) for $V_1 = 0.5 \text{ V}$. Compare the results.

6.15. For an NMOS device, plot I_D as a function of V_{GS} for different values of V_{DS} .

6.16. In Fig. 6.17, explain why the peaks of the parabolas lie on a parabola themselves.

6.17. For MOS devices with very short channel lengths, the square-law behavior is not valid, and we may instead write:

$$I_D = WC_{ox}(V_{GS} - V_{TH})v_{sat}, \quad (6.80)$$

where v_{sat} is a relatively constant velocity. Determine the transconductance of such a device.

- 6.18.** Advanced MOS devices do not follow the square-law behavior expressed by Eq. (6.17). A somewhat better approximation is:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^\alpha, \quad (6.81)$$

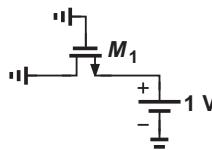
where α is less than 2. Determine the transconductance of such a device.

- *6.19.** Determine the region of operation of M_1 in each of the circuits shown in Fig. 6.38.

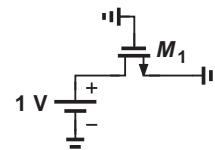
- *6.20.** Determine the region of operation of M_1 in each of the circuits shown in Fig. 6.39.

- 6.21.** Two current sources realized by identical MOSFETs (Fig. 6.40) match to within 1%, i.e., $0.99I_{D2} < I_{D1} < 1.01I_{D2}$. If $V_{DS1} = 0.5$ V and $V_{DS2} = 1$ V, what is the maximum tolerable value of λ ?

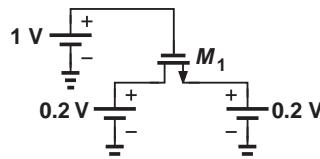
- 6.22.** Assume $\lambda = 0$, compute W/L of M_1 in Fig. 6.41 such that the device operates at the edge of saturation.



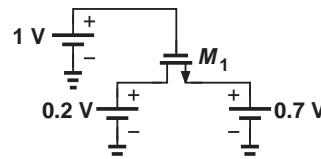
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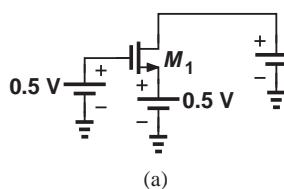


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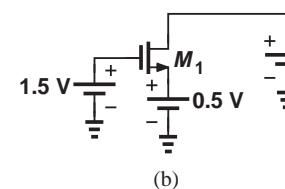


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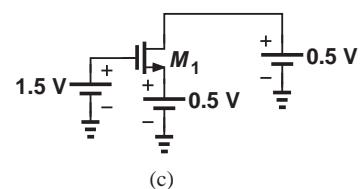
Figure 6.38



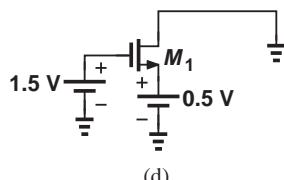
(a)



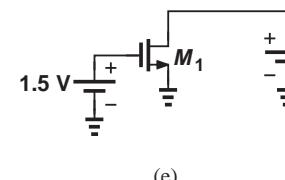
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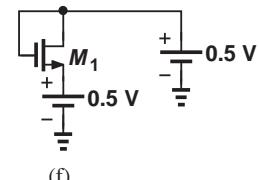
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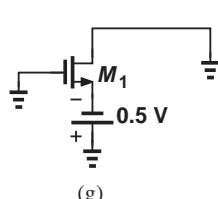
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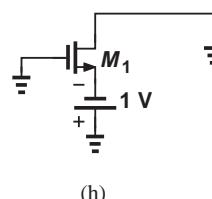
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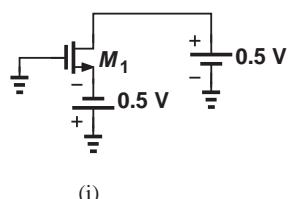
(f)



(g)



(h)



(i)

Figure 6.39

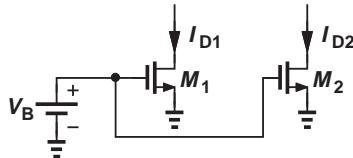


Figure 6.40

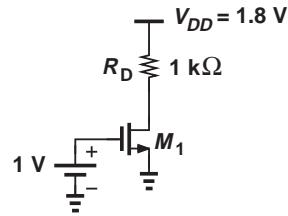


Figure 6.41

6.23. Using the value of W/L found in Problem 6.22, explain what happens if the gate oxide thickness is doubled due to a manufacturing error.

6.24. In the Fig. 6.42, what is the minimum allowable value of V_{DD} if M_1 must not enter the triode region? Assume $\lambda = 0$.

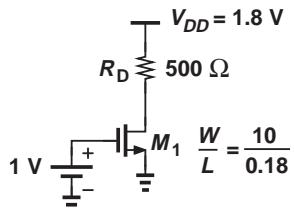


Figure 6.42

6.25. Calculate the bias current of M_1 in Fig. 6.43 if $\lambda = 0$.

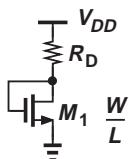


Figure 6.43

6.26. Compute the value of W/L for M_1 in Fig. 6.44 for a bias current of I_1 . Assume $\lambda = 0$.

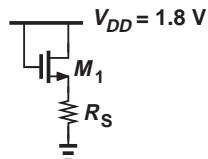


Figure 6.44

***6.27.** In Fig. 6.45, derive a relationship among the circuit parameters that guarantees M_1 operates at the edge of saturation. Assume $\lambda = 0$.

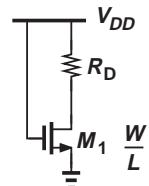


Figure 6.45

****6.28.** Sketch I_X as a function of V_X for the circuits shown in Fig. 6.46. Assume V_X goes from 0 to $V_{DD} = 1.8$ V. Also, $\lambda = 0$. Determine at what value of V_X the device changes its region of operation.

6.29. Assuming $W/L = 10/0.18$, $\lambda = 0.1 \text{ V}^{-1}$, and $V_{DD} = 1.8$ V, calculate the drain current of M_1 in Fig. 6.47.

6.30. In the circuit of Fig. 6.48, $W/L = 20/0.18$ and $\lambda = 0.1 \text{ V}^{-1}$. What value of V_B places the transistor at the edge of saturation?

6.31. An NMOS device operating in saturation with $\lambda = 0$ must provide a transconductance of $1/(50 \Omega)$.

- Determine W/L if $I_D = 0.5$ mA.
- Determine W/L if $V_{GS} - V_{TH} = 0.5$ V.
- Determine I_D if $V_{GS} - V_{TH} = 0.5$ V.

****6.32.** Determine how the transconductance of a MOSFET (operating in saturation) changes if

- W/L is doubled but I_D remains constant.
- $V_{GS} - V_{TH}$ is doubled but I_D remains constant.
- I_D is doubled but W/L remains constant.
- I_D is doubled but $V_{GS} - V_{TH}$ remains constant.

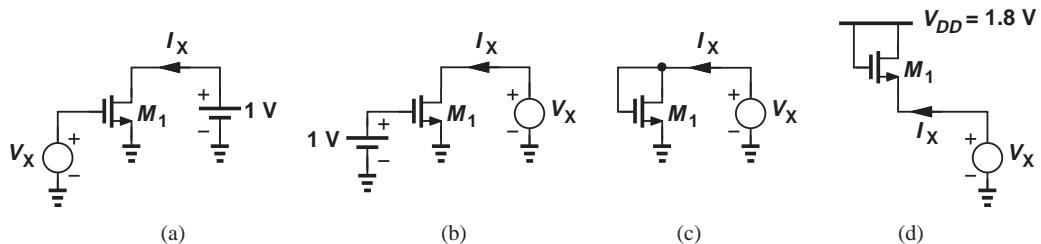


Figure 6.46

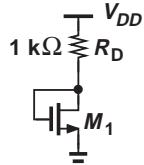


Figure 6.47

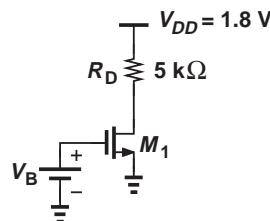
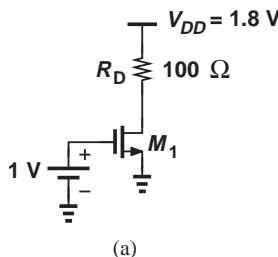
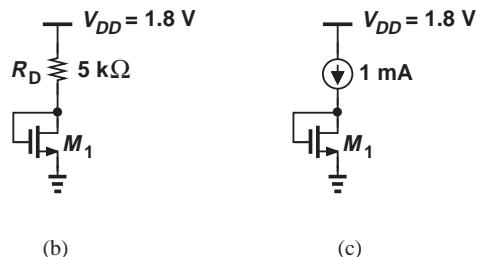


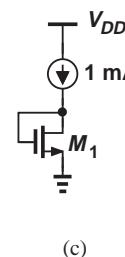
Figure 6.48



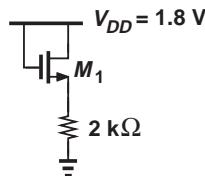
(a)



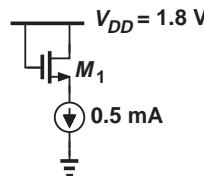
(b)



(c)



(d)



(e)

Figure 6.49

- 6.33.** The “intrinsic gain” of a MOSFET operating in saturation is defined as $g_m r_O$. Derive an expression for $g_m r_O$ and plot the result as a function of I_D . Assume V_{DS} is constant.

- 6.34.** If $\lambda = 0.1 \text{ V}^{-1}$ and $W/L = 20/0.18$, construct the small-signal model of each of the circuits shown in Fig. 6.49.

- *6.35.** Assuming a constant V_{DS} , plot the intrinsic gain, $g_m r_O$, of a MOSFET
(a) as a function of $V_{GS} - V_{TH}$ if I_D is constant.
(b) as a function of I_D if $V_{GS} - V_{TH}$ is constant.

- 6.36.** An NMOS device with $\lambda = 0.1 \text{ V}^{-1}$ must provide a $g_m r_O$ of 20 with $V_{DS} = 1.5 \text{ V}$. Determine the required value of W/L if $I_D = 0.5 \text{ mA}$.

- 6.37.** Repeat Problem 6.36 for $\lambda = 0.2 \text{ V}^{-1}$.

- 6.38.** Construct the small-signal model of the circuits depicted in Fig. 6.50. Assume all transistors operate in saturation and $\lambda \neq 0$.

Sec. 6.4 PMOS Transistor

- *6.39.** Determine the region of operation of M_1 in each circuit shown in Fig. 6.51.
***6.40.** Determine the region of operation of M_1 in each circuit shown in Fig. 6.52.

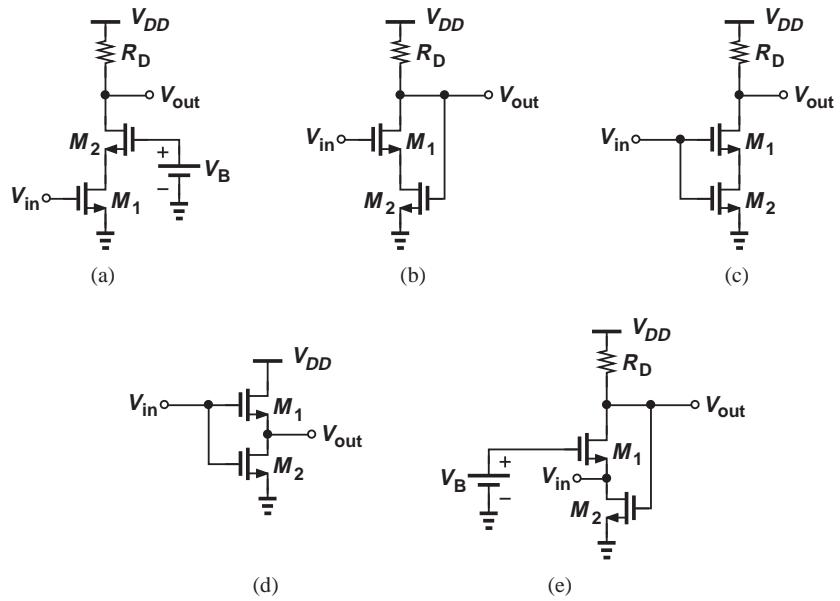


Figure 6.50

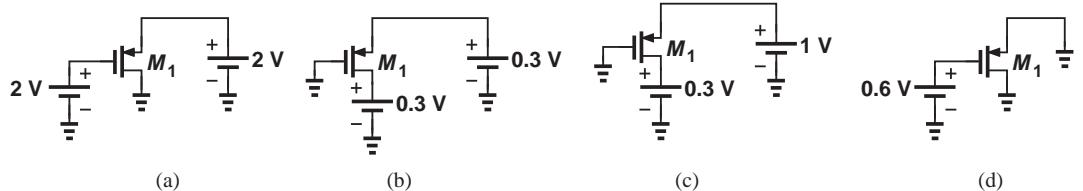


Figure 6.51

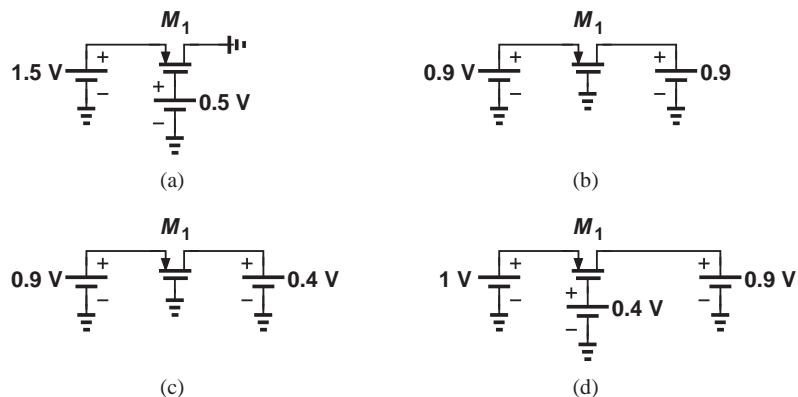
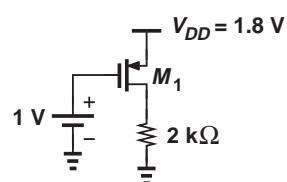


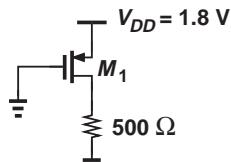
Figure 6.52

- 6.41.** If $\lambda = 0$, what value of W/L places M_1 at the edge of saturation in Fig. 6.53?
- 6.42.** With the value of W/L obtained in Problem 6.41, what happens if V_B changes to +0.8 V?
- 6.43.** If $W/L = 10/0.18$ and $\lambda = 0$, determine the operating point of M_1 in each circuit depicted in Fig. 6.54.
- 6.44.** Sketch I_X as a function of V_X for the circuits shown in Fig. 6.55. Assume V_X goes from 0 to $V_{DD} = 1.8$ V. Also, $\lambda = 0$. Determine at what value of V_X the device changes its region of operation.
- 6.45.** Construct the small-signal model of each circuit shown in Fig. 6.56 if all of the transistors operate in saturation and $\lambda \neq 0$.

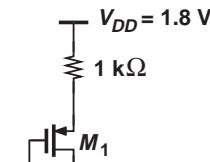


(a)

Figure 6.53

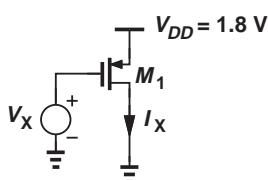


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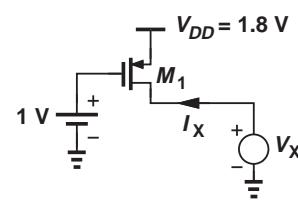


(c)

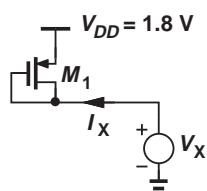
Figure 6.54



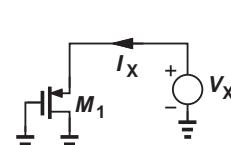
(a)



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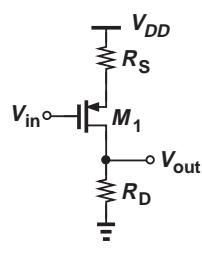


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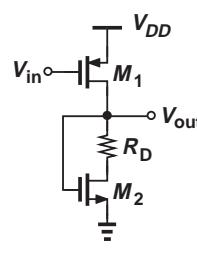


(d)

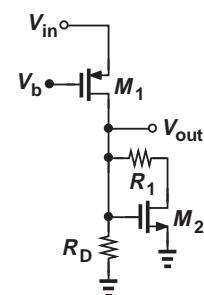
Figure 6.55



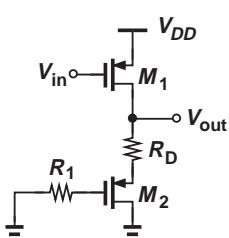
(a)



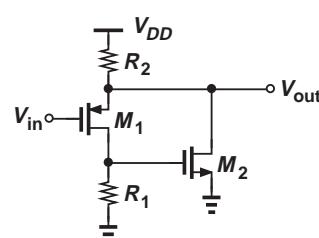
(b)



(c)



(d)



(e)

Figure 6.56

****6.46.** Consider the circuit depicted in Fig. 6.57, where M_1 and M_2 operate in saturation and exhibit channel-length modulation coefficients λ_n and λ_p , respectively.

- Construct the small-signal equivalent circuit and explain why M_1 and M_2 appear in “parallel.”
- Determine the small-signal voltage gain of the circuit.

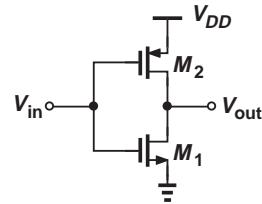


Figure 6.57

SPICE PROBLEMS

In the following problems, use the MOS models and source/drain dimensions given in Appendix A. Assume the substrates of NMOS and PMOS devices are tied to ground and V_{DD} , respectively.

6.47. For the circuit shown in Fig. 6.58, plot V_X as a function of I_X for $0 < I_X < 3$ mA. Explain the sharp change in V_X as I_X exceeds a certain value.

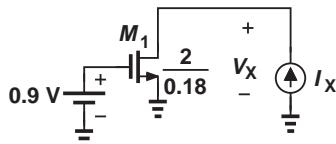


Figure 6.58

6.48. Plot the input/output characteristic of the stage shown in Fig. 6.59 for $0 < V_{in} < 1.8$ V. At what value of V_{in} does the slope (gain) reach a maximum?

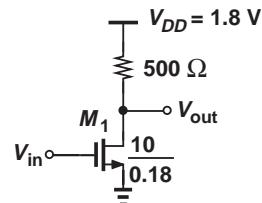
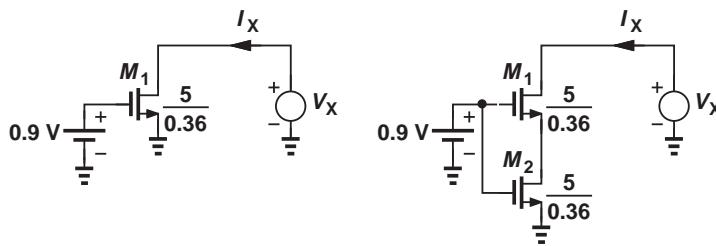


Figure 6.59

6.49. For the arrangements shown in Fig. 6.60, plot I_D as a function of V_X as V_X varies from 0 to 1.8 V. Can we say these two arrangements are equivalent?



(a)

(b)

Figure 6.60

- 6.50.** Plot I_X as a function of V_X for the arrangement depicted in Fig. 6.61 as V_X varies from 0 to 1.8 V. Can you explain the behavior of the circuit?

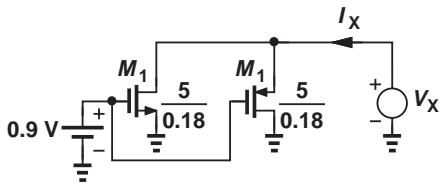


Figure 6.61

- 6.51.** Repeat Problem 6.50 for the circuit illustrated in Fig. 6.62.

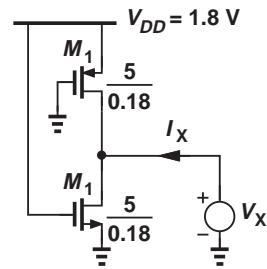
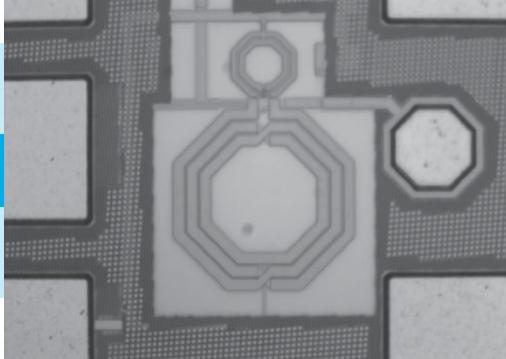


Figure 6.62



CMOS Amplifiers

Most CMOS amplifiers have identical bipolar counterparts and can therefore be analyzed in the same fashion. Our study in this chapter parallels the developments in Chapter 5, identifying both similarities and differences between CMOS and bipolar circuit topologies. It is recommended that the reader review Chapter 5, specifically, Section 5.1. We assume the reader is familiar with concepts such as I/O impedances, biasing, and dc and small-signal analysis. The outline of the chapter is shown below.

General Concepts

- **Biassing of MOS Stages**
- **Realization of Current Sources**

MOS Amplifiers

- **Common-Source Stage**
- **Common-Gate Stage**
- **Source Follower**

7.1

GENERAL CONSIDERATIONS

7.1.1 MOS Amplifier Topologies

Recall from Section 5.3 that the nine possible circuit topologies using a bipolar transistor in fact reduce to three useful configurations. The similarity of bipolar and MOS small-signal models (i.e., a voltage-controlled current source) suggests that the same must hold for MOS amplifiers. In other words, we expect three basic CMOS amplifiers: the “common-source” (CS) stage, the “common-gate” (CG) stage, and the “source follower.”

7.1.2 Biasing

Depending on the application, MOS circuits may incorporate biasing techniques that are quite different from those described in Chapter 5 for bipolar stages. Most of these techniques are beyond the scope of this book and some methods are studied in Chapter 5. Nonetheless, it is still instructive to apply some of the biasing concepts of Chapter 5 to MOS stages.

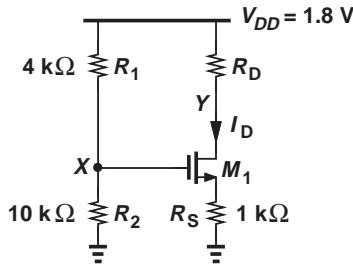


Figure 7.1 MOS stage with biasing.

Consider the circuit shown in Fig. 7.1, where the gate voltage is defined by R_1 and R_2 . We assume M_1 operates in saturation. Also, in most bias calculations, we can neglect channel-length modulation. Noting that the gate current is zero, we have

$$V_X = \frac{R_2}{R_1 + R_2} V_{DD}. \quad (7.1)$$

Since $V_X = V_{GS} + I_D R_S$,

$$\frac{R_2}{R_1 + R_2} V_{DD} = V_{GS} + I_D R_S. \quad (7.2)$$

Also,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2. \quad (7.3)$$

Equations (7.2) and (7.3) can be solved to obtain I_D and V_{GS} , either by iteration or by finding I_D from Eq. (7.2) and replacing for it in Eq. (7.3):

$$\left(\frac{R_2}{R_1 + R_2} V_{DD} - V_{GS} \right) \frac{1}{R_S} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2. \quad (7.4)$$

That is,

$$V_{GS} = -(V_1 - V_{TH}) + \sqrt{(V_1 - V_{TH})^2 - V_{TH}^2 + \frac{2R_2}{R_1 + R_2} V_1 V_{DD}}, \quad (7.5)$$

$$= -(V_1 - V_{TH}) + \sqrt{V_1^2 + 2V_1 \left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{TH} \right)}, \quad (7.6)$$

where

$$V_1 = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_S}. \quad (7.7)$$

This value of V_{GS} can then be substituted in Eq. (7.2) to obtain I_D . Of course, V_Y must exceed $V_X - V_{TH}$ to ensure operation in the saturation region.

**Example
7.1**

Determine the bias current of M_1 in Fig. 7.1 assuming $V_{TH} = 0.5$ V, $\mu_n C_{ox} = 100 \mu\text{A/V}^2$, $W/L = 5/0.18$, and $\lambda = 0$. What is the maximum allowable value of R_D for M_1 to remain in saturation?

Solution We have

$$V_X = \frac{R_2}{R_1 + R_2} V_{DD} \quad (7.8)$$

$$= 1.286 \text{ V.} \quad (7.9)$$

With an initial guess $V_{GS} = 1 \text{ V}$, the voltage drop across R_S can be expressed as $V_X - V_{GS} = 286 \text{ mV}$, yielding a drain current of $286 \mu\text{A}$. Substituting for I_D in Eq. (7.3) gives the new value of V_{GS} as

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}} \quad (7.10)$$

$$= 0.954 \text{ V.} \quad (7.11)$$

Consequently,

$$I_D = \frac{V_X - V_{GS}}{R_S} \quad (7.12)$$

$$= 332 \mu\text{A}, \quad (7.13)$$

and hence

$$V_{GS} = 0.989 \text{ V.} \quad (7.14)$$

This gives $I_D = 297 \mu\text{A}$.

As seen from the iterations, the solutions converge more slowly than those encountered in Chapter 5 for bipolar circuits. This is due to the quadratic (rather than exponential) I_D - V_{GS} dependence. We may therefore utilize the exact result in Eq. (7.6) to avoid lengthy calculations. Since $V_1 = 0.36 \text{ V}$,

$$V_{GS} = 0.974 \text{ V} \quad (7.15)$$

and

$$I_D = \frac{V_X - V_{GS}}{R_S} \quad (7.16)$$

$$= 312 \mu\text{A}. \quad (7.17)$$

The maximum allowable value of R_D is obtained if $V_Y = V_X - V_{TH} = 0.786 \text{ V}$. That is,

$$R_D = \frac{V_{DD} - V_Y}{I_D} \quad (7.18)$$

$$= 3.25 \text{ k}\Omega. \quad (7.19)$$

Exercise What is the value of R_2 that places M_1 at the edge of saturation?

**Example
7.2**

In the circuit of Example 7.1, assume M_1 is in saturation and $R_D = 2.5 \text{ k}\Omega$ and compute (a) the maximum allowable value of W/L and (b) the minimum allowable value of R_S (with $W/L = 5/0.18$). Assume $\lambda = 0$.

Solution (a) As W/L becomes larger, M_1 can carry a larger current for a given V_{GS} . With $R_D = 2.5 \text{ k}\Omega$ and $V_X = 1.286 \text{ V}$, the maximum allowable value of I_D is given by

$$I_D = \frac{V_{DD} - V_Y}{R_D} \quad (7.20)$$

$$= 406 \mu\text{A}. \quad (7.21)$$

The voltage drop across R_S is then equal to 406 mV, yielding $V_{GS} = 1.286 \text{ V} - 0.406 \text{ V} = 0.88 \text{ V}$. In other words, M_1 must carry a current of 406 μA with $V_{GS} = 0.88 \text{ V}$:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (7.22)$$

$$406 \mu\text{A} = (50 \mu\text{A}/\text{V}^2) \frac{W}{L} (0.38 \text{ V})^2; \quad (7.23)$$

thus,

$$\frac{W}{L} = 56.2. \quad (7.24)$$

(b) With $W/L = 5/0.18$, the minimum allowable value of R_S gives a drain current of 406 μA . Since

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}} \quad (7.25)$$

$$= 1.041 \text{ V}, \quad (7.26)$$

the voltage drop across R_S is equal to $V_X - V_{GS} = 245 \text{ mV}$. It follows that

$$R_S = \frac{V_X - V_{GS}}{I_D} \quad (7.27)$$

$$= 604 \Omega. \quad (7.28)$$

Exercise Repeat the above example if $V_{TH} = 0.35 \text{ V}$.

The self-biasing technique of Fig. 5.22 can also be applied to MOS amplifiers. Depicted in Fig. 7.2, the circuit can be analyzed by noting that M_1 is in saturation (why?) and the voltage drop across R_G is zero. Thus,

$$I_D R_D + V_{GS} + R_S I_D = V_{DD}. \quad (7.29)$$

Finding V_{GS} from this equation and substituting it in Eq. (7.3), we have

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{DD} - (R_S + R_D) I_D - V_{TH}]^2, \quad (7.30)$$

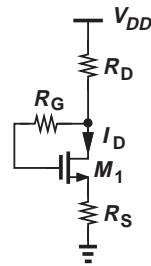


Figure 7.2 Self-biased MOS stage.

where channel-length modulation is neglected. It follows that

$$(R_S + R_D)^2 I_D^2 - 2 \left[(V_{DD} - V_{TH})(R_S + R_D) + \frac{1}{\mu_n C_{ox} \frac{W}{L}} \right] I_D + (V_{DD} - V_{TH})^2 = 0. \quad (7.31)$$

**Example
7.3**

Calculate the drain current of M_1 in Fig. 7.3 if $\mu_n C_{ox} = 100 \mu\text{A}/\text{V}^2$, $V_{TH} = 0.5 \text{ V}$, and $\lambda = 0$. What value of R_D is necessary to reduce I_D by a factor of two?

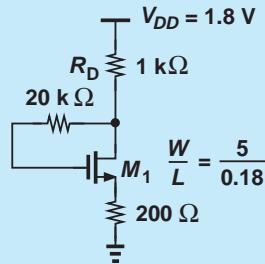


Figure 7.3 Example of self-biased MOS stage.

Solution Equation (7.31) gives

$$I_D = 556 \mu\text{A}. \quad (7.32)$$

To reduce I_D to $278 \mu\text{A}$, we solve Eq. (7.31) for R_D :

$$R_D = 2.867 \text{ k}\Omega. \quad (7.33)$$

Exercise Repeat the above example if V_{DD} drops to 1.2 V.

7.1.3 Realization of Current Sources

MOS transistors operating in saturation can act as current sources. As illustrated in Fig. 7.4(a), an NMOS device serves as a current source with one terminal tied to ground, i.e., it draws current from node X to ground. On the other hand, a PMOS transistor

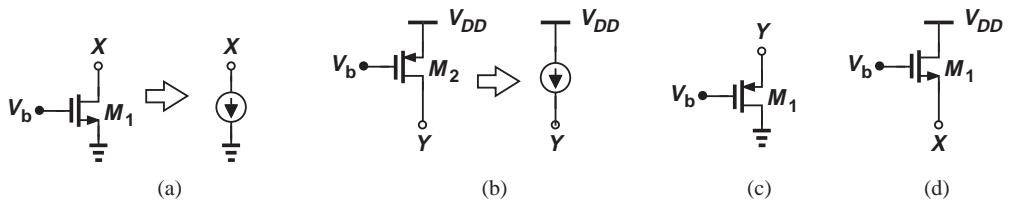


Figure 7.4 (a) NMOS device operating as a current source, (b) PMOS device operating as a current source, (c) PMOS topology not operating as a current source, (d) NMOS topology not operating as a current source.

[Fig. 7.4(b)] draws current from V_{DD} to node Y . If $\lambda = 0$, these currents remain independent of V_X or V_Y (so long as the transistors are in saturation).

It is important to understand that only the *drain* terminal of a MOSFET can draw a dc current and still present a high impedance. Specifically, NMOS or PMOS devices configured as shown in Figs. 7.4(c) and (d) do *not* operate as current sources because variation of V_X or V_Y directly changes the gate-source voltage of each transistor, thus changing the drain current considerably. From another perspective, the small-signal model of these two structures is identical to that of the diode-connected devices in Fig. 6.34, revealing a small-signal impedance of only $1/g_m$ (if $\lambda = 0$) rather than infinity.

7.2

COMMON-SOURCE STAGE

7.2.1 CS Core

Shown in Fig. 7.5(a), the basic CS stage is similar to the common-emitter topology, with the input applied to the gate and the output sensed at the drain. For small signals, M_1 converts the input voltage variations to proportional drain current changes, and R_D transforms the drain currents to the output voltage. If channel-length modulation is neglected, the small-signal model in Fig. 7.5(b) yields $v_{in} = v_1$ and $v_{out} = -g_m v_1 R_D$. That is,

$$\frac{v_{out}}{v_{in}} = -g_m R_D, \quad (7.34)$$

a result similar to that obtained for the common emitter stage in Chapter 5.

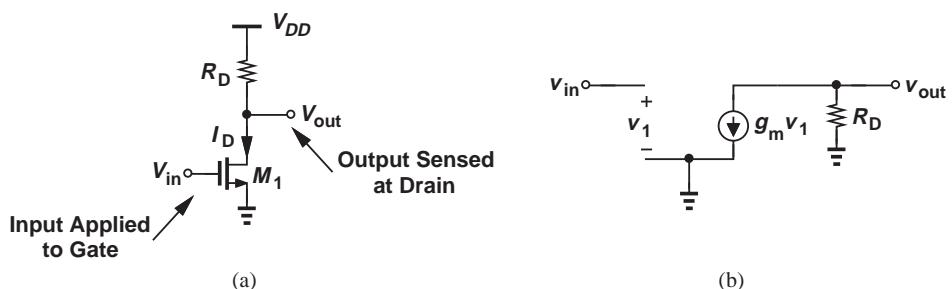


Figure 7.5 (a) Common-source stage, (b) small-signal mode.

The voltage gain of the CS stage is also limited by the supply voltage. Since $g_m = \sqrt{2\mu_n C_{ox} (W/L) I_D}$, we have

$$A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D R_D}, \quad (7.35)$$

concluding that if I_D or R_D is increased, so is the voltage drop across R_D ($= I_D R_D$).¹ For M_1 to remain in saturation,

$$V_{DD} - R_D I_D > V_{GS} - V_{TH}, \quad (7.36)$$

that is,

$$R_D I_D < V_{DD} - (V_{GS} - V_{TH}). \quad (7.37)$$

**Example
7.4**

Calculate the small-signal voltage gain of the CS stage shown in Fig. 7.6 if $I_D = 1$ mA, $\mu_n C_{ox} = 100 \mu\text{A/V}^2$, $V_{TH} = 0.5$ V, and $\lambda = 0$. Verify that M_1 operates in saturation.

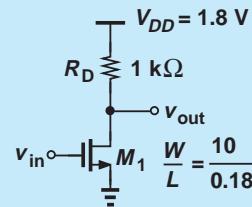


Figure 7.6 Example of CS stage.

Solution We have

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \quad (7.38)$$

$$= \frac{1}{300 \Omega}. \quad (7.39)$$

Thus,

$$A_v = -g_m R_D \quad (7.40)$$

$$= 3.33. \quad (7.41)$$

To check the operation region, we first determine the gate-source voltage:

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}} \quad (7.42)$$

$$= 1.1 \text{ V}. \quad (7.43)$$

¹It is possible to raise the gain to some extent by increasing W , but “subthreshold conduction” eventually limits the transconductance. This concept is beyond the scope of this book.

The drain voltage is equal to $V_{DD} - R_D I_D = 0.8$ V. Since $V_{GS} - V_{TH} = 0.6$ V, the device indeed operates in saturation and has a margin of 0.2 V with respect to the triode region. For example, if R_D is doubled with the intention of doubling A_v , then M_1 enters the triode region and its transconductance drops.

Exercise What value of V_{TH} places M_1 at the edge of saturation?

Since the gate terminal of MOSFETs draws a zero current (at very low frequencies), we say the CS amplifier provides a current gain of infinity. By contrast, the current gain of a common-emitter stage is equal to β .

Let us now compute the I/O impedances of the CS amplifier. Since the gate current is zero (at low frequencies),

$$R_{in} = \infty, \quad (7.44)$$

a point of contrast to the CE stage (whose R_{in} is equal to r_π). The high input impedance of the CS topology plays a critical role in many analog circuits.

The similarity between the small-signal equivalents of CE and CS stages indicates that the output impedance of the CS amplifier is simply equal to

$$R_{out} = R_D. \quad (7.45)$$

This is also seen from Fig. 7.7.

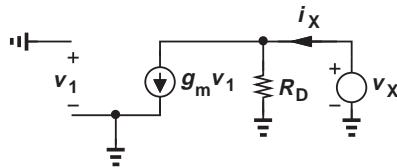


Figure 7.7 Output impedance of CS stage.

In practice, channel-length modulation may not be negligible, especially if R_D is large. The small-signal model of CS topology is therefore modified as shown in Fig. 7.8, revealing that

$$A_v = -g_m(R_D || r_O) \quad (7.46)$$

$$R_{in} = \infty \quad (7.47)$$

$$R_{out} = R_D || r_O. \quad (7.48)$$

In other words, channel-length modulation and the Early effect impact the CS and CE stages, respectively, in a similar manner.

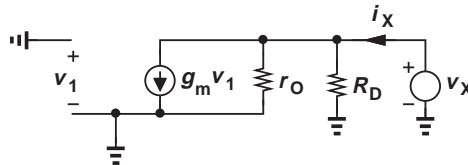


Figure 7.8 Effect of channel-length modulation on CS stage.

**Example
7.5**

Assuming M_1 operates in saturation, determine the voltage gain of the circuit depicted in Fig. 7.9(a) and plot the result as a function of the transistor channel length while other parameters remain constant.

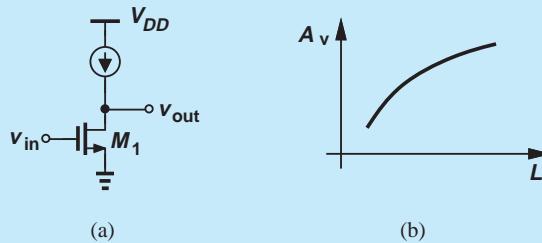


Figure 7.9 (a) CS stage with ideal current source as a load, (b) gain as a function of device channel length.

Solution The ideal current source presents an infinite small-signal resistance, allowing the use of Eq. (7.46) with $R_D = \infty$:

$$A_v = -g_m r_O. \quad (7.49)$$

This is the highest voltage gain that a single transistor can provide. Writing $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}$ and $r_O = (\lambda I_D)^{-1}$, we have

$$|A_v| = \frac{\sqrt{2\mu_n C_{ox} \frac{W}{L}}}{\lambda \sqrt{I_D}}. \quad (7.50)$$

This result may imply that $|A_v|$ falls as L increases, but recall from Chapter 6 that $\lambda \propto L^{-1}$:

$$|A_v| \propto \sqrt{\frac{2\mu_n C_{ox} WL}{I_D}}. \quad (7.51)$$

Consequently, $|A_v|$ increases with L [Fig. 7.9(b)].

Exercise Repeat the above example if a resistor of value R_1 is tied between the gate and drain of M_1 .

7.2.2 CS Stage With Current-Source Load

As seen in the above example, the trade-off between the voltage gain and the voltage headroom can be relaxed by replacing the load resistor with a current source. The observations made in relation to Fig. 7.4(b) therefore suggest the use of a PMOS device as the load of an NMOS CS amplifier [Fig. 7.10(a)].

Let us determine the small-signal gain and output impedance of the circuit. Having a constant gate-source voltage, M_2 simply behaves as a resistor equal to its

Did you know?

The intrinsic gain, $g_m r_o$, of MOSFETs has fallen with technology scaling, i.e., as the minimum channel length has gone from about 10 μm in the 1960s to 25 nm today. Due to severe channel-length modulation, the intrinsic gain of these short-channel devices is on the order of 5 to 10, making it difficult to achieve a high voltage gain in many analog circuits. This issue has prompted extensive research on analog design using low-gain building blocks. For example, the analog-to-digital converter that digitizes the image in your camera may need an op amp with a gain of 4,000 but must now be designed with a gain of only 20.

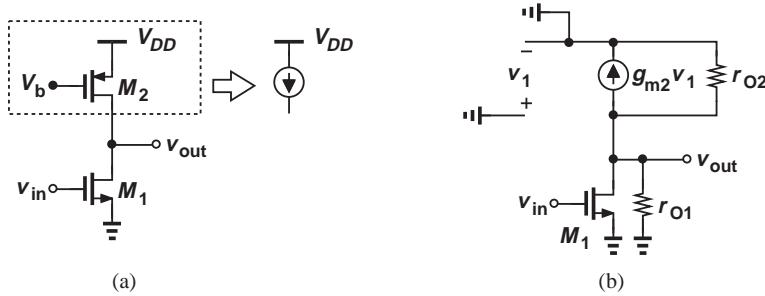


Figure 7.10 (a) CS stage using a PMOS device as a current source, (b) small-signal model.

output impedance [Fig. 7.10(b)] because \$v_1 = 0\$ and hence \$g_{m2}v_1 = 0\$. Thus, the drain node of \$M_1\$ sees both \$r_{O1}\$ and \$r_{O2}\$ to ac ground. Equations (7.46) and (7.48) give

$$A_v = -g_{m1}(r_{O1}||r_{O2}) \quad (7.52)$$

$$R_{out} = r_{O1}||r_{O2}. \quad (7.53)$$

**Example
7.6**

Figure 7.11 shows a PMOS CS stage using an NMOS current source load. Compute the voltage gain of the circuit.

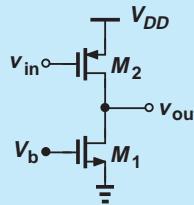


Figure 7.11 CS stage using an NMOS device as current source.

Solution Transistor \$M_2\$ generates a small-signal current equal to \$g_{m2}v_{in}\$, which then flows through \$r_{O1}||r_{O2}\$, producing \$v_{out} = -g_{m2}v_{in}(r_{O1}||r_{O2})\$. Thus,

$$A_v = -g_{m2}(r_{O1}||r_{O2}). \quad (7.54)$$

Exercise

Calculate the gain if the circuit drives a loads resistance equal to \$R_L\$.

7.2.3 CS Stage With Diode-Connected Load

In some applications, we may use a diode-connected MOSFET as the drain load. Illustrated in Fig. 7.12(a), such a topology exhibits only a moderate gain due to the relatively low impedance of the diode-connected device (Section 7.1.3). With \$\lambda = 0\$, \$M_2\$ acts as a small-signal resistance equal to \$1/g_{m2}\$, and Eq. (7.34) yields

$$A_v = -g_{m1} \cdot \frac{1}{g_{m2}} \quad (7.55)$$

$$= -\frac{\sqrt{2\mu_n C_{ox} (W/L)_1} I_D}{\sqrt{2\mu_n C_{ox} (W/L)_2} I_D} \quad (7.56)$$

$$= -\sqrt{\frac{(W/L)_1}{(W/L)_2}}. \quad (7.57)$$

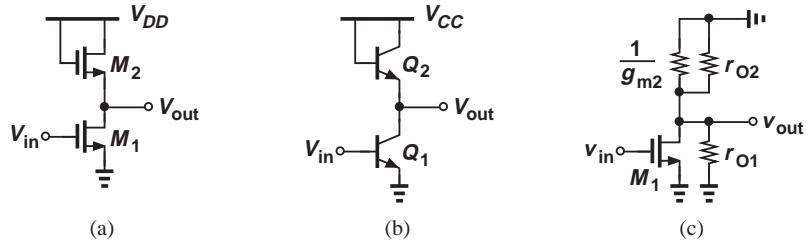


Figure 7.12 (a) MOS stage using a diode-connected load, (b) bipolar counterpart, (c) simplified circuit of (a).

Interestingly, the gain is given by the dimensions of \$M_1\$ and \$M_2\$ and remains independent of process parameters \$\mu_n\$ and \$C_{ox}\$ and the drain current, \$I_D\$.

The reader may wonder why we did not consider a common-emitter stage with a diode-connected load in Chapter 5. Shown in Fig. 7.12(b), such a circuit is not used because it provides a voltage gain of only unity:

$$A_v = -g_{m1} \cdot \frac{1}{g_{m2}} \quad (7.58)$$

$$= -\frac{I_{C1}}{V_T} \cdot \frac{1}{I_{C2}/V_T} \quad (7.59)$$

$$\approx -1. \quad (7.60)$$

The contrast between Eqs. (7.57) and (7.60) arises from a fundamental difference between MOS and bipolar devices: transconductance of the former depends on device dimensions whereas that of the latter does not.

A more accurate expression for the gain of the stage in Fig. 7.12(a) must take channel-length modulation into account. As depicted in Fig. 7.12(c), the resistance seen at the drain is now equal to \$(1/g_{m2})||r_{o2}||r_{o1}\$, and hence

$$A_v = -g_{m1} \left(\frac{1}{g_{m2}} || r_{o2} || r_{o1} \right). \quad (7.61)$$

Similarly, the output resistance of the stage is given by

$$R_{out} = \frac{1}{g_{m2}} || r_{o2} || r_{o1}. \quad (7.62)$$

**Example
7.7**

Determine the voltage gain of the circuit shown in Fig. 7.13(a) if \$\lambda \neq 0\$.

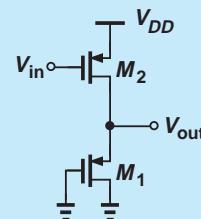


Figure 7.13 CS stage with diode-connected PMOS device.

Solution This stage is similar to that in Fig. 7.12(a), but with NMOS devices changed to PMOS transistors: M_1 serves as a common-source device and M_2 as a diode-connected load. Thus,

$$A_v = -g_{m2} \left(\frac{1}{g_{m1}} || r_{O1} || r_{O2} \right). \quad (7.63)$$

Exercise Repeat the above example if the gate of M_1 is tied to a constant voltage equal to 0.5 V.

7.2.4 CS Stage With Degeneration

Recall from Chapter 5 that a resistor placed in series with the emitter of a bipolar transistor alters characteristics such as gain, I/O impedances, and linearity. We expect similar results for a degenerated CS amplifier.

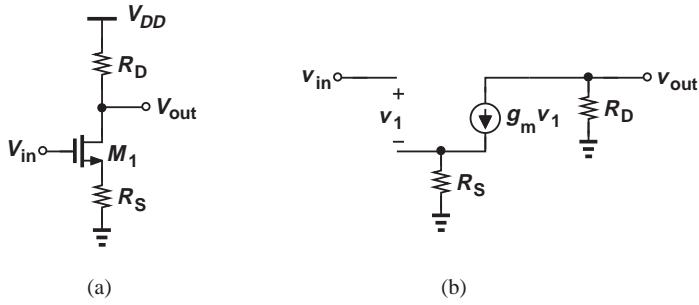


Figure 7.14 (a) CS stage with degeneration, (b) small-signal model.

Figure 7.14 depicts the stage along with its small-signal equivalent (if $\lambda = 0$). As with the bipolar counterpart, the degeneration resistor sustains a fraction of the input voltage change. From Fig. 7.14(b), we have

$$v_{in} = v_1 + g_m v_1 R_S \quad (7.64)$$

and hence

$$v_1 = \frac{v_{in}}{1 + g_m R_S}. \quad (7.65)$$

Since $g_m v_1$ flows through R_D , $v_{out} = -g_m v_1 R_D$ and

$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_D}{1 + g_m R_S} \quad (7.66)$$

$$= -\frac{\frac{R_D}{1 + g_m R_S}}{\frac{g_m}{g_m + R_S}}, \quad (7.67)$$

a result identical to that expressed by Eq. (5.157) for the bipolar counterpart.

**Example
7.8**

Compute the voltage gain of the circuit shown in Fig. 7.15(a) if $\lambda = 0$.

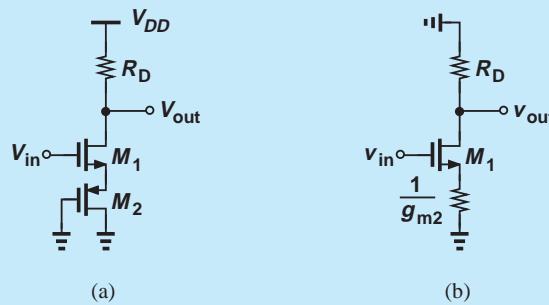


Figure 7.15 (a) Example of CS stage with degeneration, (b) simplified circuit.

Solution Transistor M_2 serves as a diode-connected device, presenting an impedance of $1/g_{m2}$ [Fig. 7.15(b)]. The gain is therefore given by Eq. (7.67) if R_S is replaced with $1/g_{m2}$:

$$A_v = -\frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}. \quad (7.68)$$

Exercise What happens if $\lambda \neq 0$ for M_2 ?

In parallel with the developments in Chapter 5, we may study the effect of a resistor appearing in series with the gate (Fig. 7.16). However, since the gate current is zero (at low frequencies), R_G sustains no voltage drop and does not affect the voltage gain or the I/O impedances.

Effect of Transistor Output Impedance As with the bipolar counterparts, the inclusion of the transistor output impedance complicates the analysis and is studied in Problem 7.32. Nonetheless, the output impedance of the degenerated CS stage plays a critical role in analog design and is worth studying here.

Figure 7.17 shows the small-signal equivalent of the circuit. Since R_S carries a current equal to i_X (why?), we have $v_1 = -i_X R_S$. Also, the current through r_O is equal to

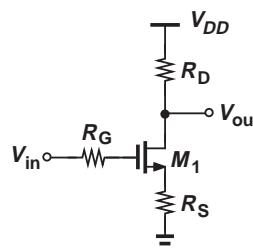


Figure 7.16 CS stage with gate resistance.

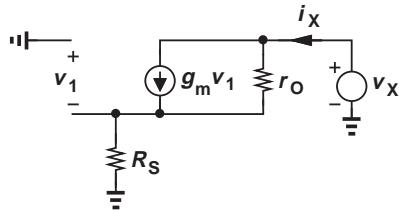


Figure 7.17 Output impedance of CS stage with degeneration.

$i_X - g_m v_1 = i_X - g_m(-i_X R_S) = i_X + g_m i_X R_S$. Adding the voltage drops across r_O and R_S and equating the result to v_X , we have

$$r_O(i_X + g_m i_X R_S) + i_X R_S = v_X, \quad (7.69)$$

and hence

$$\frac{v_X}{i_X} = r_O(1 + g_m R_S) + R_S \quad (7.70)$$

$$= (1 + g_m r_O)R_S + r_O \quad (7.71)$$

$$\approx g_m r_O R_S + r_O. \quad (7.72)$$

Alternatively, we observe that the model in Fig. 7.17 is similar to its bipolar counterpart in Fig. 5.46(a) but with $r_\pi = \infty$. Letting $r_\pi \rightarrow \infty$ in Eqs. (5.196) and (5.197) yields the same results as above. As expected from our study of the bipolar degenerated stage, the MOS version also exhibits a “boosted” output impedance.

**Example
7.9**

Compute the output resistance of the circuit in Fig. 7.18(a) if M_1 and M_2 are identical.

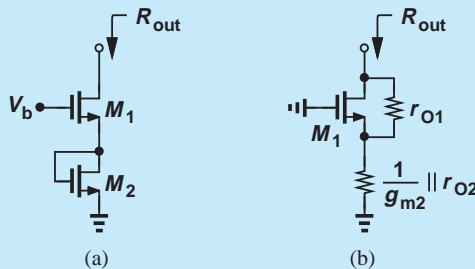


Figure 7.18 (a) Example of CS stage with degeneration, (b) simplified circuit.

Solution The diode-connected device M_2 can be represented by a small-signal resistance of $(1/g_{m2})||r_{O2} \approx 1/g_{m2}$. Transistor M_1 is degenerated by this resistance, and from Eq. (7.70):

$$R_{out} = r_{O1} \left(1 + g_{m1} \frac{1}{g_{m2}} \right) + \frac{1}{g_{m2}} \quad (7.73)$$

which, since $g_{m1} = g_{m2} = g_m$, reduces to

$$R_{out} = 2r_{O1} + \frac{1}{g_m} \quad (7.74)$$

$$\approx 2r_{O1}. \quad (7.75)$$

Exercise Do the results remain unchanged if M_2 is replaced with a diode-connected PMOS device?

**Example
7.10**

Determine the output resistance of the circuit in Fig. 7.19(a) and compare the result with that in the above example. Assume M_1 and M_2 are in saturation.

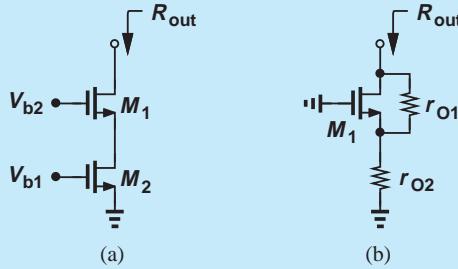


Figure 7.19 (a) Example of CS stage with degeneration, (b) simplified circuit.

Solution With its gate-source voltage fixed, transistor M_2 operates as a current source, introducing a resistance of r_{O2} from the source of M_1 to ground [Fig. 7.19(b)].

Equation (7.71) can therefore be written as

$$R_{out} = (1 + g_{m1}r_{O1})r_{O2} + r_{O1} \quad (7.76)$$

$$\approx g_{m1}r_{O1}r_{O2} + r_{O1}. \quad (7.77)$$

Assuming $g_{m1}r_{O2} \gg 1$ (which is valid in practice), we have

$$R_{out} \approx g_{m1}r_{O1}r_{O2}. \quad (7.78)$$

We observe that this value is quite higher than that in Eq. (7.75).

Exercise Repeat the above example for the PMOS counterpart of the circuit.

7.2.5 CS Core With Biasing

The effect of the simple biasing network shown in Fig. 7.1 is similar to that analyzed for the bipolar stage in Chapter 5. Depicted in Fig. 7.20(a) along with an input coupling capacitor (assumed a short circuit), such a circuit no longer exhibits an infinite input impedance:

$$R_{in} = R_1 || R_2. \quad (7.79)$$

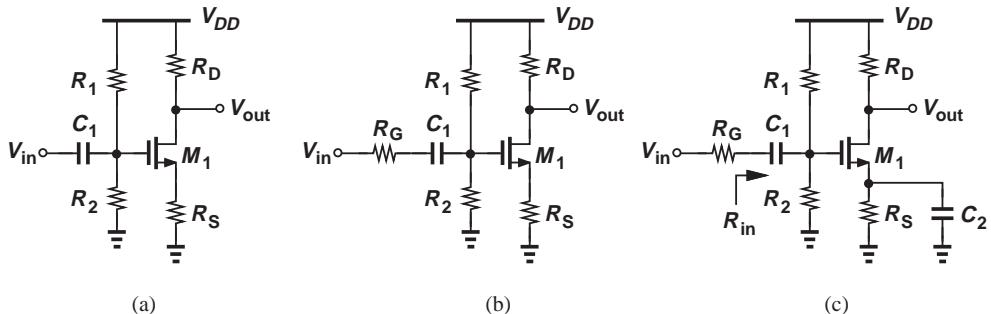


Figure 7.20 (a) CS stage with input coupling capacitor, (b) inclusion of gate resistance, (c) use of bypass capacitor.

Thus, if the circuit is driven by a finite source impedance [Fig. 7.20(b)], the voltage gain falls to

$$A_v = \frac{R_1 || R_2}{R_G + R_1 || R_2} \cdot \frac{-R_D}{\frac{1}{g_m} + R_S}, \quad (7.80)$$

where λ is assumed to be zero.

As mentioned in Chapter 5, it is possible to utilize degeneration for bias point stability but eliminate its effect on the small-signal performance by means of a bypass capacitor [Fig. 7.20(c)]. Unlike the case of bipolar realization, this does not alter the input impedance of the CS stage:

$$R_{in} = R_1 || R_2, \quad (7.81)$$

but raises the voltage gain:

$$A_v = -\frac{R_1 || R_2}{R_G + R_1 || R_2} g_m R_D. \quad (7.82)$$

Example 7.11

Design the CS stage of Fig. 7.20(c) for a voltage gain of 5, an input impedance of $50 \text{ k}\Omega$, and a power budget of 5 mW. Assume $\mu_n C_{ox} = 100 \mu\text{A}/\text{V}^2$, $V_{TH} = 0.5 \text{ V}$, $\lambda = 0$, and $V_{DD} = 1.8 \text{ V}$. Also, assume a voltage drop of 400 mV across R_S .

Solution

The power budget along with $V_{DD} = 1.8 \text{ V}$ implies a maximum supply current of 2.78 mA. As an initial guess, we allocate 2.7 mA to M_1 and the remaining 80 μA to R_1 and R_2 . It follows that

$$R_S = 148 \Omega. \quad (7.83)$$

As with typical design problems, the choice of g_m and R_D is somewhat flexible so long as $g_m R_D = 5$. However, with I_D known, we must ensure a reasonable value for V_{GS} , e.g., $V_{GS} = 1 \text{ V}$. This choice yields

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}} \quad (7.84)$$

$$= \frac{1}{92.6 \Omega}, \quad (7.85)$$

and hence

$$R_D = 463 \Omega. \quad (7.86)$$

Writing

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (7.87)$$

gives

$$\frac{W}{L} = 216. \quad (7.88)$$

With $V_{GS} = 1$ V and a 400-mV drop across R_S , the gate voltage reaches 1.4 V, requiring that

$$\frac{R_2}{R_1 + R_2} V_{DD} = 1.4 \text{ V}, \quad (7.89)$$

which, along with $R_{in} = R_1 || R_2 = 50 \text{ k}\Omega$, yields

$$R_1 = 64.3 \text{ k}\Omega \quad (7.90)$$

$$R_2 = 225 \text{ k}\Omega. \quad (7.91)$$

We must now check to verify that M_1 indeed operates in saturation. The drain voltage is given by $V_{DD} - I_D R_D = 1.8 \text{ V} - 1.25 \text{ V} = 0.55 \text{ V}$. Since the gate voltage is equal to 1.4 V, the gate-drain voltage difference exceeds V_{TH} , driving M_1 into the triode region!

How did our design procedure lead to this result? For the given I_D , we have chosen an excessively large R_D , i.e., an excessively small g_m (because $g_m R_D = 5$), even though V_{GS} is reasonable. We must therefore increase g_m so as to allow a lower value for R_D . For example, suppose we halve R_D and double g_m by increasing W/L by a factor of four:

$$\frac{W}{L} = 864 \quad (7.92)$$

$$g_m = \frac{1}{46.3 \Omega}. \quad (7.93)$$

The corresponding gate-source voltage is obtained from (7.84):

$$V_{GS} = 250 \text{ mV}, \quad (7.94)$$

yielding a gate voltage of 650 mV.

Is M_1 in saturation? The drain voltage is equal to $V_{DD} - R_D I_D = 1.17 \text{ V}$, a value higher than the gate voltage minus V_{TH} . Thus, M_1 operates in saturation.

Exercise Repeat the above example for a power budget of 3 mW and $V_{DD} = 1.2 \text{ V}$.

7.3

COMMON-GATE STAGE

Shown in Fig. 7.21, the CG topology resembles the common-base stage studied in Chapter 5. Here, if the input rises by a small value, ΔV , then the gate-source voltage of M_1 decreases by the same amount, thereby lowering the drain current by $g_m \Delta V$ and

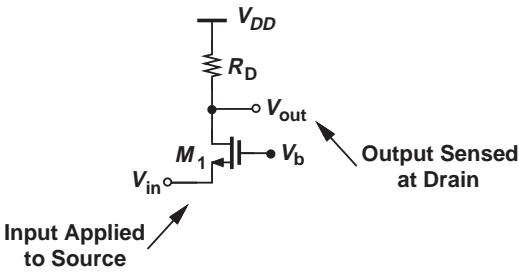


Figure 7.21 Common-gate stage.

raising V_{out} by $g_m \Delta V R_D$. That is, the voltage gain is positive and equal to

$$A_v = g_m R_D. \quad (7.95)$$

The CG stage suffers from voltage headroom-gain trade-offs similar to those of the CB topology. In particular, to achieve a high gain, a high I_D or R_D is necessary, but the drain voltage, $V_{DD} - I_D R_D$, must remain above $V_b - V_{TH}$ to ensure M_1 is saturated.

**Example
7.12**

A microphone having a dc level of zero drives a CG stage biased at $I_D = 0.5$ mA. If $W/L = 50$, $\mu_n C_{ox} = 100 \mu\text{A}/\text{V}^2$, $V_{TH} = 0.5$ V, and $V_{DD} = 1.8$ V, determine the maximum allowable value of R_D and hence the maximum voltage gain. Neglect channel-length modulation.

Solution With W/L known, the gate-source voltage can be determined from

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (7.96)$$

as

$$V_{GS} = 0.947 \text{ V}. \quad (7.97)$$

For M_1 to remain in saturation,

$$V_{DD} - I_D R_D > V_b - V_{TH} \quad (7.98)$$

and hence

$$R_D < 2.71 \text{ k}\Omega. \quad (7.99)$$

Also, the above value of W/L and I_D yield $g_m = (447 \Omega)^{-1}$ and

$$A_v \leq 6.06. \quad (7.100)$$

Figure 7.22 summarizes the allowable signal levels in this design. The gate voltage can be generated using a resistive divider similar to that in Fig. 7.20(a).

Exercise

If a gain of 10 is required, what value should be chosen for W/L ?

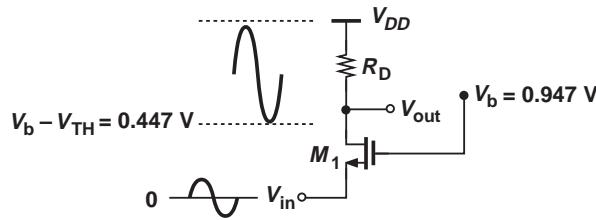


Figure 7.22 Signal levels in CG stage.

We now compute the I/O impedances of the CG stage, expecting to obtain results similar to those of the CB topology. Neglecting channel-length modulation for now, we have from Fig. 7.23(a) $v_1 = -v_X$ and

$$i_X = -g_m v_1 \quad (7.101)$$

$$= g_m v_X. \quad (7.102)$$

That is,

$$R_{in} = \frac{1}{g_m}, \quad (7.103)$$

a relatively *low* value. Also, from Fig. 7.23(b), $v_1 = 0$ and hence

$$R_{out} = R_D, \quad (7.104)$$

an expected result because the circuits of Figs. 7.23(b) and 7.7 are identical.

Let us study the behavior of the CG stage in the presence of a finite source impedance (Fig. 7.24) but still with $\lambda = 0$. In a manner similar to that depicted in Chapter 5 for the CB topology, we write

$$v_X = \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_S} v_{in} \quad (7.105)$$

$$= \frac{1}{1 + g_m R_S} v_{in}. \quad (7.106)$$

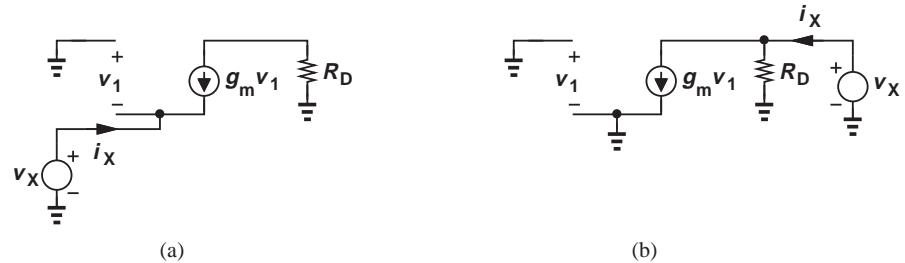


Figure 7.23 (a) Input and (b) output impedances of CG stage.

Did you know?

The common-gate stage is sometimes used as a low-noise RF amplifier, e.g., at the input of your WiFi receiver. This topology is attractive because its low input impedance allows simple “impedance matching” with the antenna. However, with the reduction of the intrinsic gain, $g_m r_o$, as a result of scaling, the input impedance, R_{in} , is now too high! It can be shown that with channel-length modulation

$$R_{in} = \frac{R_D + r_o}{1 + g_m r_o}$$

which reduces to $1/g_m$ if $g_m r_o \gg 1$ and $R_D \ll r_o$. Since neither of these conditions holds anymore, the CG stage presents new challenges to RF designers.

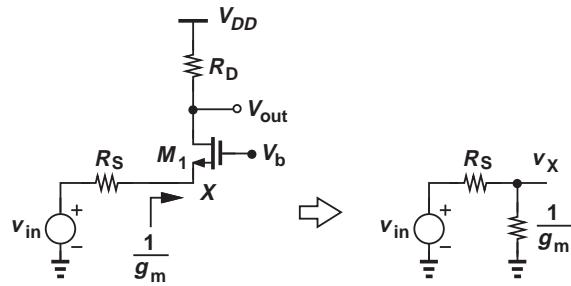


Figure 7.24 Simplification of CG stage with signal source resistance.

Thus,

$$\frac{v_{out}}{v_{in}} = \frac{v_{out}}{v_X} \cdot \frac{v_X}{v_{in}} \quad (7.107)$$

$$= \frac{g_m R_D}{1 + g_m R_S} \quad (7.108)$$

$$= \frac{R_D}{\frac{1}{g_m} + R_S}. \quad (7.109)$$

The gain is therefore equal to that of the degenerated CS stage except for a negative sign.

In contrast to the common-source stage, the CG amplifier exhibits a current gain of unity: the current provided by the input voltage source simply flows through the channel and emerges from the drain node.

The analysis of the common-gate stage in the general case, i.e., including both channel-length modulation and a finite source impedance, is beyond the scope of this book (Problem 7.42). However, we can make two observations. First, a resistance appearing in series with the gate terminal [Fig. 7.25(a)] does not alter the gain or I/O impedances (at low frequencies) because it sustains a zero potential drop—as if its value were zero. Second, the output resistance of the CG stage in the general case [Fig. 7.25(b)] is identical to that of the degenerated CS topology:

$$R_{out} = (1 + g_m r_O) R_S + r_O. \quad (7.110)$$

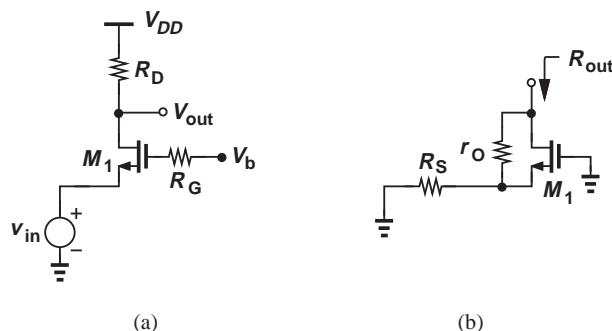


Figure 7.25 (a) CG stage with gate resistance, (b) output resistance of CG stage.

**Example
7.13**

For the circuit shown in Fig. 7.26(a), calculate the voltage gain if $\lambda = 0$ and the output impedance if $\lambda > 0$.

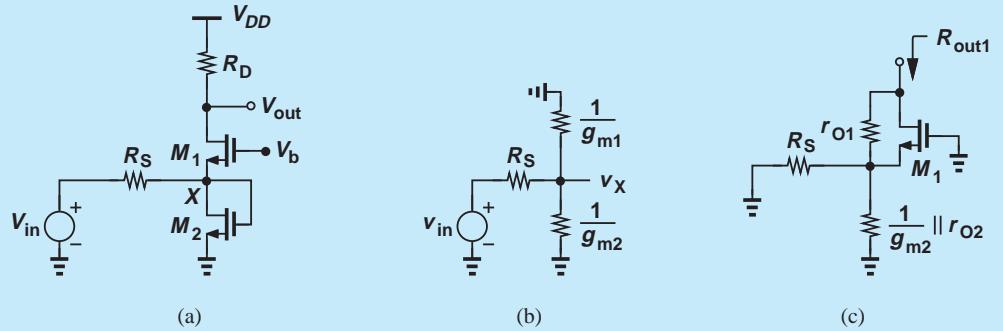


Figure 7.26 (a) Example of CG stage, (b) equivalent input network, (c) calculation of output resistance.

Solution We first compute v_X/v_{in} with the aid of the equivalent circuit depicted in Fig. 7.26(b):

$$\frac{v_X}{v_{in}} = \frac{\frac{1}{g_{m2}} \parallel \frac{1}{g_{m1}}}{\frac{1}{g_{m2}} \parallel \frac{1}{g_{m1}} + R_S} \quad (7.111)$$

$$= \frac{1}{1 + (g_{m1} + g_{m2})R_S}. \quad (7.112)$$

Noting that $v_{out}/v_X = g_{m1}R_D$, we have

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}R_D}{1 + (g_{m1} + g_{m2})R_S}. \quad (7.113)$$

To compute the output impedance, we first consider R_{out1} , as shown in Fig. 7.26(c), which from Eq. (7.110) is equal to

$$R_{out1} = (1 + g_{m1}r_{O1}) \left(\frac{1}{g_{m2}} || r_{O2} || R_S \right) + r_{O1} \quad (7.114)$$

$$\approx g_{m1}r_{O1} \left(\frac{1}{g_{m2}} || R_S \right) + r_{O1}. \quad (7.115)$$

The overall output impedance is then given by

$$R_{out} = R_{out1} || R_D \quad (7.116)$$

$$\approx \left[g_{m1}r_{O1} \left(\frac{1}{g_{m2}} || R_S \right) + r_{O1} \right] || R_D. \quad (7.117)$$

Exercise Calculate the output impedance if the gate of M_2 is tied to a constant voltage.

7.3.1 CG Stage With Biasing

Following our study of the CB biasing in Chapter 5, we surmise the CG amplifier can be biased as shown in Fig. 7.27. Providing a path for the bias current to ground, resistor R_3 lowers the input impedance—and hence the voltage gain—if the signal source exhibits a finite output impedance, R_S .

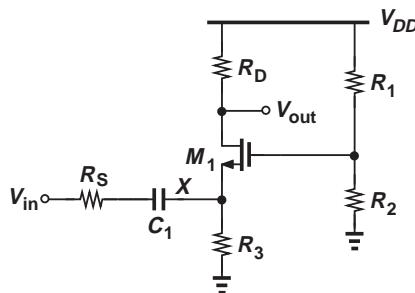


Figure 7.27 CG stage with biasing.

Since the impedance seen to the right of node X is equal to $R_3||(1/g_m)$, we have

$$\frac{v_{out}}{v_{in}} = \frac{v_X}{v_{in}} \cdot \frac{v_{out}}{v_X} \quad (7.118)$$

$$= \frac{R_3||(1/g_m)}{R_3||(1/g_m) + R_S} \cdot g_m R_D, \quad (7.119)$$

where channel-length modulation is neglected. As mentioned earlier, the voltage divider consisting of R_1 and R_2 does not affect the small-signal behavior of the circuit (at low frequencies).

**Example
7.14**

Design the common-gate stage of Fig. 7.27 for the following parameters: $v_{out}/v_{in} = 5$, $R_S = 0$, $R_3 = 500 \Omega$, $1/g_m = 50 \Omega$, power budget = 2 mW, $V_{DD} = 1.8$ V. Assume $\mu_n C_{ox} = 100 \mu\text{A/V}^2$, $V_{TH} = 0.5$ V, and $\lambda = 0$.

Solution From the power budget, we obtain a total supply current of 1.11 mA. Allocating 10 μA to the voltage divider, R_1 and R_2 , we leave 1.1 mA for the drain current of M_1 . Thus, the voltage drop across R_3 is equal to 550 mV.

We must now compute two interrelated parameters: W/L and R_D . A larger value of W/L yields a greater g_m , allowing a lower value of R_D . As in Example 7.11, we choose an initial value for V_{GS} to arrive at a reasonable guess for W/L . For example, if $V_{GS} = 0.8$ V, then $W/L = 244$, and $g_m = 2I_D/(V_{GS} - V_{TH}) = (136.4 \Omega)^{-1}$, dictating $R_D = 682 \Omega$ for $v_{out}/v_{in} = 5$.

Let us determine whether M_1 operates in saturation. The gate voltage is equal to V_{GS} plus the drop across R_3 , amounting to 1.35 V. On the other hand, the drain voltage is given by $V_{DD} - I_D R_D = 1.05$ V. Since the drain voltage exceeds $V_G - V_{TH}$, M_1 is indeed in saturation.

The resistive divider consisting of R_1 and R_2 must establish a gate voltage equal to 1.35 V while drawing 10 μA :

$$\frac{V_{DD}}{R_1 + R_2} = 10 \mu\text{A} \quad (7.120)$$

$$\frac{R_2}{R_1 + R_2} V_{DD} = 1.35 \text{ V}. \quad (7.121)$$

It follows that $R_1 = 45 \text{ k}\Omega$ and $R_2 = 135 \text{ k}\Omega$.

Exercise If W/L cannot exceed 100, what voltage gain can be achieved?

**Example
7.15**

Suppose in Example 7.14, we wish to minimize W/L (and hence transistor capacitances). What is the minimum acceptable value of W/L ?

Solution For a given I_D , as W/L decreases, $V_{GS} - V_{TH}$ increases. Thus, we must first compute the maximum allowable V_{GS} . We impose the condition for saturation as

$$V_{DD} - I_D R_D > V_{GS} + V_{R3} - V_{TH}, \quad (7.122)$$

where V_{R3} denotes the voltage drop across R_3 , and set $g_m R_D$ to the required gain:

$$\frac{2I_D}{V_{GS} - V_{TH}} R_D = A_v. \quad (7.123)$$

Eliminating R_D from Eqs. (7.122) and (7.123) gives:

$$V_{DD} - \frac{A_v}{2}(V_{GS} - V_{TH}) > V_{GS} - V_{TH} + V_{R3} \quad (7.124)$$

and hence

$$V_{GS} - V_{TH} < \frac{V_{DD} - V_{R3}}{\frac{A_v}{2} + 1}. \quad (7.125)$$

In other words,

$$W/L > \frac{2I_D}{\mu_n C_{ox} \left(2 \frac{V_{DD} - V_{R3}}{A_v + 2} \right)^2}. \quad (7.126)$$

It follows that

$$W/L > 172.5. \quad (7.127)$$

Exercise Repeat the above example for $A_v = 10$.

7.4

SOURCE FOLLOWER

The MOS counterpart of the emitter follower is called the “source follower” (or the “common-drain” stage) and shown in Fig. 7.28. The amplifier senses the input at the gate and produces the output at the source, with the drain tied to V_{DD} . The circuit’s behavior is similar to that of the bipolar counterpart.

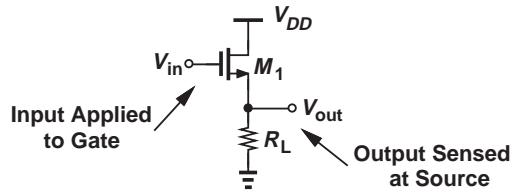


Figure 7.28 Source follower.

7.4.1 Source Follower Core

If the gate voltage of M_1 in Fig. 7.28 is raised by a small amount, ΔV_{in} , the gate-source voltage tends to increase, thereby raising the source current and hence the output voltage. Thus, V_{out} “follows” V_{in} . Since the dc level of V_{out} is lower than that of V_{in} by V_{GS} , we say the follower can serve as a “level shift” circuit. From our analysis of emitter followers in Chapter 5, we expect this topology to exhibit a subunity gain, too.

Figure 7.29(a) depicts the small-signal equivalent of the source follower, including channel-length modulation. Recognizing that r_O appears in parallel with R_L , we have

$$g_m v_1 (r_O || R_L) = v_{out}. \quad (7.128)$$

Also,

$$v_{in} = v_1 + v_{out}. \quad (7.129)$$

It follows that

$$\frac{v_{out}}{v_{in}} = \frac{g_m (r_O || R_L)}{1 + g_m (r_O || R_L)} \quad (7.130)$$

$$= \frac{r_O || R_L}{\frac{1}{g_m} + r_O || R_L}. \quad (7.131)$$

The voltage gain is therefore positive and less than unity. It is desirable to maximize R_L (and r_O).

As with emitter followers, we can view the above result as voltage division between a resistance equal to $1/g_m$ and another equal to $r_O || R_L$ [Fig. 7.29(b)]. Note, however, that a resistance placed in series with the gate does not affect Eq. (7.131) (at low frequencies) because it sustains a zero drop.

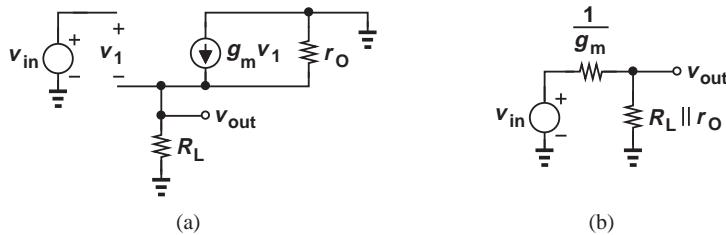


Figure 7.29 (a) Small-signal equivalent of source follower, (b) simplified circuit.

**Example
7.16**

A source follower is realized as shown in Fig. 7.30(a), where M_2 serves as a current source. Calculate the voltage gain of the circuit.

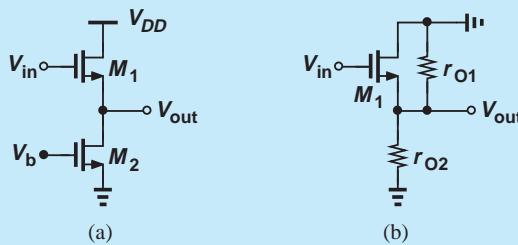


Figure 7.30 (a) Follower with ideal current source, (b) simplified circuit.

Solution Since M_2 simply presents an impedance of r_{O2} from the output node to ac ground [Fig. 7.30(b)], we substitute $R_L = r_{O2}$ in Eq. (7.131):

$$A_v = \frac{r_{O1}||r_{O2}}{\frac{1}{g_m} + r_{O1}||r_{O2}}. \quad (7.132)$$

If $r_{O1}||r_{O2} \gg 1/g_m$, then $A_v \approx 1$.

Exercise Repeat the above example if a resistance of value R_S is placed in series with the source of M_2 .

**Example
7.17**

Design a source follower to drive a $50\text{-}\Omega$ load with a voltage gain of 0.5 and a power budget of 10 mW . Assume $\mu_nC_{ox} = 100\text{ }\mu\text{A/V}^2$, $V_{TH} = 0.5\text{ V}$, $\lambda = 0$, and $V_{DD} = 1.8\text{ V}$.

Solution With $R_L = 50\text{ }\Omega$ and $r_O = \infty$ in Fig. 7.28, we have

$$A_v = \frac{R_L}{\frac{1}{g_m} + R_L} \quad (7.133)$$

and hence

$$g_m = \frac{1}{50\text{ }\Omega}. \quad (7.134)$$

The power budget and supply voltage yield a maximum supply current of 5.56 mA . Using this value for I_D in $g_m = \sqrt{2\mu_nC_{ox}(W/L)I_D}$ gives

$$W/L = 360. \quad (7.135)$$

Exercise What voltage gain can be achieved if the power budget is raised to 15 mW ?

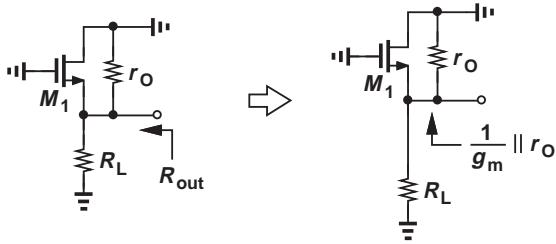


Figure 7.31 Output resistance of source follower.

It is instructive to compute the output impedance of the source follower.² As illustrated in Fig. 7.31, R_{out} consists of the resistance seen looking up into the source in parallel with that seen looking down into R_L . With $\lambda \neq 0$, the former is equal to $(1/g_m) \parallel r_O$, yielding

$$R_{out} = \frac{1}{g_m} \parallel r_O \parallel R_L \quad (7.136)$$

$$\approx \frac{1}{g_m} \parallel R_L. \quad (7.137)$$

In summary, the source follower exhibits a very high input impedance and a relatively low output impedance, thereby providing buffering capability.

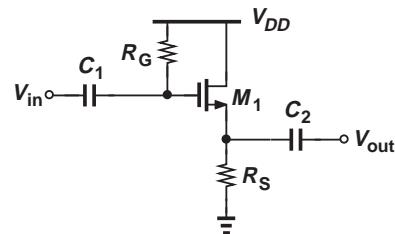


Figure 7.32 Source follower with input and output coupling capacitors.

7.4.2 Source Follower With Biasing

The biasing of source followers is similar to that of emitter followers (Chapter 5). Figure 7.32 depicts an example where R_G establishes a dc voltage equal to V_{DD} at the gate of M_1 (why?) and R_S sets the drain bias current. Note that M_1 operates in saturation because the gate and drain voltages are equal. Also, the input impedance of the circuit has dropped from infinity to R_G .

Let us compute the bias current of the circuit. With a zero voltage drop across R_G , we have

$$V_{GS} + I_D R_S = V_{DD}. \quad (7.138)$$

²The input impedance is infinite at low frequencies.

Neglecting channel-length modulation, we write

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (7.139)$$

$$= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{DD} - I_D R_S - V_{TH})^2. \quad (7.140)$$

The resulting quadratic equation can be solved to obtain I_D .

**Example
7.18**

Design the source follower of Fig. 7.32 for a drain current of 1 mA and a voltage gain of 0.8. Assume $\mu_n C_{ox} = 100 \mu\text{A/V}^2$, $V_{TH} = 0.5 \text{ V}$, $\lambda = 0$, $V_{DD} = 1.8 \text{ V}$, and $R_G = 50 \text{ k}\Omega$.

Solution The unknowns in this problem are V_{GS} , W/L , and R_S . The following three equations can be formed:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (7.141)$$

$$I_D R_S + V_{GS} = V_{DD} \quad (7.142)$$

$$A_v = \frac{R_S}{\frac{1}{g_m} + R_S}. \quad (7.143)$$

If g_m is written as $2I_D/(V_{GS} - V_{TH})$, then Eqs. (7.142) and (7.143) do not contain W/L and can be solved to determine V_{GS} and R_S . With the aid of Eq. (7.142), we write Eq. (7.143) as

$$A_v = \frac{R_S}{\frac{V_{GS} - V_{TH}}{2I_D} + R_S} \quad (7.144)$$

$$= \frac{2I_D R_S}{V_{GS} - V_{TH} + 2I_D R_S} \quad (7.145)$$

$$= \frac{2I_D R_S}{V_{DD} - V_{TH} + I_D R_S}. \quad (7.146)$$

Thus,

$$R_S = \frac{V_{DD} - V_{TH}}{I_D} \frac{A_v}{2 - A_v} \quad (7.147)$$

$$= 867 \Omega. \quad (7.148)$$

and

$$V_{GS} = V_{DD} - I_D R_S \quad (7.149)$$

$$= V_{DD} - (V_{DD} - V_{TH}) \frac{A_v}{2 - A_v} \quad (7.150)$$

$$= 0.933 \text{ V}. \quad (7.151)$$

It follows from Eq. (7.141) that

$$\frac{W}{L} = 107. \quad (7.152)$$

Exercise What voltage gain can be achieved if W/L cannot exceed 50?

Equation (7.140) reveals that the bias current of the source follower varies with the supply voltage. To avoid this effect, integrated circuits bias the follower by means of a current source (Fig. 7.33).

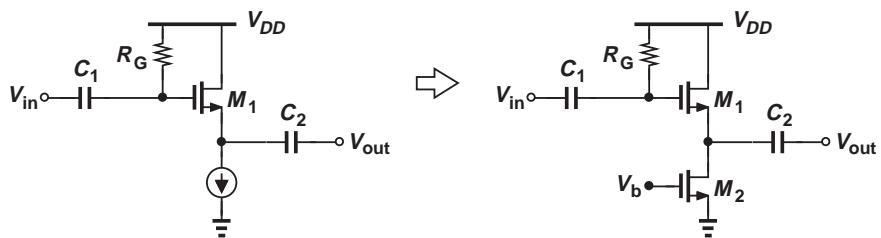


Figure 7.33 Source follower with biasing.

7.5

SUMMARY AND ADDITIONAL EXAMPLES

In this chapter, we have studied three basic CMOS building blocks, namely, the common-source stage, the common-gate stage, and the source follower. As observed throughout the chapter, the small-signal behavior of these circuits is quite similar to that of their bipolar counterparts, with the exception of the high impedance seen at the gate terminal. We have noted that the biasing schemes are also similar, with the quadratic I_D - V_{GS} relationship supplanting the exponential I_C - V_{BE} characteristic.

In this section, we consider a number of additional examples to solidify the concepts introduced in this chapter, emphasizing analysis by inspection.

Example 7.19

Calculate the voltage gain and output impedance of the circuit shown in Fig. 7.34(a).

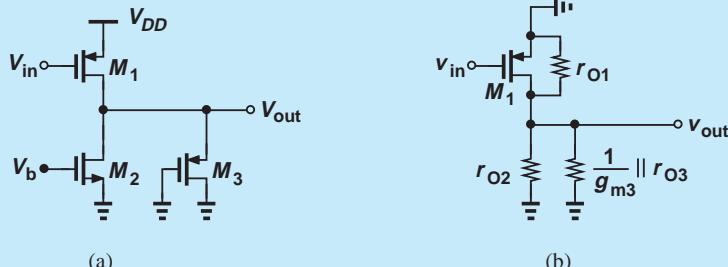


Figure 7.34 (a) Example of CS stage, (b) simplified circuit.

Solution We identify M_1 as a common-source device because it senses the input at its gate and generates the output at its drain. Transistors M_2 and M_3 therefore act as the load, with the former serving as a current source and the latter as a diode-connected device. Thus, M_2 can be replaced with a small-signal resistance equal to r_{O2} , and M_3 with another equal to $(1/g_{m3})||r_{O3}$. The circuit now reduces to that depicted in Fig. 7.34(b), yielding

$$A_v = -g_{m1} \left(\frac{1}{g_{m3}} || r_{O1} || r_{O2} || r_{O3} \right) \quad (7.153)$$

and

$$R_{out} = \frac{1}{g_{m3}} || r_{O1} || r_{O2} || r_{O3}. \quad (7.154)$$

Note that $1/g_{m3}$ is dominant in both expressions.

Exercise 7.20 Repeat the above example if M_2 is converted to a diode-connected device.

Example 7.20

Compute the voltage gain of the circuit shown in Fig. 7.35(a). Neglect channel-length modulation in M_1 .

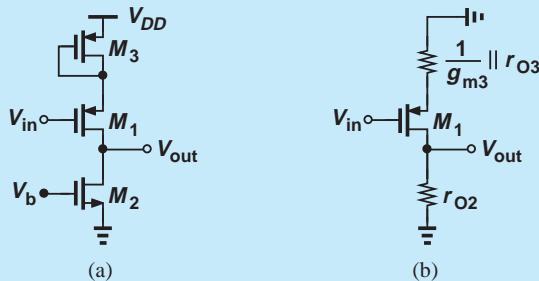


Figure 7.35 (a) Example of CS stage, (b) simplified circuit.

Solution Operating as a CS stage and degenerated by the diode-connected device M_3 , transistor M_1 drives the current-source load, M_2 . Simplifying the amplifier to that in Fig. 7.35(b), we have

$$A_v = -\frac{r_{O2}}{\frac{1}{g_{m1}} + \frac{1}{g_{m3}} || r_{O3}}. \quad (7.155)$$

Exercise Repeat the above example if the gate of M_3 is tied to a constant voltage.

**Example
7.21**

Determine the voltage gain of the amplifiers illustrated in Fig. 7.36. For simplicity, assume $r_{O1} = \infty$ in Fig. 7.36(b).

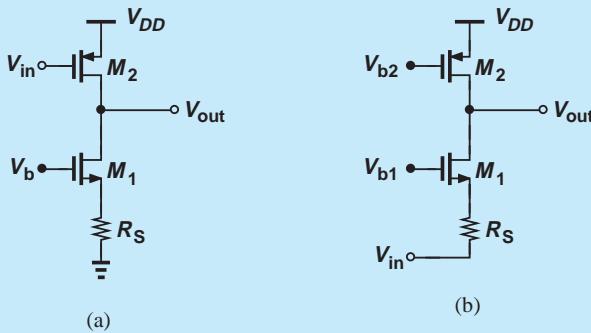


Figure 7.36 Examples of (a) CS and (b) CG stages.

Solution Degenerated by R_S , transistor M_1 in Fig. 7.36(a) presents an impedance of $(1 + g_{m1}r_{O1})R_S + r_{O1}$ to the drain of M_2 . Thus the total impedance seen at the drain is equal to $[(1 + g_{m1}r_{O1})R_S + r_{O1}]||r_{O2}$, giving a voltage gain of

$$A_v = -g_{m2}\{[(1 + g_{m1}r_{O1})R_S + r_{O1}]||r_{O2}\}. \quad (7.156)$$

In Fig. 7.36(b), M_1 operates as a common-gate stage and M_2 as the load, obtaining Eq. (7.109):

$$A_{v2} = \frac{r_{O2}}{\frac{1}{g_{m1}} + R_S}. \quad (7.157)$$

**Exercise
7.22**

Replace R_S with a diode-connected device and repeat the analysis.

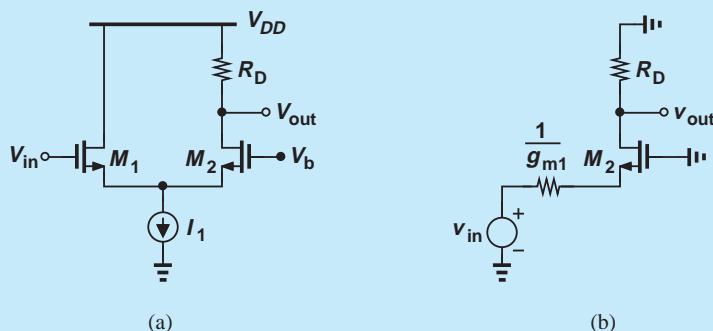


Figure 7.37 (a) Example of a composite stage, (b) simplified circuit.

Solution In this circuit, M_1 operates as a source follower and M_2 as a CG stage (why?). A simple method of analyzing the circuit is to replace v_{in} and M_1 with a Thevenin equivalent. From Fig. 7.29(b), we derive the model depicted in Fig. 7.37(b). Thus,

$$A_v = \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}. \quad (7.158)$$

Exercise What happens if a resistance of value R_1 is placed in series with the drain of M_1 ?

**Example
7.23**

The circuit of Fig. 7.38 produces two outputs. Calculate the voltage gain from the input to Y and to X . Assume $\lambda = 0$ for M_1 .

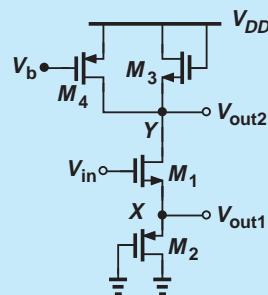


Figure 7.38 Example of composite stage.

Solution For V_{out1} , the circuit serves as a source follower. The reader can show that if $r_{O1} = \infty$, then M_3 and M_4 do not affect the source follower operation. Exhibiting a small-signal impedance of $(1/g_{m2})||r_{O2}$, transistor M_2 acts as a load for the follower, yielding from Eq. (7.131)

$$\frac{v_{out1}}{v_{in}} = \frac{\frac{1}{g_{m2}}||r_{O2}}{\frac{1}{g_{m2}}||r_{O2} + \frac{1}{g_{m1}}}. \quad (7.159)$$

For V_{out2} , M_1 operates as a degenerated CS stage with a drain load consisting of the diode-connected device M_3 and the current source M_4 . This load impedance is equal to $(1/g_{m3})||r_{O3}||r_{O4}$, resulting in

$$\frac{v_{out2}}{v_{in}} = -\frac{\frac{1}{g_{m3}}||r_{O3}||r_{O4}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}||r_{O2}}. \quad (7.160)$$

Exercise Which one of the two gains is higher? Explain intuitively why.

- The impedances seen looking into the gate, drain, and source of a MOSFET are equal to infinity, r_O (with source grounded), and $1/g_m$ (with gate grounded), respectively.
- In order to obtain the required small-signal MOS parameters such as g_m and r_O , the transistor must be “biased,” i.e., carry a certain drain current and sustain certain gate-source and drain-source voltages. Signals simply perturb these conditions.
- Biassing techniques establish the required gate voltage by means of a resistive path to the supply rails or the output node (self-biasing).
- With a single transistor, only three amplifier topologies are possible: common-source and common-gate stages and source followers.
- The CS stage provides a moderate voltage gain, a high input impedance, and a moderate output impedance.
- Source degeneration improves the linearity but lowers the voltage gain.
- Source degeneration raises the output impedance of CS stages considerably.
- The CG stage provides a moderate voltage gain, a low input impedance, and a moderate output impedance.
- The voltage gain expressions for CS and CG stages are similar but for a sign.
- The source follower provides a voltage gain less than unity, a high input impedance, and a low output impedance, serving as a good voltage buffer.

PROBLEMS

In the following problems, unless otherwise stated, assume $\mu_n C_{ox} = 200 \mu\text{A}/\text{V}^2$, $\mu_p C_{ox} = 100 \mu\text{A}/\text{V}^2$, $\lambda = 0$, and $V_{TH} = 0.4 \text{ V}$ for NMOS devices and -0.4 V for PMOS devices.

Sec. 7.1.2 Biasing

- 7.1.** In the circuit of Fig. 7.39, determine the maximum allowable value of W/L if M_1 must remain in saturation. Assume $\lambda = 0$.

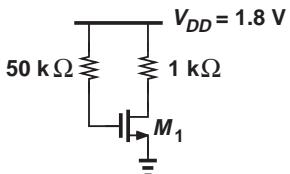


Figure 7.39

- 7.2.** We wish to design the circuit of Fig. 7.40 for a drain current of 1 mA. If $W/L = 20/0.18$, compute R_1 and R_2 such that the input impedance is at least 20 kΩ.

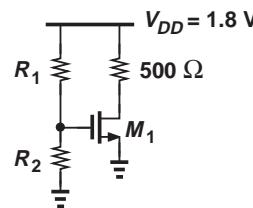


Figure 7.40

- 7.3.** Consider the circuit shown in Fig. 7.41. Calculate the maximum transconductance that M_1 can provide (without going into the triode region.)

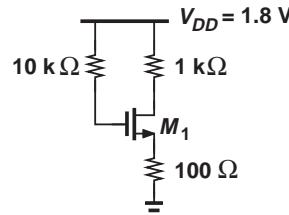


Figure 7.41

7.4. The circuit of Fig. 7.42 must be designed for a voltage drop of 200 mV across R_S .

- Calculate the minimum allowable value of W/L if M_1 must remain in saturation.
- What are the required values of R_1 and R_2 if the input impedance must be at least $30 \text{ k}\Omega$?

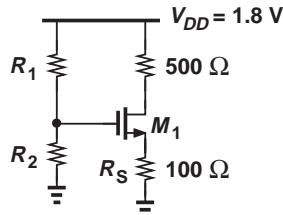


Figure 7.42

7.5. Consider the circuit depicted in Fig. 7.43, where $W/L = 20/0.18$. Assuming the current flowing through R_2 is one-tenth of I_{D1} , calculate the values of R_1 and R_2 so that $I_{D1} = 0.5 \text{ mA}$.

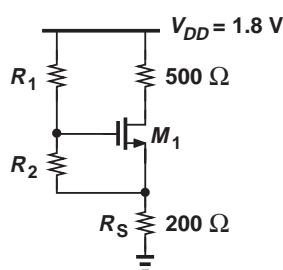


Figure 7.43

7.6. The self-biased stage of Fig. 7.44 must be designed for a drain current of 1 mA. If M_1 is to provide a transconductance of $1/(100 \Omega)$, calculate the required value of R_D .

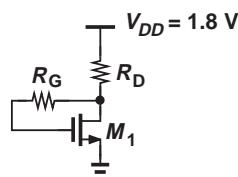


Figure 7.44

7.7. We wish to design the stage in Fig. 7.45 for a drain current of 0.5 mA. If $W/L = 50/0.18$, calculate the values of R_1 and R_2 such that these resistors carry a current equal to one-tenth of I_{D1} .

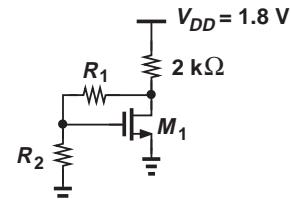


Figure 7.45

***7.8.** Due to a manufacturing error, a parasitic resistor, R_P has appeared in the circuit of Fig. 7.46. We know that circuit samples free from this error exhibit $V_{GS} = V_{DS} + 100 \text{ mV}$ whereas defective samples exhibit $V_{GS} = V_{DS} + 50 \text{ mV}$. Determine the values of W/L and R_P .

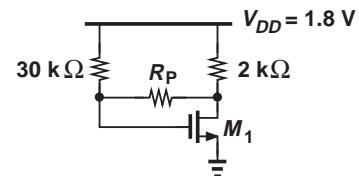


Figure 7.46

***7.9.** Due to a manufacturing error, a parasitic resistor, R_P has appeared in the circuit of Fig. 7.47. We know that circuit samples free from this error exhibit $V_{GS} = V_{DS}$ whereas defective samples exhibit $V_{GS} = V_{DS} + V_{TH}$. Determine the values of W/L and R_P if the drain current is 1 mA without R_P .

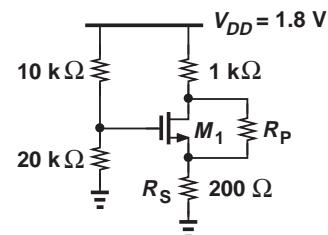


Figure 7.47

Sec. 7.1.3 Realization of Current Sources

- 7.10.** In the circuit of Fig. 7.48, M_1 and M_2 have lengths equal to $0.25 \mu\text{m}$ and $\lambda = 0.1 \text{ V}^{-1}$. Determine W_1 and W_2 such that $I_X = 2I_Y = 1 \text{ mA}$. Assume $V_{DS1} = V_{DS2} = V_B = 0.8 \text{ V}$. What is the output resistance of each current source?

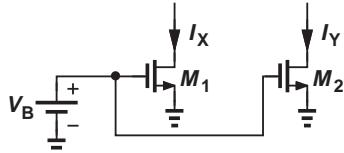


Figure 7.48

- 7.11.** An NMOS current source must be designed for an output resistance of $20 \text{ k}\Omega$ and an output current of 0.5 mA . What is the maximum tolerable value of λ ?

- 7.12.** The two current sources in Fig. 7.49 must be designed for $I_X = I_Y = 0.5 \text{ mA}$. If $V_{B1} = 1 \text{ V}$, $V_{B2} = 1.2 \text{ V}$, $\lambda = 0.1 \text{ V}^{-1}$, and $L_1 = L_2 = 0.25 \mu\text{m}$, calculate W_1 and W_2 . Compare the output resistances of the two current sources.

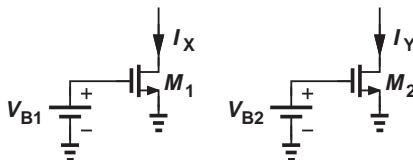


Figure 7.49

- 7.13.** Consider the circuit shown in Fig. 7.50, where $(W/L)_1 = 10/0.18$ and $(W/L)_2 = 30/0.18$. If $\lambda = 0.1 \text{ V}^{-1}$, calculate V_B such that $V_X = 0.9 \text{ V}$.

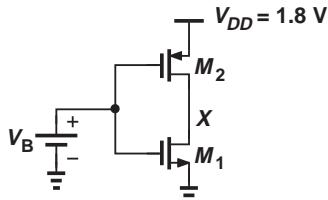


Figure 7.50

- 7.14.** In the circuit of Fig. 7.51, M_1 and M_2 serve as current sources. Calculate I_X and I_Y if $V_B = 1 \text{ V}$ and $W/L = 20/0.25$. How are the output resistances of M_1 and M_2 related?

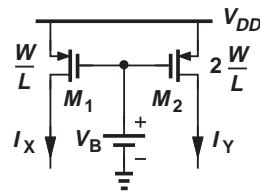


Figure 7.51

- *7.15.** A student mistakenly uses the circuit of Fig. 7.52 as a current source. If $W/L = 10/0.25$, $\lambda = 0.1 \text{ V}^{-1}$, $V_{B1} = 0.2 \text{ V}$, and V_X has a dc level of 1.2 V , calculate the impedance seen at the source of M_1 .

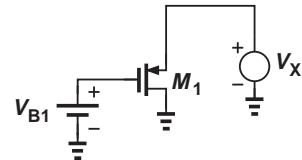


Figure 7.52

- *7.16.** In the circuit of Fig. 7.53, $(W/L)_1 = 5/0.18$, $(W/L)_2 = 10/0.18$, $\lambda_1 = 0.1 \text{ V}^{-1}$, and $\lambda_2 = 0.15 \text{ V}^{-1}$.

- (a) Determine V_B such that $|I_{D1}| = |I_{D2}| = 0.5 \text{ mA}$ for $V_X = 0.9 \text{ V}$.
(b) Now sketch I_X as a function of V_X as V_X goes from 0 to V_{DD} .

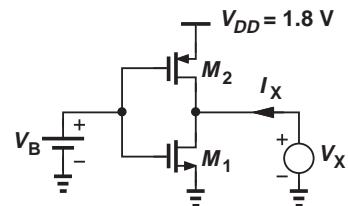


Figure 7.53

Sec. 7.2 Common-Source Stage

- 7.17.** In the common-source stage of Fig. 7.54, $W/L = 30/0.18$ and $\lambda = 0$.

- (a) What gate voltage yields a drain current of 0.5 mA ? (Verify that M_1 operates in saturation.)

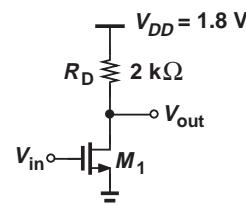


Figure 7.54

- (b) With such a drain bias current, calculate the voltage gain of the stage.

- 7.18.** The circuit of Fig. 7.54 is designed with $W/L = 20/0.18$, $\lambda = 0$, and $I_D = 0.25 \text{ mA}$.
- Compute the required gate bias voltage.
 - With such a gate voltage, how much can W/L be increased while M_1 remains in saturation? What is the maximum voltage gain that can be achieved as W/L increases?

- 7.19.** We wish to design the stage of Fig. 7.55 for a voltage gain of 5 with $W/L \leq 20/0.18$. Determine the required value of R_D if the power dissipation must not exceed 1 mW.

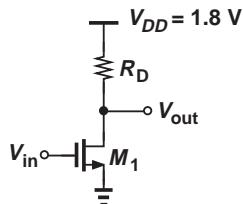


Figure 7.55

- 7.20.** The CS stage of Fig. 7.56 must provide a voltage gain of 10 with a bias current of 0.5 mA. Assume $\lambda_1 = 0.1 \text{ V}^{-1}$, and $\lambda_2 = 0.15 \text{ V}^{-1}$.

- Compute the required value of $(W/L)_1$.
- If $(W/L)_2 = 20/0.18$, calculate the required value of V_b .

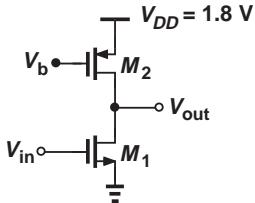


Figure 7.56

- 7.21.** In the stage of Fig. 7.56, M_2 has a long length so that $\lambda_2 \ll \lambda_1$. Calculate the voltage gain if $\lambda_1 = 0.1 \text{ V}^{-1}$, $(W/L)_1 = 20/0.18$, and $I_D = 1 \text{ mA}$.

- 7.22.** The circuit of Fig. 7.56 is designed for a bias current of I_1 with certain dimensions for M_1 and M_2 . If the width and the length of both transistors are doubled, how does the voltage gain change? Consider two cases:

- the bias current remains constant, or
- the bias current is doubled.

- 7.23.** The CS stage depicted in Fig. 7.57 must achieve a voltage gain of 15 at a bias current of 0.5 mA. If $\lambda_1 = 0.15 \text{ V}^{-1}$ and $\lambda_2 = 0.05 \text{ V}^{-1}$, determine the required value of $(W/L)_2$.

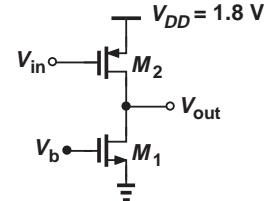


Figure 7.57

- 7.24.** Explain which one of the topologies shown in Fig. 7.58 is preferred.

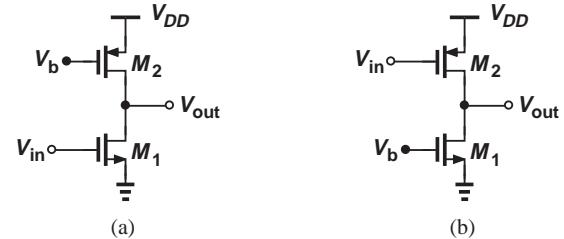


Figure 7.58

- 7.25.** We wish to design the circuit shown in Fig. 7.59 for a voltage gain of 3. If $(W/L)_1 = 20/0.18$, determine $(W/L)_2$. Assume $\lambda = 0$.

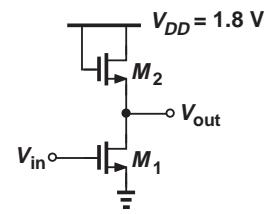


Figure 7.59

- 7.26.** In the circuit of Fig. 7.59, $(W/L)_1 = 10/0.18$ and $I_{D1} = 0.5 \text{ mA}$.

- If $\lambda = 0$, determine $(W/L)_2$ such that M_1 operates at the edge of saturation.
- Now calculate the voltage gain.
- Explain why this choice of $(W/L)_2$ yields the maximum gain.

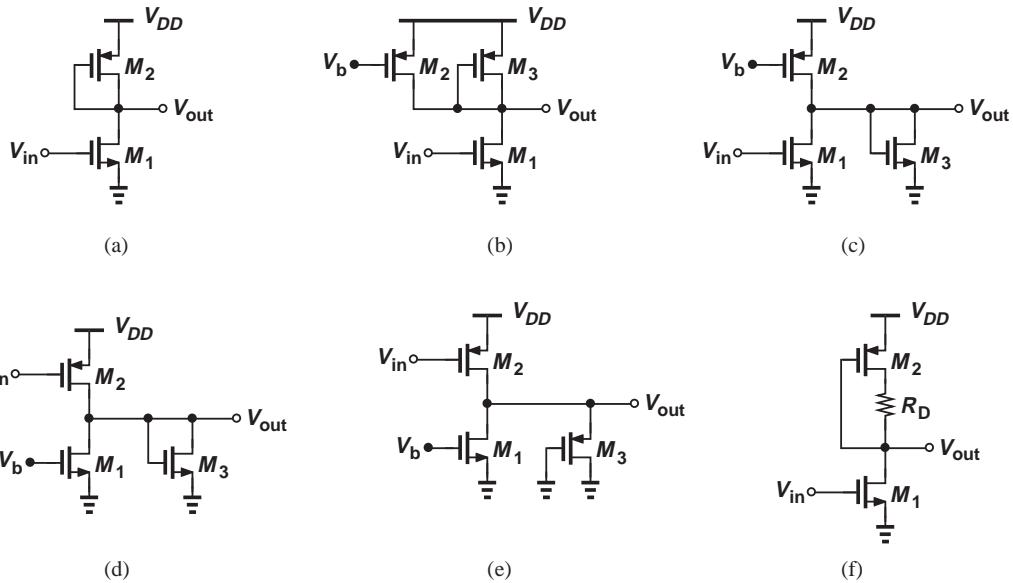


Figure 7.60

7.27. The CS stage of Fig. 7.59 must achieve a voltage gain of 5.

- If $(W/L)_2 = 2/0.18$, compute the required value of $(W/L)_1$.
- What is the maximum allowable bias current if M_1 must operate in saturation?

****7.28.** If $\lambda \neq 0$, determine the voltage gain of the stages shown in Fig. 7.60.

***7.29.** In the circuit of Fig. 7.61, determine the gate voltage such that M_1 operates at the edge of saturation. Assume $\lambda = 0$.

***7.30.** The degenerated CS stage of Fig. 7.61 must provide a voltage gain of 4 with a bias current of 1 mA. Assume a drop of 200 mV across R_S and $\lambda = 0$.

(a) If $R_D = 1 \text{ k}\Omega$, determine the required value of W/L . Does the transistor operate in saturation for this choice of W/L ?

(b) If $W/L = 50/0.18$, determine the required value of R_D . Does the transistor operate in saturation for this choice of R_D ?

****7.31.** Calculate the voltage gain of the circuits depicted in Fig. 7.62. Assume $\lambda = 0$.

***7.32.** Consider a degenerated CS stage with $\lambda > 0$. Assuming $g_m r_O \gg 1$, calculate the voltage gain of the circuit.

***7.33.** Determine the output impedance of each circuit shown in Fig. 7.63. Assume $\lambda \neq 0$.

7.34. The CS stage of Fig. 7.64 carries a bias current of 1 mA. If $R_D = 1 \text{ k}\Omega$ and $\lambda = 0.1 \text{ V}^{-1}$, compute the required value of W/L for a gate voltage of 1 V. What is the voltage gain of the circuit?

7.35. Repeat Problem 7.34 with $\lambda = 0$ and compare the results.

7.36. An adventurous student decides to try a new circuit topology wherein the input is applied to the drain and the output is sensed at the source (Fig. 7.65). Assume $\lambda \neq 0$, determine the voltage gain of the circuit and discuss the result.

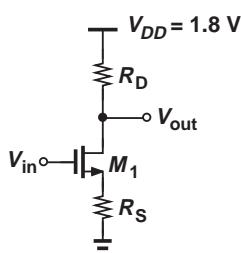


Figure 7.61

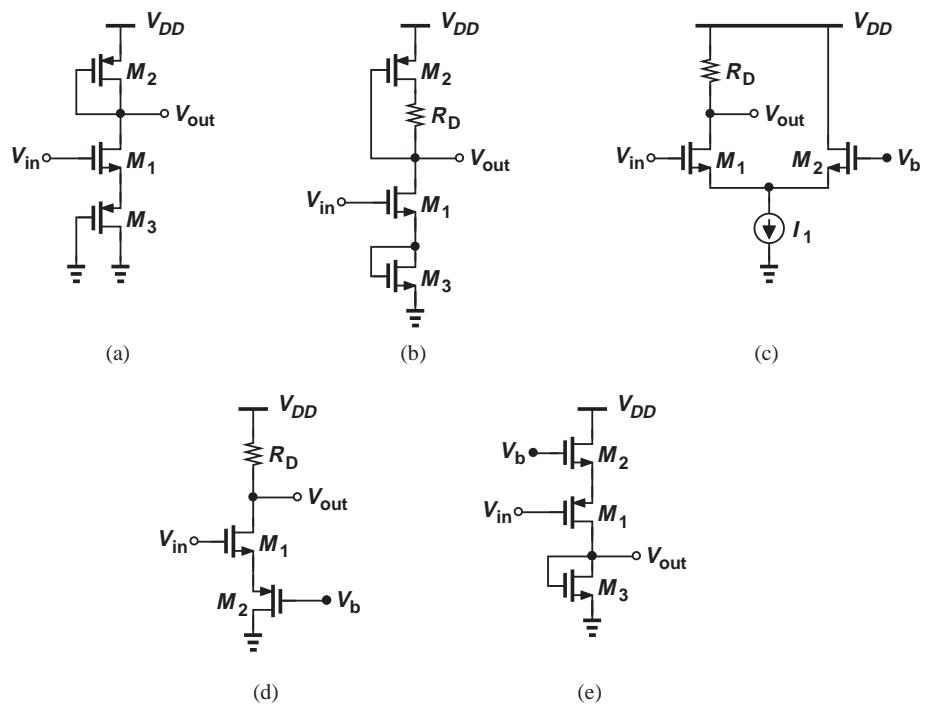


Figure 7.62

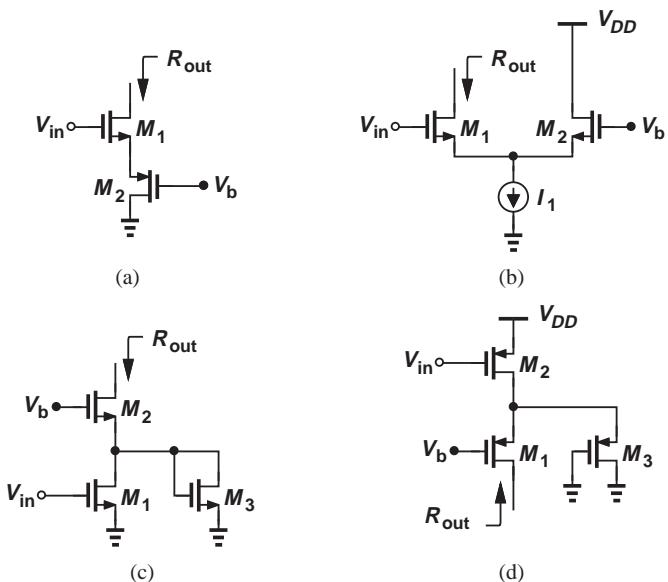


Figure 7.63

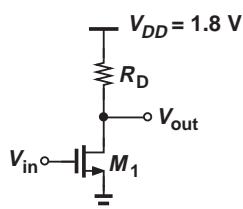


Figure 7.64

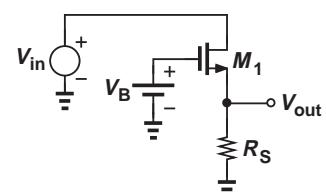


Figure 7.65

7.37. In the common-source stage depicted in Fig. 7.66, the drain current of M_1 is defined by the ideal current source I_1 and remains independent of R_1 and R_2 (why?). Suppose $I_1 = 1 \text{ mA}$, $R_D = 500 \Omega$, $\lambda = 0$, and C_1 is very large.

- Compute the value of W/L to obtain a voltage gain of 5.
- Choose the values of R_1 and R_2 to place the transistor 200 mV away from the triode region while $R_1 + R_2$ draws no more than 0.1 mA from the supply.
- With the values found in (b), what happens if W/L is twice that found in (a)? Consider both the bias conditions (e.g., whether M_1 comes closer to the triode region) and the voltage gain.

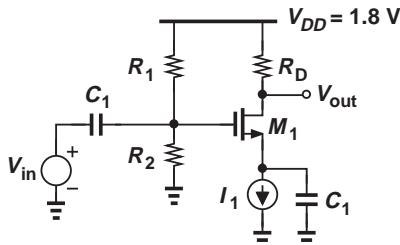


Figure 7.66

7.38. Consider the CS stage shown in Fig. 7.67, where I_1 defines the bias current of M_1 and C_1 is very large.

- If $\lambda = 0$ and $I_1 = 1 \text{ mA}$, what is the maximum allowable value of R_D for M_1 to remain in saturation?
- With the value found in (a), determine W/L to obtain a voltage gain of 5.

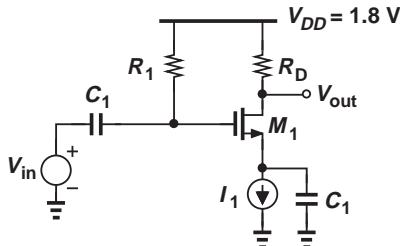


Figure 7.67

Sec. 7.3 Common-Gate Stage

7.39. The common-gate stage shown in Fig. 7.68 must provide a voltage gain of 4 and an input impedance of 50Ω . If $I_D = 0.5 \text{ mA}$, and $\lambda = 0$, determine the values of R_D and W/L .

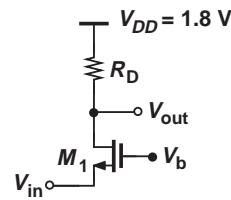


Figure 7.68

7.40. Suppose in Fig. 7.68, $I_D = 0.5 \text{ mA}$, $\lambda = 0$, and $V_b = 1 \text{ V}$. Determine the values of W/L and R_D for an input impedance of 50Ω and maximum voltage gain (while M_1 remains in saturation).

7.41. The CG stage depicted in Fig. 7.69 must provide an input impedance of 50Ω and an output impedance of 500Ω . Assume $\lambda = 0$.

- What is the maximum allowable value of I_D ?
- With the value obtained in (a), calculate the required value of W/L .
- Compute the voltage gain.

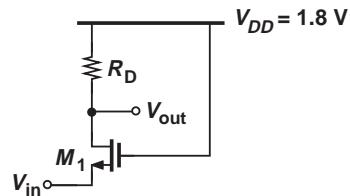


Figure 7.69

***7.42.** A CG stage with a source resistance of R_S employs a MOSFET with $\lambda > 0$. Assuming $g_m r_o \gg 1$, calculate the voltage gain of the circuit.

7.43. The CG amplifier shown in Fig. 7.70 is biased by means of $I_1 = 1 \text{ mA}$. Assume $\lambda = 0$ and C_1 is very large.

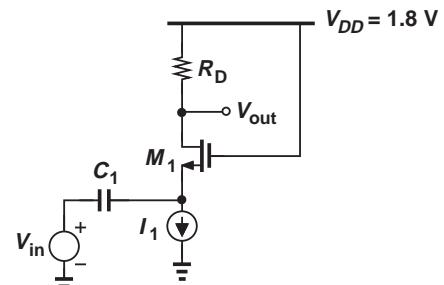


Figure 7.70

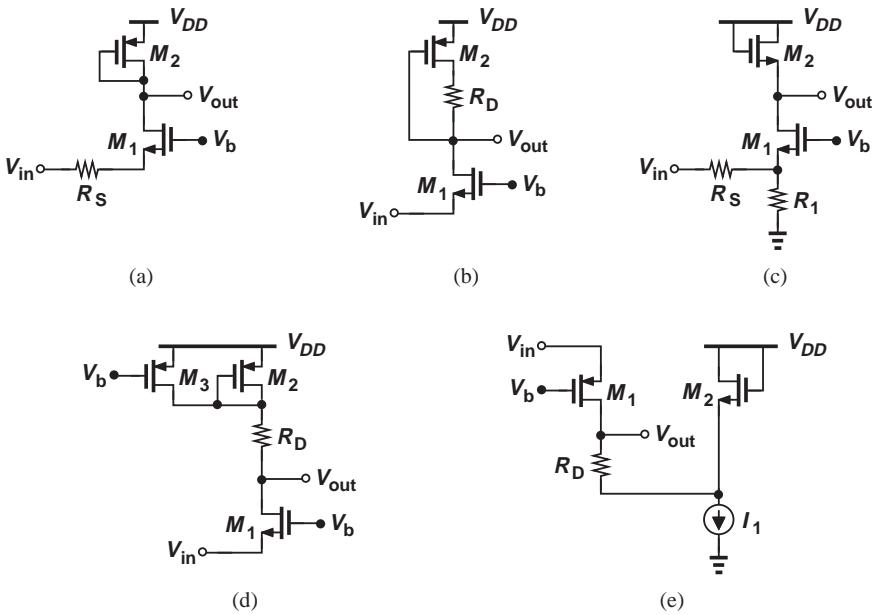


Figure 7.71

- (a) What value of R_D places the transistor M_1 100 mV away from the triode region?
- (b) What is the required W/L if the circuit must provide a voltage gain of 5 with the value of R_D obtained in (a)?
- *7.44.** Determine the voltage gain of each stage depicted in Fig. 7.71. Assume $\lambda = 0$.
- 7.45.** Consider the circuit of Fig. 7.72, where a common-source stage (M_1 and R_{D1}) is followed by a common-gate stage (M_2 and R_{D2}).
- Writing $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$ and assuming $\lambda = 0$, compute the overall voltage gain.
 - Simplify the result obtained in (a) if $R_{D1} \rightarrow \infty$. Explain why this result is to be expected.

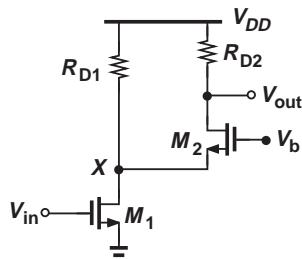


Figure 7.72

- 7.46.** Repeat Problem 7.45 for the circuit shown in Fig. 7.73.

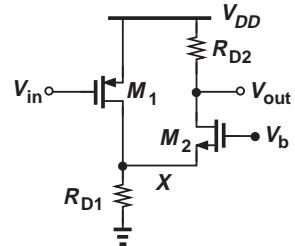


Figure 7.73

- 7.47.** Assuming $\lambda = 0$, calculate the voltage gain of the circuit shown in Fig. 7.74. Explain why this stage is *not* a common-gate amplifier.

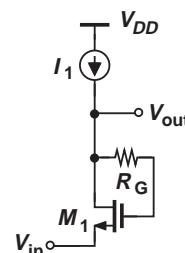


Figure 7.74

- 7.48.** Calculate the voltage gain of the stage depicted in Fig. 7.75. Assume $\lambda = 0$ and the capacitors are very large.

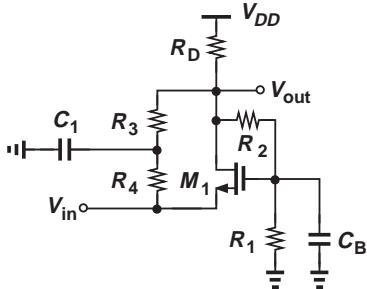


Figure 7.75

Sec. 7.4 Source Follower

- 7.49.** The source follower shown in Fig. 7.76 is biased through R_G . Calculate the voltage gain if $W/L = 20/0.18$ and $\lambda = 0.1 \text{ V}^{-1}$.

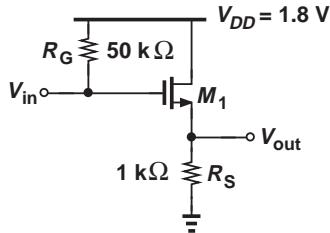


Figure 7.76

- 7.50.** We wish to design the source follower shown in Fig. 7.77 for a voltage gain of 0.8. If $W/L = 30/0.18$ and $\lambda = 0$, determine the required gate bias voltage.

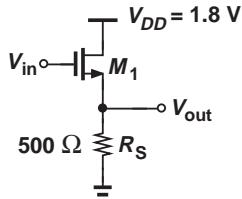


Figure 7.77

- 7.51.** The source follower of Fig. 7.77 is to be designed with a maximum bias gate voltage of 1.8 V. Compute the required value of W/L for a voltage gain of 0.8 if $\lambda = 0$.

- 7.52.** The source follower depicted in Fig. 7.78 employs a current source. Determine the values of I_1 and W/L if the circuit must provide an output impedance less than 100 Ω with $V_{GS} = 0.9 \text{ V}$. Assume $\lambda = 0$.

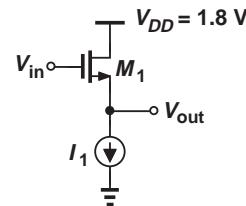


Figure 7.78

- 7.53.** The circuit of Fig. 7.78 must exhibit an output impedance of less than 50 Ω with a power budget of 2 mW. Determine the required value of W/L . Assume $\lambda = 0$.

- 7.54.** We wish to design the source follower of Fig. 7.79 for a voltage gain of 0.8 with a power budget of 3 mW. Compute the required value of W/L . Assume C_1 is very large and $\lambda = 0$.

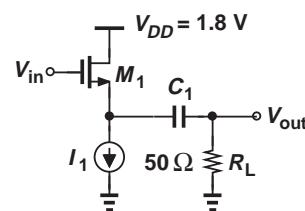


Figure 7.79

- *7.55.** Determine the voltage gain of the stages shown in Fig. 7.80. Assume $\lambda \neq 0$.

- *7.56.** Consider the circuit shown in Fig. 7.81, where a source follower (M_1 and I_1) precedes a common-gate stage (M_2 and R_D).
 (a) Writing $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$, compute the overall voltage gain.
 (b) Simplify the result obtained in (a) if $g_{m1} = g_{m2}$.

Design Problems

In the following problems, unless otherwise stated, assume $\lambda = 0$.

- 7.57.** Design the CS stage shown in Fig. 7.82 for a voltage gain of 5 and an output impedance of 1 k Ω . Bias the transistor so that it operates 100 mV away from the triode region. Assume the capacitors are very large and $R_D = 10 \text{ k}\Omega$.

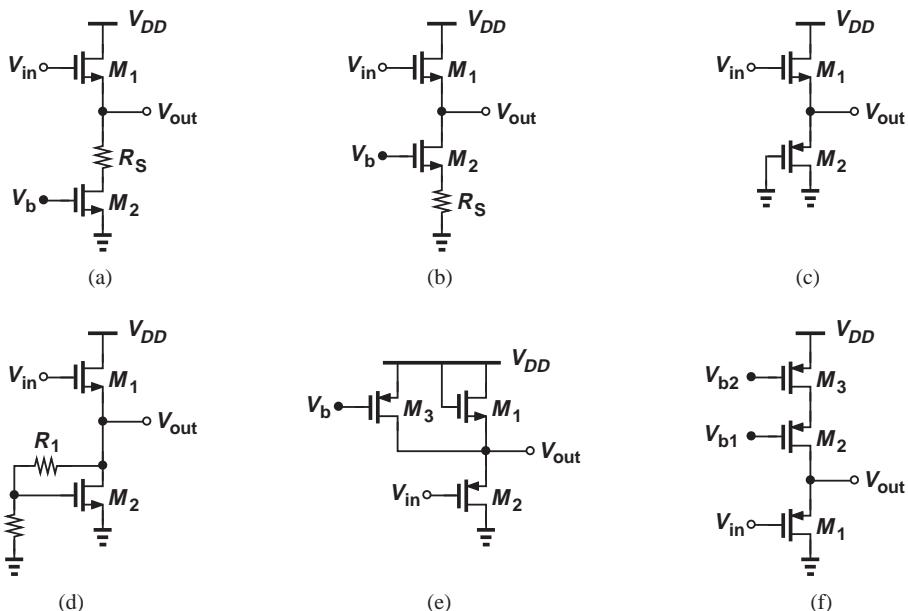


Figure 7.80

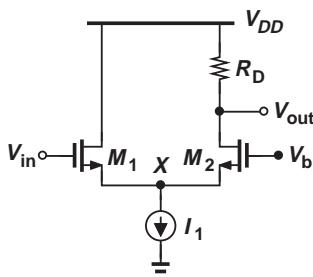


Figure 7.81

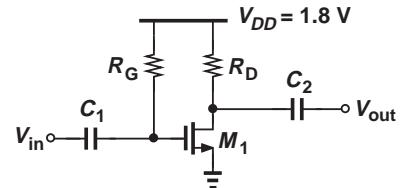


Figure 7.82

7.58. The CS amplifier of Fig. 7.82 must be designed for a voltage gain of 5 with a power budget of 2 mW. If $R_D I_D = 1$ V, determine the required value of W/L . Make the same assumptions as those in Problem 7.57.

7.59. We wish to design the CS stage of Fig. 7.82 for maximum voltage gain but with $W/L \leq 50/0.18$ and a maximum output impedance of 500Ω . Determine the required current. Make the same assumptions as those in Problem 7.57.

7.60. The degenerated stage depicted in Fig. 7.81 must provide a voltage gain of 4 with a power budget of 2 mW while the voltage drop across R_S is equal to 200 mV. If the overdrive voltage of the transistor must not exceed 300 mV and $R_1 + R_2$

must consume less than 5% of the allocated power, design the circuit. Make the same assumptions as those in Problem 7.57.

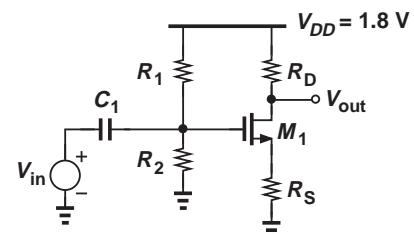


Figure 7.83

7.61. Design the circuit of Fig. 7.83 for a voltage gain of 5 and a power budget of 6 mW. Assume the voltage drop across R_S is equal to the overdrive voltage of the transistor and $R_D = 200 \Omega$.

- 7.62.** The circuit shown in Fig. 7.84 must provide a voltage gain of 6, with C_S serving as a low impedance at the frequencies of interest. Assuming a power budget of 2 mW and an input impedance of $20\text{ k}\Omega$, design the circuit such that M_1 operates 200 mV away from the triode region. Select the values of C_1 and C_S so that their impedance is negligible at 1 MHz.

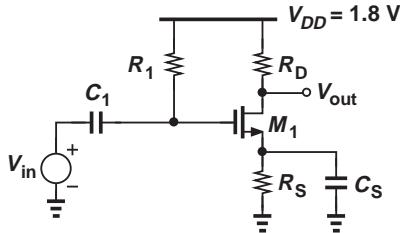


Figure 7.84

- 7.63.** In the circuit of Fig. 7.85, M_2 serves as a current source. Design the stage for a voltage gain of 20 and a power budget of 2 mW. Assume $\lambda = 0.1 \text{ V}^{-1}$ for both transistors and the maximum allowable level at the output is 1.5 V (i.e., M_2 must remain in saturation if $V_{out} \leq 1.5 \text{ V}$).

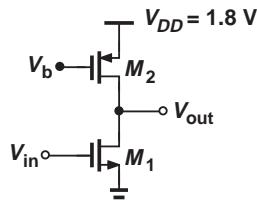


Figure 7.85

- 7.64.** Consider the circuit shown in Fig. 7.86, where C_B is very large and $\lambda_n = 0.5\lambda_p = 0.1 \text{ V}^{-1}$.

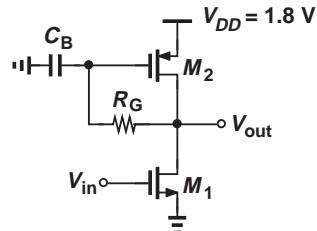


Figure 7.86

- (a) Calculate the voltage gain.

- (b) Design the circuit for a voltage gain of 15 and a power budget of 3 mW. Assume $R_G \approx 10(r_{o1}||r_{o2})$ and the dc level of the output must be equal to $V_{DD}/2$.

- 7.65.** The CS stage of Fig. 7.87 incorporates a degenerated PMOS current source. The degeneration must raise the output impedance of the current source to about $10r_{o1}$ such that the voltage gain remains nearly equal to the intrinsic gain of M_1 . Assume $\lambda = 0.1 \text{ V}^{-1}$ for both transistors and a power budget of 2 mW.

- (a) If $V_B = 1 \text{ V}$, determine the values of $(W/L)_2$ and R_S so that the impedance seen looking into the drain of M_2 is equal to $10r_{o1}$.
- (b) Determine $(W/L)_1$ to achieve a voltage gain of 30.

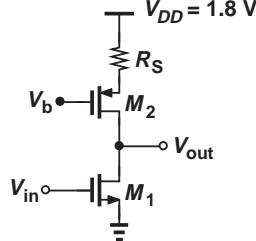


Figure 7.87

- 7.66.** Assuming a power budget of 1 mW and an overdrive of 200 mV for M_1 , design the circuit shown in Fig. 7.88 for a voltage gain of 4.

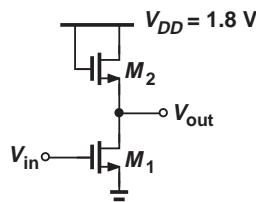


Figure 7.88

- 7.67.** Design the common-gate stage depicted in Fig. 7.89 for an input impedance of 50Ω and a voltage gain of 5. Assume a power budget of 3 mW.

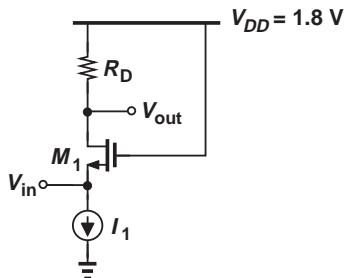


Figure 7.89

- 7.68.** Design the circuit of Fig. 7.90 such that M_1 operates 100 mV away from the triode region while providing a voltage gain of 4. Assume a power budget of 2 mW.

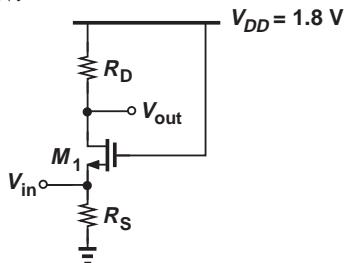


Figure 7.90

- 7.69.** Figure 7.91 shows a self-biased common-gate stage, where $R_G \approx 10R_D$ and C_G serves as a low impedance so that the voltage gain is still given by $g_m R_D$. Design the circuit for a power budget of 5 mW and a voltage gain of 5. Assume $R_S \approx 10/g_m$ so that the input impedance remains approximately equal to $1/g_m$.

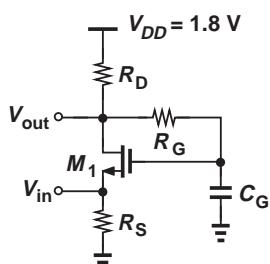


Figure 7.91

- 7.70.** Design the CG stage shown in Fig. 7.92 such that it can accommodate an output swing of 500 mV_{pp} , i.e., V_{out} can fall below its bias value by 250 mV without driving

M_1 into the triode region. Assume a voltage gain of 4 and an input impedance of 50Ω . Select $R_S \approx 10/g_m$ and $R_1 + R_2 = 20 \text{ k}\Omega$. (Hint: since M_1 is biased 250 mV away from the triode region, we have $R_S I_D + V_{GS} - V_{TH} + 250 \text{ mV} = V_{DD} - I_D R_D$.)

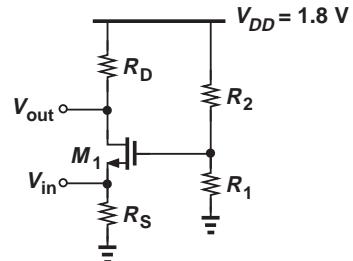


Figure 7.92

- 7.71.** Design the source follower depicted in Fig. 7.93 for a voltage gain of 0.8 and a power budget of 2 mW. Assume the output dc level is equal to $V_{DD}/2$ and the input impedance exceeds $10 \text{ k}\Omega$.

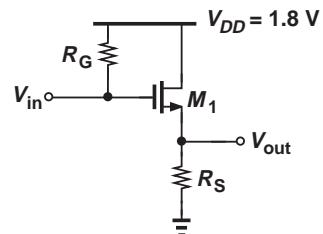


Figure 7.93

- 7.72.** Consider the source follower shown in Fig. 7.94. The circuit must provide a voltage gain of 0.6 at 100 MHz. Design the circuit such that the dc voltage at node X is equal to $V_{DD}/2$. Assume the input impedance exceeds $20 \text{ k}\Omega$.

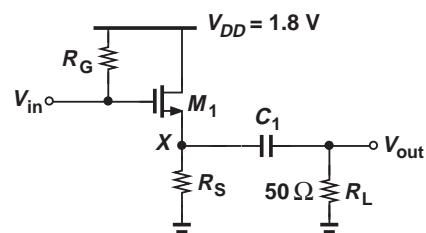


Figure 7.94

- 7.73.** In the source follower of Fig. 7.95, M_2 serves as a current source. The circuit must operate with a power budget of 3 mW, a voltage gain of 0.9, and a minimum allowable output of 0.3 V (i.e., M_2 must remain in saturation if $V_{DS2} \geq 0.3$ V). Assuming $\lambda = 0.1 \text{ V}^{-1}$ for both transistors, design the circuit.

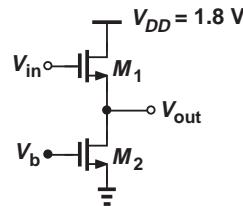


Figure 7.95

SPICE PROBLEMS

In the following problems, use the MOS models and source/drain dimensions given in Appendix A. Assume the substrates of NMOS and PMOS devices are tied to ground and V_{DD} , respectively.

- 7.74.** In the circuit of Fig. 7.96, I_1 is an ideal current source equal to 1 mA.
- Using hand calculations, determine $(W/L)_1$ such that $g_{m1} = (100 \Omega)^{-1}$.
 - Select C_1 for an impedance of $\approx 100 \Omega (\ll 1 \text{ k}\Omega)$ at 50 MHz.
 - Simulate the circuit and obtain the voltage gain and output impedance at 50 MHz.
 - What is the change in the gain if I_1 varies by $\pm 20\%$?

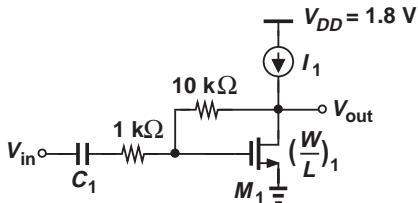


Figure 7.96

- 7.75.** The source follower of Fig. 7.97 employs a bias current source, M_2 .
- What value of V_{in} places M_2 at the edge of saturation?
 - What value of V_{in} places M_1 at the edge of saturation?
 - Determine the voltage gain if V_{in} has a dc value of 1.5 V.

- (d) What is the change in the gain if V_b changes by $\pm 50 \text{ mV}$?

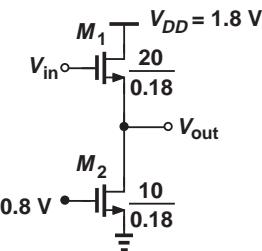


Figure 7.97

- 7.76.** Figure 7.98 depicts a cascade of a source follower and a common-gate stage. Assume $V_b = 1.2 \text{ V}$ and $(W/L)_1 = (W/L)_2 = 10 \mu\text{m}/0.18 \mu\text{m}$.
- Determine the voltage gain if V_{in} has a dc value of 1.2 V.
 - Verify that the gain drops if the dc value of V_{in} is higher or lower than 1.2 V.
 - What dc value at the input reduces the gain by 10% with respect to that obtained in (a)?

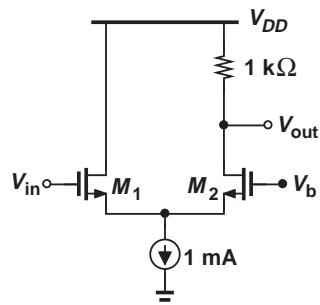


Figure 7.98

- 7.77.** Consider the CS stage shown in Fig. 7.99, where M_2 operates as a resistor.

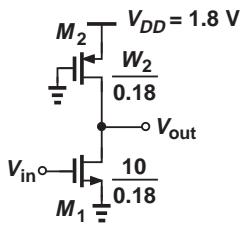


Figure 7.99

- Determine W_2 such that an input dc level of 0.8 V yields an output dc level of 1 V. What is the voltage gain under these conditions?
- What is the change in the gain if the mobility of the NMOS device varies by

$\pm 10\%$? Can you explain this result using the expressions derived in Chapter 6 for the transconductance?

- 7.78.** Repeat Problem 7.77 for the circuit illustrated in Fig. 7.100 and compare the sensitivities to the mobility.

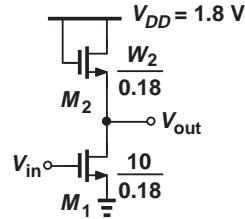
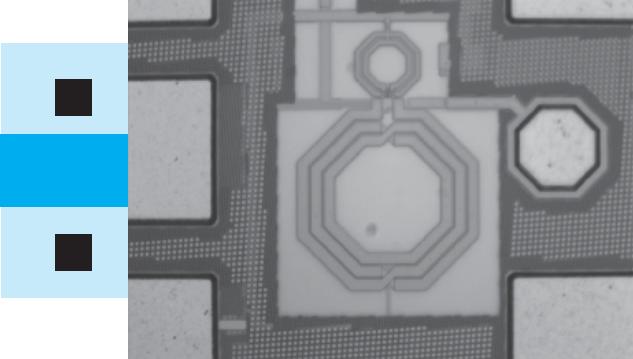


Figure 7.100

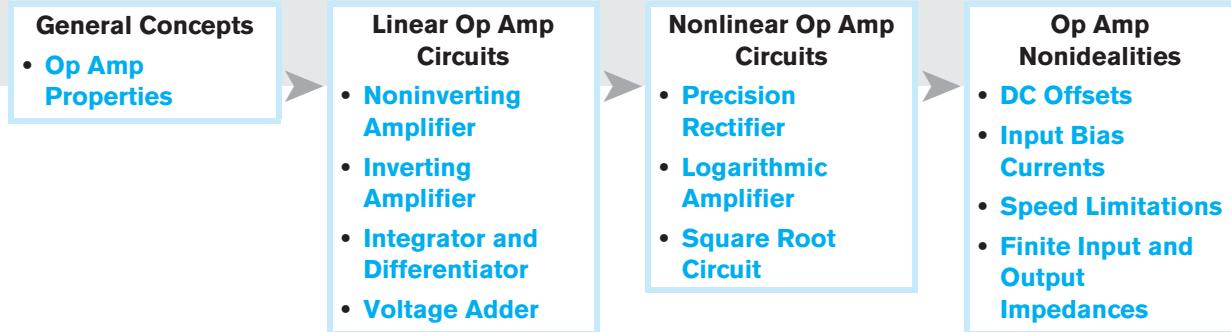


Operational Amplifier as a Black Box

The term “operational amplifier” (op amp) was coined in the 1940s, well before the invention of the transistor and the integrated circuit. Op amps realized by vacuum tubes¹ served as the core of electronic “integrators,” “differentiators,” etc., thus forming systems whose behavior followed a given differential equation. Called “analog computers,” such circuits were used to study the stability of differential equations that arose in fields such as control or power systems. Since each op amp implemented a mathematical *operation* (e.g., integration), the term “operational amplifier” was born.

Op amps find wide application in today’s discrete and integrated electronics. In the cellphone studied in Chapter 1, for example, integrated op amps serve as building blocks in (active) filters. Similarly, the analog-to-digital converter(s) used in digital cameras often employ op amps.

In this chapter, we study the operational amplifier as a black box, developing op-amp-based circuits that perform interesting and useful functions. The outline is shown below.



¹Vacuum tubes were amplifying devices consisting of a filament that released electrons, a plate that collected them, and another that controlled the flow—somewhat similar to MOSFETs.