BHUSHAN KIRAN MUNOLI

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EDUCATION

- **Texas A&M University** *August 2025-May 2027*
  *MS in Electrical and Computer Engineering - **GPA - 3.7*** College Station, Texas
  - **Courses:** Digital IC Design, Microprocessor System Design, Computer Architecture, Advanced Computer Architecture, Advanced Hardware Verification
- **PES University** *August 2019-May 2023*
  *B-Tech Electronics and Communications Engineering - **GPA - 3.7*** India

PROFESSIONAL EXPERIENCE

- **Maven Silicon** *Mar 2025 - Dec 2025*
  ASIC Physical Design Engineer India
  - Built Net-list to GDS II design flow of **RISC V for a 32nm design** with 6.34k standard cell count, constraint files, along with analysis of area, power and time tradeoff
  - Performed floor planning, placement, clock tree synthesis, Routing, post optimization and finally sign-off
  - Trained on **Advanced Physical Design** and Verification and covered concepts: **floor planning, STA, Place and Route, CTS, Timing Closure and Physical Verification**
- **Deloitte South Asia LLP** *July 2023- July 2025*
  SAP Success Factors Consultant & CPI Developer India
  - Built test-scripts iFlows & performed **Odata API & SFTP integration** using **Groovy Script & Java Script**
- **Zebra Technologies** *January 2023 - July 2023*
  Network Engineer (Intern) India
  - Developed system apps for Android Devices to verify Wi-Fi & Bluetooth connectivity and worked on synchronization of system clock between multiple devices in the test environment to improve test efficiency

SKILLS

- **Skills :** C, C++, LINUX Shell, Make file, Perl, TCL, Clock Domain Crossing, Floor-planning, Placement & Routing, Static Timing Analysis, Clock Tree Synthesis(CTS), ASIC Design
- **Tools :** Synopsys - Design Compiler, IC Compiler, Prime Time, Cadence - Virtuoso, Spectre

CERTIFICATIONS

- **Cadence | Basic Static Timing Analysis v3.0**
- **Cadence | System Verilog Assertions v5.2**
- **Cadence | System Verilog for Design and Verification v25.03**
- **Maven Silicon | Advanced VLSI Design**

PROJECTS

- **Implementation of Random Double Bit and Burst ECC for HBM3** *January 2027*
  Tools: Xilinx Vivado, Cadence Virtuoso, Spectre
  - Developed a **Matlab script** to analyze and match the results & algorithm in the research paper
  - Designed an RTL level error correction code using verilog. Tested the design using a **FPGA board**
  - Building a design on **180nm technology** to meet the encoder and decoder specification **21.27% less area** compared to Unit-ECC
- **Design of Pipelined Adder with Buffered H-clock Tree** *November 2025*
  Tools: Cadence Virtuoso, Spectre
  - Designed and analyzed **NAND XOR, NOT logic gates, flip-flop and SRAM** schematics and layouts
  - Built a transistor-level schematic and layout for the **8-bit pipelined adder** with a **Buffered H-clock Tree**
  - Applied the logical effort method to optimize transistor sizing and achieved a **delay reduction of 33%**
- **RISC-V Implementation** *October 2025*
  Tools: Synopsys DC Compiler and ICC II Compiler
  - Designed **32 bit Microprocessor (RISC-V core)** from **RTL to GDSII** using **32nm Technology** modules to operate reliably at a clock period of **7ns**, with a **T-shaped floor-plan** and **29338.9 µm²** total cell area
  - Performed full **Clock Tree Synthesis**, to optimize clock distribution and minimize skew
  - Analyzed power distribution, with detailed breakdown of static and dynamic power contributions
- **Router 1x3 Implementation** *July 2025*
  Tools: Synopsys - Fusion Compiler
  - Designed a Router 1x3 using **32nm technology** with L Shaped floor-planning and **333MHz** clock frequency
  - Performed full Clock Tree Synthesis and initialized DRC check to correct violations in the router design