

BHUSHAN KIRAN MUNOLI

 Bhushan Munoli | +1-979-344-6100 | munolibhushan@gmail.com |  Bhushan Kiran Munoli | College Station, Tx
EDUCATION

- Texas A&M University August 2025-May 2027
College Station, Texas
MS in Electrical and Computer Engineering - GPA - 3.66
- Courses: Introduction To Hardware Design Verification, Introduction to Formal Verification, Advanced Hardware Verification, Digital IC Design, Computer Architecture, Microprocessor System Design
- PES University August 2019-May 2023
India
B-Tech Electronics and Communications Engineering - GPA - 3.7

PROFESSIONAL EXPERIENCE

- Maven Silicon Mar 2025 - Dec 2025
India (Remote)
ASIC Physical Design Engineer
 - Trained on **Advanced Physical Design** and Verification and covered concepts: **floor planning, STA, Place and Route, CTS, Timing Closure and Physical Verification**. Performed synthesis and Design for Test
 - Built Netlist to GDSII design flow of **RISC V for a 32nm design** with 6.34k standard cell count, constraint files, along with analysis of area, power and time tradeoff
 - Performed floor planning, placement, clock tree synthesis, Routing, post optimization and finally sign-off
- Deloitte South Asia LLP July 2023- July 2025
SAP SuccessFactors Consultant & CPI Developer
 - Built test-scripts iFlows & performed **Odata API & SFTP integration** using **Groovy Script & Java Script**
- Zebra Technologies January 2023 - July 2023
Network Engineer (Intern)
 - Developed system apps for **Android Devices** to verify Wi-Fi and Bluetooth connectivity and collaborated with cross-functional teams to reduced the system time difference between the devices to **1 millisecond** by sending a **modified NTP packet** from the host server and test **4+ devices** simultaneously

PROJECTS

- Implementation of Random Double Bit and Burst ECC for HBM3 In progress
Tools: Xilinx Vivado, Cadence Virtuoso, Spectre, Xilinx Artix-7
 - Developed a **Matlab script** to analyze and match the results & algorithm in the research paper
 - Designed an RTL level error correction code using verilog. Tested the design using a **FPGA board**
 - Built a design on **180nm technology** with decoder having **21.27% less area** compared to Unit-ECC
- Functional Verification of Hyper Transport Advanced X-Bar in UVM environment November 2025
Tools: Xilinx Vivado, Cadence vManager, SimVision, IMC
 - Developed a verification plan using vManager to review and track the functional specifications of **HTAX**
 - Set up the verification environment by developing and integrating the **UVM test bench components** including **assertions, cover points, drivers and monitors**
 - Executed random sequence regression and performed **root cause analysis** to achieve **100% coverage**
- Design of Pipelined Adder with Buffered H-clock Tree November 2025
Tools: Cadence Virtuoso, Spectre
 - Designed and analyzed **NAND XOR, NOT logic gates, flip-flop and SRAM** schematics and layouts
 - Built a transistor-level schematic and layout for the 8-bit pipelined adder with a **Buffered H-clock Tree**
 - Applied the logical effort method to optimize transistor sizing and achieved a **delay reduction of 33%**
- RISC-V Implementation October 2025
Tools: Synopsys DC Compiler and ICC II Compiler
 - Designed **32 bit Microprocessor (RISC-V core)** from **RTL to GDSII** using **32nm Technology** modules to operate reliably at a clock period of **7ns**, with a **T-shaped floor-plan** and **29338.9 μm²** total cell area
 - Performed full **Clock Tree Synthesis**, to optimize clock distribution and minimize skew
 - Analyzed power distribution, with detailed breakdown of static and dynamic power contributions
- Router 1x3 Implementation July 2025
Tools: Synopsys - Fusion Compiler
 - Designed a Router 1x3 using **32nm technology** with L Shaped floor-planning and **333MHz** clock frequency
 - Performed full Clock Tree Synthesis and initialized DRC check to correct violations in the router design

SKILLS

- Skills : UVM, System Verilog, Verilog, C, C++, Python, LINUX Shell, Git, Make file, Perl, TCL FPGA Design, RTL Design, Timing Analysis, Floor-planning, Placement & Routing, Static Timing Analysis, Clock Tree Synthesis(CTS), ASIC, Soc Design and Verification, Design-for-Test(DFT), GPU & CPU Architectur
- Tools : Xilinx Vivado, Synopsys - Design Compiler, Fusion Compiler, IC Compiler, Prime Time, Cadence - Virtuoso, Xcelium, Spectre, vManager, SimVision, IMC