BHUSHAN KIRAN MUNOLI

+1-979-344-6100 | munolibhushan@gmail.com | College Station, TX
https://bhushanmunoli.github.io/Bhushan-Portfolio/ | https://www.linkedin.com/in/bhushan-kiran-munoli/

I am deeply interested in **ASIC design** and motivated to apply my skills and **transferable experience** in the industry. With a strong technical foundation, I aim to contribute meaningfully and deliver quality solutions in the semiconductor domain.

EDUCATION

- **Texas A&M University** August 2025-May 2027
  MS in Electrical and Computer Engineering College Station,Tx
  - **Courses:** Digital IC Design, Computer Architecture, Advanced Computer Architecture, Advanced Hardware Verification
- **PES University** B-Tech Electronics and Communications Engineering August 2019-May 2023

SKILLS

- **Concepts :** Clock Domain Crossing, Static Timing Analysis, Clock Tree Synthesis, Floor-planning, Placement & Routing
- **Programming Languages :** Verilog, SystemVerilog, UVM, LINUX Shell, Perl, TCL, C, C++, Python, Java
- **Tools :** Cadence - Virtuoso, Spectre Synopsys - Design Compiler, IC Compiler, Prime Time

PROFESSIONAL EXPERIENCE

- **MAVEN SILICON** Mar 2025 - Dec 2025
  ASIC Physical Design Engineer India
  - Built Net-list to GDS II design flow of RISC V for a 32nm design with constraint files, along with analysis of area, power & time tradeoff. Performed placement, routing for macros and standard cells along with Concurrent Clock and Data Optimization and Integrated Clock Gating
  - Performed Static Timing Analysis and Clock Tree Synthesis to manage timing delays for a 5ns clock. Analyzed timing reports for input and output delay constraints. Worked on Clock domain Crossing to manage clocks of different frequencies.
  - Achieved standard cell and core area reduction by 11.8% and total power reduction by 70% with 5ns clock, minimizing congestion and meeting setup and hold time requirements.
- **DELOITTE SOUTH ASIA LLP** July 2023- July 2025
  SAP SuccessFactors Consultant & CPI Developer India
  - Created integration suites to send messages between S/4HANA, LinkedIn, Docusign, Adobe Acrobat etc. and SAP SuccessFactors. Collaborated with the pre-sales team to conducted client workshops to boost sales & build customer relations

PROJECT

- **Implementation of Random Double Bit and Burst ECC for HBM3** January 2026
  Tools: Xilinx Vivado, Cadence Virtuoso, Spectre
  - Designed RTL level error correction code. Tested the design on a FPGA board. Developed a Matlab script to analyze results
  - Building a design on 180nm technology to meet the SoC specification with 21.27% reduction in area
- **Design of 8-bit Pipelined Adder with Buffered H-clock Tree** November 2025
  Tools: Cadence Virtuoso, Spectre
  - Designed layouts and performed LVS and DRC checks for NAND, XOR, NOT logic gates, flip-flop and SRAM
  - Built a schematic and layout for the 8-bit pipelined adder. Performed clock tree synthesis & designed a H-clock Tree
  - Applied the logical effort method to optimize transistor sizing and achieved a delay reduction of 33%
- **RISC-V Implementation** October 2025
  Tools: Synopsys DC Compiler and ICC II Compiler
  - Designed 32 bit Microprocessor (RISC-V core) from RTL to GDSII using 32nm Technology modules Performed full Clock Tree Synthesis, to optimize clock distribution and minimize skew
  - Performed Macro, Standard cell placement & congestion analysis. Completed placement and post route optimization
  - Optimized the design to operate reliably at a clock period of 7ns with an area of 29338.9μm^2 .
- **Router 1x3 Implementation** July 2025
  Tools: Synopsys - Fusion Compiler
  - Designed a Router 1x3 using 32nm technology with L Shaped floor-planning and 333MHz clock frequency
  - Performed full Clock Tree Synthesis and initialized DRC check to correct violations in the router design

CERTIFICATIONS

- Cadence | Basic Static Timing Analysis
- Cadence | SystemVerilog Assertions
- Cadence | SystemVerilog for Design and Verification
- Maven Silicon | Advanced VLSI Design