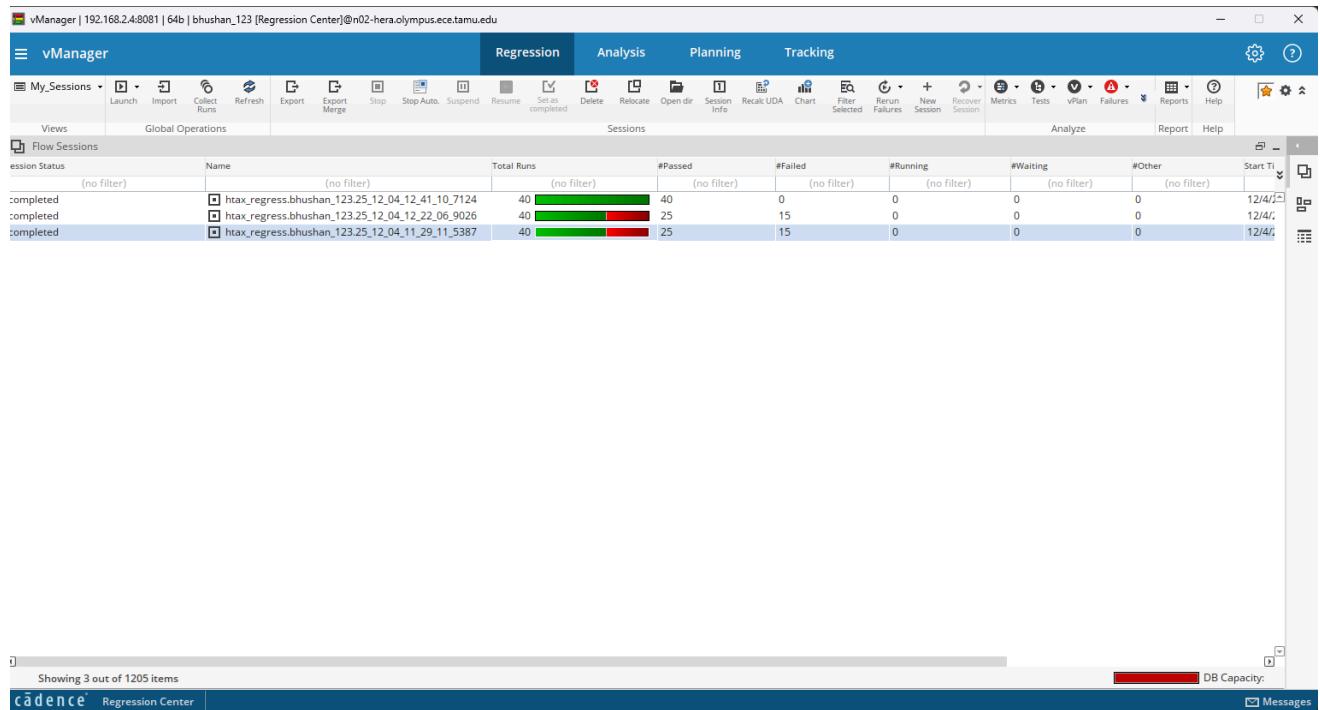


Lab - 10 Report

Bhushan Kiran Munoli - 837004070

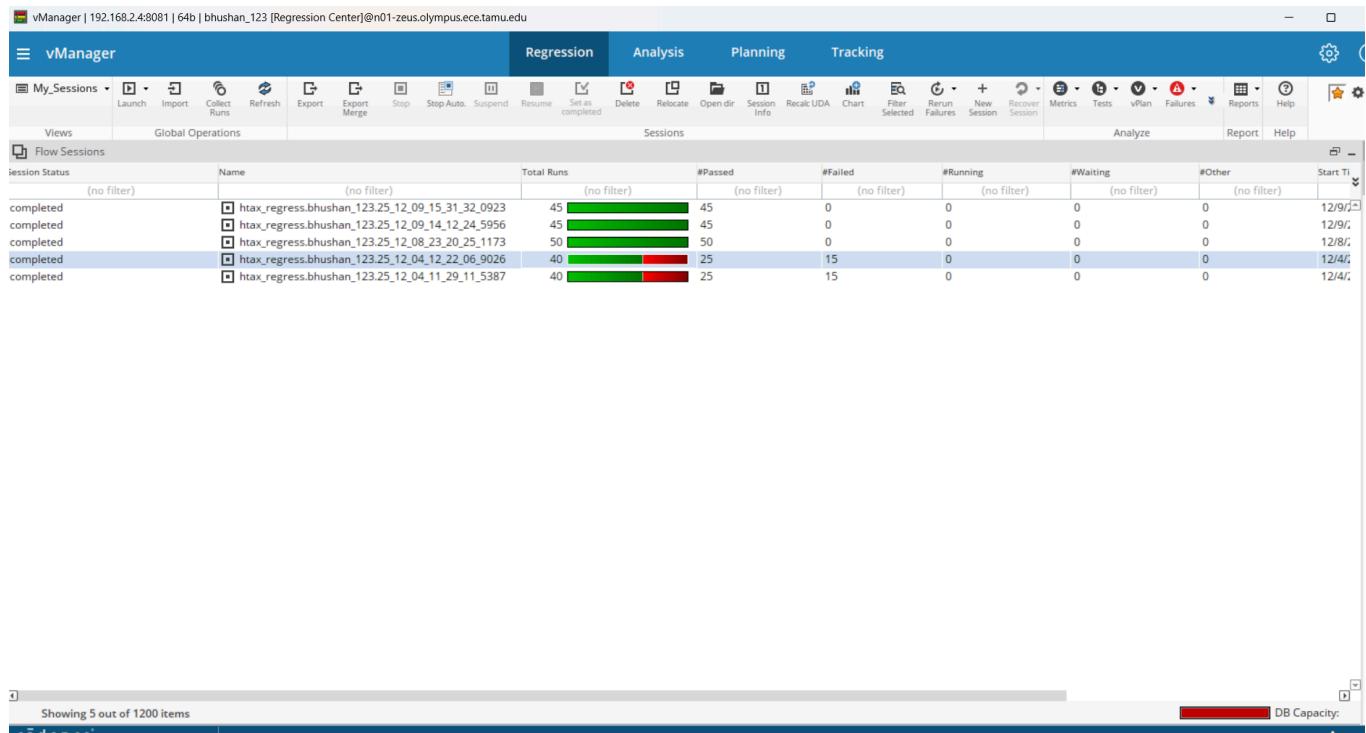
Screenshot of Failing Regression:



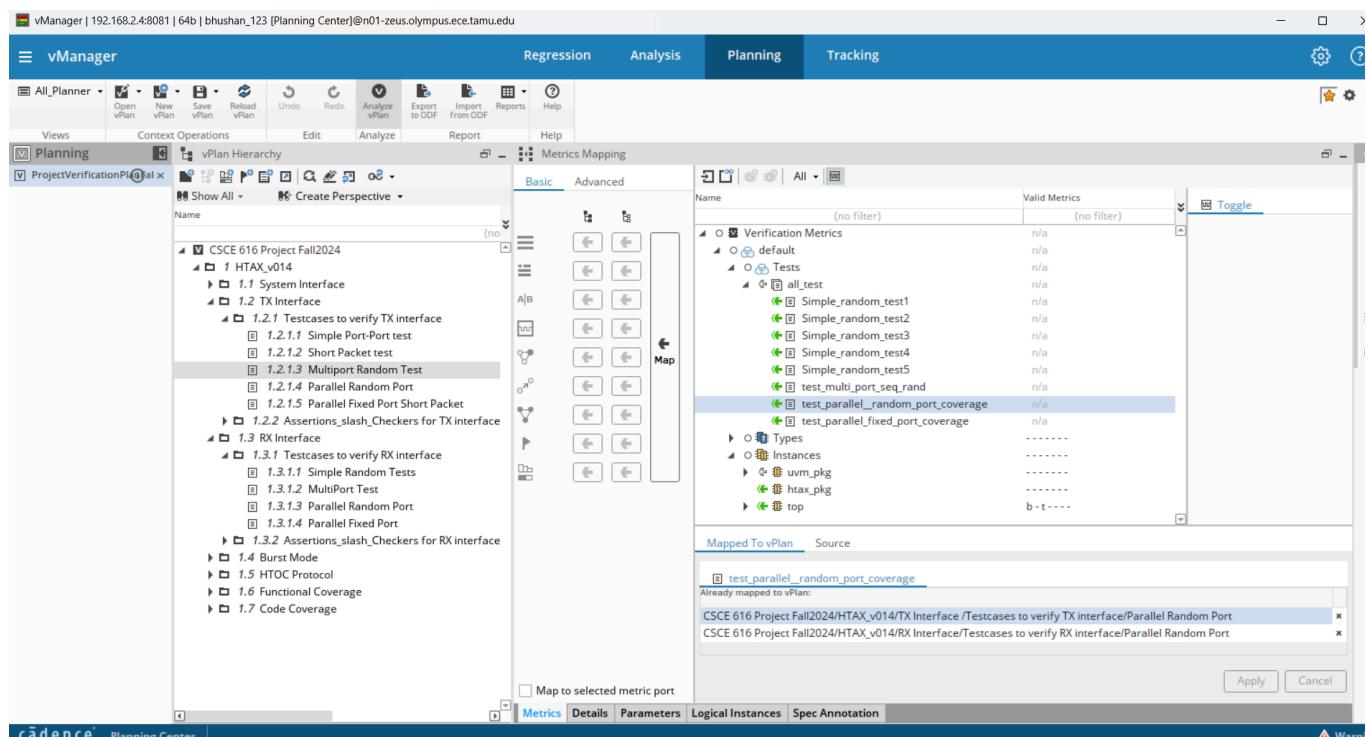
The screenshot shows the vManager Regression Center interface. The top navigation bar includes tabs for Regression, Analysis, Planning, and Tracking. The Regression tab is selected. The main content area displays a table of sessions. The table has columns for session, status, name, total runs, passed, failed, running, waiting, other, and start time. Three sessions are listed, all of which are completed. The first two sessions have 40 total runs, with 0 failed and 0 running. The third session has 40 total runs, with 15 failed and 0 running. The interface also shows a progress bar for DB Capacity and a message bar at the bottom.

session	status	Name	Total Runs	#Passed	#Failed	#Running	#Waiting	#Other	Start Ti
completed	(no filter)	htax_regress.bhushan_123.25_12_04_12_41_10_7124	40	40	0	0	0	0	12/4/2023
completed	(no filter)	htax_regress.bhushan_123.25_12_04_12_22_06_9026	40	25	15	0	0	0	12/4/2023
completed	(no filter)	htax_regress.bhushan_123.25_12_04_11_29_11_5387	40	25	15	0	0	0	12/4/2023

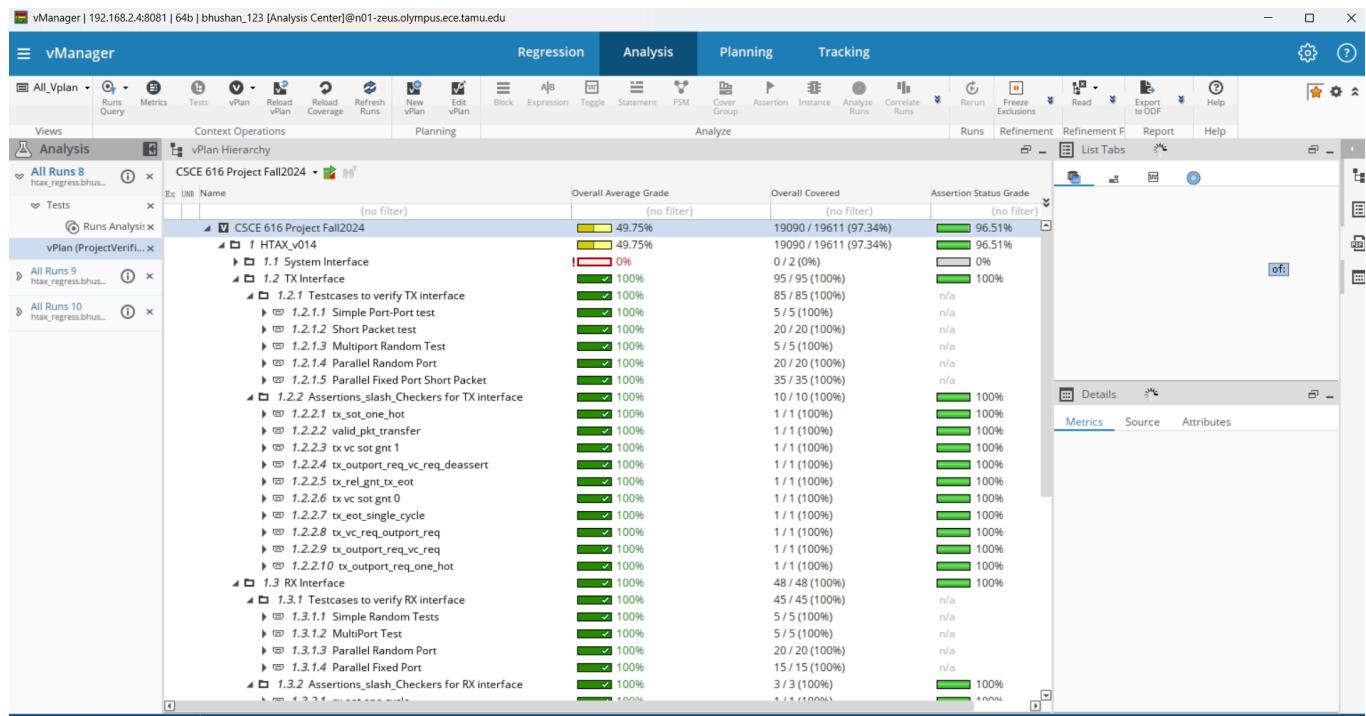
Screenshot of Passing Regression after the failing regression



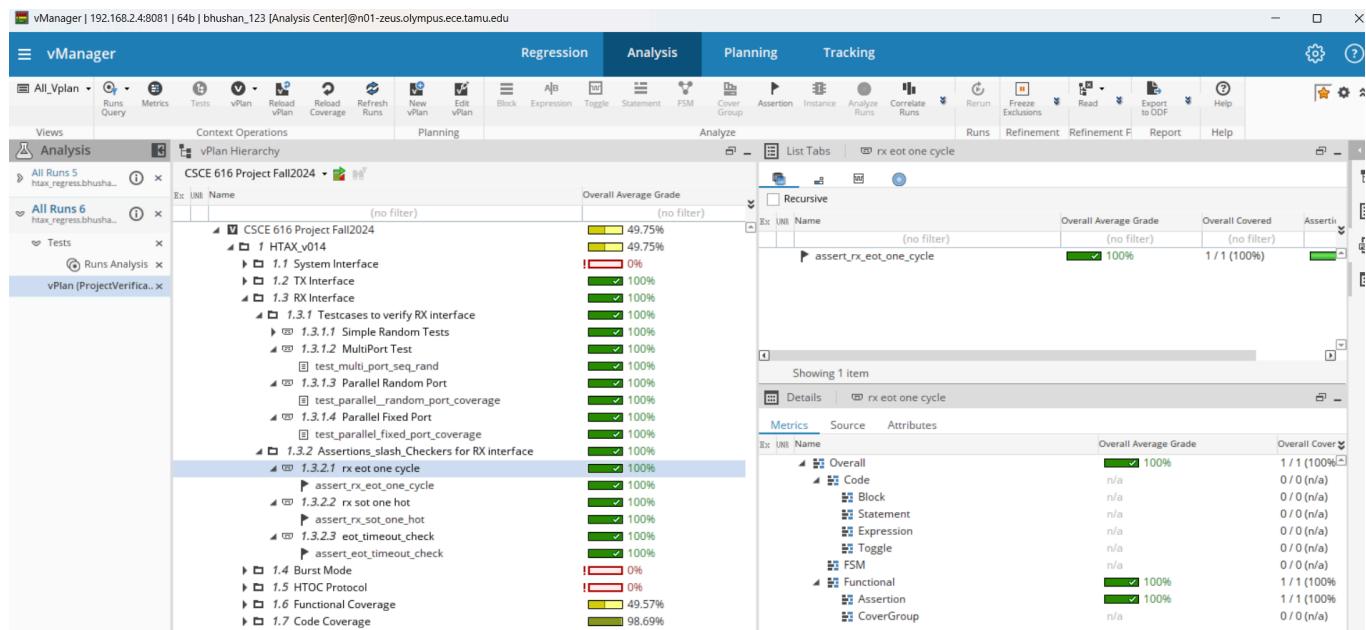
Test Case Mapped



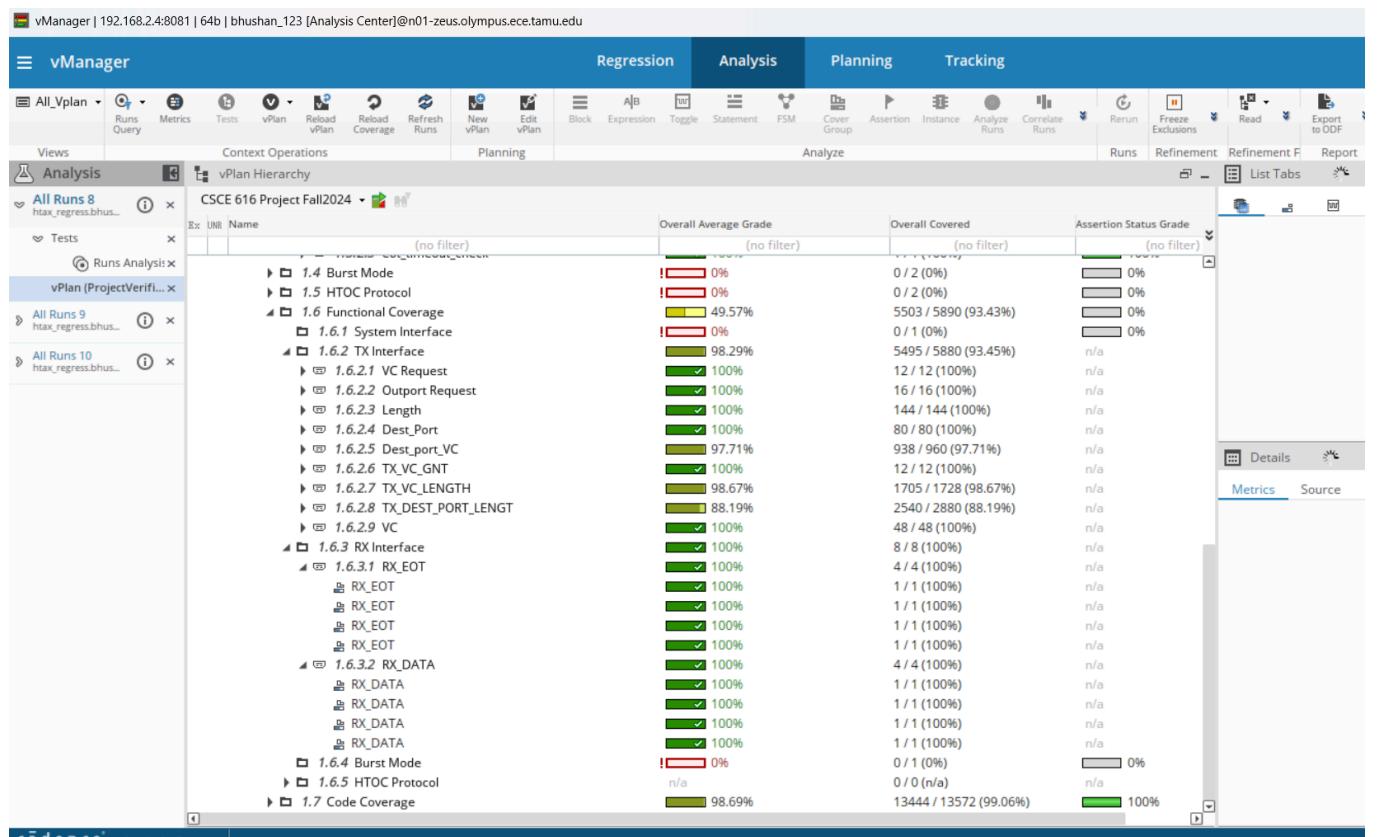
Assertions Checkers for TX interface



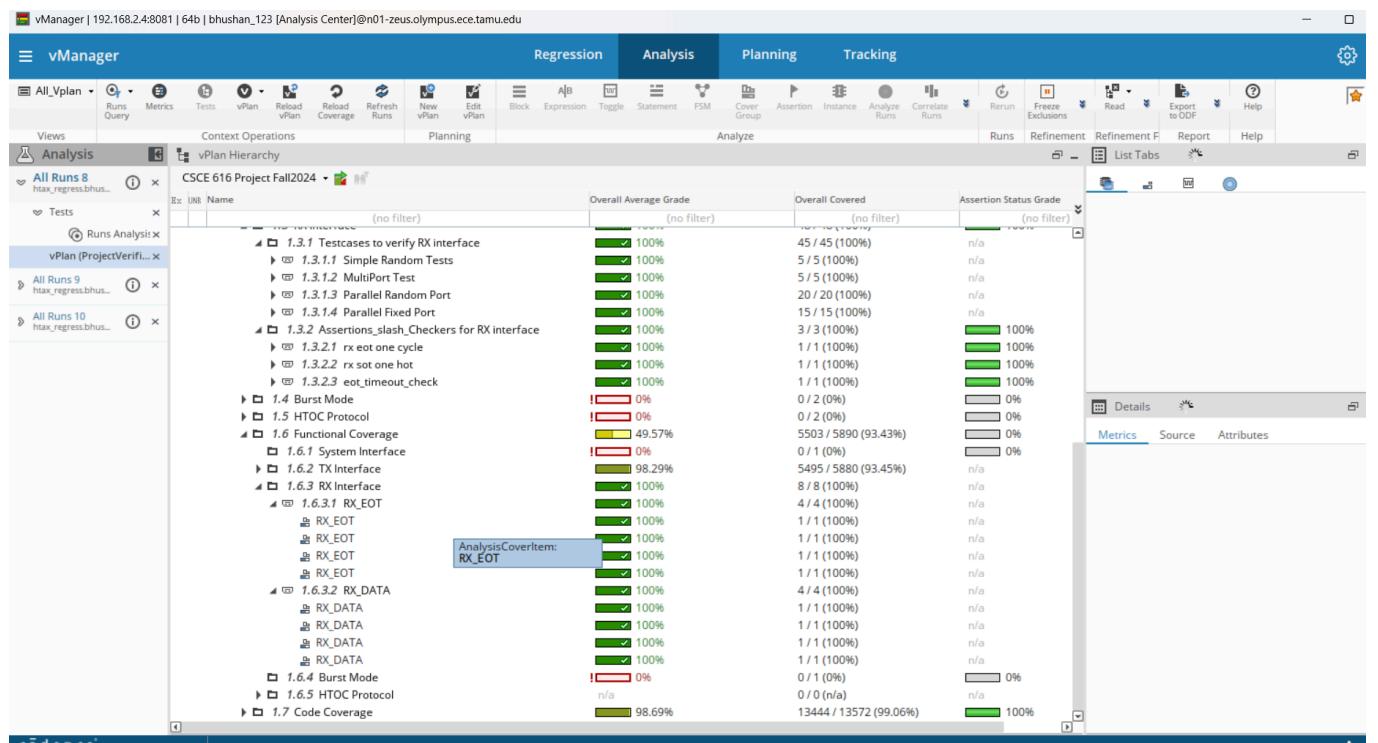
Assertions/ Checkers for RX interface



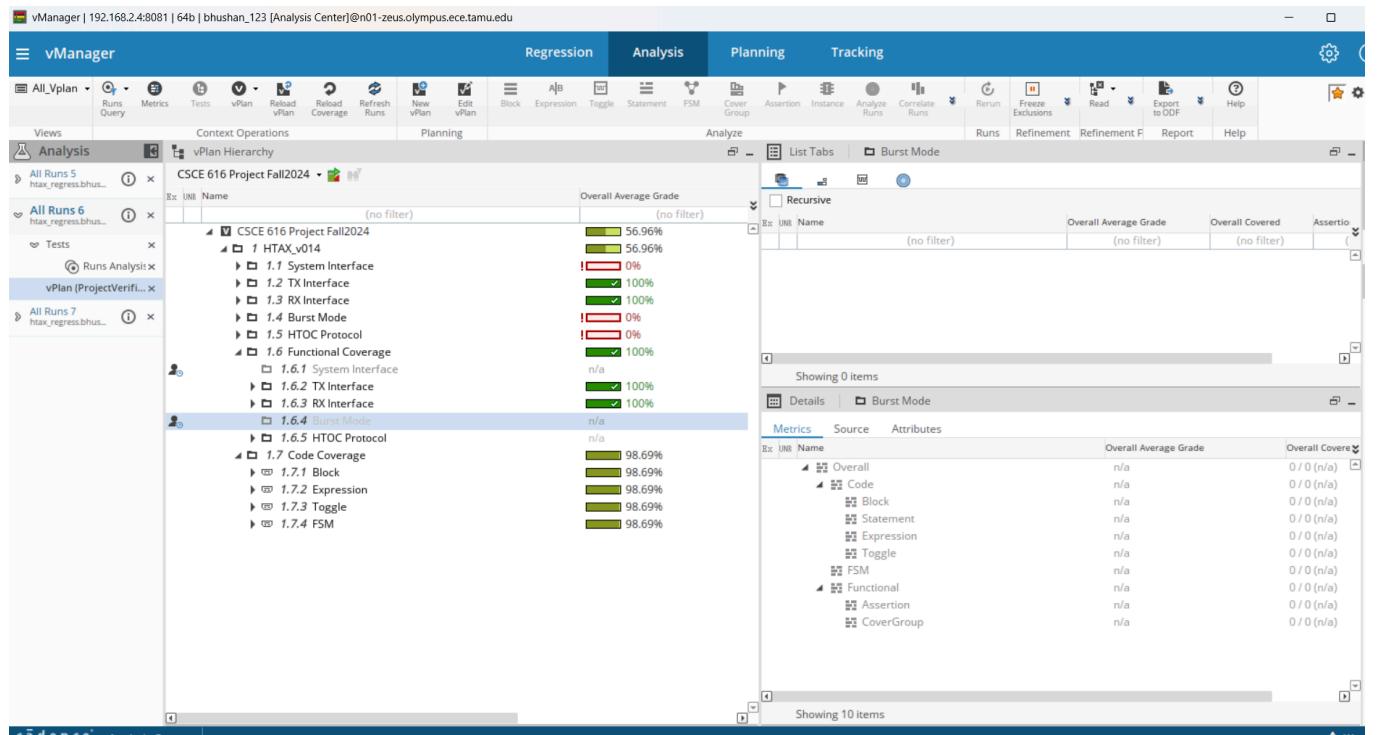
Functional Coverage for TX interface



Functional Coverage for Rx Interface



Code Coverage



Code coverage Holes

Code coverage reached 98.69% as Burst and HTOC mode are excluded. If those cases are tested, the Code coverage will result in 100% result

Bug report

Bug 1

What is the bug?

The bug occurs when data transmission to all destination ports finishes at the same time. In this condition, the rx_eot signal never asserts even after 1000 cycles from the assertion of rx_sot. This results in the eot_timeout_check assertion failing. When EOT is asserted simultaneously for all four ports, selected_eot incorrectly evaluates to 0, causing no EOT to propagate. Consequently, the assertion expecting an EOT within 1000 cycles after SOT is violated.

Where is it?

Module: lab-10-BhushanKM/work/design/

File: htax_outport_data_mux.v

Line number(s): 43

How to reproduce:

Constrain all 4 ports to send packets with by keeping the constraints constant

Constant Length (e.g., length == 3)

Constant Delay (e.g., delay == 1)

Valid VC (e.g., vc == 1)

This simulation will force the condition eot_in = 4'b1111 at the end of the packet transfer.

Expected behavior:

The selected_eot output signal should go HIGH (1) to indicate the packet has finished, regardless of how many other ports are also finishing at the same time. The receiver should see the EOT and the simulation should pass.

Actual behavior:

The selected_eot signal stays LOW (0) due to the logic error. The receiver waits indefinitely for the packet to end, eventually triggering the HTAX_RX_INF ERROR : TIMEOUT assertion fatal error.

Bug fix:

Change the code as follows:

- OLD CODE
 - assign selected_eot = |(eot_in & inport_sel_reg) & ~(&(eot_in));
- NEW CODE
 - assign selected_eot = |(eot_in & inport_sel_reg);

Failing Assertion:

olympus.ece.tamu.edu (1)

Terminal Sessions View X server Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...

olympus.ece.tamu.edu (1)

```

dest_port          integral 32 'h3
vc                integral 2 'h2
length           integral 32 'h1f
data
[0]              integral 64 'hf4bd0fcf6c6d95e
[1]              integral 64 'hb9eff276ffd2fb34
[2]              integral 64 'h482bd93e929351bb
[3]              integral 64 'he33760ee44df3f6
[4]              integral 64 'h37e2e907a18e096
...
[26]             integral 64 'h484e0cf232f91159
[27]             integral 64 'hc83500466c75f056
[28]             integral 64 'h862ffd50951e0d95
[29]             integral 64 'h11485ab4b5de84
[30]             integral 64 'h77bc9424bb201cf9
begin_time        time    64 210
depth             int     32 'd2
parent sequence (name) string 24 parallel_fixed_port_vseq
parent sequence (full name) string 51 uvm_test_top_tb.vsequencer.parallel_fixed_port_vseq
sequencer         string 36 uvm_test_top_tb.tx_port[3].sequencer

xsim: *F,ASRTST (.../tb/htax_rx_interface.sv,56): (time 20150 NS) Assertion top.inst_htax_rx_intf[3].assert_eot_timeout_check has failed
Memory Usage - Current physical: 115.9M, Current virtual: 163.2M
CPU Usage - 0.1s system + 0.1s user = 0.2s total (3.9% cpu)
Simulation terminated via $fatal(2) at time 20150 NS + 2
.../tb/htax_rx_interface.sv:56      $fatal("HTAX_RX_INF ERROR : TIMEOUT rx_eot did not occur within 1000 cycles after rx_sot");
xcelium> exit

coverage setup:
  workdir : ./cov_work
  dutinst : top(top)
  scope   : scope
  testname: test_sv_40634040

coverage files:
  model/design data) : ./cov_work/scope/icc_4e8e3c4e_636b2083.ucm (reused)
  data      : ./cov_work/scope/test_sv_40634040/icc_4e8e3c4e_636b2083.ucd
  TOOL: xrun 22.03-s012: Exiting on Dec 09, 2025 at 19:15:46 CST (total: 00:00:33)
[bhushan_123@n01-zeus ~]$
```

allow terminal fold: olympos-login.engr.tamu.edu 18% 76.81 GB / 1007.61 GB 39.68 Mb/s 280.36 Mb/s 118 days j-polsek-t2 ujwald36 shassan buhrt (x2) vishwanath.shastray adityabiradar25 (x2) willfaerber ryanhuang hzzy ferni

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: <https://mobaxterm.mobatek.net>

vManager | 192.168.2.4:8081 | 64b | bhushan_123 [Analysis Center]@n01-zeus.olympus.ece.tamu.edu

Analysis Regression Analysis Planning Tracking

Views Context Operations Planning Analyze

Analysis Runs

All Runs 8 htax_regress.bhushan_123 All Runs 9 htax_regress.bhushan_123 All Runs 10 htax_regress.bhushan_123

Runs Analysis

Showing 40 items

Errors Warnings/Info

Name	Description	Tool
ASRTST.assert_eot_timeout_check	Assertion top.inst_htax_rx_intf[3].assert_eot_timeout_check has failed	xsim
RUN	run 26 script 'cd /home/grads/b/bhushan_123/lab-10-BhushanKM... n/a	
ASRTST.assert_eot_timeout_check	Assertion top.inst_htax_rx_intf[3].assert_eot_timeout_check has failed	xsim
VMREXEC	'cd /home/grads/b/bhushan_123/lab-10-BhushanKM/work/sim; ... vm_runner	

Showing 4 items

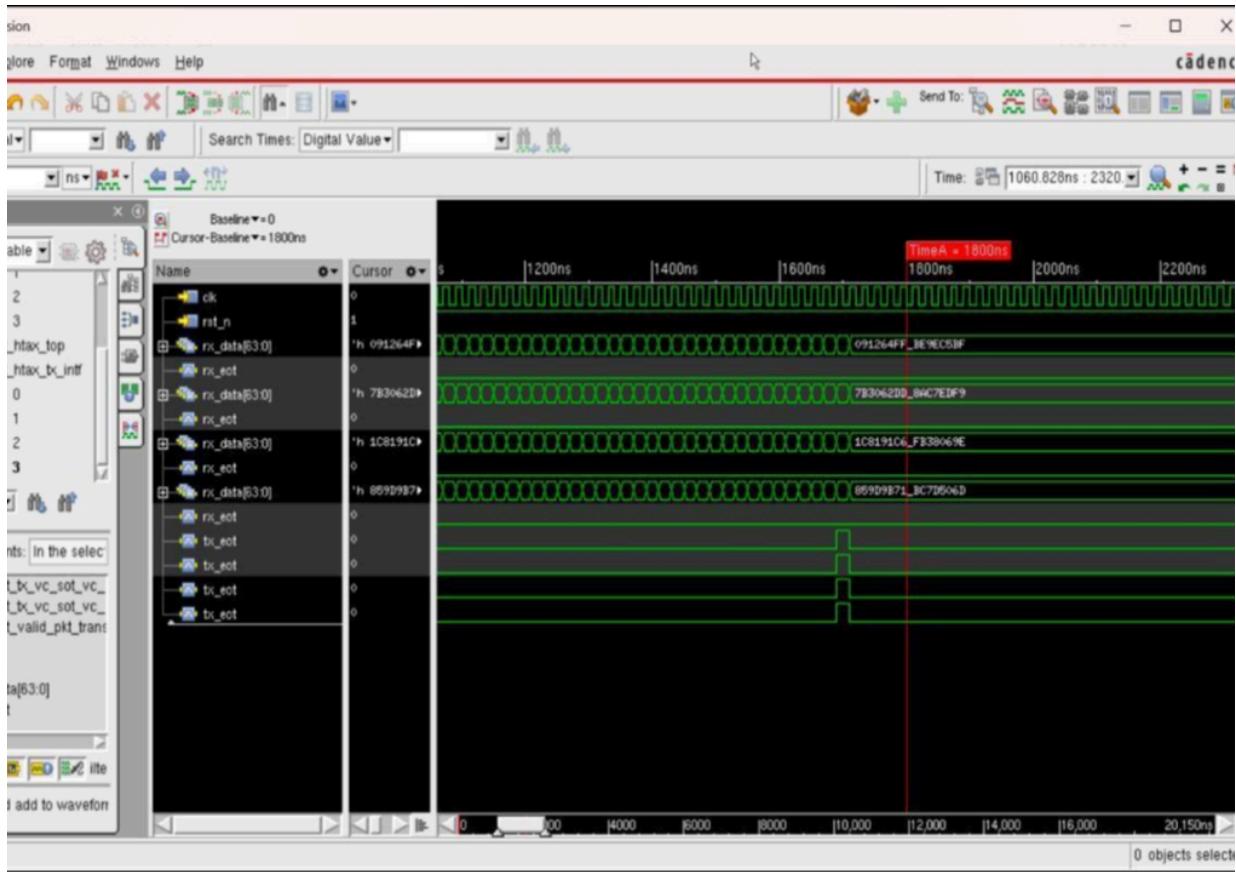
Details /all_test/test_parallel_fixed_port_coverage

Attributes Logs

vm_brun.log xrun.log local_log.log

1 RUN - INFO - Initializing run phase
2 RUN - INFO - Starting run phase
3 RUN - INFO - Debug log file: /home/grads/b/bhushan_123/lab-10-BhushanKM/work/sim/regression/htax_regress.bhushan_123
4 RUN - INFO - Running run no. 26
5 RUN - INFO - Timeout is set to 13000000 seconds
6 RUN - INFO - Executing run script: "cd /home/grads/b/bhushan_123/lab-10-BhushanKM/work/sim; xrun -f run_vm.f +UVM"

Failing Scenario Waveform:



Failing Assertion Passing after the fix:

```
UVM_INFO .../tb/htax_scoreboard_c.sv(104) @ 15300670: uvm_test_top.tb.htax_sb [SCOREBOARD] Data matches for received pkt on port 0
UVM_INFO .../tb/htax_scoreboard_c.sv(107) @ 15300670: uvm_test_top.tb.htax_sb [SCOREBOARD] Dropping pkt from queue 0
UVM_INFO /opt/coe/cadence/XCELUM/tools/methodology/UVM/CDS-1.1d/sv/src/base/uvm_objection.svh(1268) @ 15350650: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
UVM_INFO .../tb/htax_scoreboard_c.sv(150) @ 15350650: uvm_test_top.tb.htax_sb [SCOREBOARD] End of Simulation Checking
UVM_INFO .../tb/htax_scoreboard_c.sv(152) @ 15350650: uvm_test_top.tb.htax_sb [SCOREBOARD] Port 0 Queue is empty
UVM_INFO .../tb/htax_scoreboard_c.sv(156) @ 15350650: uvm_test_top.tb.htax_sb [SCOREBOARD] Port 1 Queue is empty
UVM_INFO .../tb/htax_scoreboard_c.sv(160) @ 15350650: uvm_test_top.tb.htax_sb [SCOREBOARD] Port 2 Queue is empty
UVM_INFO .../tb/htax_scoreboard_c.sv(164) @ 15350650: uvm_test_top.tb.htax_sb [SCOREBOARD] Port 3 Queue is empty
--- UVM Report catcher Summary ---
Number of demoted UVM_FATAL reports : 0
Number of demoted UVM_ERROR reports : 0
Number of demoted UVM_WARNING reports: 0
Number of caught UVM_FATAL reports : 0
Number of caught UVM_ERROR reports : 0
Number of caught UVM_WARNING reports : 0
--- UVM Report Summary ---
** Report counts by severity
UVM_INFO :244816
UVM_WARNING : 0
UVM_ERROR : 0
UVM_FATAL : 0
** Report counts by id
[RNTST] 1
[SCOREBOARD] 163205
[TEST_DONE] 1
[TOP] 5
[UVMTOP] 1
[htax_parallel_fixed_port_test] 1
[htax_tx_driver_c] 81600
[parallel_fixed_port_vseq] 2
```

Analysis Regression Analysis Planning Tracking

All vPlan Runs Metrics Tests vPlan Refresh vPlan Refresh Runs New vPlan Edit vPlan

Views Context Operations Planning

Analysis vPlan Hierarchy

All Runs 8 Max_regress.bhus... Tests vPlan [ProjectVerify...]

All Runs 9 Max_regress.bhus... All Runs 10 Max_regress.bhus...

CSCE 616 Project Fall2024

Overall Average Grade Overall Covered Assertion

Recursive

Ex UNB Name Overall Average Grade

assert_eot_timeout_check 100%

Showing 1 item

Details eot_timeout_check

Metrics Source Attributes

Ex UNB Name Overall Average Grade

Overall 100%

Code n/a

Block n/a

Statement n/a

Expression n/a

Toggle n/a

FSM n/a

Functional 100%

Assertion 100%

CoverGroup n/a

Showing 10 items

Overall Average Grade

1.2.2.3 tx vc sat gnt 1 100% 1/1 (100%)

1.2.2.4 tx_outport_req_vc_req_deassert 100% 1/1 (100%)

1.2.2.5 tx_rel_gnt_tx_eot 100% 1/1 (100%)

1.2.2.6 tx_vc sat gnt 0 100% 1/1 (100%)

1.2.2.7 tx_eot_single_cycle 100% 1/1 (100%)

1.2.2.8 tx_vc_req_outport_req 100% 1/1 (100%)

1.2.2.9 tx_outport_req_vc_req 100% 1/1 (100%)

1.2.2.10 tx_outport_req_one_hot 100% 1/1 (100%)

1.3 RX Interface

1.3.1 Testcases to verify RX interface

1.3.1.1 Simple Random Tests 100% 45 / 45 (100%)

1.3.1.2 MultiPort Test 100% 5 / 5 (100%)

1.3.1.3 Parallel Random Port 100% 5 / 5 (100%)

1.3.1.4 Parallel Fixed Port 100% 20 / 20 (100%)

1.3.2 Assertions_slash_Checkers for RX interface

1.3.2.1 rx_eot one cycle 100% 1 / 1 (100%)

1.3.2.2 rx sat one hot 100% 1 / 1 (100%)

1.3.2.3 eot_timeout_check 100% 1 / 1 (100%)

1.4 Burst Mode

1.5 HTOC Protocol

1.6 Functional Coverage

1.6.1 System Interface

1.6.2 TX Interface

1.6.2.1 VC Request 98.29% 5495 / 5880 (93.45%)

1.6.2.2 Outport Request 100% 12 / 12 (100%)

1.6.2.3 Length 100% 16 / 16 (100%)

1.6.2.4 Dest_Port 100% 144 / 144 (100%)

1.6.2.5 Dest_port_VC 97.71% 80 / 80 (100%)

938 / 960 (97.71%)