ALU - VERIFICATION

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CHAPTER 1: PROJECT OVERVIEW AND SPECIFICATION

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1.1 PROJECT OVERVIEW

The project focuses on the verification of a parameterized Arithmetic Logic Unit (ALU) which supports a wide range of arithmetic and logical operations. ALU are an integral part of any SOC that performs Arithmetic and logical operations. The ALU supports variety of functions including arithmetic operations such as addition, subtraction, increment, decrement, and multiplication, as well as logical operations such as AND, OR, XOR, NOT, NAND, NOR, and XNOR. In addition, it supports shift and rotate operations. The design also has comparator functions and error checking for invalid command conditions.

1.2 VERIFICATION OBJECTIVE

The objective of the project is to:

- Verify functional correctness of all ALU operations — including arithmetic, logical, comparison, and shift/rotate — as determined by CMD and MODE.
- Ensure input protocol compliance by checking that INP_VALID reflects operand availability (2'b01, 2'b10, or 2'b11) and operations proceed only when valid.
- Verify that when only one operand is valid (INP_VALID = 2'b01 or 2'b10), the ALU waits up to 16 clock cycles for the second operand, and asserts ERR if it doesn't arrive.
- Confirm timing behaviour, ensuring results are available after 1 or 2 clock cycles, depending on the operation.
- Apply constrained-random testing and functional coverage to explore all valid/invalid input combinations, including edge cases like overflow, underflow, and invalid rotate commands.

1.3 DUT INTERFACES
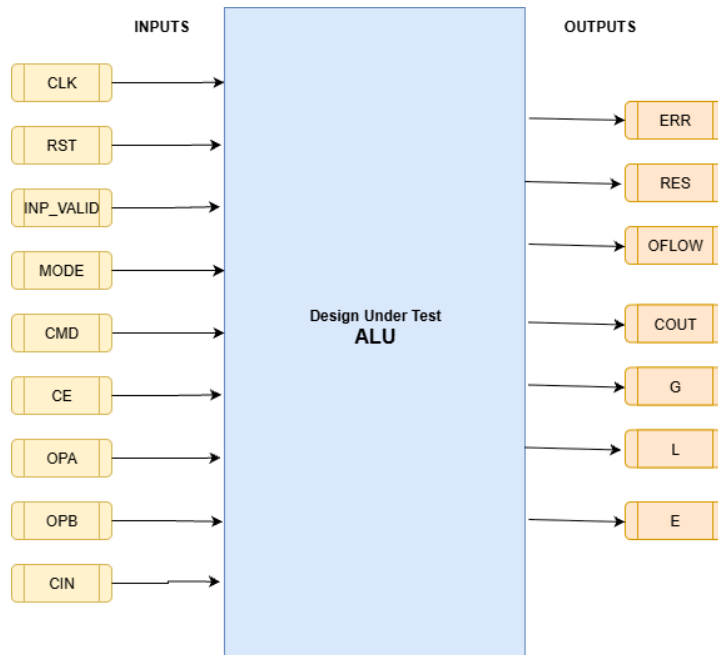
Block diagram of parameterized ALU is shown in Figure 1.

Figure 1. ALU under test

Below is the table which describes about the pins in the ALU which is design under test.

	PIN NAME	PIN DESCRIPTION
INPUTS	CLK (Clock)	Synchronous clock
	RST (Reset)	Asynchronous reset
	CE (Clock Enable)	Enables the ALU to perform operations on the clock edge
	CDM	A 4-bit command input that specifies the operation to be performed
	MODE	Determines the type of operation i.e. if MODE = 1 then Arithmetic operation else Logical operation
	CIN (Carry In)	Used for addition/subtraction with carry/borrow
	OPA / OPB [Width-1:0]	Parameterized inputs for operand A and operand B
	INP_VALID	It is a 2-bit input which indicates validity of input operands i.e. 00: No operand is valid 01: Operand A is valid 10: Operand B is valid 11: Both operands are valid
OUTPUTS	ERR	Error signal for invalid operations
	RES [Width-1:0]	Result from the logical or arithmetic operation
	G, L, E	Comparator outputs indicating relationship between operands i.e. greater-than, less-than and equal-to
	COUT	Carry out for arithmetic operation
	OFLOW	Overflow flag for arithmetic operation

Below is the table for the ALU showing specific arithmetic operation cases for given inputs, where the resulting outputs must be carefully considered as follows:

Command number	Command Operation	Description	ALU Behaviour / Operation	Flags Affected
0	ADD	Unsigned Addition	RES = OPA + OPB	COUT, OFLOW
1	SUB	Unsigned Subtraction	RES = OPA - OPB	COUT, OFLOW
2	ADD_CIN	Addition with Carry-In	RES = OPA + OPB + CIN	COUT, OFLOW
3	SUB_CIN	Subtraction with Borrow (Carry-In)	RES = OPA - OPB - CIN	COUT, OFLOW
4	INC_A	Increment A	RES = OPA + 1	OFLOW
5	DEC_A	Decrement A	RES = OPA - 1	OFLOW
6	INC_B	Increment B	RES = OPB + 1	OFLOW
7	DEC_B	Decrement B	RES = OPB - 1	OFLOW
8	CMP	Compare A and B	Sets G, L, E based on comparison	G, L, E
9	INC_A_B_MUL	Increment A and B, then multiply	RES = (OPA + 1) * (OPB + 1)	-
10	SHL_A_MUL_B	Left shift A by 1, then multiply with B	RES = (OPA << 1) * OPB	-
11	ADD_SIGNED	Signed Add, sets all relevant flags	RES = OPA + OPB with signed consideration	COUT, OFLOW, G, L, E
12	SUB_SIGNED	Signed Subtract, sets all relevant flags	RES = OPA - OPB with signed consideration	COUT, OFLOW, G, L, E

The designed ALU supports various logical operations when the signal MODE is deasserted which includes AND, OR, NAND, NOR, XOR, XNOR, NOT_A, NOT_B, SHR1_A, SHL1_A, SHR1_B, SHL1_B, ROL_A_B (Rotate Left A by bits specified in B), ROR_A_B (Rotate Right A by bits specified in B)

Below is the table for the ALU showing specific logical operation cases for given inputs, where the resulting outputs must be carefully considered as follows:

Command number	Command Operation	Description	ALU Behaviour / Operation	Flags Affected
0	AND	Bitwise AND between A and B	RES = OPA & OPB	-
1	NAND	Bitwise NAND between A and B	RES = ~ (OPA & OPB)	-
2	OR	Bitwise OR between A and B	RES = OPA | OPB	-
3	NOR	Bitwise NOR between A and B	RES = ~ (OPA | OPB)	-
4	XOR	Bitwise XOR between A and B	RES = OPA ^ OPB	-
5	XNOR	Bitwise XNOR between A and B	RES = ~ (OPA ^ OPB)	-
6	NOT_A	Bitwise NOT of A	RES = ~OPA	-
7	NOT_B	Bitwise NOT of B	RES = ~OPB	-
8	SHR1_A	Shift Right A by 1	RES = OPA >> 1	-
9	SHL1_A	Shift Left A by 1	RES = OPA << 1	-
10	SHR1_B	Shift Right B by 1	RES = OPB >> 1	-
11	SHL1_B	Shift Left B by 1	RES = OPB << 1	-
12	ROL_A_B	Rotate Left A by bits specified in B	Rotate A left by the lowest bits of B needed to cover the operand width; set ERR if any higher bits of B, are nonzero.	ERR

13	ROR_A_B	Rotate Right A by bits specified in B	Rotate A right by the lowest bits of B needed to cover the operand width; set ERR if any higher bits of B, are nonzero.	ERR

CHAPTER 2: TESTBENCH ARCHITECTURE AND METHODOLOGY

2.1 TESTBENCH ARCHITECTURE
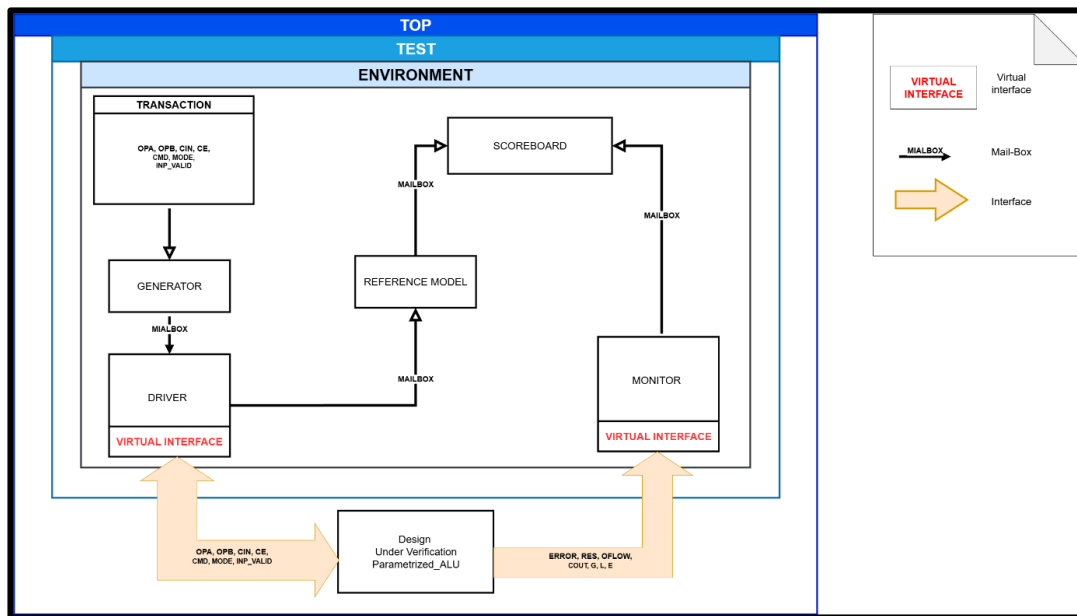
GENERAL TESTBENCH ARCHITECTURE

Figure 1. General Testbench Architecture

ALU TESTBENCH ARCHITECTURE
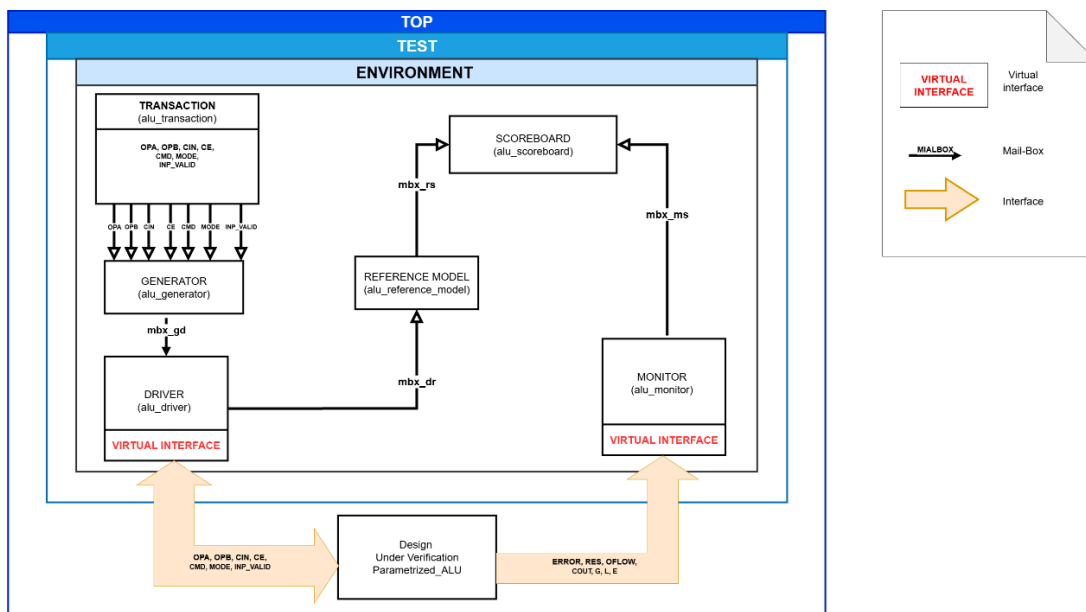

Figure 2. ALU Testbench Architecture

2.2 COMPONENT DETAILS AND FLOWCHART

The ALU testbench architecture consist as follows:

Transaction Class:

- All the inputs and outputs used by the ALU (like OPA, OPB, CIN, CE, CMD, MODE, and INP_VALID) are included in the transaction class.
- Clock and reset signals are excluded since they are generated in the Top module.
- The transaction class can also contain constraints on the input values to generate meaningful scenarios (e.g., valid operand ranges, operation types).
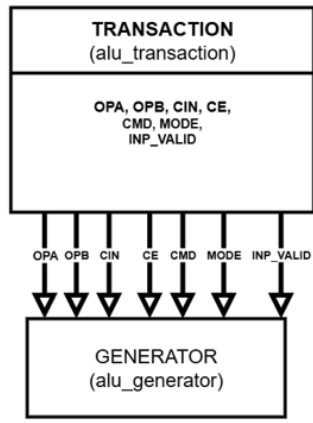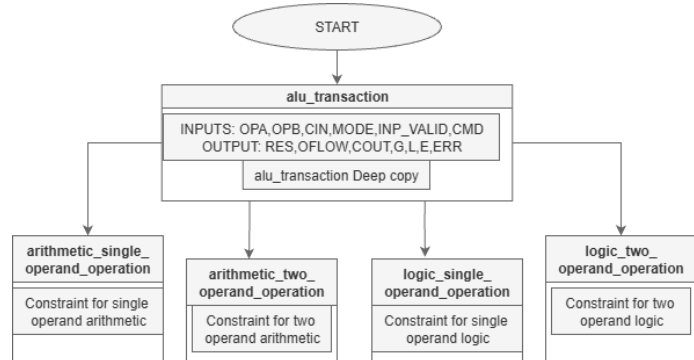

Figure 3. ALU_Transaction block   Figure 4. Flowchart of ALU_Transaction Class

Generator:

- This component creates random input combinations for the ALU, respecting the constraints defined in the transaction class.
- It generates transactions and sends them to the driver using a mailbox.
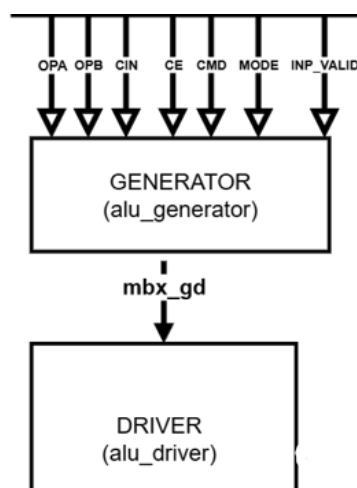- The generator helps cover different kinds of operations and edge cases.
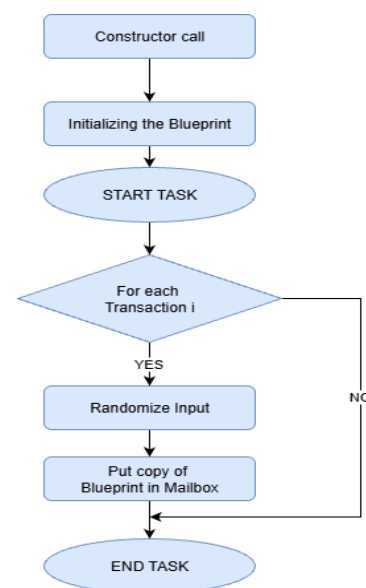

Figure 5. ALU_Generator Block   Figure 6. Flowchart of ALU_Generator

Driver:

- The driver receives transactions from the generator and applies them to the ALU inputs using a virtual interface.
- It translates the high-level transaction data into signal activity on the ALU pins.
- It also forwards the same transactions to the reference model, which is used for checking expected behaviour.
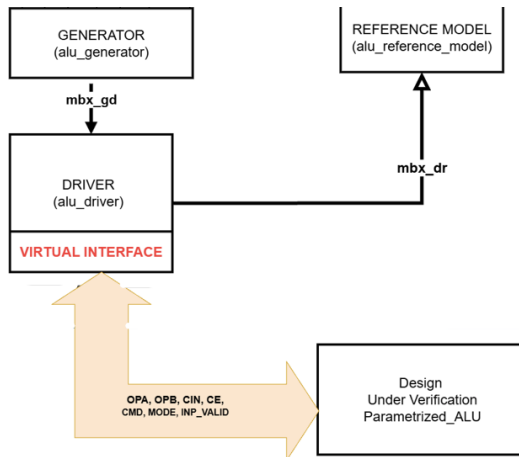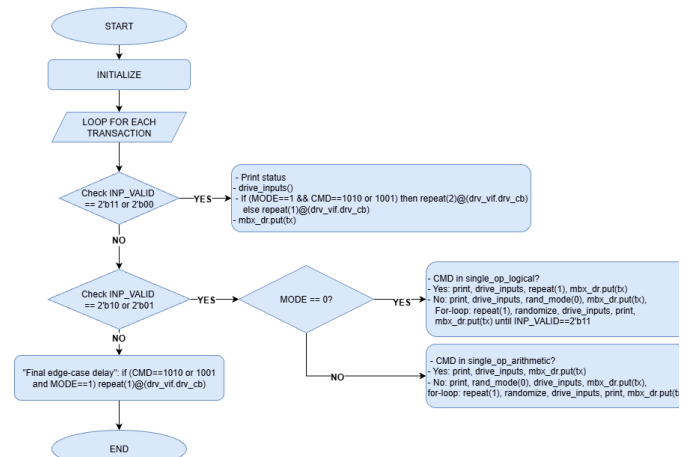

Figure 7. ALU_Driver Block   Figure 8. Flowchart of ALU_Driver

Monitor:

- The monitor observes the outputs of the ALU (like RES, COUT, OFLOW, ERR, G, L, and E) using a virtual interface.
- It converts these low-level signals into a high-level transaction and sends them to the scoreboard through a mailbox.
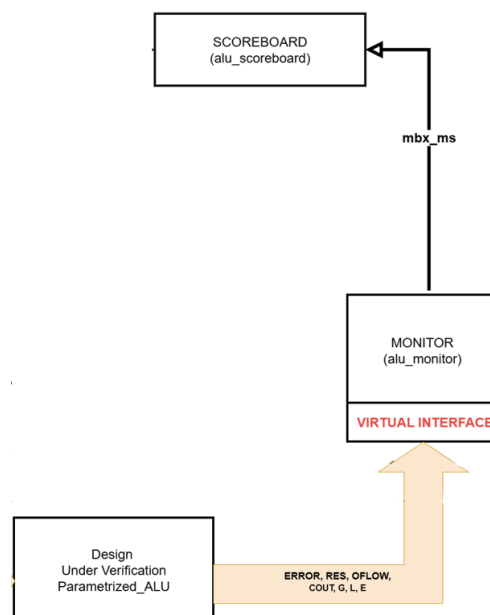
Figure 9. ALU_Monitor Block
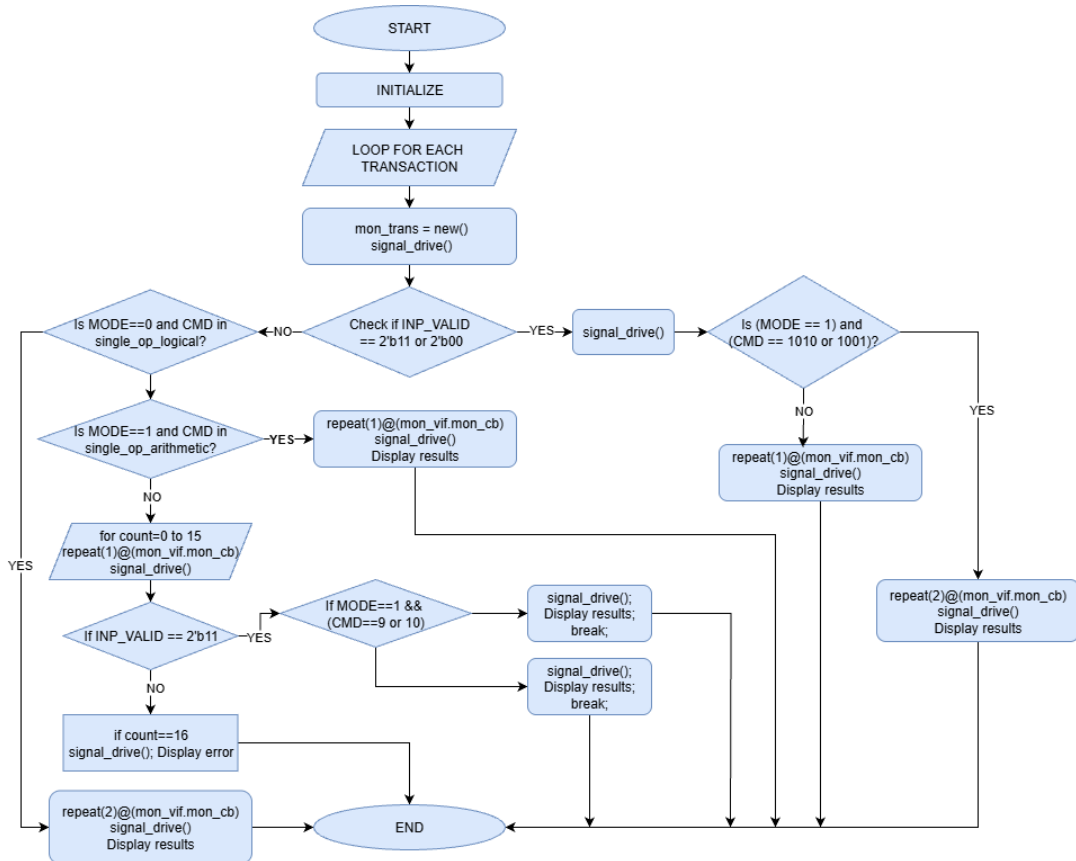
Figure 10. Flowchart of ALU_Monitor

Reference Model:

- This is the ideal or "golden" model of the ALU, implemented at a high level.
- It performs the same operation as the real ALU using the input transaction and produces the expected output.
- The input to the reference model comes from the driver, and its output is passed to the scoreboard for comparison.

Figure 11. ALU_Reference_Model Block
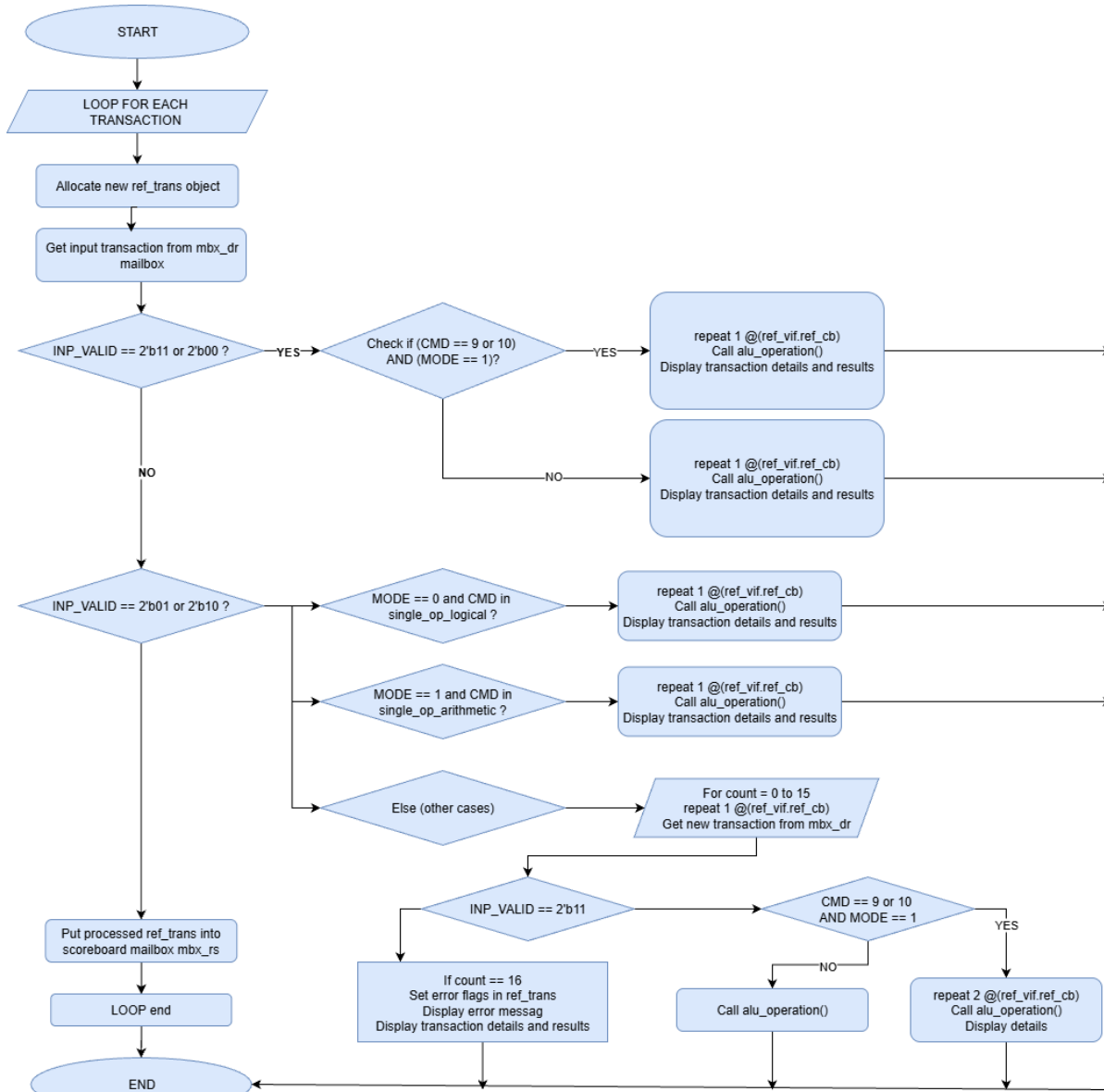
Figure 12. Flowchart of ALU_Reference_Model

Scoreboard:

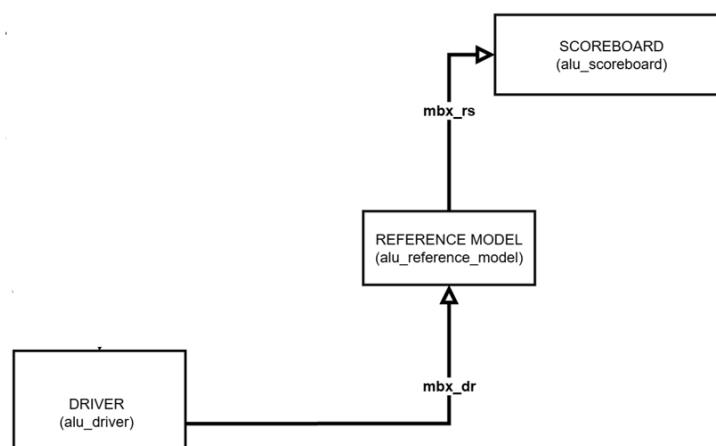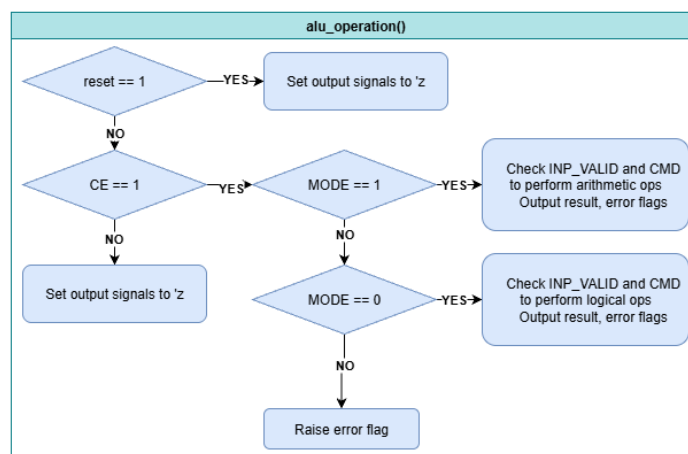- The scoreboard compares the expected output from the reference model with the actual output from the monitor.
- If the values match, the test passes; otherwise, it logs a mismatch and raises an error.
- The scoreboard is central to identifying bugs or mismatches in ALU functionality.
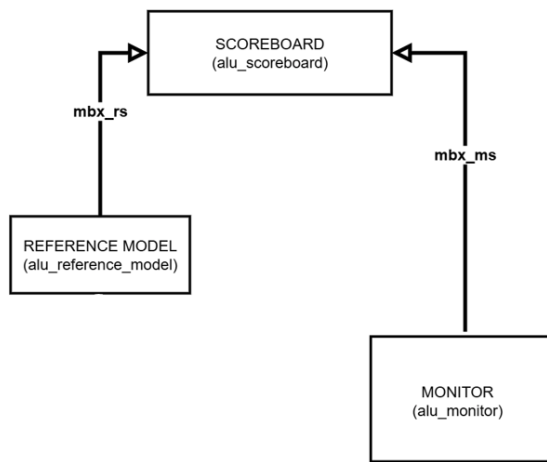
Figure 13. ALU_ScoreBoard
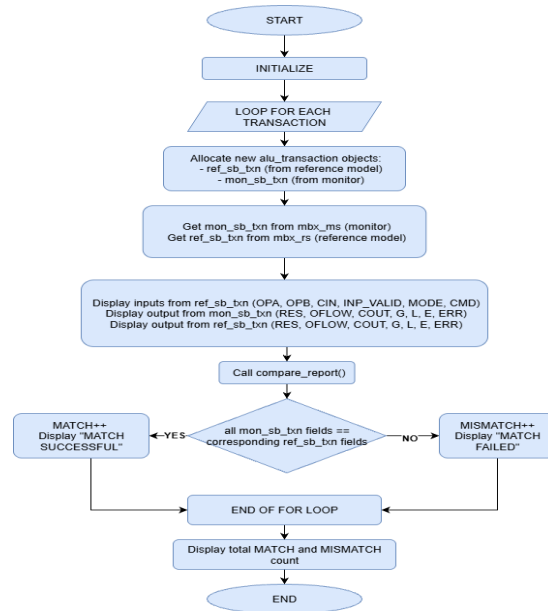
Figure 14. Flowchart of ALU_Scoreboard

Environment:

- The environment contains all the above components: generator, driver, monitor, reference model, and scoreboard.
- It handles their construction, configuration, and connection using mailboxes and virtual interfaces.
- The environment acts as a container for building the full testbench.

Test:

- This is where different test cases are defined (e.g., testing addition, subtraction, overflow, rotate, etc.).
- The test instantiates the environment and runs specific scenarios.
- It is written inside a class and helps run both directed and randomized tests.

CHAPTER 3: VERIFICATION RESULT AND ANALYSIS

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3.1 ERROR IN THE DUT

- The increment operation on operand A (OPA) is incorrect according to the specification
- The operation of increment and decrement on operand B (OPB) is incorrect according to the specification
- CMD 13 performs a left rotation instead of the required right rotation, leading to incorrect output
- When OPB[7:4] ≠ 0 in CMD 13, the ERR flag is not set, failing to indicate an invalid input condition
- RES is declared with a hardcoded width [8:0] instead of using parameter DW, breaking scalability
- The design does not verify INP_VALID = 2'b11 before executing dual-operand commands, allowing operations with missing operands
- For single-operand operations, the design accepts both operands instead of ignoring the unused one
- There is no priority handling when one operand arrives late (beyond 16 cycles) the later operand should overwrite the earlier one but does not
- The ALU does not flag an error when only one operand is present for operations that require both
- The command (CMD) is not validated against the required number of operands before execution, leading to unexpected behaviour
- Connection width does not match the declared port width for RES, causing simulation or synthesis issues

3.2 COVERAGE REPORT

Below is the coverage report obtained on verifying the ALU design.

Input Coverage:

Figure 15. shows the input coverage for the ALU

Scope: /alu_pkg/alu_driver

Covergroup type:

drv_cg

Summary	Total Bins	Hits	Hit %
Coverpoints	30	29	96.66%
Crosses	104	58	55.76%

Search: [ ]

CoverPoints ▲	Total Bins	Hits	Misses	Hit %	Goal %	Coverage %
A_cp	3	3	0	100.00%	100.00%	100.00%
B_cp	3	3	0	100.00%	100.00%	100.00%
CIN_cp	2	2	0	100.00%	100.00%	100.00%
CMD_cp	16	15	1	93.75%	93.75%	93.75%
INP_VALID_cp	4	4	0	100.00%	100.00%	100.00%
MODE_cp	2	2	0	100.00%	100.00%	100.00%

Search: [ ]

Crosses ▲	Total Bins	Hits	Misses	Hit %	Goal %	Coverage %
CMD_x_INP_VALID	64	28	36	43.75%	43.75%	43.75%
MODE_x_CMD	32	22	10	68.75%	68.75%	68.75%
MODE_x_INP_VALID	8	8	0	100.00%	100.00%	100.00%

Figure 15. Input Coverage for ALU

Output Coverage:

Figure 16. shows the output coverage for the ALU

Scope: /alu_pkg/alu_monitor

Covergroup type:

mon_cg

Summary	Total Bins	Hits	Hit %
Coverpoints	10	8	80.00%
Crosses	0	0	0.00%

Search: [ ]

CoverPoints ▲	Total Bins	Hits	Misses	Hit %	Goal %	Coverage %
COUT_CP	2	2	0	100.00%	100.00%	100.00%
EQUAL	1	0	1	0.00%	0.00%	0.00%
ERROR	2	2	0	100.00%	100.00%	100.00%
GREATER	1	0	1	0.00%	0.00%	0.00%
LESSER	1	1	0	100.00%	100.00%	100.00%
OF_LOW	2	2	0	100.00%	100.00%	100.00%
RESULT	1	1	0	100.00%	100.00%	100.00%

Figure 16. Output Coverage for ALU

Assertion Coverage:

Figure 17. shows the assertion coverage for the ALU

Assertions Coverage Summary:

Search: [   ]

Assertions	Failure Count	Pass Count	Attempt Count	Vacuous Count	Disable Count	Active Count	Peak Active Count	Status
/top/intrf/assert__CE_ASSERT	0	16	139	123	0	0	16	Covered
/top/intrf/assert__TIMEOUT_16Clk	0	0	139	139	0	0	5	ZERO
/top/intrf/assert__VALID_INPUTS_CHECK	0	123	139	16	0	0	1	Covered
/top/intrf/assert__VERIFY_RESET	0	0	139	139	0	0	0	ZERO
/work.alu_if/assert__CE_ASSERT	0	16	139	123	0	0	16	Covered
/work.alu_if/assert__TIMEOUT_16Clk	0	0	139	139	0	0	5	ZERO
/work.alu_if/assert__VALID_INPUTS_CHECK	0	123	139	16	0	0	1	Covered
/work.alu_if/assert__VERIFY_RESET	0	0	139	139	0	0	0	ZERO

Figure 17. Assertion Coverage Summary for ALU

Overall Coverage:

Figure 18. shows the overall coverage for the ALU

Coverage Summary by Type:

Total Coverage:					74.21%	69.49%
Coverage Type	Bins	Hits	Misses	Weight	% Hit	Coverage
Covergroups	144	95	49	1	65.97%	80.50%
Statements	570	422	148	1	74.03%	74.03%
Branches	186	136	50	1	73.11%	73.11%
FEC Conditions	66	37	29	1	56.06%	56.06%
Toggles	310	258	52	1	83.22%	83.22%
Assertions	4	2	2	1	50.00%	50.00%

Figure 18. Overall Coverage for ALU

Output waveform:

Figure 19. shows the output waveform from the interface in the ALU testbench architecture
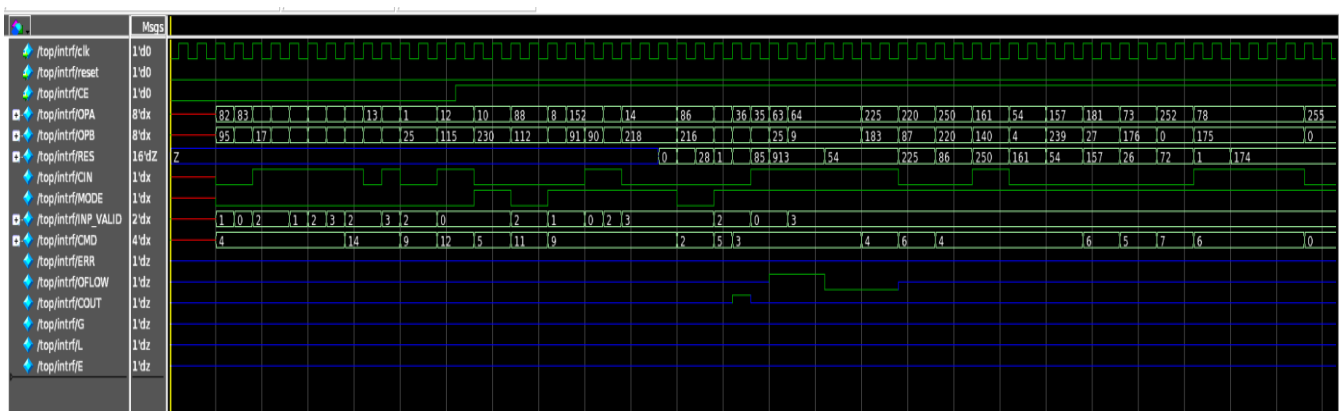

Figure 19. Output waveform from the interface in the ALU testbench architecture

CONCLUSION

The testbench for the ALU design helped identify whether the design functioned correctly. The testbench was organized into separate parts—generator, driver, monitor, reference model, and scoreboard—making it easier to test and debug each section of the design.

Several issues were found during simulation, such as incorrect handling of specific commands, missing error detection, and lack of parameterization, which reduced design flexibility. These problems were clearly visible due to the structured approach of the testbench.

FUTURE SCOPE

- The design is not fully parameterized; while DW (data width) and CW (command width) are declared as parameters, internal hardcoded values like bit widths (e.g., [8:0] for RES) should instead use parameter expressions to ensure scalability.
- The current implementation of CMD 13 performs a left-rotation instead of the required right-rotation; this must be corrected to match the expected behaviour.
- In CMD 13, when OPB [7:4] ≠ 0, the error flag (ERR) is incorrectly set to 0; it should be set to 1 to indicate an invalid rotation input, as per specification.
- The ALU does not enforce that both operands must be present (INP_VALID = 2'b11) for dual-operand commands like ADD, SUB, and MUL; operand validity checking should be enforced before processing.
- Single-operand operations such as INC_A or DEC_A do not restrict the design from accepting both operands; logic should be added to accept only the necessary operand(s).
- There is no priority logic to handle timing violations when one operand is delayed by more than 16 cycles; the later operand should overwrite the earlier one as per the requirement.
- Error handling is missing when invalid operand sequences are received (e.g., only one operand present when two are required); the design should flag an error in such cases.
- The design does not validate if the provided command (CMD) matches the expected number of operands before execution; this validation logic should be incorporated.

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TEST PLAN

Click on the link to access the test plan of the ALU : ALU_TEST_PLAN

FUNCTIONAL COVERAGE PLAN

Click on the link to access the coverage plan of the ALU : ALU_COVERAGE_PLAN

ASSERTIONS PLAN

Click on the link to access the assertion plan of the ALU : ALU_ASSERTION_PLAN