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LOW-POWER VLSI MINI PROJECT

A Project report on

Power Reduction in Half Subtractor using Cadence Tool

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CHAPTER 1

INTRODUCTION

1.1 HALF SUBTRACTOR

A half subtractor is a digital logic circuit that performs binary subtraction of two single-bit binary numbers. It has two inputs, A and B, and two outputs, DIFFERENCE and BORROW. The DIFFERENCE output is the difference between the two input bits, while the BORROW output indicates whether borrowing was necessary during the subtraction.

The half subtractor can be implemented using basic gates such as XOR and NOT gates. The DIFFERENCE output is the XOR of the two inputs A and B, while the BORROW output is the NOT of input A and the AND of inputs A and B.

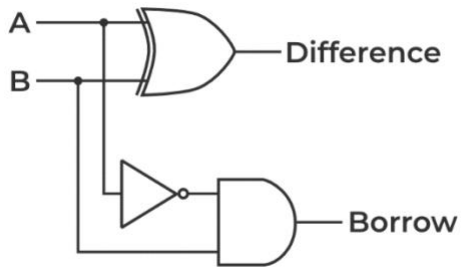

Figure 1.1 Logic circuit of Half Subtractor

The SOP form of the Diff and Borrow is as follows:

Diff= A'B+AB'

Borrow = A'B

Table 1.1 Truth Table of Half Subtractor

A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

The working of Half Subtractor referring the Table 1.1 is as follows:

- When A=0 and B=0:
  Since both inputs are 0, there's nothing to subtract. So, the difference (D) is 0.
  There's no need for borrowing, so the borrow-out (Bout) is also 0.

- When A=0 and B=1:
  Here, B is bigger than A, so we need to subtract.
  The difference (D) is 1 because we're subtracting 1 from 0.
  Since we're borrowing (taking from the next higher number), the borrow-out (Bout) is 1.
- When A=1 and B=0:
  In this case, A is bigger than B, so subtraction is needed.
  The difference (D) is 1 because we're subtracting 0 from 1.
  No borrowing is required, so the borrow-out (Bout) is 0.
- When A=1 and B=1:
  Both inputs are the same, so there's nothing to subtract. The difference (D) is 0.
  Since there's no borrowing needed, the borrow-out (Bout) is also 0.
  These scenarios show how the half subtractor works by comparing the binary numbers A and B and producing the appropriate difference and borrow-out signals based on the subtraction operation.

CHAPTER 2

IMPLEMENTATION IN CADENCE TOOL

The schematic circuit for Half Subtractor using Cadence tool is shown in Figure 2.1

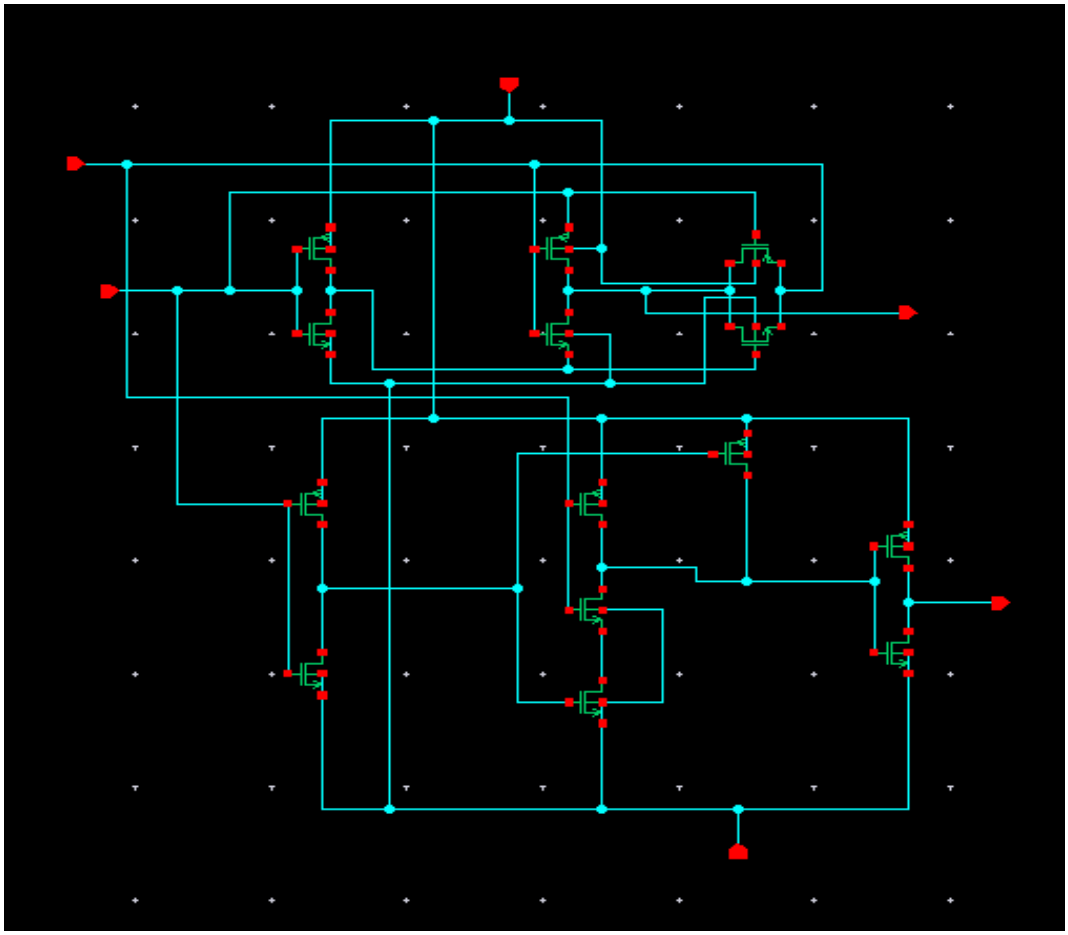

Figure 2.1 Schematic circuit of Half Subtractor

The block diagram for Half Subtractor done using Cadence tool is shown in figure 2.2

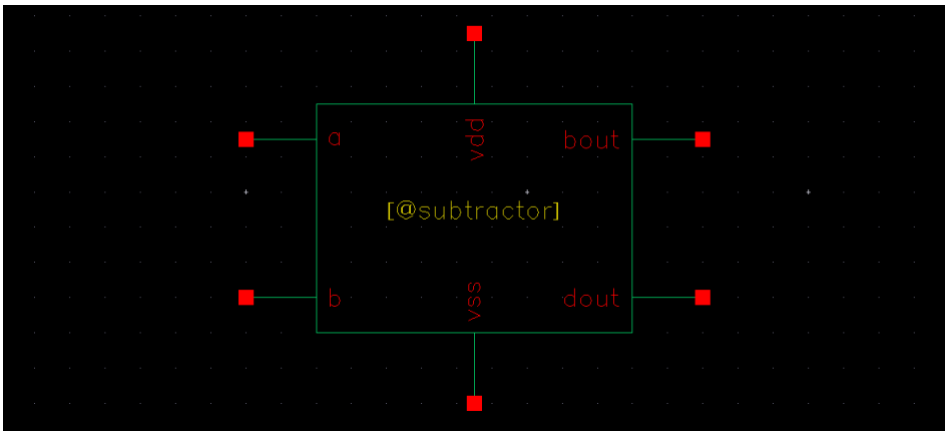

Figure 2.2 Block diagram for Half Subtractor

The test circuit for the Half Subtractor is shown in Figure 2.3 for the specification given in Table 2.1

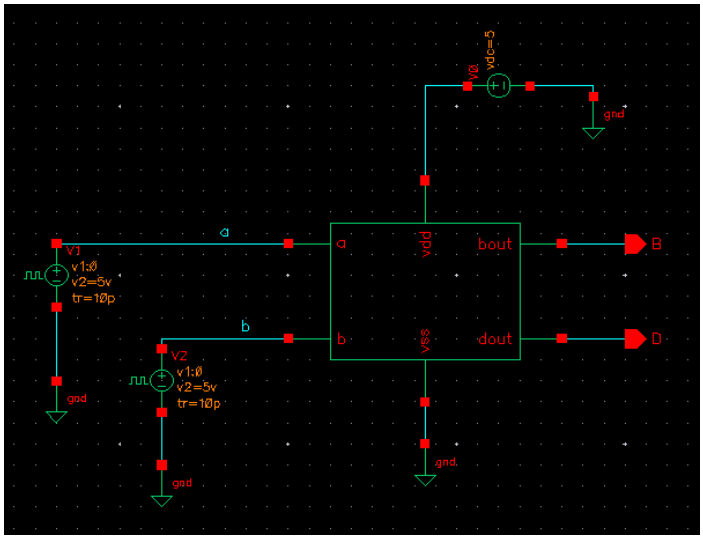

Figure 2.3 Test circuit for Half Subtractor

Table 2.1 Component Specification

Library name	Cellview name	Properties/Comments
gpdk180	pmos	W=2µ; L=180n
gpdk180	nmos	W=2µ; L=180n
subtractor_c	subtractor	Symbol
analogLib	vdc	5V
analogLib	vpulse(a)	V1=0 ; V2=5V; ton=5ns ; tp=10ns ; tr=tf=10ps
analogLib	vpulse(b)	V1=0 ; V2=5V; ton=10ns ; tp=20ns ; tr=tf=10ps

CHAPTER 3

RESULT

The output waveform of Half Subtractor is show in Figure 3.1

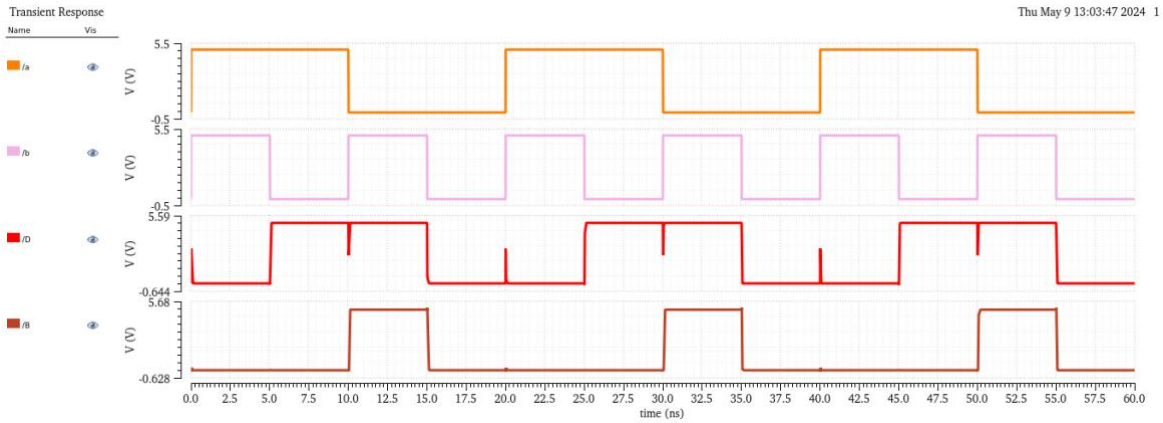

Figure 3.1 Output waveform of Half Subtractor

The transient power analysis of Half Subtractor for the values in Table 3.1 is shown in Figure 3.2 is:

Table 3.1 Power Dissipation table

β_p / β_n	PMOS	NMOS	Average Power for $V_{DD} = 5V$
1	W=2µ; L=180n	W=2µ; L=180n	131.2µW

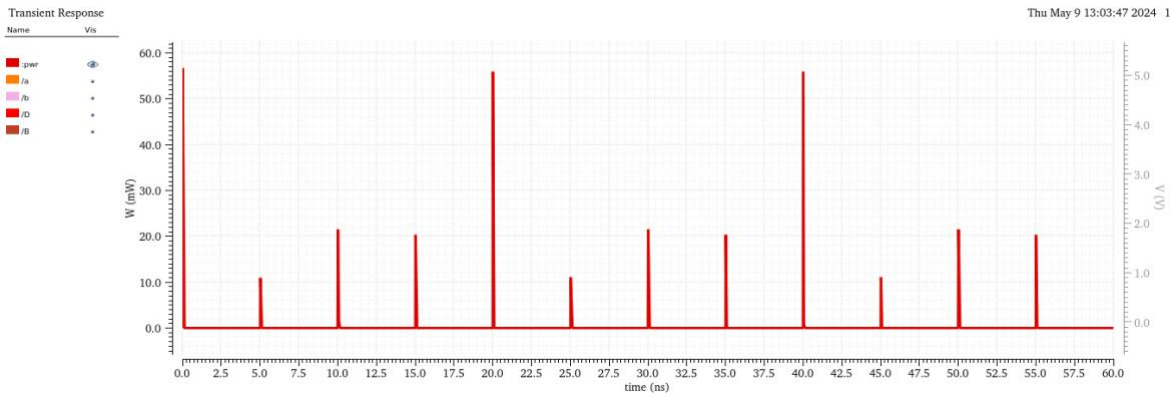

Figure 3.2 Transient Analysis of Half Subtractor

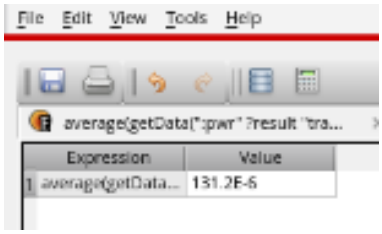

Figure 3.3 Average power shown in calculator window

Table 3.2 Power Dissipation table for different values

β_p/β_n	PMOS		NMOS		Average Power for V_{DD} = 5V	Average Power for V_{DD} = 2.5V
	W	L	W	L		
0.5	2µ	180n	4µ	180n	192.1 µW	43.08 µW
1	2µ	180n	2µ	180n	131.2 µW	29.47 µW
0.25	2µ	180n	8µ	180n	311.5 µW	70.15 µW

The analysis of the average power consumption for different configurations of the half subtractor circuit reveals notable trends and implications. Across varying βp/βn ratios and transistor dimensions, there is a discernible impact on power consumption at both 5V and 2.5V supply voltages. Notably, configurations with smaller βp/βn ratios and reduced transistor sizes tend to exhibit lower average power consumption, indicating the effectiveness of transistor sizing in managing power efficiency. Additionally, the decrease in supply voltage from 5V to 2.5V leads to a significant reduction in power consumption across all configurations, highlighting the importance of voltage scaling as a key strategy for mitigating power usage in digital circuits. These findings underscore the significance of careful transistor sizing and voltage optimization in achieving energy-efficient designs for digital circuits, crucial for a wide range of applications where power consumption is a critical consideration.