Verification Lab: 15
RAM Verification

1. Given 1024x8 Synchronous RAM. Perform directed Verification. Use tasks to obtain good code density. Identify bugs if any.

```
//memory module
 module mem1024x8(clk,
                  rst_n,
                  wr,
                  data_in,
                  address,
                  data_out);

   input wr,clk,rst_n;
   input [7:0]data_in;
   input [9:0] address;
   output [7:0]data_out;

 reg  [7:0] mem [0:1024]; // Memory Array 1024x8
 reg [7:0] data_out;
 integer i;
 wire [9:0] mem_address = {address[9:1],1'b1};
 always @(posedge clk or negedge rst_n)
 begin
  if(!rst_n)
  begin
    for(i=0;i<1024;i=i+1)
      mem[i]<=8'd0;
  end
  else if(wr)
   mem[mem_address]<=data_in;
  else
    data_out<=mem[mem_address];
end
endmodule
```