Verification Lab: 14
Mod10 Counter Verification

1. Given a mod10 counter with load facility. The behavior of the circuit is load would be valid for one clock pulse along with data in. The counter should start count from data in and roll over to zero after 9.
   a) Develop Test environment (test bench)
   b) Display the count values on standard output. Identify and fix the bugs if any.

```
//four bit mod 10 counter with load//
module mod10counter (clk,rst,count,load,din);
input clk,rst,load;
input [0:3]din;
output [0:3]count;
reg[0:3]count;
always@(posedge clk or negedge rst)
  begin
    if(rst)
      count <= 4'd0;
    else if(load)
      count <= din;
    else if(count < 4'd10)
      count <= count + 4'd1;
  end

endmodule
```