#100 DAYS OF RTL

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Description:

An **8-bit Demultiplexer (1:8 DEMUX)** takes a single input and routes it to one of eight outputs depending on a 3-bit select line.

Objective:

To learn how to implement a **1-to-8 Demultiplexer** using select logic and verify its operation through simulation.

Inputs:

- **d**: 1-bit data input.
- **s[2:0]**: 3-bit select line.

Outputs:

- **y[7:0]**: 8-bit output vector, only one bit is active HIGH at any time based on the select lines.

Design Approach:

- The demultiplexer decodes the 3-bit select input s to activate one of the 8 outputs.
- Logical AND gates combined with NOT/INVERT logic are used to direct the single input d to the selected output line.
- Only one output bit will be HIGH for any given select input.

Verilog Code:

8-bit Demultiplexer

```
module eb_demux(
   input d,
   input [2:0] s,
   output [7:0] y
);
```

```
    assign y[0] = (d & ~s[0] & ~s[1] & ~s[2]);
    assign y[1] = (d & ~s[0] & ~s[1] &  s[2]);
    assign y[2] = (d & ~s[0] &  s[1] & ~s[2]);
    assign y[3] = (d & ~s[0] &  s[1] &  s[2]);
    assign y[4] = (d &  s[0] & ~s[1] & ~s[2]);
    assign y[5] = (d &  s[0] & ~s[1] &  s[2]);
    assign y[6] = (d &  s[0] &  s[1] & ~s[2]);
    assign y[7] = (d &  s[0] &  s[1] &  s[2]);
endmodule
```

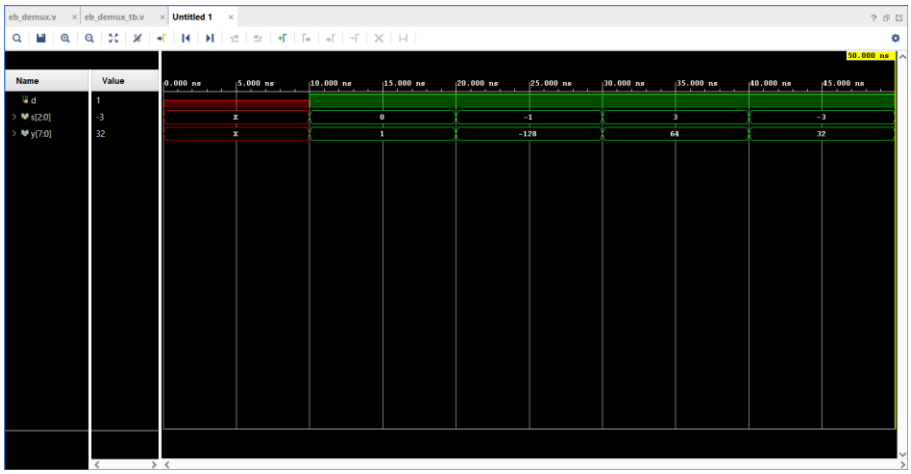
Testbench:

```
module eb_demux_tb;
    reg d;
    reg [2:0] s;
    wire [7:0] y;

    eb_demux dut (d, s, y);

    initial begin
        #10;
        s = 3'b000; d = 1'b1;  // Activates y[0]
        #10;
        s = 3'b111; d = 1'b1;  // Activates y[7]
        #10;
        s = 3'b011; d = 1'b1;  // Activates y[3]
        #10;
        s = 3'b101; d = 1'b1;  // Activates y[5]
        #10;
        $finish();
    end
endmodule
```

Waveform:



Schematic: