#100 DAYS OF RTL

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Description:

A Full Subtractor subtracts two binary digits along with a borrow input and outputs the difference and borrow output. A 4-bit Ripple Borrow Subtractor connects four full subtractors sequentially to handle multi-bit subtraction.

Objective:

Understand multi-bit binary subtraction and learn how borrow signals propagate across stages.

Inputs:

- a: 4-bit binary input
- b: 4-bit binary input
- bin: 1-bit initial borrow input

Outputs:

- d: 4-bit output representing the difference
- bor: 1-bit final borrow output

Design Approach:

- Use four Full Subtractors in series.
- Each stage calculates its own difference and passes a borrow to the next stage.
- Use XOR and basic logic gates to compute difference and borrow.

Verilog Code:

Full Subtractor

```
`timescale 1ns / 1ps
module full_sub(
   input a,
   input b,
   input bin,
   output d,
   output bor
);
   assign d = a ^ b ^ bin;
   assign bor = (~a & b) | (b & bin) | (bin & ~a);
endmodule
```

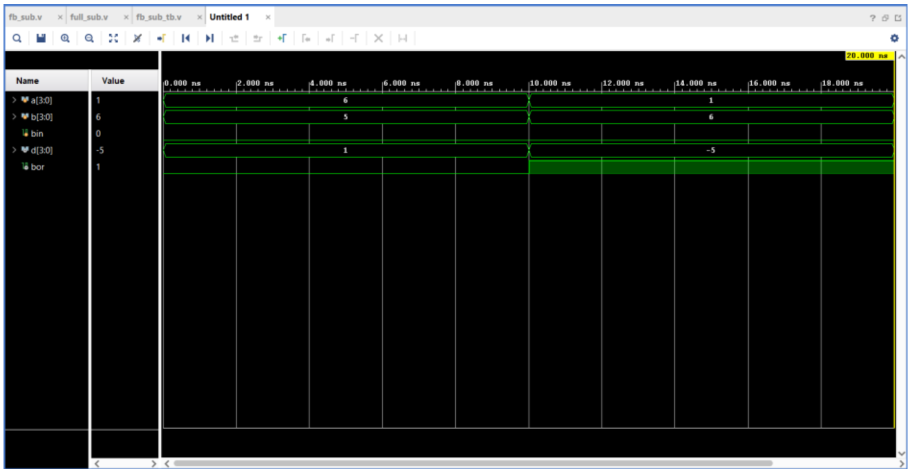
A 4-bit Ripple Borrow Subtractor

```
module fb_sub(
    input [3:0] a,
    input [3:0] b,
    input bin,
    output [3:0] d,
    output bor,
    wire b1, b2, b3
);
    full_sub s1(a[0], b[0], bin, d[0], b1);
    full_sub s2(a[1], b[1], b1, d[1], b2);
    full_sub s3(a[2], b[2], b2, d[2], b3);
    full_sub s4(a[3], b[3], b3, d[3], bor);
endmodule
```

Testbench:

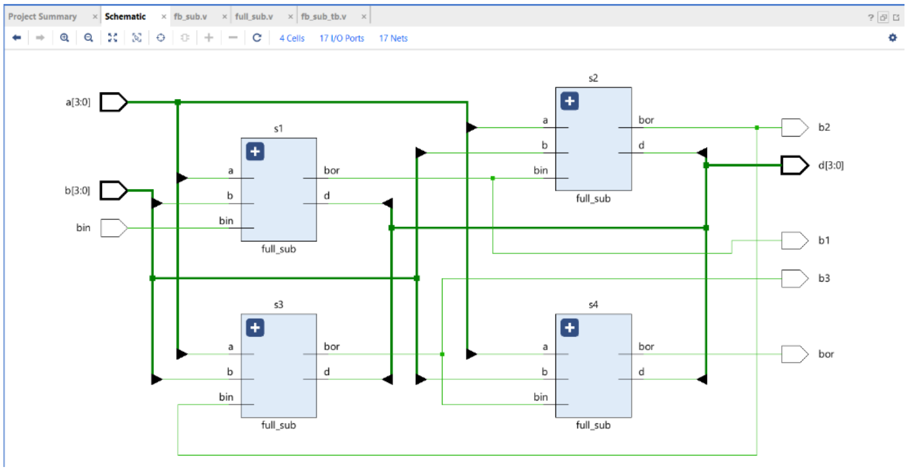
```
module fb_sub_tb;
    reg [3:0] a, b;
    reg bin;
    wire [3:0] d;
    wire bor;

    fb_sub dut (a, b, bin, d, bor);

    initial begin
        bin = 1'b0;
        a = 4'b0110; b = 4'b0101; // Test case 1
        #10;
        a = 4'b0001; b = 4'b0110; // Test case 2
        #10;
        $finish();
    end
endmodule
```

Waveform:



Name	Value
a[3:0]	1
b[3:0]	6
bin	0
d[3:0]	-5
bor	1

Schematic:



Project Summary
Schematic
fb_sub.v
full_sub.v
fb_sub_tb.v
4 Cells
17 I/O Ports
17 Nets
a[3:0]
b[3:0]
bin
s1
a
b
bin
bor
d
full_sub
s2
a
b
bin
bor
d
full_sub
s3
a
b
bin
bor
d
full_sub
s4
a
b
bin
bor
d
full_sub
b2
d[3:0]
b1
b3
bor