#100 DAYS OF RTL

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Description:

A 4-bit Comparator compares two 4-bit binary numbers a and b, and outputs three flags:

- a_gt_b – Indicates if A is greater than B
- a_lt_b – Indicates if A is less than B
- a_eq_b – Indicates if A is equal to B

Objective:

Learn to perform binary comparisons using relational operators and generate status flags accordingly.

Inputs:

- a: 4-bit binary input
- b: 4-bit binary input

Outputs:

- a_gt_b: High if A > B
- a_eq_b: High if A == B
- a_lt_b: High if A < B

Design Approach:

- Use Verilog's built-in relational operators (>, <, ==) to compare two 4-bit inputs.
- Each result is assigned to a separate output flag.

Verilog Code:

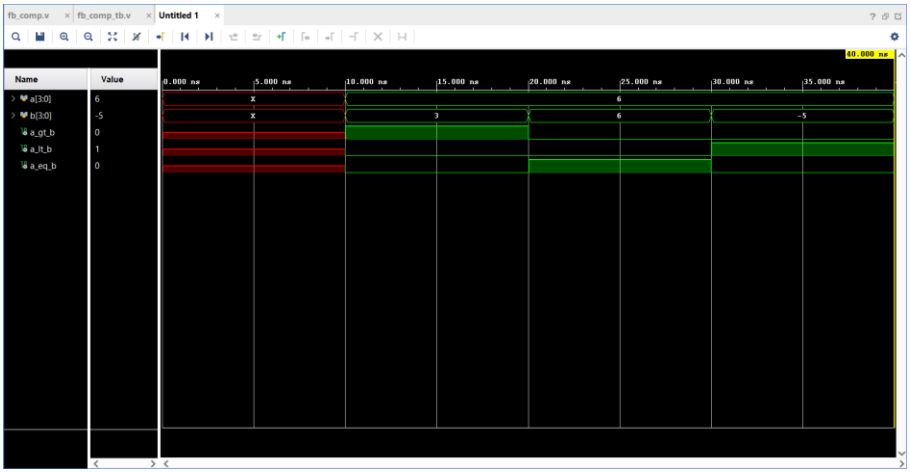
```
module fb_comp(
   input [3:0] a,
   input [3:0] b,
   output a_gt_b,
```

```
    output a_lt_b,
    output a_eq_b
);
    assign a_gt_b = (a > b);
    assign a_eq_b = (a == b);
    assign a_lt_b = (a < b);
endmodule
```

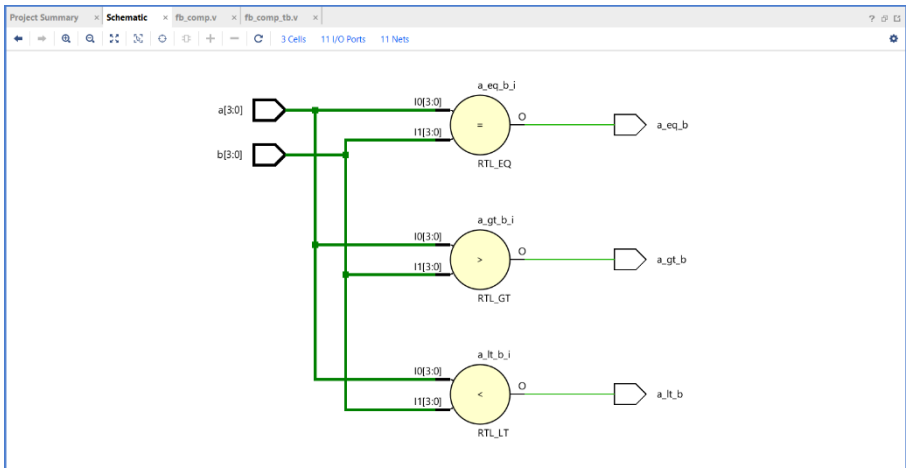
Testbench:

```
module fb_comp_tb;
    reg [3:0] a, b;
    wire a_gt_b, a_lt_b, a_eq_b;

    fb_comp dut (a, b, a_gt_b, a_lt_b, a_eq_b);

    initial begin
        #10
        a = 4'b0110; b = 4'b0011; // A > B
        #10;
        a = 4'b0110; b = 4'b0110; // A == B
        #10;
        a = 4'b0110; b = 4'b1011; // A < B
        #10;
        $finish();
    end
endmodule
```

Waveform:



Schematic:


Project Summary
Schematic
fb_comp.v
fb_comp_tb.v
3 Cells
11 I/O Ports
11 Nets
a[3:0]
b[3:0]
a_eq_b_i
I0[3:0]
I1[3:0]
=
O
RTL_EQ
a_eq_b
a_gt_b_i
I0[3:0]
I1[3:0]
>
O
RTL_GT
a_gt_b
a_lt_b_i
I0[3:0]
I1[3:0]
<
O
RTL_LT
a_lt_b