#100 DAYS OF RTL

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Description:

A Half Adder adds two binary digits and outputs the sum and carry.

Objective:

Understand basic combinational logic and implement simple binary arithmetic.

Inputs:

- a: 1-bit binary input
- b: 1-bit binary input

Outputs:

- sum: 1-bit output representing A ^ B
- cout: 1-bit output representing A & B

Design Approach:

Use basic logic gates (XOR and AND) to compute the sum and carry.

Verilog Code:

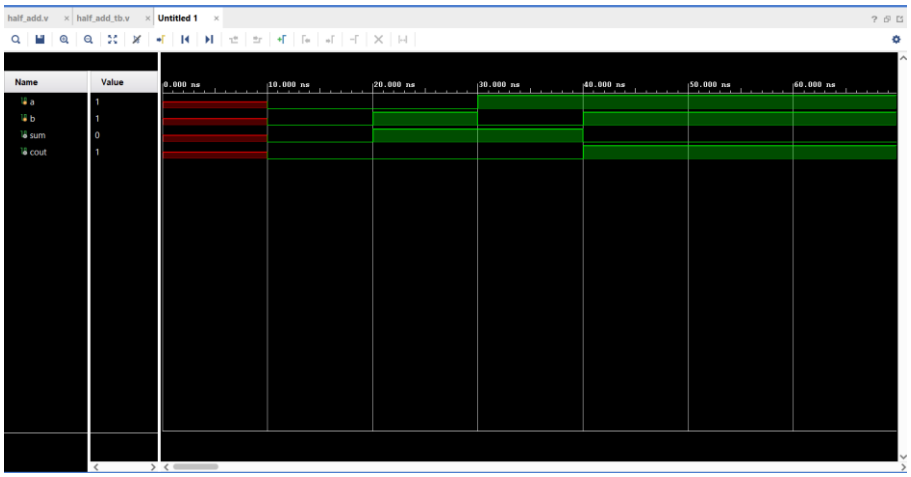
```
module half_add(
input a,
input b,
output sum,
output cout
   );

   assign sum = a^b;
   assign cout = a&b;
endmodule
```

Testbench:

```
module half_add_tb;
reg a;
reg b;
wire sum;
wire cout;
half_add dut (a,b,sum,cout);
initial
begin
#10 a = 1'b0; b=1'b0;
#10 a = 1'b0; b=1'b1;
#10 a = 1'b1; b=1'b0;
#10 a = 1'b1; b=1'b1;
end
endmodule
```

Waveform:



Schematic: