

EE-309: Microprocessor

Project 1: IITB-RISC

Multi-Cycle Implementation

Team:

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R Type Instruction format

Opcode (4 bit)	Register A (RA) (3 bit)	Register B (RB) (3-bit)	Register B (RB) (3-bit)	Unused (1 bit)	Condition (CZ) (2 bit)
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I Type Instruction format

Opcode (4 bit)	Register A (RA) (3 bit)	Register C (RC) (3-bit)	Immediate (6 bits signed)
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J Type Instruction format

Opcode (4 bit)	Register A (RA) (3 bit)	Immediate (9 bits signed)
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Instructions Encoding:

ADD:	00_01	RA	RB	RC	0	00
ADC:	00_01	RA	RB	RC	0	10
ADZ:	00_01	RA	RB	RC	0	01
ADL:	00_01	RA	RB	RC	0	11
ADI:	00_00	RA	RB	6 bit Immediate		
NDU:	00_10	RA	RB	RC	0	00
NDC:	00_10	RA	RB	RC	0	10
NDZ:	00_10	RA	RB	RC	0	01
LHI:	00_00	RA	9 bit Immediate			
LW:	01_11	RA	RB	6 bit Immediate		
SW:	01_01	RA	RB	6 bit Immediate		
LM:	11_00	RA	0 + 8 bits corresponding to Reg R0 to R7 (right to left)			
SM:	11_01	RA	0 + 8 bits corresponding to Reg R0 to R7 (right to left)			
BEQ:	10_00	RA	RB	6 bit Immediate		
JAL:	10_01	RA	9 bit Immediate offset			
JLR:	10_10	RA	RB	000_000		
JRI	10_11	RA	9 bit Immediate offset			

Project Aims:-

Designing multi-cycle processor, IITB-RISC-22 with its instruction set architecture given. It is a 16-bit very simple computer developed for teaching based on Computer Architecture. It is implemented using 8-registers, 16-bit system using VHDL as hardware description language that uses point to point communication infrastructure.

ALU :

→ takes 2 vectors of size 16-bit and performs addition & NAND operations according to another input and gives output vector of performed operation and C & Z flags.

Immediate - 6bit and 9bit:-

These components extend sign of input vectors of size 6, 9 bits to vector size - 16.

Memory Unit:-

This component outputs the data in given address if read input is '1' & writes given data if write is '1' and there's a rise in edge of clock (CLK).

Register - file:-

This consists of 8 registers which we use according to the state where we are currently in.

RISU unit:-

This is important unit of machine. It integrates various sub-components we already implemented. This is a ~~memory~~ really machine as output depends on input - (FSM).

This takes opcode & values of C, Z registers as input to give output.

→ There are 3 machine code instruction formats R, I, J and total of 15 instructions.

States:-

(S1)

PC → mem-A
mem-D → IR
PC → ALU-A
r2 → ALU-B
ALU-C → T4

(S2)

IR {8-0} → LE-16
LE-16 → T1

(S3)

T1 → RF-D3
IR {11-9} → RF-A3
T4 → PC

(S4)

IR {11-9} → RF-A₁
 IR {8-6} → RF-A₂
 RF-D₁ → T₁
 RF-D₂ → T₂

(S5)

T₁ → ALU-A
 T₂ → ALU-B
 ALU-C → T₁
 ALU-Z → Z
 ALU-CA → C
 Subtraction.

(S6)

T₁ → RF-D3
 IR {5-3} → RF-A3
 T₄ → PC

(S7)

IR {11-9} → RF-A1
 RF-D1 → T1
 IR {5-0} → SE-16
 SE-16 → T2

(S8)

IR {8-6} → RE-A2
 RF-D2 → T2
 IR {5-0} → SE-16
 SE-16 → T1

(S9)

IR {4-9} → RE-A1
 RE-A1 → T1
 '000' → T2

(S10)

T₁ + mem-A
 Mem-D → T₃

(S11)

T₃ → RF-D3
 T₂ {2-0} → RF-A3
 T₂ → ALU-A
 T₁ → ALU-B
 ALU-C → T₂

(S12)

T₁ → ALU-A
 T₂ → ALU-B
 ALU-C → T₄
 T₄ → PC

(S13)

T₂ → ALU-A
 T₁ → ALU-B
 ALU-C → T₂

(S14)

IR {8-6} → RE-A1
 ↓
 RE-A1
 RE-D4 → PC

(S15)

T₂ → ALU-A
 T₁ → ALU-B
 ALU-C → T₂

(S16)

T₂ {2-0} → RE-A2
 RF-D₂ → T₃
 T₁ → Mem-A
 T₂ → Mem-D

(S18)

PC → ALU-A
 IR {5-0} → SE-16
 SE-16 → ALU-B
 ALU-C → PC

(S19)

T₁ → mem-A
 mem-D → RF-D3
 IR {11-9} → RF-A3
 T₄ → PC

S20

$IR_{11-9} \rightarrow RF-A1$

$RF-D1 \rightarrow T2$

$T1 \rightarrow mem-A$

$T2 \rightarrow mem-D$

S21

$T1 \rightarrow RF-D3$

$IR_{8-6} \rightarrow RF-A3$

$T4 \rightarrow PC$

S22

$PC \rightarrow RF-D3$

$IR_{11-9} \rightarrow RF-A3$

S23

$IR_{11-9} \rightarrow RF-A2$

$RF-D2 \rightarrow T1$

$T1 \rightarrow ALU-A$

$Imm9 \rightarrow ALU-B$

$ALU-out \rightarrow PC$

ADD, ADC, ADZ, AD2

(S1) → (S4) → (S5) → (S6)

ADI

(S1) → (S7) → (S5) → (S21)

NDU, NDC, NDZ

(S1) → (S4) → (S5) → (S6)

LHI

(S1) → (S2) → (S3)

LW

(S1) → (S8) → (S5) → (S19)

SW

(S1) → (S8) → (S5) → (S20)

LM

(S1) → (S9) → (S10) → (S11) → (S12)
if $T2 < 8$

SM

(S1) → (S9) → (S16) → (S13) → (S12)
if $T2 < 8$

BEQ

(S1) → (S4) → (S5) → (S18)

JAL

(S1) → (S22) → (S14)

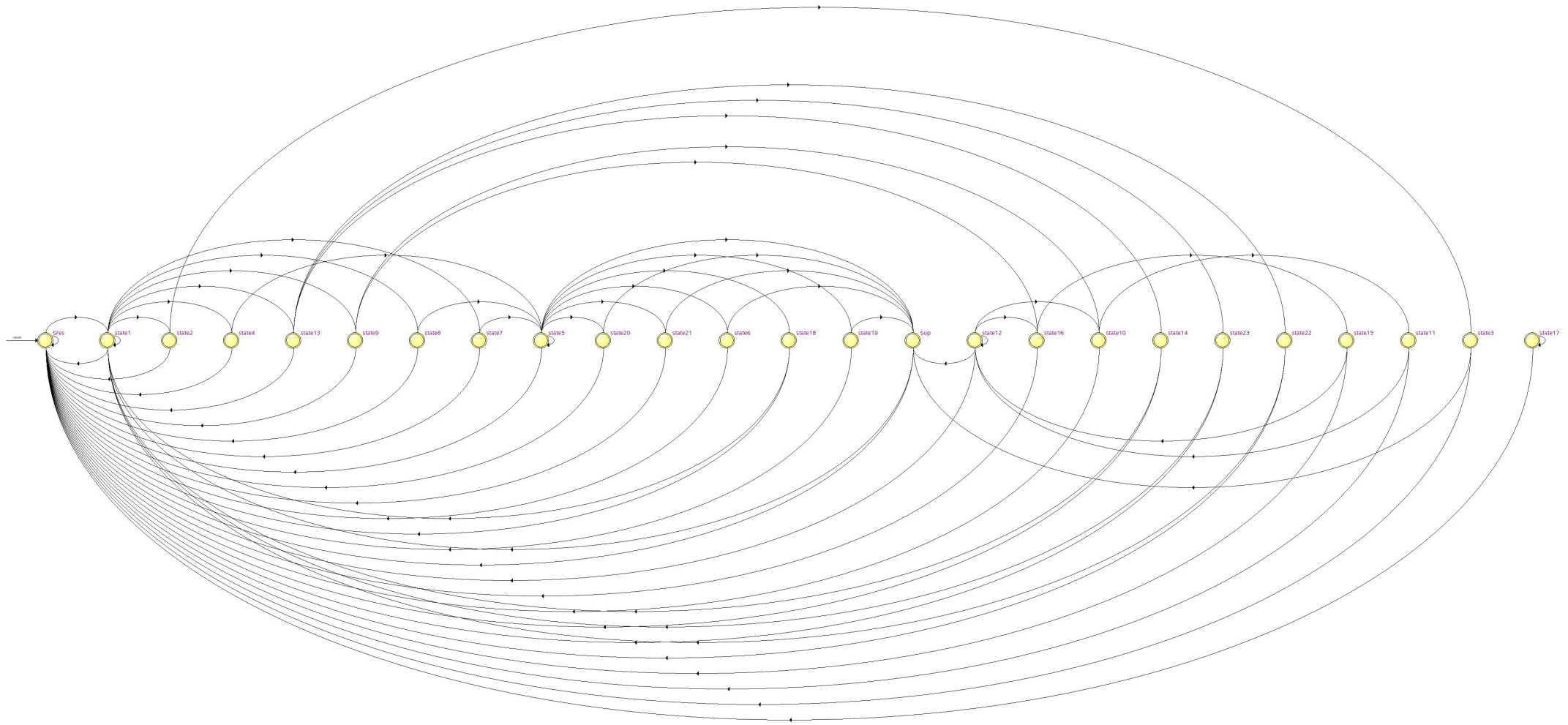
JLR

(S1) → (S13) → (S14)

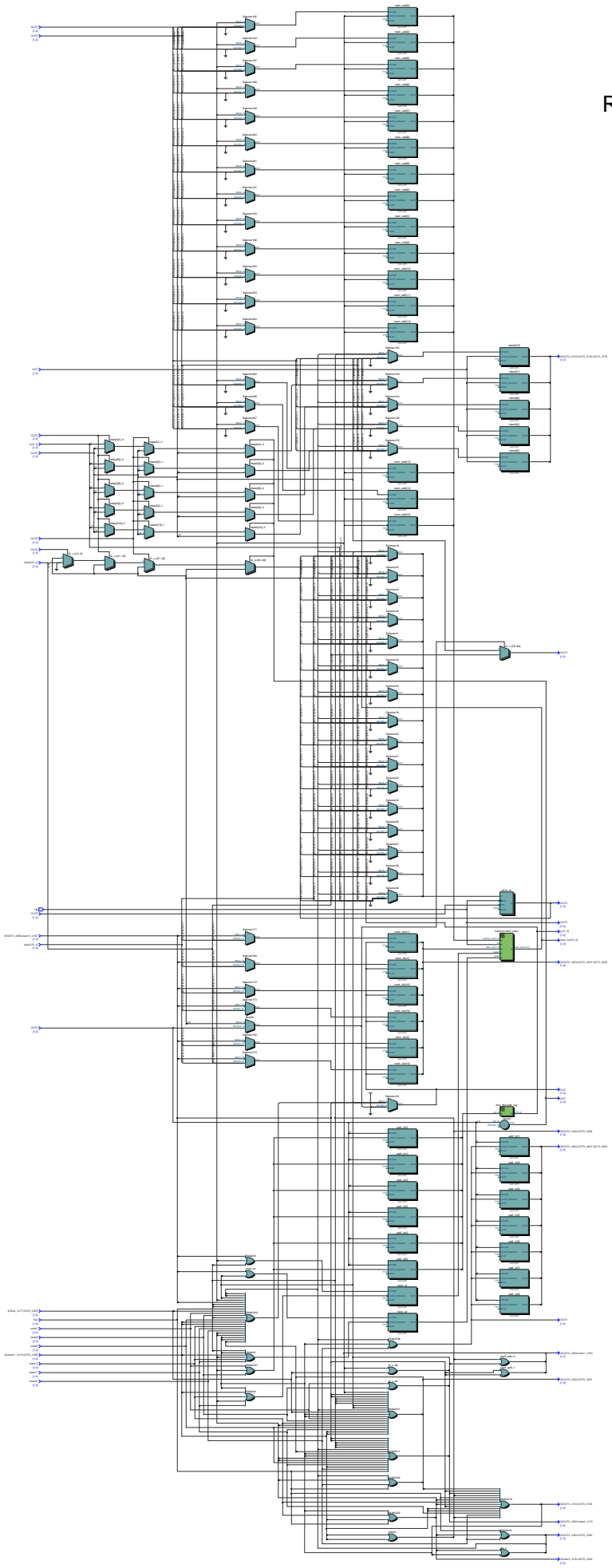
JRI

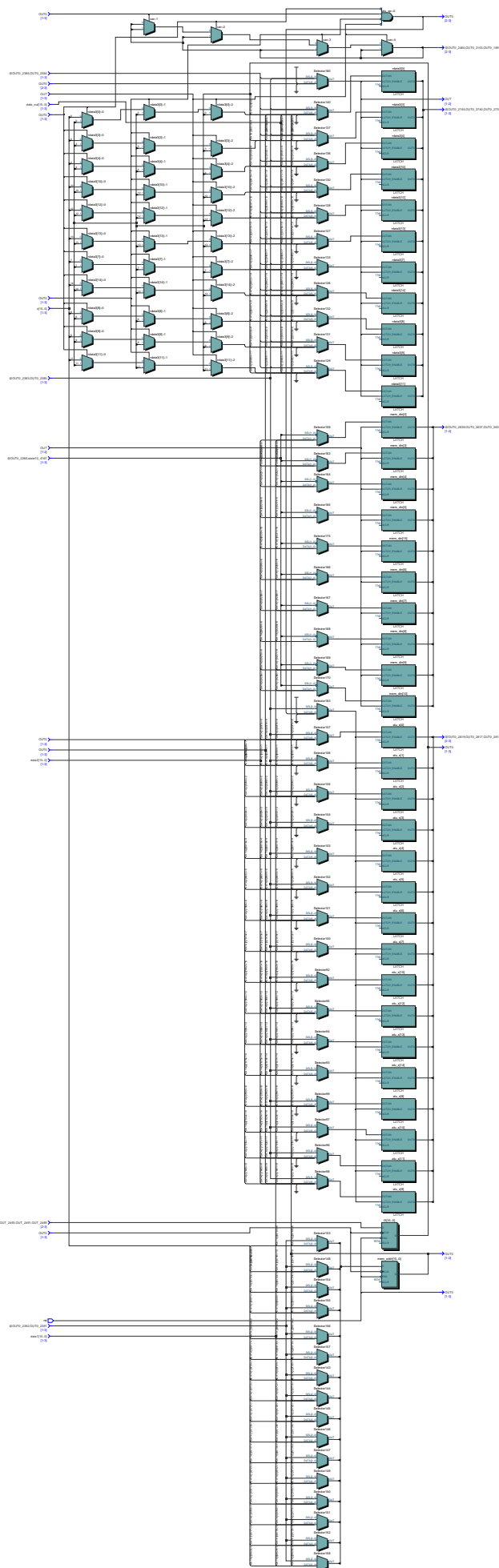
(S1) → (S13) → (S23)

State Machine View



RTL View 1





RTL View 2

RTL View 3

