EE2301: Lab Report 5

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1 Objective

To build a 5 bit Successive Approximation Register (SAR) Analog To Digital Converter (ADC).

2 Theory

2.1 Sample and Hold Circuit

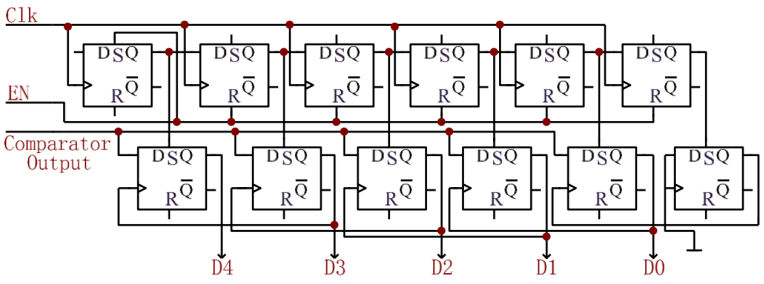
Sample and Hold (S/H) circuit samples the time varying input signal according to the clock input and holds the signal for a required amount of time. It consists of a Field Effect Transistor (FET) to which the clock signal is given as the gate voltage, so that it switches on and off accordingly. The signal is then used to charge a capacitor, which holds the signal for the required amount of time, as it discharges slowly. The resistances and capacitances have to be chosen accurately to achieve the optimal holding time.

2.2 Comparator

A comparator is used to figure out whether the approximated voltage value of the SAR register is greater or lesser than the input signal (output of the S/H circuit). In the next clock cycle, the value of the SAR register changes according to the comparator output.
If the input signal is lesser than the approximated value of the SAR register, the comparator outputs logical 0 (0 V), else it outputs logical 1 ($+V_{cc}$).

2.3 Successive Approximation Register (SAR)

A Successive Approximation Register is a register which gives the approximate binary representation of the input signal. It takes the comparator output and based off its value, adjusts its approximation. A typical SAR control circuit looks like this,



2.4 Digital to Analog Converter (DAC)

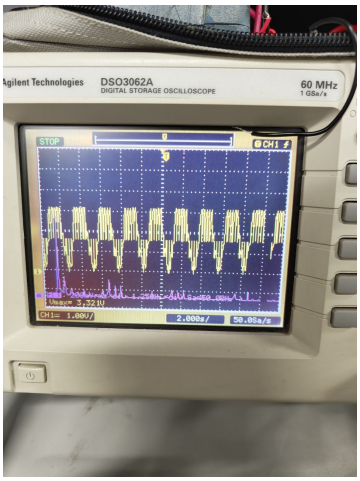
A Digital to Analog Converter (DAC) is a circuit which converts a digital signal into its analog equivalent signal. The output bits of the SAR (labelled D_4, D_3, D_2, D_1, D_0) are given as the inputs to the DAC, and it converts it into an analog voltage. R-2R is a typical DAC widely used. It has a ladder of resistances of values R and 2R, which are binarily weighted, which when added give the analog voltage output.

3 Working

The encode / preset signal is given to the SAR such that at the start of the first clock cycle, the MSB is HIGH and all the other bits are LOW. Then, this output of the SAR is given to the DAC, which compares it to the input signal sampled and held by the S/H circuit. According to the output of the DAC, the comparator gives an output. If the comparator output is HIGH, the next bit of the SAR is set to HIGH and the process continues. If the comparator output is LOW, the next bit is set to LOW, and the process continues. This cycle continues for 6 clock cycles here (since this is a 5 bit ADC). At the end of 6 clock cycles, the best 5 bit approximate of the input signal is given by the ADC circuit. After the 6 clock cycles, the encode signal is given. This process is continued.

4 Observations

The following is the output of the ADC for a 400 *mHz* sine signal.



5 Sources of Error

The impedences of the breadboard and of the wires caused the circuit to behave in an unintended manner sometimes. The repeated failure of the ICs caused a lot of delay in building the circuit. The 5 bit precision of the ADC might introduce some round-off errors, which deviate the output of the ADC from the original input signal.

6 Conclusion

A 5 bit SAR ADC was built successfully.